

IAYAA

LA-3391P REV 0.3 Schematic

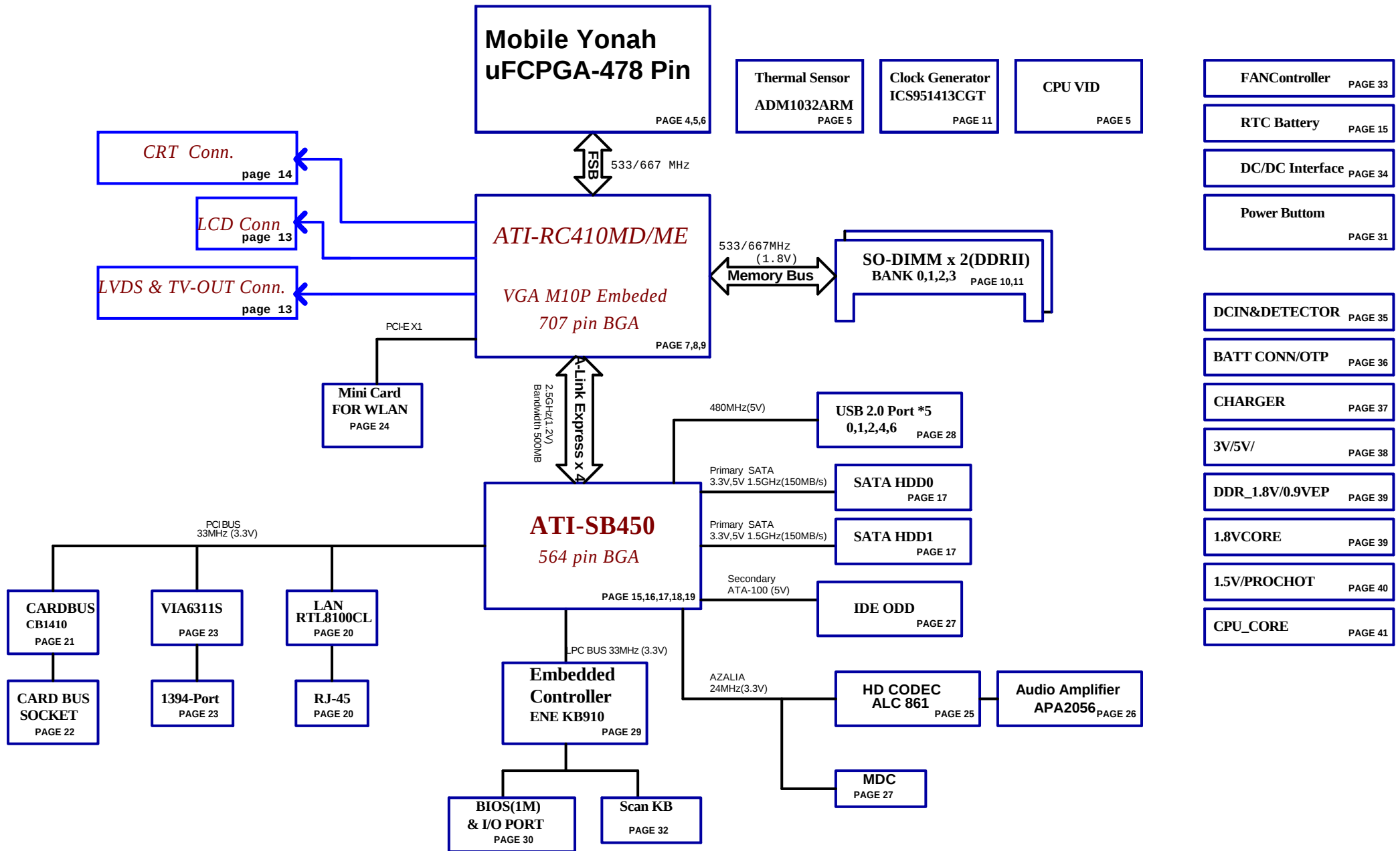
UFC-PGA Yonah/ RC410MD(ME)/ SB450

2006-10-05 Rev. 0.3

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Issued Date	2006/05/18	Deciphered Date	2007/05/18	Title Black Diagram	
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IVYAA LA-3391P FUNCTION BLOCK DIAGRAM



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPUVID	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+VGA_CORE	1.0V/1.2V switched power rail for VGA chip	ON	OFF	OFF
+1.2VS	1.2VS for PCI-Express	ON	OFF	OFF
+0.9VS	0.9V switched power rail	ON	OFF	OFF
+1.5VS	DOTHAN B	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8V	1.8V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
Card Bus	AD20	2	PIRQB
LAN	AD22	1	PIRQG
1394	AD16	0	PIRQA

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b

EC SM Bus2 address

SB450 SM Bus address

Device	Address
Clock Generator (ICS951413CGLFT)	1101 001Xb
DDR DIMM0	1010 0100b A4
DDR DIMM1	1010 0110b A6

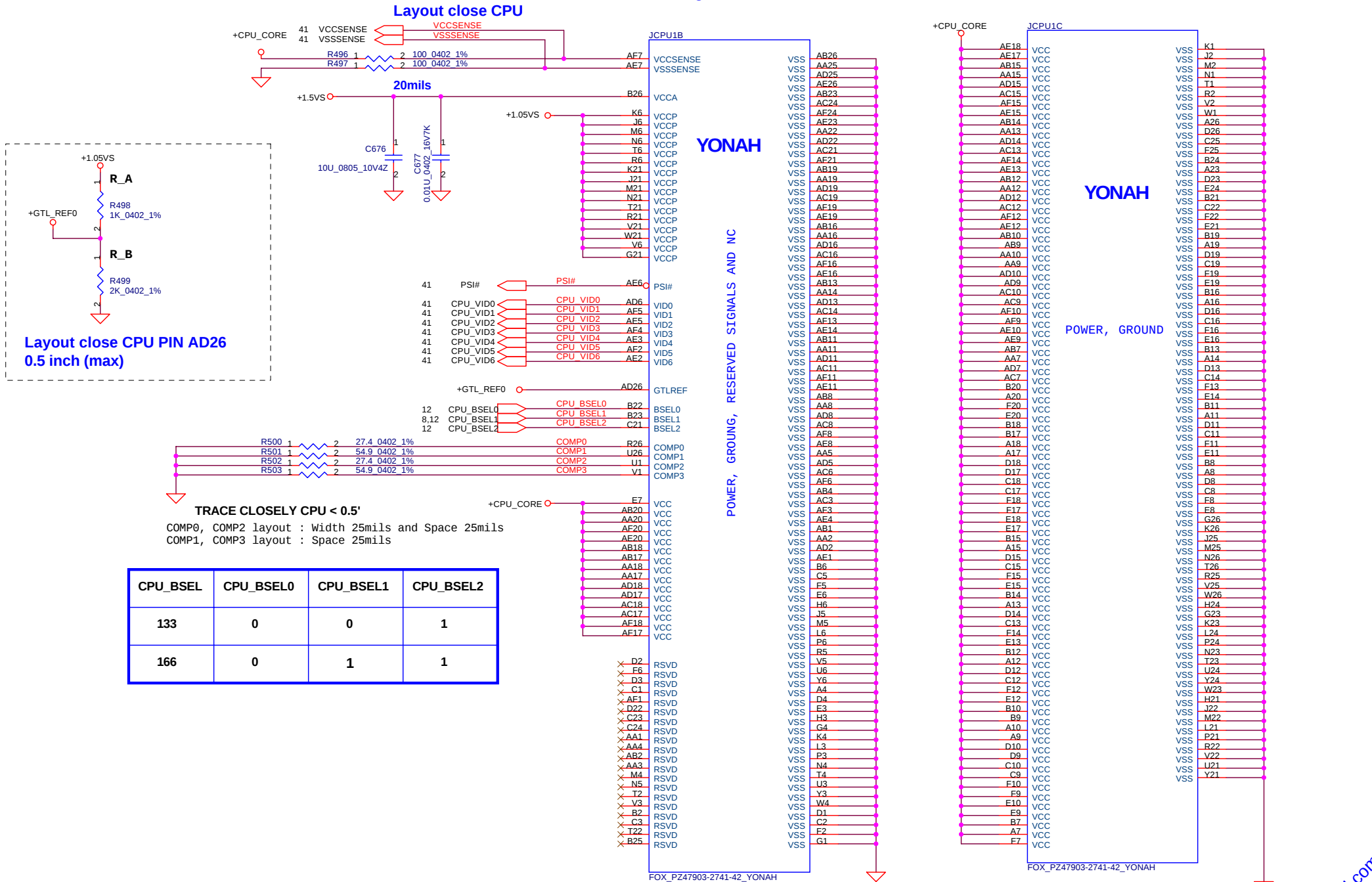
STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

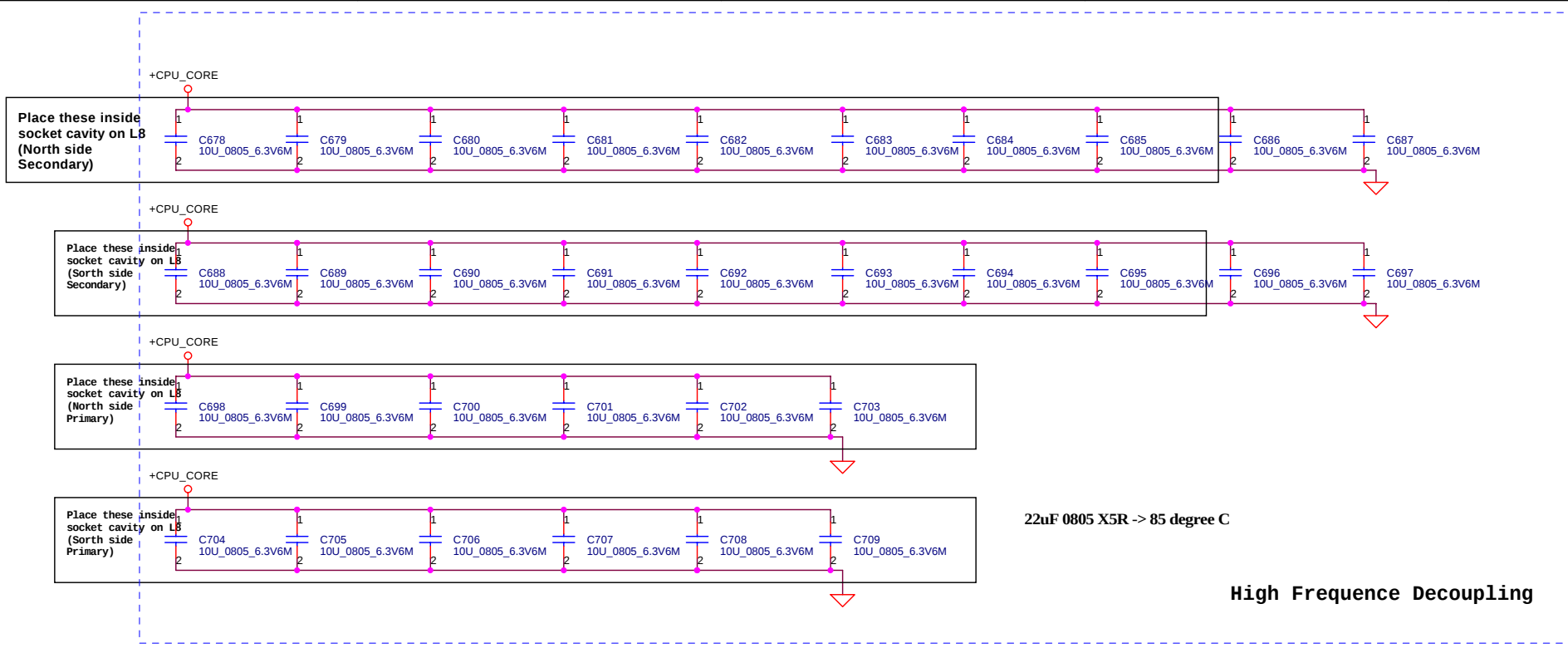
Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision	BTO	BOM STURCTURE
0	0.1	WIRELESS	WLAN@
1	0.2	1394	1394@
2	0.3	MIC	MIC@, 45 MIC@
3	1.0	Second HDD	2H@
4		NB Chipset	MD@, ME@
5		MDC	MDC@
6			
7			

SKU ID	BTN_ID	SKU_ID
0	1 Buttons	WW
1		
2		
3		
4	7 Buttons	JP
5		
6		
7		

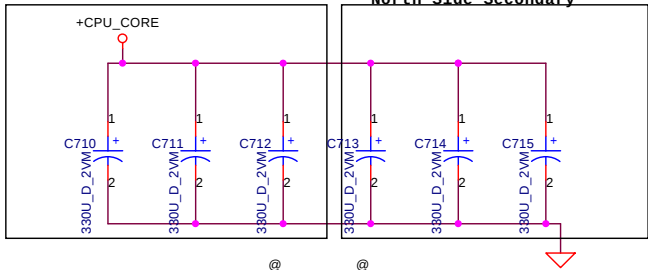




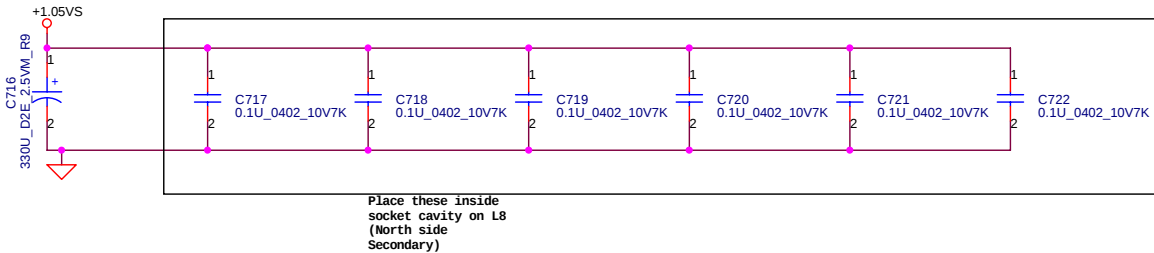
Near VCORE regulator.

South Side Secondary

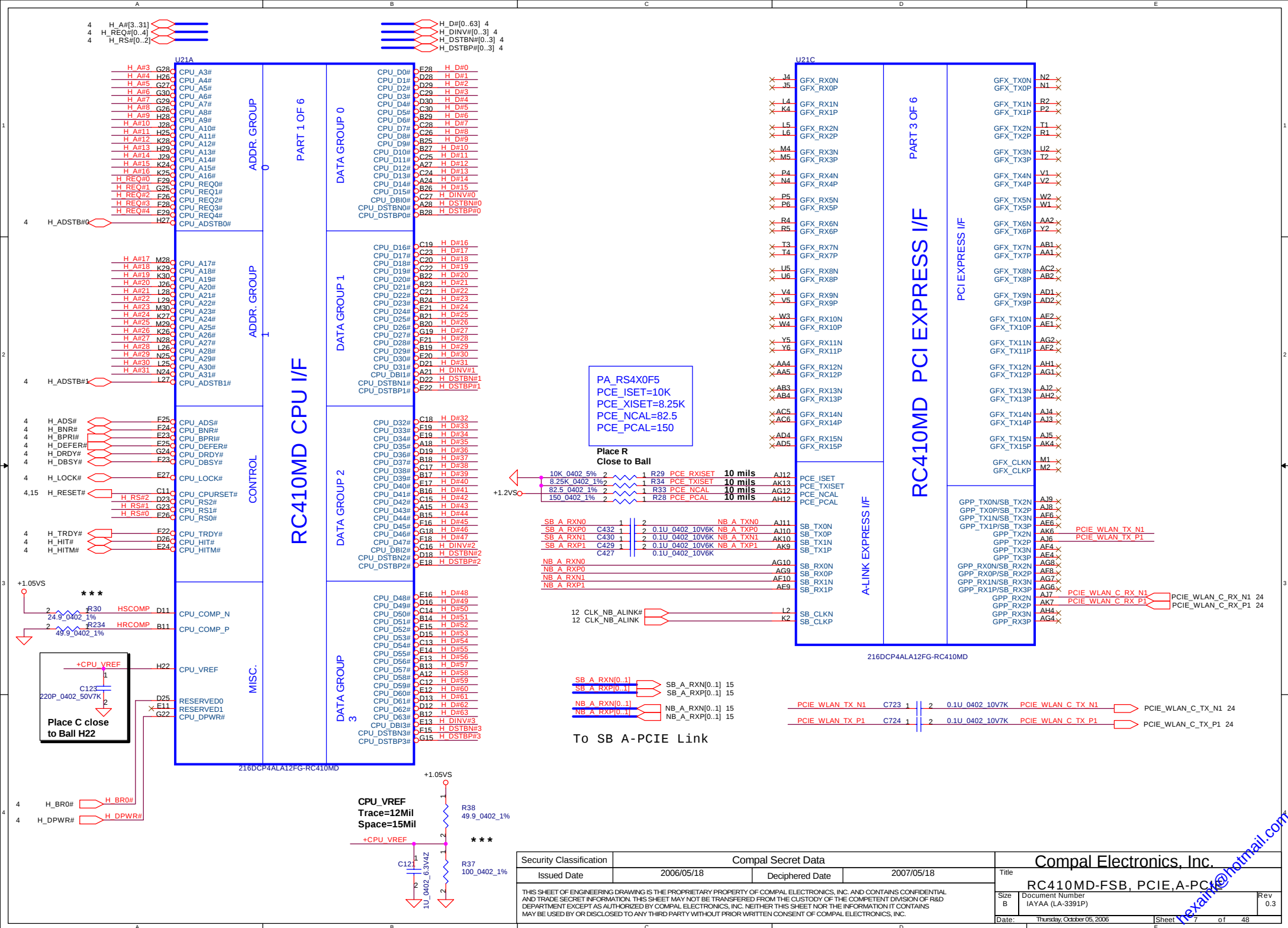
North Side Secondary

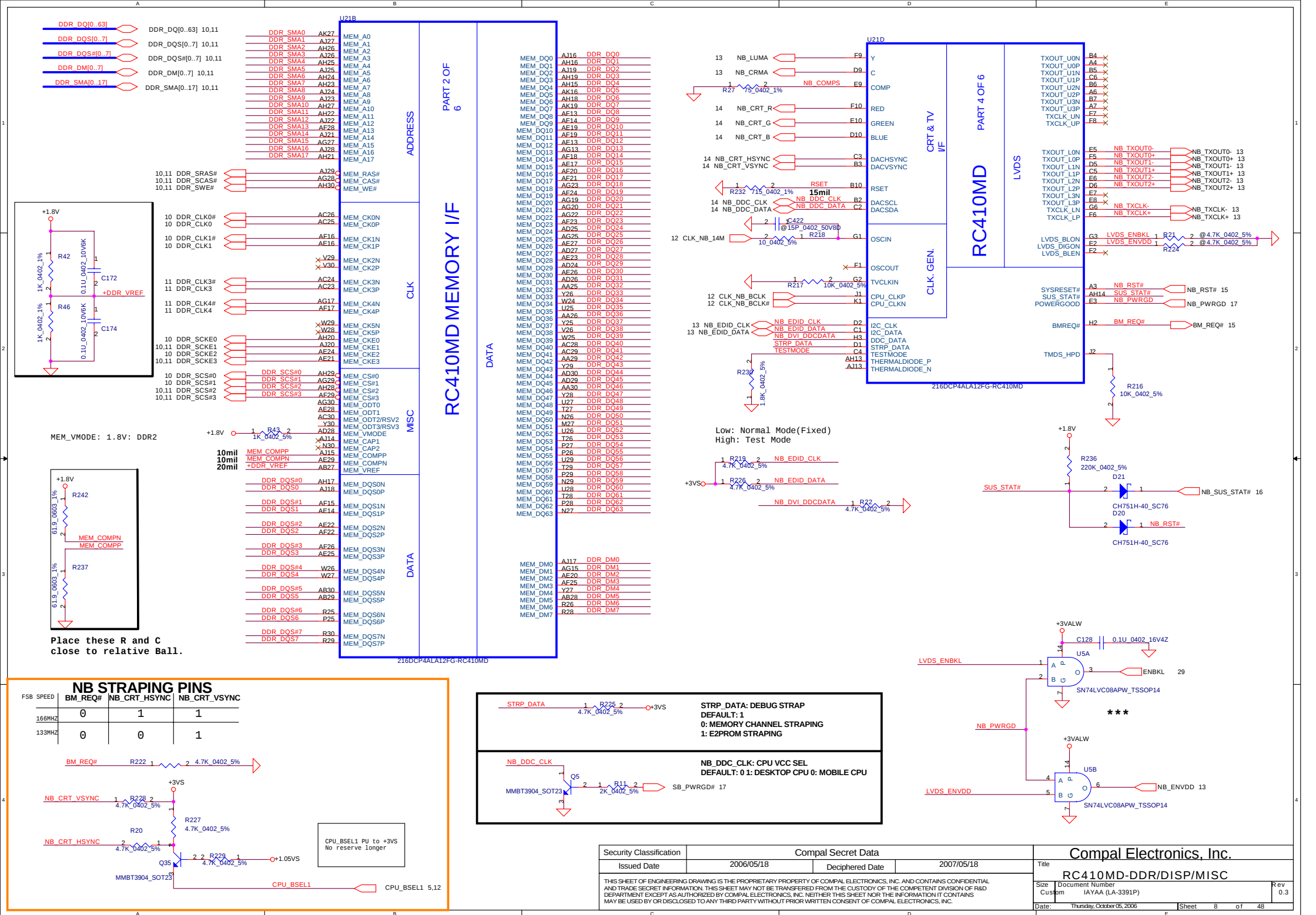


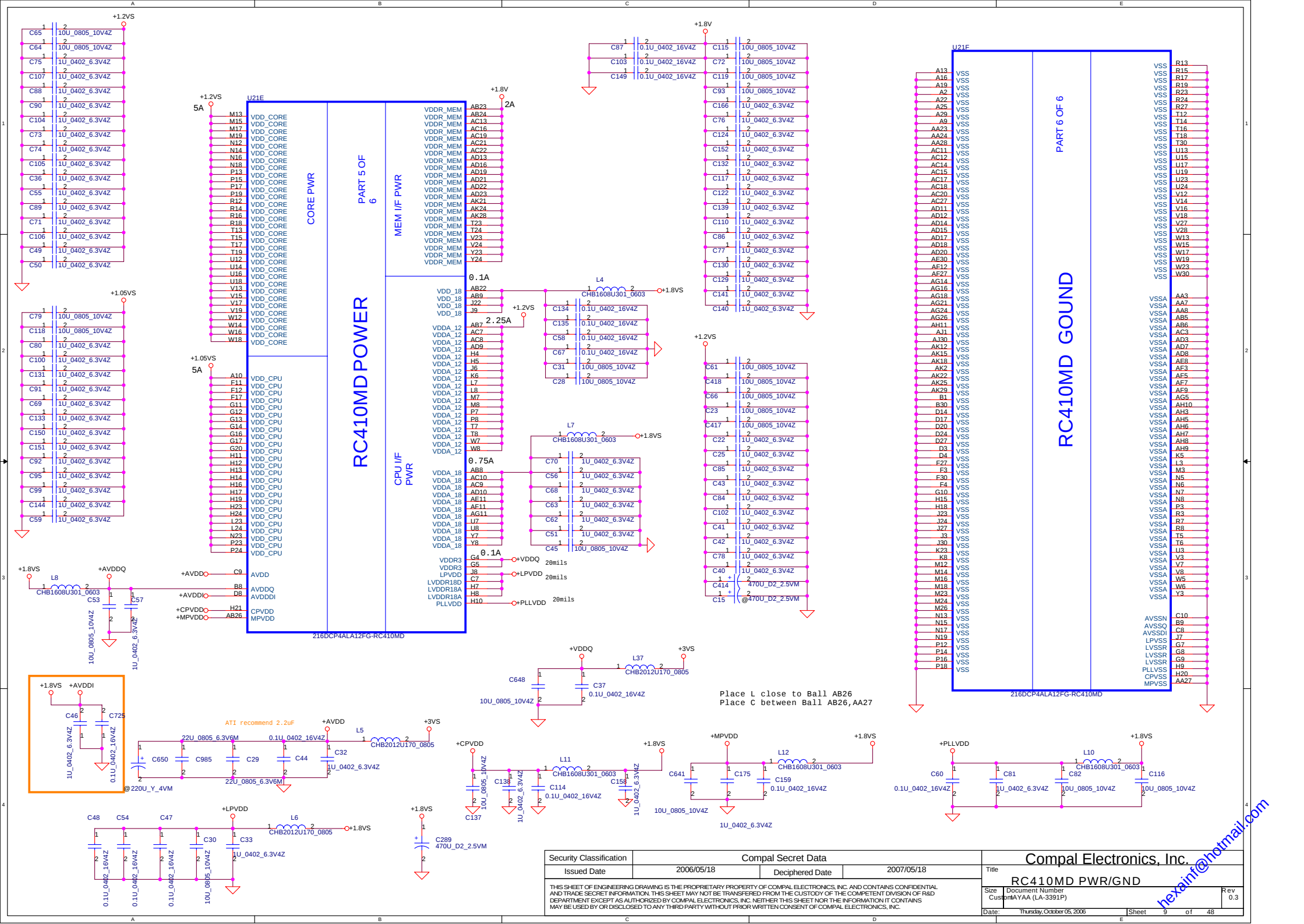
9mOhm 9mOhm 9mOhm 9mOhm 9mOhm 9mOhm
7343 7343 7343 7343 7343 7343
PS CAP PS CAP PS CAP PS CAP PS CAP PS CAP



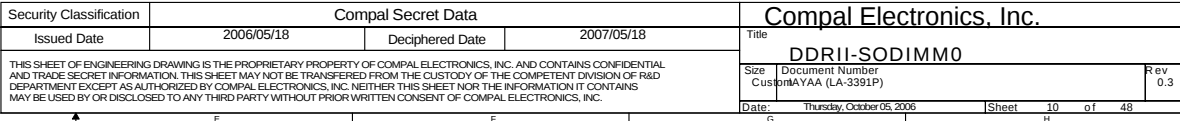
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Issued Date	2006/05/18	Deciphered Date	2007/05/18	Title	Yonah Bypass
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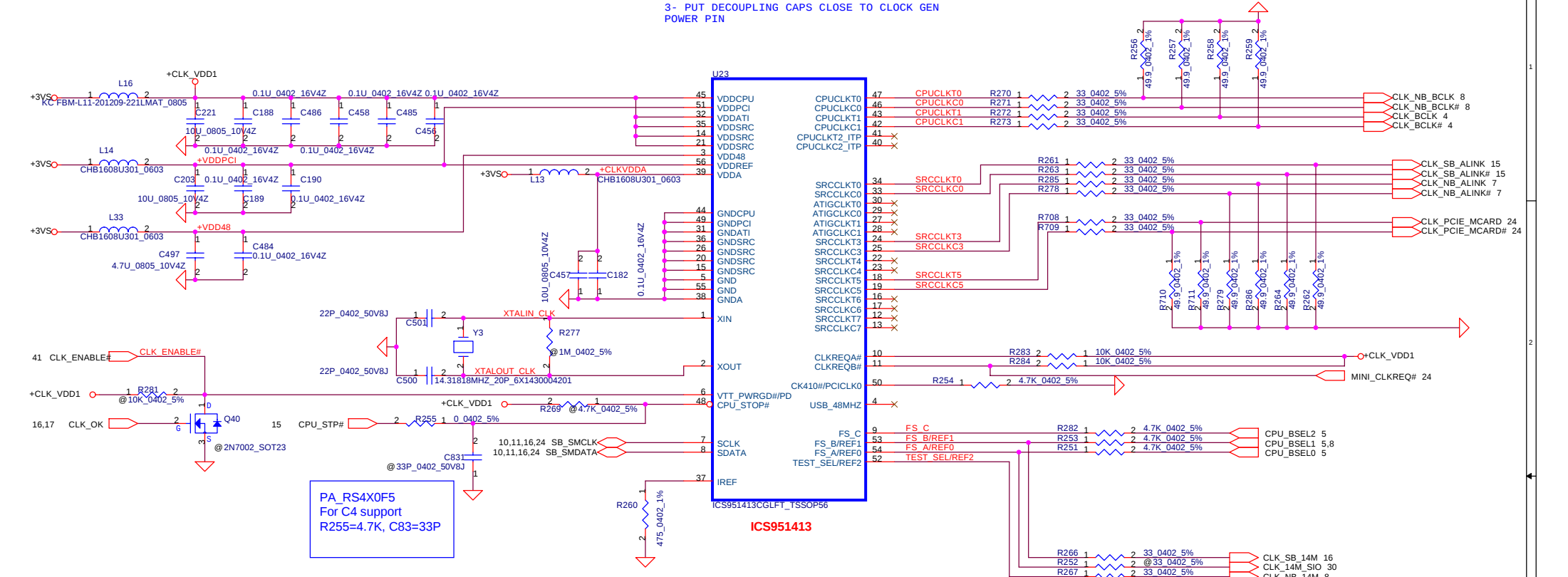


CS, Inc.	Rev 0.3
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Clock Generator

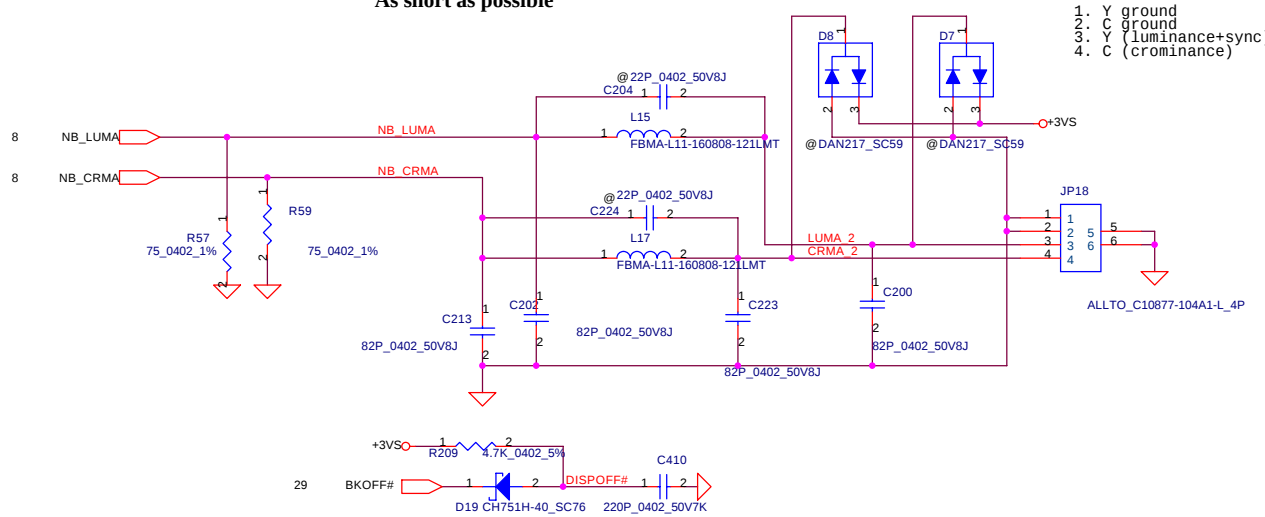
- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO CLOCK GEN AS POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBCLK/#, ITPCLK/# AND SCR/# ,AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO CLOCK GEN POWER PIN



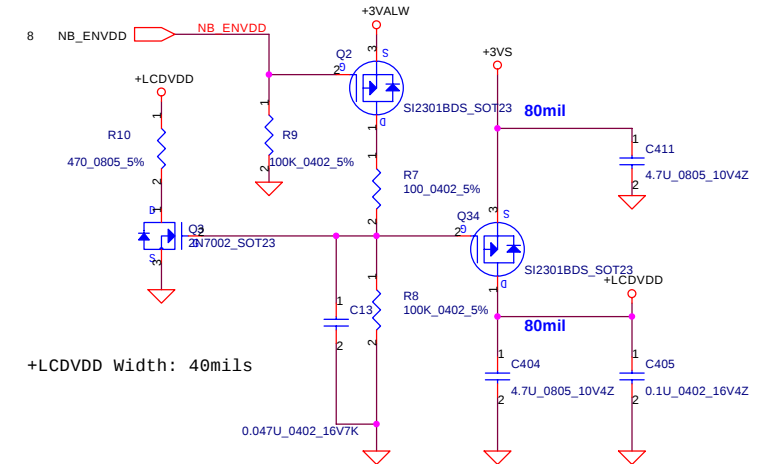
FS_C	FS_B	FS_A	CPU	SRC	PCI	REF	USB
1	0	1	100.00	100.00	33.33	14.318	48.000
0	0	1	133.33	100.00	33.33	14.318	48.000
0	1	1	166.66	100.00	33.33	14.318	48.000

TV-OUT CONNECTOR

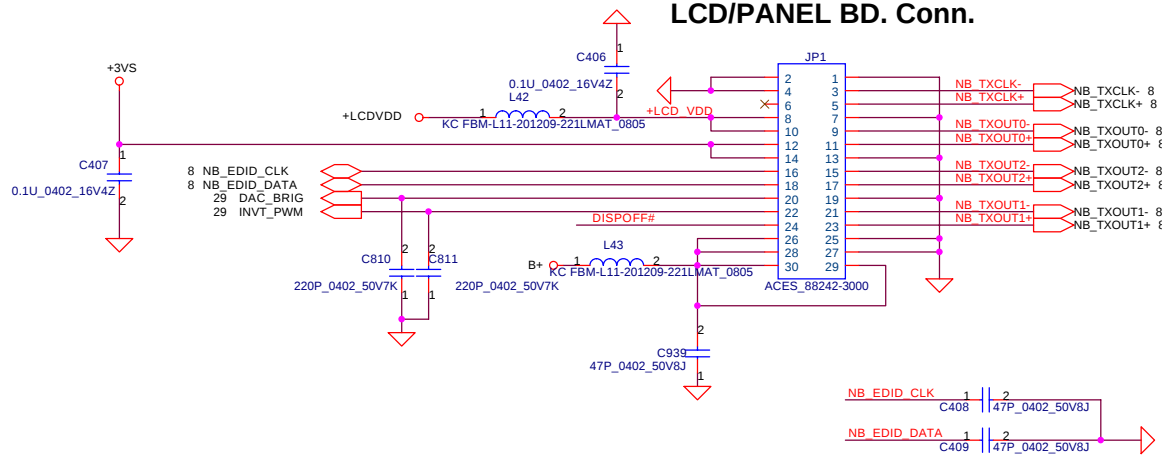
Reduce LUMA_1 and CRMA_1 length
As short as possible



PANEL +LCDVDD CTRL CKT

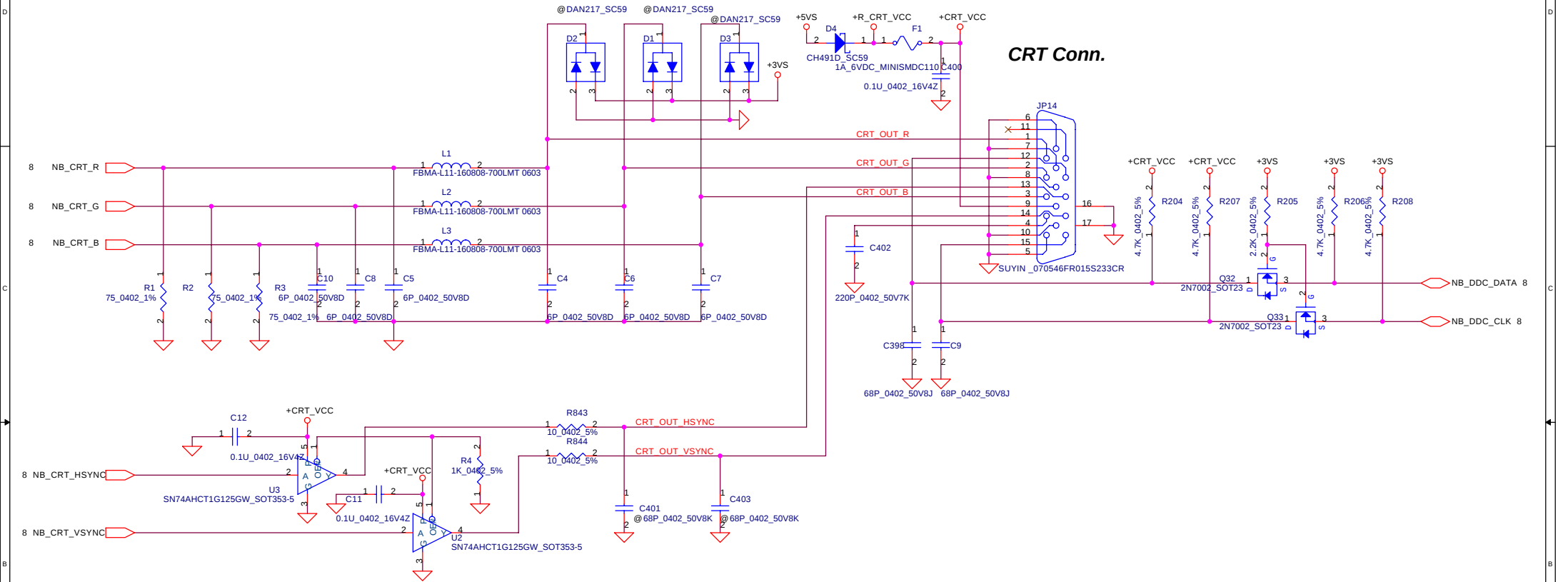


LCD/PANEL BD. Conn.

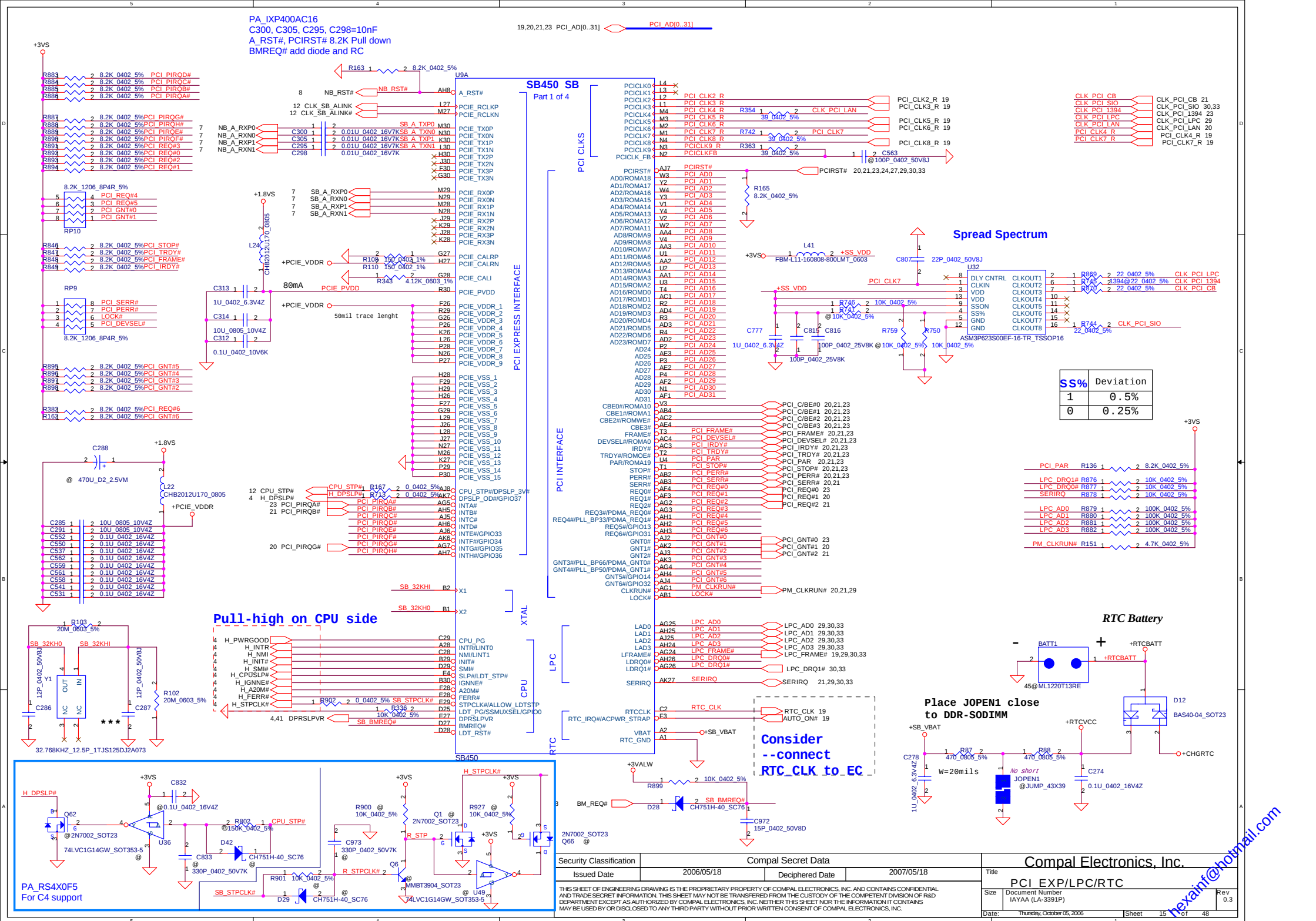


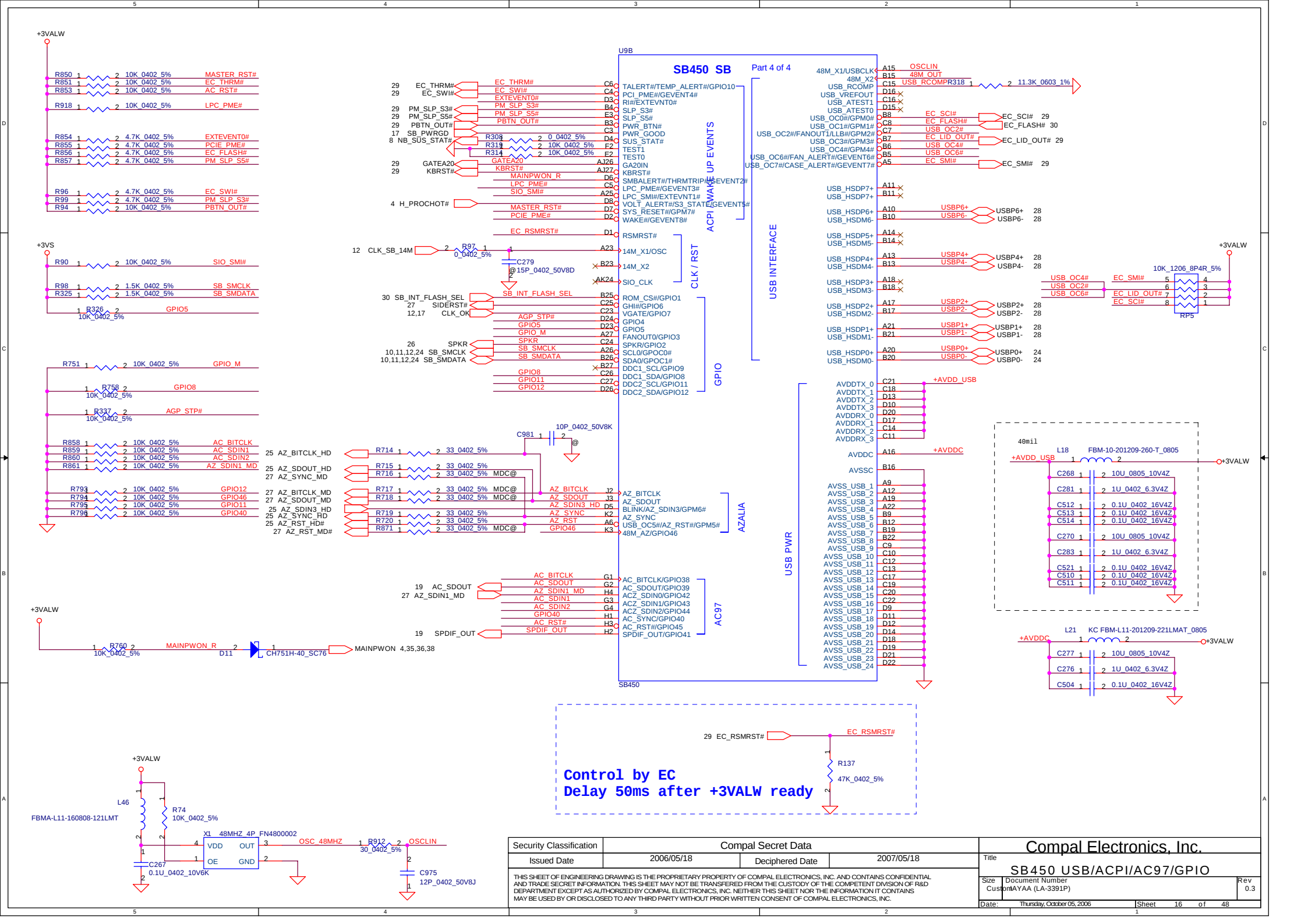
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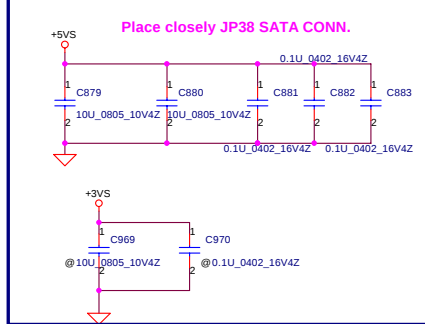
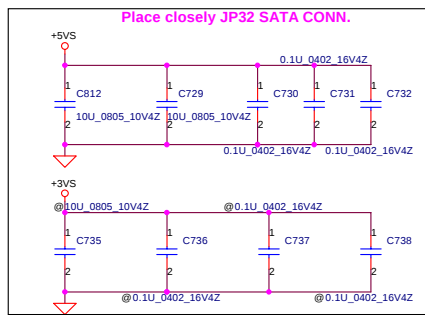
CRT CONNECTOR



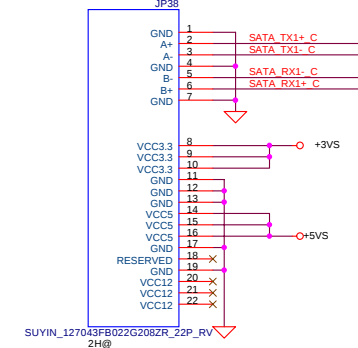
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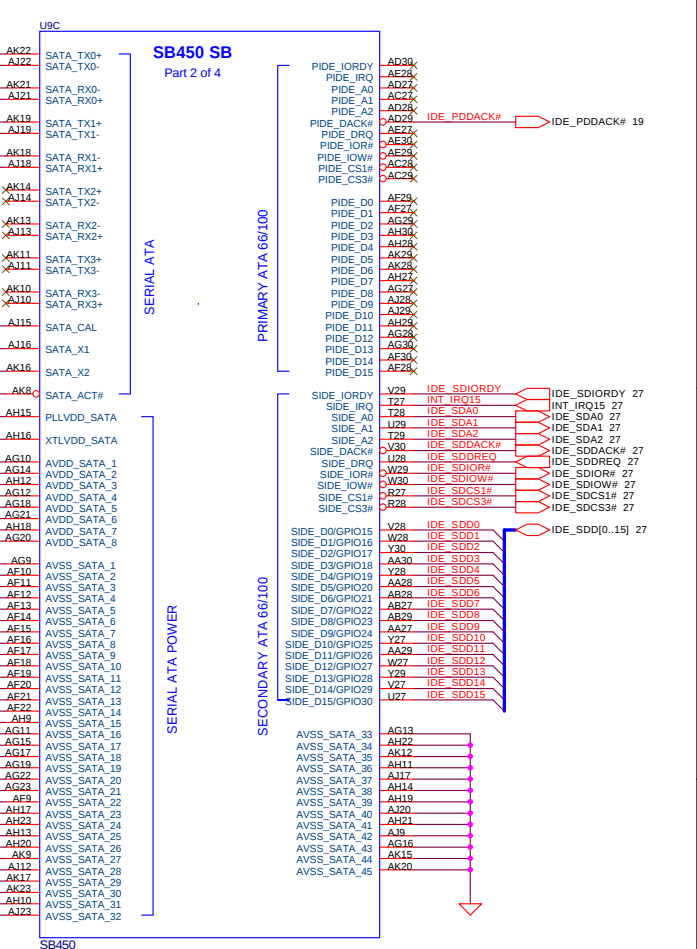
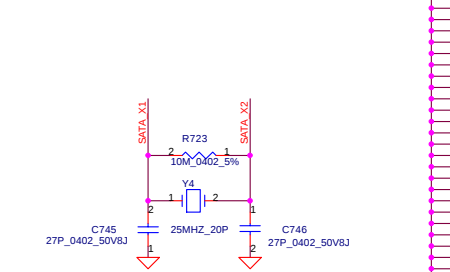
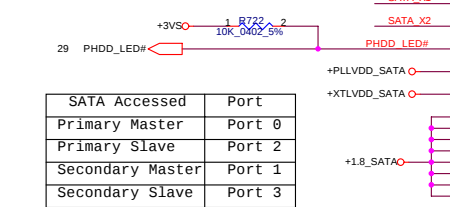
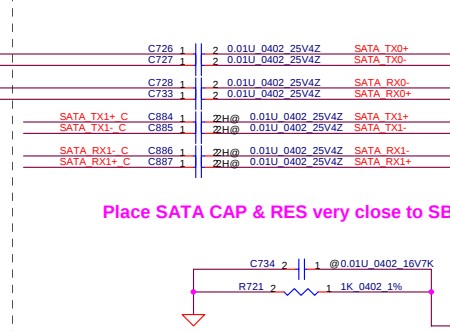




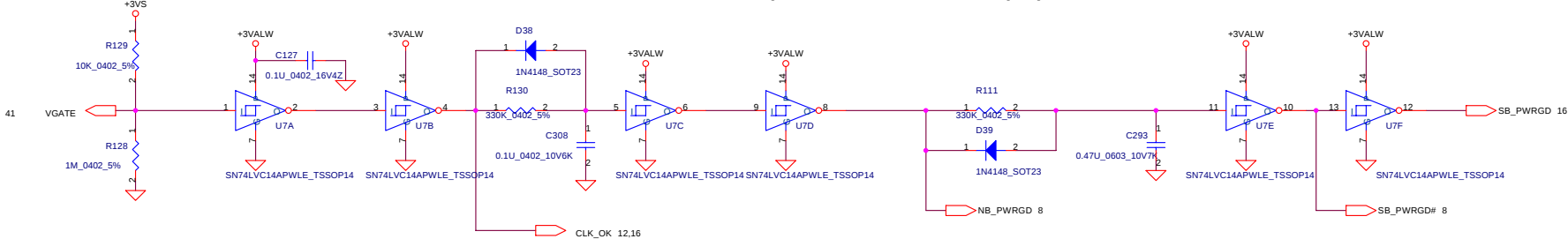
SATA HDD CONNECTOR

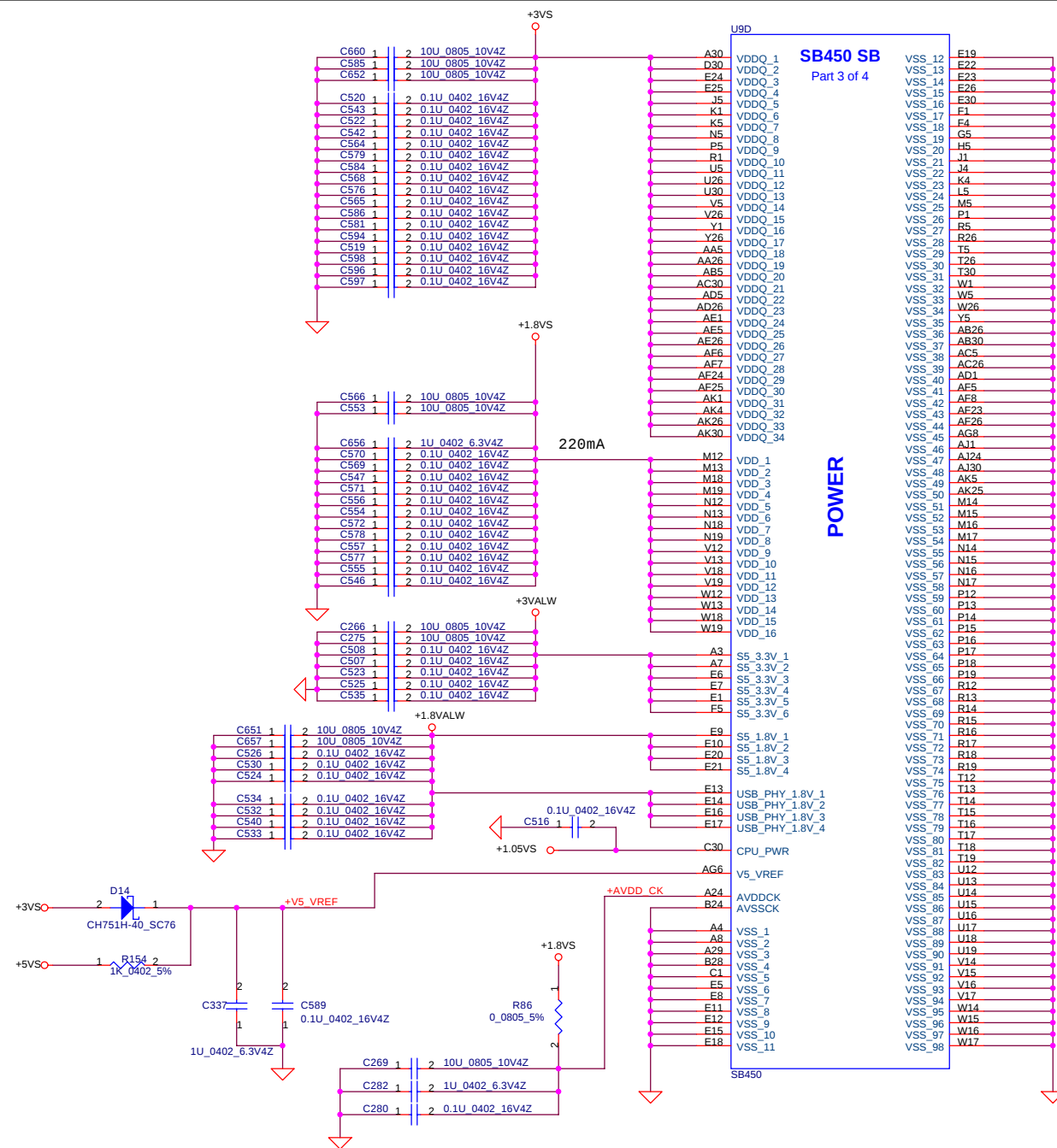


SATA HDD CONNECTOR



U7-->please close to SB450(U9)

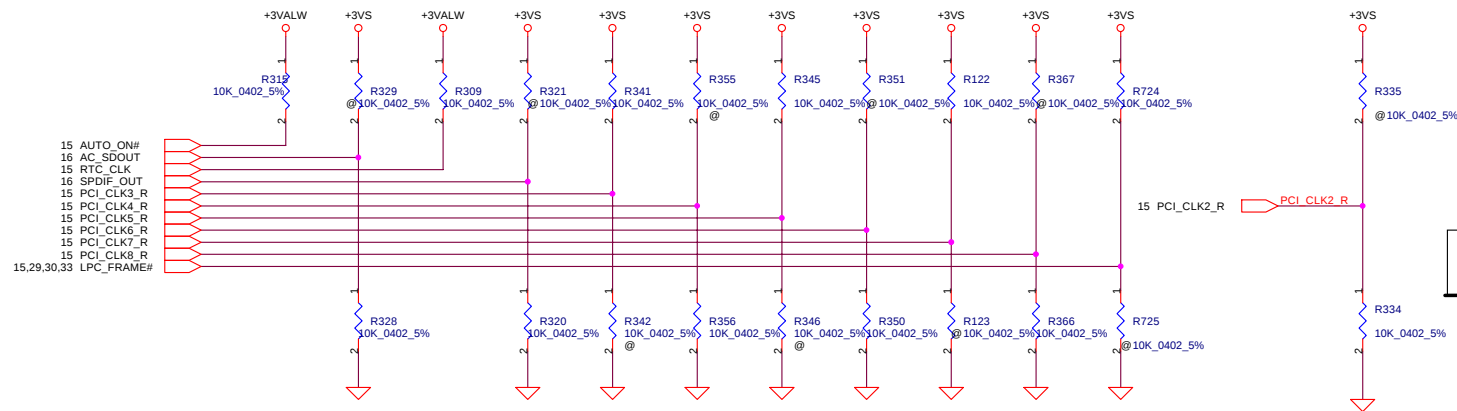




SB450 SB
Part 3 of 4

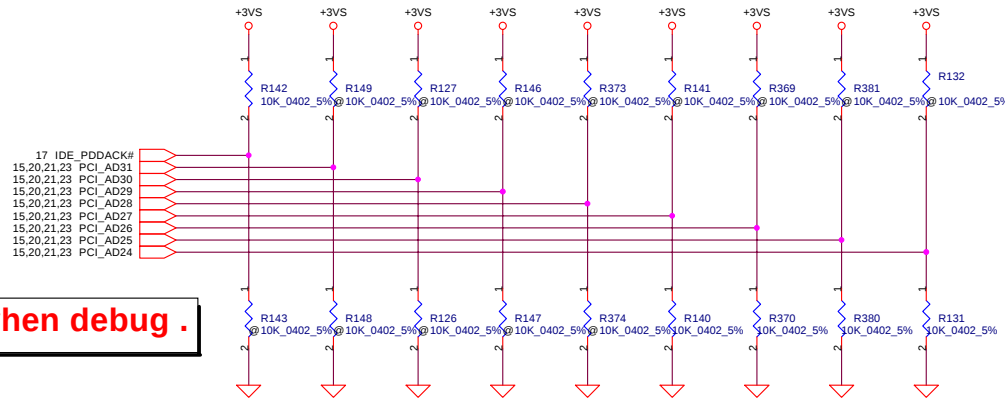
POWER

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REQUIRED STRAPS

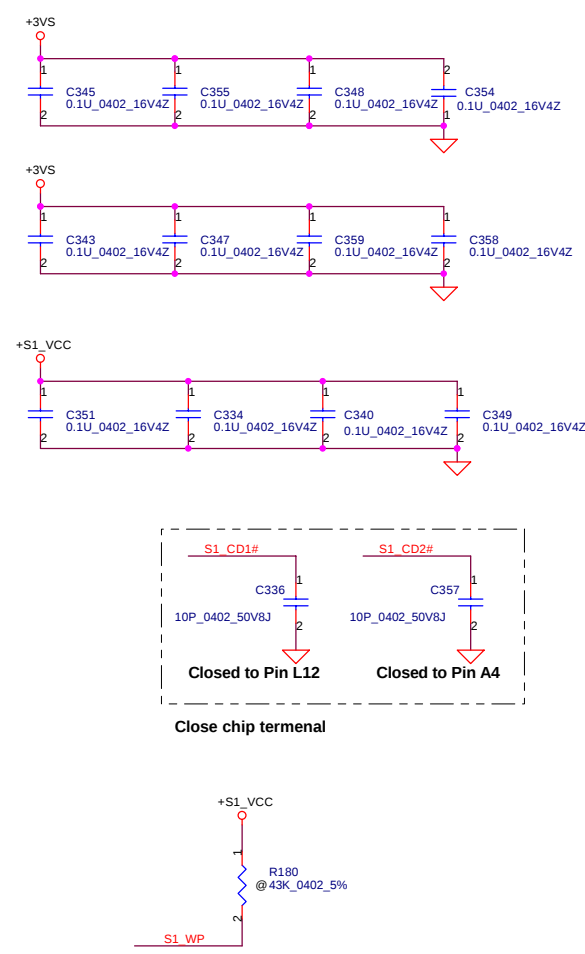
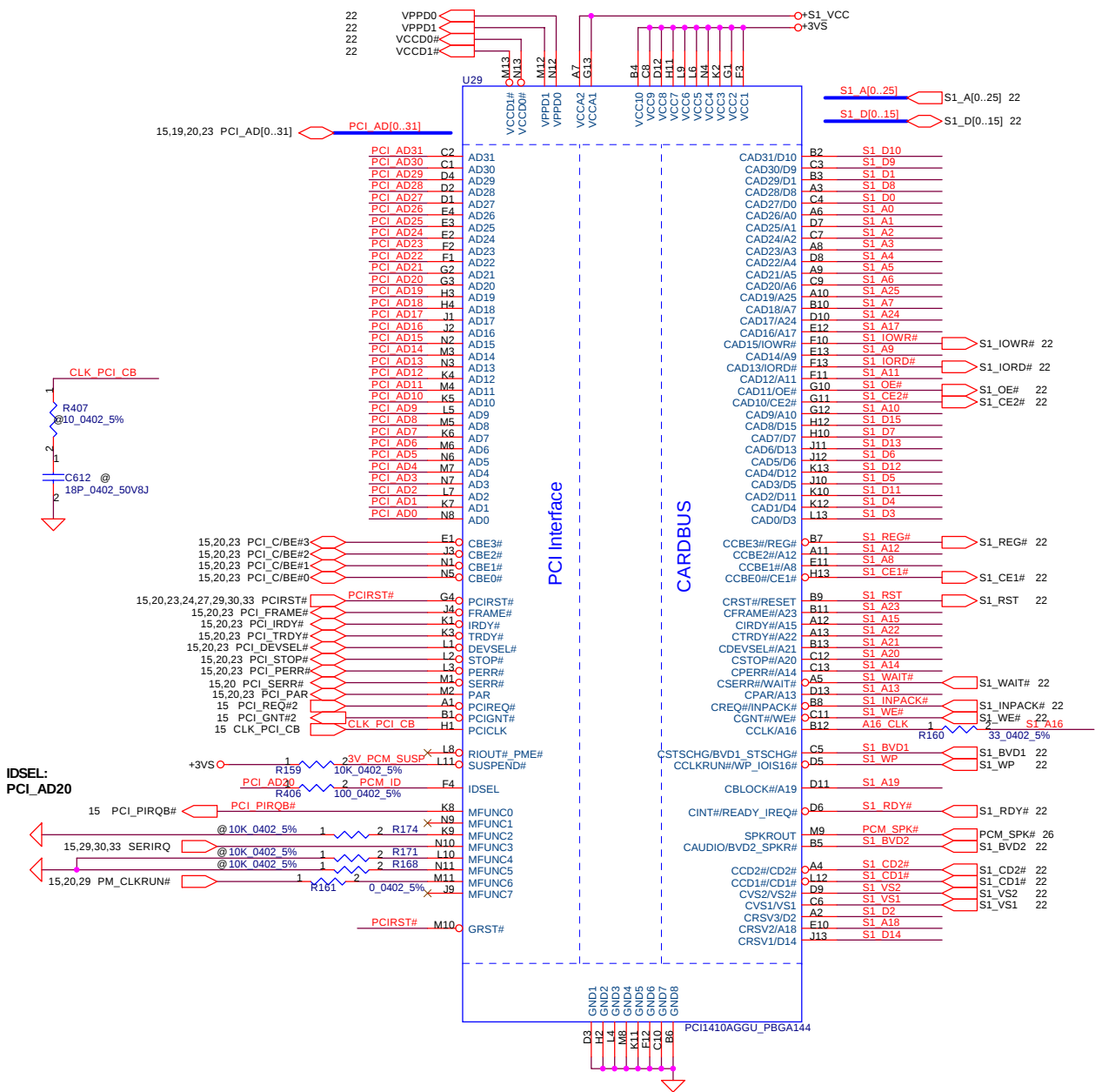
	AUTO_ON#	AC97_SDOUT	RTC_CLK	SPDIF_OUT	CLK_PCI3	CLK_PCI_LAN	CLK_PCI_LPC	PCI_CLK6	PCI_CLK7	PCI_CLK8	PCI_CLK2_R	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHZ	USB PHY PWRDOWN DISABLE	Internal PLL	PCIE CM_SET low DEFAULT	CPU I/F = K8 DEFAULT	ROM TYPE H,H = PCI ROM H,L = LPC ROM I		Crytsal Pad	THERMTIP# ENABLE
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHZ DEFAULT	USB PHY PWRDOWN ENABLE DEFAULT	External Clock DEFAULT	PCIE CM_SET HIGH	CPU I/F = P4 DEFAULT	L,H = LPC ROM II L,L = FWH ROM		Clock input buffer DEFAULT	THERMTIP# DISENABLE



DEBUG STRAPS

	IDE_PDDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24
PULL HIGH	USE LONG RESET DEFAULT	Reserved	Reserved	Reserved	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT

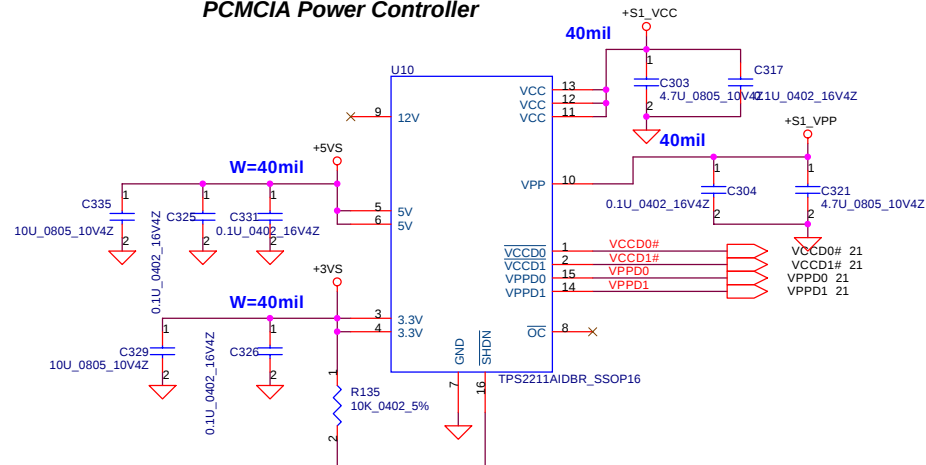
AD23 strapping
No reserve longer



IDSEL:
PCI_AD20

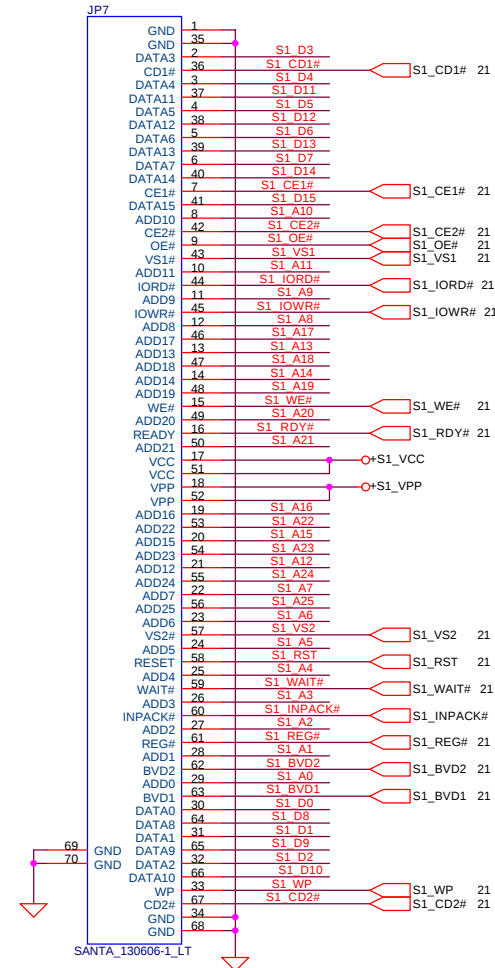
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PCMCIA Power Controller



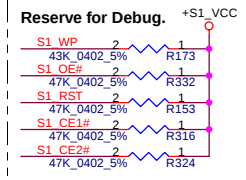
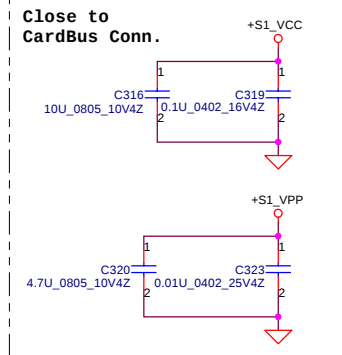
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21 S1_D[0..15] S1 D[0..15]

CardBus Socket

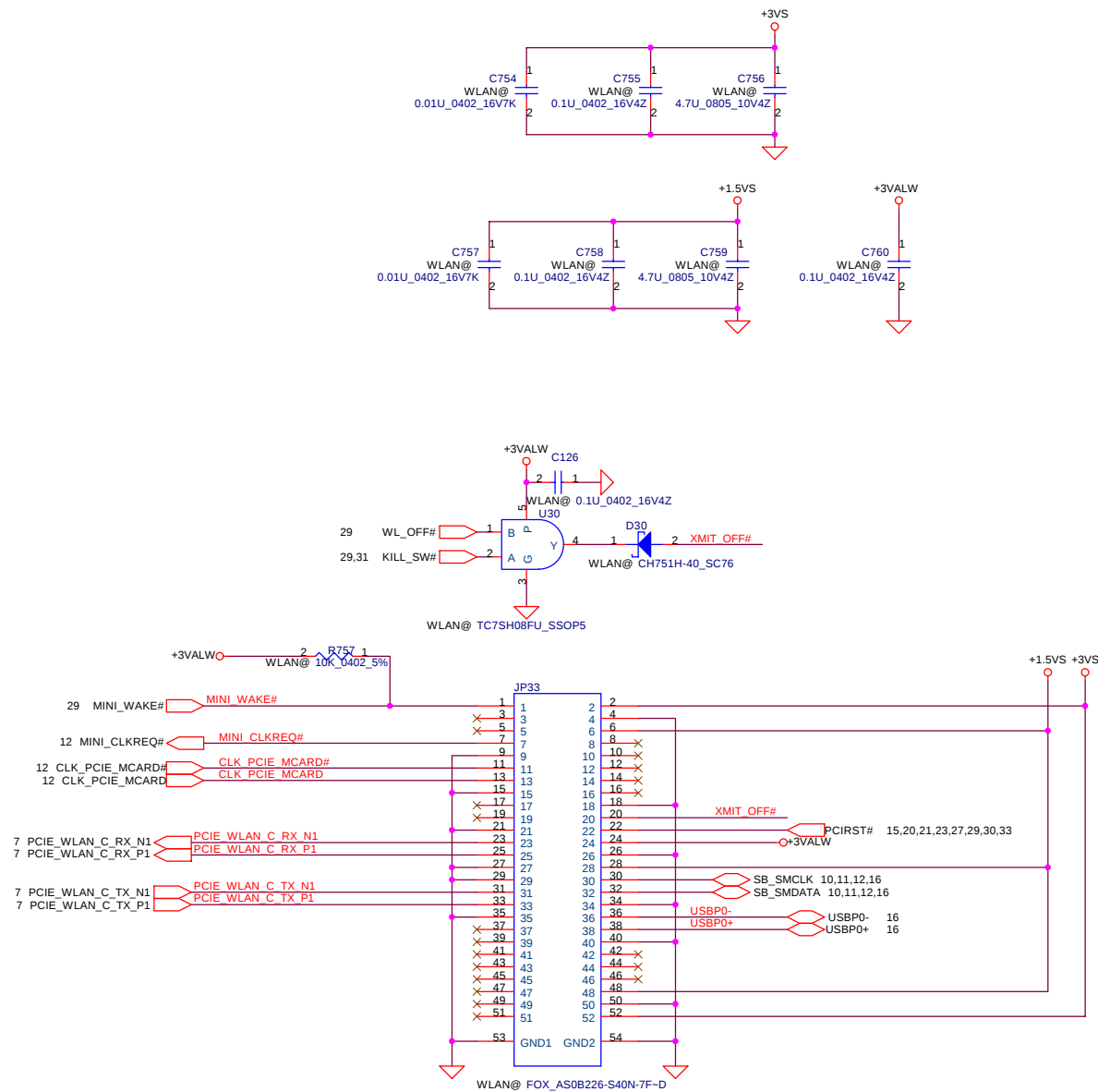


CardBus Socket

21 S1_A[0..25] S1 A[0..25]
21 S1_D[0..15] S1 D[0..15]



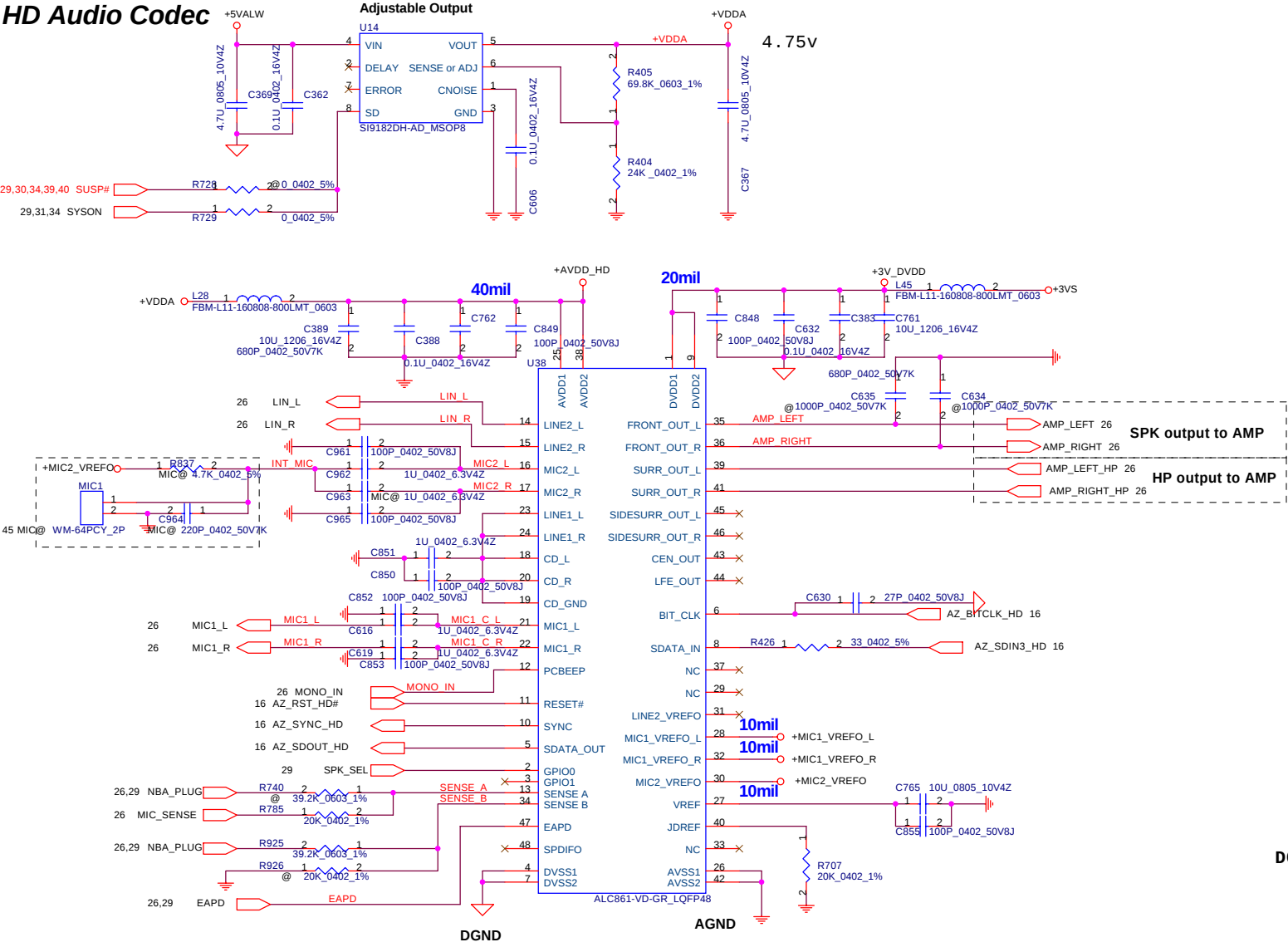
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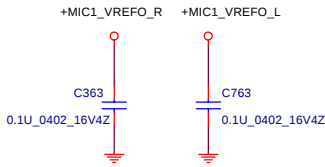
Mini-Express Card

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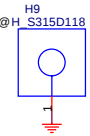
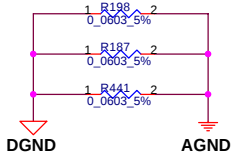
HD Audio Codec



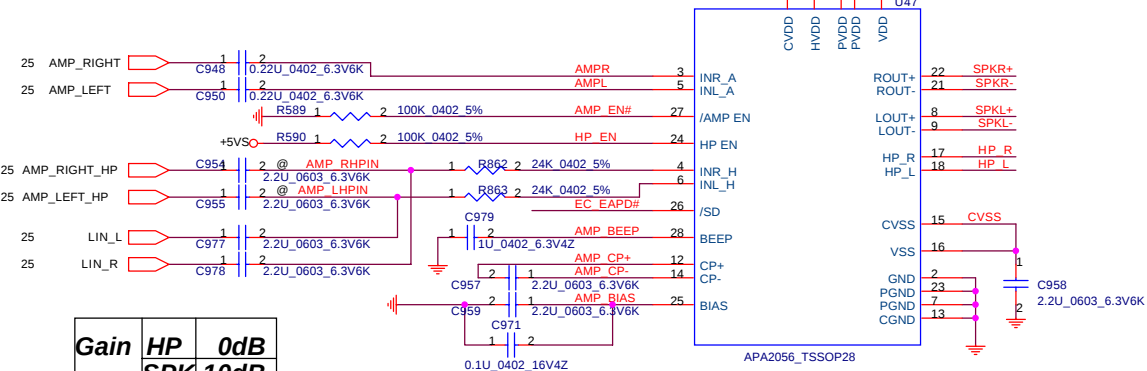
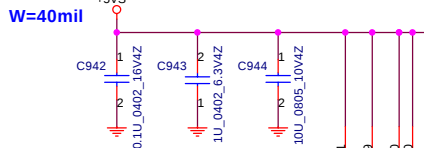
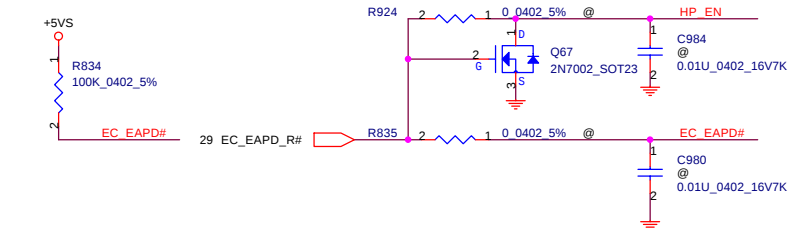
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	5.1K	PORT-H (PIN 45, 46)
	20K	PORT-F (PIN 16, 17)



DGND To AGND Bypass



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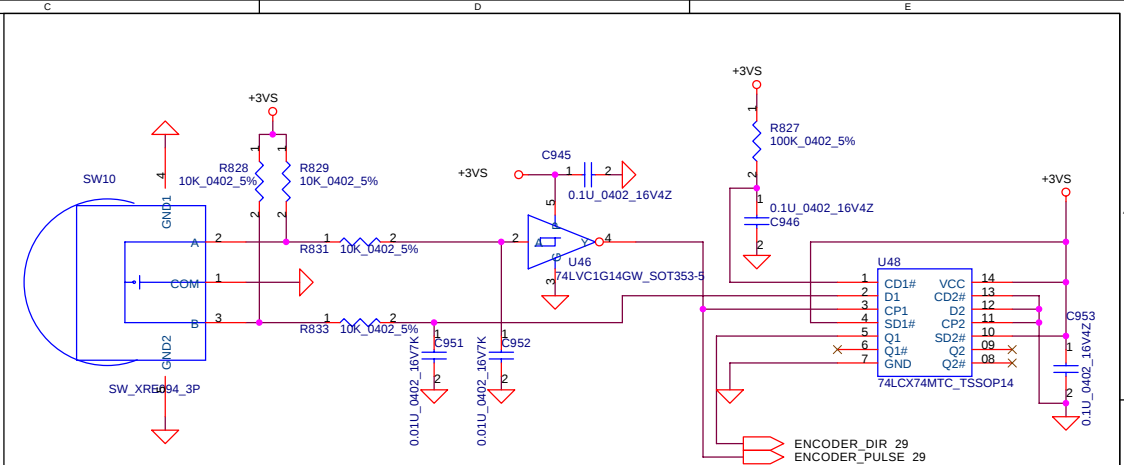
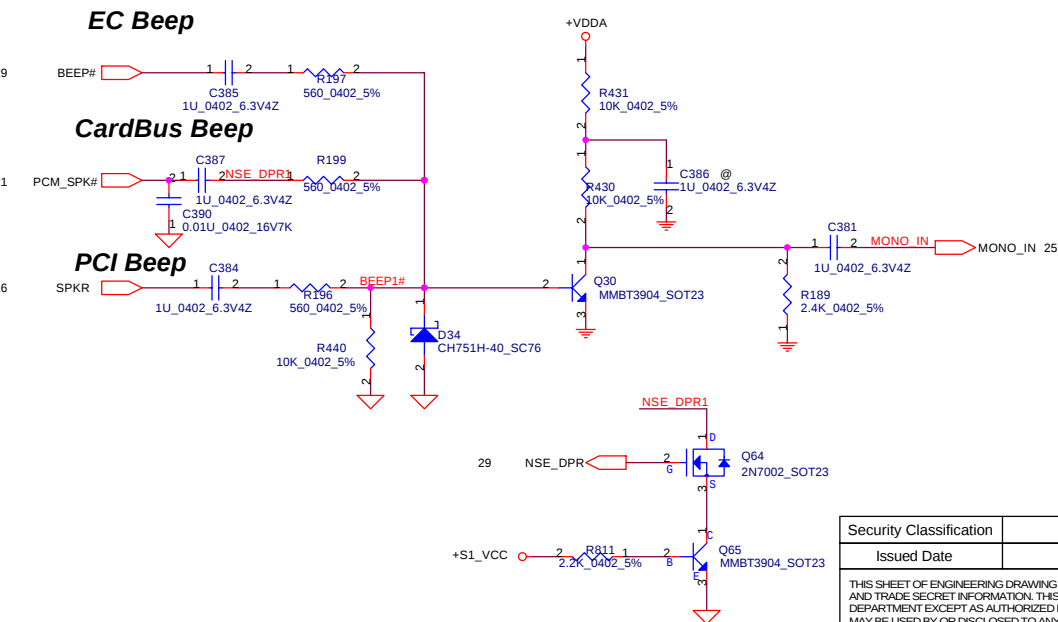


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	SPK	10dB

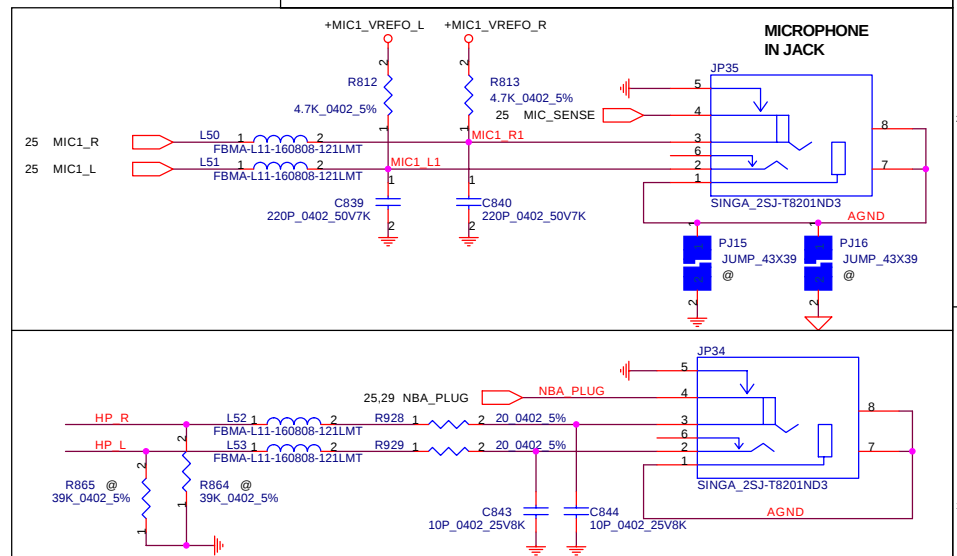
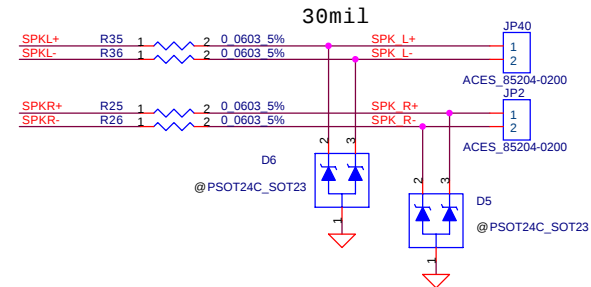
EC Beep

CardBus Beep

PCI Beep

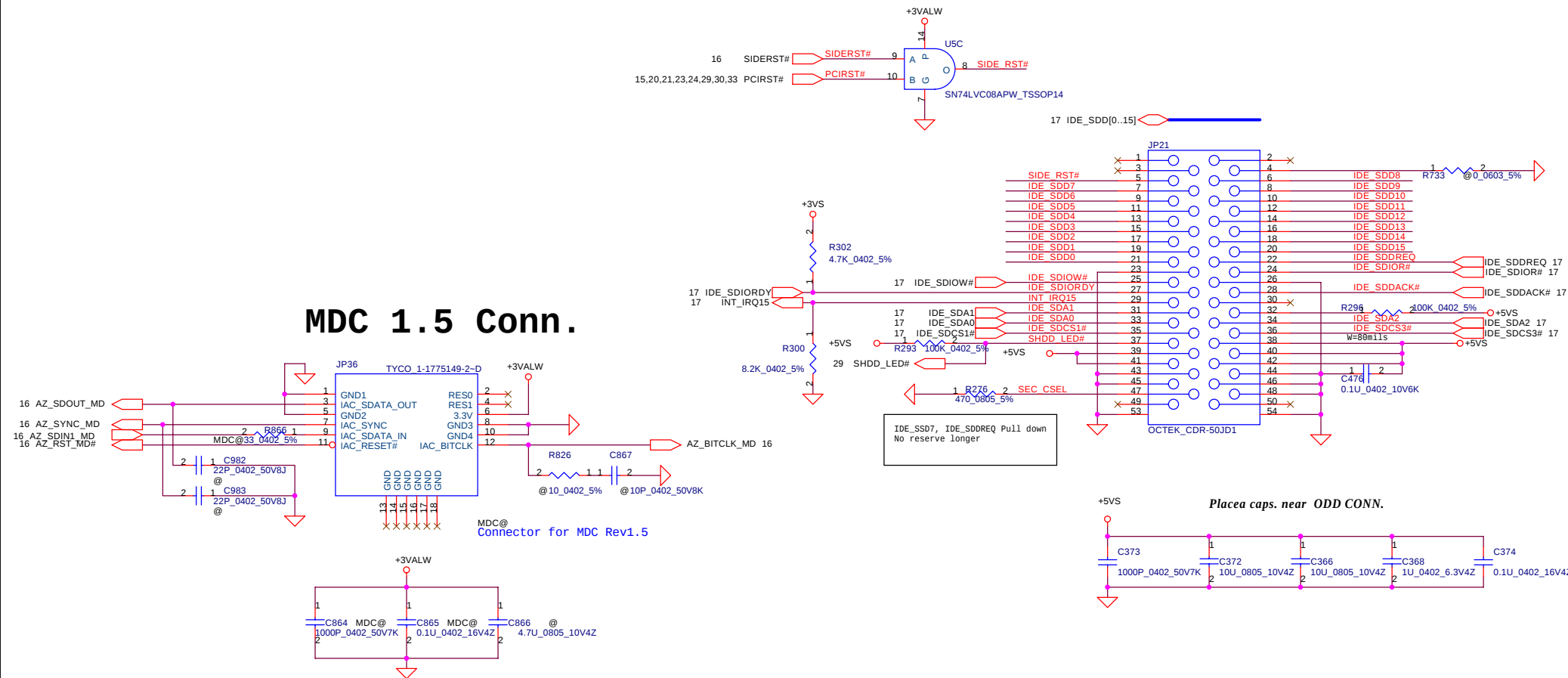


Speaker Conn.



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2006/05/18				2007/05/18				AMP&Audio Jack/MDC			
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MDC 1.5 Conn.



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Size	B	Document Number	IAYAA (LA-3391P)	Rev
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Left USB CONNECTOR

16 USBP2- USBP2-
16 USBP2+ USBP2+

2 R922 1 @
0_0402_5%

L34

WCM2012F2S-900T04_0805

2 C USB2-
3 C USB2+

+USB_AS

JP23

1 VBUS
2 D-
3 D+
4 GND
5 GND
6 GND
7 GND
8 GND

SUYIN_020167MR004S511ZR

Back side USB Conn.

16 USBP1- USBP1-
16 USBP1+ USBP1+

2 R920 1 @
0_0402_5%

L35

WCM2012F2S-900T04_0805

2 C USB1-
3 C USB1+

+USB_AS

JP13

1 VCC
2 D-
3 D+
4 GND
5 GND1
6 GND2
7 GND3
8 GND4

SUYIN_020173MR004G565ZR

USB SW Board

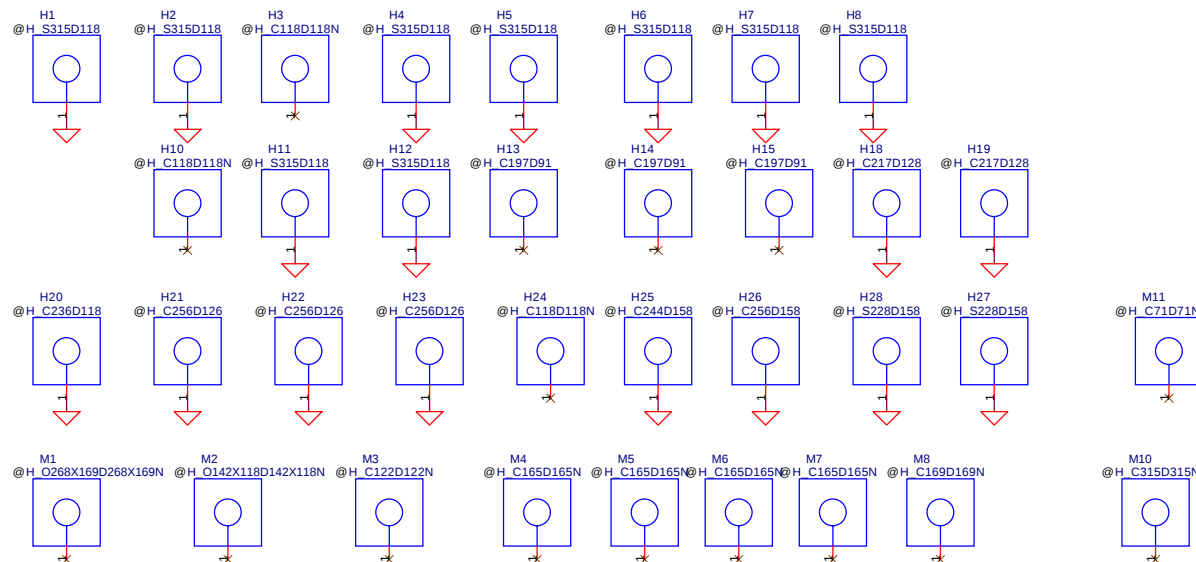
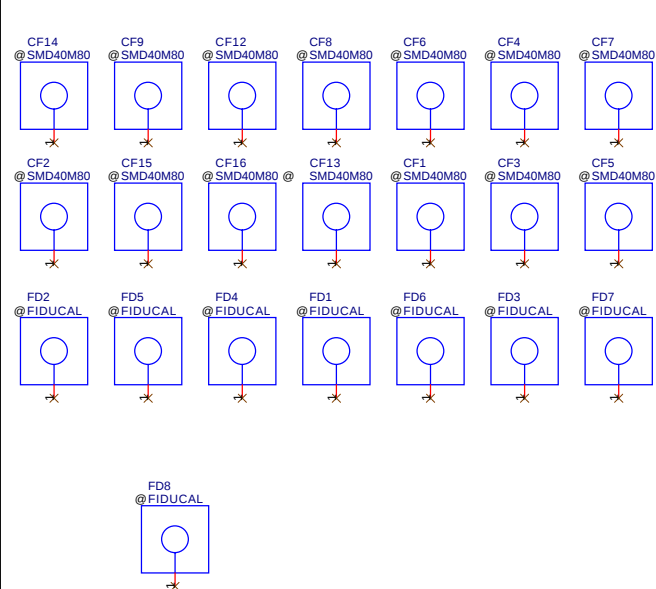
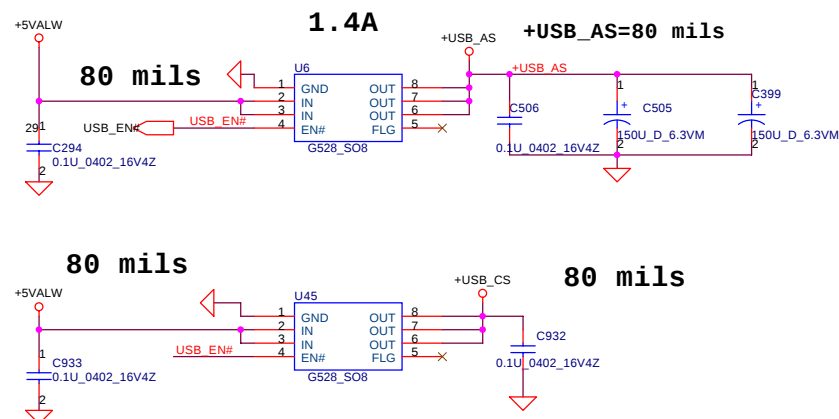
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16 USBP6- USBP6-
16 USBP4+ USBP4+
16 USBP4- USBP4-

+USB_CS

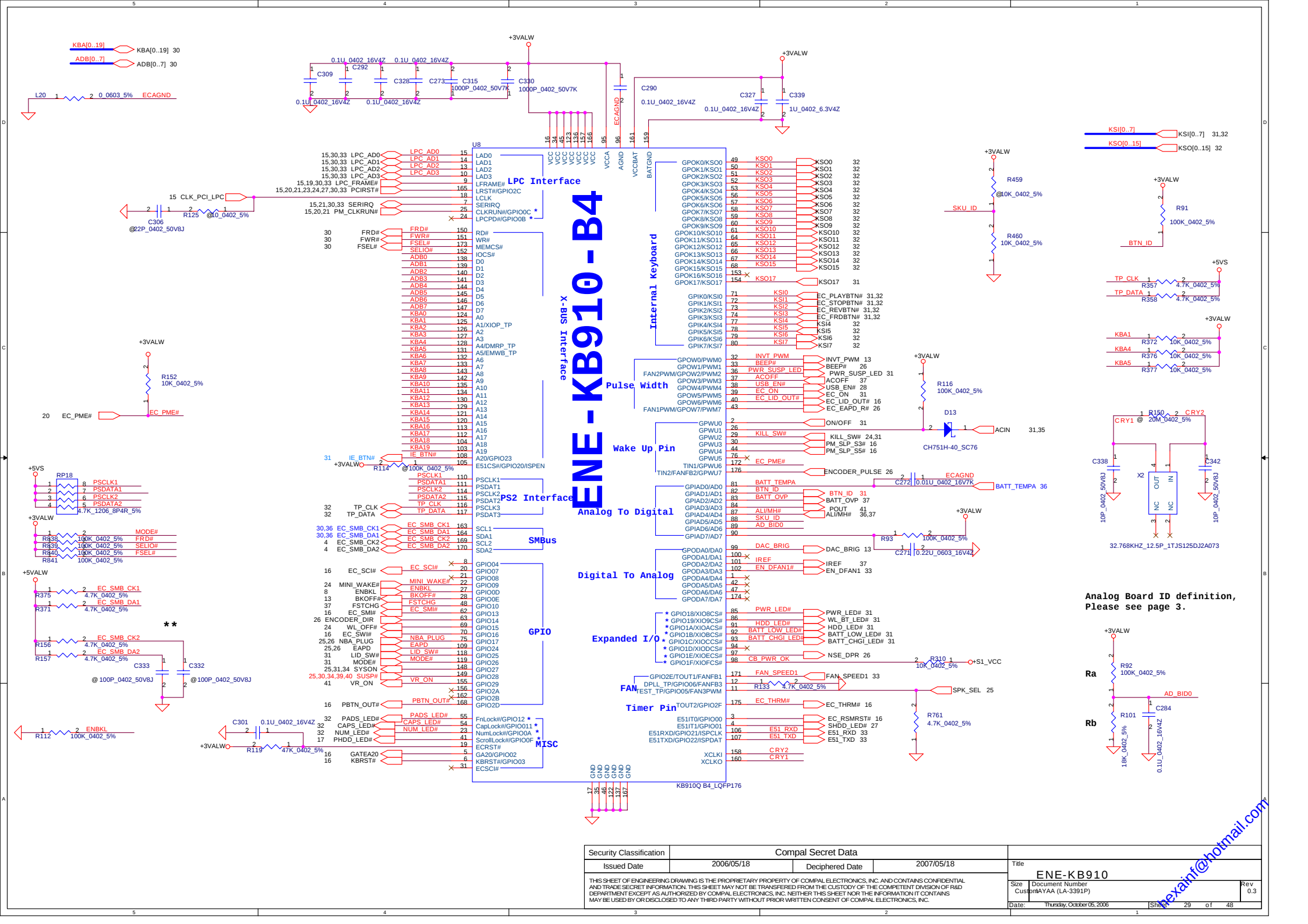
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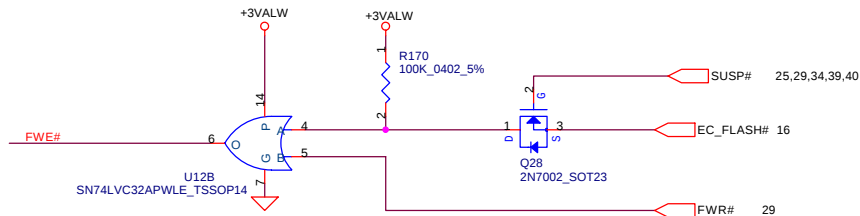
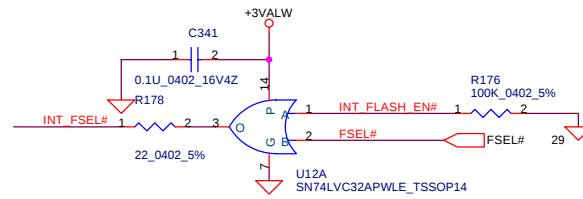
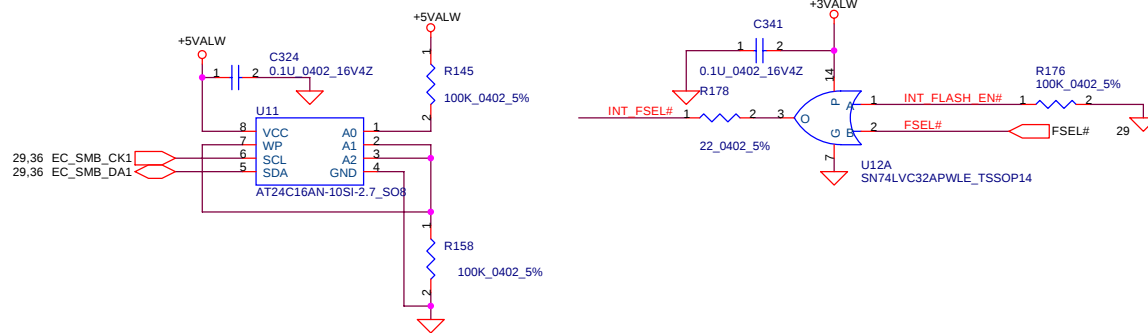
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ACES_85201-1205

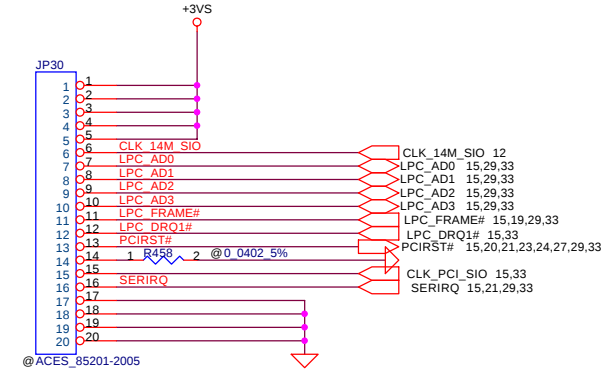


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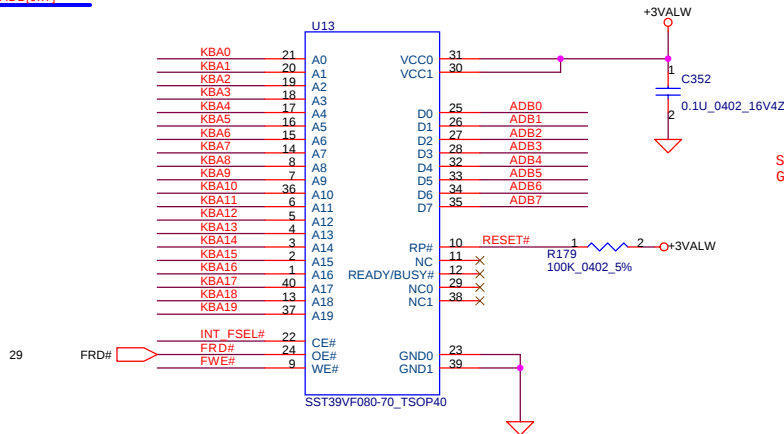




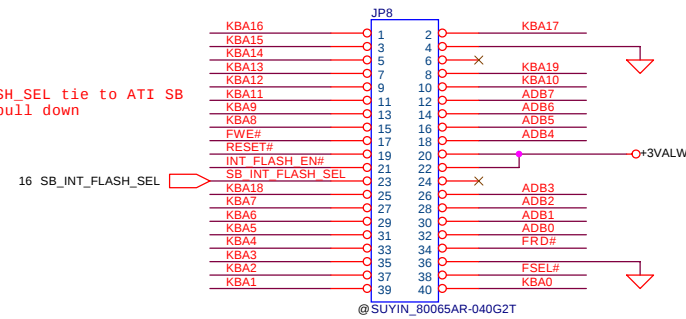
LPC Debug Port



1MB Flash ROM

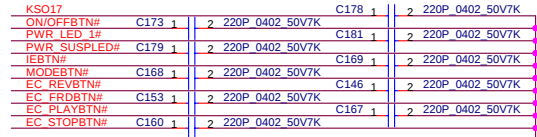
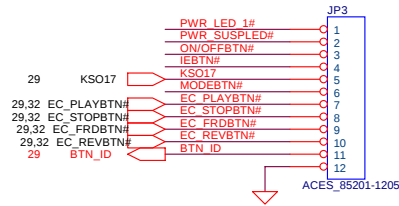


1MB ROM Socket

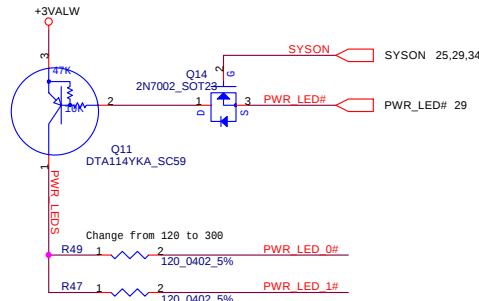
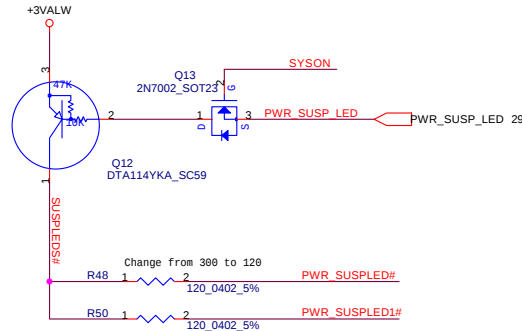
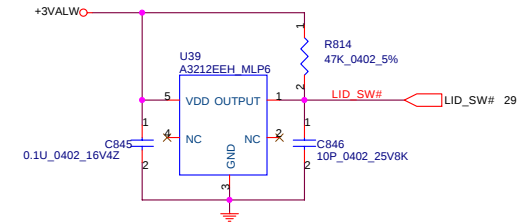


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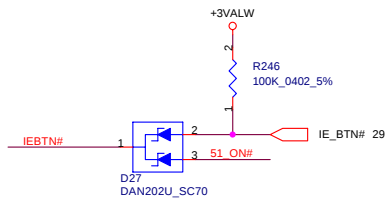
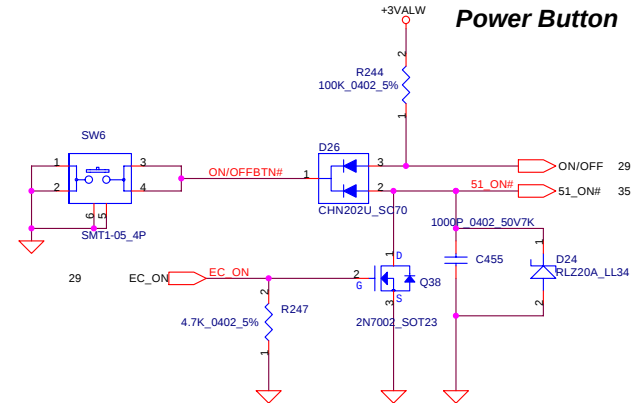
Switch Board Conn.



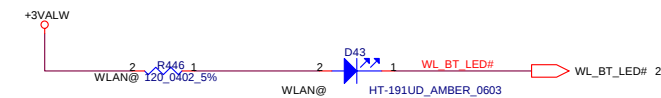
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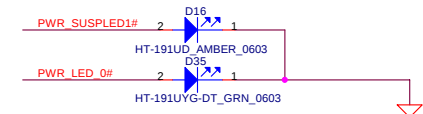
Power Button



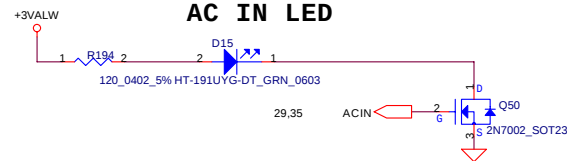
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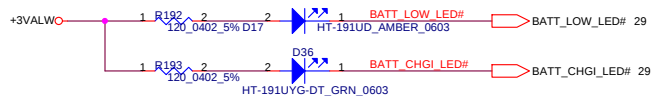
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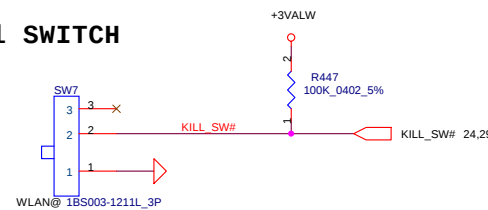
AC IN LED



BATTERY CHG



Kill SWITCH

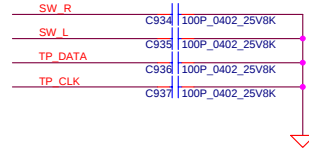
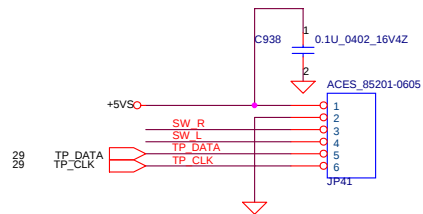


HDD LED

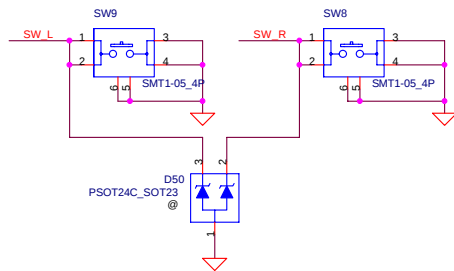


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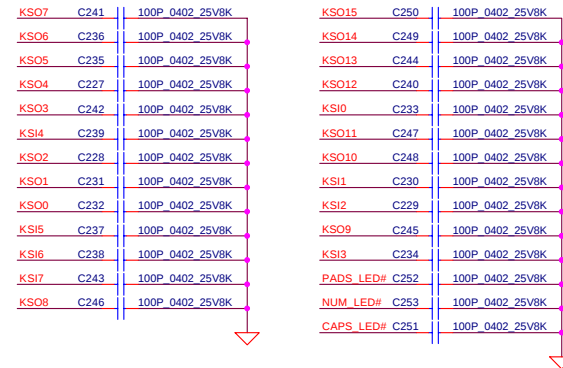
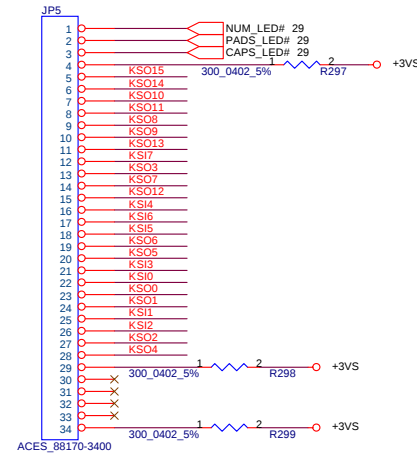
TP Conn.



T/P Button

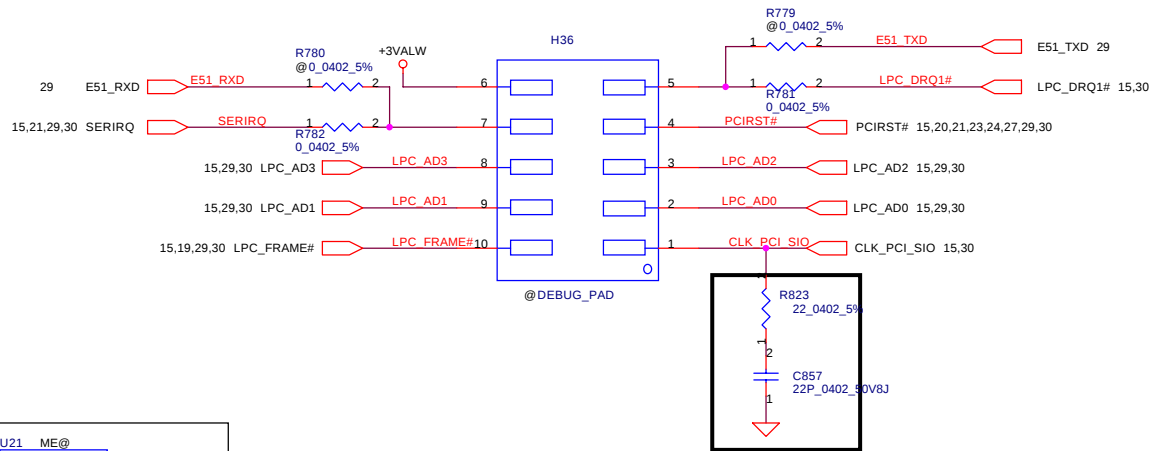
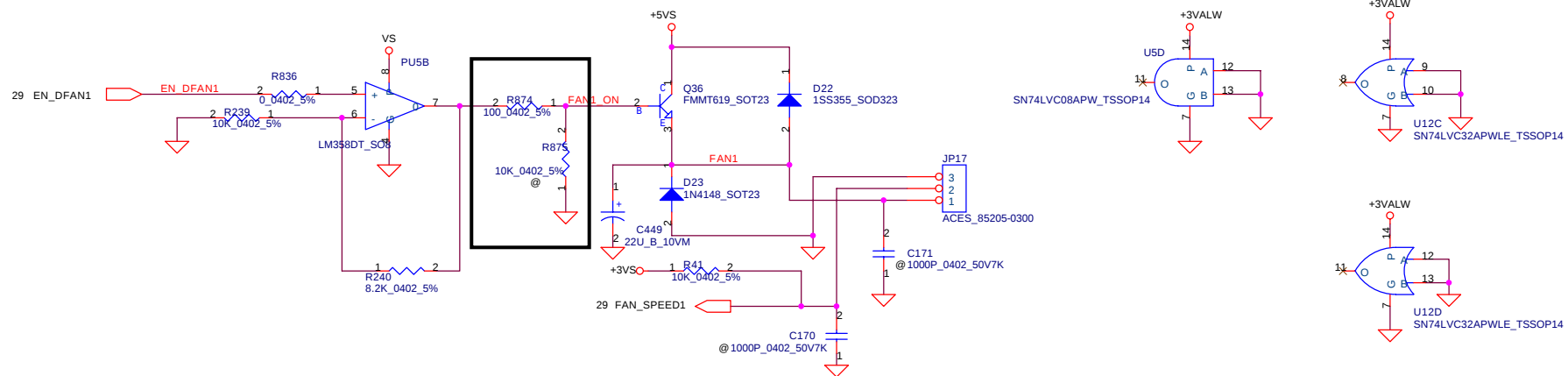


INT_KBD CONN.



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FAN Conn



LPC Debug card

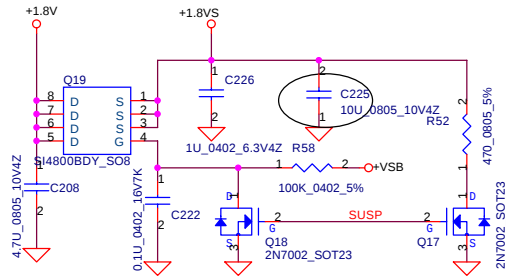
BOM

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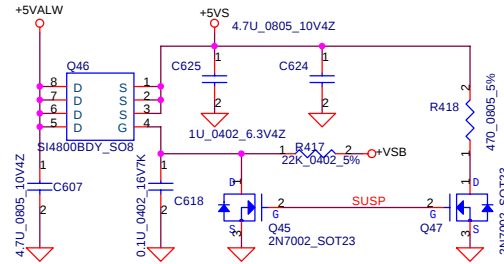
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Issued Date	2006/05/18	Deciphered Date	2007/05/18	Title	FAN & MDC
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hexain@hotmail.com

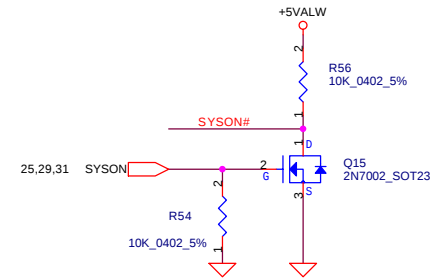
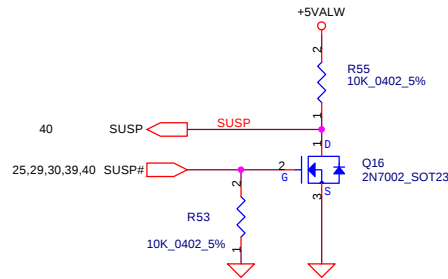
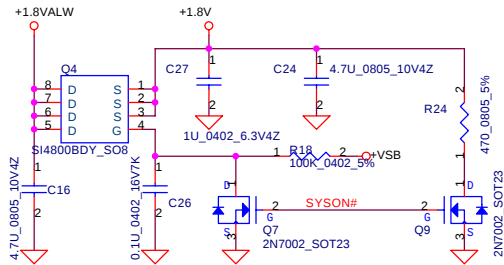
+1.8V TO +1.8VS



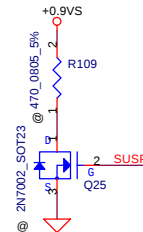
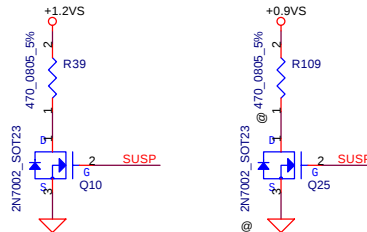
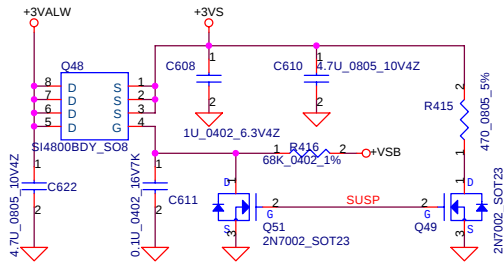
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+1.8VALW TO +1.8V

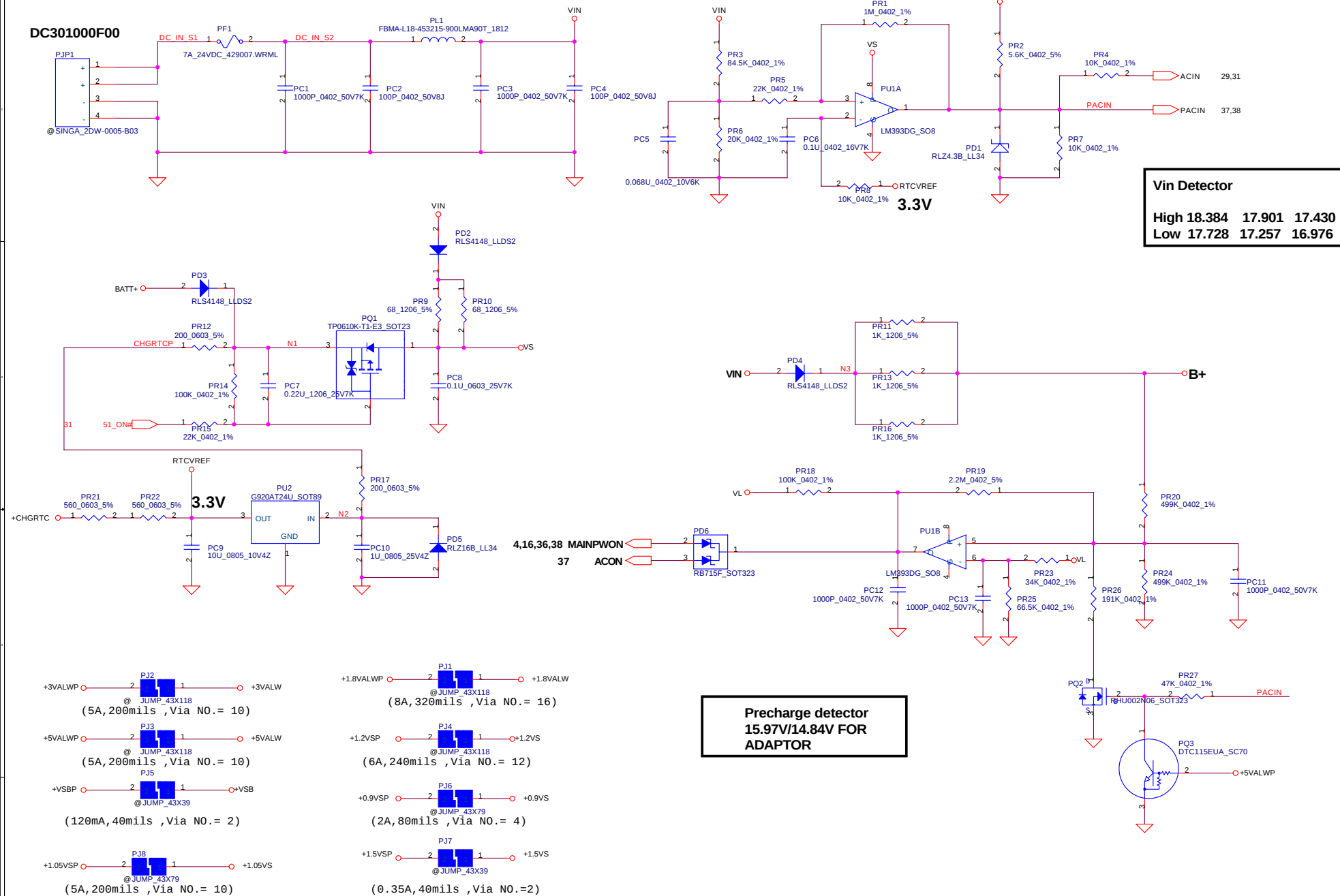


+3VALW TO +3VS



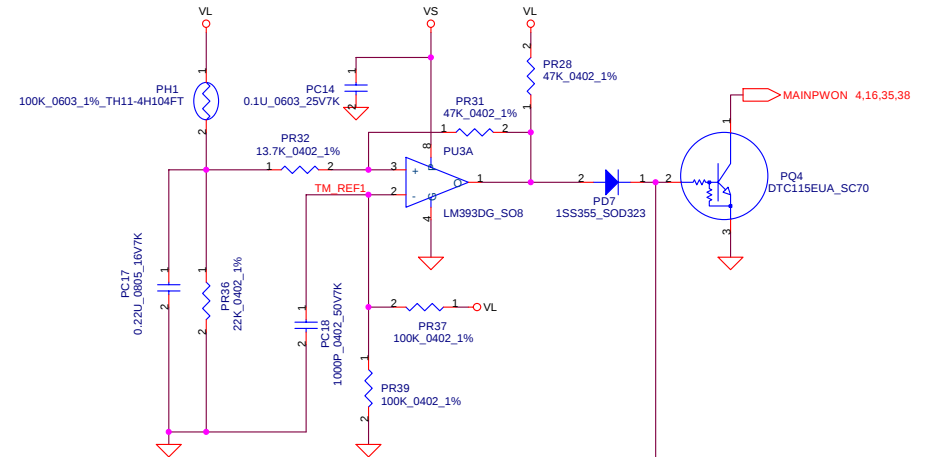
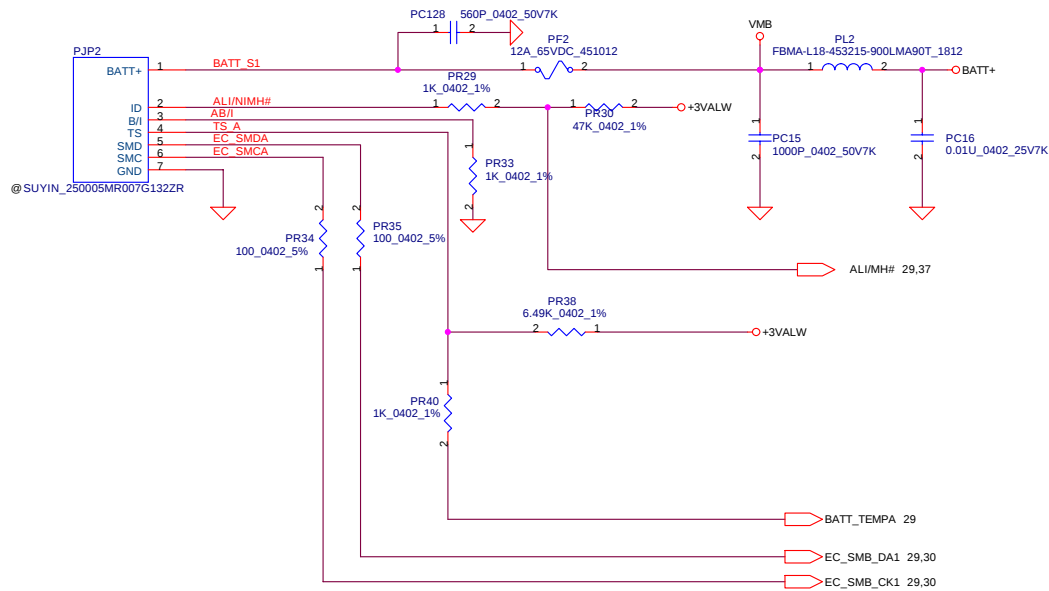
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DC301000F00

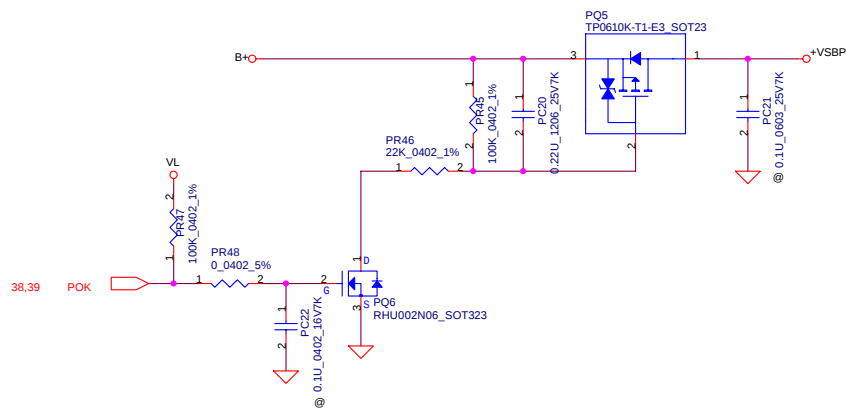
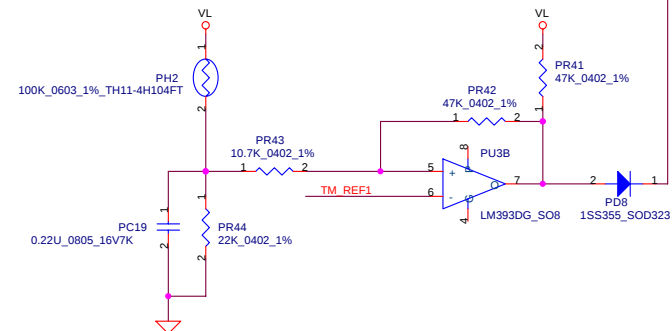


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PH1 under CPU botten side :
CPU thermal protection at 84 degree C
Recovery at 45 degree C

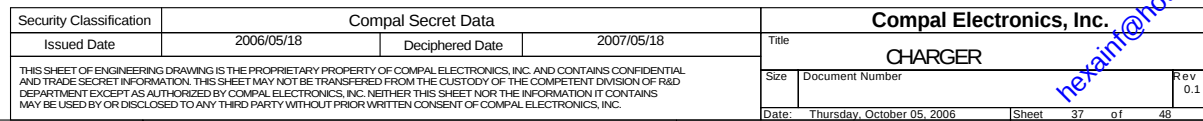


PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 45 degree C

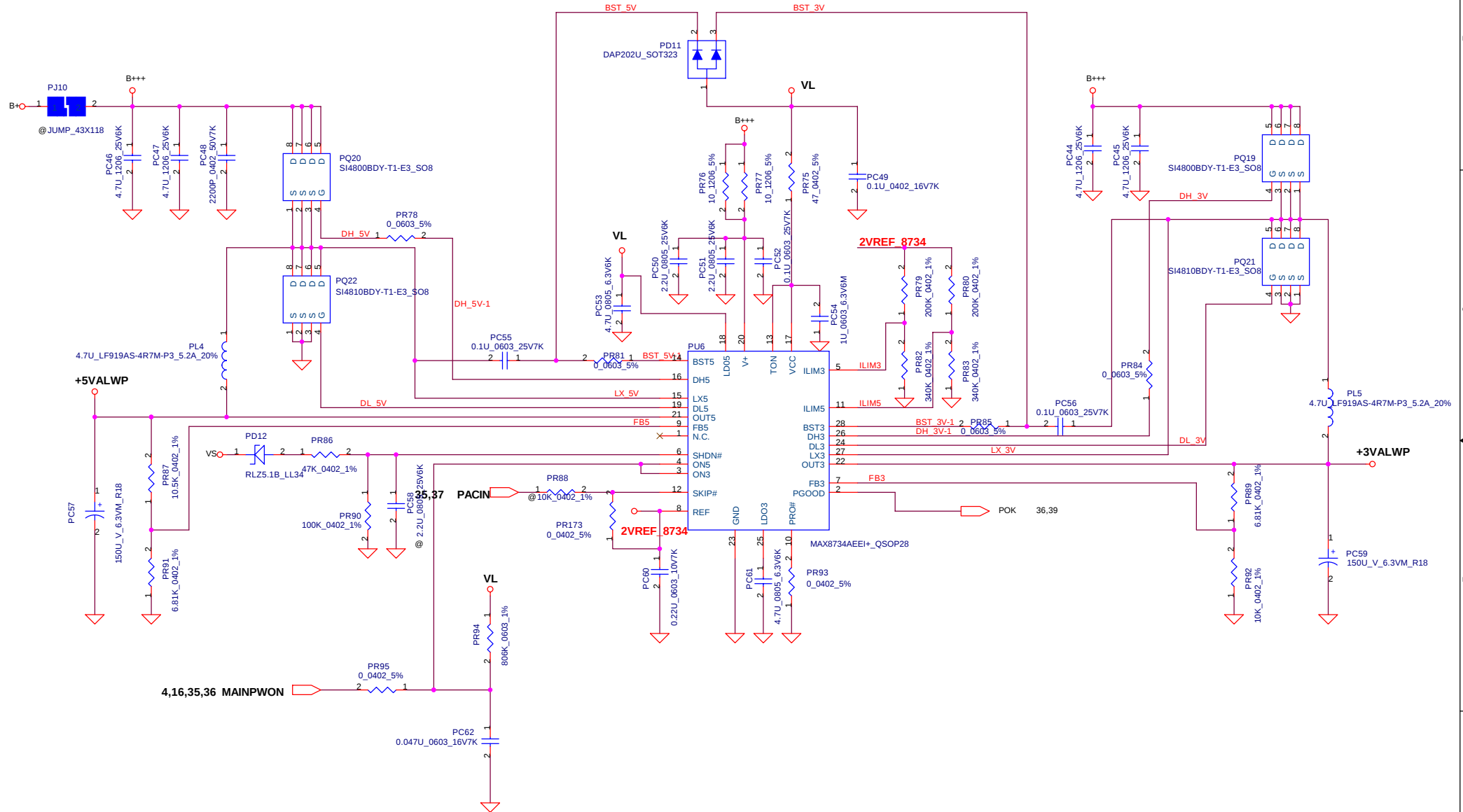


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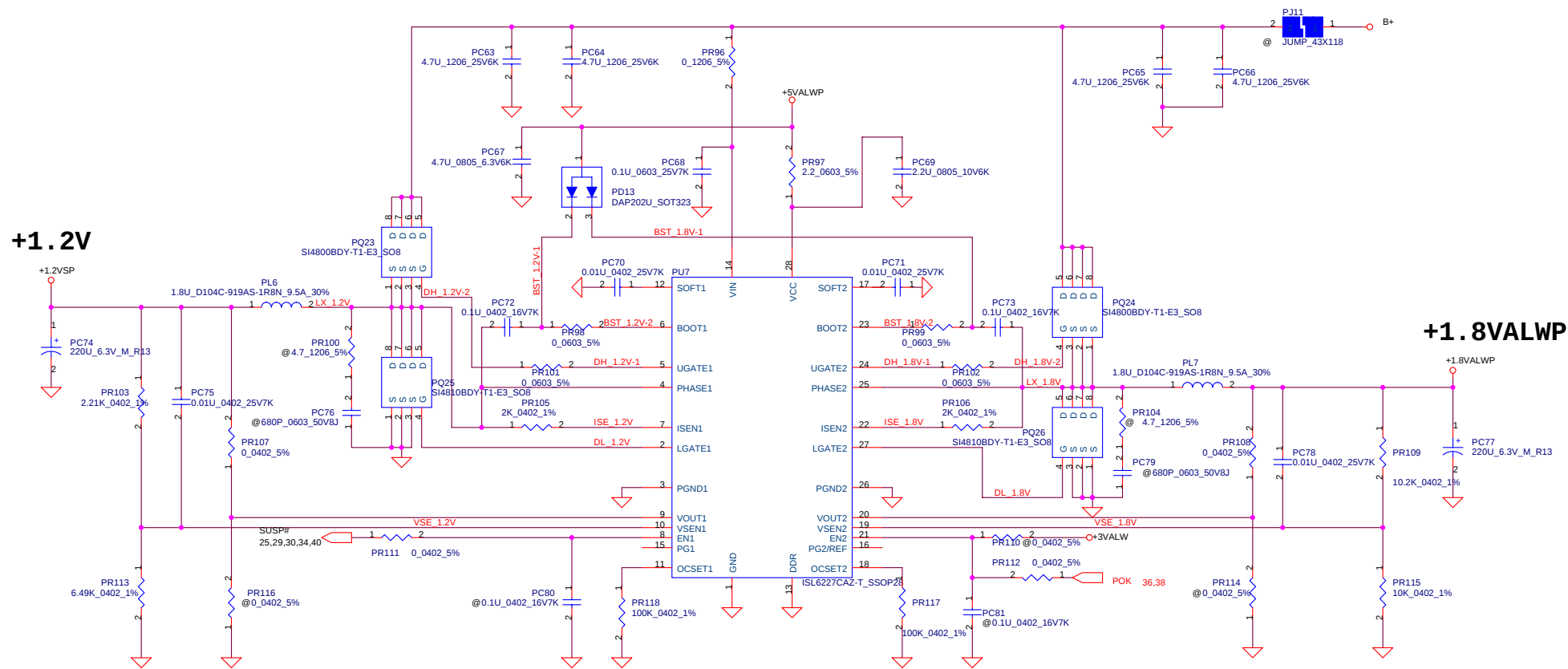
ics, Inc.	Rev 0.1
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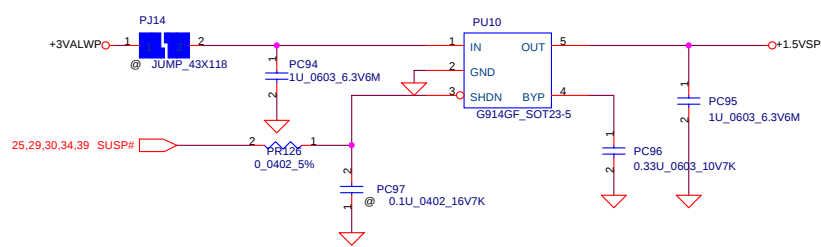
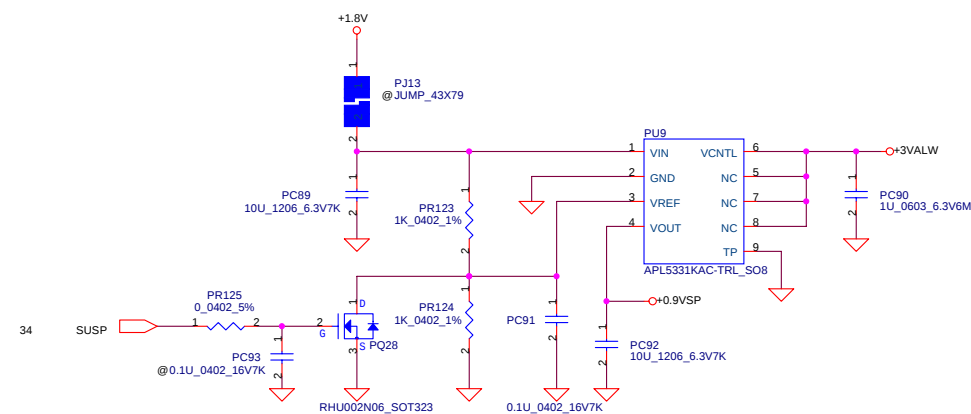
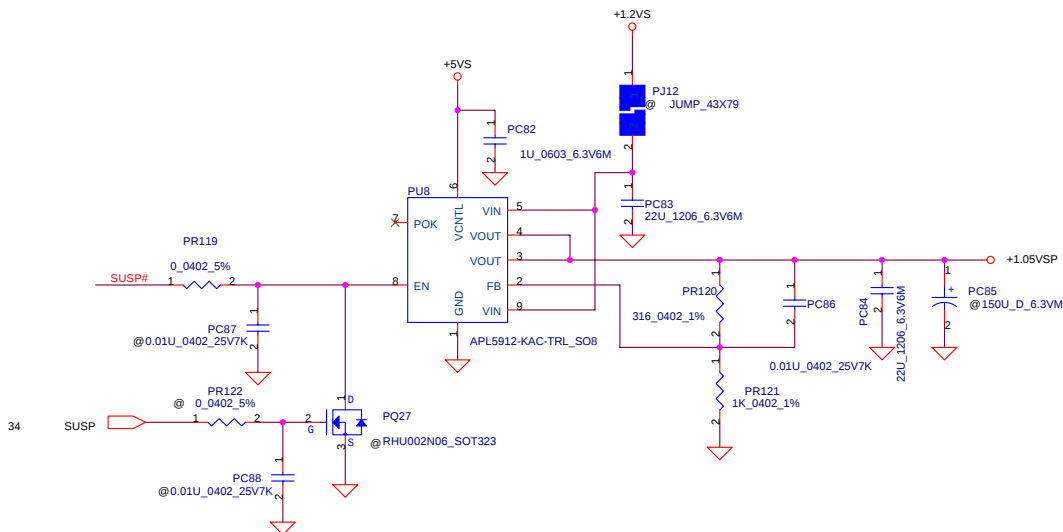


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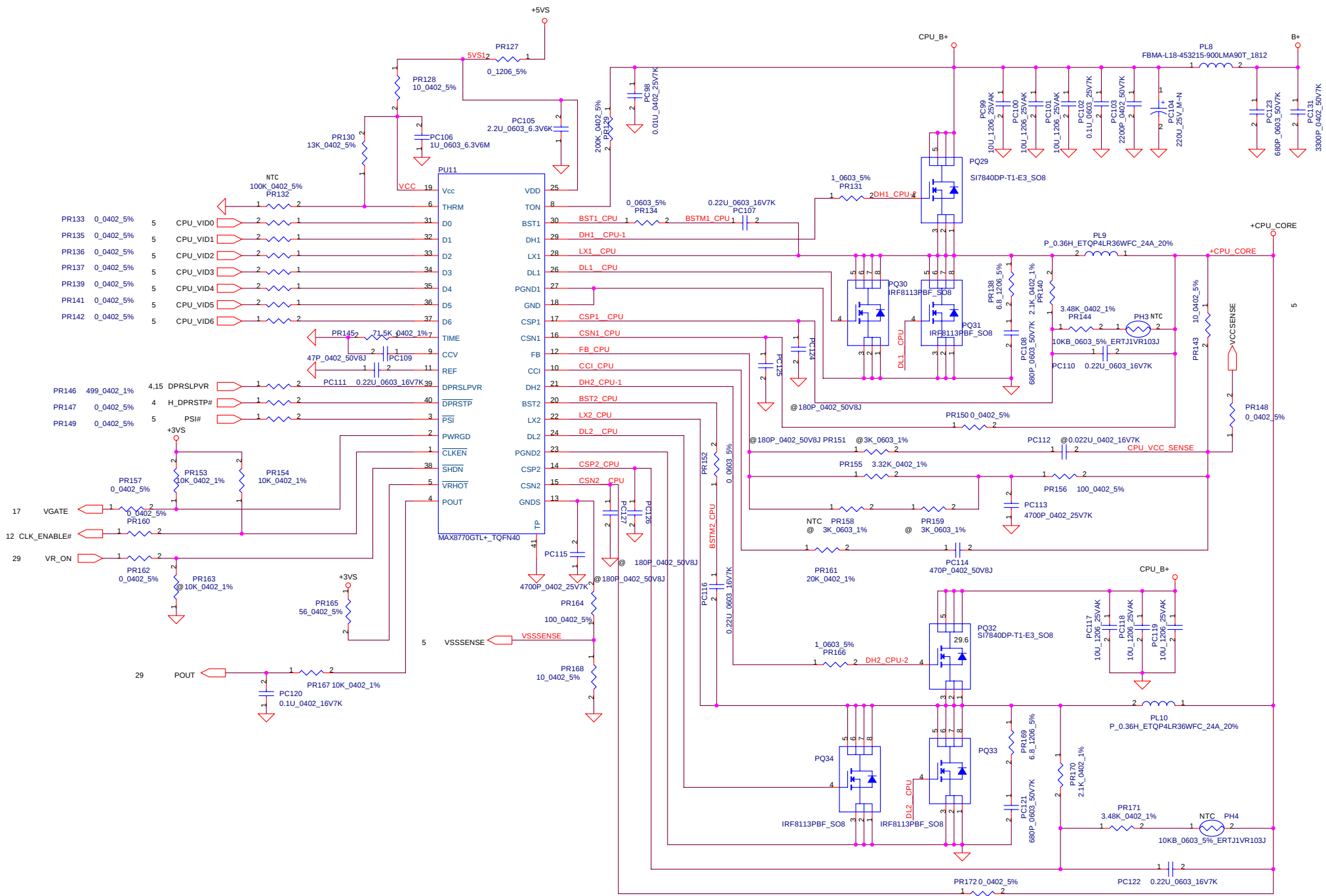


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hexaint@hotmail.com



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HW4 Product Improvement Record (P.I.R.)

Phase: A to B		Date: 2006/07/29			Writer: Gino Lu		
Page#	Action Plan (add; del; change)	Location or Net_List	Before value (Attached file)	After value (Attached file)	Detail Discretion and Root Cause	Rev.	DL/DM Check
8	Net connection	U21.AG30 (MEM_ODT0) U21.AE28 (MEM_ODT1) U21.AC30 (MEM_ODT2) U21.Y30 (MEM_ODT3)	DDR_ODT0 DDR_ODT1 DDR_ODT2 DDR_ODT3	NC NC NC NC	DDR 667 workaround, ATI recommend (PA_RS400R2)	0.2	
10	Net connection	JP16.80 (DIMMA_CKE1)	DDR_SCKE1	DDR_SCKE0			
11	Net connection	JP15.79 (DIMMB_CKE0) JP15.79 (DIMMB_CKE1)	DDR_SCKE2 DDR_SCKE3	DDR_SCKE1 DDR_SCKE1			
10	Net connection	JP16.114 (DIMMA_ODT0) JP16.119 (DIMMA_ODT1) JP15.114 (DIMMB_ODT0) JP16.119 (DIMMB_ODT1)	DDR_ODT0 DDR_ODT2 DDR_ODT1 DDR_ODT3	DDR_SCKE2 GND DDR_SCKE3 GND			
		RP1.4 (CKE3 PU) RP1.1 (CKE2 PU) RP4.4 (ODT3 PU) RP14.3 (ODT0 PU) RP14.2 (ODT1 PU)	DDR_SCKE3 DDR_SCKE2 DDR_ODT3 DDR_ODT0 DDR_ODT1	NC NC NC DDR_SCKE2 DDR_SCKE3			
		Del part Add part	56_0402_5%				
		R40 (ODT2 PU) R12 (CKE2 PD) R17 (CKE3 PD)		180_0402_5% 180_0402_5%			
9	Change part	C70, C68, C63, C62, C51	0.1U_0402_6.3V4Z	1U_0402_6.3V4Z	VDDA_18 decoupling, ATI recommend	0.2	
15	Change part	C295, C298, C300, C305	0.1U_0402_6.3V4Z	0.01U_0402_16V7K	ALINK coupling cap for differential signal, ATI recommend	0.2	
16	Net connection	U9.A21(USB_HSDP1+) U9.B21(USB_HSDM1-)	USBP1- USBP1+	USBP1+ USBP1-	Fix USB function fail	0.2	
16	Net connection	R760.1 (MAINPWONR PU)	+3VS	+3VALW	For SB mainpwron (Gevent) is S5 power pin	0.2	
25	Net connection Del part Change part	R740.2 (PH sensor) R785 (Mic sensor) R872, R873 R786, R842 Q59, Q67 JP34, JP35	N17081292 N16810569 0_0402_5%(@) 100K_0402_5% 2N7002_SOT23 FOX_JA6033L-B5S3-7F	NBA_PLUG MIC_SENSE FOX_JA6333L-B3T0-7F	For audio jack change to normal open	0.2	
26	Net connection	U47.16 (VSS)	GND	CVSS	Fix audio left channel no function	0.2	
29	Change part	R116	10K_0402_5%	100K_0402_5%	Fix BATT charge LED always light, for power workaround	0.2	

HW4 Product Improvement Record (P.I.R.)

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Page#	Action Plan (add; del; change)	Location or Net_List	Before value (Attached file)	After value (Attached file)	Detail Discretion and Root Cause	Rev.	DL/DM Check
15	Add part	D28 R899 C972		CH751H-40_SC76 10K_0402_5% 15P_0402_50V8D SB_BM_REQ#	For C3 pop-up and C1e HW rework. ATI recommend (PA_IXP400AC16)	0.2	
	Net connection	U9.D27 (SB_BMREQ#)	BM_REQ#				
15	Change part	U36 R802	TC7SH00FU_SSOP5	74LVC1G14GW_SOT353-5	C4 timing on Yonah-M platforms workaround, ATI recommend (PA_IXP400BR4)	0.2	
	Add part	R900, R901 C973 D29 Q6 Q1 R902	200K_0402_5%(@)	150K_0402_5% 10K_0402_5% 330P_0402_50V7J CH751H-40_SC76 MMBT3904_SOT23 2N7002_SOT23 0_0402_5% SB_STPCLK#			
	Net connection	U9.E29 (SB_STPCLK#)	H_STPCLK#				
	BOM Structure	Q62, U36, C832, C833, D42	@				
12	Change part	R255	0_0402_5%	4.7K_0402_5%			
	BOM Structure	C831	@				
7,8,9	Change part	U21	216CPP4AKA21HK RC410ME	216DCP4ALA12FG RC410MD	For Product spec	0.2	
9	Change part	C650	220U_D_6.3VM(@)	220U_Y_4VM(@)	For height limit, change to 2mm	0.2	
10		C148	220U_D2_4VM	220U_Y_4VM			
11		C52	220U_D2_4VM	220U_Y_4VM			
17	BOM Structure	C884, C885, C886, C887		2H@	For 2 HDD configuration	0.2	
26	Change part	SW10	EVQWA4001_6P	XRE094_2	For new digital VR	0.2	
26	Add part	C977, C978		1U_0402_6.3V4Z	Reserve for ALC861D/ ALC268 HP out, for Vista integrate driver	0.2	
	BOM Structure	C954, C955		@			
25	Net connection	U38.14 (LINE2_L) U38.15 (LINE2_R)	NC NC	LIN_L LIN_R			
4	DEL PART	R463 R465	47K_0402_5%(@) 10K_0402_5%(@)		Remove useless parts	0.2	
8	DEL PART	R762	4.7K_0402_5%				
19	DEL PART	R23 R138, R139	4.7K_0402_5%(@) 10K_0402_5%(@)				

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27 4 12	Delete part	R305 R304 C665 R268	10K_0402_5%(@) 5.6K_0603_1%(@) 0.1U_0402_16V4Z(@) 4.7K_0402_5%(@)	 	Remove useless parts	0.2	
14	Net rename	DVI_R DVI_G DVI_B DVI_HSYNC DVI_VSYNC	DVI_R DVI_G DVI_B DVI_HSYNC DVI_VSYNC	CRT_OUT_R CRT_OUT_G CRT_OUT_B CRT_OUT_HSYNC CRT_OUT_VSYNC	For designer check	0.2	
29	Net connection	X2.1(X'tal X1) X2.2(X'tal X2)	CRY1 CRY2	CRY2 CRY1	For layout smooth	0.2	
16	Add part BOM structure	Y7 C974, C975 R910 R911, R912 L46, R74, C267, X1, R335 R334	 @	48MHZ 20PF X6G048000FK3H-H 20P_0402_50V8J 1M_0402_5% 0_0402_5% @	Chnage USB clock from osciallor to crystal	0.2	
16	Net connection	R326.1 (GPIO5 PU) R751.1 (GPIO_M PD)	GND +3VS	+3VS GND	For ATi requirement	0.2	
13	BOM structure	C406, C407, C810, C811	@		EMI solution for LVDS	0.2	
14	Change Part BOM structure	L1, L2, L3 C1, C2, C3	FCM2012C-800_0805 @	BK1608LL121-T 0603	EMI solution for CRT	0.2	
14	Change Part	JP23	SUYIN 020133MR004S529ZL~N	SUYIN 020167MR004S511ZR	ME change	0.2	
20	Add part	R913, R914 C976		49.9_0402_1%(@) 0.1U_0402_16V4Z(@)	For LAN reverse	0.2	
4	Change part	R475, R476 R490	40.2_0402_1% 150_0402_5% 27.4_0402_1%	54.9_0402_1% 54.9_0402_1% 54.9_0402_1%	For CPU ITP	0.2	
29	Change part	L20, L23	FBM-L11 160808-800LMT_0603	0_0603_5%	Change EC power sorce and gnd source	0.2	
23	Net rename	U34.26(EECS) U34.28(EEDI) U34.29(EECK)	EECS EEDI EECK	1394_EECS 1394_EEDI 1394_EECK	Name Name duplication	0.2	

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29	Del part Add part Net Rename	Q66 C980 EC_EAPD	2N7002 EC_EAPD	0.01U_0402_16V7K(@) EC_EAPD_R#	For Audio EAPD	0.2	
29	Add part	C979 Q67 R915 R916 R917 R919		1U_0402_6.3V4Z(@) 2N7002_S0T23(@) 8.2K_0402_5%(@) 20K_0402_5%(@) 2.4K_0402_5%(@) 1K_0402_5%(@)	For POST BEEP no sound issue	0.2	
16	Del part	R384(GATE20 PU) R385(KBRST# PU)	10_0402_5% 10_0402_5%		No need external pull up	0.2	
16	Net connection Add part	U9.D6(LPC_PME#) R918	EC_PME#	LPC_PEM# 10K_0402_5%	Disconnect SB PME# to EC PME#	0.2	
16 27	Add part	C981 C982, C983		10P_0402_50V8K(@) 22P_0402_50V8J(@)	For EMI reserve	0.2	
12	Del part Net connector	R712 U23.11 (Clock REQ B)	0_0402_5%(@) N19175427	MINI_CLKREQ#	For mini card clock request	0.2	
28	BOM Structure	C712, C715		@	Transion test pass	0.2	
29	Change part	U46	NC7SZ14M5X_S0T23-5	74LVC1G14GW S0T353-5	Change package for logic IC standard	0.2	
29	Del part Net connection	R867, R868 R714.2 (BITCLK to HD) R715.2 (BITCLK to MDC)	0_0402_5% N52707434 N52707448	AZ_BITCLK_HD AZ_BITCLK_MD	Azalia signal, no need two serial reisistor	0.2	
28	Add part	R920, R921, R922, R923		0_0402_5%(@)	Reserve resistor for USB signal	0.2	
26	Add part	R924 C984		0_0402_5% (@) 0.01U_0402_16V7K(@)	Reserve function for EC control HP_EN	0.2	
26	BOM Structure	C406, C407, C810, C811	@		For LVDS EMI solution	0.2	
29	Change part	R101	0_0402_5%	8.2K_0402_5%	Board ID change to 1 for Rev0.2	0.2	
25	Add part	R925		39.2K_0603_5%	For ALC861 +Vista driver	0.3	
26	BOM Sturcture	C977, C978 C954, C955	@	@	For Vista intergated driver	0.3	

HW4 Product Improvement Record (P.I.R.)

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26	Del part	R919 R916 R917 Q67	1K_0402_5%(@) 20K_0402_5%(@) 2.4K_0402_5%(@) 2N7002_SOT23(@)	 	Remove POST BEEP no sound issue	0.3	
29	Change part	R101	8.2_0402_5%	18_0402_5%	PCB revision ID	0.3	
4 15	BOM Sturcture	R491 R167 R713	@ @	 @	For C4 timing	0.3	
19	BOM Sturcture	R334 R335	@ 	 @	48M oscillator select	0.3	
20	Del part Change part	R235 C433	10_0402_5%(@) 22P_0402_50V8J(@)	 18P_0402_50V8J(@)	LAN PCI clock for EMI	0.3	
15	BOM Structure	C832, C833, C973, D29, D42, Q1, Q6, Q62, R802, R900, R901, U36 R713, R902	 @	@ 	No need C4 support	0.3	
12 15	Change part BOM Structure Add part	R255 C831 Q66 U49 R927	4.7K_0402_5% 	0_0402_5% @ 2N7002_SOT23(@) 74LVC1G14GW_SOT353-5(@) 10K_0402_5%(@)			
20	Add part	R926	 	20K_0402_1%(@)	Internal MIC sensor	0.3	
20	Change part	C286, C287	18P_0402_50v8D	12P_0402_50v8J	RTC timing	0.3	
20	Del part	L23	0_0603_5%	 	Component reduce (EC A-power)	0.3	
15	Del part	R317	0_0402_5%(@)	 	Layout reduce (SB H_RESET#)	0.3	
15	Change part	R318	11.8K_0603_1%	11.3K_0603_1%	USB adjust and EMI	0.3	
16 27	BOM Sturcture	R716, R717, R718, R871 R886, C864, C865, JP36	 	MDC@ MDC@	MDC option	0.3	
26	Add part Change part	R928, R929 R862, R863	 39K_0402_5%	20_0402_5% 24K_0402_5%	HP serial resistor for AP2056 noise when use mono HP gain adjust	0.3	

HW4 Product Improvement Record (P.I.R.)

Phase: B to C		Date: 2006/09/29			Writer: Gino Lu		
Page#	Action Plan (add; del; change)	Location or Net_List	Before value (Attached file)	After value (Attached file)	Detail Discretion and Root Cause	Rev.	DL/DM Check
16	Del part Change part Net connect BOM Structure	C974 Y7 R910 R911 C975 R912 R912.1 (48MHz source) X1.3 (48MHz source) C975.2 (48MHz source) L46, R74, C267, X1	20P_0402_50V8J 48MHZ_20PF_ 1M_0402_5% 0_0402_5% 20P_0402_50V8J 0_0402_5% 48M_XTAL1 48M_XTAL1 48M_XTAL1 @	 12P_0402_50V8J 30_0402_5% OSC_48MHZ OSC_48MHZ OSC_48MHZ	For USB logo and EMI	0.3	
26	Add part	Q67		2N7002_S0T23	De- Bo noise	0.3	
26	Change part Del part Change part	C954, C955 C977, C978 C957 R830, R832 C947, C949 C948, C950	1U_0603_6.3V4Z(@) 1U_0603_6.3V4Z 1U_0603_16V6K 1.5K_0402_5% 1U_0402_6.3V4Z 1U_0402_6.3V4Z	2.2U_0603_6.3V6K(@) 2.2U_0603_6.3V6K 2.2U_0603_6.3V6K 0.22U_0402_6.3V6K	Audio precision	0.3	
33	Change part	C449	10U 10V M A NOJ H1.6	22U 10V M B NOJ H1.9	For De-fan noise	0.3	
13	Net connect			B+	For dual lamp LCD	0.3	
33	Net connect Change part BOM Structure	PU5.5 (0P+) PU5.6 (0P-) R240.2 R836 R240 R874 R875, C449	N19688420 (FAN FB) N19688478 (EC_FANCTRL) FAN1 10K_0402_5% 5.1K_0402_5% 5.1K_0402_5% @	N19688478 (EC_FANCTRL) N19688420 (FAN FB) N19688714 (FAN FB) 0_0402_5% 8.2K_0402_5% 100_0402_5%	Update FAN control circuit	0.3	

5 4 3 2 1

IAYAA POWER Product Improvement Record (P.I.R.)

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	0807	P.39	Change net susp# to pok and pok to susp#	
2.	0807	P.41	Add PC124,PC125,PC126,PC127	reserve for in-phase issue
3.	0929	P.36,37	Add PC128,PC129,PC130	For EMI solve 200MHz-300MHz Broad band
4.	0929	P.41	Add PC131	For EMI solve 80MHz-100MHz Broad band

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