

COMPAL CONFIDENTIAL

MODEL NAME : *HBT10*
COMPAL P/N : *DA600001K10*
PCB NO : *LA-2811*
Revision : *1.0*

Sakhir 10E
LA-2811 Rev1.0 Schematic

HBT10 Schematics Document
uFCBGA/uFCPGA Mobile Dothan
ATI RL300MB + SB200(IXP150)
2005 - 05 - 04<A>

Function/B
LS-2811

LAN/B
LS-2812

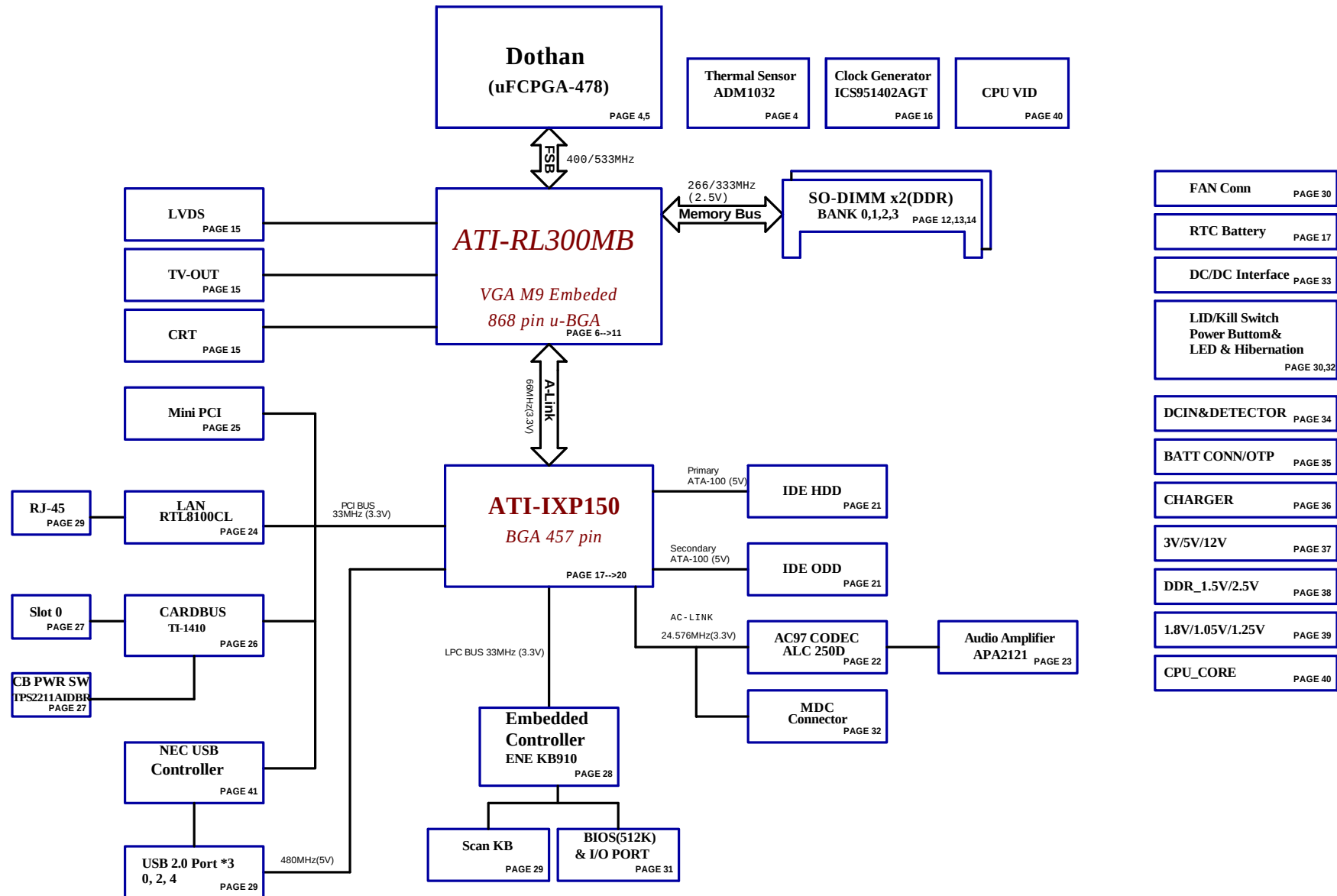
M/B LA-2811

USB/B
LS-2813

TP/B
LS-2814

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Issued Date	2005/03/01	Deciphered Date	2006/03/01	Cover Sheet	
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BLOCK DIAGRAM



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPUVID	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+VGA_CORE	1.0V/1.2V switched power rail for VGA chip	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	AGP 4X/8X	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF
+2.5VALW	2.5V always on power rail	ON	ON	ON*
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ##GNT#	Interrupts
CardBus	AD20	2	PIRQA
LAN	AD19	3	PIRQD
Mini-PCI1	AD18	1(for Wireless Lan)	PIRQC/PIRQD

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02)	1010 000X b		
(24C04)	1011 000Xb		

IXP150 SM Bus address

Device	Address
Clock Generator (1CS951402AGT)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM2	1010 001Xb

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

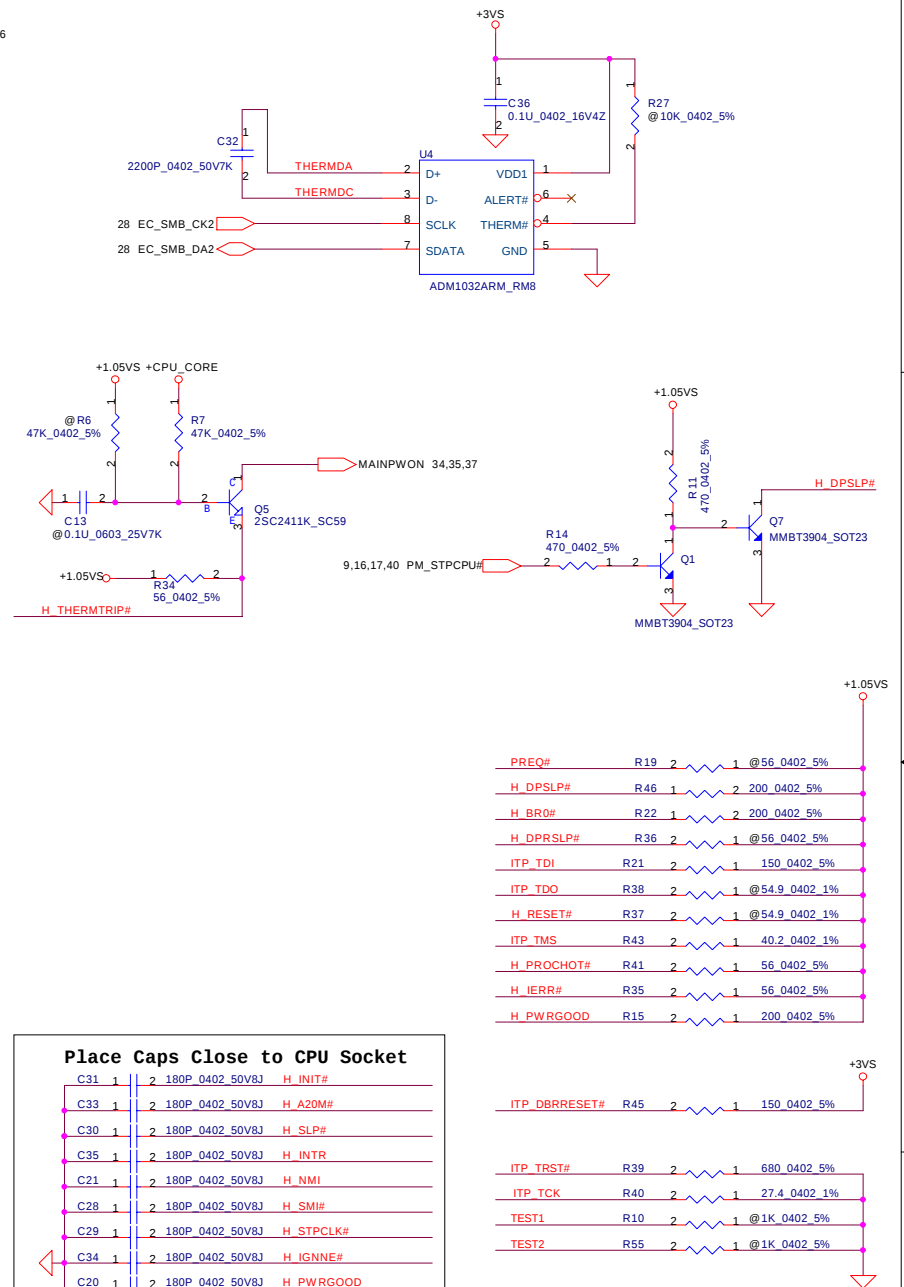
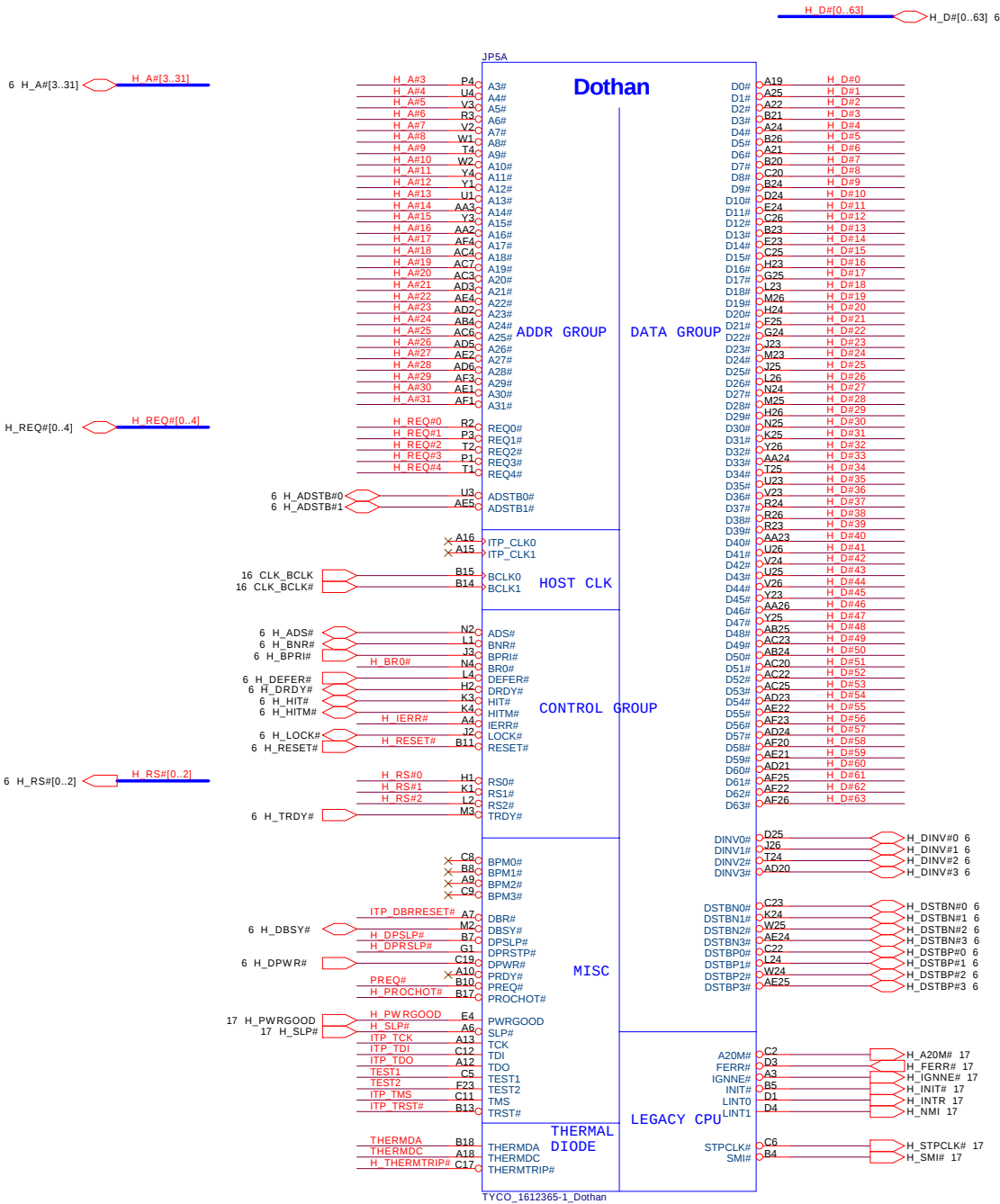
Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

SKU ID Table

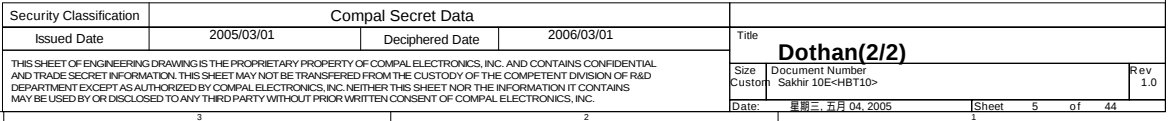
10E		
SKU_ID	Board ID	Scan Code
1-Button	7	3
7-Buttons-W	5	2
7-Buttons-J	4	10
1-Button-J-HDD	3	11

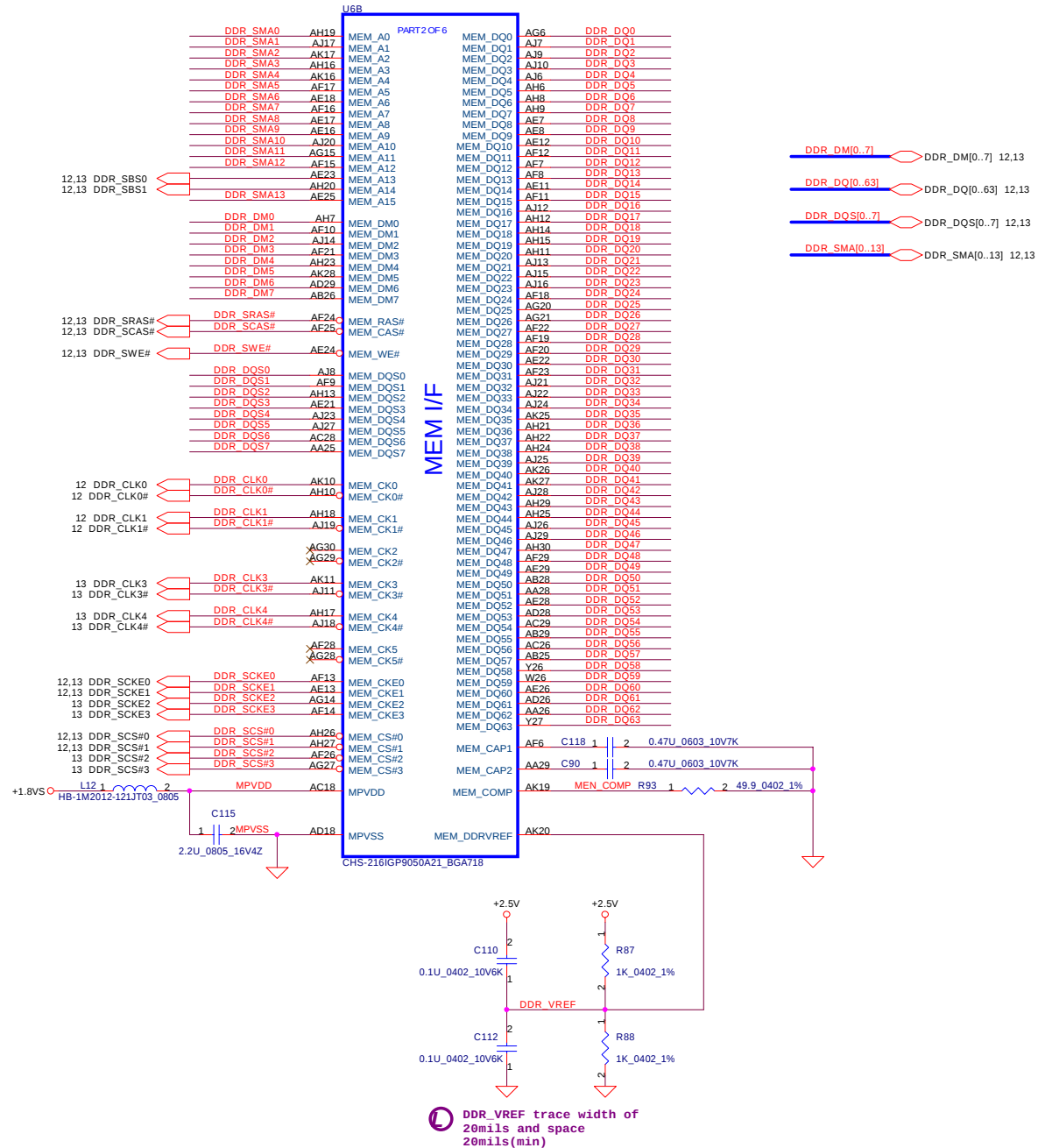
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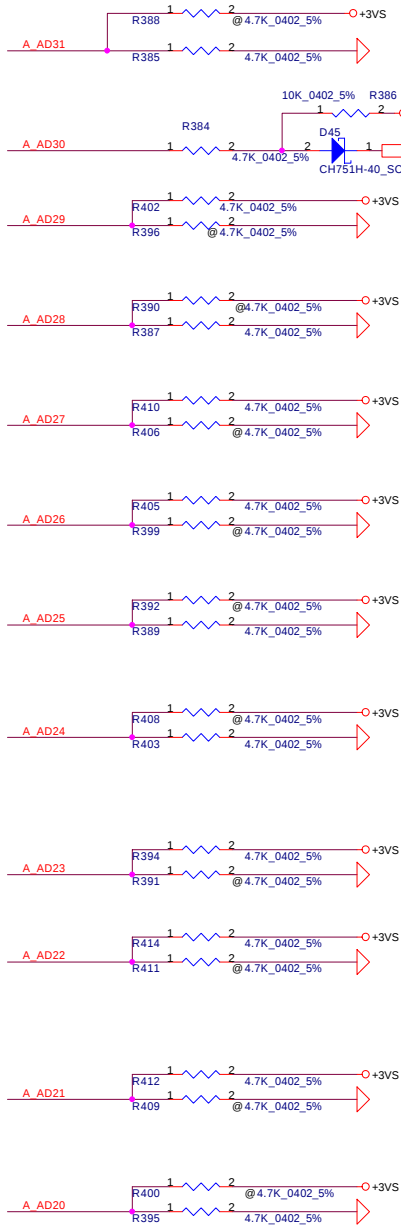
THERMDA & THERMDC Trace / Space = 10 / 10 mil

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8,17 A_AD[0..31] A_AD[0..31]

A_AD[31..30] : FSB CLK SPEED

DEFAULT: 01

00: 100 MHZ
01: 133 MHZ
10: 200MHZ
11:166 MHZ

A_AD29: STRAP CONFIGURATION

DEFAULT: 1

0: REDUCE SET
1: FULL SET

A_AD28: SPREAD SPECTRUM ENABLE

DEFAULT: 0

0: DISABLE
1: ENABLE

A_AD27: FrcShortReset#

DEFAULT: 1

0: TEST MODE
1: NORMAL MODE

A_AD26 : ENABLE IOQ

DEFAULT: 1

0: IOQ=1
1: IOQ=12

A_AD25/A_AD17 : CPU VOLTAGE[1..0]

DEFAULT: 10

00: 1.05V
01: 1.35V
11: 1.75V
10: 1.45V
AD25=1 DESTOP CPU
AD25=0 MOBILE CPU
AD17 - - DON'T CARE

A_AD24 : MOBILE CPU SELECT

DEFAULT: 1

0: BANIAS CPU
1: OTHER CPU

A_AD23 : CLOCK BYPASS DISABLE

DEFAULT: 1

0: TEST MODE
1: NORMAL

A_AD22 : OSC PAD OUTPUT PCICLK

DEFAULT : 1

0: PCICLK OUT
1: OSC CLK OUT

A_AD21 : AUTO_CAL ENABLE

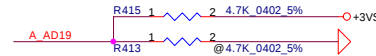
DEFAULT : 1

0: DISABLE
1: ENABLE

A_AD20 : INTERNAL CLK GEN ENABLE

DEFAULT : 0

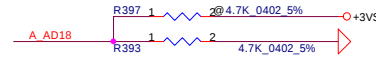
0: DISABLE
1: ENABLE



A_AD19 : MEMORY IO VOLTAGE

DEFAULT: 1

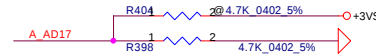
0: 1.8V
1: 2.5V



A_AD18 : ENABLE PHASE CALIBRATION

DEFAULT: 0

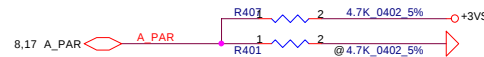
0: DISABLE
1: ENABLE



A_AD25/A_AD17 : CPU VOLTAGE[1..0]

DEFAULT: 0

00: 1.05V
01: 1.35V
11: 1.75V
10: 1.45V

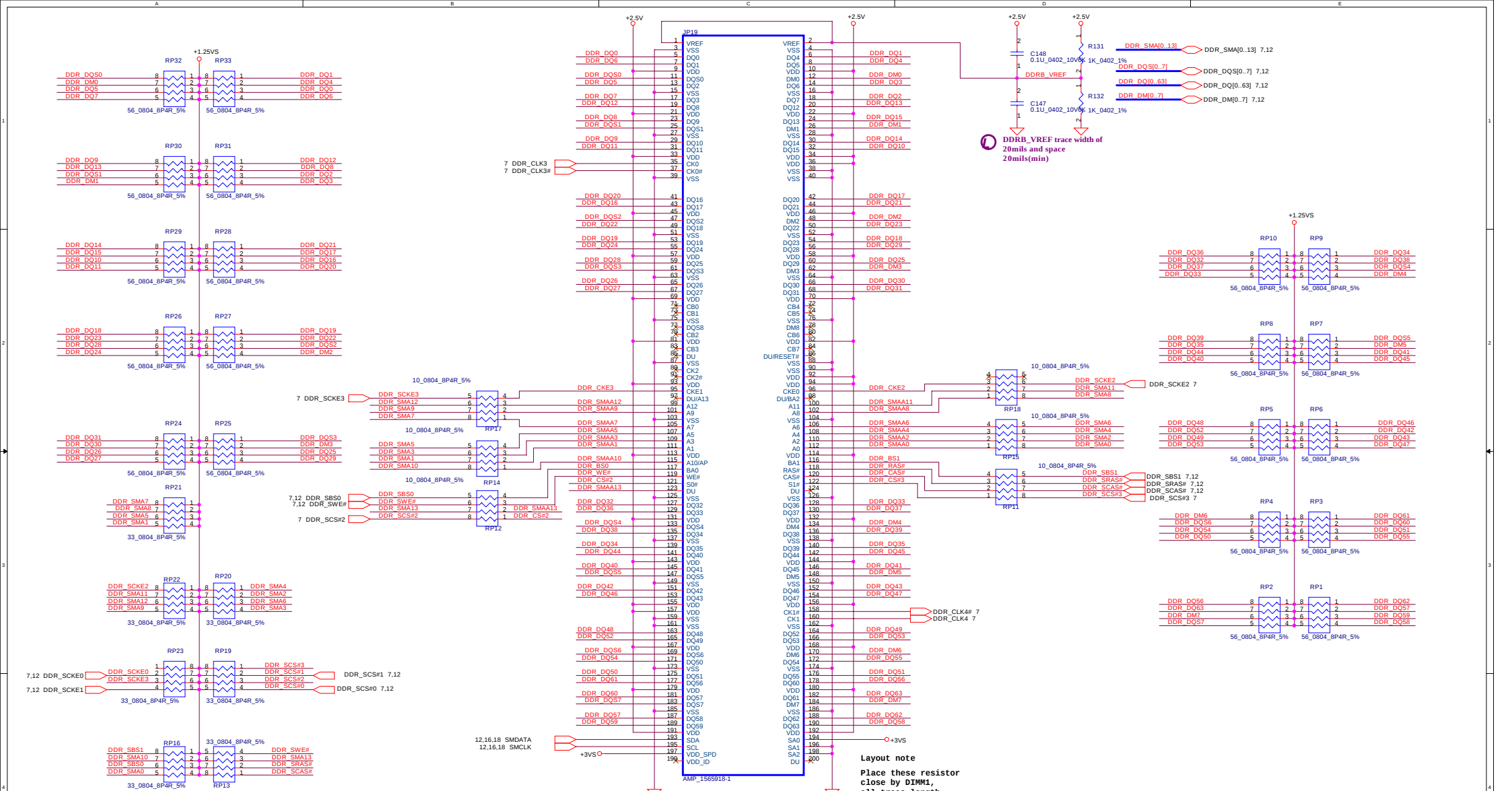


PAR: EXTENDED DEBUG MODE

DEFAULT : 1

0: DEBUG MODE
1: NORMAL

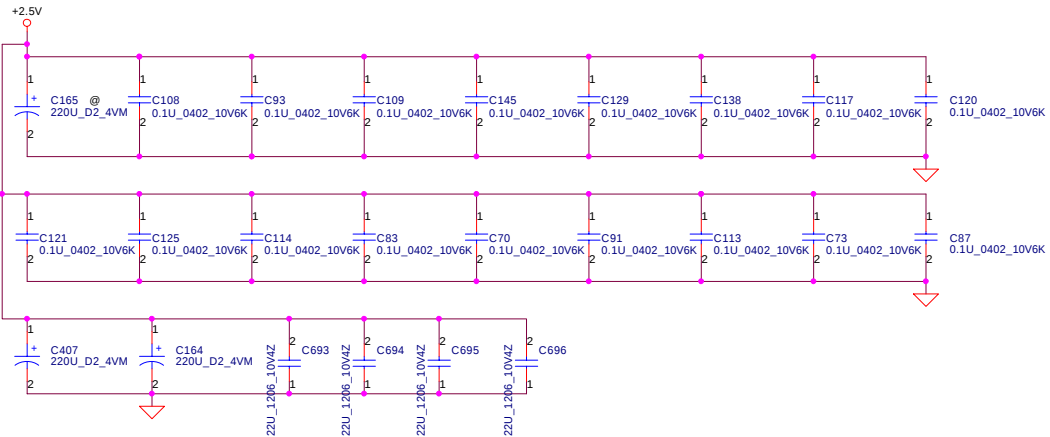
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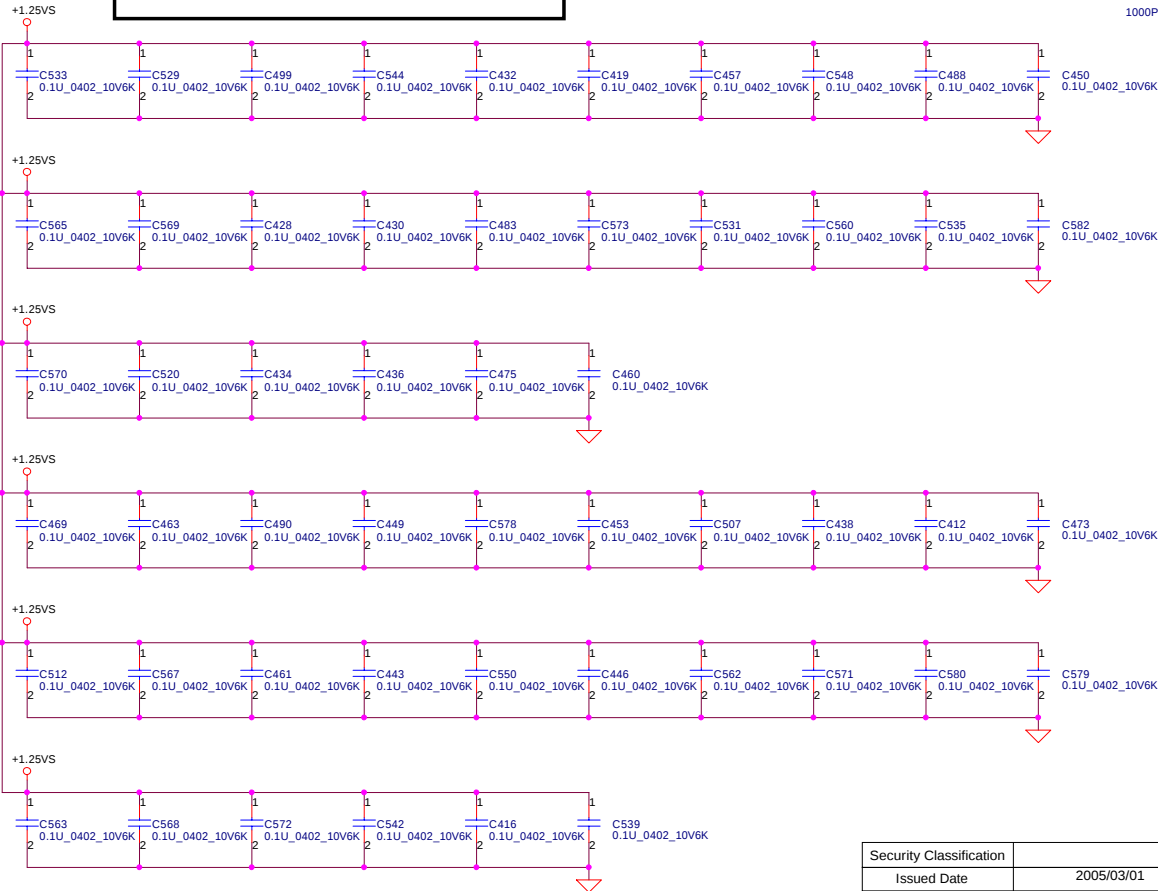
DDR TOPOLOGY 1 FOR SMAA[0, 3, 6:12], SBA[1, 0], SRAS#, SCAS#, SWE#

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				DDR-SODIMM SLOT1				
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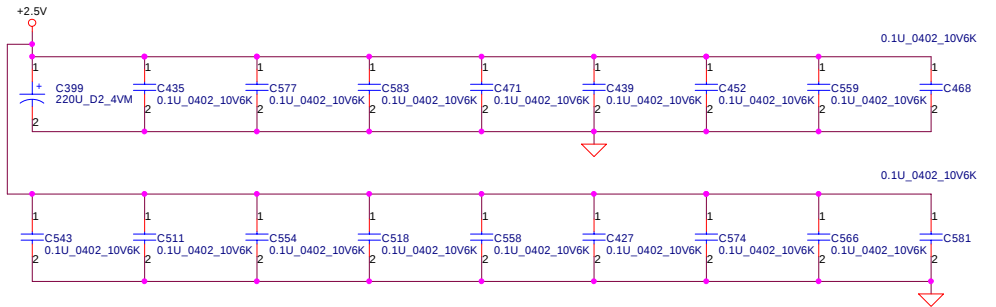
Layout note :
Distribute as close as possible
to DDR-SODIMM0.



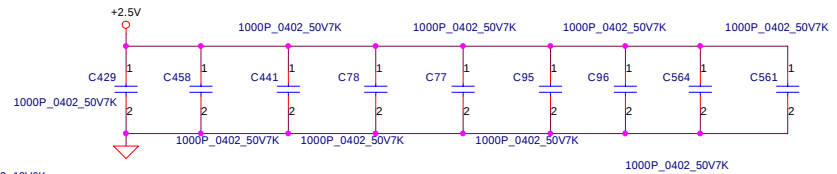
Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25VS



Layout note :
Distribute as close as possible
to DDR-SODIMM1.

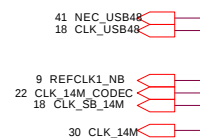
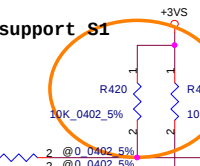


Layout note :
for EMI solution

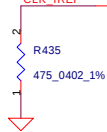


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Unpop when support S1



Pop when using LPC debug card



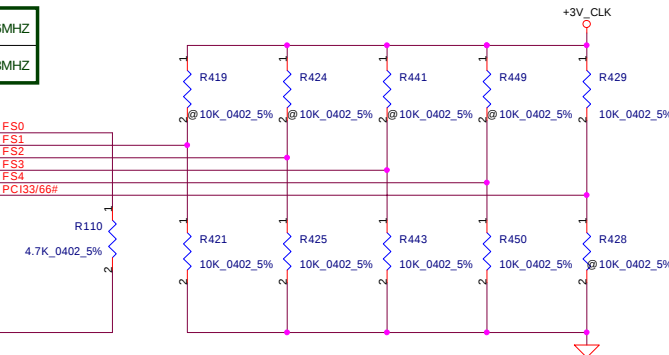
CLOCK FREQUENCY SELECT TABLE

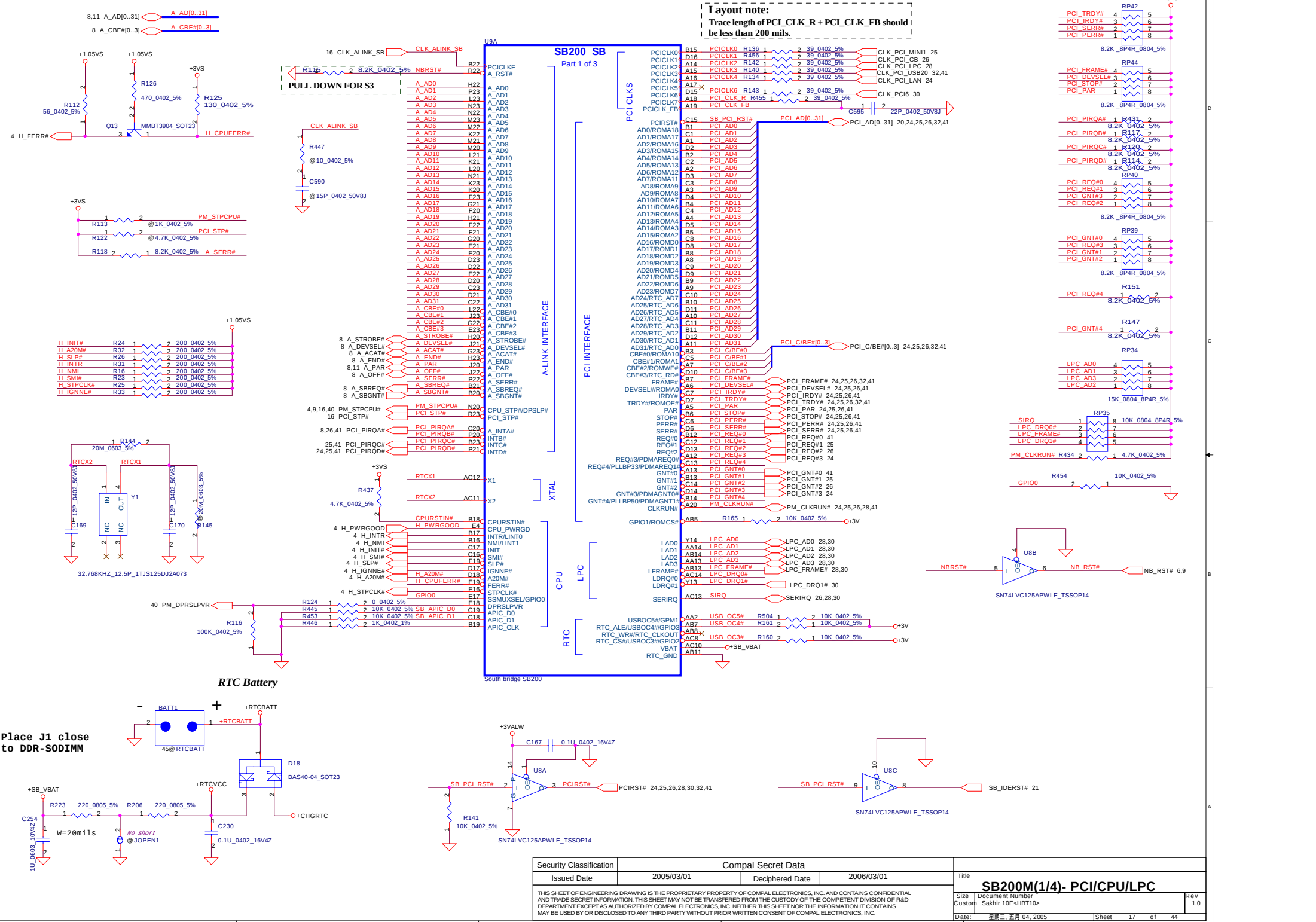
FS4	FS3	FS2	FS1	FS0	CPU	MEM	With Spread Enabled...
0	0	0	1	0	200	200	Spread OFF OR Center spread +/-0.3%
0	0	0	0	1	133	133	
0	0	0	0	0	100	100	

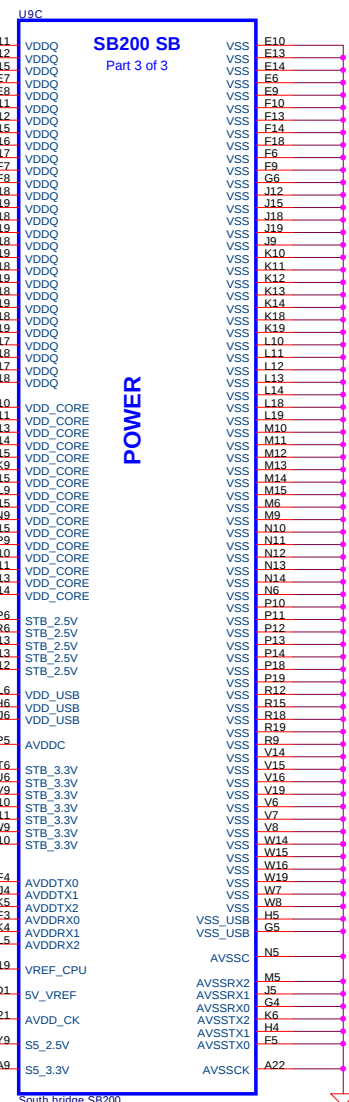
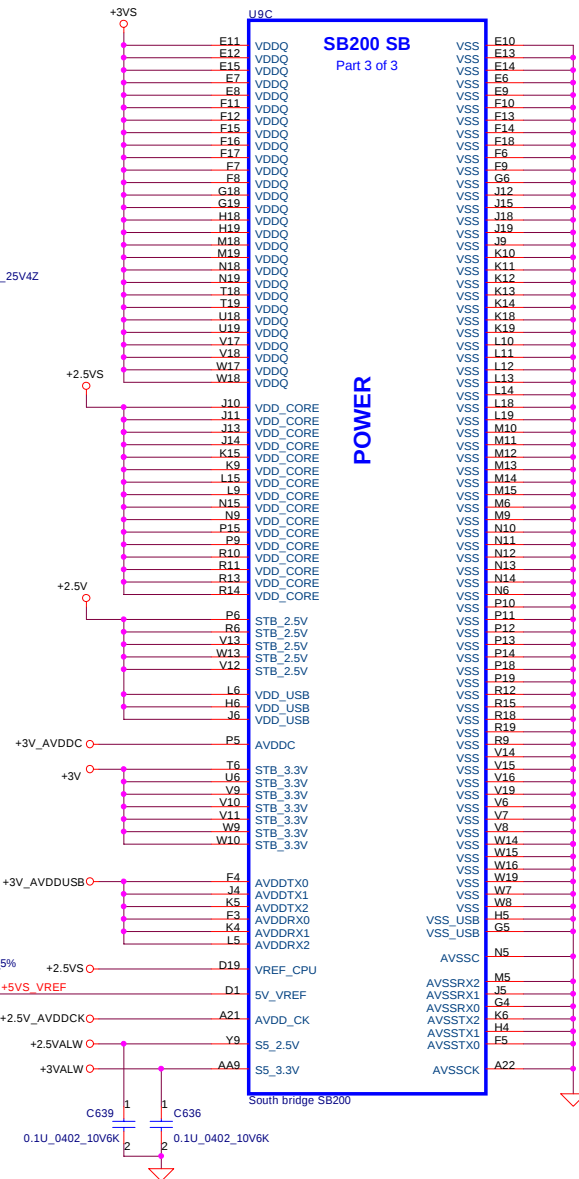
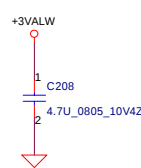
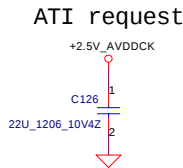
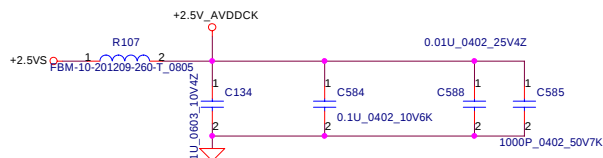
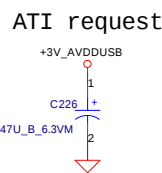
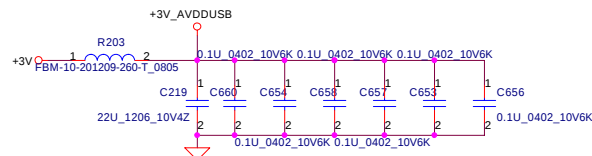
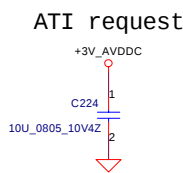
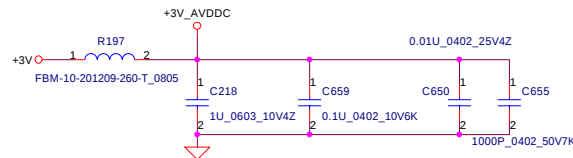
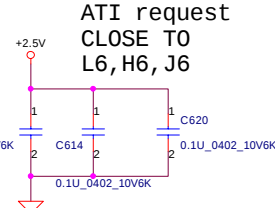
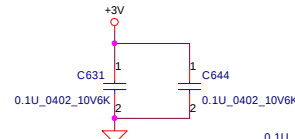
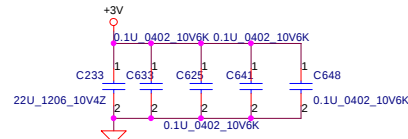
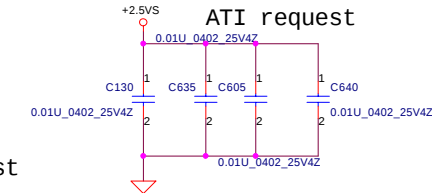
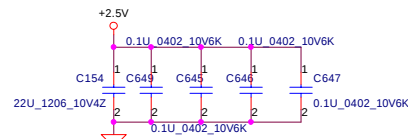
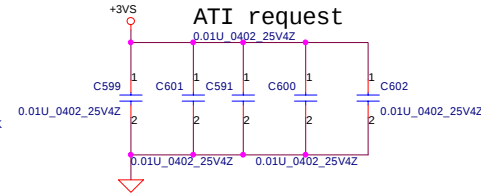
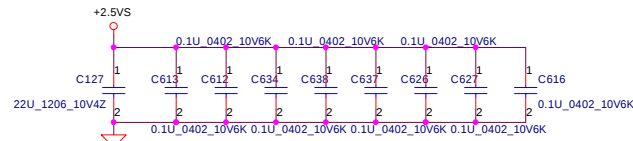
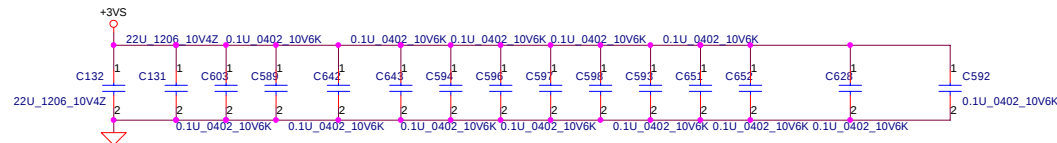
A-LINK FREQ

PCI33/66# = HIGH	66MHZ
PCI33/66# = LOW	33MHZ

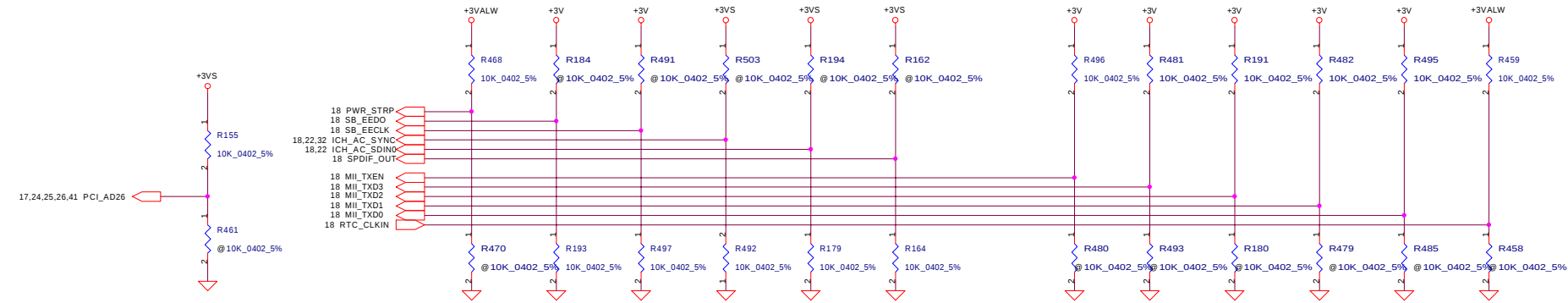
Note: 0 = PULL LOW
1 = PULL HIGH







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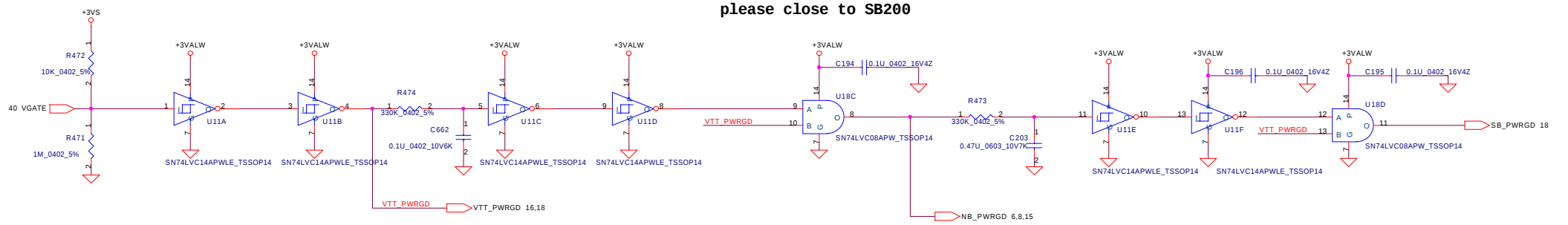


PCI_AD26 H: ENE910
L: NS87591

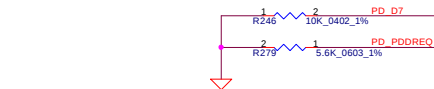
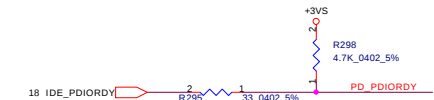
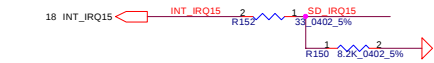
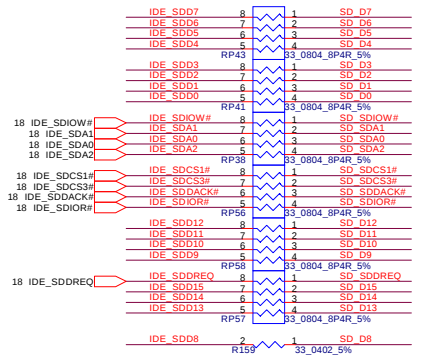
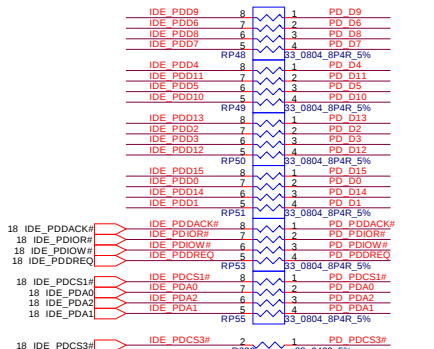
REQUIRED SYSTEM STRAPS

	PWR_STRP	IGN DEBUG EEDO	EECK	IAC_SYNC	IAC_SDAT0A	SPDIF_OUT	FREQOLTH TX_EN	ETHERNET TXD[3:0]	32KHZ S5 RTC_CLKIN
STRAP HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	ROM ON PCI BUS	INIT ACTIVE HIGH	33MHZ NB BUS	SIO 24MHz	DISABLE CPU FREQ SETTING DEFAULT	PROCESSOR FREQ MULTIPLIER	32KHZ OUTPUT FROM SB200 (INT RTC) DEFAULT
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	ROM ON LPC BUS DEFAULT	INIT ACTIVE LOW (PIII) DEFAULT	HI SPEED A-LINK DEFAULT	SIO 48MHz DEFAULT	ENABLE CPU FREQSETTING		32KHZ INPUT TO SB200 (EXT RTC)

please close to SB200

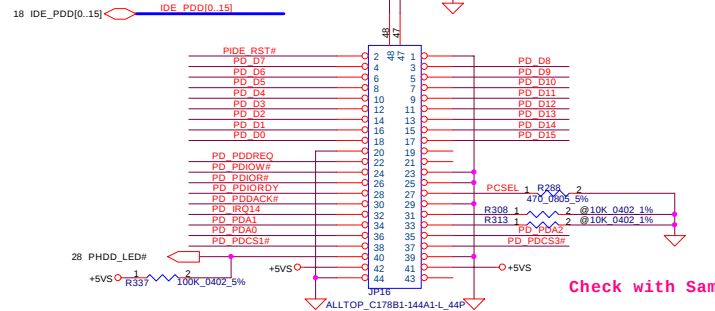


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Size	Document Number		Customer		Date	
	Sakhr 10E<HBT10>				星期三, 2005	1.0
Date:		星期三, 2005		Sheet 20 of 44		



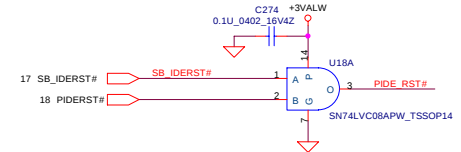
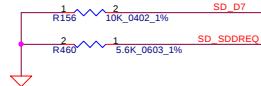
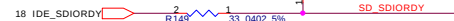
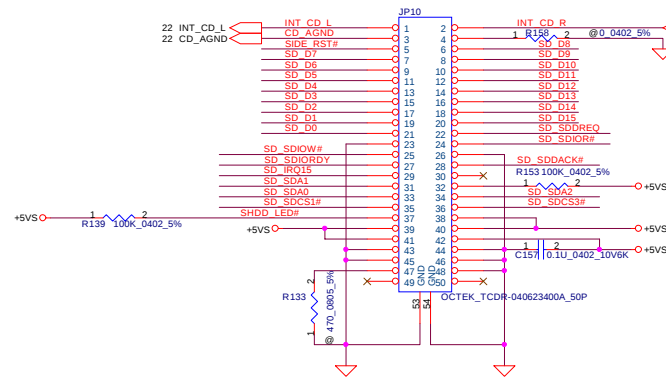
Should place close to SB side

HDD CONNECTOR

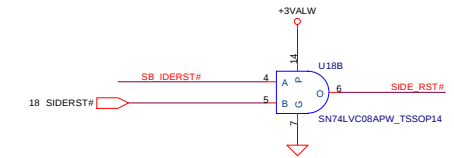


Check with Sam

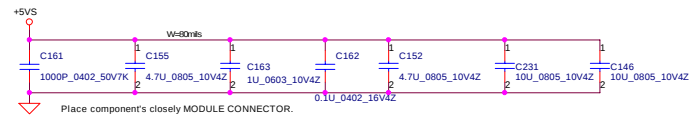
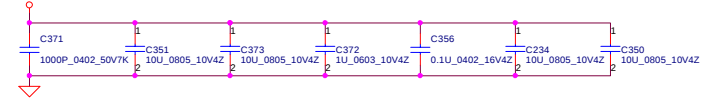
Check with ME new connector and Pin 1



Place U11 near SB side



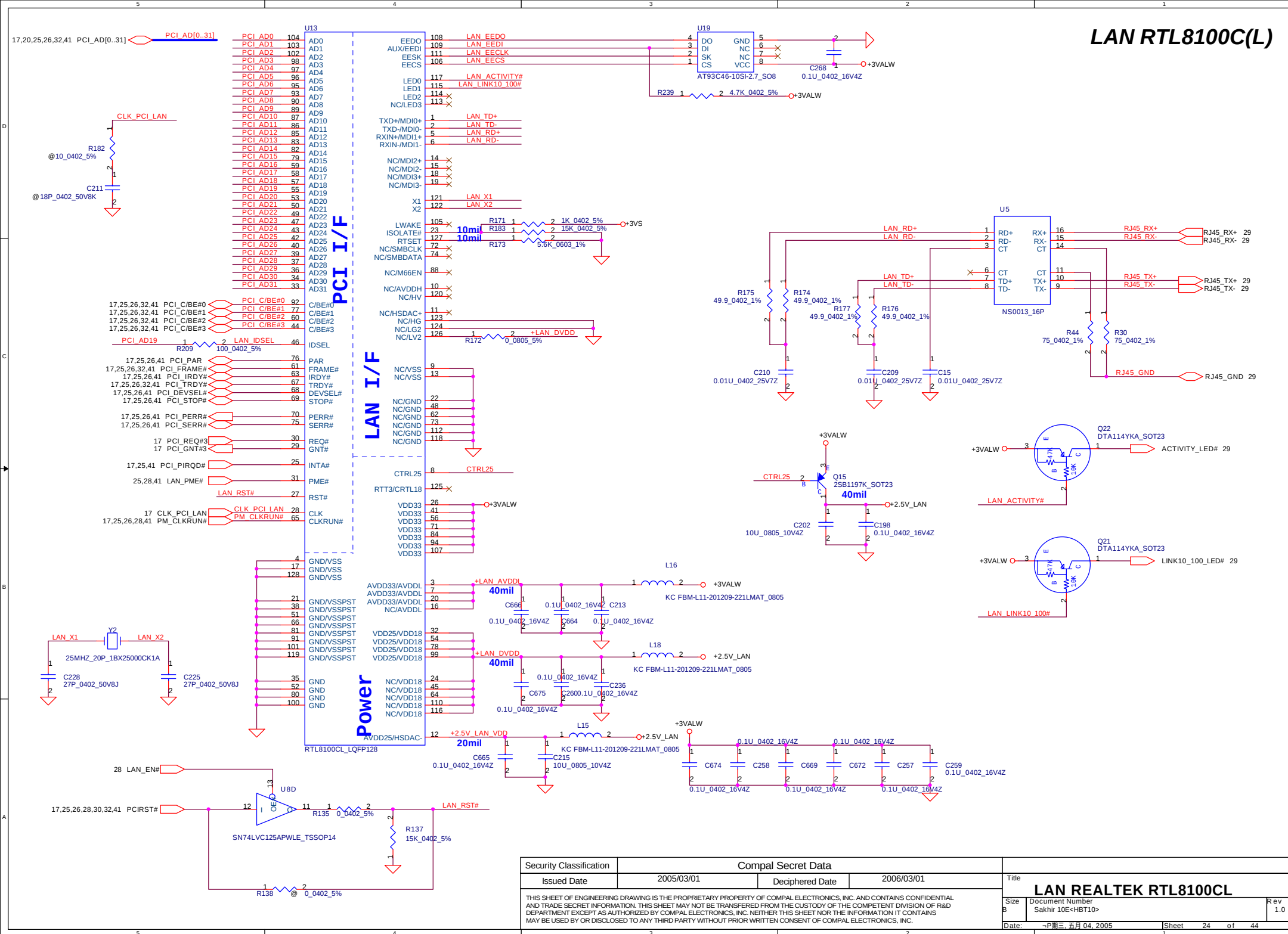
Place caps. near HDD CONN.

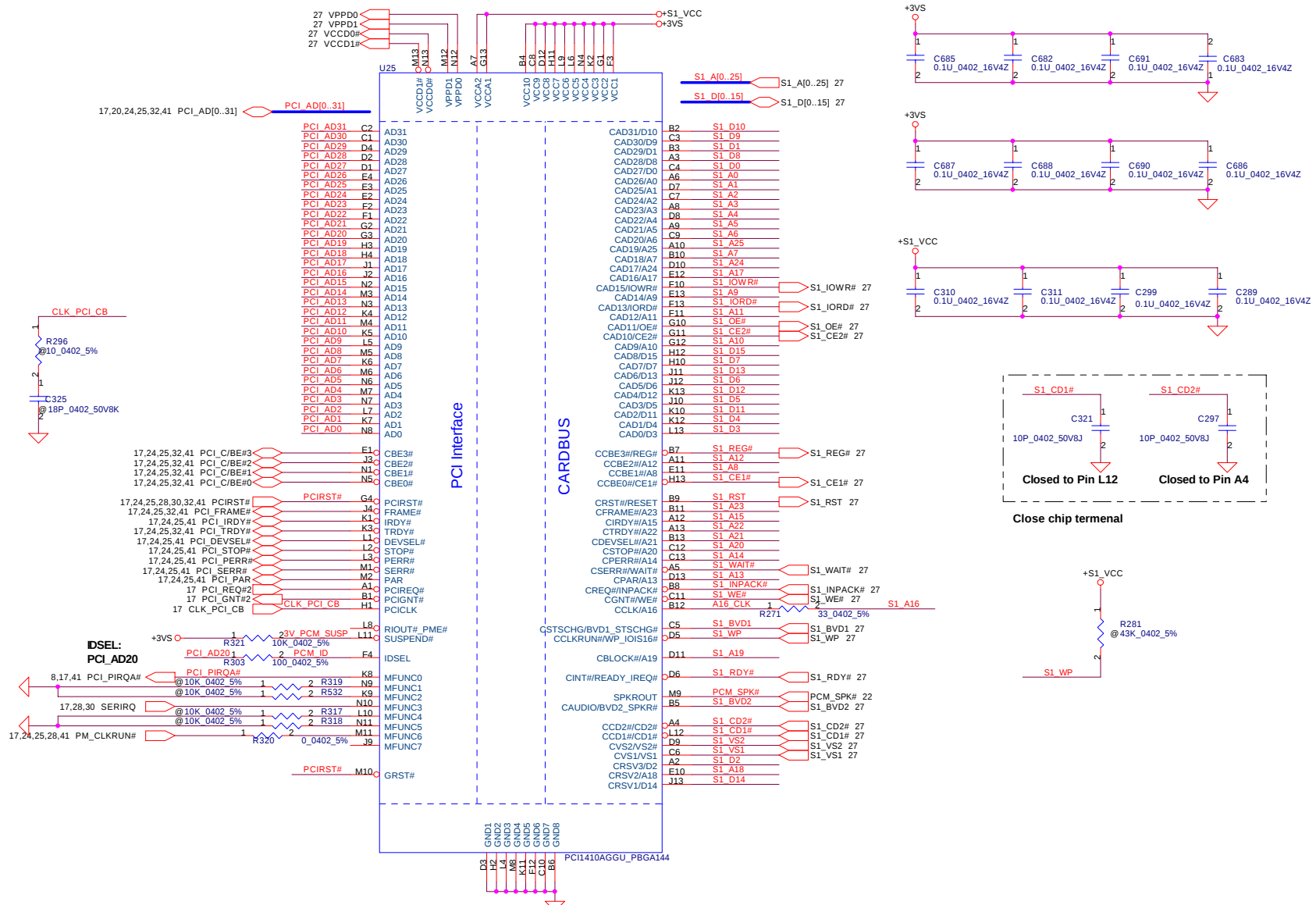


Place component's closely MODULE CONNECTOR.

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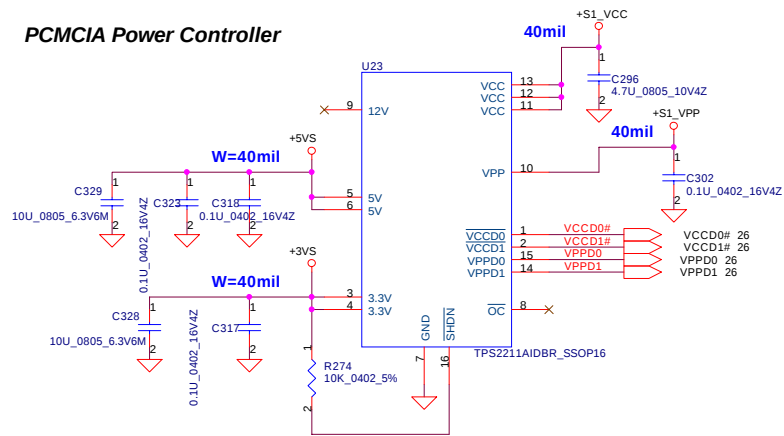
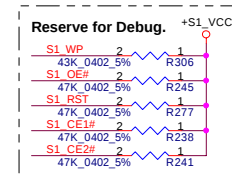
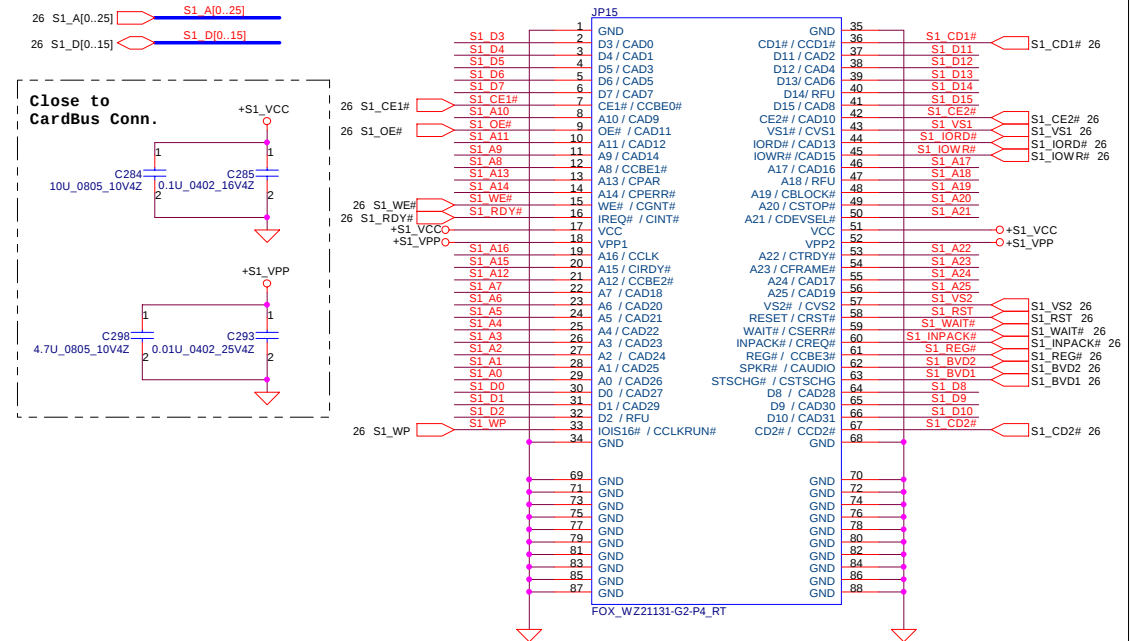
LAN RTL8100C(L)



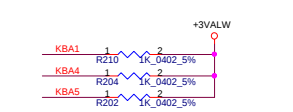
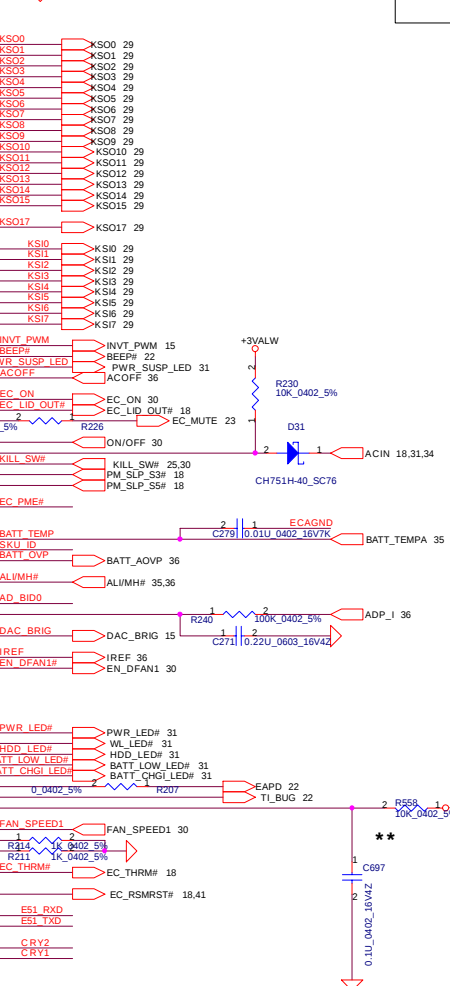
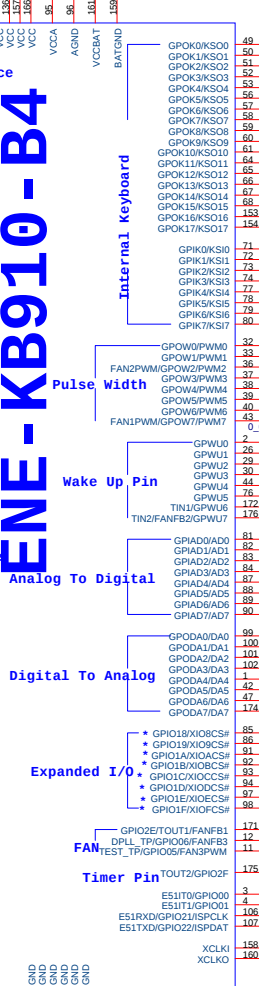
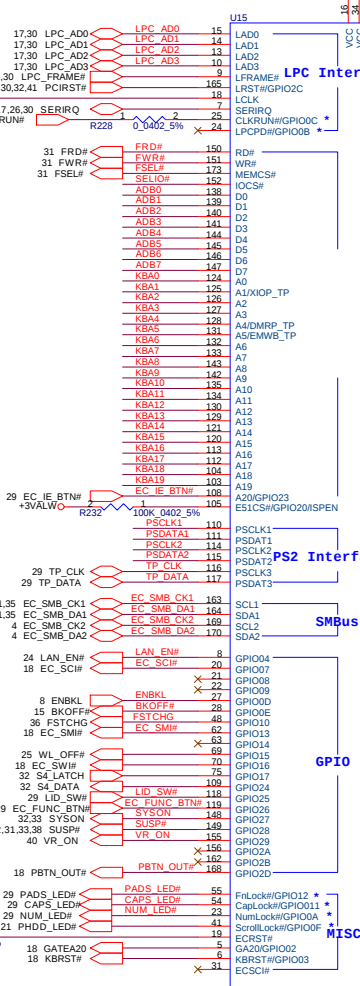
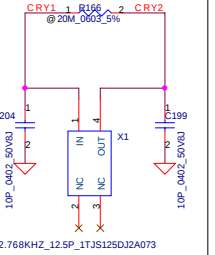
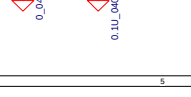
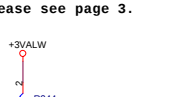
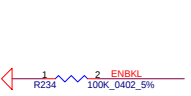
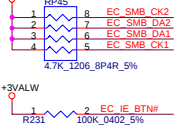
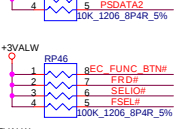
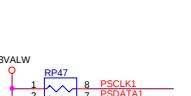
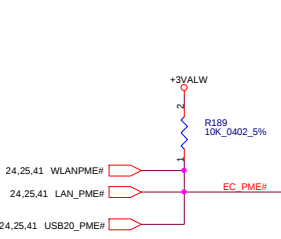
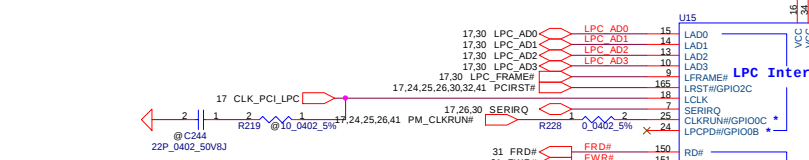
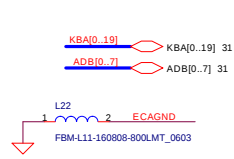


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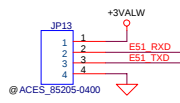
PCMCIA Power Controller

**CardBus Socket**

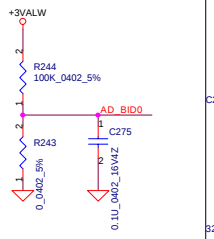
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				Size Custom	Document Number Saknr 10E<HBT10>	Rev 1.0
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For EC Tools



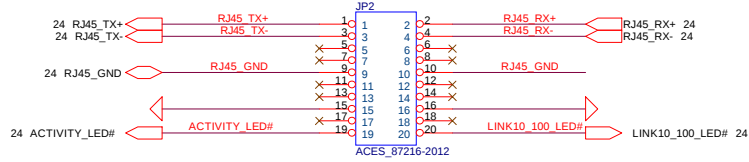
Analog Board ID definition, Please see page 3.



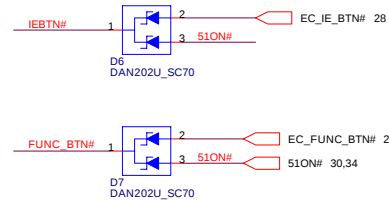
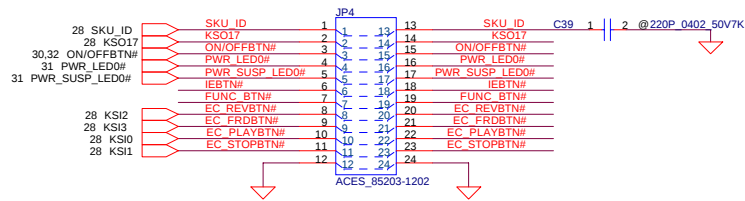
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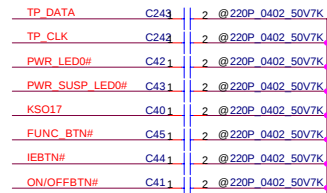
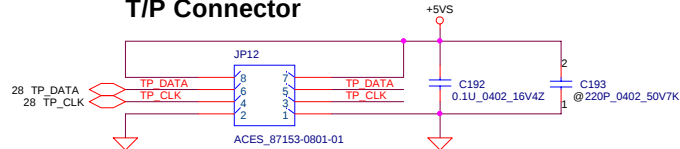
RJ45 Board Conn.



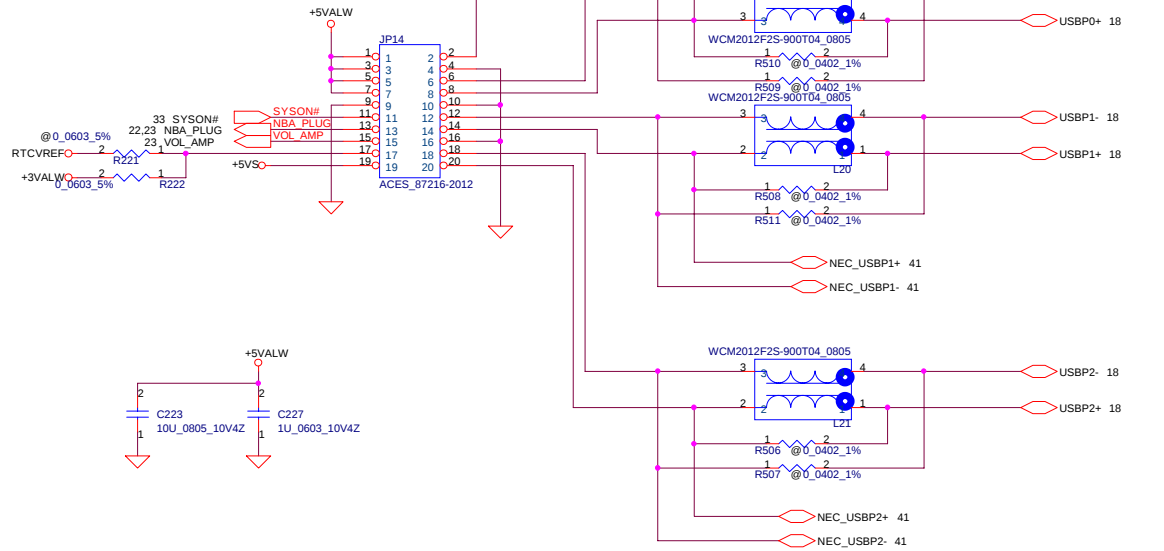
Power / LED Board Conn.



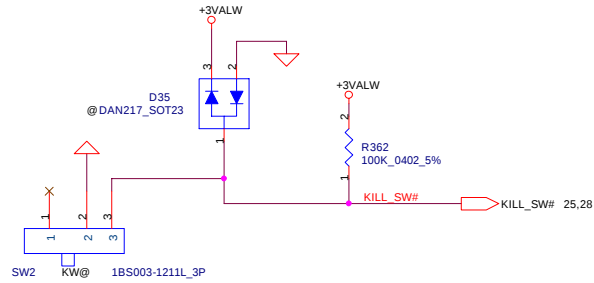
T/P Connector



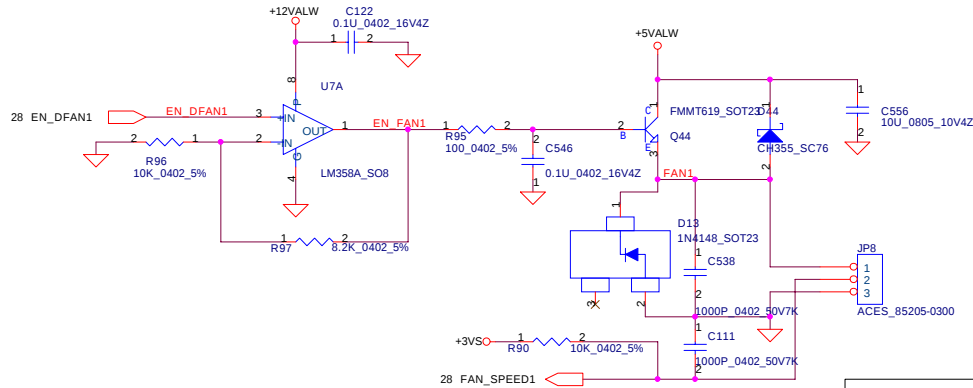
USB Board Conn.



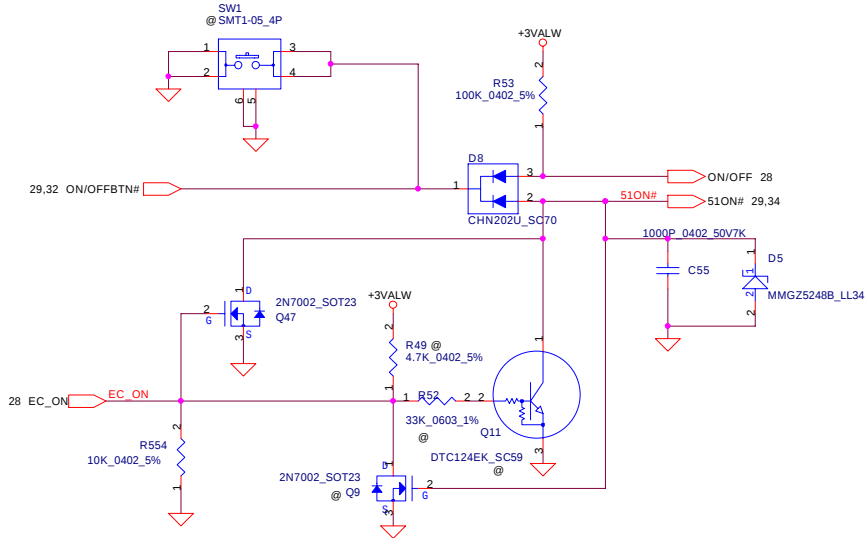
Kill SWITCH



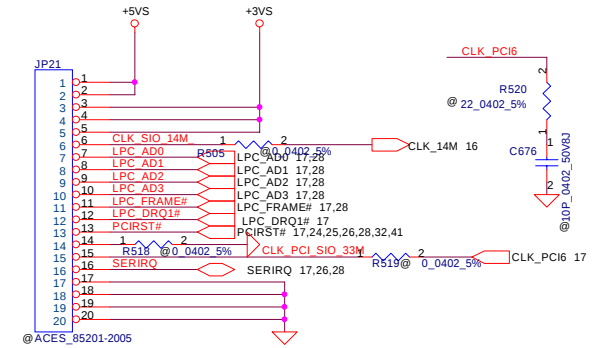
FAN CONN.



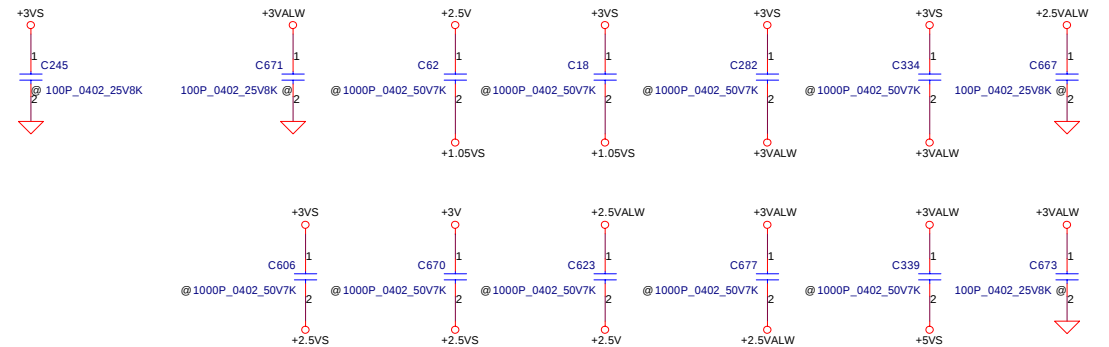
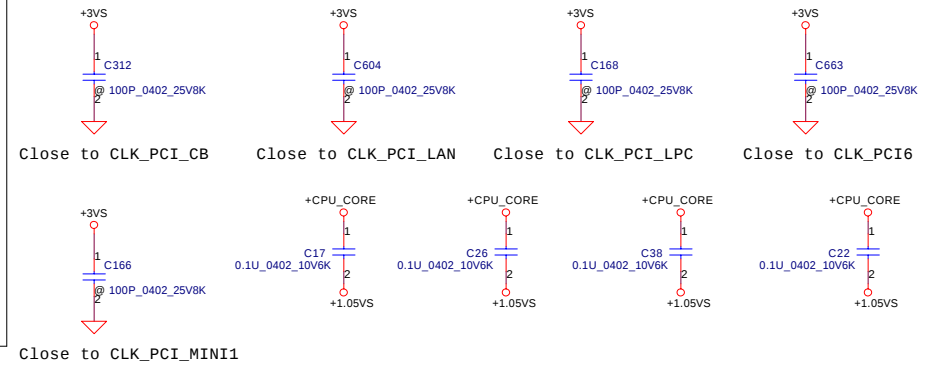
Power Button



LPC Debug Port

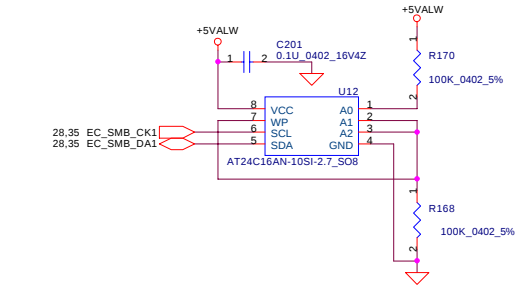


For EMI solution

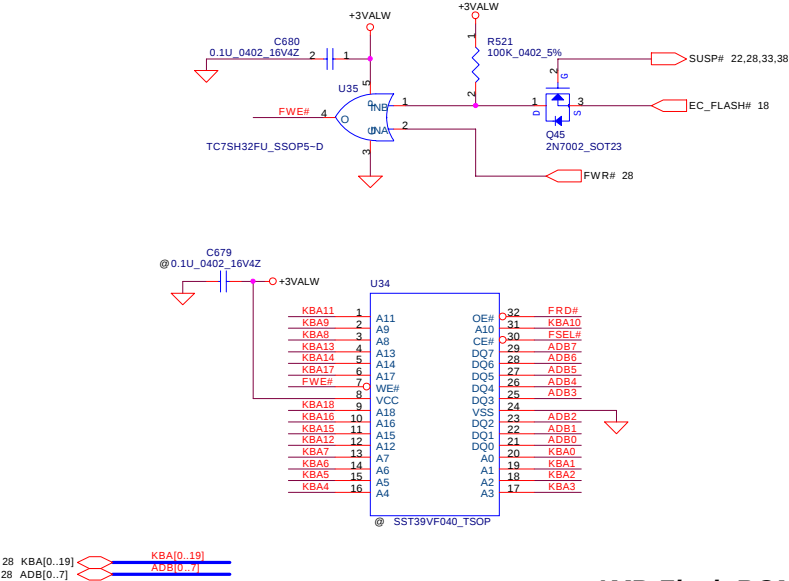


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Switches & Connectors			

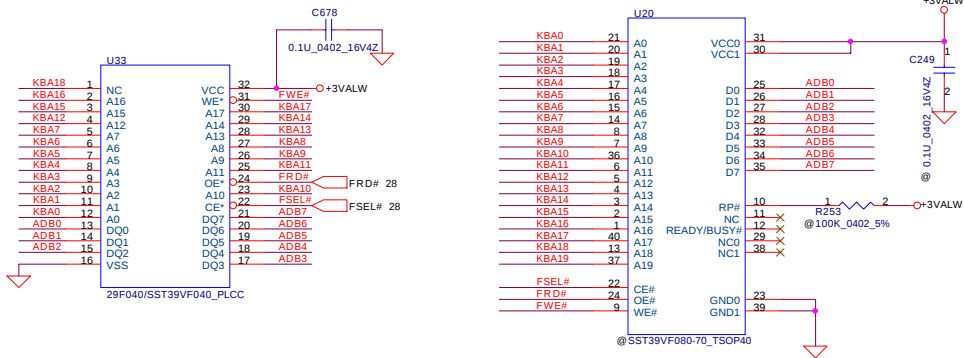
SMBus EEPROM



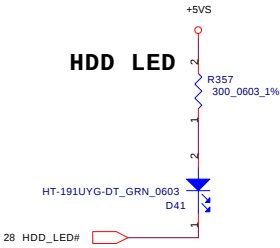
System BIOS



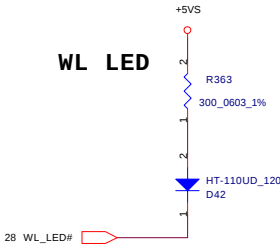
1MB Flash ROM



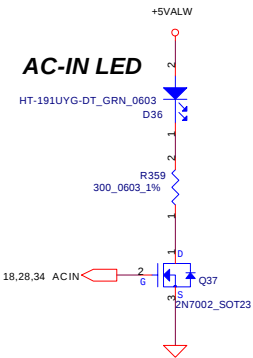
HDD LED



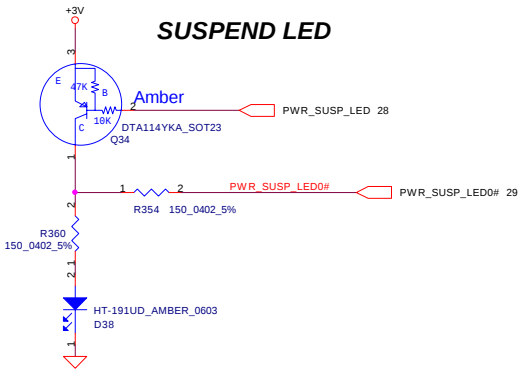
WL LED



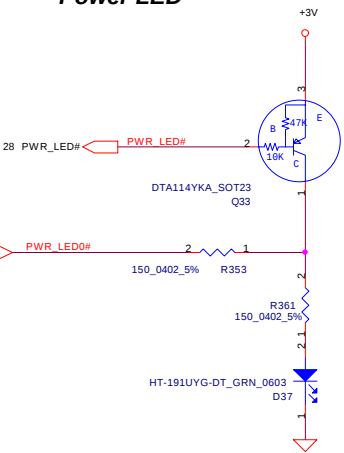
AC-IN LED



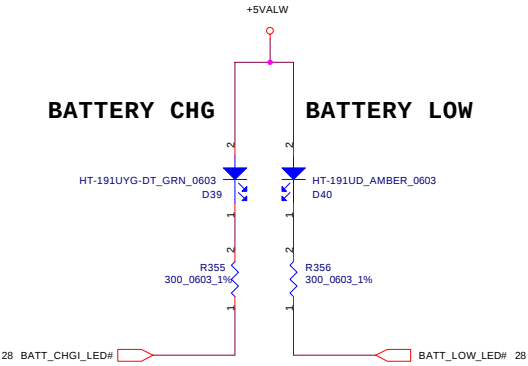
SUSPEND LED



Power LED

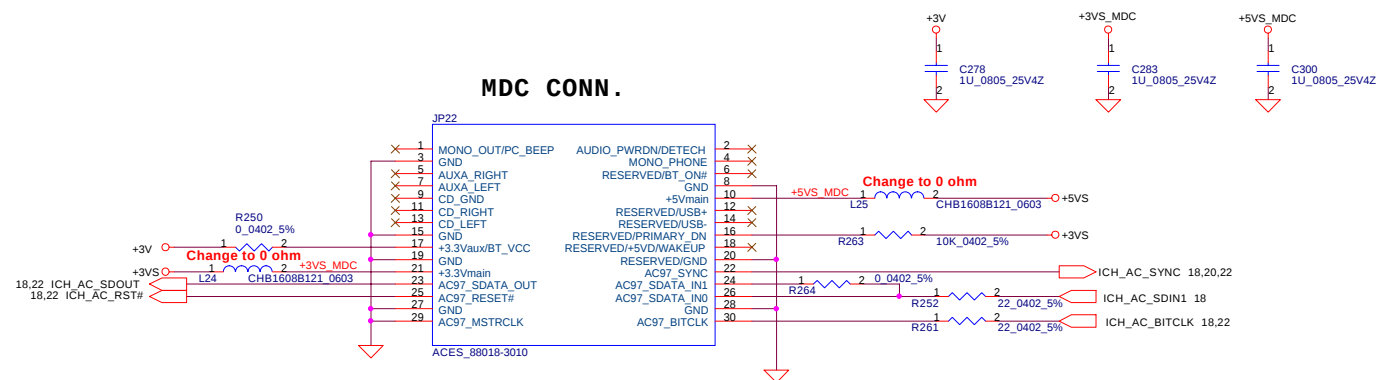
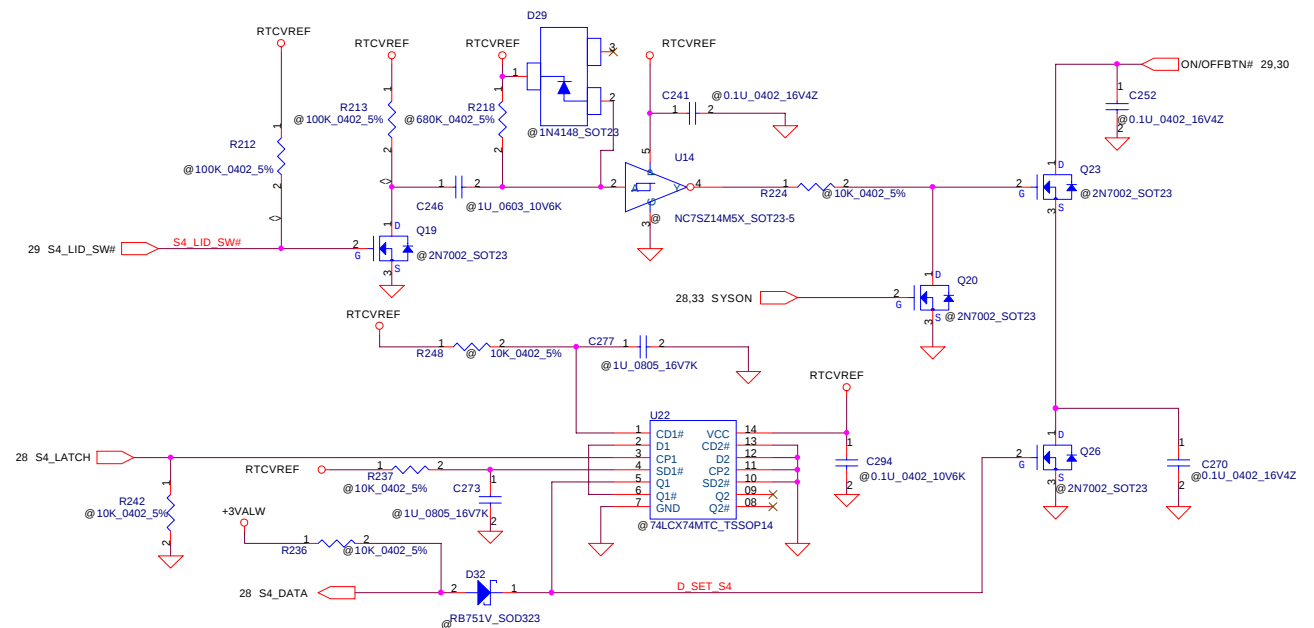
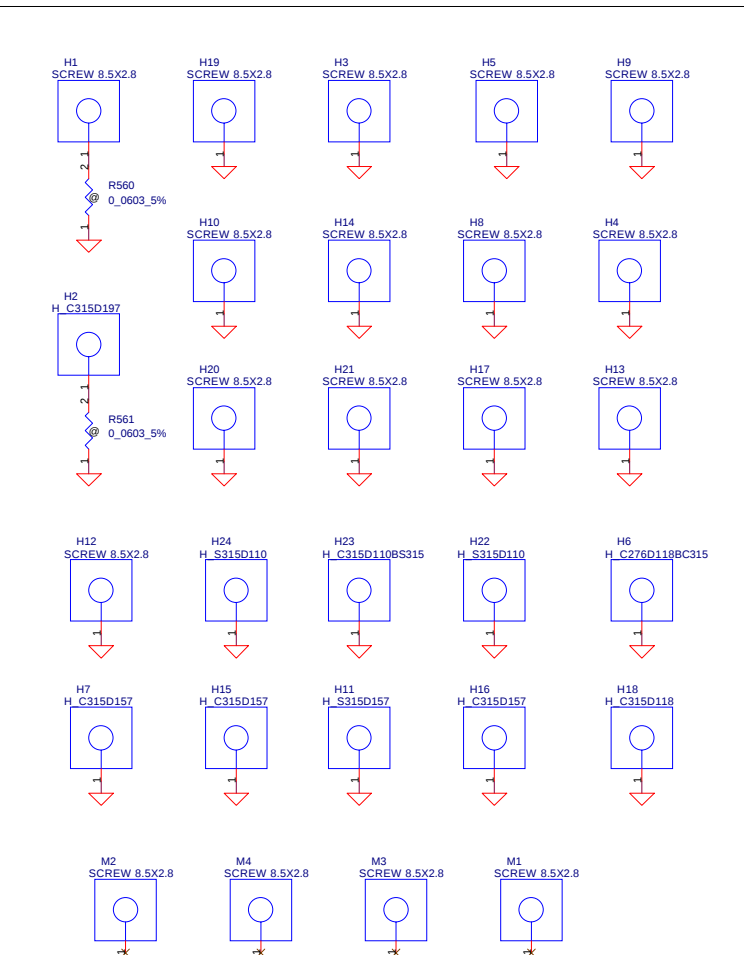
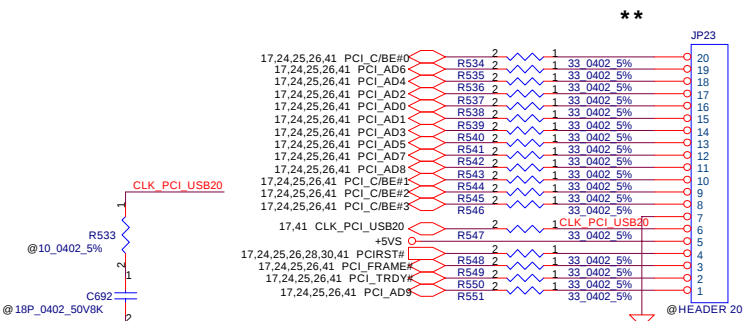


Battery LED

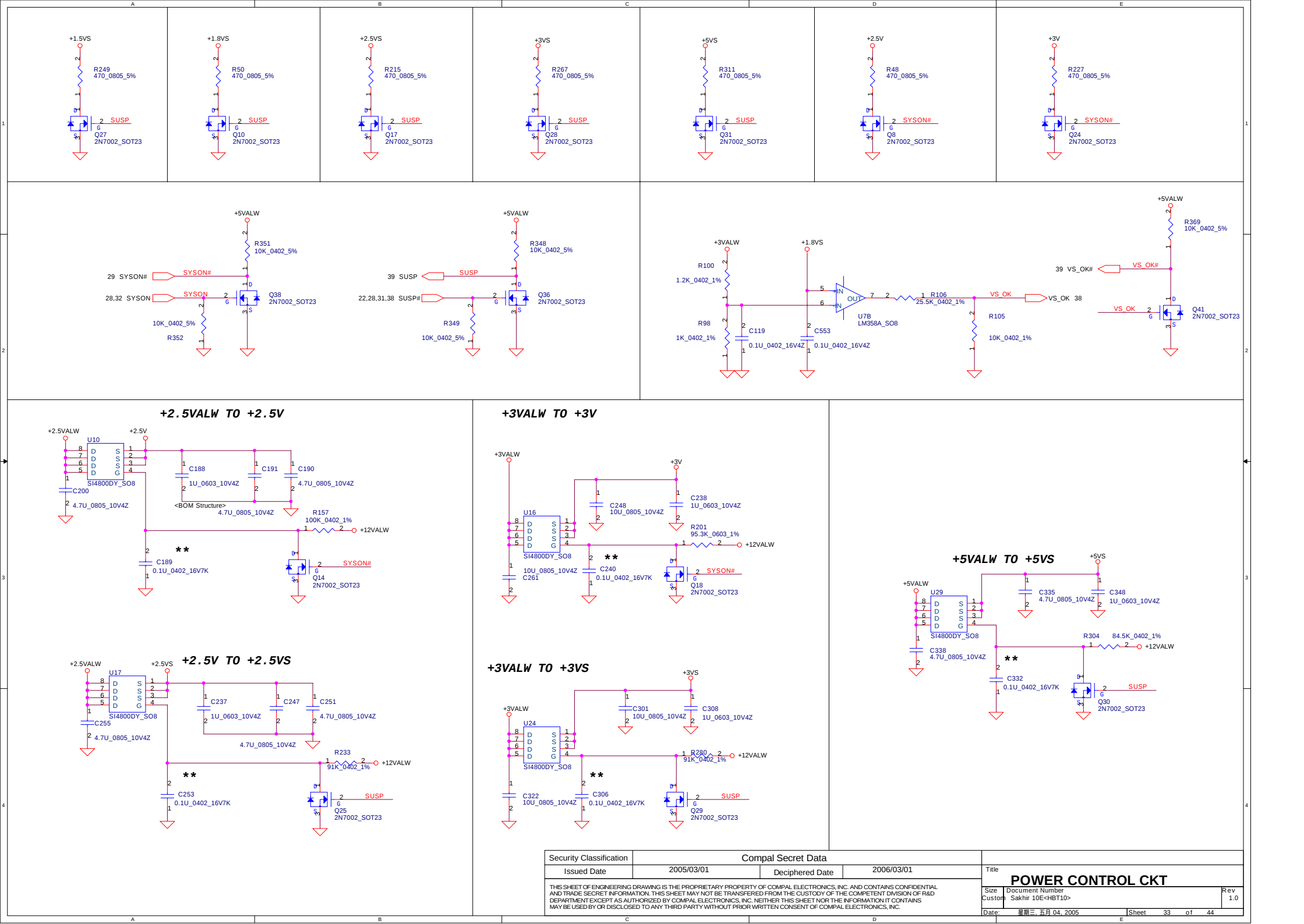


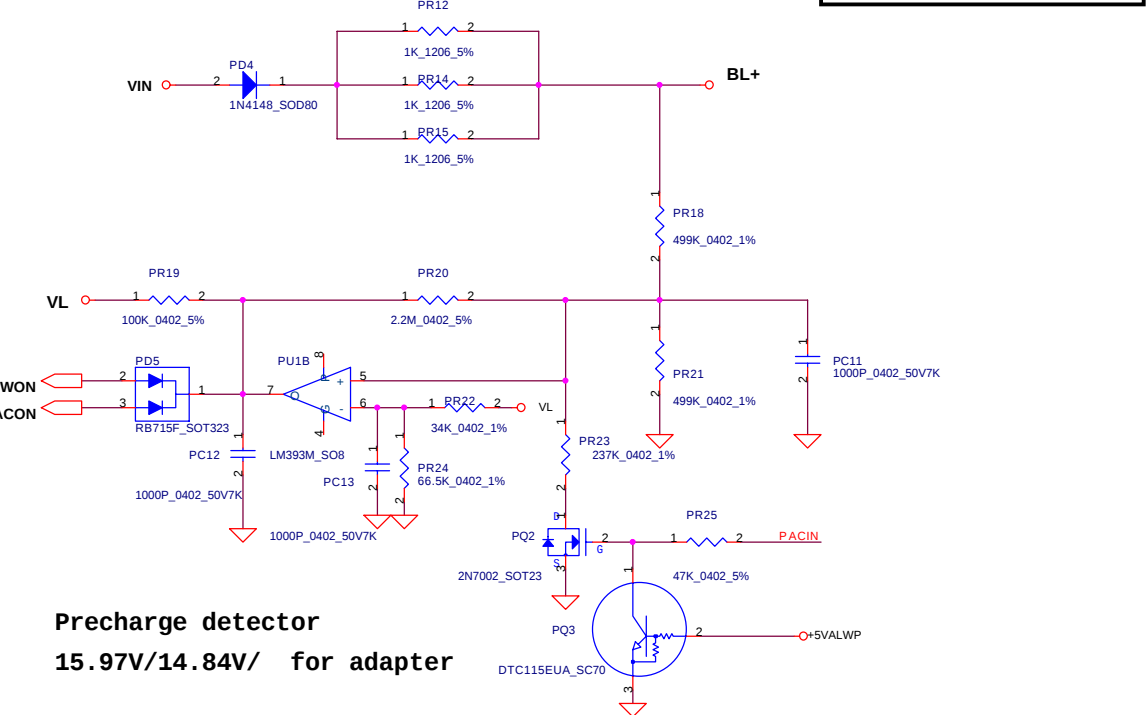
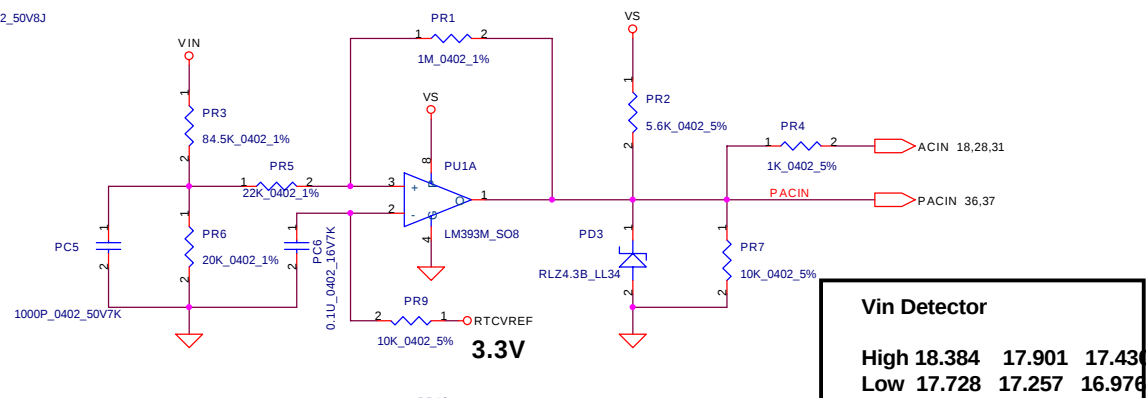
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				Date:	星期三, 五月 04, 2005	Sheet	31 of 44

Port 80 Debug Card Connector



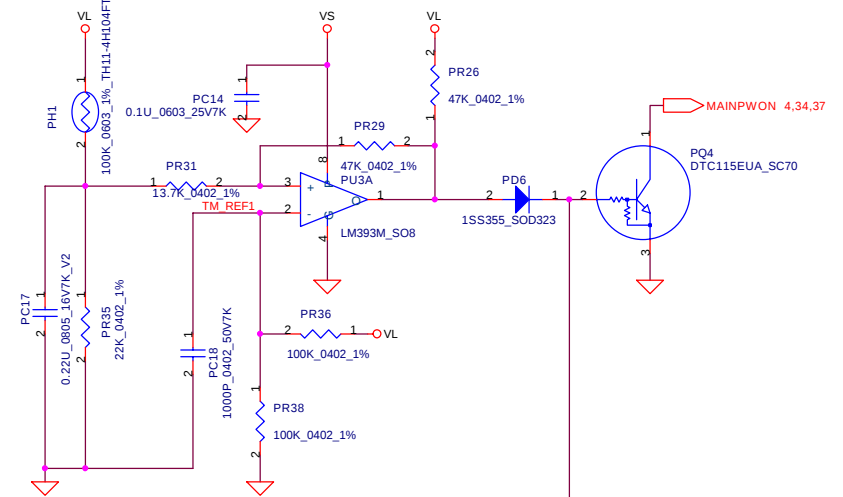
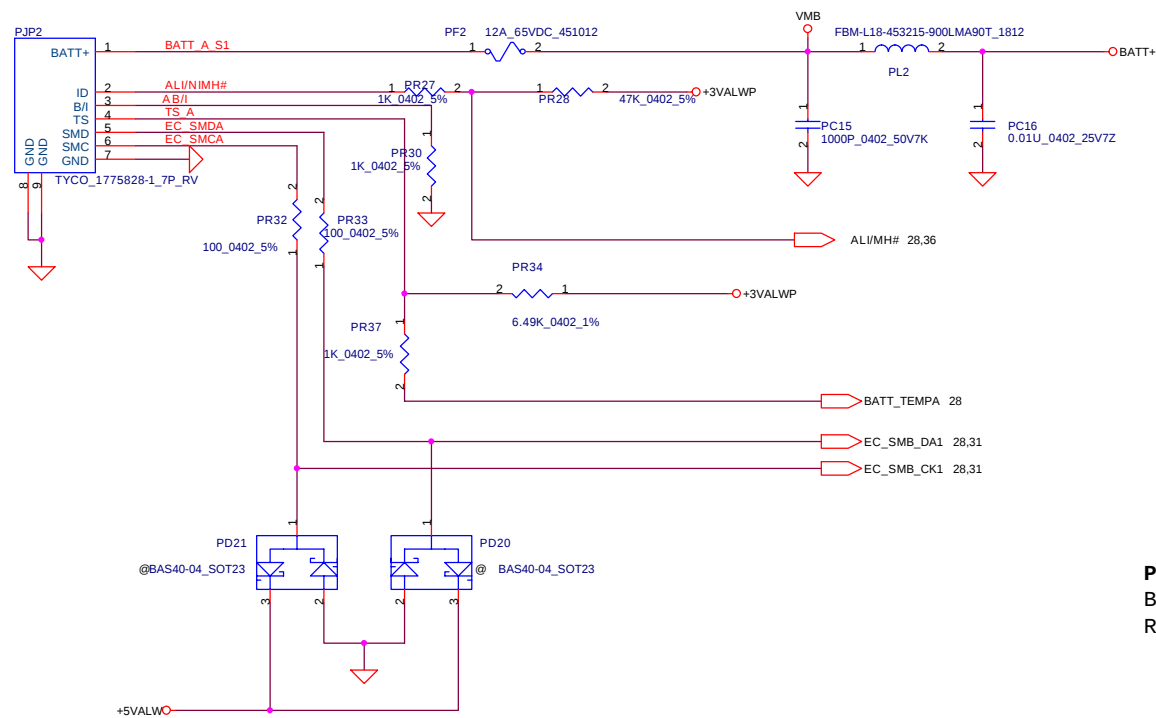
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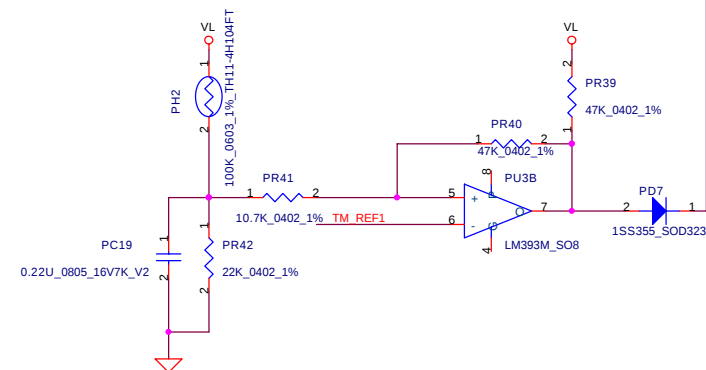


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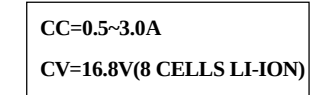
PH1 under CPU botten side :
CPU thermal protection at 84 degree C
Recovery at 45 degree C



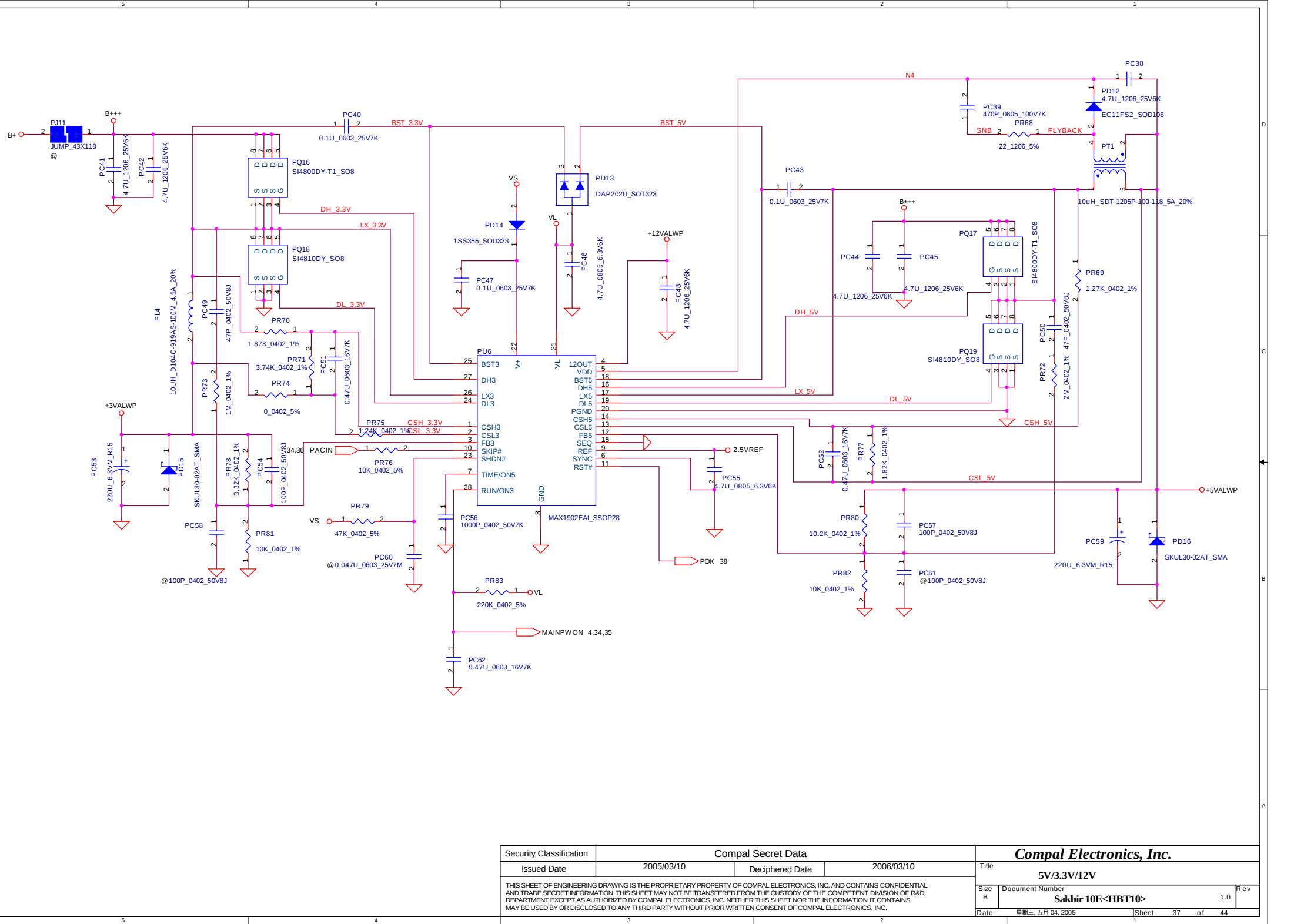
PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 45 degree C



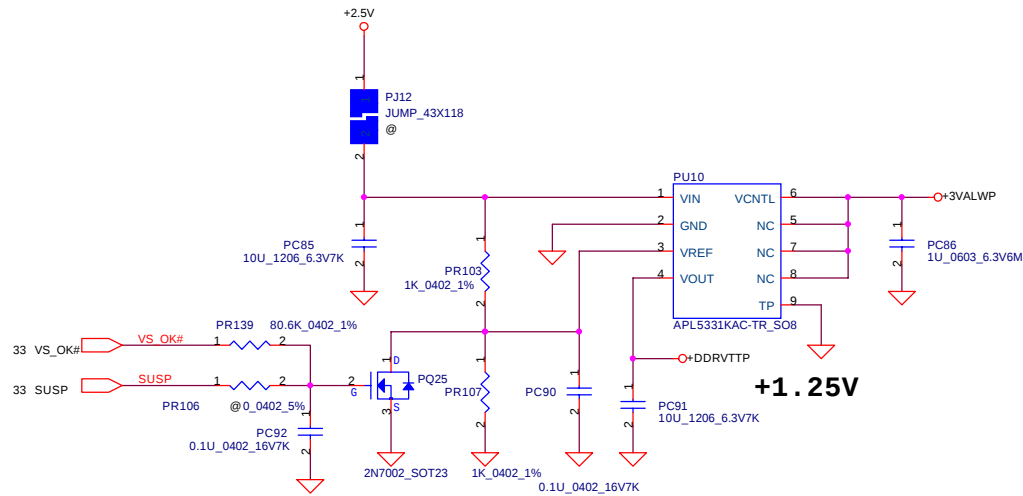
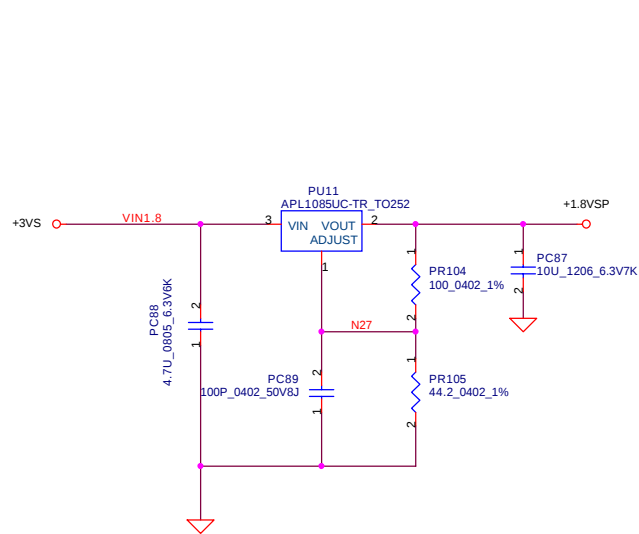
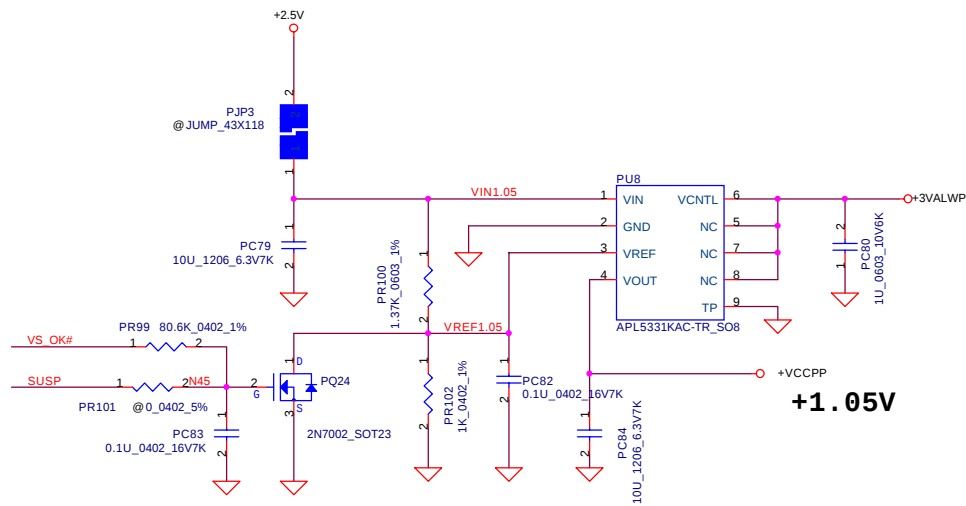
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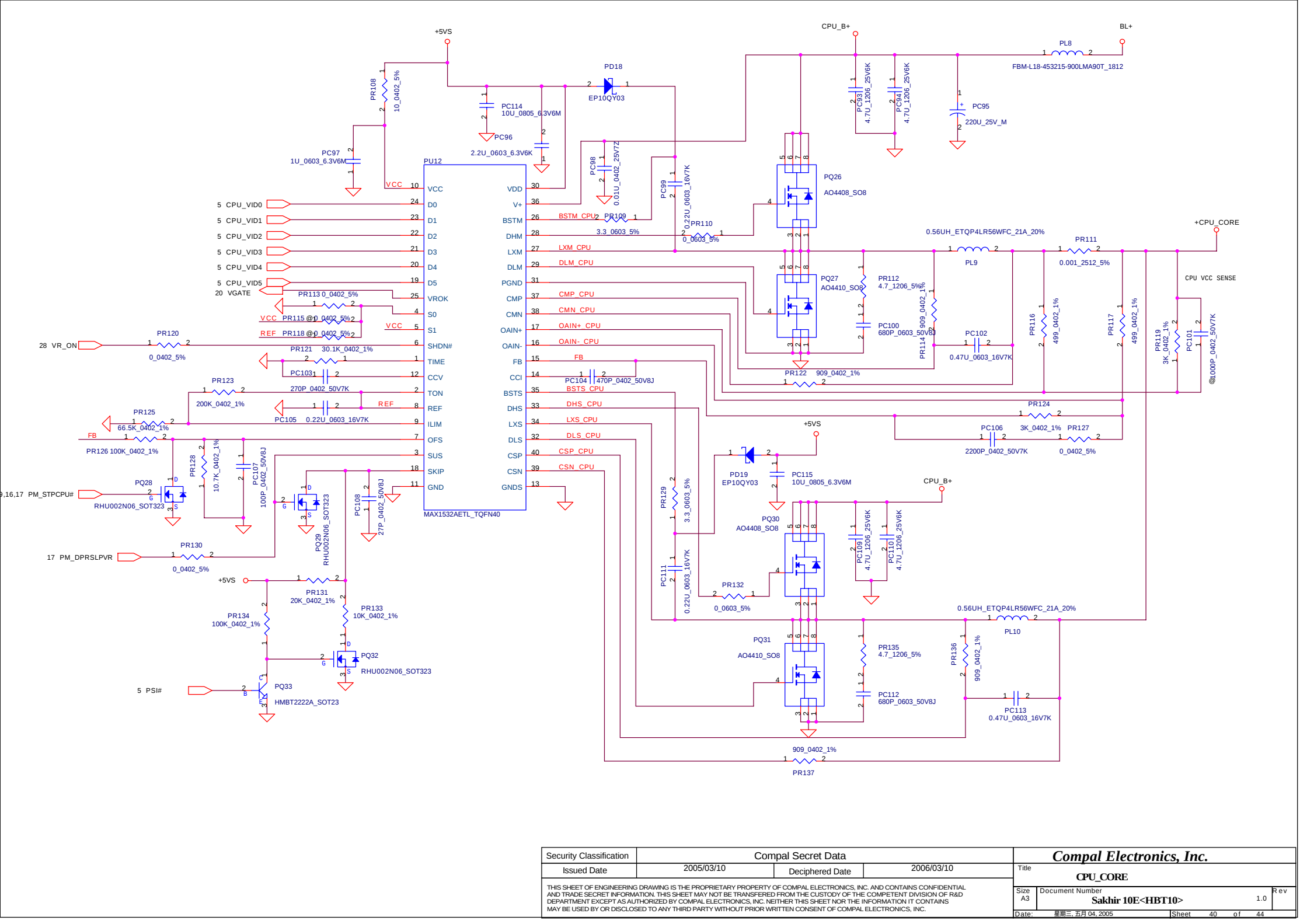
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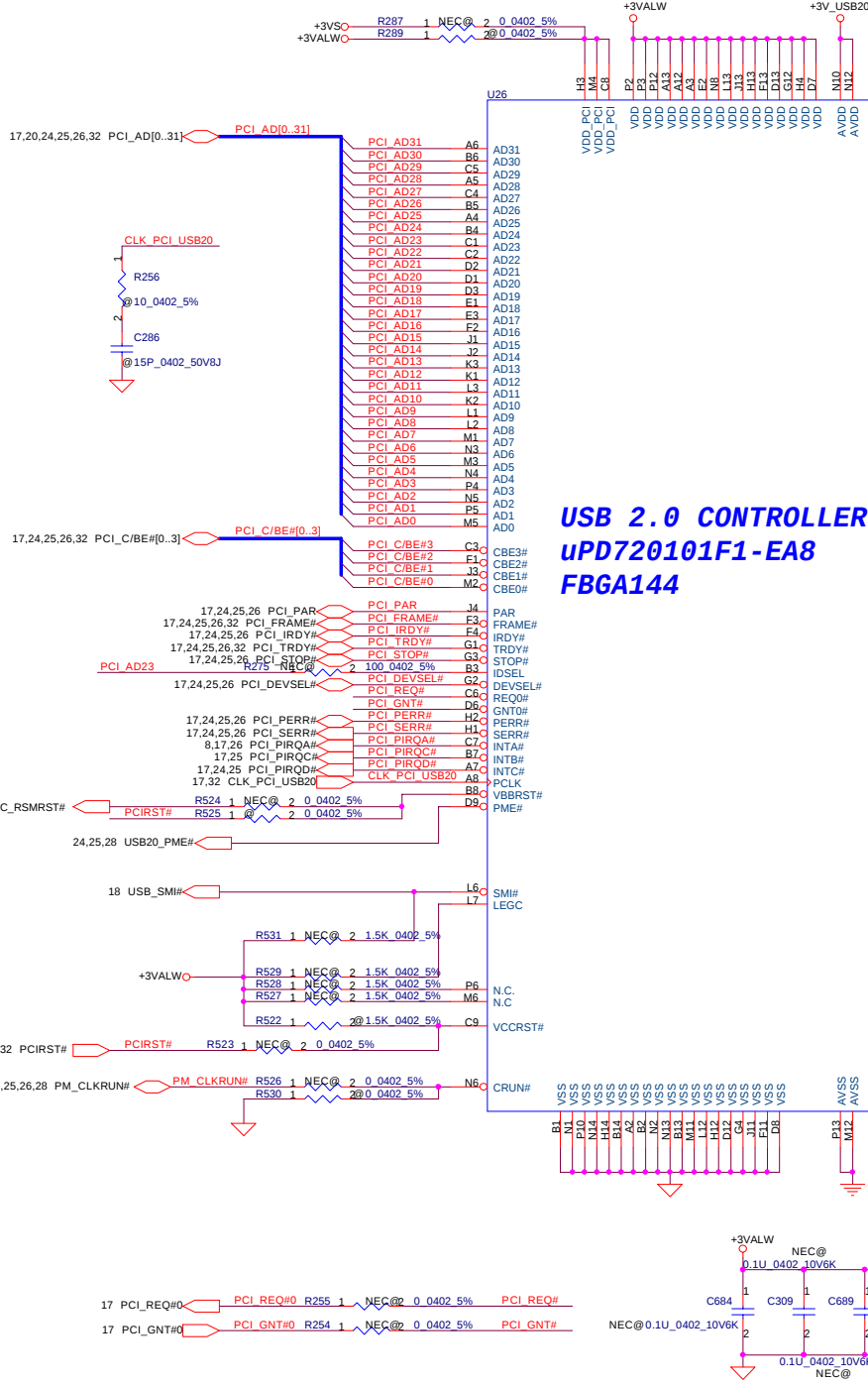
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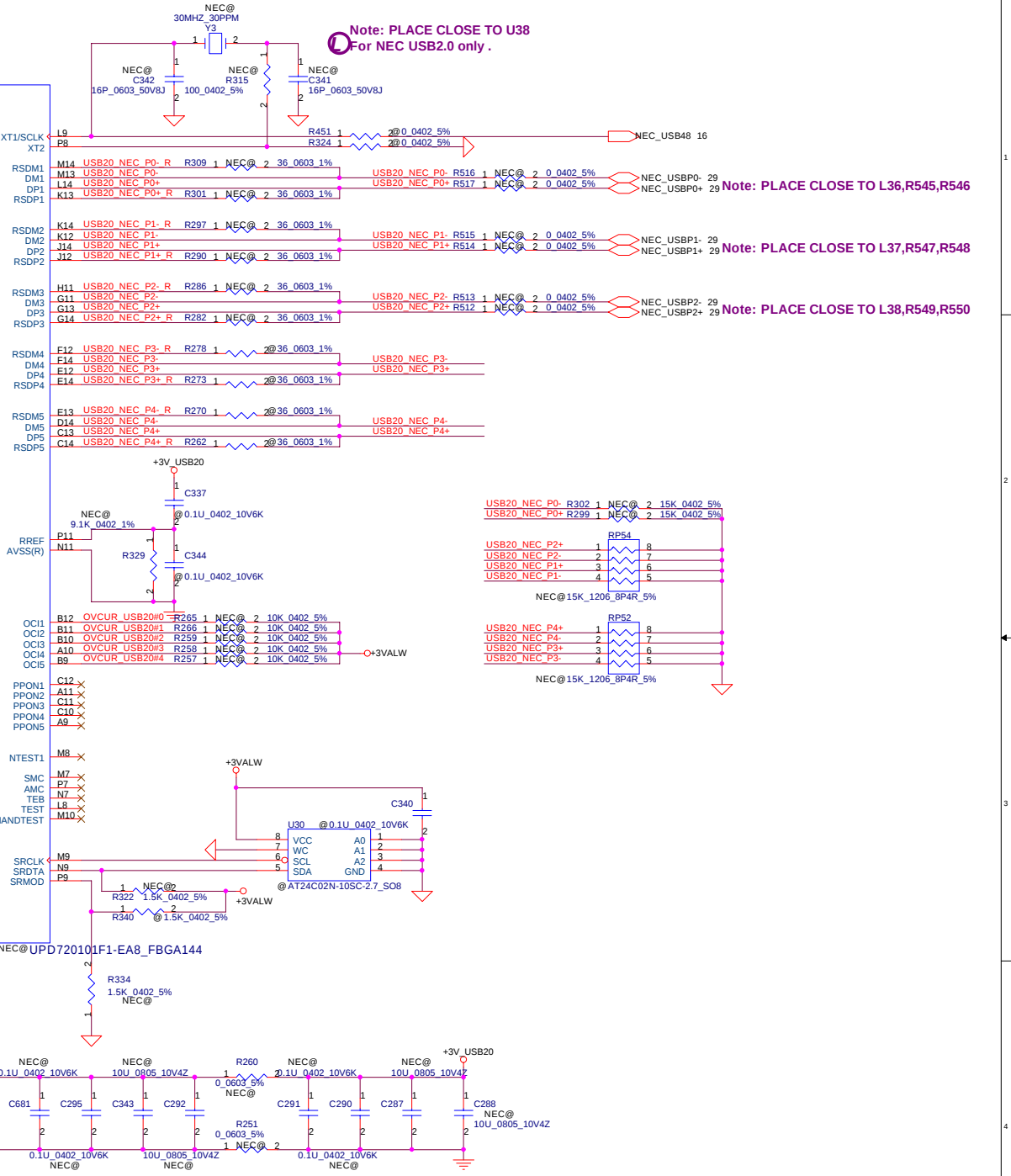
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USB 2.0 CONTROLLER
uPD720101F1-EA8
FBGA144



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Version Change List (P. I. R. List) for HW Circuit

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Version Change List (P. I. R. List) for Power Circuit

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Changed-List History-1			
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	LA-2811		1.0
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