

Compal confidential

Low Cost Los Angeles 10AL+

NBWAE LA-5831P Schematics Document

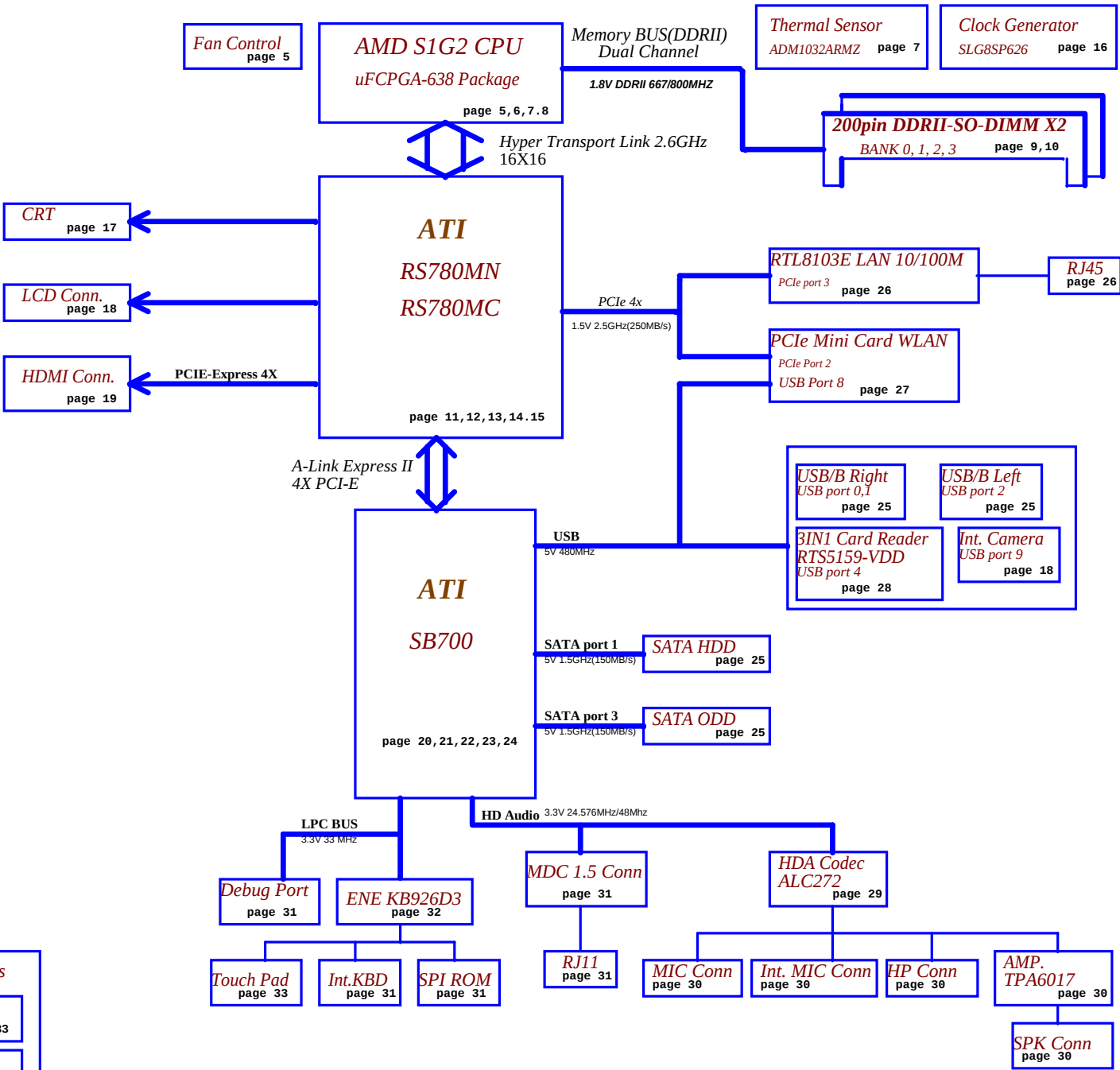
**Mobile AMD S1G2
RS780MN & RS780MC / SB700
2009-08-12 Rev. 1.0**

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2009-02-12	Deciphered Date	2009-02-12	Cover Sheet	
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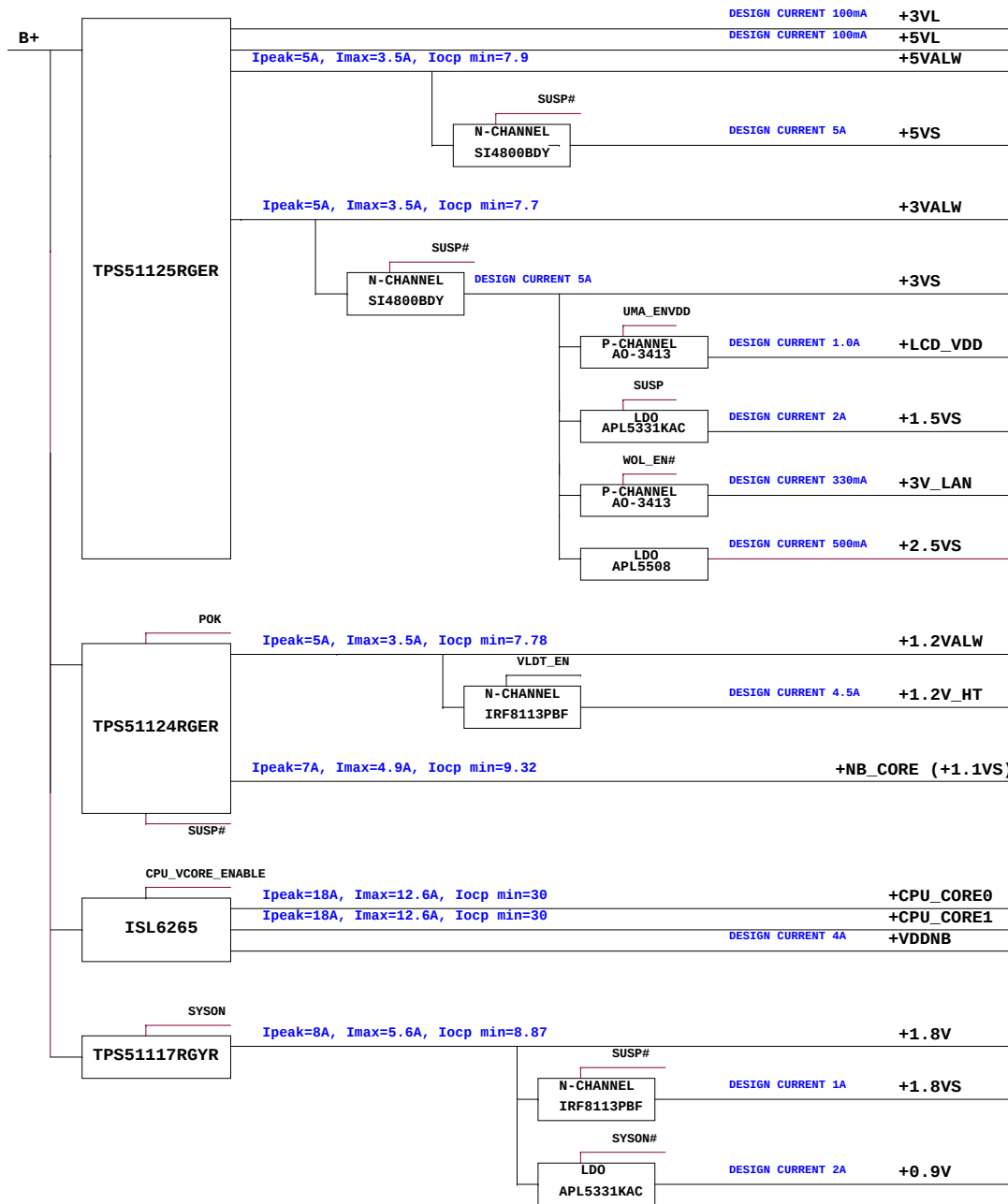
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Model Name : NBWAE

File Name : LA-5831P



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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009-02-12	Deciphered Date	2009-02-12	Title	Power Map
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Voltage Rails

O : ON
X : OFF

State \ power plane				
	B+ +3VL +5VL +RTCVCC	+5VALW +3VALW +1.2VALW +3V_LAN	+1.8V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +1.2V_HT +VDDNB +CPU_CORE_0 +CPU_CORE_1
	S0	0	0	0
	S1	0	0	0
	S3	0	0	X
	S5 S4/AC	0	0	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SB700 SM Bus0 Address				SB700 SM Bus1 Address			
Power	Device	HEX	Address	Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b	+3VALW	WLAN/WIMAX		
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b				
+3VS	Clock Generator	D2 H	1101 0010 b				

KB926 SM Bus1 Address				KB926 SM Bus2 Address			
Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 011X b	+3VS	CPU_ADM1032-1	98 H	1001 100X b
KB926 ESB Address							
	Power	Device	HEX	Address			
	+3VL	Cap. Sensor		Virtual I2C			

Platform	CPU	NB	SB
PUMA@	S1G2	RS780MC	SB700
	S1G2	RS780MN	SB700
TIGRIS@	S1G3	RS880MC	SB710
	S1G3	RS880M	SB710

@ : just reserve , no build

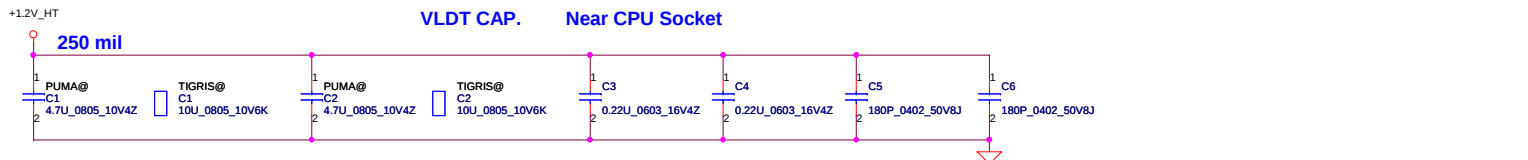
BTO (Build-To-Order) Option Table

Function	Modem	HDMI	CAMERA & MIC	
Description	(R)	(Y)	(X)	
Explain			CAMERA	MIC
BTO	MDC@	HDMI@	CAM@	MIC@

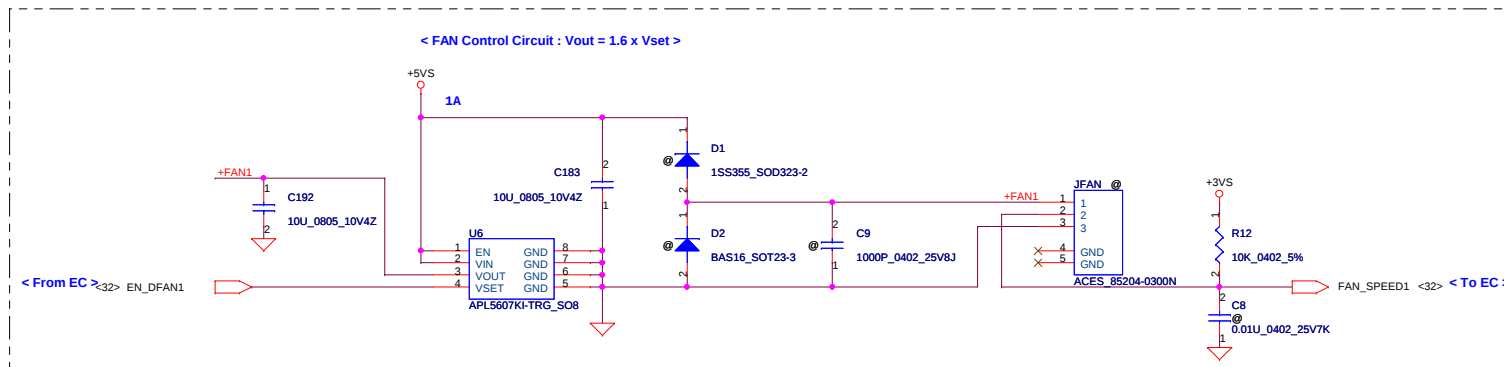
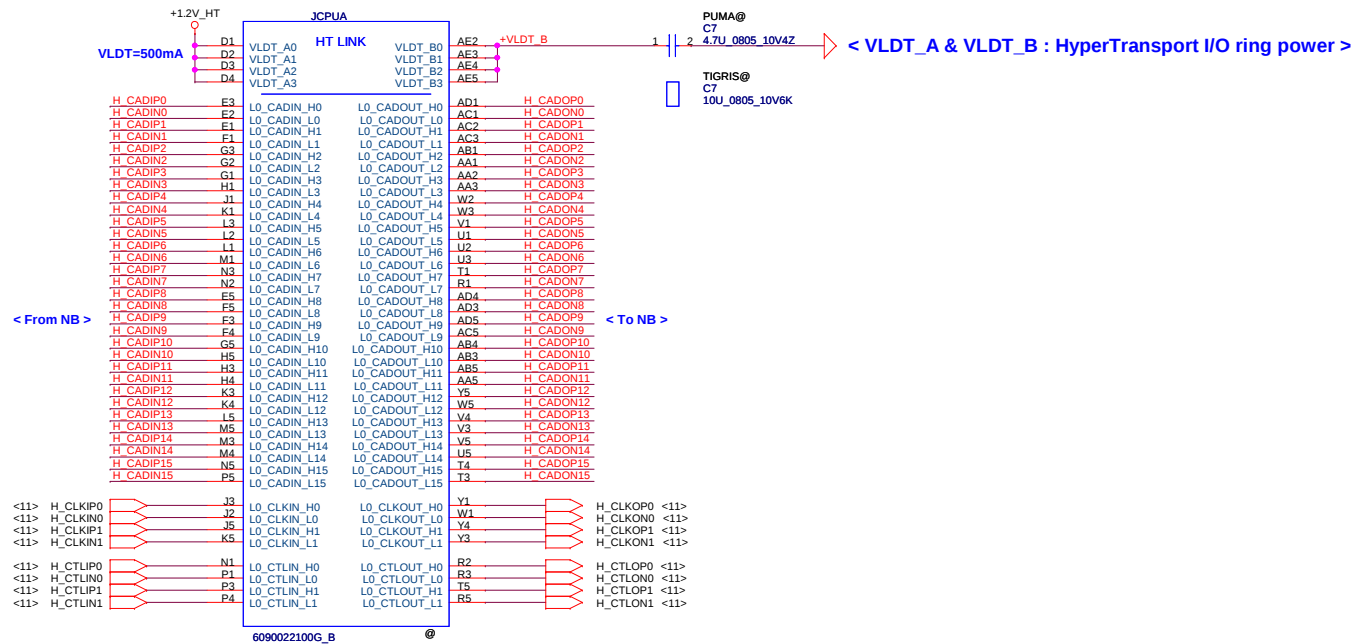
SMBUS Control Table

	SOURCE	INVERTER	BATT	HDMI CEC	CPU THERMAL SENSOR	SODIMM I / II	CLK GEN	WLAN	LCD DDC ROM	HDMI DDC ROM	NEW CARD
EC_SMB_CK1 EC_SMB_DA1	KB926		V								
EC_SMB_CK2 EC_SMB_DA2	KB926				V						
I2C_CLK I2C_DATA	RS780MN RS780MC								V		
DDC_CLK0 DDC_DATA0	RS780MN RS780MC									V	
DDC_CLK1 DDC_DATA1	RS780MN RS780MC										
SCL0 SDA0	SB700					V	V				
SCL1 SDA1	SB700							V			
SCL2 SDA2	SB700										
SCL3 SDA3	SB700										

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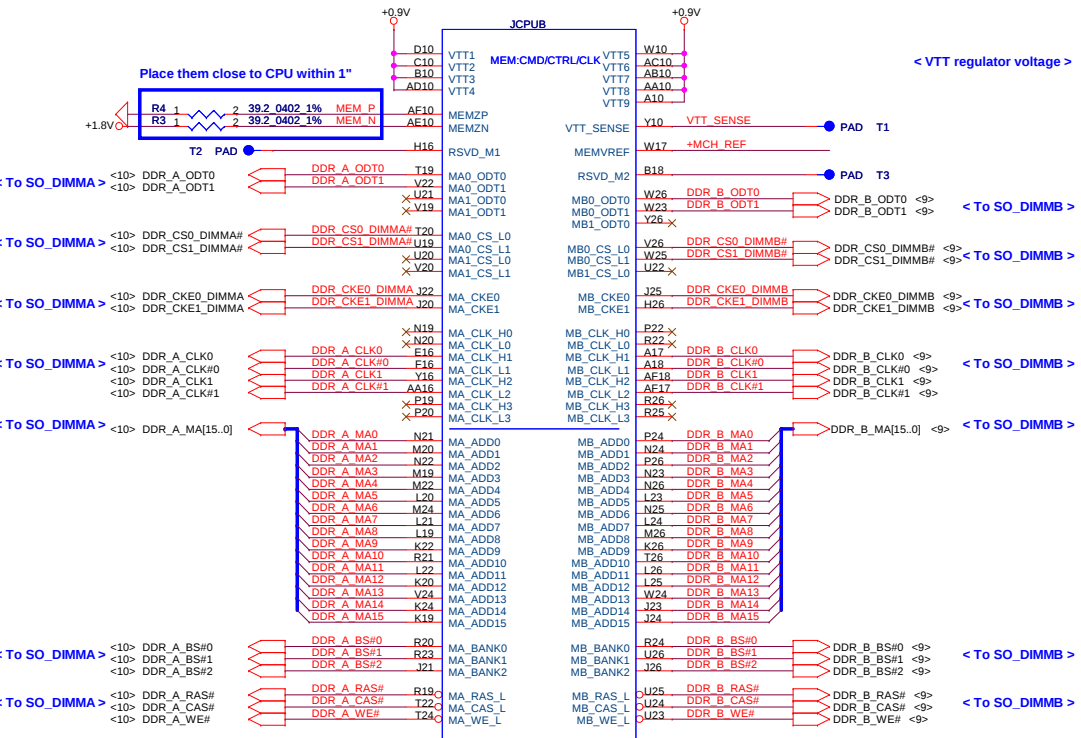
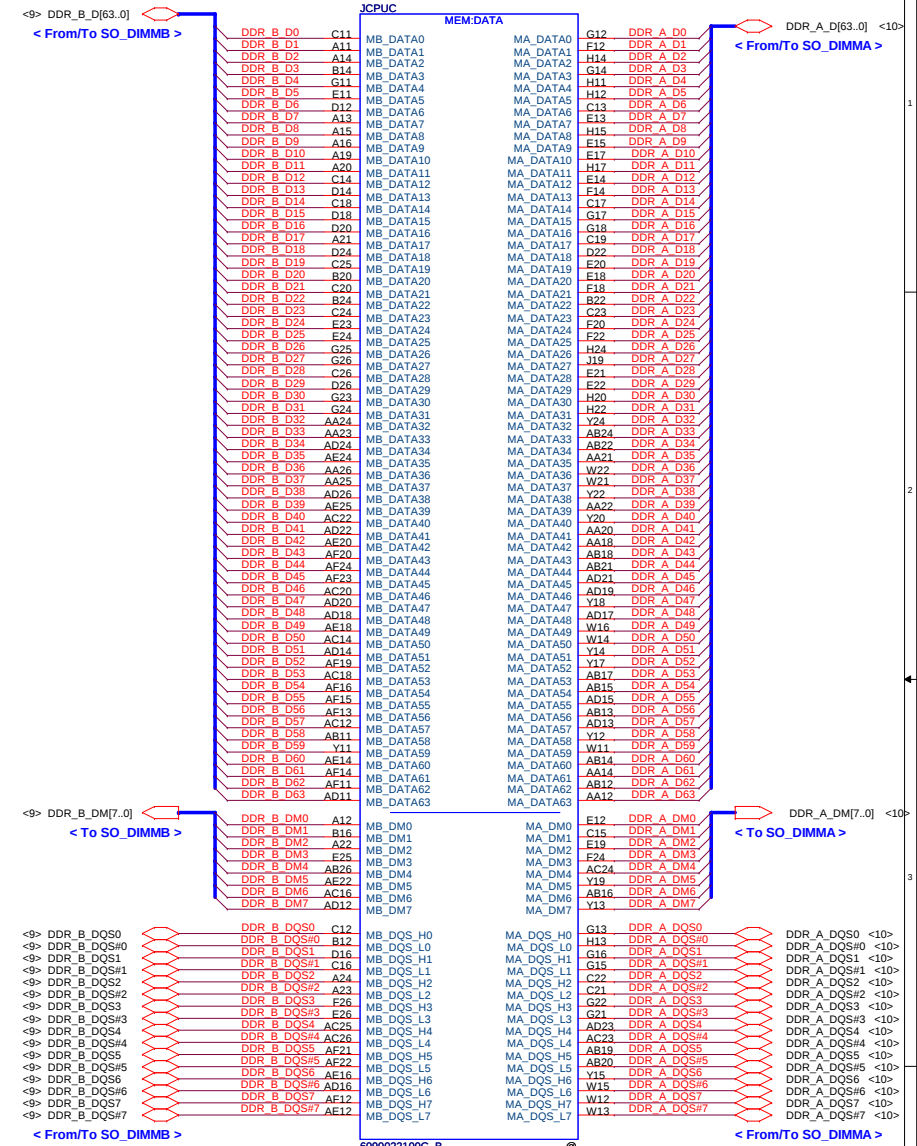
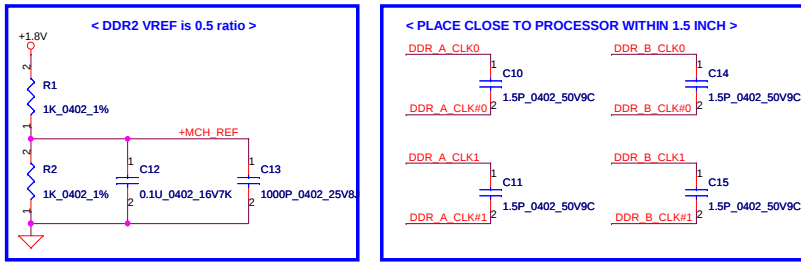


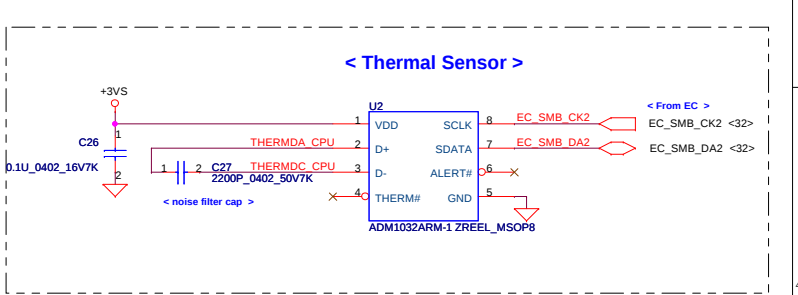
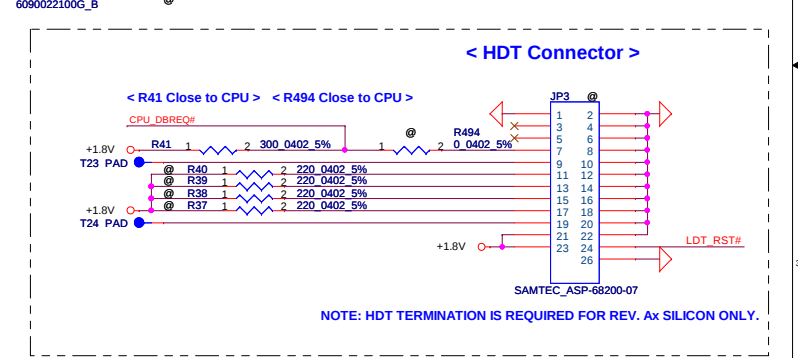
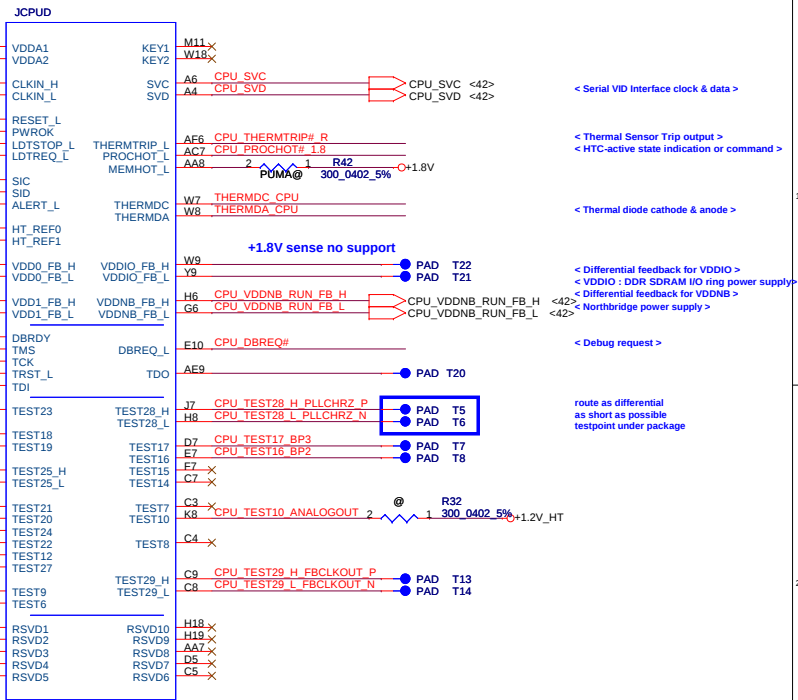
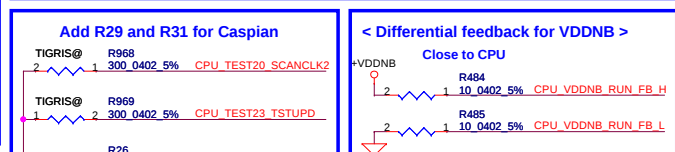
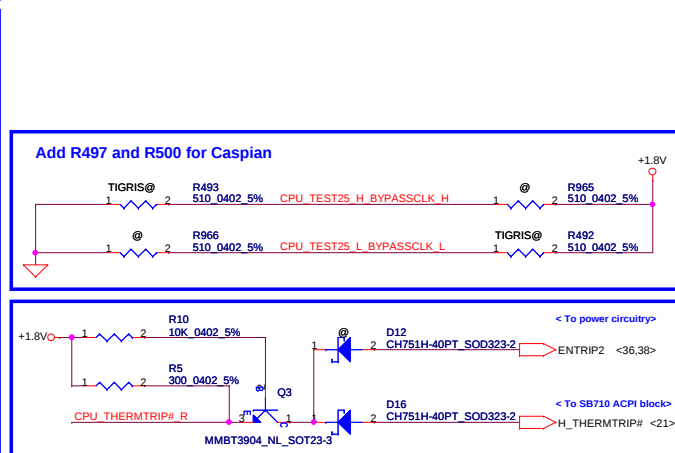
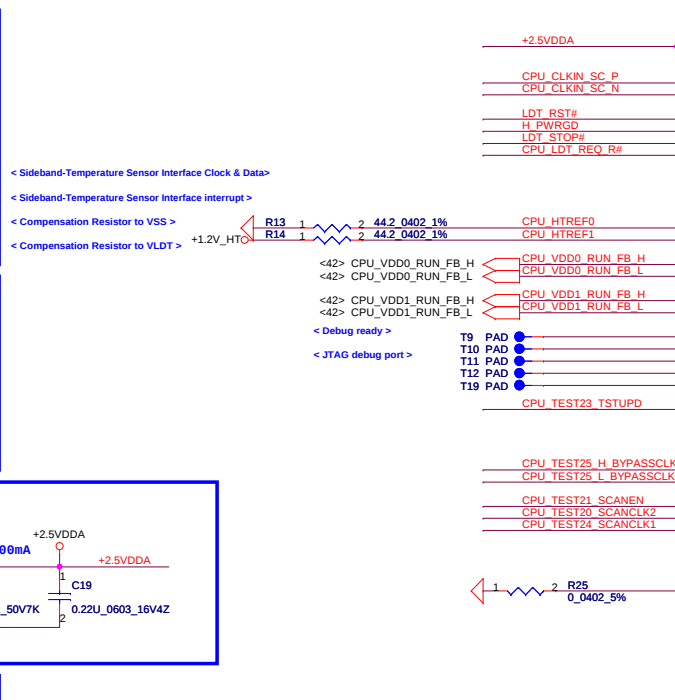
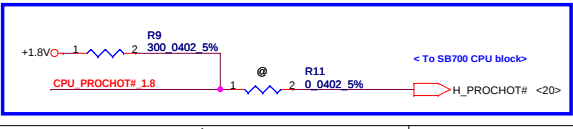
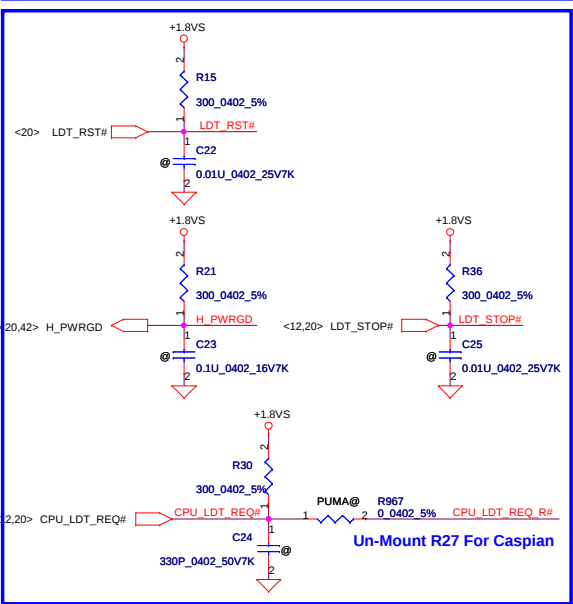
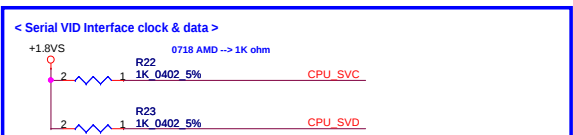
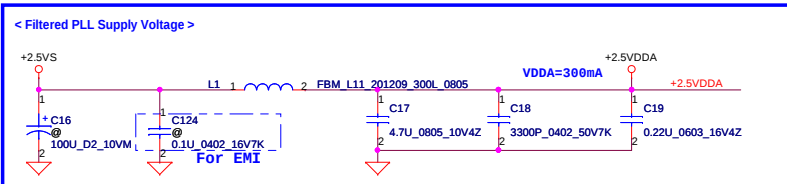
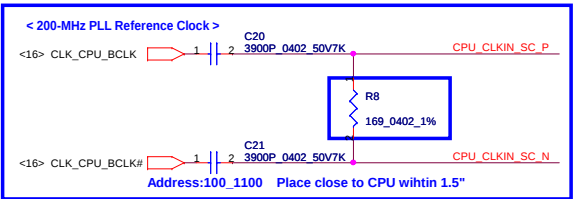
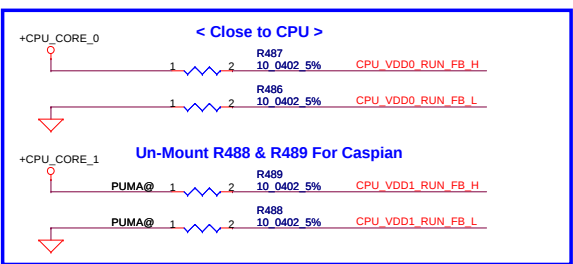
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 <11> H_CADIN[0..15] → H_CADIN[0..15] → H_CADON[0..15] <11>



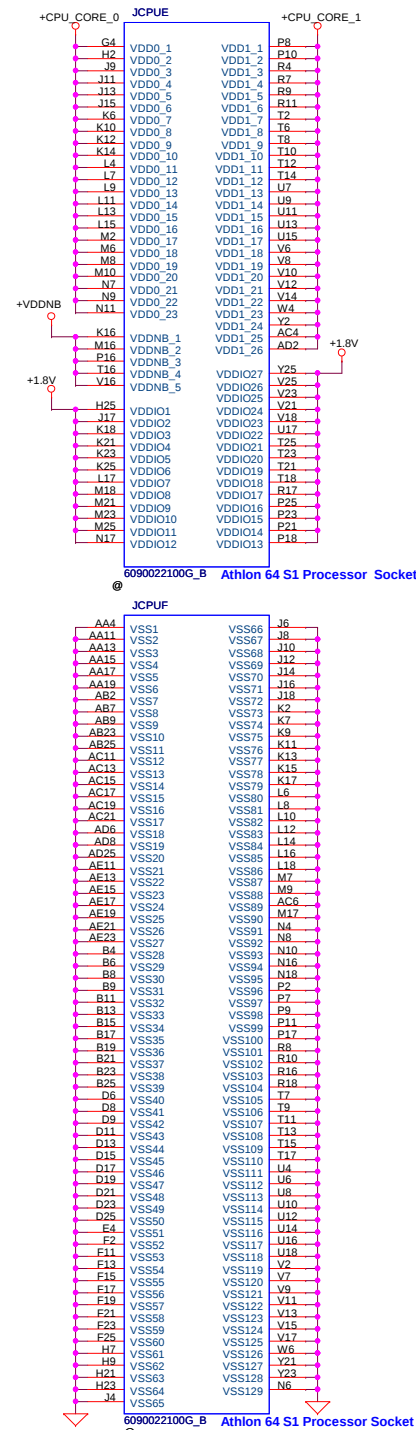
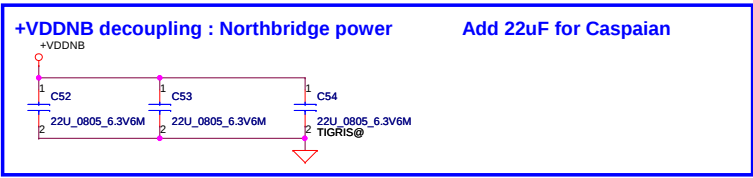
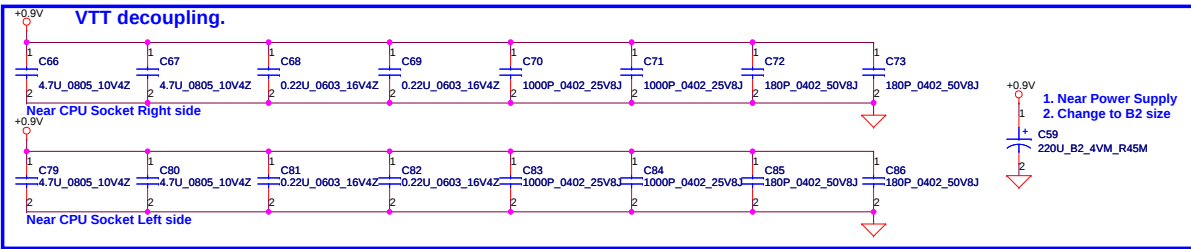
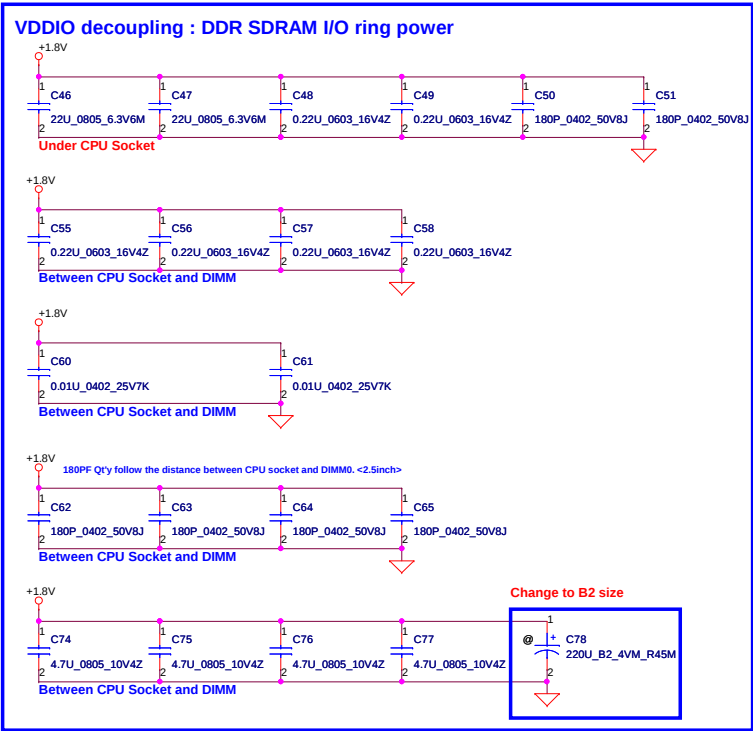
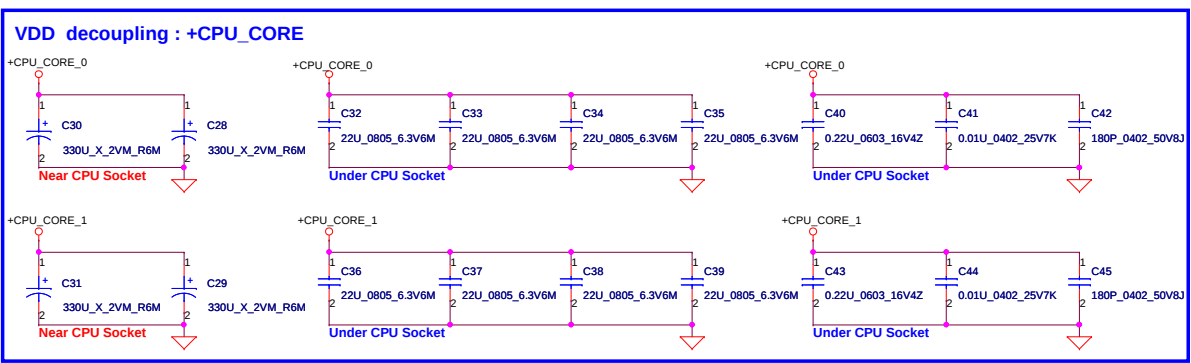
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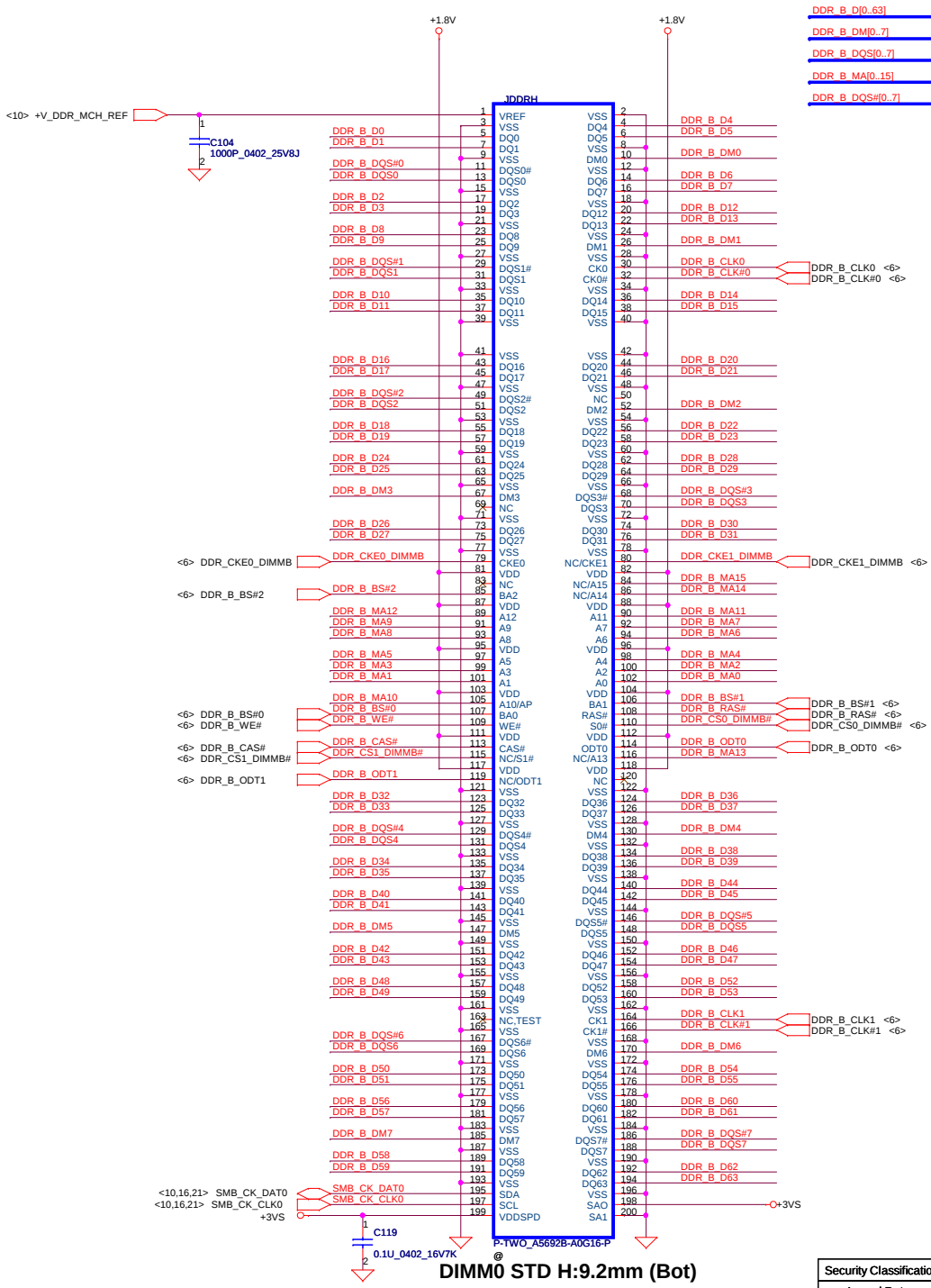
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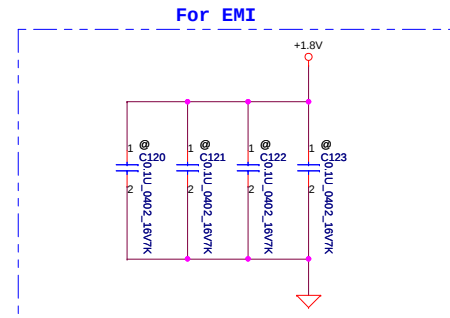
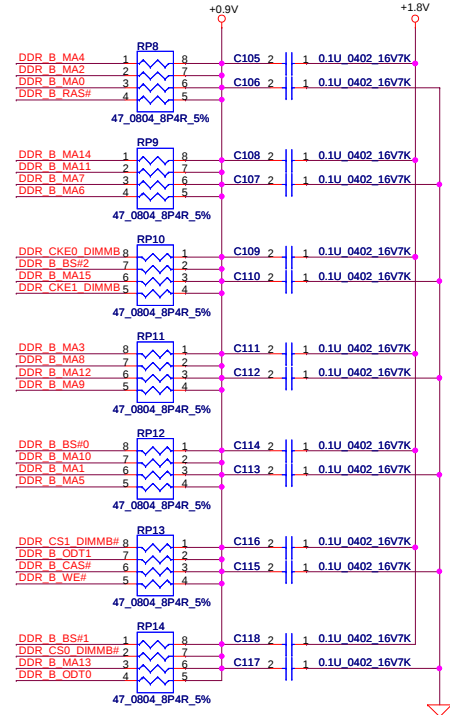


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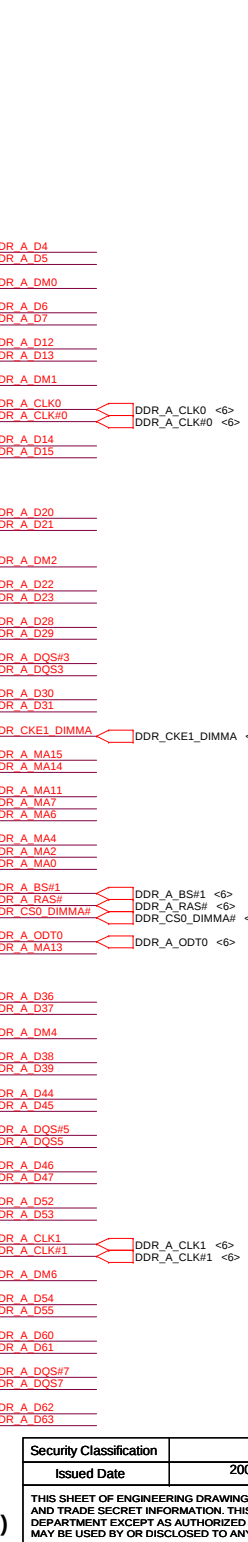
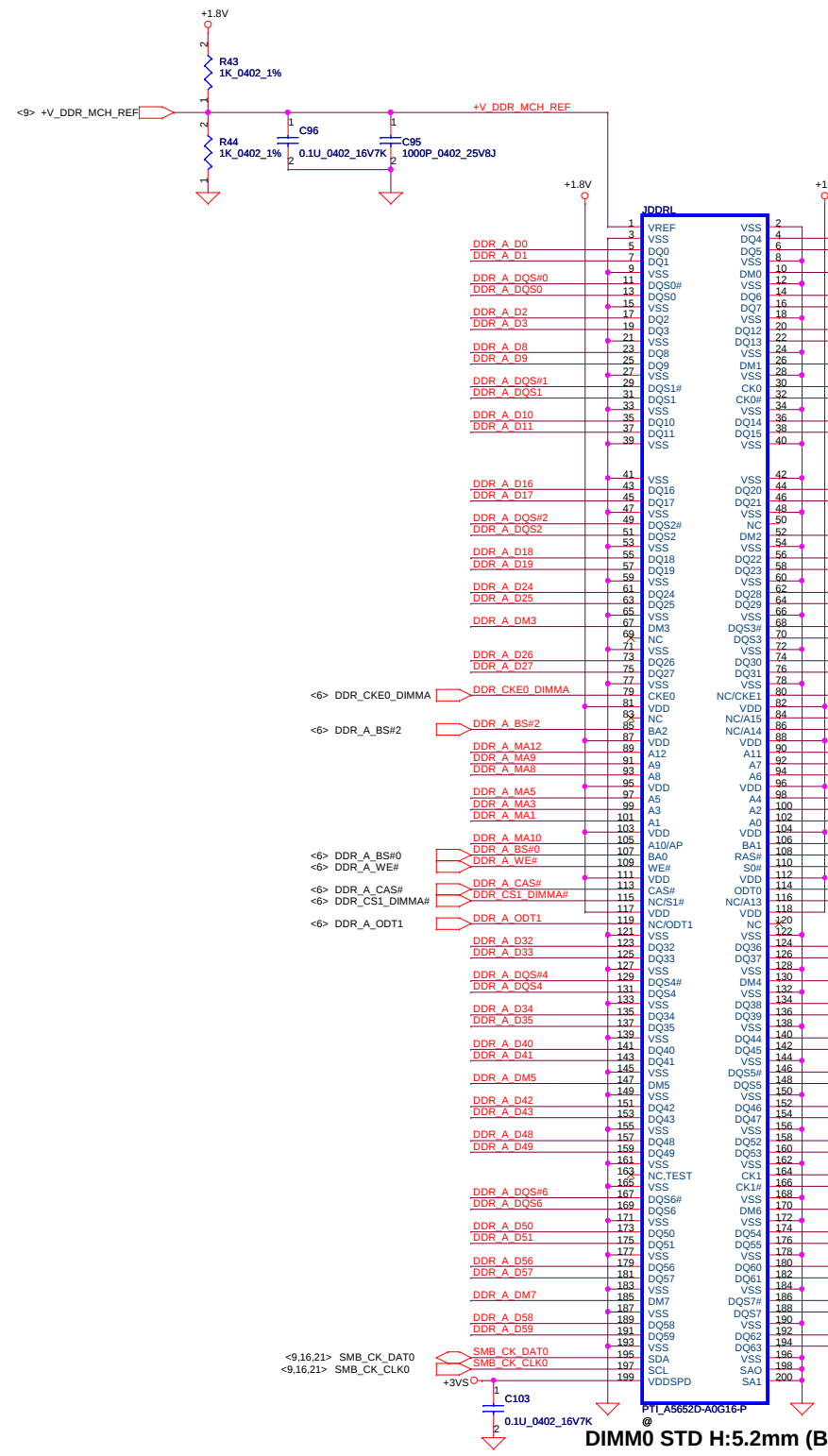


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DDR_B DM[0..7] <6>
DDR_B DQS[0..7] <6>
DDR_B MA[0..15] <6>
DDR_B DQS[0..7] <6>

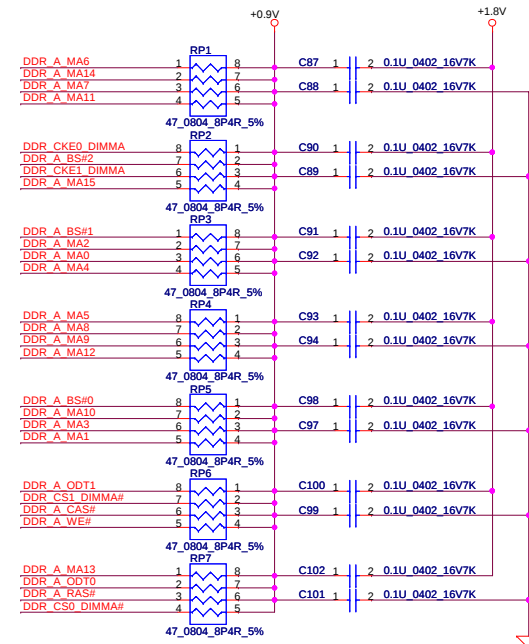


DIMM0 STD H:9.2mm (Bot)

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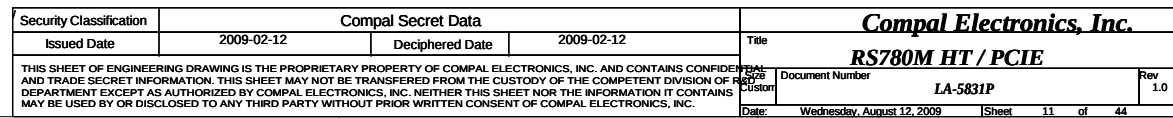
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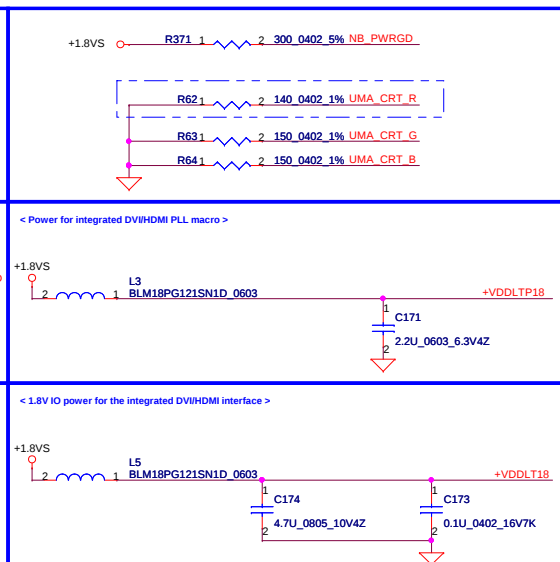
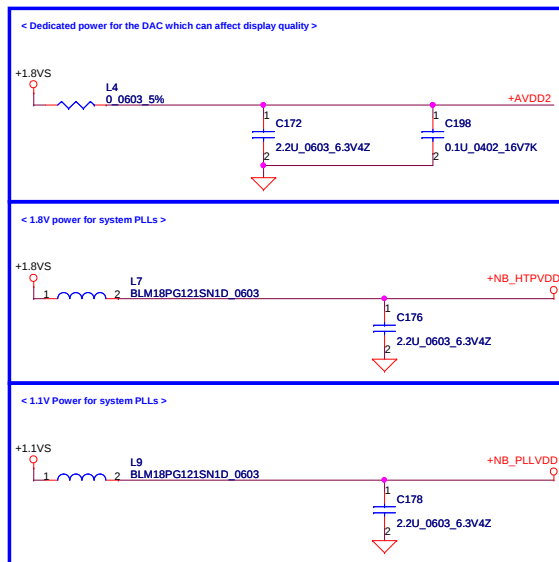
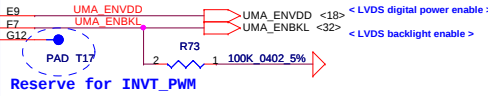


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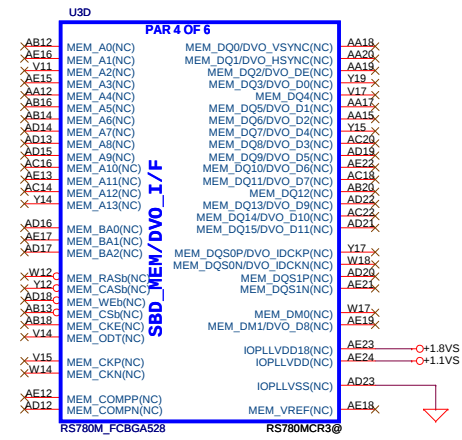
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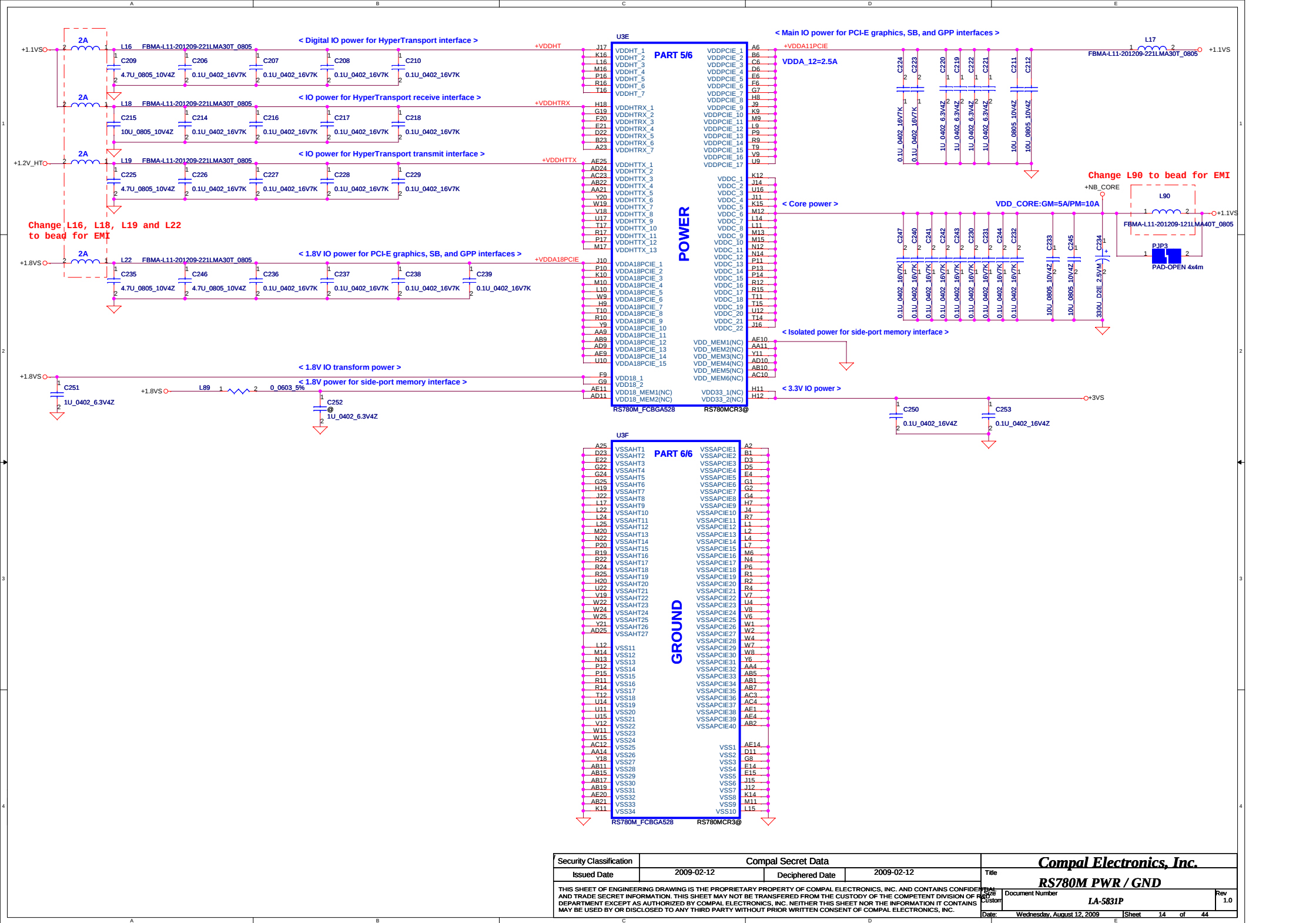
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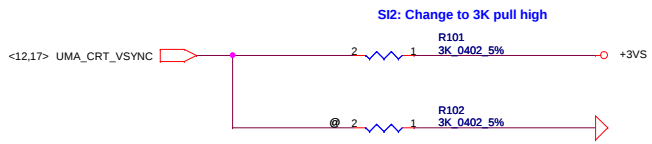
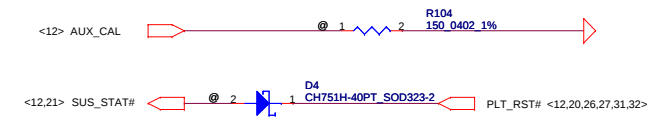
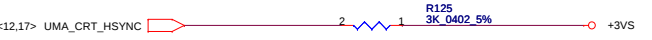


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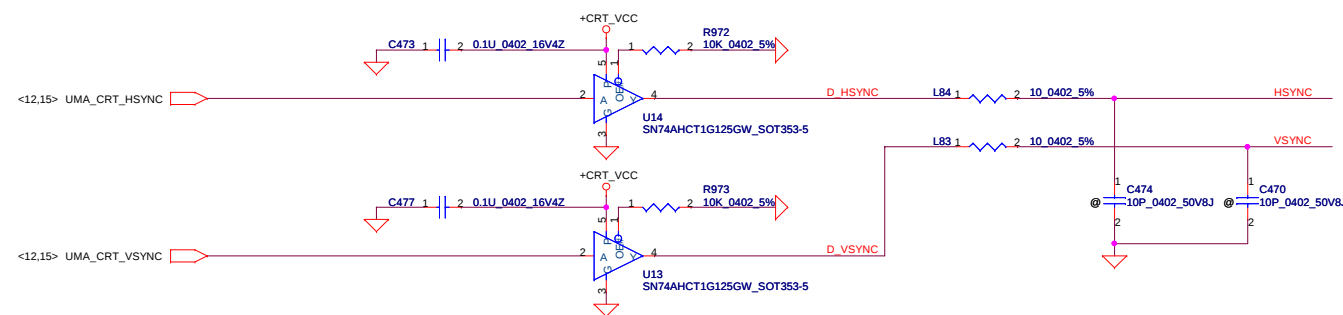
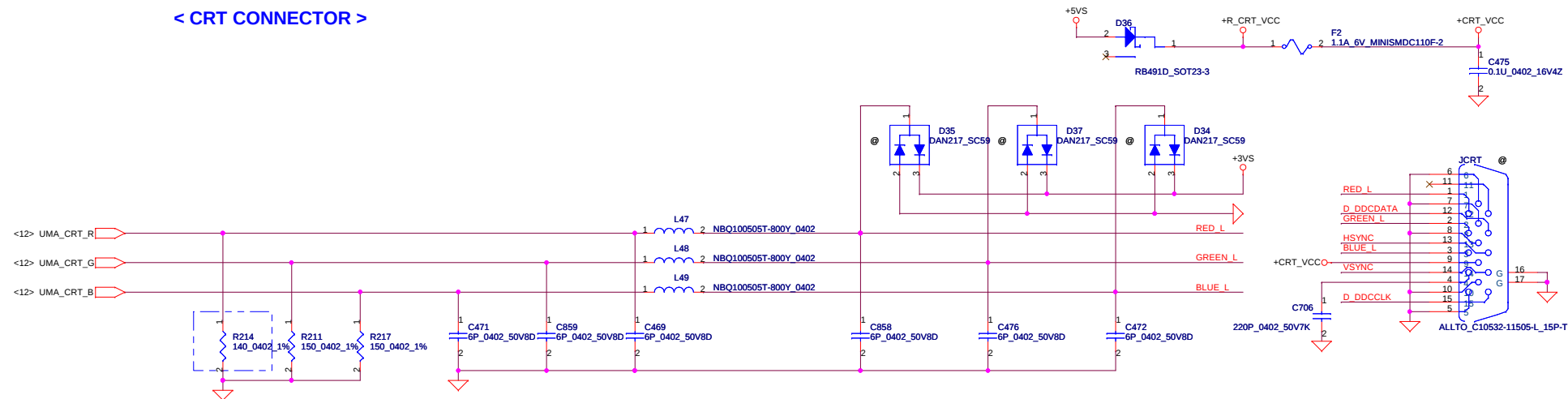
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Issued Date	2009-02-12	Deciphered Date	2009-02-12	Title	RS780M PWR / GND	
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< RS780 DFT_GPIO5 mux at CRT_VSYNC pull High to 3K > SI2: Change to 3K pull high 	< DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb > Enables the Test Debug Bus using GPIO. 1 : Enable (RX780, RS780) 0 : Disable (RX780, RS780) PIN: RS740-->RS780_AUX_CAL; RX780-->NB_TV_C; RS780--> VSYNC#
< RS780 use register to control PCI-E configure >	< DFT_GPIO[4:2] : STRAP_PCIE_GPP_CFG[2:0] > These pin straps are used to configure PCI-E GPP mode. 000 : 00001 001 : 00010 010 : 01011 011 : 00100 100 : 01010 101 : 01100 111 : 01011
< RS780 DFT_GPIO1 > 	< DFT_GPIO1 : LOAD_EEPROM_STRAPS > Selects Loading of STRAPS from EPROM 1 : Bypass the loading of EEPROM straps and use Hardware Default Values 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected RS740/RX780: DFT_GPIO1 RS780:SUS_STAT
< RS780 use HSYNC to enable SIDE PORT (internal pull high) > 	< DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb > RX780: Enables the Test Debug Bus using PCIE bus 1 : Disable (Can still be enabled using nbcfg register access) 0 : Enable RS780: Enables Side port memory (RS780 use HSYNC#) 1. Disable (RS780) 0 : Enable (RS780)

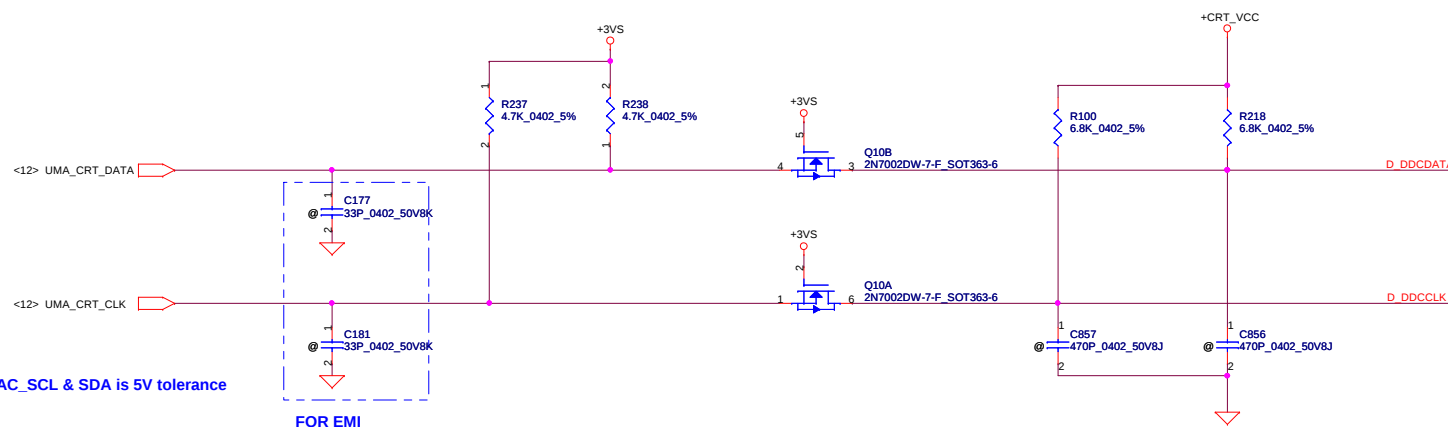
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2009-02-12	Deciphered Date	2009-02-12	Title	RS780M STRAPS	
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Compal Electronics, Inc.			
Title			
Clock Generator			
Part No.	Document Number	Rev	Rev
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< CRT CONNECTOR >



< SYNC SIGNAL >

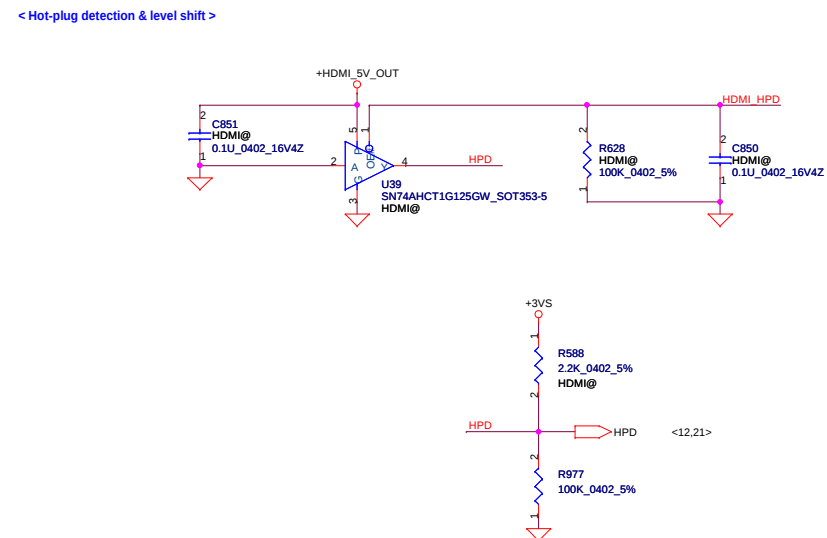
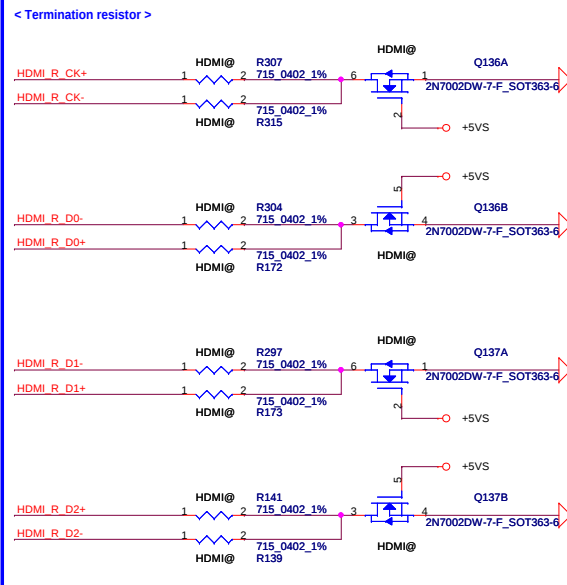
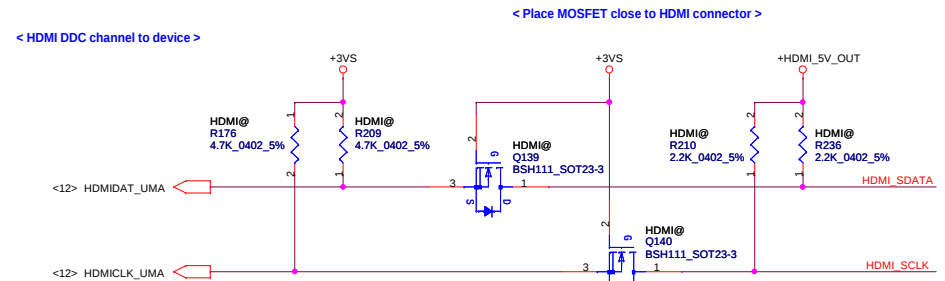
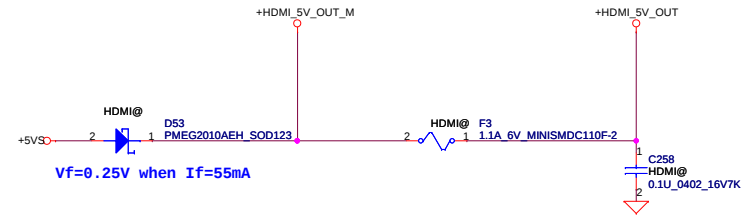


< Display Data Channel >

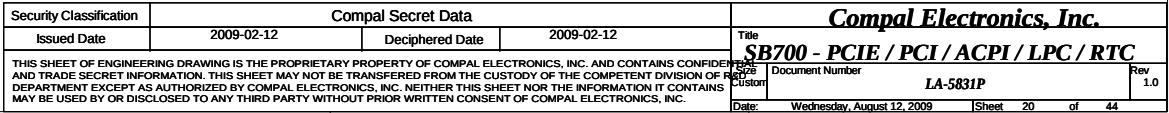
RS780 DAC_SCL & SDA is 5V tolerance

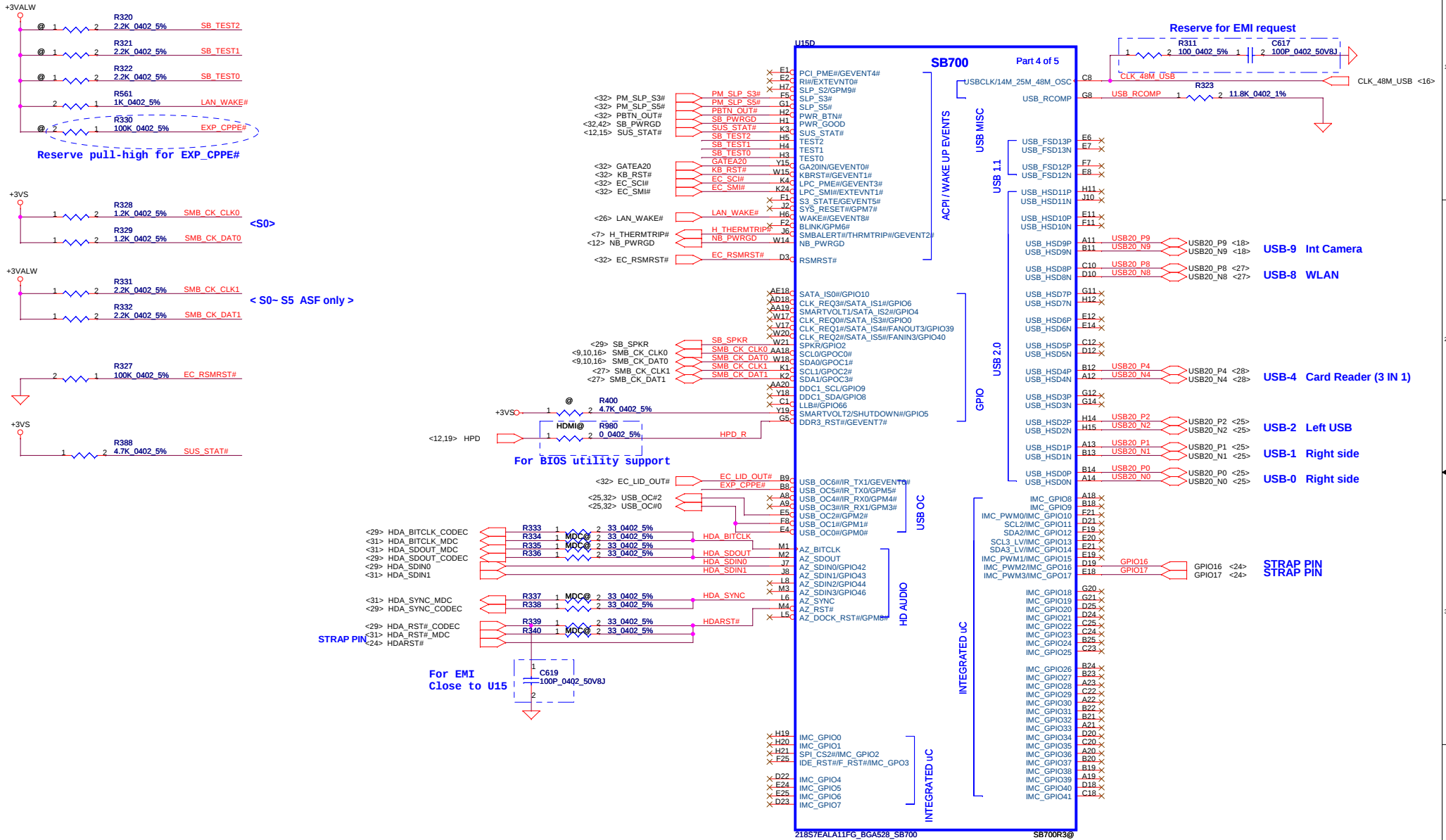
FOR EMI

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Issued Date	2009-02-12	Deciphered Date	2009-02-12	HDMI			
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				Docu- ment Number	LA-5831P		Rev 1.0
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				Date: Wednesday, August 12, 2009	Sheet 21 of 44

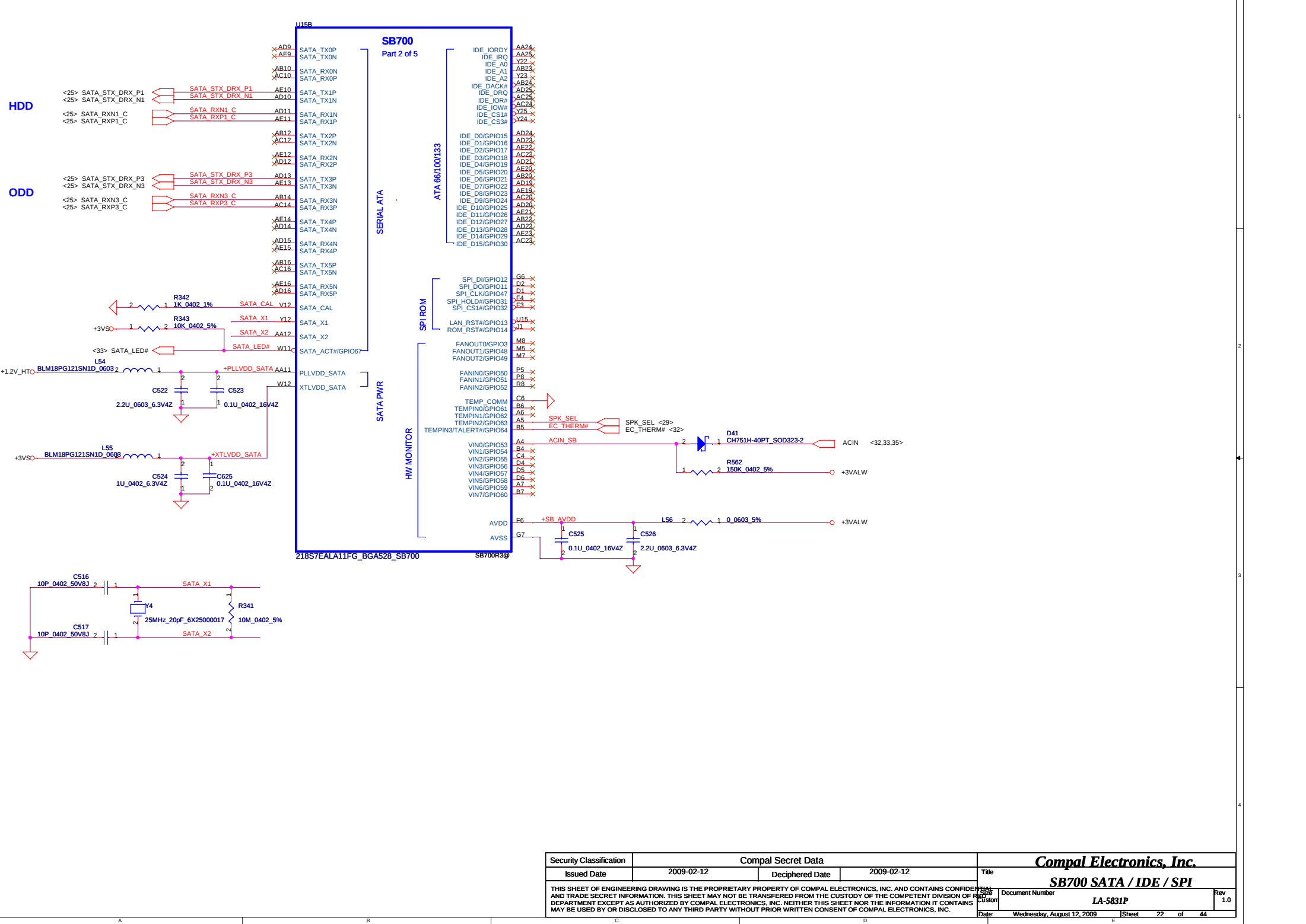
HDD

ODD

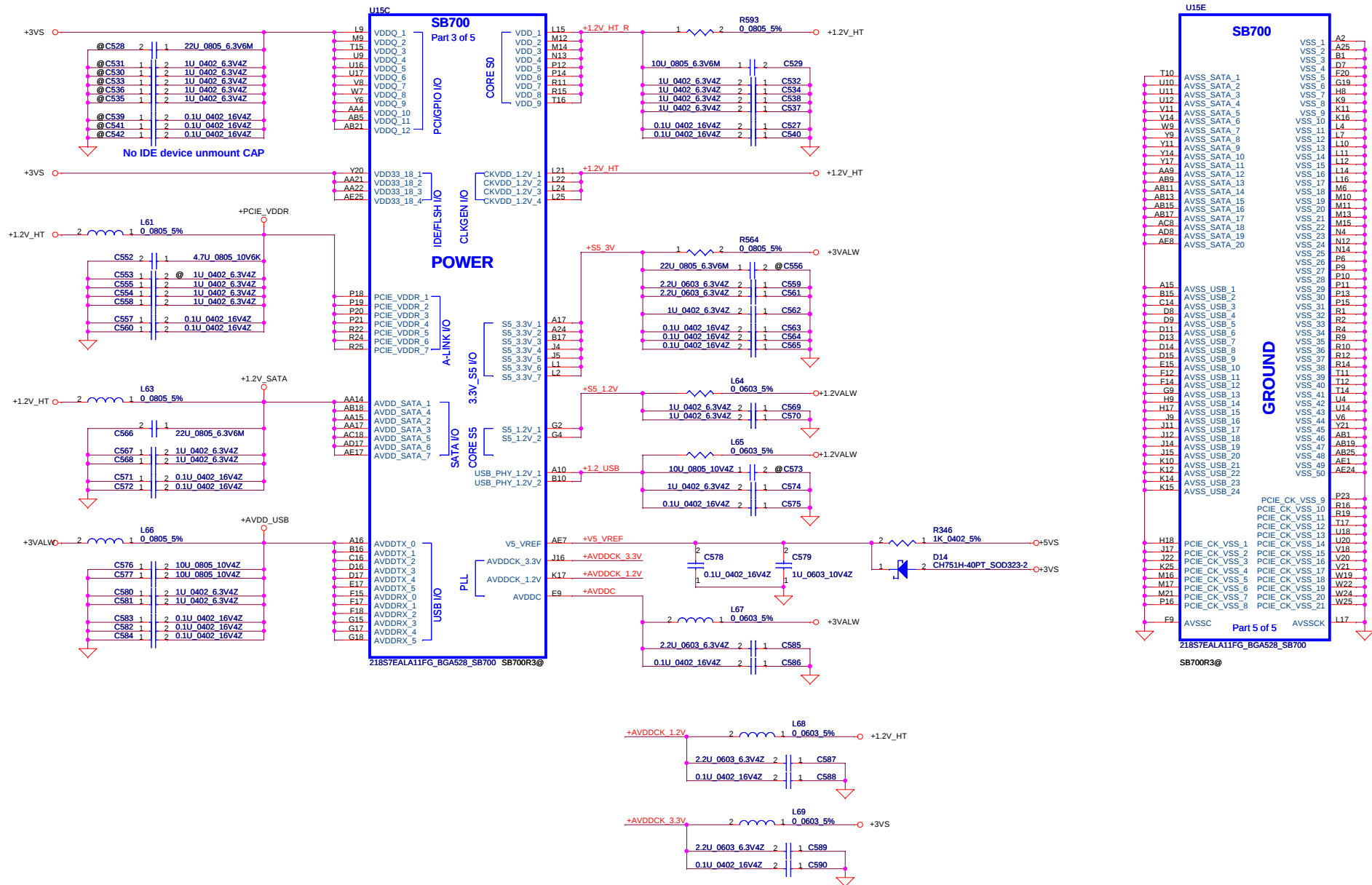
2

3

4



Security Classification		Compal Secret Data		Title	
Issued Date	2009-02-12	Deciphered Date	2009-02-12	SB700 SATA / IDE / SPI	
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Date: Wednesday, August 12, 2009				Sheet	22 of 44

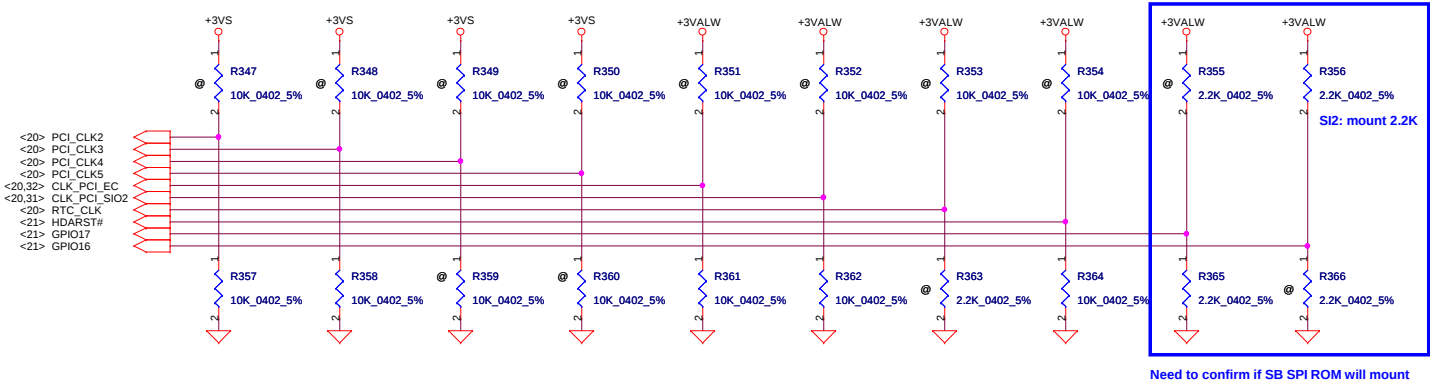


Security Classification		Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2009-02-12		Deciphered Date		2009-02-12		Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						SB700 Power / GND			
						Document Number		Rev	
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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

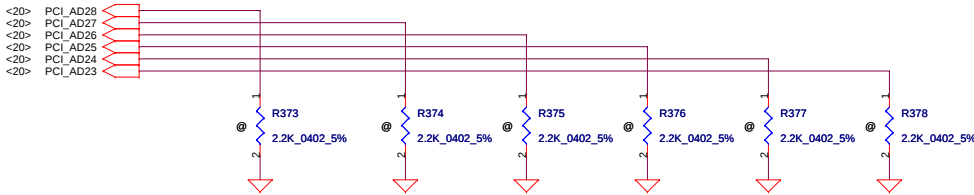
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		L,H = LPC ROM (Default) L,L = FWH ROM



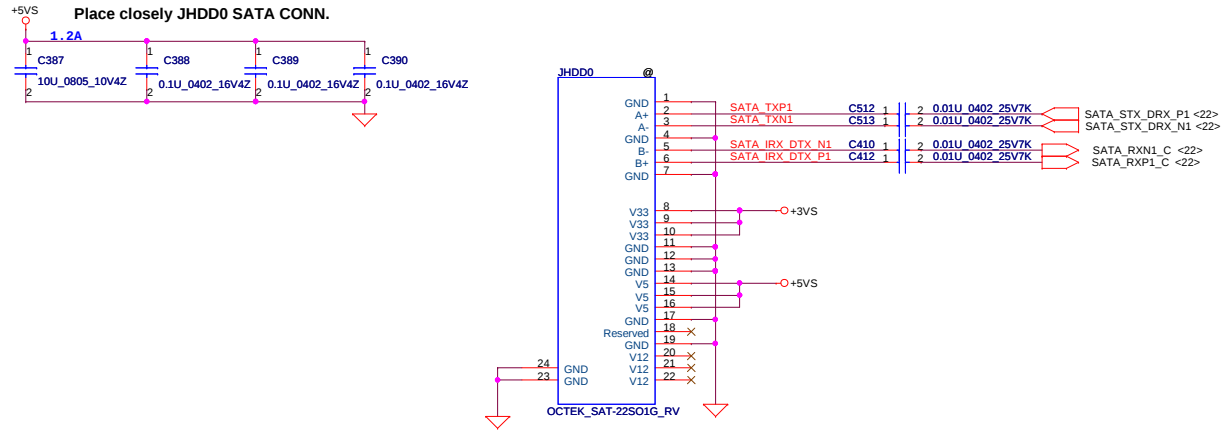
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

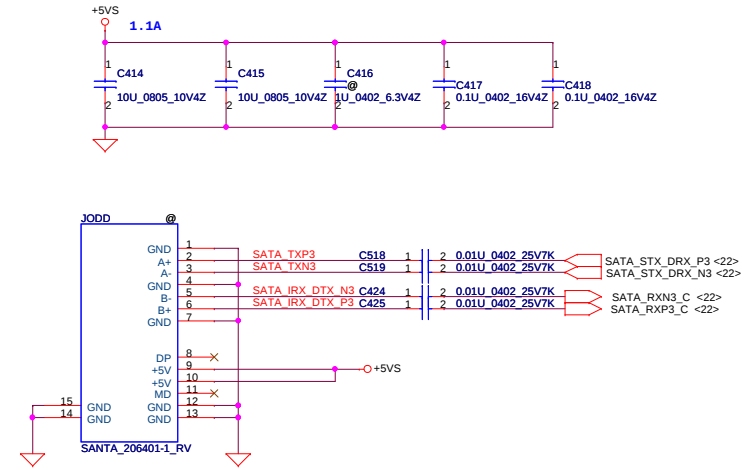
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



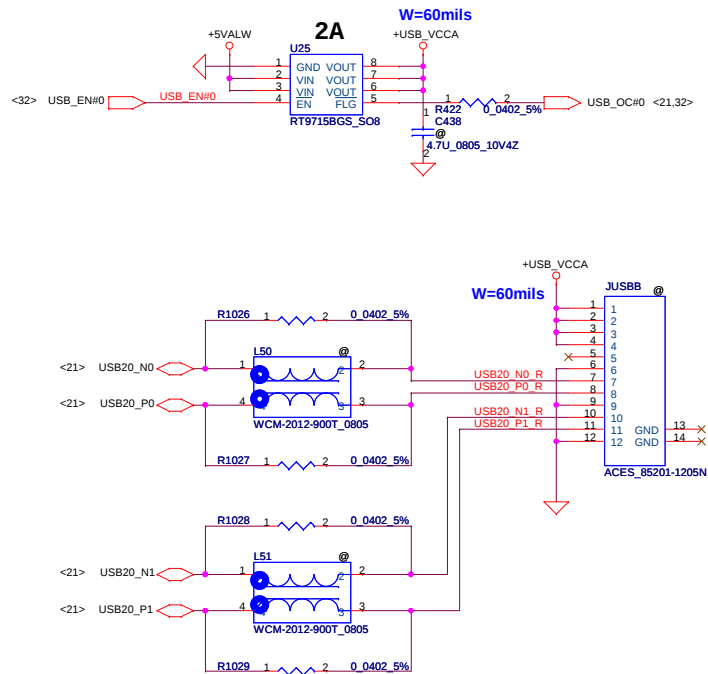
SATA HDD Conn.



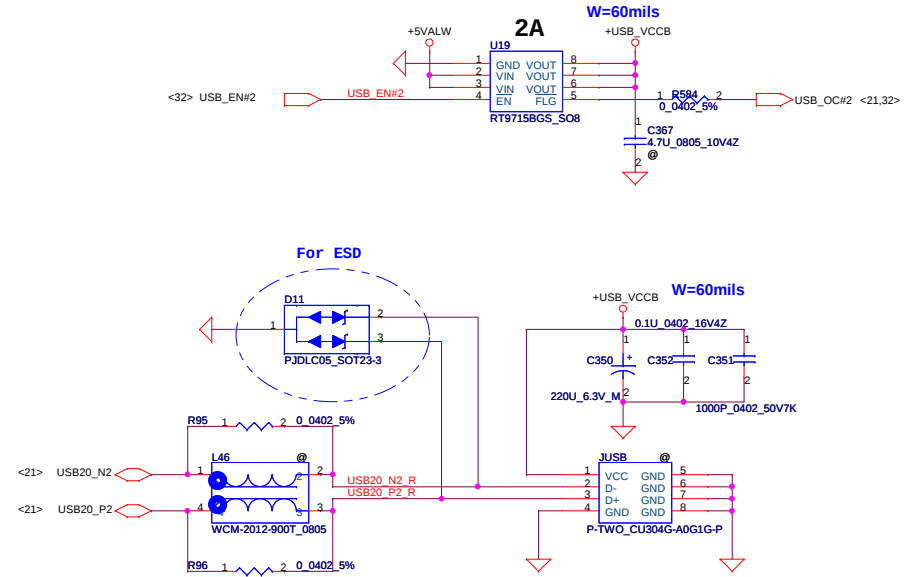
SATA ODD Conn



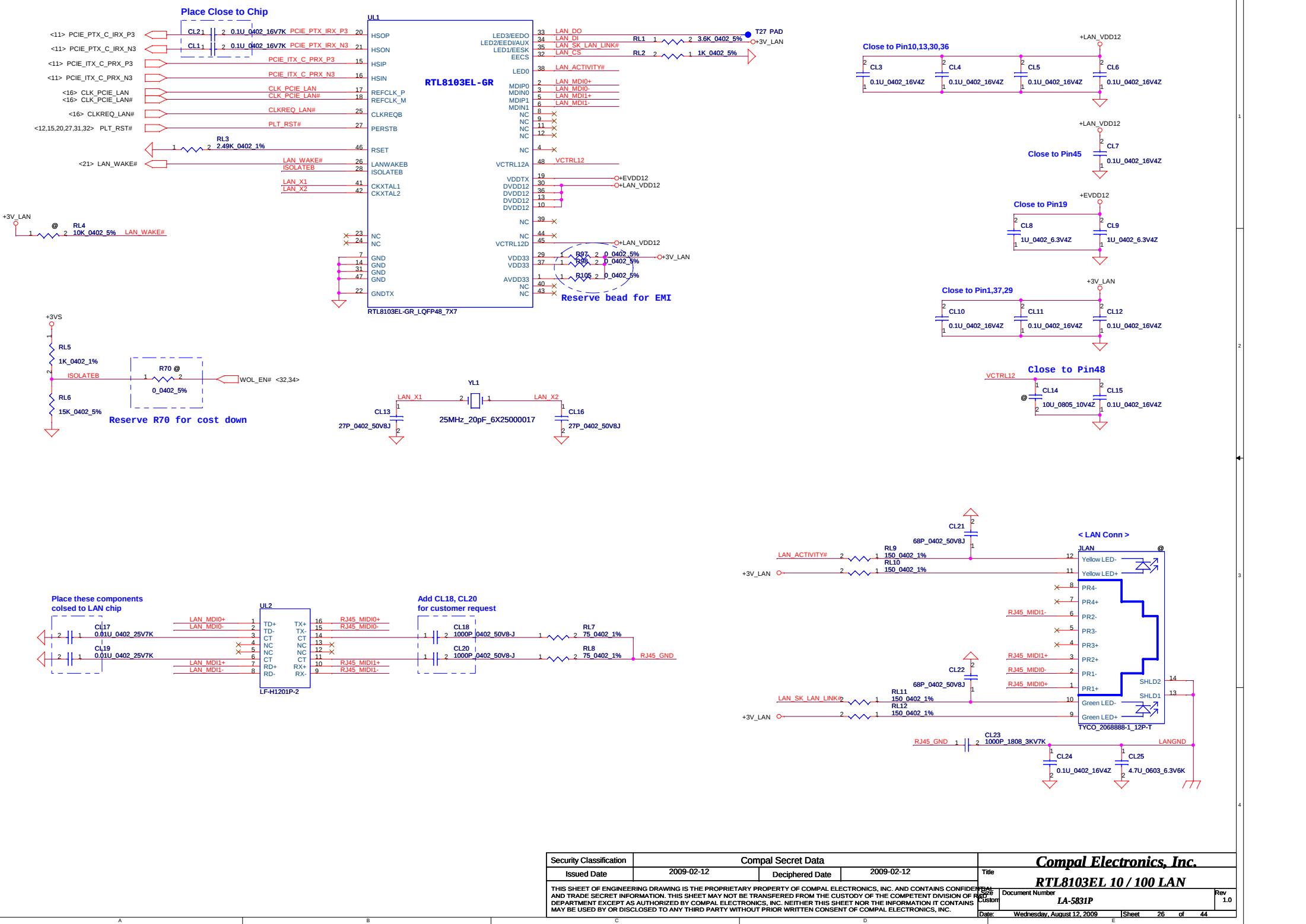
USB Right Board



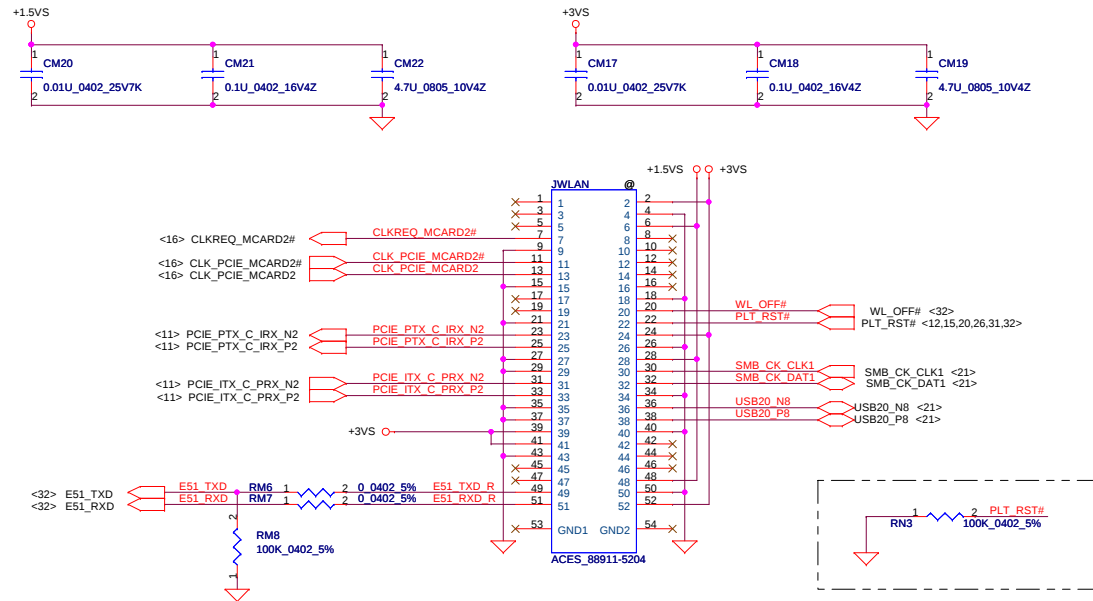
USB Left Conn



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< PCIe Mini Card for WLAN/ WiMAX >



<NB & SB >

< R1 for customer BOM STRUCTURE >

< R3 for mass production BOM STRUCTURE >

RS780MN
U3
RS780MN R1
RS780MNR1@

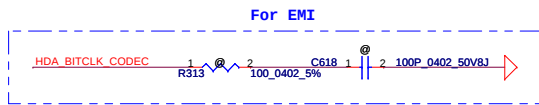
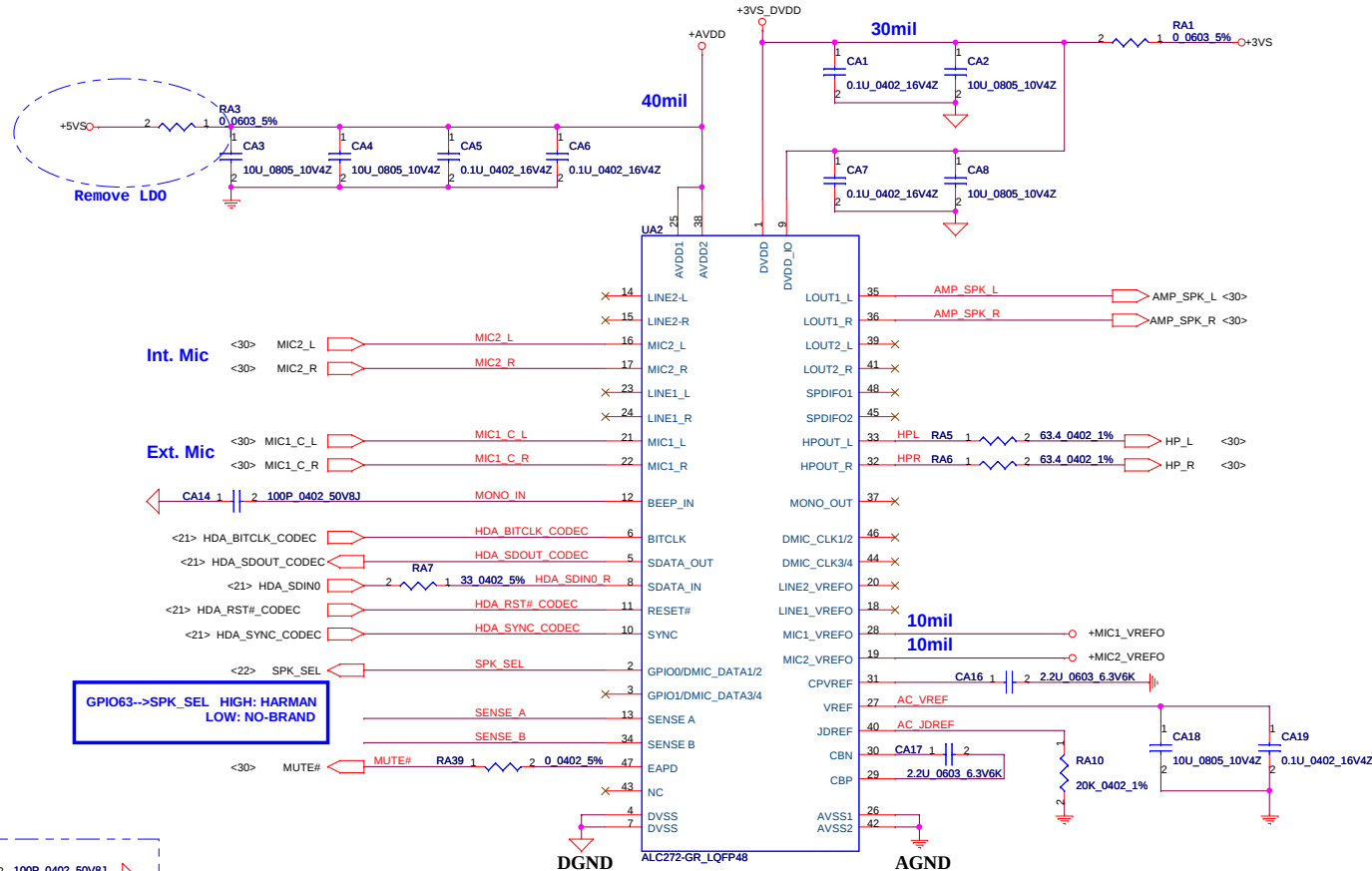
RS780MN
U3
RS780MN R3
RS780MNR3@

RS780MC
U3
RS780MC R1
RS780MCR1@

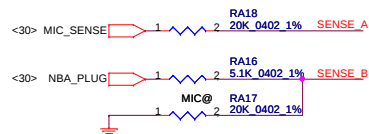
SB700
U15
SB700R1
SB700R1@

< PCB >

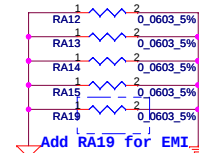
PCB
ZZZ
PCB 075 LA-5831P REV1 M/B



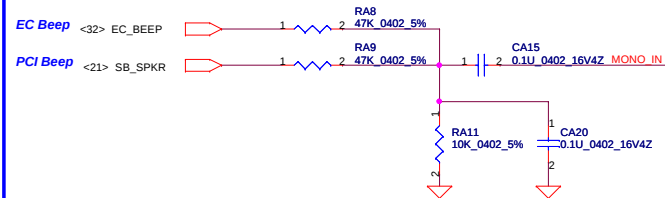
< SENSE_A & SENSE_B, place close to chip >



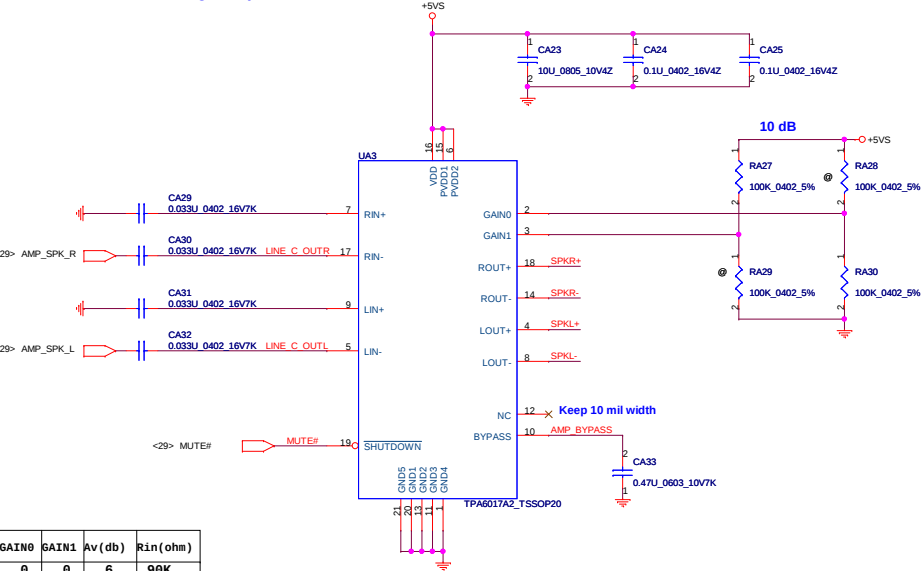
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	PORT-D (PIN 35, 36)	SPK out
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out



< MONO_IN SOURCE >

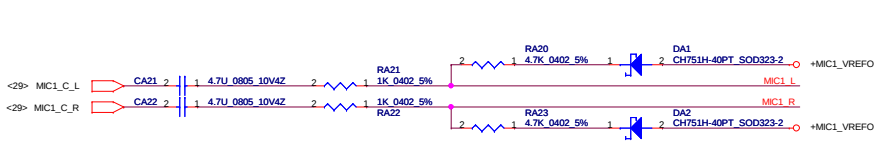


< TPA6017 Medium Range Amplifier >

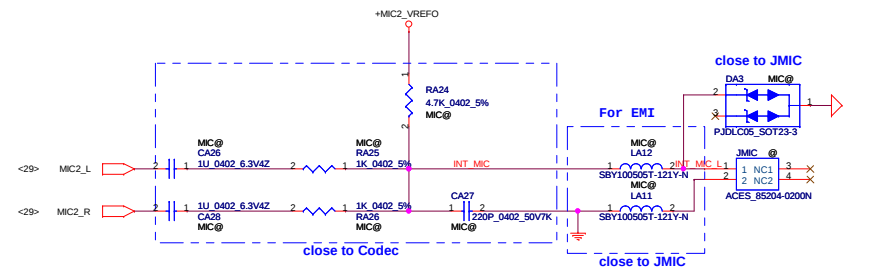


GAIN0	GAIN1	Av (db)	Rin(ohm)
0	0	6	90K
0	1	10	70K
1	0	15.6	45K
1	1	21.6	25K

< Ext. Mic >

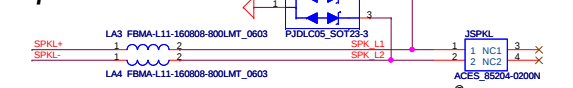


< Int. Mic >



< Speaker Connector >

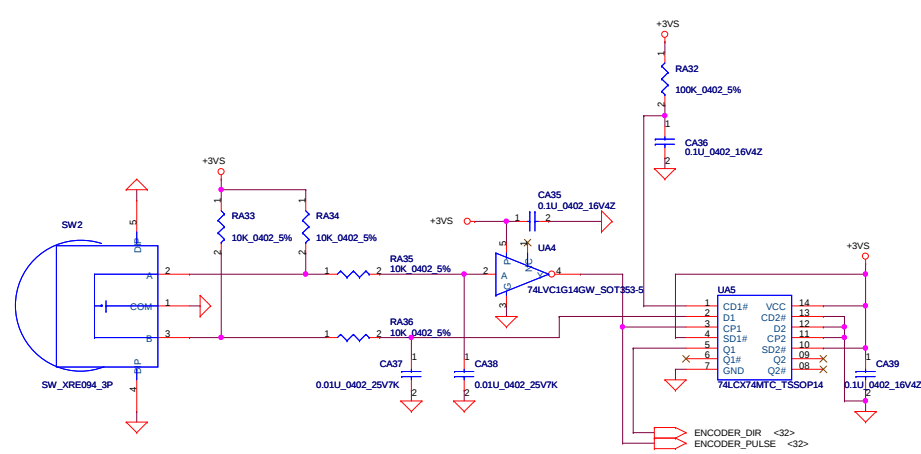
Left Connector



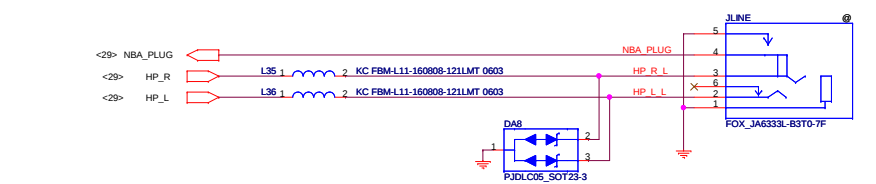
Right Connector



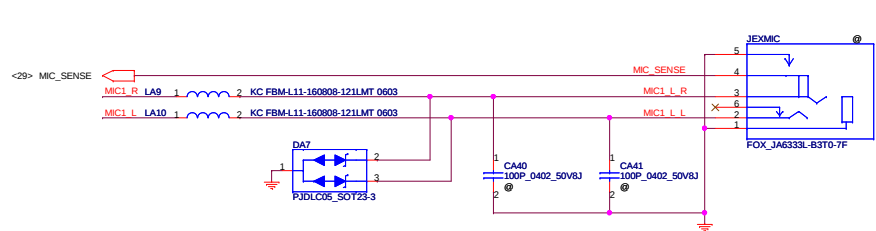
< Volume Control >



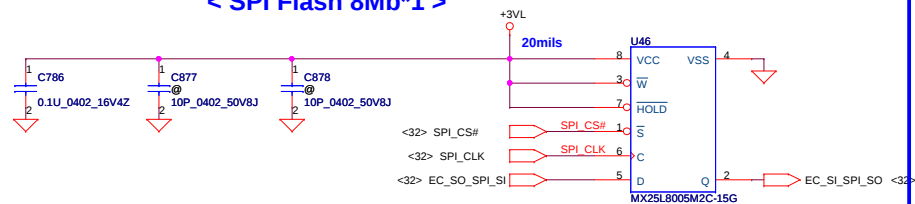
< HeadPhone JACK >



< Ext.MIC/LINE IN JACK >

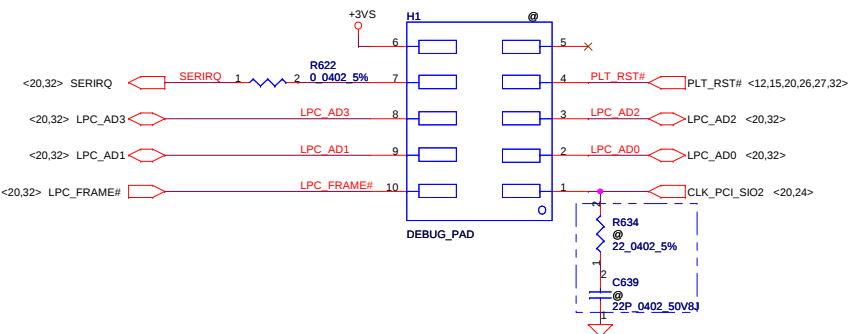


< SPI Flash 8Mb*1 >

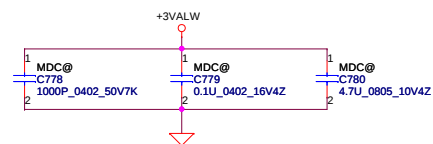
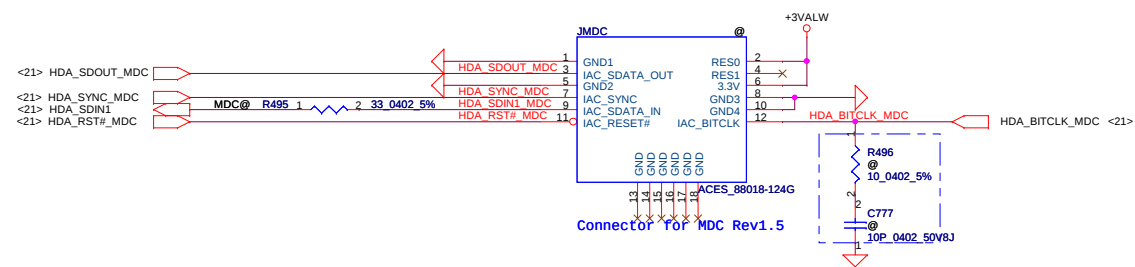


< LPC Debug Port >

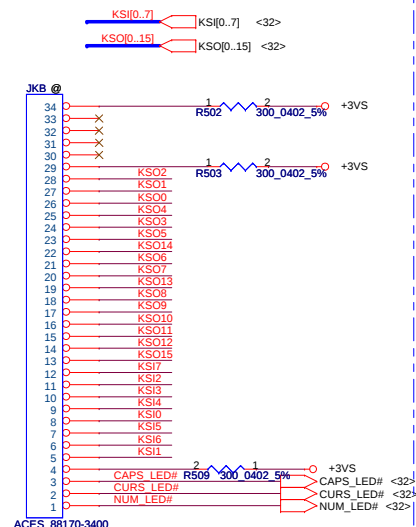
Please place the PAD under DDR DIMM.



< MDC 1.5 Conn >



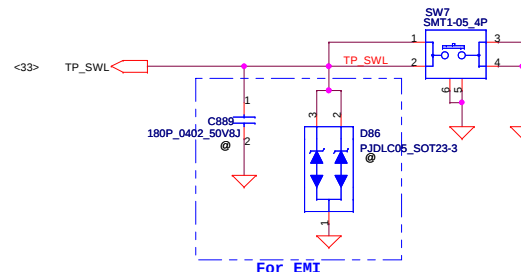
KEYBOARD CONN.



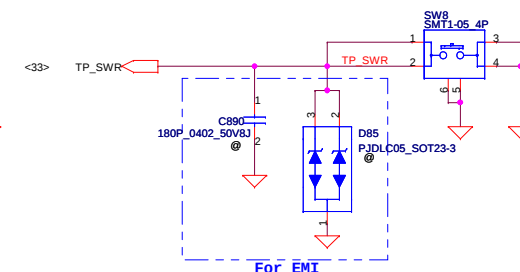
For EMI

KS02	1	2
	C725	100P_0402_50VB3
KS01	1	2
	C717	100P_0402_50VB3
KS00	1	2
	C721	100P_0402_50VB3
KS04	1	2
	C609	100P_0402_50VB3
KS03	1	2
	C724	100P_0402_50VB3
KS05	1	2
	C728	100P_0402_50VB3
KS014	1	2
	C730	100P_0402_50VB3
KS06	1	2
	C715	100P_0402_50VB3
KS07	1	2
	C732	100P_0402_50VB3
KS013	1	2
	C733	100P_0402_50VB3
KS08	1	2
	C740	100P_0402_50VB3
KS09	1	2
	C737	100P_0402_50VB3
KS010	1	2
	C729	100P_0402_50VB3
KS011	1	2
	C738	100P_0402_50VB3
KS012	1	2
	C718	100P_0402_50VB3
KS015	1	2
	C736	100P_0402_50VB3
KS17	1	2
	C716	100P_0402_50VB3
KS12	1	2
	C741	100P_0402_50VB3
KS13	1	2
	C726	100P_0402_50VB3
KS14	1	2
	C723	100P_0402_50VB3
KS10	1	2
	C731	100P_0402_50VB3
KS15	1	2
	C739	100P_0402_50VB3
KS16	1	2
	C735	100P_0402_50VB3
KS11	1	2
	C734	100P_0402_50VB3
CAPS_LED#	1	2
	C722	100P_0402_50VB3
CURS_LED#	1	2
	C727	100P_0402_50VB3
NUM_LED#	1	2
	C714	100P_0402_50VB3

Left switch

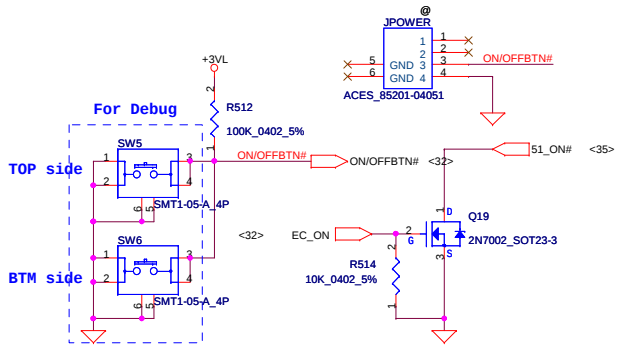


Right Switch

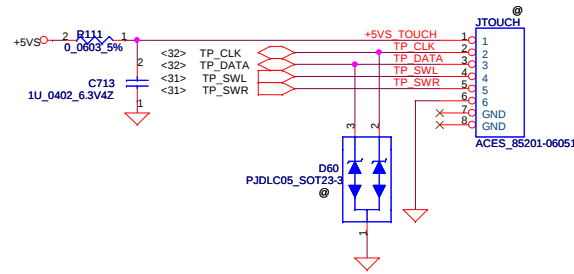


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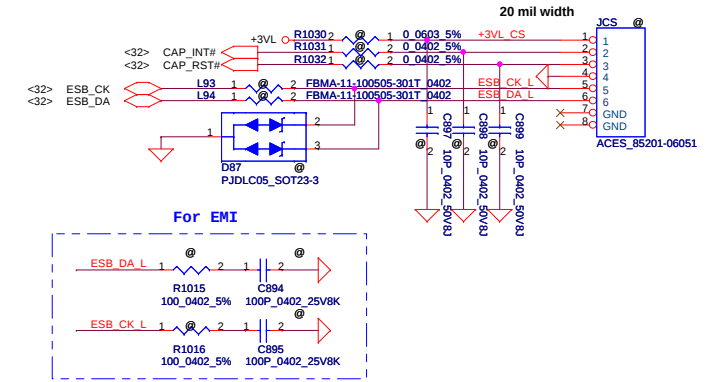
Power Button/ PWR/B



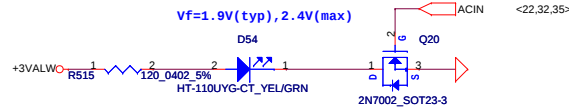
Touch Pad Connector



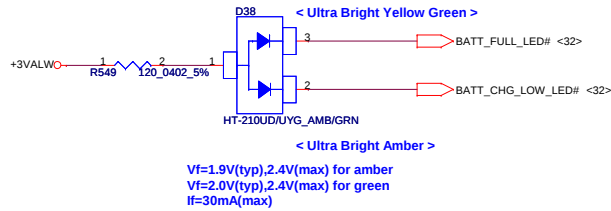
CS/B Connector



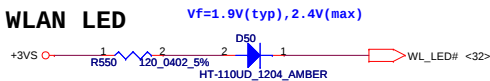
DC-IN LED



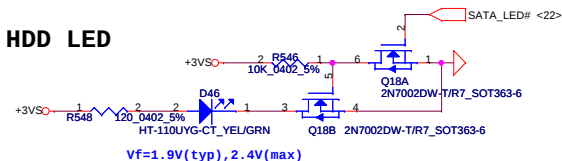
BATT CHARGE/FULL LED



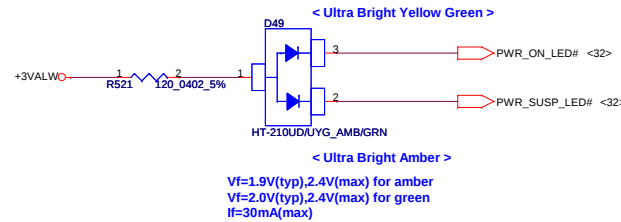
WLAN LED



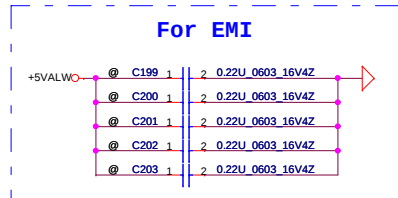
HDD LED



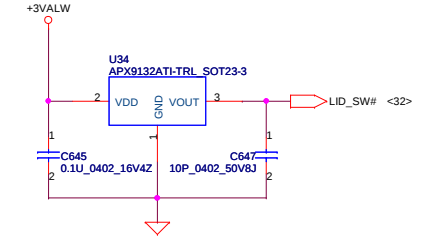
POWER ON/SUSPEND LED



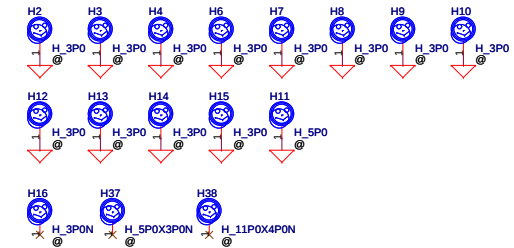
For EMI



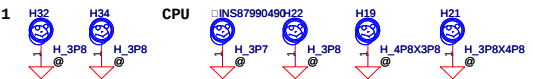
Lid SW



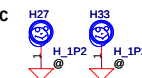
Screw Hole



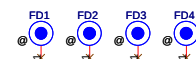
MINI CARD-1



MDC

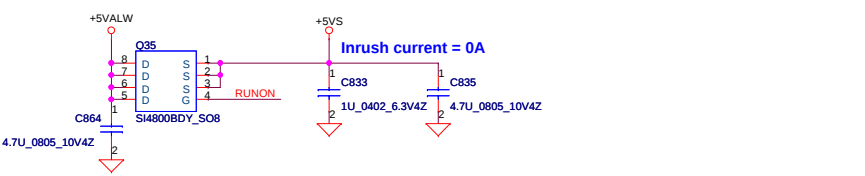


PCB Fedical Mark PAD

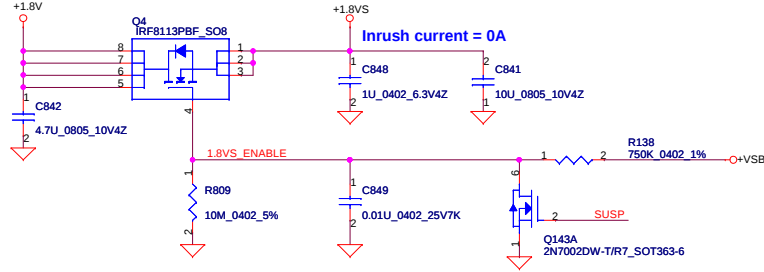


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Issued Date	2008/04/14	Deciphered Date	2009/04/14	LED/LID/PB/FB/SCREW HOLE
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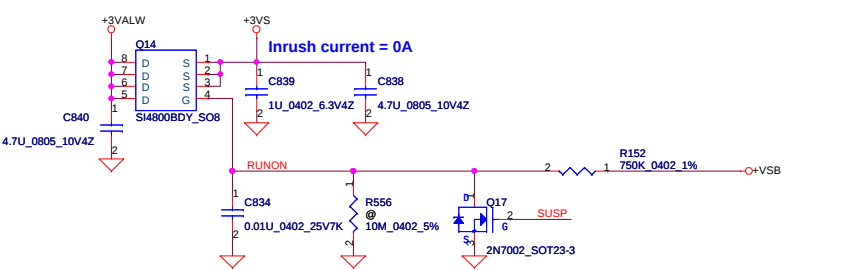
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< close to PQ20, must EMI confirm > < +1.8V TO +1.8VS >

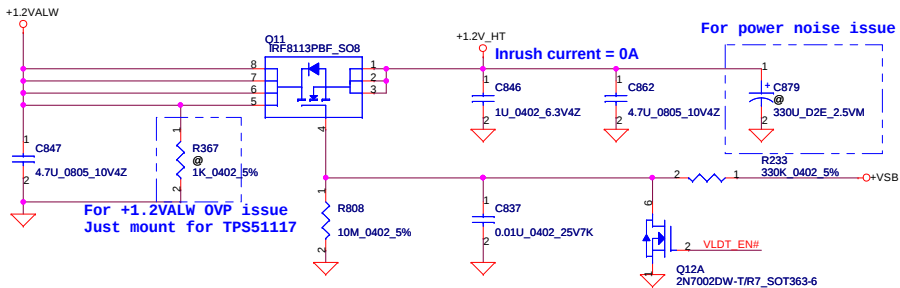


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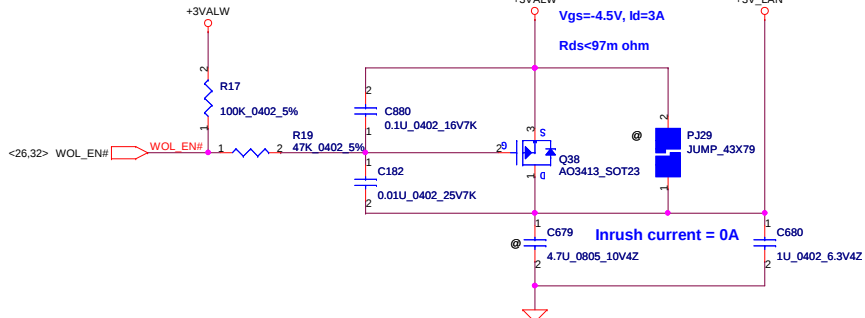


< close to PQ20, must EMI confirm >

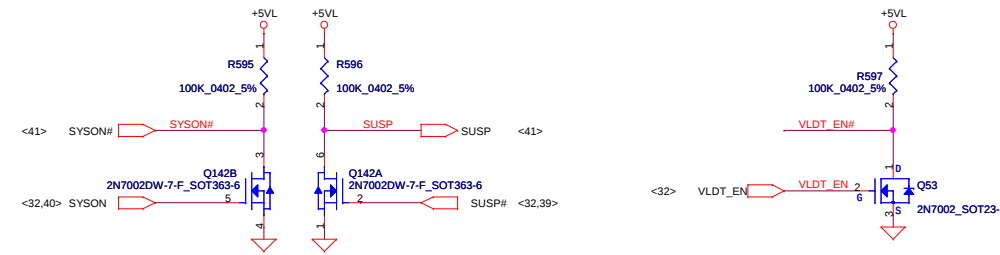
< +1.2VALW TO +1.2V_HT >



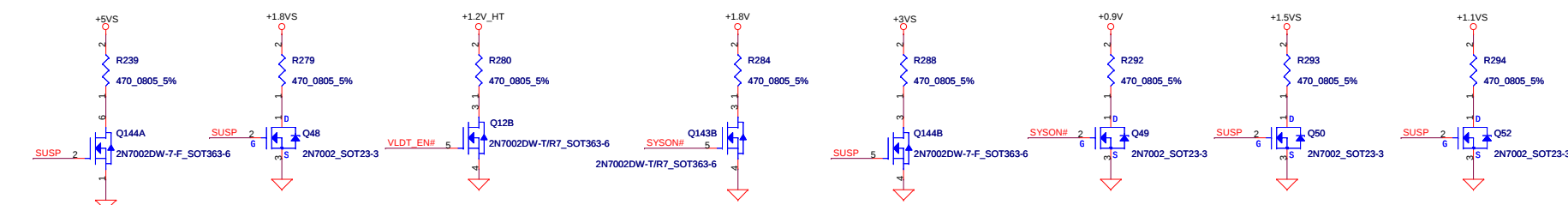
< +3VALW TO +3V_LAN >



< Inversion of SYSON, SUSP#, VLDT_EN, EC_ON >

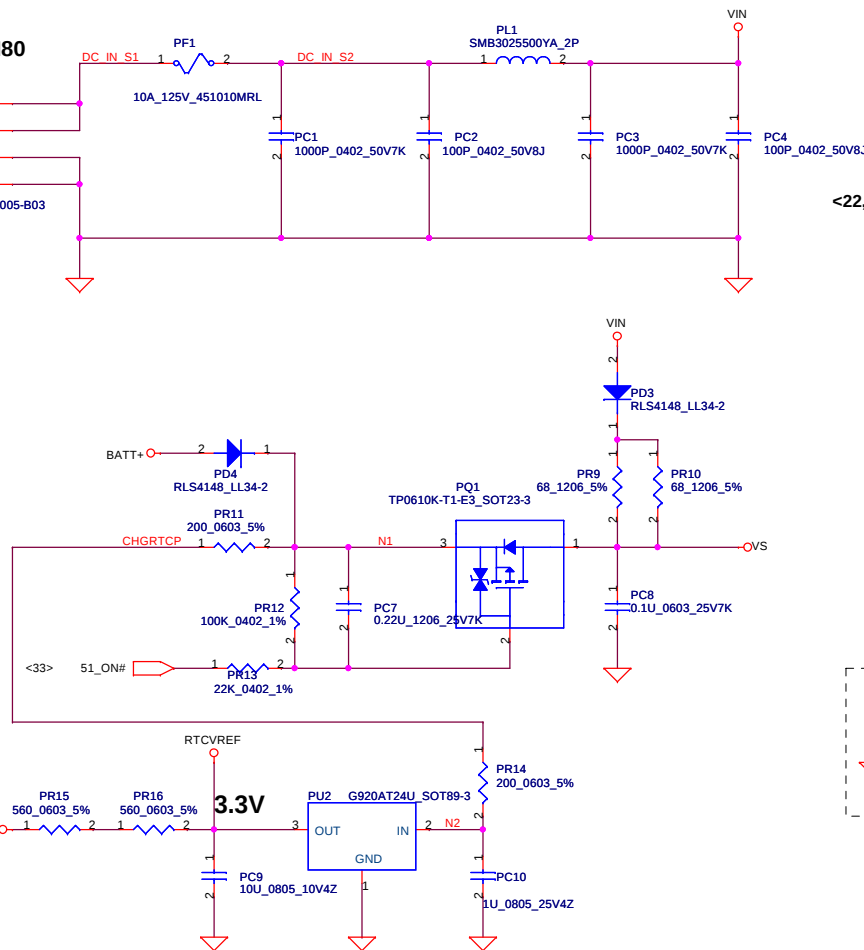


< Discharge circuit >



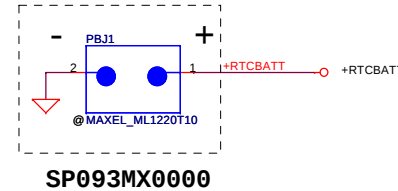
DC301001M80

@ SINGA_2DW-0005-B03



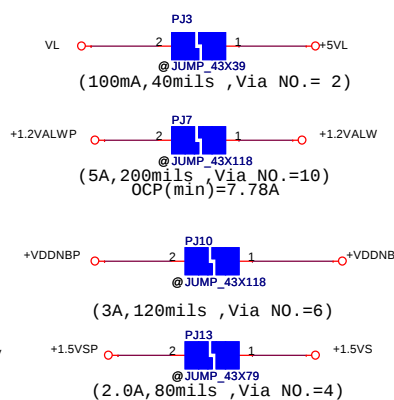
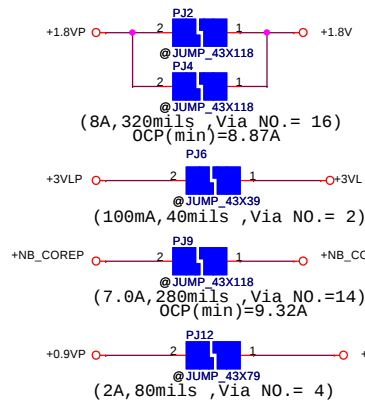
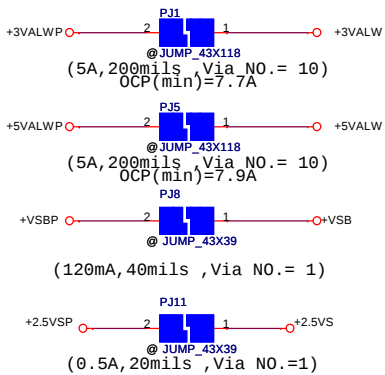
<22,32,33> ACIN

RTC Battery

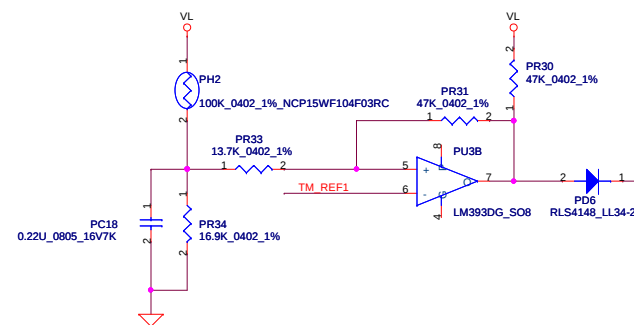
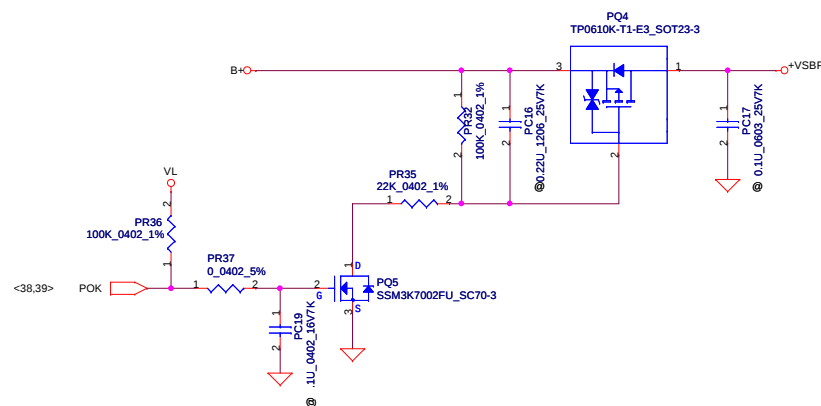
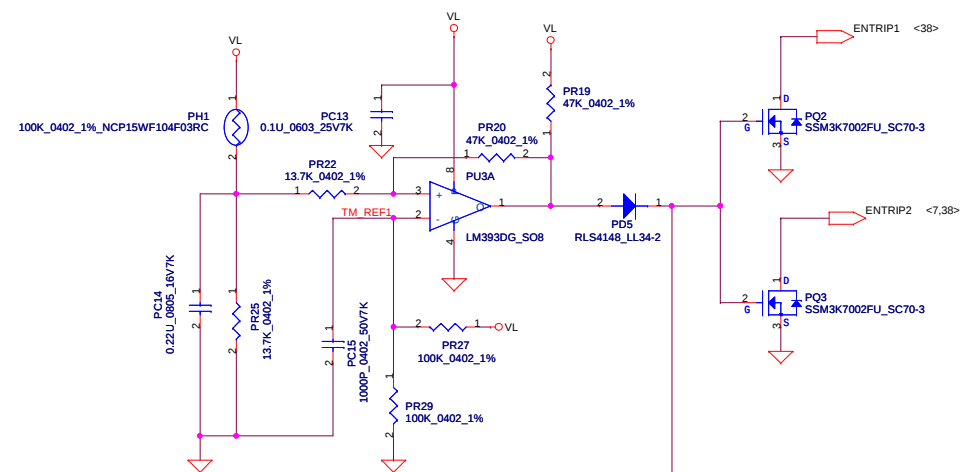
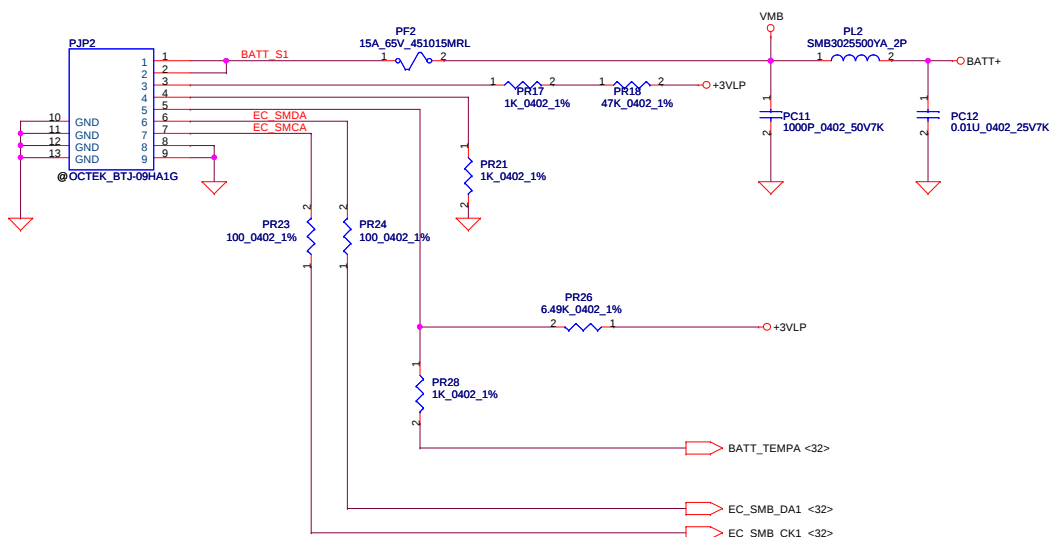


Vin Detector

High 18.384 17.901 17.430
Low 17.728 17.257 16.976

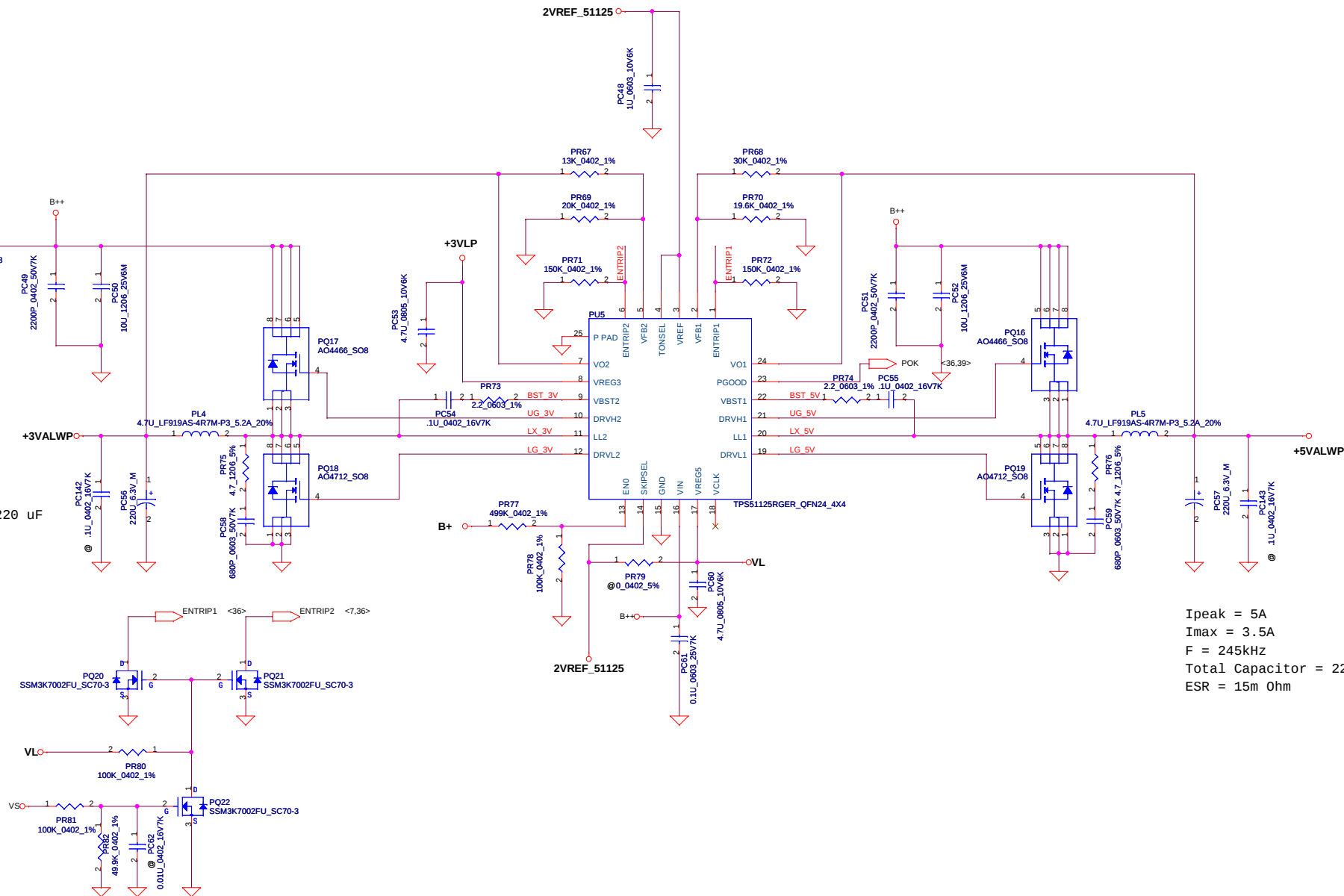


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						Size		Document Number		Rev	
								LA-5831P		1.0	
						Date:		Wednesday, August 12, 2009		Sheet 35 of 44	



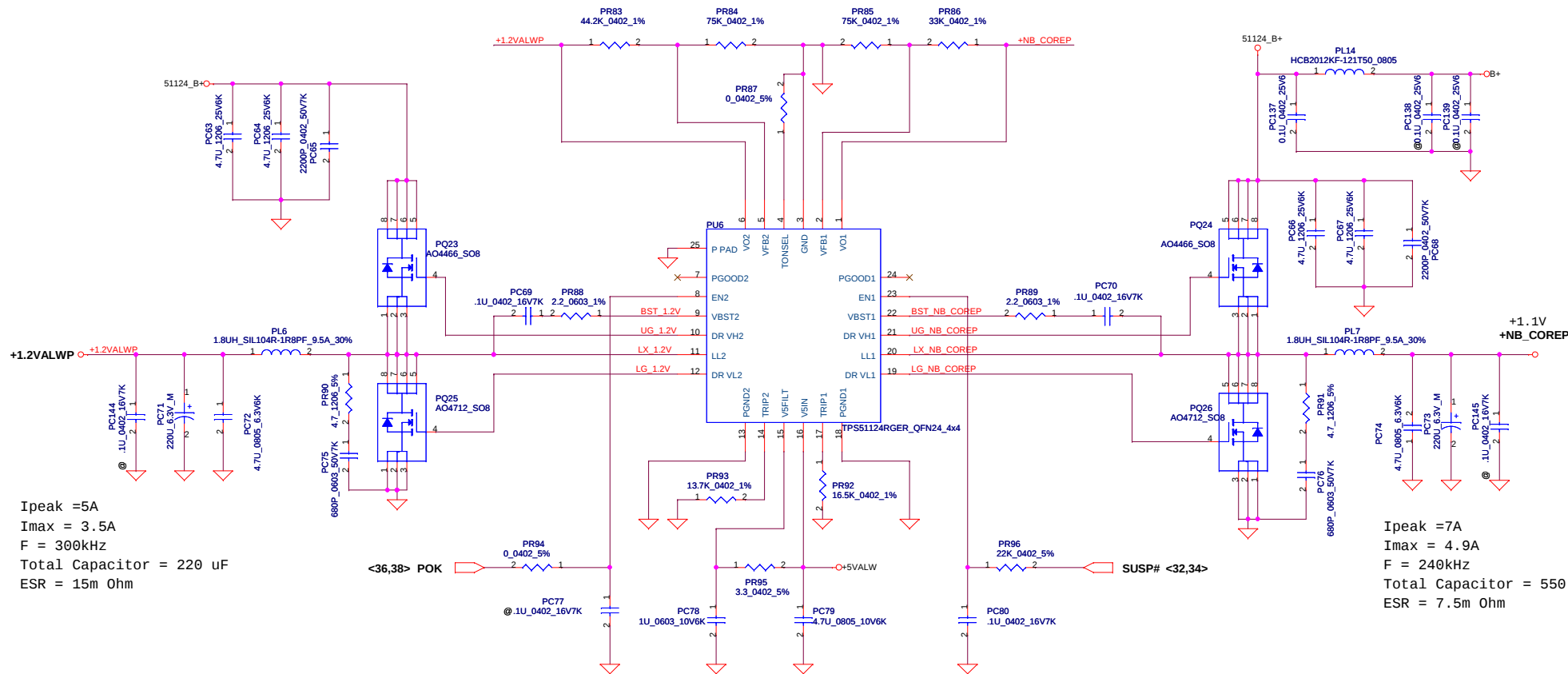
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			Date: Wednesday, August 12, 2009	Sheet 36 of 44

Ipeak = 5A
Imax = 3.5A
F = 305kHz
Total Capacitor = 220 uF
ESR = 15m Ohm

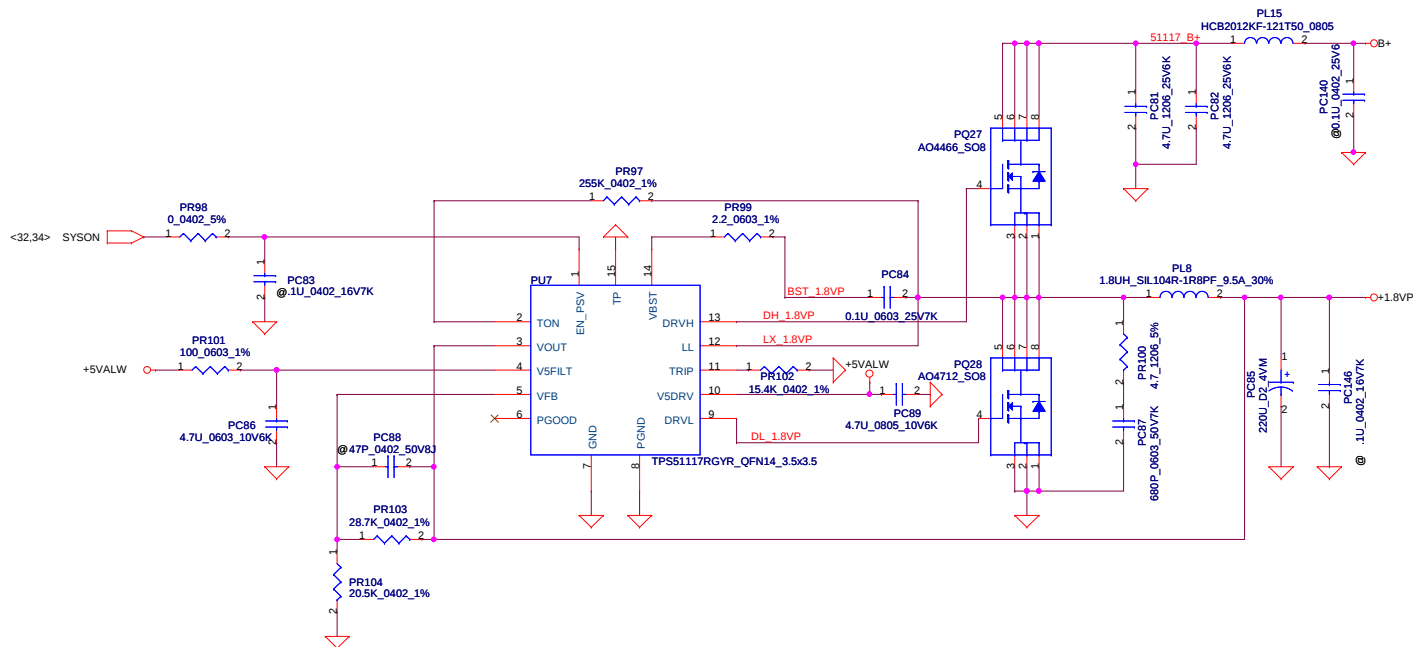


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Imax = 3.5A
F = 245kHz
Total Capacitor = 220 uF
ESR = 15m Ohm

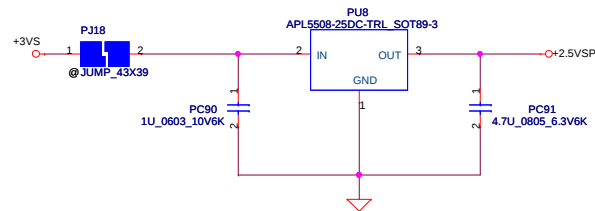
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Issued Date	2008/04/14	Deciphered Date	2009/04/14	3VALW/5VALW
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				Date: Wednesday, August 12, 2009
				Sheet 38 of 44



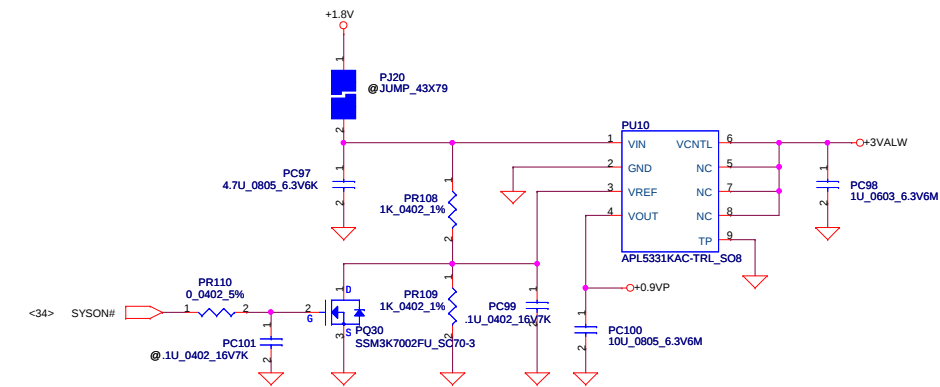
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Issued Date	2008/04/14	Deciphered Date	2009/04/14	Compal Electronics, Inc.	
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Date: Wednesday, August 12, 2009				Sheet	39 of 44



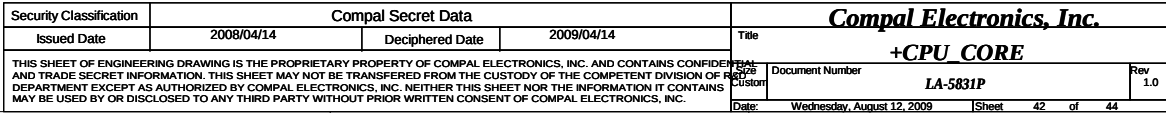
$I_{peak} = 8A$
 $I_{max} = 5.6A$
 $F = 312kHz$
 Total Capacitor = 220 μF
 ESR = 15m Ohm



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								Document Number	
								LA-5831P	
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				Document Number LA-5831P	
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Version Change List (P. I. R, List) for Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
35-43	PVT		2009/07/20	Release			
39-40	Pre-MP	Change PL6,PL7,PL8	2009/07/30	POWER		Change PL6,PL7,PL8 footprint	
38	Pre-MP	Change PC56	2009/07/30	POWER		change to common circuit.	
36	Pre-MP	Change PH1,PH2	2009/08/4	POWER		change to common circuit.	
37	Pre-MP	Change PR38,PR45	2009/08/4	POWER		change to common circuit.	

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HW4 Product Improvement Record (P.I.R.)

NBWA E LA-5831P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 1.0
GERBER-OUT DATE: 2009/08/07

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	7/21	25	Change JUSBB footprint back to E-T_6905-E12N-00R_12P	USB/B pin define reverse
2	7/27	25	Add D11	For ESD
3	7/27	9	Add C120-C123	For EMI
4	7/27	32	Add R344 and R345	For EC pin damage issue
5	7/30	26	Add R97, R98 and R105	Reserve bead for EMI
6	8/6	18	Add C707, C708 and C709	For EMI
7	8/6	30	Add LA11 and LA12	For EMI
8	8/6	32	Add R74 and C607	For EMI
9	8/6	31	Delete R518 and C606	For EMI
10	8/6	7	Add C124	For EMI

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