SAPPORO 150A+G

LA-2101 REV0.1 Schematic

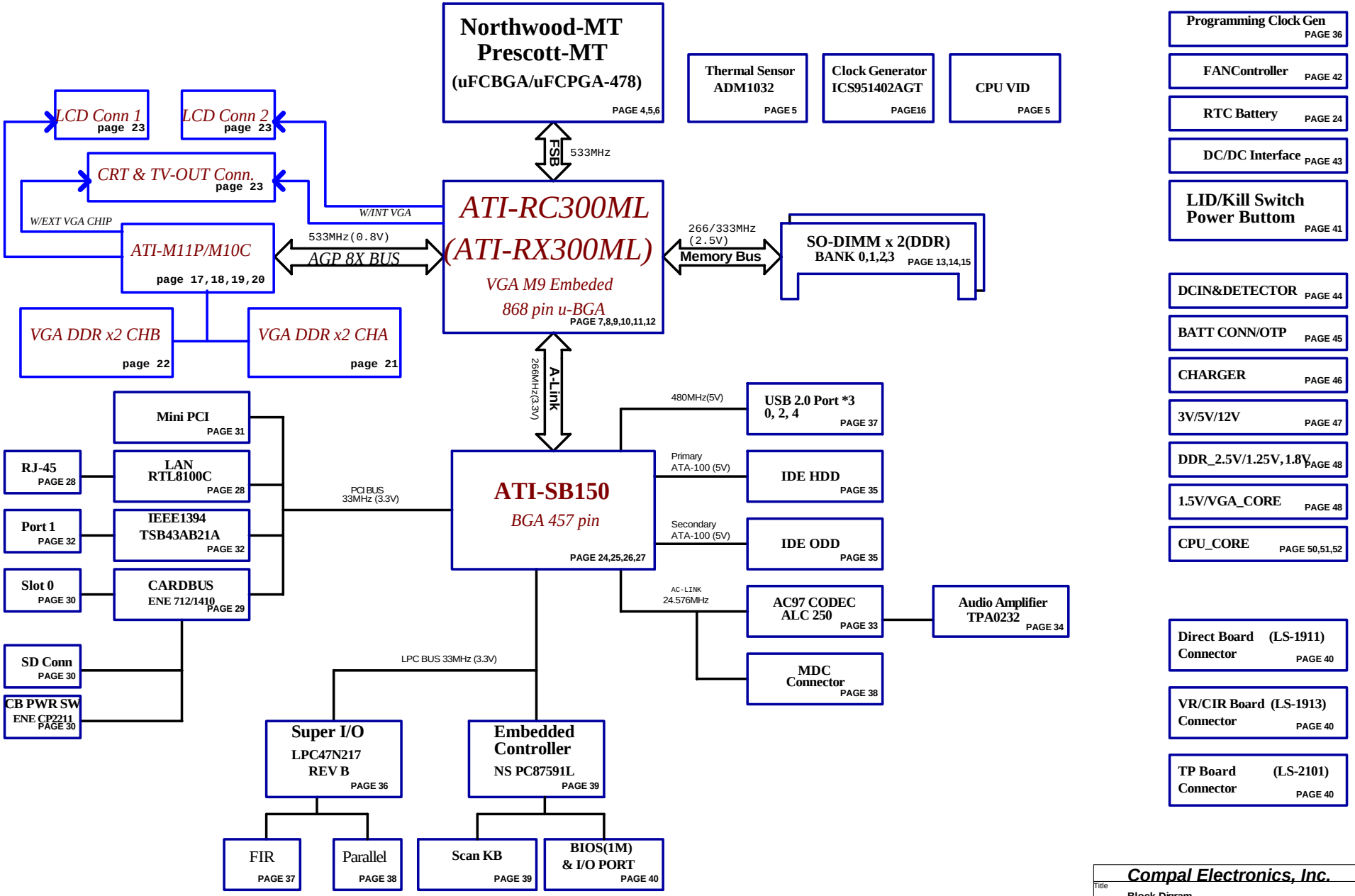
Portability Prescott/Northwood

RC300ML(RX300ML)+IXP150+ATI M11P/M10C(128MB VRAM)

2003-11-10

Compal Electronics, Inc.		
Title: Cover Page		
Size: B	Document Number	Rev: 0.1
Date: Tuesday, November 18, 2003	Sheet 1 of 52	

DAL01 LA-2101 BLOCK DIAGRAM



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Title: Block Digram			
Size: Custom	Document Number		Rev 0.1
Date: Tuesday, November 18, 2003	Sheet 2 of 52		

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPUVID	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+VGA_CORE	1.0V/1.2V switched power rail for VGA chip	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	AGP 4X/8X	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF
+2.5VALW	2.5V always on power rail	ON	ON	ON*
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
VGA	AD16		PIRQA
CardBus	AD20	2	PIRQA
LAN	AD19	3	PIRQD
Mini-PCI	AD18	1/4	PIRQC/PIRQD
1394	AD16	0	PIRQA
SD	AD20	2	PIRQB

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
(24C04)	1011 000Xb

EC SM Bus2 address

Device	Address
ADM1032	1001 110X b
ICS960011	1101 110X b

IXP150 SM Bus address

Device	Address
Clock Generator (ICS951402AGT)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM2	1010 001Xb

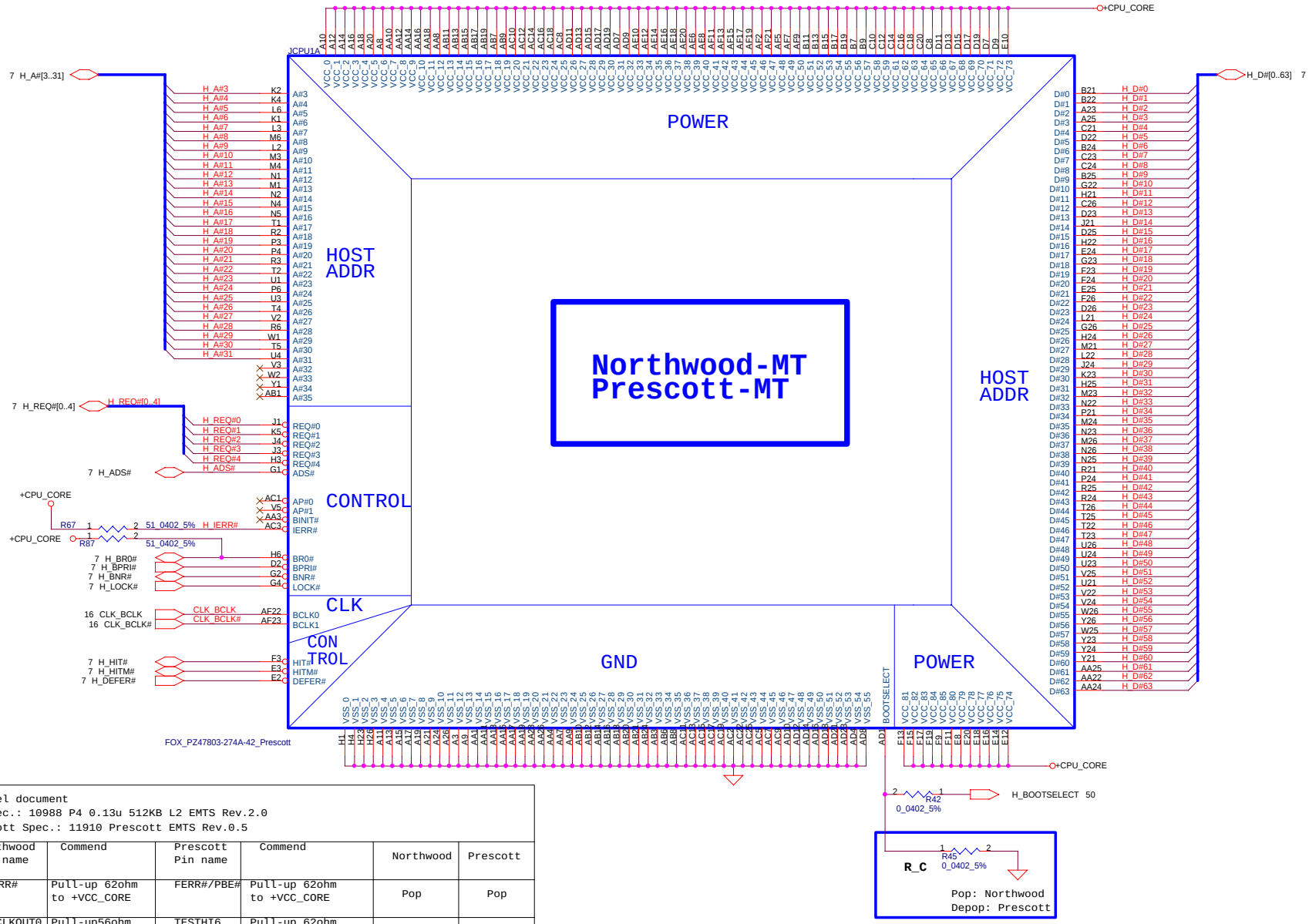
STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	



Reference Intel document
Desktop P4 Spec.: 10988 P4 0.13u 512KB L2 EMTS Rev.2.0
Desktop Prescott Spec.: 11910 Prescott EMTS Rev.0.5

Pin number	Northwood Pin name	Commend	Prescott Pin name	Commend	Northwood	Prescott
B6	FERR#	Pull-up 62ohm to +VCC_CORE	FERR#/PBE#	Pull-up 62ohm to +VCC_CORE	Pop	Pop
AA20	ITPCLKOUT0	Pull-up56ohm to +VCC_CORE	TESTHI6	Pull-up 62ohm to +VCC_CORE	Pop	Pop
AB22	ITPCLKOUT1	Pull-up 56ohm to +VCC_CORE	TESTHI7	Pull-up 62ohm to +VCC_CORE	Pop	Pop
AD2	NC	float	VIDPWRGD	Pull-up 8.2Kohm to +VCCVID	Depop	Pop
AD3	NC	float	VID5	Pull-up1Kohm to +3VRUN & connect to PWRIC	Depop	Pop
AF3	NC	float	VCCVIDLB	Connect to +VCCVID	Depop	Pop
AD20	VCCA	Connect to CPU Filter	VCCIOPLL	Connect to CPU Filter		
AF23	VCCIOPLL	Connect to CPU Filter	VCCA	Connect to CPU Filter		
AD1	VSS	Connect to GND	BOOTSELECT	CPU determine	Pop	Depop
AE26	VSS	Connect to GND	OPTIMIZED/ COMPAT#	float	Pop	Depop

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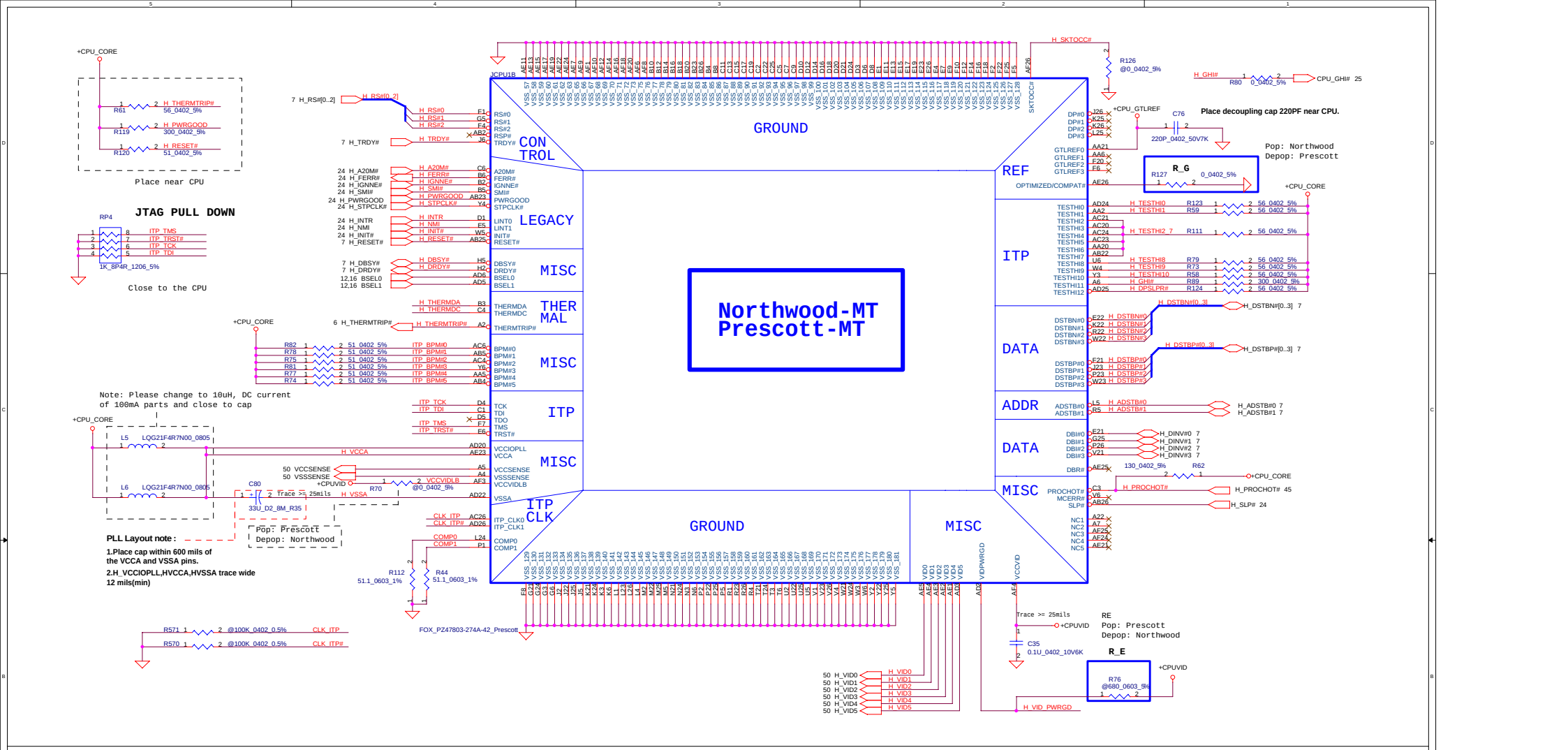
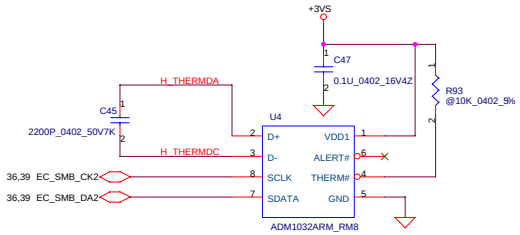
Title: **Prescott Processor in uFCPGA478 (1/2)**

Size: Custom | Document Number: **LA-2101** | Rev: 0.1

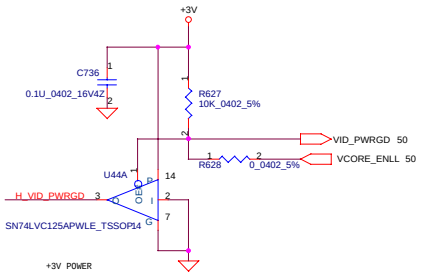
Date: Saturday, November 22, 2003 | Sheet 4 of 52



Thermal Sensor



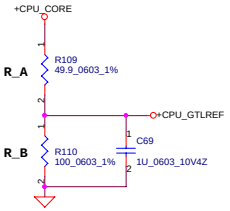
VID PWRGD Circuit

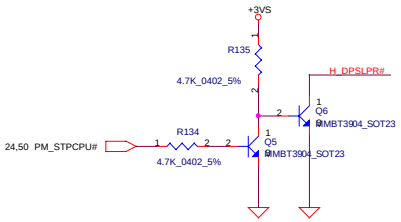


GTL Reference Voltage

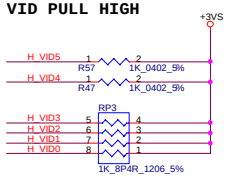
Layout note :

1. Place R_A and R_B near CPU (Within 1.5").
2. +CPU_GTLREF Trace wide 12mils(min),Space 15mils





VID PULL HIGH



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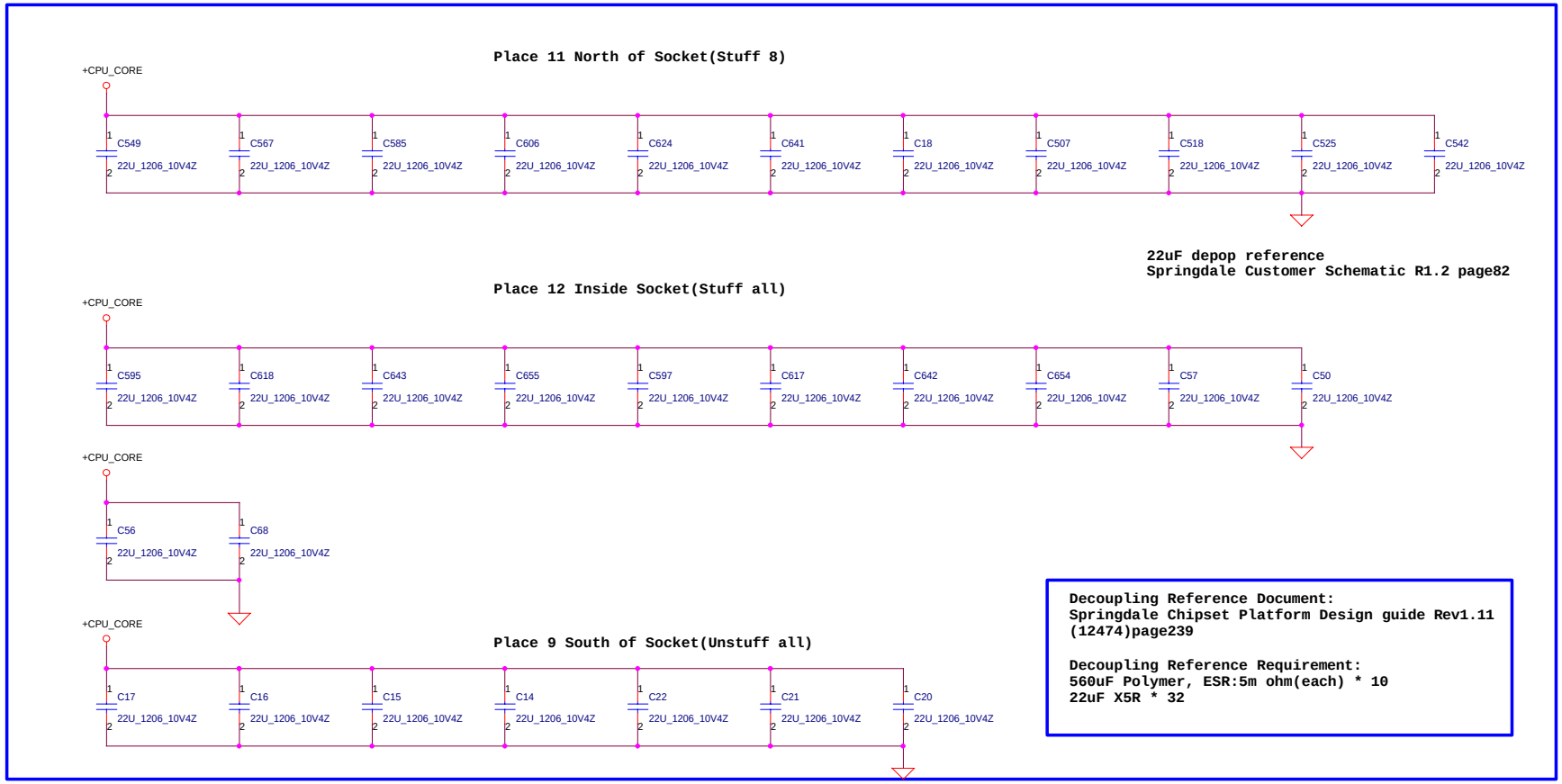
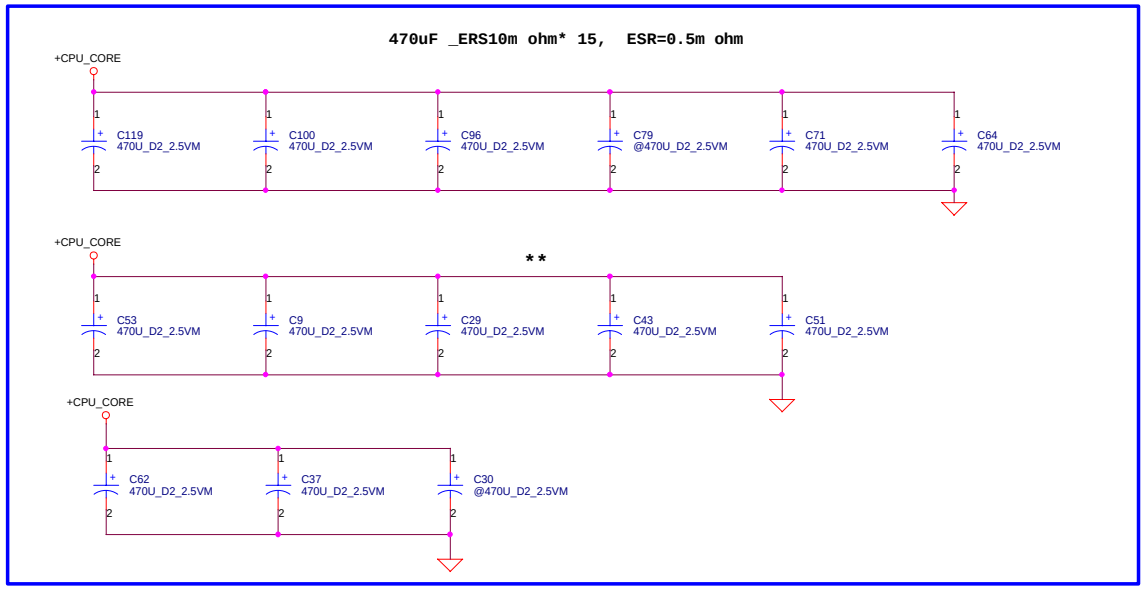
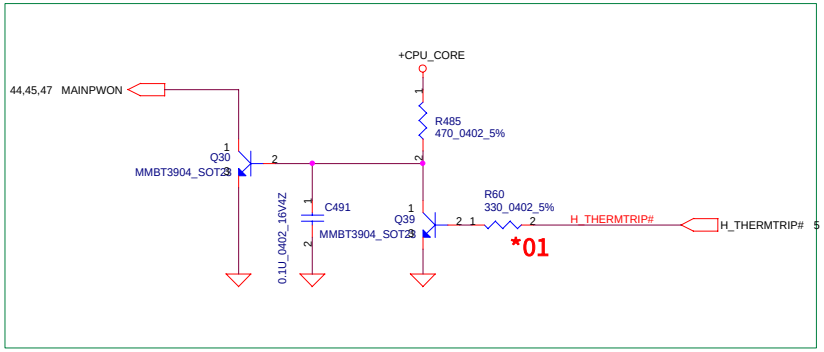
Size C	Document Number LA-2101
Rev	0.1
Date: Saturday, November 22, 2003	Sheet 5 of 52







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Title	CPU Decoupling	
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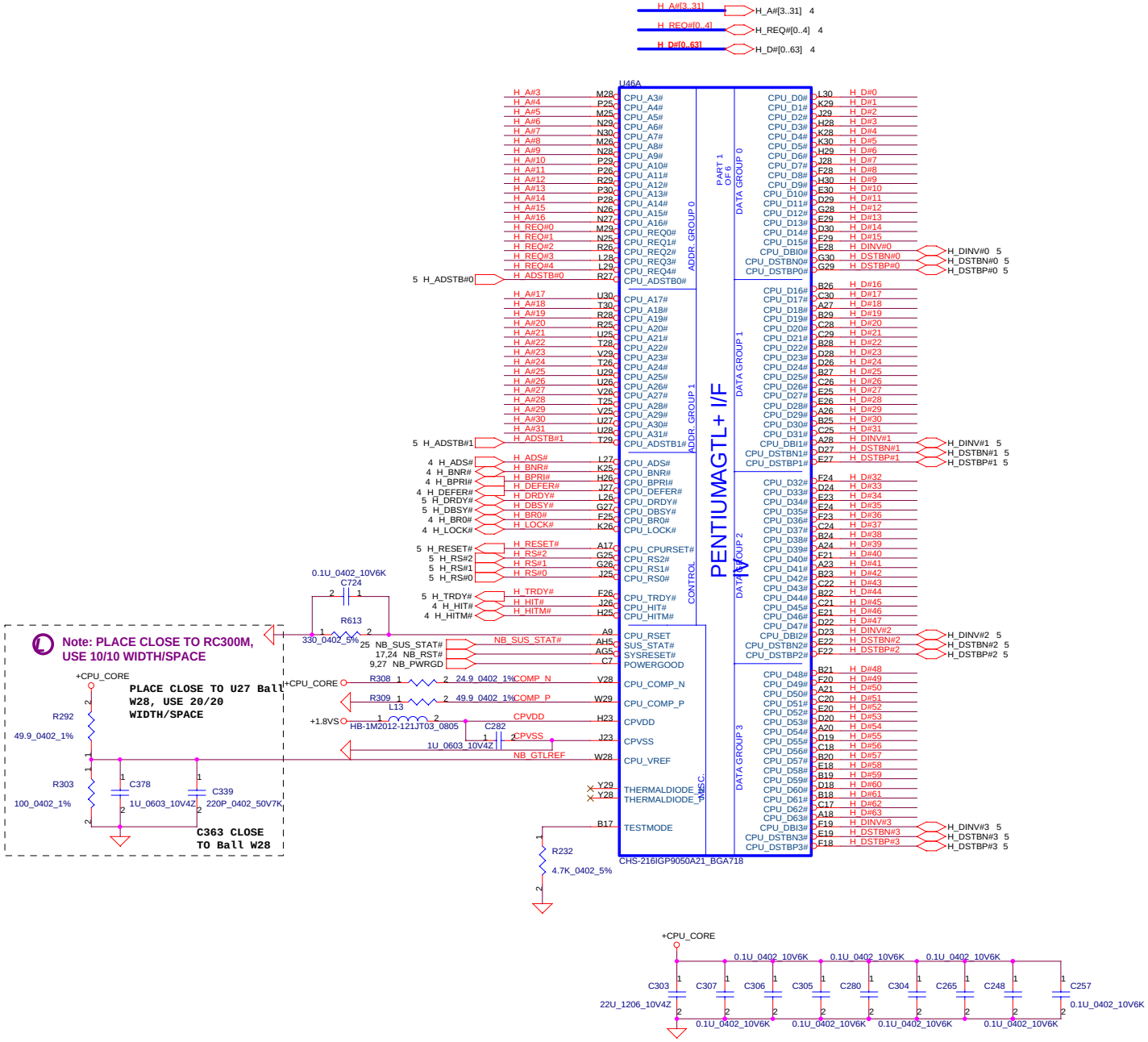
Date: Saturday, November 22, 2003	Sheet 6 of 52	



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Title	ATI RC300M-AGTL+
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Rev	0.1
Date: Saturday, November 22, 2003	Sheet 7 of 52

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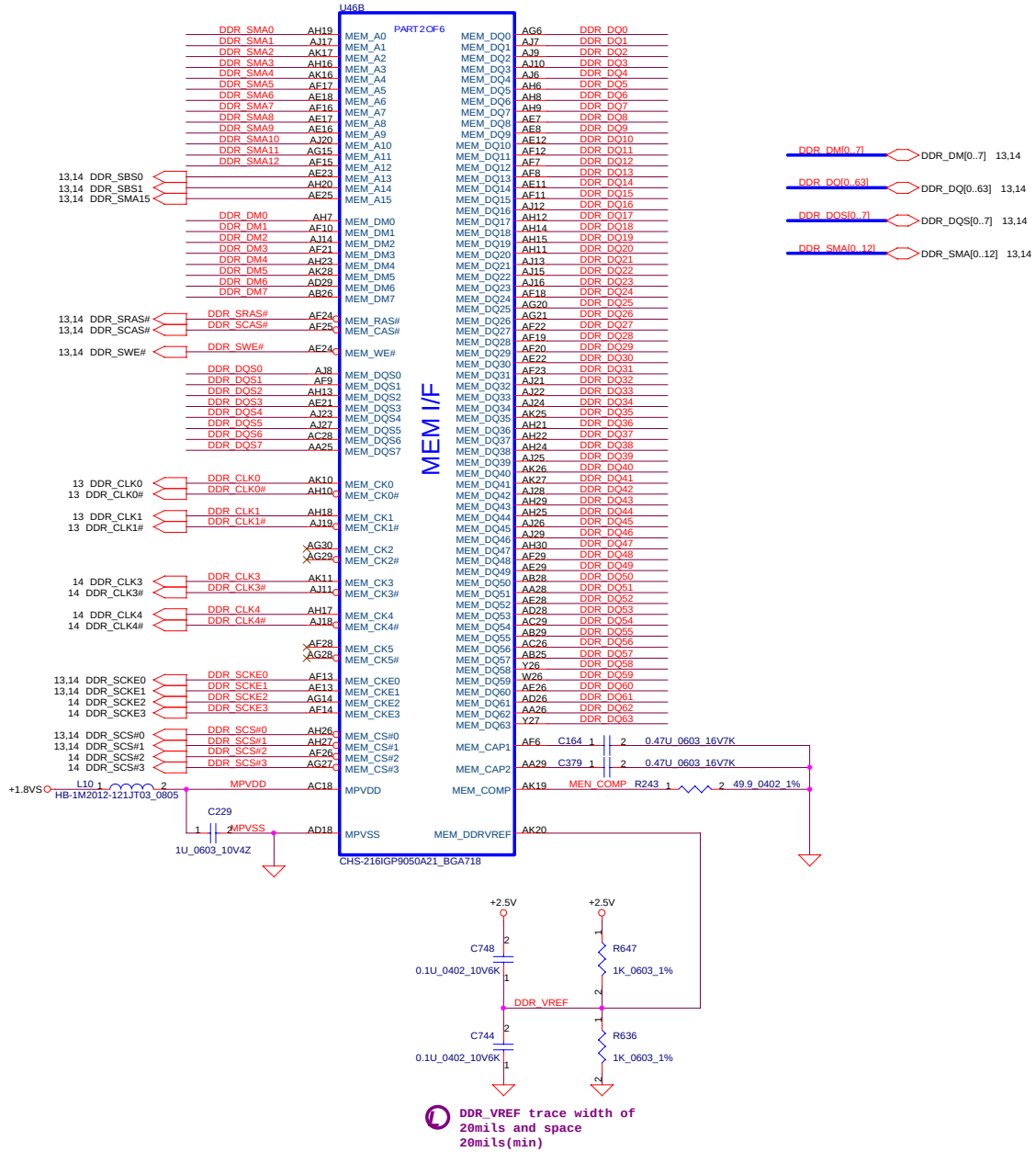

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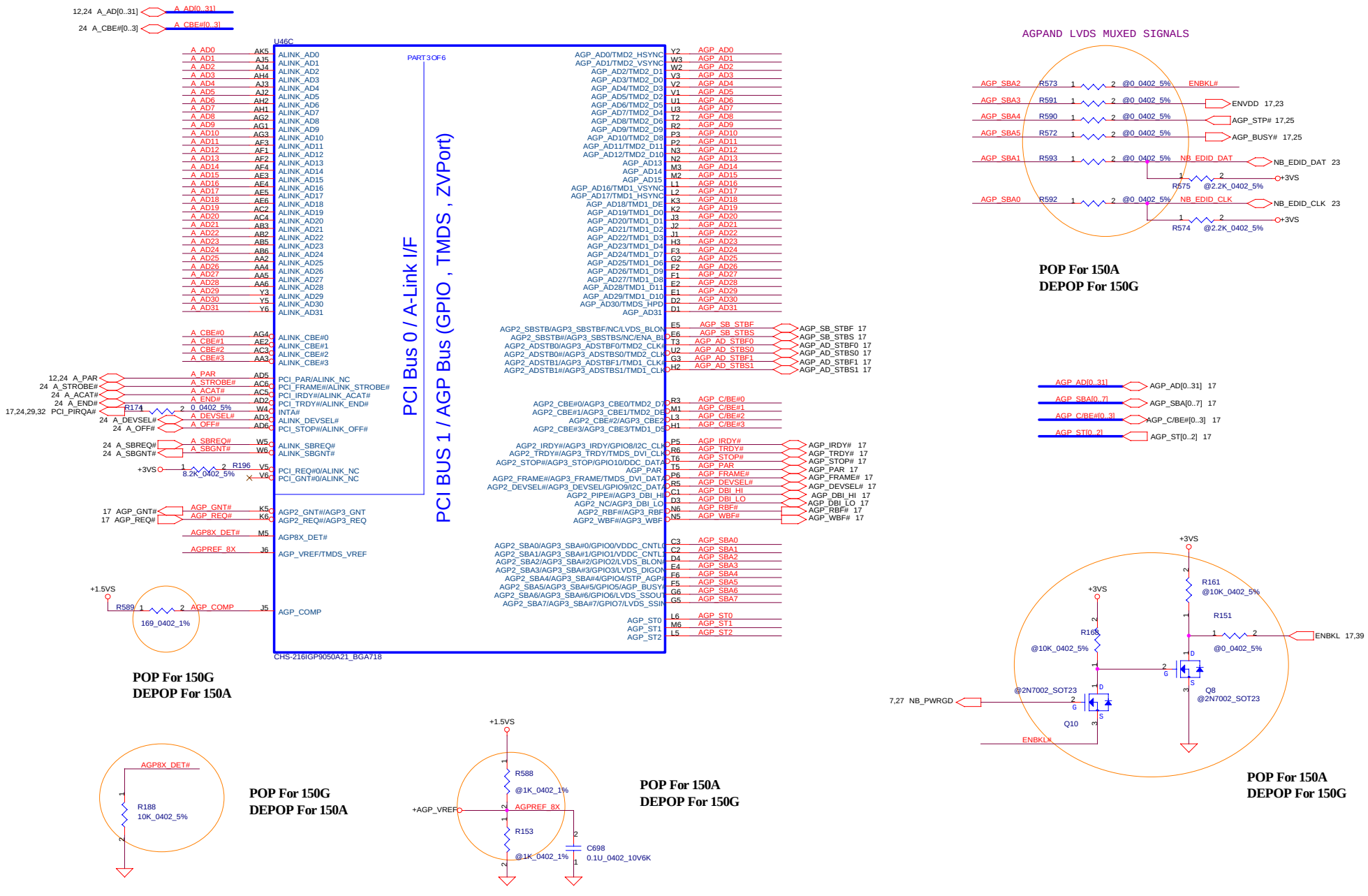
Date: Saturday, November 22, 2003	Sheet 8 of 52	



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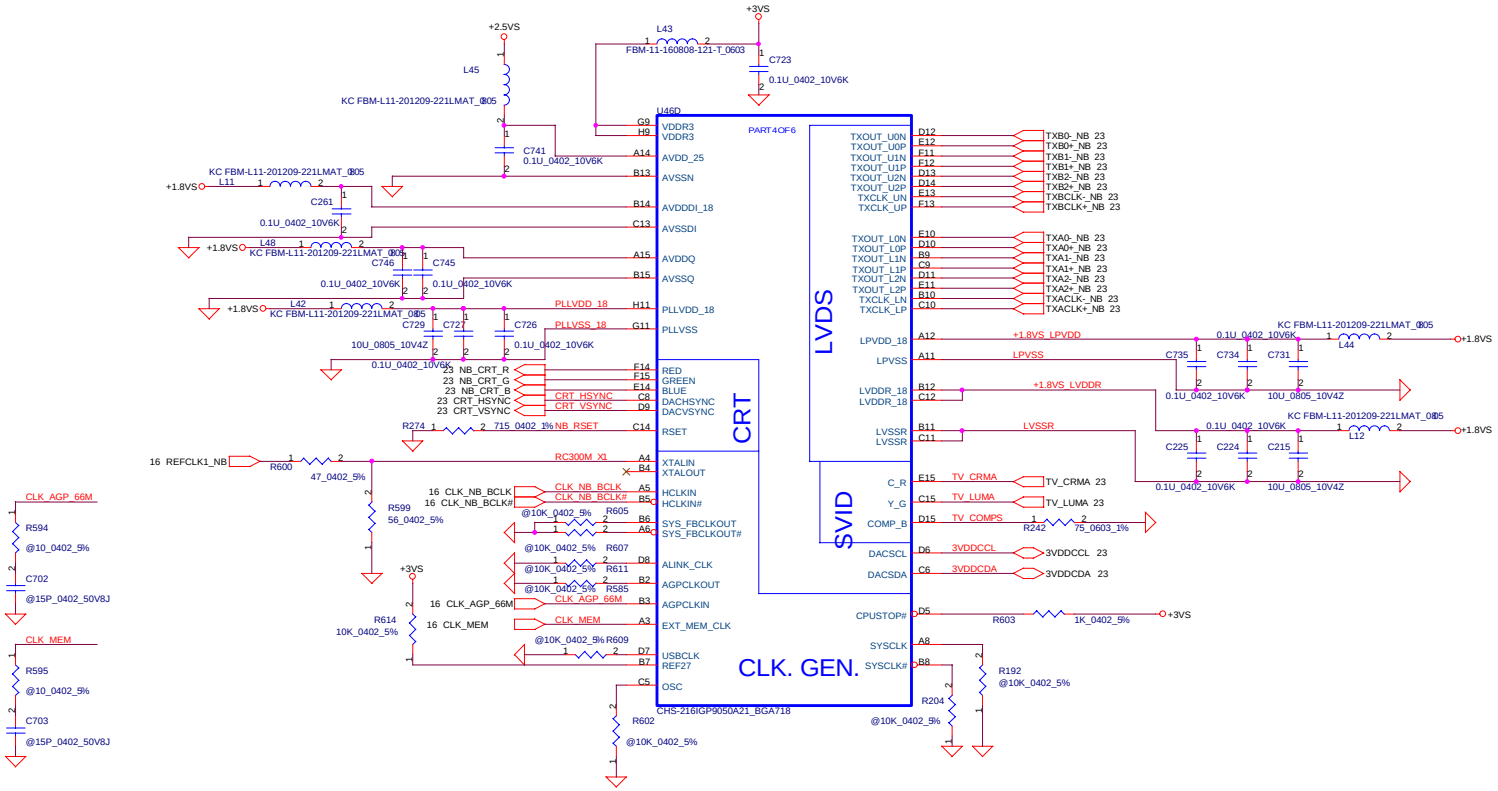
Size	Document Number LA-2101		Rev 0.1
Date: Saturday, November 22, 2003	Sheet 9 of 52		



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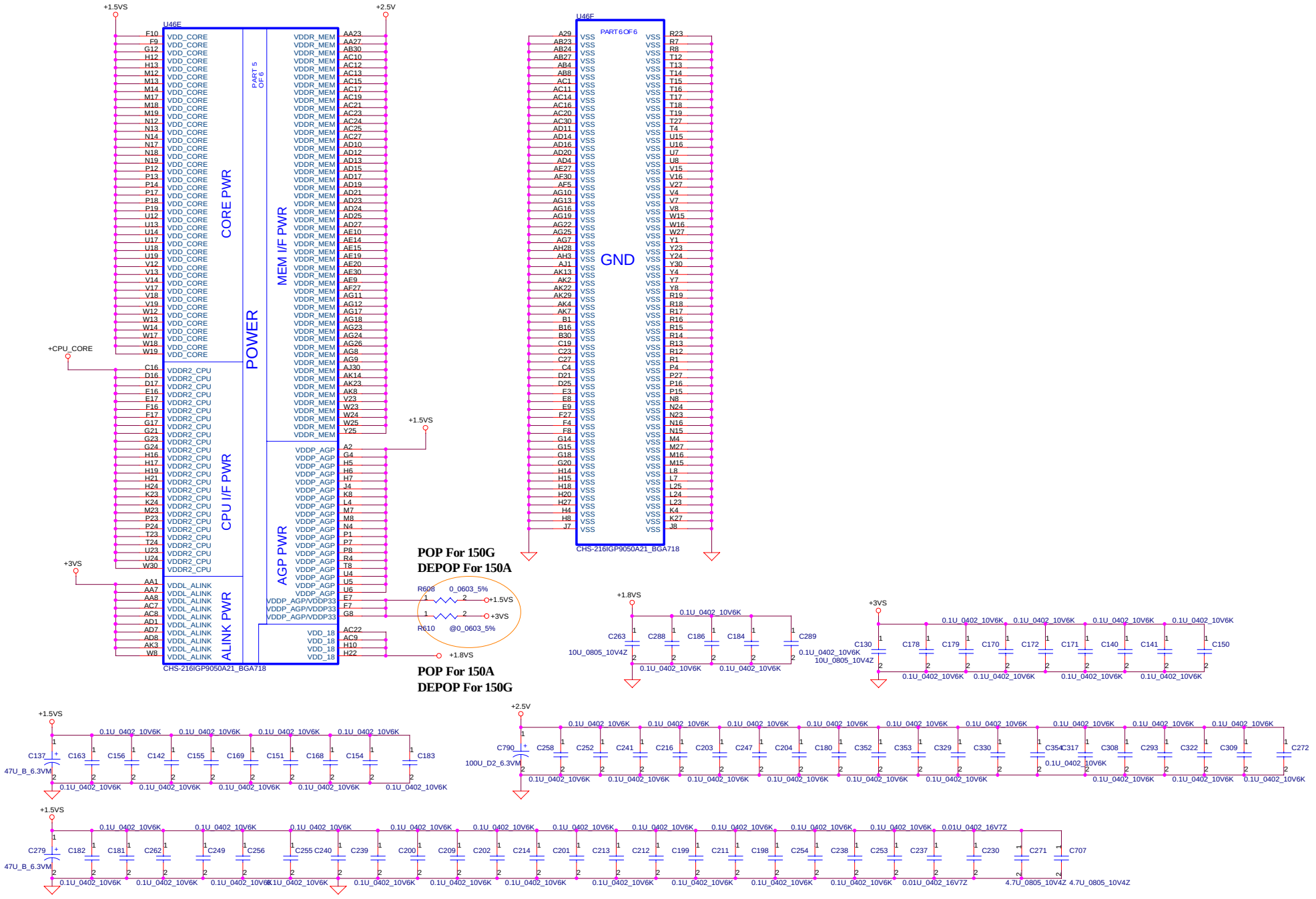
Size	Document Number **LA-2101**	Rev 0.1
Date: Saturday, November 22, 2003	Sheet 10 of 52	



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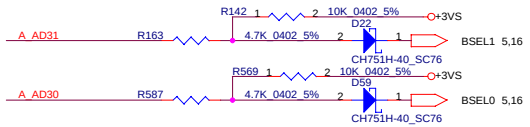
Title	ATI RC300M-POWER
Size	Document Number: LA-2101
Rev	0.1
Date: Tuesday, November 18, 2003	Sheet 11 of 52

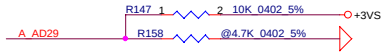
9,24 A_AD[0..31] A_AD[0..31]



A_AD[31..30] : FSB CLK SPEED

DEFAULT: 01

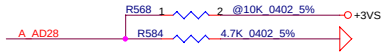
00: 100 MHZ
01: 133 MHZ
10: 200MHZ
11:166 MHZ



A_AD29: STRAP CONFIGURATION

DEFAULT:1

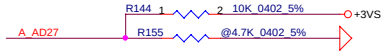
0: REDUCEDE SET
1: FULL SET



A_AD28: SPREAD SPECTRUM ENABLE

DEFAULT:0

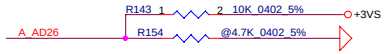
0: DISABLE
1: ENABLE



A_AD27: FrcShortReset#

DEFAULT: 1

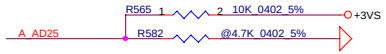
0: TEST MODE
1: NORMAL MODE



A_AD26 : ENABLE IOQ

DEFAULT: 1

0: IOQ=1
1: IOQ=12



A_AD25/A_AD17 : CPU VOLTAGE[1..0]

DEFAULT: 10

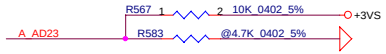
00: 1.05V
01: 1.35V
11: 1.75V
10: 1.45V

AD25=1 DESTOP CPU
AD25=0 MOBILE CPU
AD17--DON'T CARE

A_AD24 : MOBILE CPU SELECT

DEFAULT: 1

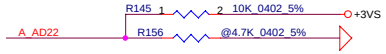
0: BANIAS CPU
1: OTHER CPU



A_AD23 : CLOCK BYPASS DISABLE

DEFAULT: 1

0: TEST MODE
1: NORMAL



A_AD22 : OSC PAD OUTPUT PCICLK

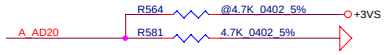
DEFAULT : 1

0: PCICLK OUT
1: OSC CLK OUT

A_AD21 : AUTO_CAL ENABLE

DEFAULT : 1

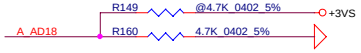
0: DISABLE
1: ENABLE



A_AD20 : INTERNAL CLK GEN ENABLE

DEFAULT : 0

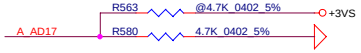
0: DISABLE
1: ENABLE



A_AD18 : ENABLE PHASE CALIBRATION

DEFAULT: 0

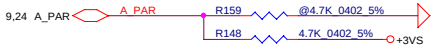
0: DISABLE
1:ENABLE



A_AD25/A_AD17 : CPU VOLTAGE[1..0]

DEFAULT: 0

00: 1.05V
01: 1.35V
11: 1.75V
10: 1.45V



PAR: EXTENDED DEBUG MODE

DEFAULT : 1

0: DEBUG MODE
1: NORMAL

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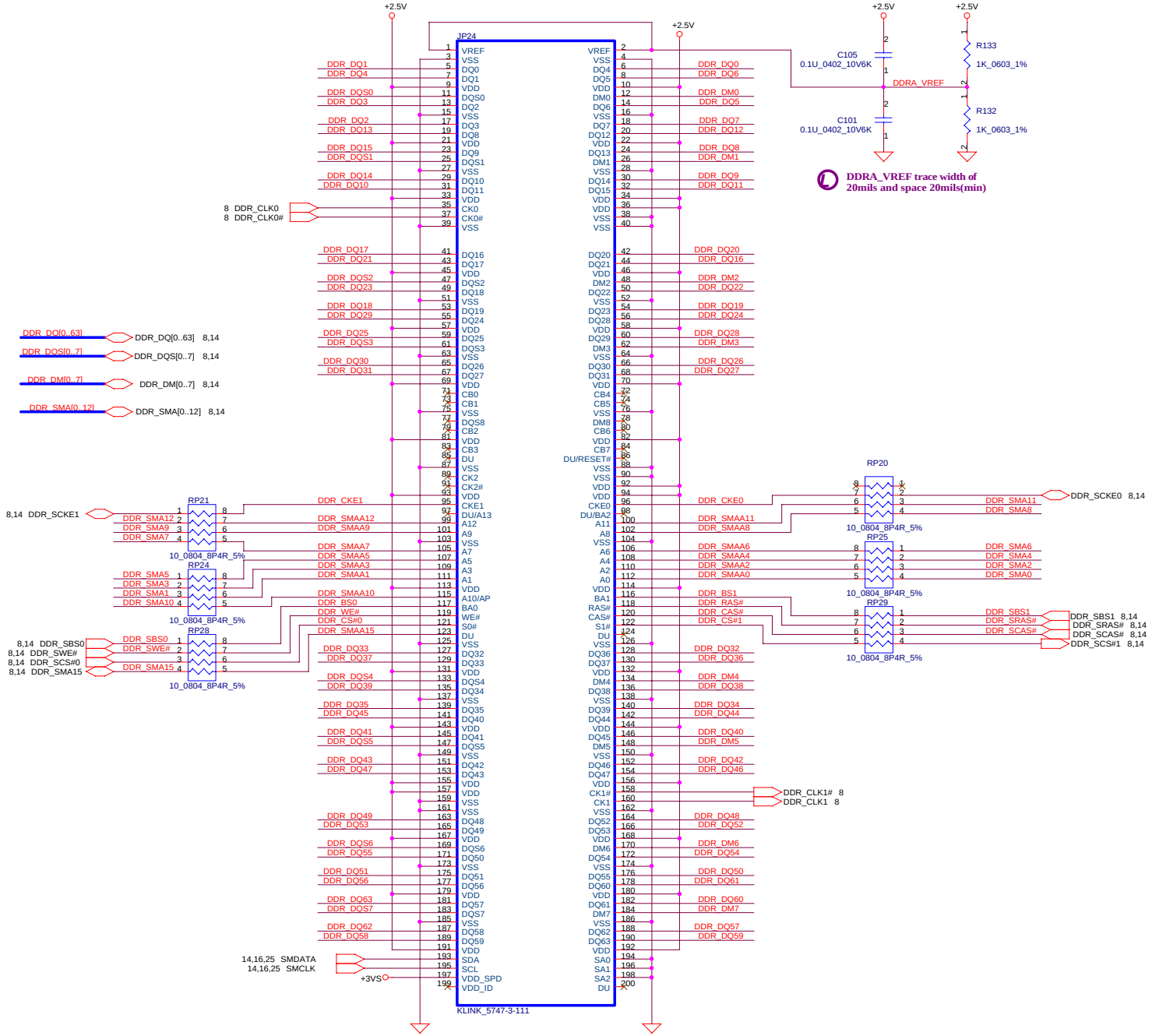
Title	ATI RC300M-SYSTEM STRAP		
Size	Document Number LA-2101		Rev 0.1
Date: Saturday, November 22, 2003	Sheet 12 of 52		



Layout note

Layout note
Place Add/Command resisotrs
Close to Pin, max L = 300 mils

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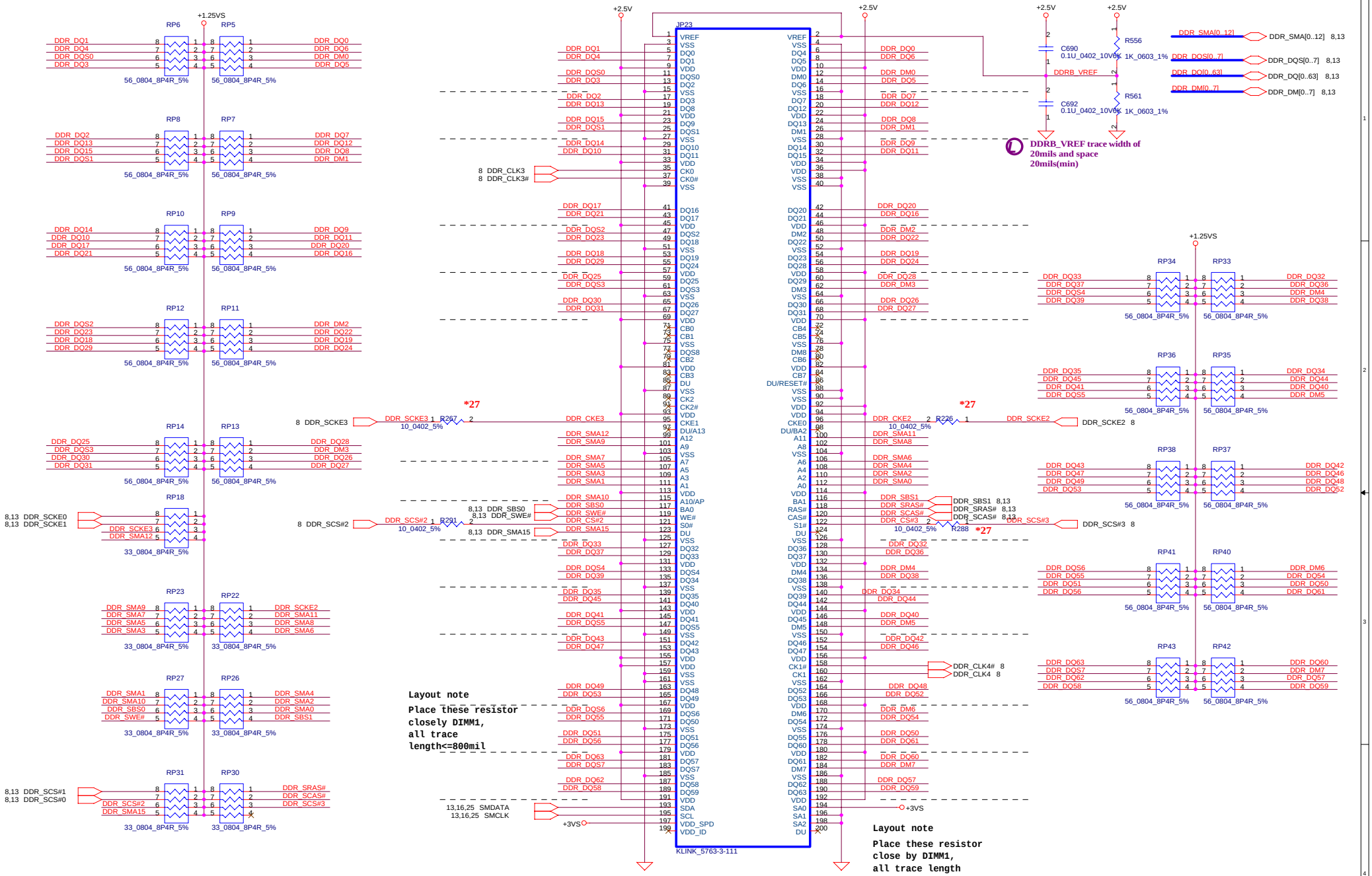
Title	**DDR-SODIMM SLOT0**		
Size	Document Number **LA-2101**		Rev 0.1
Date: Saturday, November 22, 2003	Sheet 13 of 52		



DDR TOPOLOGY 1 FOR SMAA[0, 3, 6:12], SBA[1, 0], SRAS#, SCAS#, SWE#

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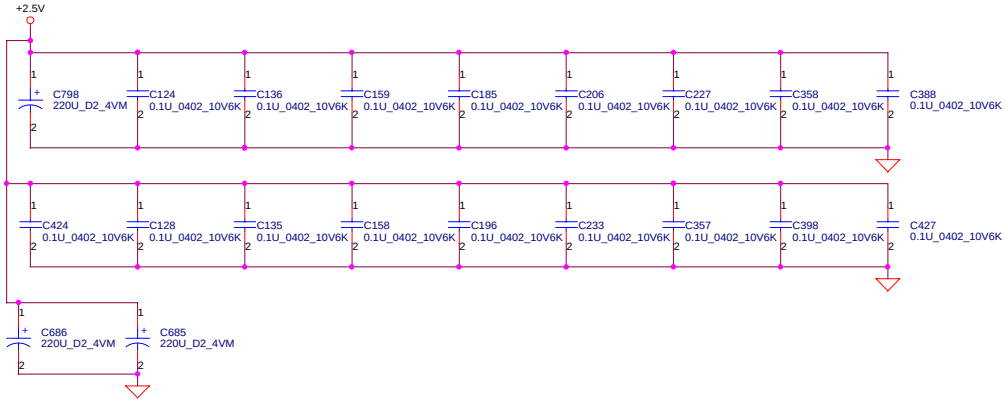
Compal Electronics, Inc.	
Title	DDR-SODIMM SLOT1
Size	Document Number: LA-2101
Rev	0.1
Date: Saturday, November 22, 2003	Sheet 14 of 52

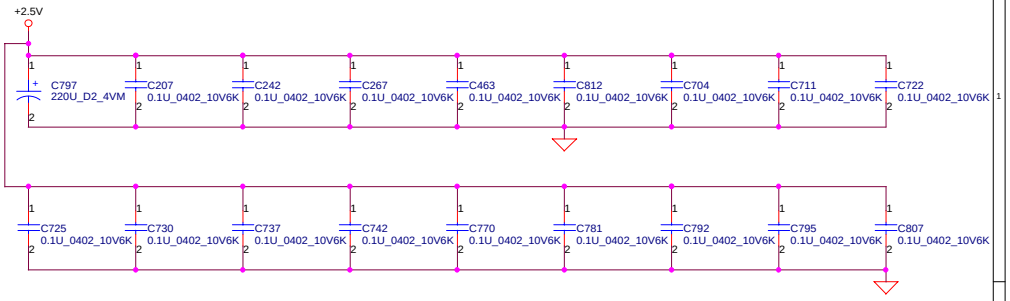
Layout note :

Distribute as close as possible to DDR-SODIMM0.



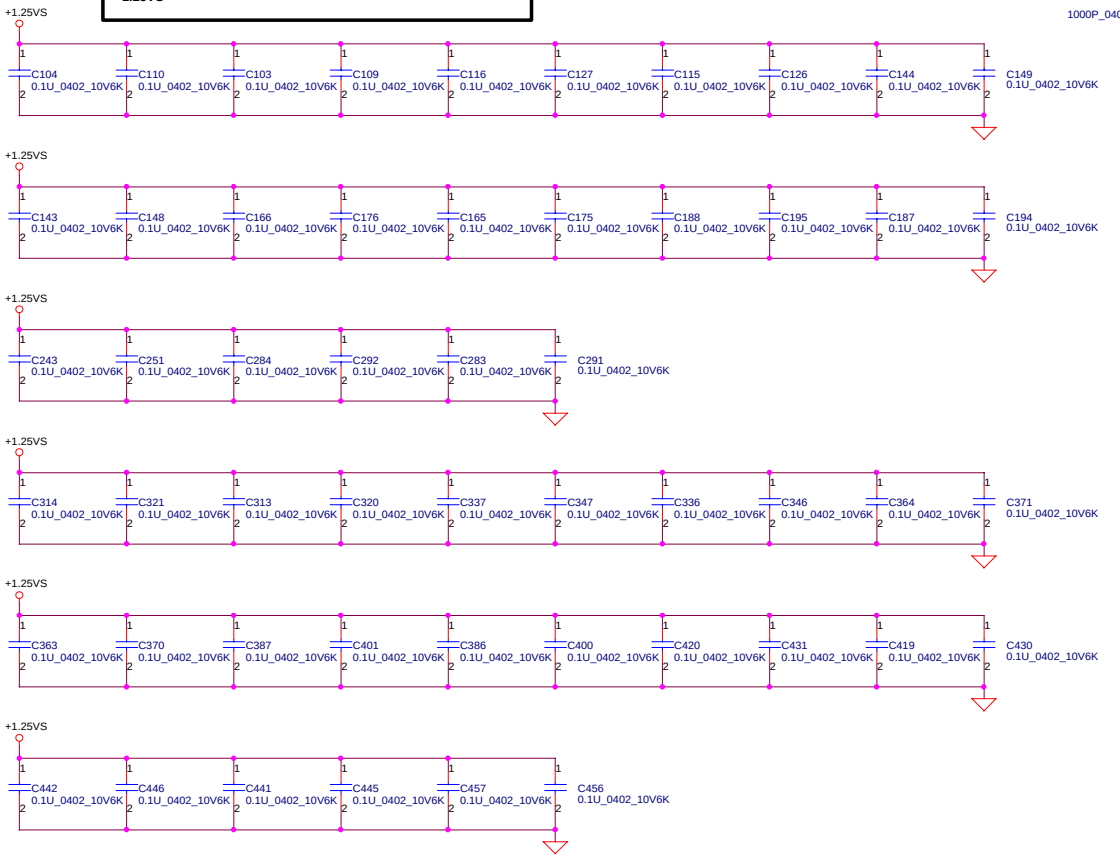
Layout note :

Distribute as close as possible to DDR-SODIMM1.



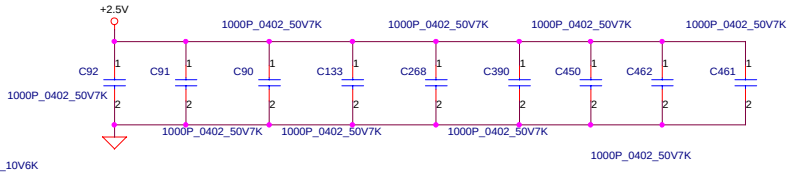
Layout note :

Place one cap close to every 2 pull up resistors termination to +1.25VS



Layout note :

for EMI solution



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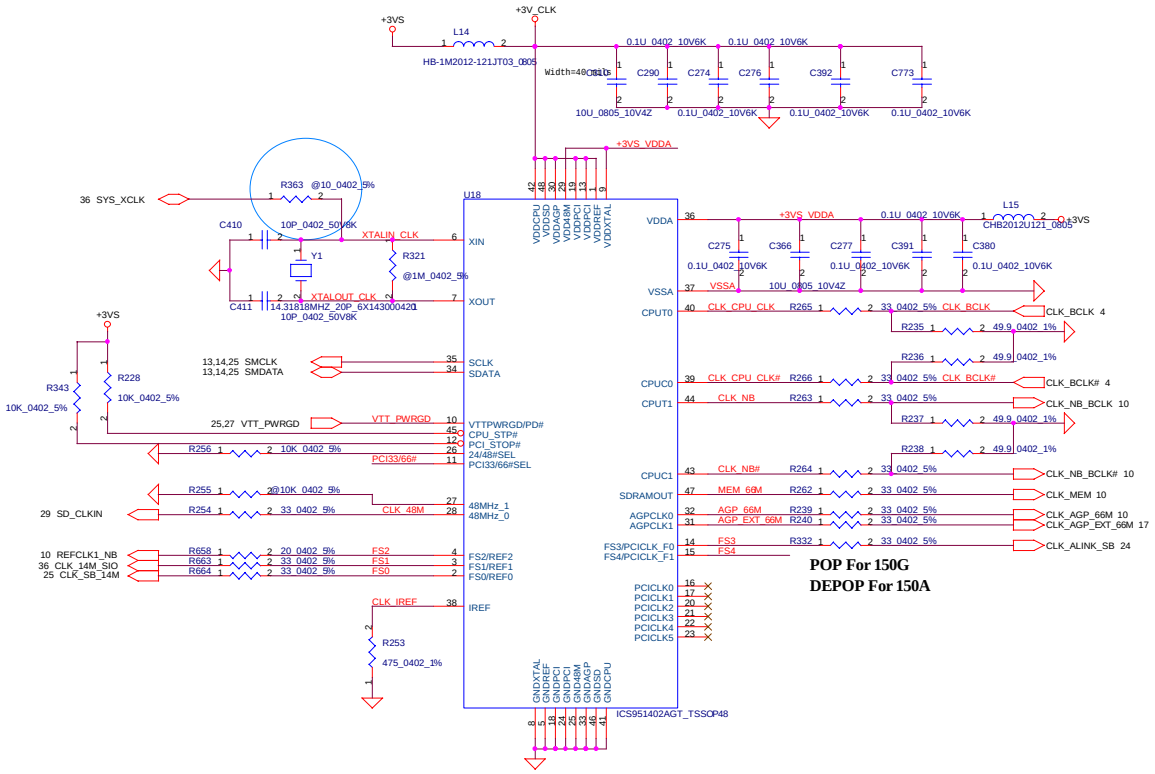
Compal Electronics, Inc.		
Title: **DDR SODIMM Decoupling**		
Size	Document Number: **LA-2101**	Rev 0.1
Date: Tuesday, November 18, 2003	Sheet 15 of 52	



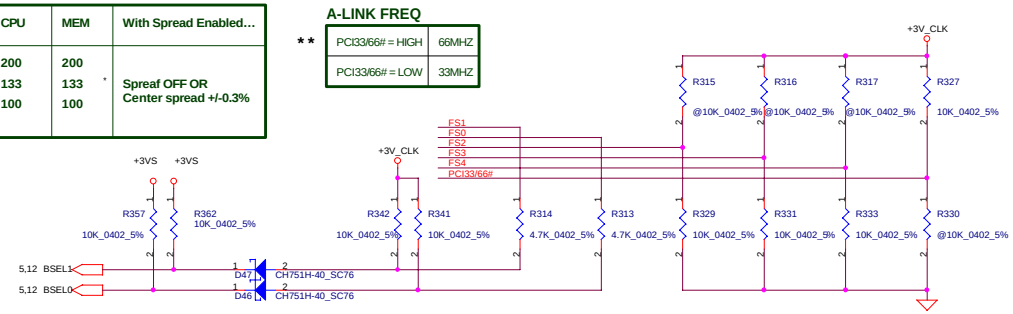
POP For 150G
DEPOP For 150A

CLOCK FREQUENCY SELECT TABLE

FS4	FS3	FS2	FS1	FS0	CPU	MEM	With Spread Enabled…
0	0	0	1	0	200	200	
** 0	0	0	0	1	133	133	Spreaf OFF OR Center spread +/-0.3%
0	0	0	0	0	100	100	

A-LINK FREQ

**	PCI33/66# = HIGH	66MHZ
	PCI33/66# = LOW	33MHZ



Note: 0 = PULL LOW
1 = PULL HIGH

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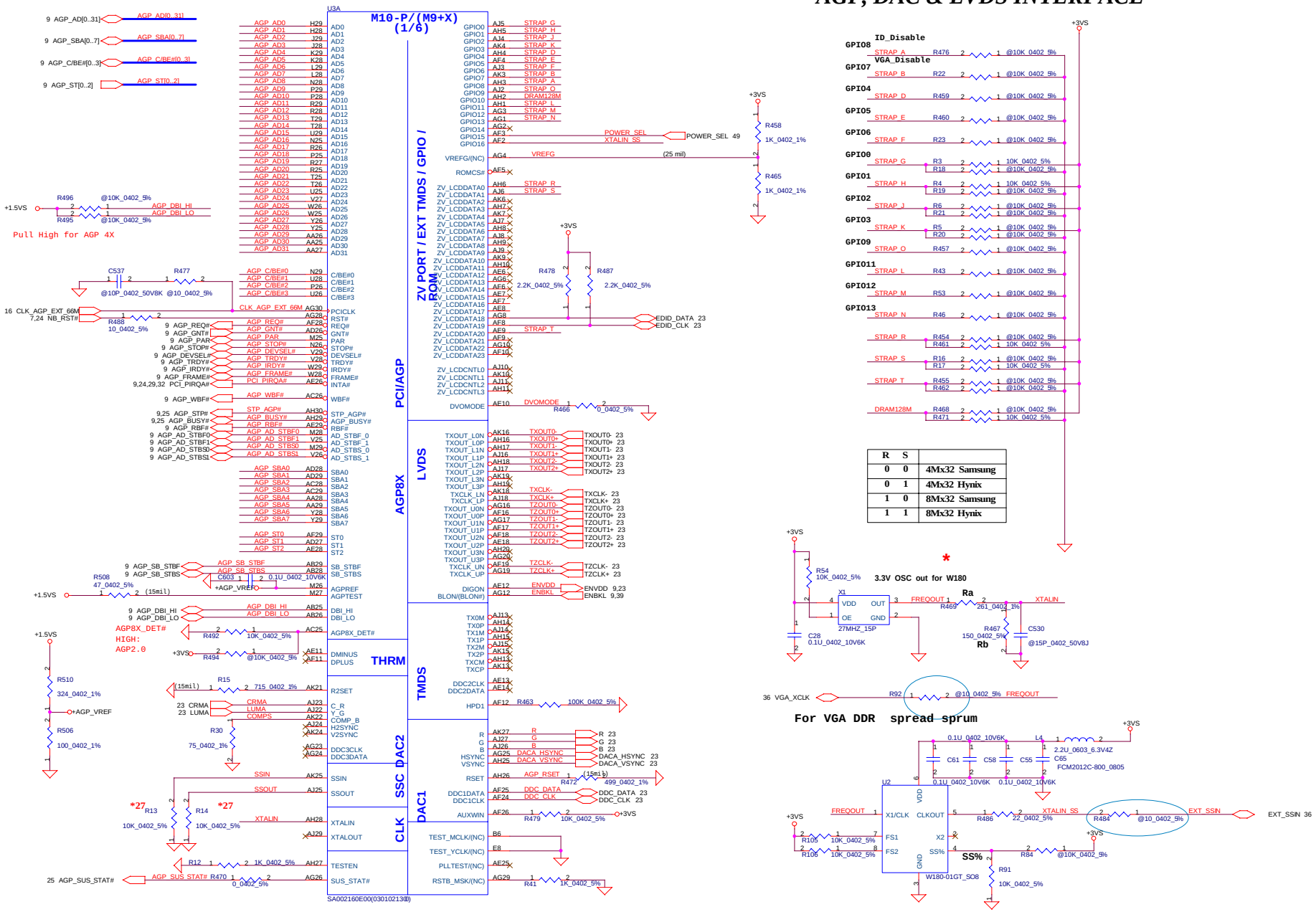
Compal Electronics, Inc.		
Title: Clock Generator		
Size	Document Number: LA-2101	Rev 0.1
Date: Saturday, November 22, 2003	Sheet 16 of 52	

AGP, DAC & LVDS INTERFACE



R	S	
0	0	4Mx32 Samsung
0	1	4Mx32 Hynix
1	0	8Mx32 Samsung
1	1	8Mx32 Hynix

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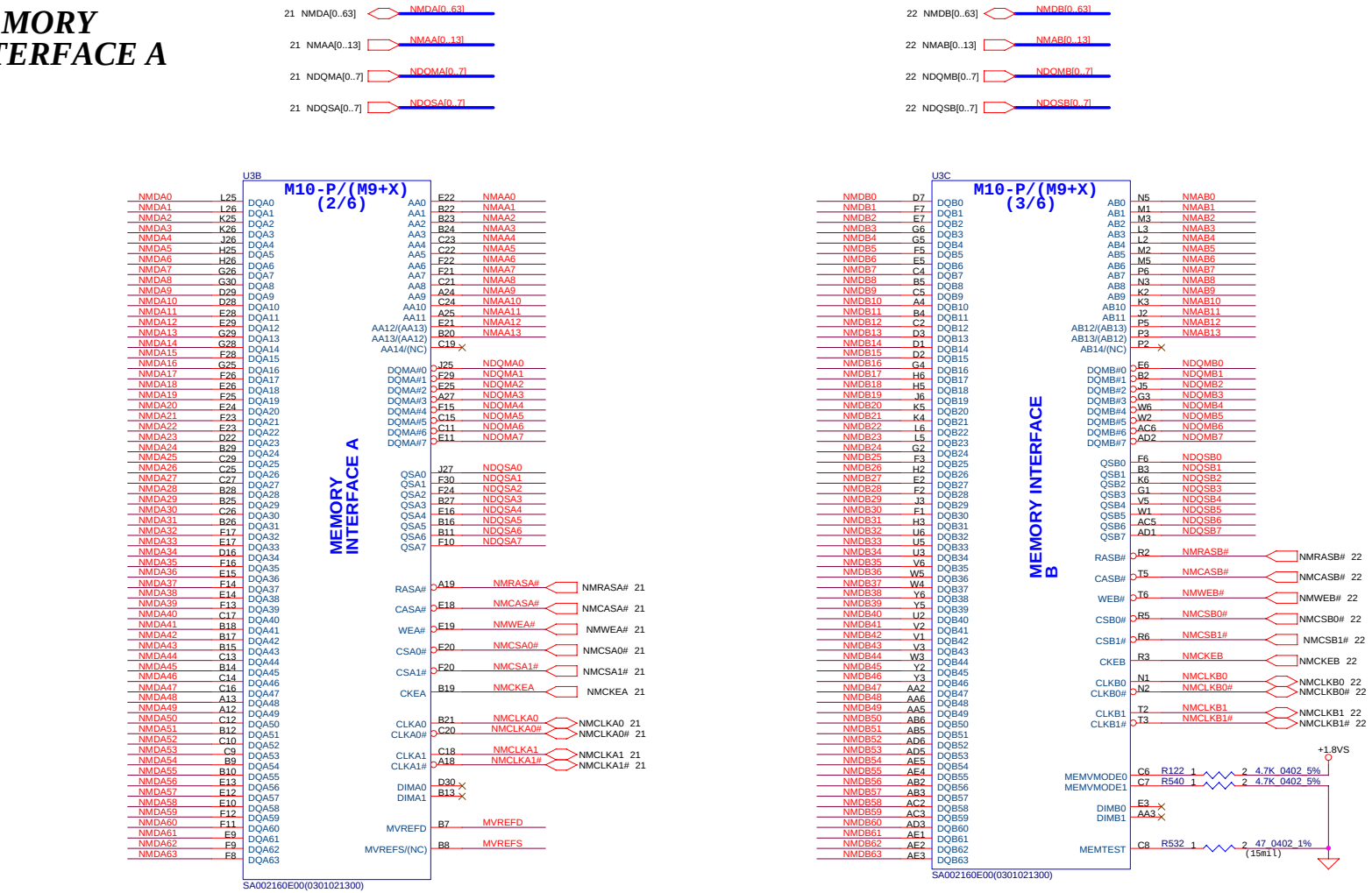
Compal Electronics, Inc.			
Title: ATI M10-P & M9+X (AGP BUS)			
Size	Document Number: LA-2101		Rev 0.1
Date: Saturday, November 22, 2003	Sheet 17 of 52		

MEMORY INTERFACE A



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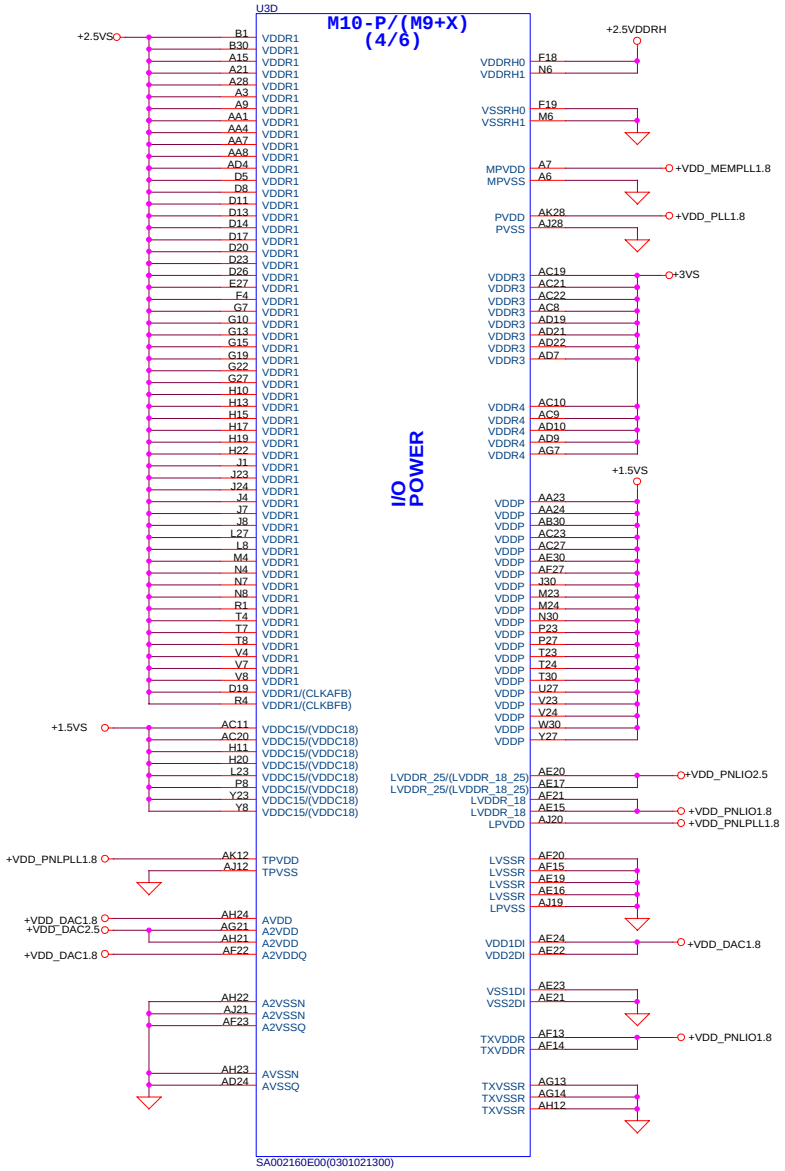
Compal Electronics, Inc.			
Title: ATI M10-P/M9+X DDR-A			
Size	Document Number: LA-2101		Rev 0.1
Date: Saturday, November 22, 2003	Sheet 18 of 52		

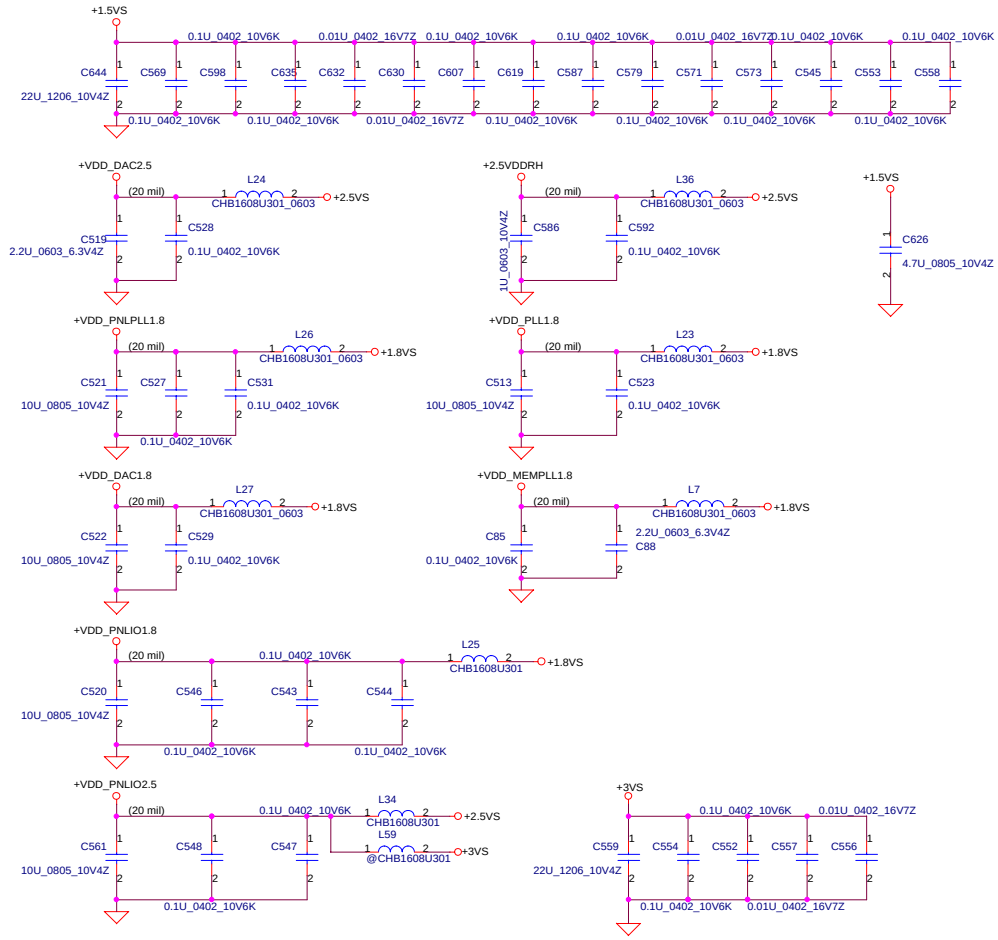
POWER INTERFACE



POWER Sequence

3.3VS --> 2.5VS --> 1.8VS --> +VGA_Core --> +1.5VS

The differ between +2.5VS and +1.8VS should not be greater than 1.2V



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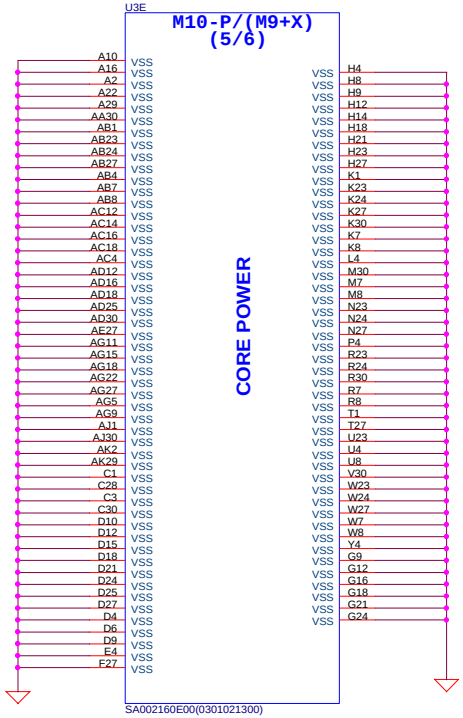
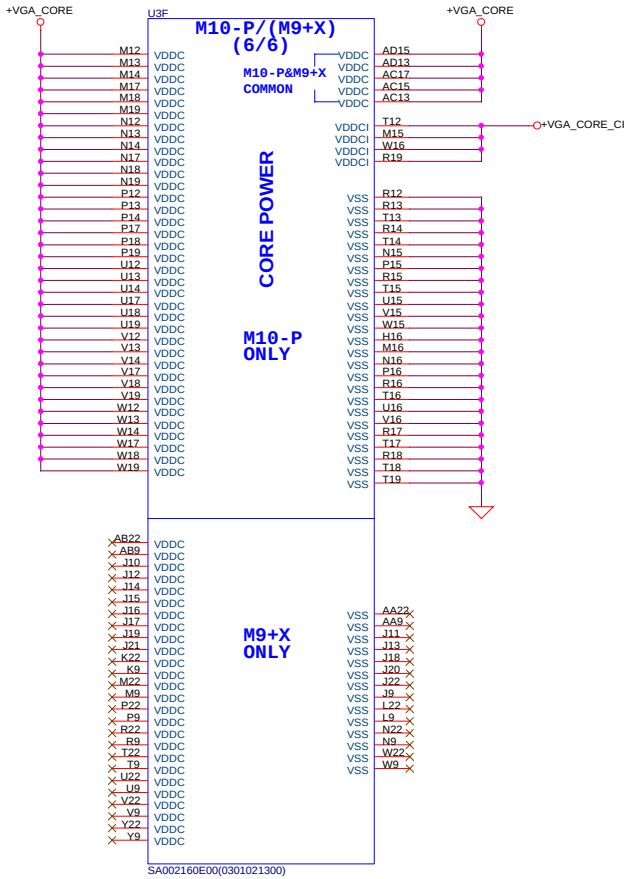
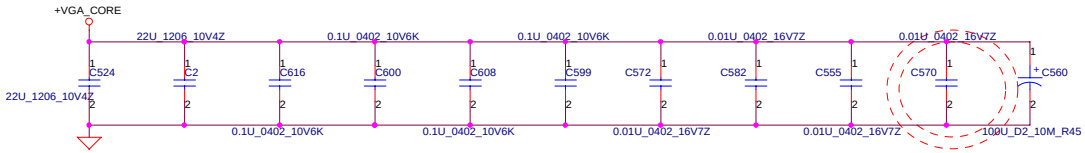
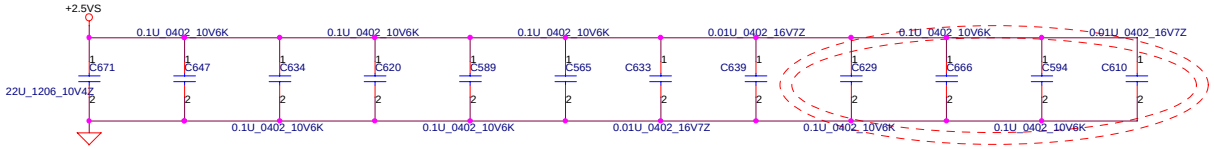
Compal Electronics, Inc.			
Title: ATI M10-P/M9+X POWER-A			
Size	Document Number: LA-2101		Rev 0.1
Date: Tuesday, November 18, 2003	Sheet 19 of 52		

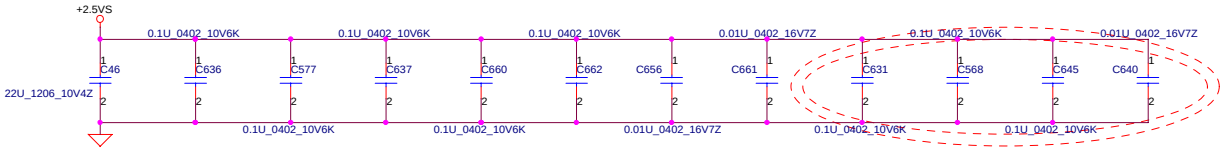
POWER INTERFACE



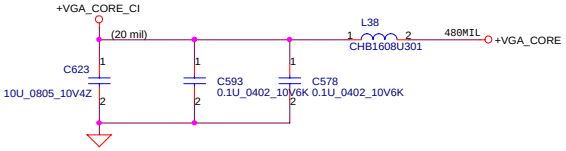








As close as ppossible to related pin



As close as ppossible to related pin

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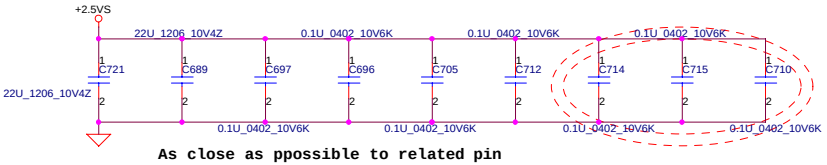
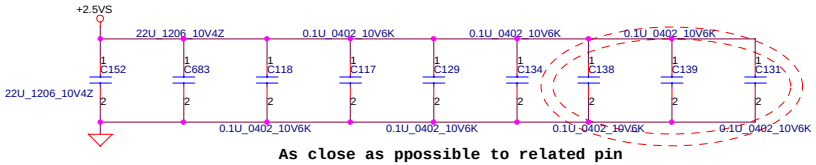
Compal Electronics, Inc.			
Title: ATI M10-P/M9+X POWER-B			
Size	Document Number: LA-2101		Rev 0.1
Date: Tuesday, November 18, 2003	Sheet 20 of 52		

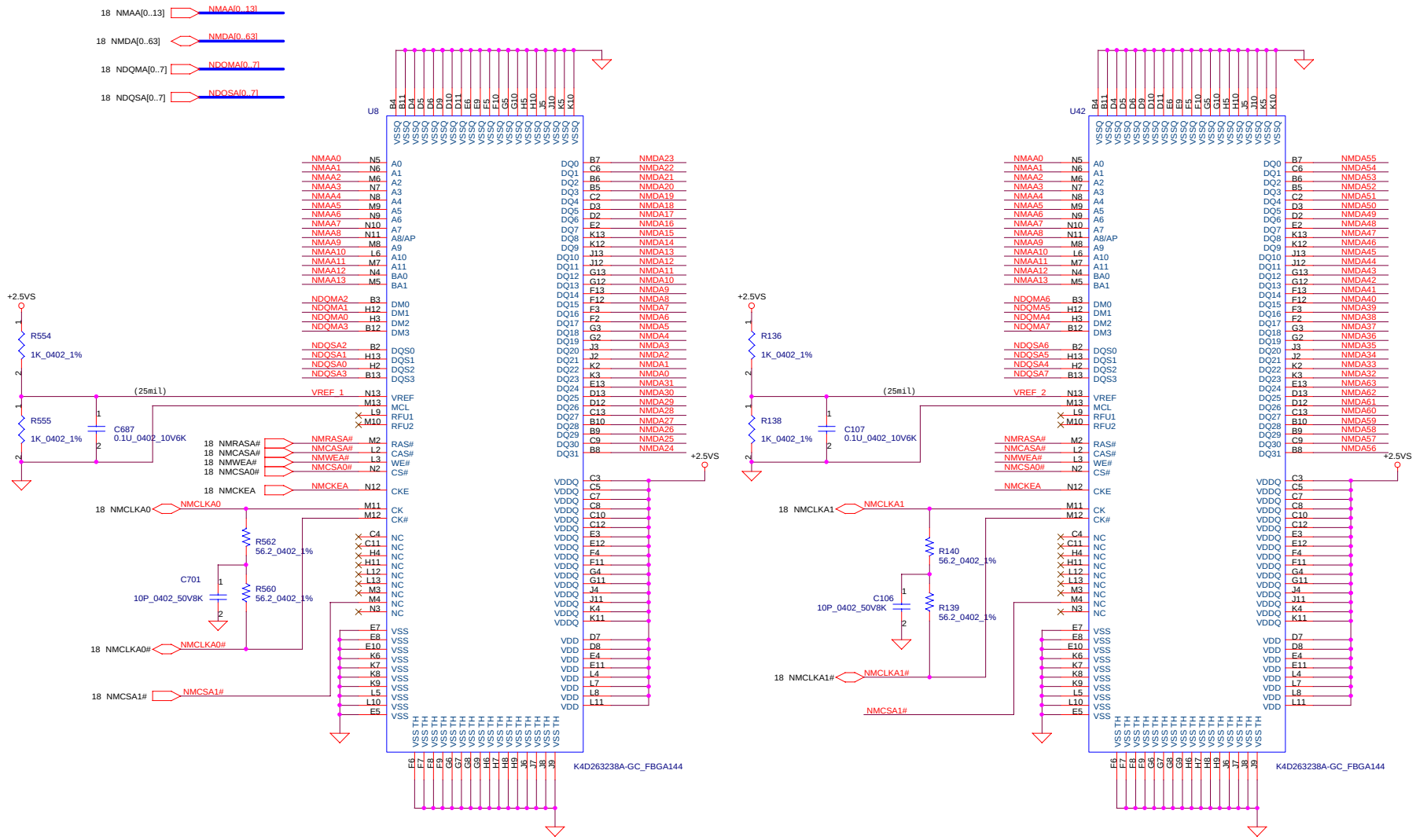
VGA DDR FOR CHANNEL A



As close as ppossible to related pin



As close as ppossible to related pin



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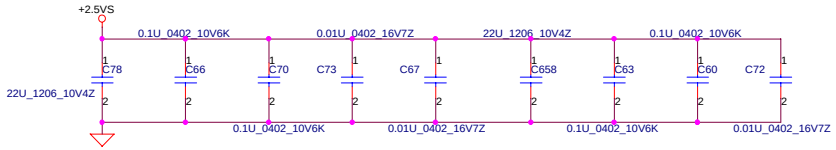
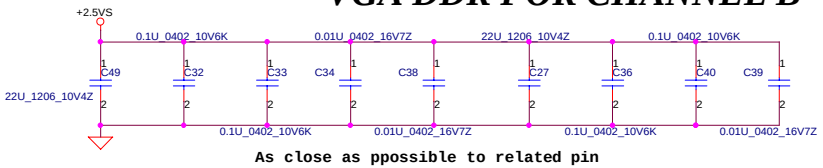
Compal Electronics, Inc.			
Title: VGA DDR FOR CHANNEL A			
Size	Document Number: LA-2101		Rev 0.1
Date: Saturday, November 22, 2003	Sheet 21 of 52		

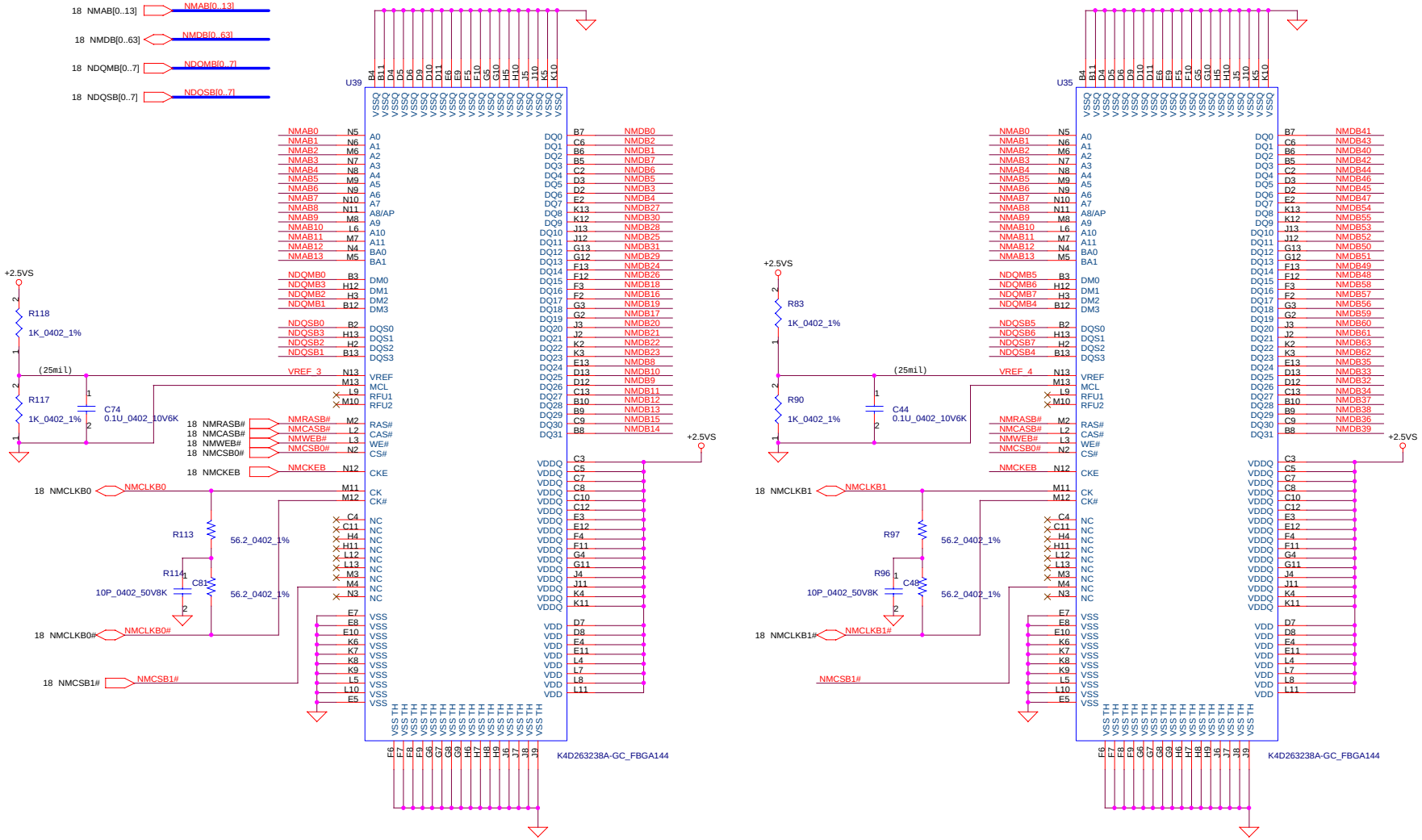
VGA DDR FOR CHANNEL B



As close as ppossible to related pin



As close as ppossible to related pin



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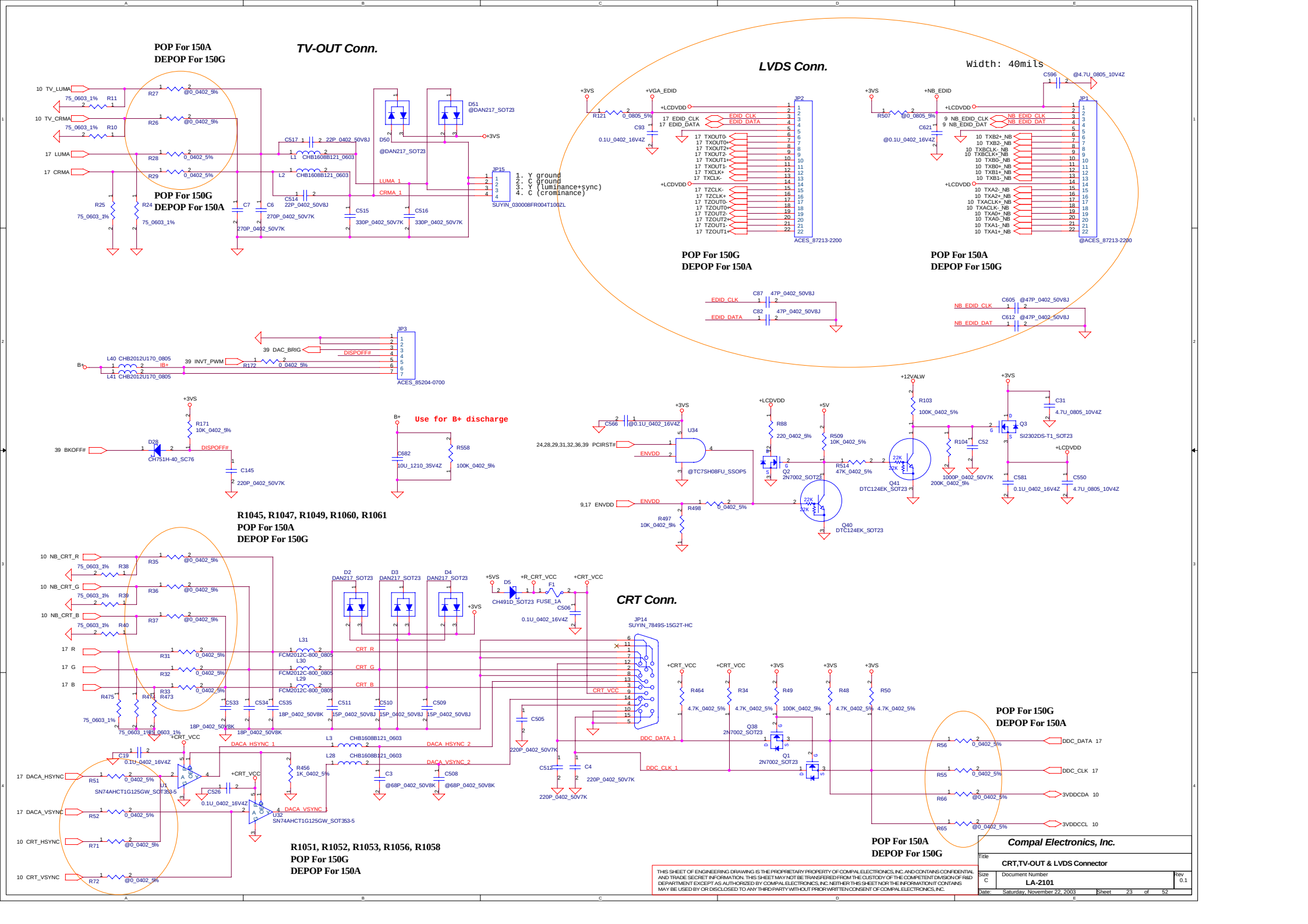
Compal Electronics, Inc.			
Title: VGA DDR FOR CHANNEL B			
Size	Document Number: LA-2101		Rev 0.1
Date: Saturday, November 22, 2003	Sheet 22 of 52		


TV-OUT Conn.
POP For 150A
DEPOP For 150G
POP For 150G
DEPOP For 150A
10 TV_LUMA
10 TV_CRMA
17 LUMA
17 CRMA
R27 @0_0402_5%
R26 @0_0402_5%
R28 0_0402_5%
R29 0_0402_5%
R11 75_0603_1%
R10 75_0603_1%
R25 75_0603_1%
R24 75_0603_1%
C7 270P_0402_50V7K
C6 270P_0402_50V7K
C517 22P_0402_50V8J
L1 CHB1608B121_0603
L2 CHB1608B121_0603
C514 22P_0402_50V8J
C515 330P_0402_50V7K
C516 330P_0402_50V7K
D50 @DAN217_SOT23
D51 @DAN217_SOT23
+3VS
LUMA_1
CRMA_1
JP15
SUYIN_030008FR004T100ZL
1. Y ground
2. C ground
3. Y (luminance+sync)
4. C (crominance)
LVDS Conn.
Width: 40mils
+3VS
+VGA_EDID
R121 0_0805_5%
C93 0.1U_0402_16V4Z
+LCDVDD
17 EDID_CLK
17 EDID_DATA
EDID_CLK
EDID_DATA
17 TXOUT0-
17 TXOUT0+
17 TXOUT2+
17 TXOUT2-
17 TXOUT1+
17 TXOUT1-
17 TXCLK+
17 TXCLK-
17 TZCLK-
17 TZCLK+
17 TZOUT0-
17 TZOUT0+
17 TZOUT2-
17 TZOUT2+
17 TZOUT1-
17 TZOUT1+
JP2
ACES_87213-2200
POP For 150G
DEPOP For 150A
+3VS
+NB_EDID
R507 @0_0805_5%
C621 @0.1U_0402_16V4Z
C596 @4.7U_0805_10V4Z
9 NB_EDID_CLK
9 NB_EDID_DAT
NB_EDID_CLK
NB_EDID_DAT
10 TXB2+_NB
10 TXB2-_NB
10 TXBCLK-_NB
10 TXBCLK+_NB
10 TXB0-_NB
10 TXB0+_NB
10 TXB1+_NB
10 TXB1-_NB
10 TXA2-_NB
10 TXA2+_NB
10 TXACLK+_NB
10 TXACLK-_NB
10 TXA0+_NB
10 TXA0-_NB
10 TXA1-_NB
10 TXA1+_NB
JP1
@ACES_87213-2200
POP For 150A
DEPOP For 150G
C87 47P_0402_50V8J
C82 47P_0402_50V8J
C605 @47P_0402_50V8J
C612 @47P_0402_50V8J
JP3
ACES_85204-0700
39 DAC_BRIG
DISPOFF#
39 INVT_PWM
R172 0_0402_5%
B+
L40 CHB2012U170_0805
L41 CHB2012U170_0805
IB+
+3VS
R171 10K_0402_5%
39 BKOFF#
D28 CR751H-40_SC76
DISPOFF#
C145 220P_0402_50V7K
B+
Use for B+ discharge
C682 10U_1210_35V4Z
R558 100K_0402_5%
R1045, R1047, R1049, R1060, R1061
POP For 150A
DEPOP For 150G
+3VS
C566 @0.1U_0402_16V4Z
U34 @TC7SH08FU_SSOP5
24,28,29,31,32,36,39 PCIRST#
ENVDD
9,17 ENVDD
R498 0_0402_5%
R497 10K_0402_5%
+LCDVDD
R88 220_0402_5%
Q2 2N7002_SOT23
+5V
R509 10K_0402_5%
R514 47K_0402_5%
Q40 DTC124EK_SOT23
+12VALW
R103 100K_0402_5%
Q41 DTC124EK_SOT23
R104 200K_0402_5%
C52 1000P_0402_50V7K
+3VS
C31 4.7U_0805_10V4Z
Q3 SI2302DS-T1_SOT23
+LCDVDD
C581 0.1U_0402_16V4Z
C550 4.7U_0805_10V4Z
CRT Conn.
10 NB_CRT_R
10 NB_CRT_G
10 NB_CRT_B
R35 @0_0402_5%
R36 @0_0402_5%
R37 @0_0402_5%
R38 75_0603_1%
R39 75_0603_1%
R40 75_0603_1%
17 R
17 G
17 B
R31 0_0402_5%
R32 0_0402_5%
R33 0_0402_5%
R475 75_0603_1%
R473 75_0603_1%
D2 DAN217_SOT23
D3 DAN217_SOT23
D4 DAN217_SOT23
+3VS
L31 FCM2012C-800_0805
L30 FCM2012C-800_0805
L29 FCM2012C-800_0805
CRT_R
CRT_G
CRT_B
CRT_VCC
C533 18P_0402_50V8K
C534 18P_0402_50V8K
C535 18P_0402_50V8K
C511 15P_0402_50V8J
C510 15P_0402_50V8J
C509 15P_0402_50V8J
+5VS
D5 CH491D_SOT23
+R_CRT_VCC
F1 FUSE_1A
+CRT_VCC
C506 0.1U_0402_16V4Z
JP14
SUYIN_7849S-15G2T-HC
C505 220P_0402_50V7K
C512 220P_0402_50V7K
C4 220P_0402_50V7K
+CRT_VCC
R464 4.7K_0402_5%
R34 4.7K_0402_5%
+3VS
R49 100K_0402_5%
R48 4.7K_0402_5%
R50 4.7K_0402_5%
Q38 2N7002_SOT23
Q1 2N7002_SOT23
DDC_DATA_1
DDC_CLK_1
POP For 150G
DEPOP For 150A
R56 0_0402_5%
R55 0_0402_5%
R66 @0_0402_5%
R65 @0_0402_5%
DDC_DATA 17
DDC_CLK 17
3VDDCDA 10
3VDDCCL 10
POP For 150A
DEPOP For 150G
+CRT_VCC
C19 0.1U_0402_16V4Z
17 DACA_HSYNC
17 DACA_VSYNC
10 CRT_HSYNC
10 CRT_VSYNC
R51 0_0402_5%
R52 0_0402_5%
R71 @0_0402_5%
R72 @0_0402_5%
U1 SN74AHCT1G125GW_SOT353-5
C526 0.1U_0402_16V4Z
U32 SN74AHCT1G125GW_SOT353-5
DACA_HSYNC_1
DACA_VSYNC_1
R456 1K_0402_5%
L3 CHB1608B121_0603
L28 CHB1608B121_0603
DACA_HSYNC_2
DACA_VSYNC_2
C3 @68P_0402_50V8K
C508 @68P_0402_50V8K
R1051, R1052, R1053, R1056, R1058
POP For 150G
DEPOP For 150A
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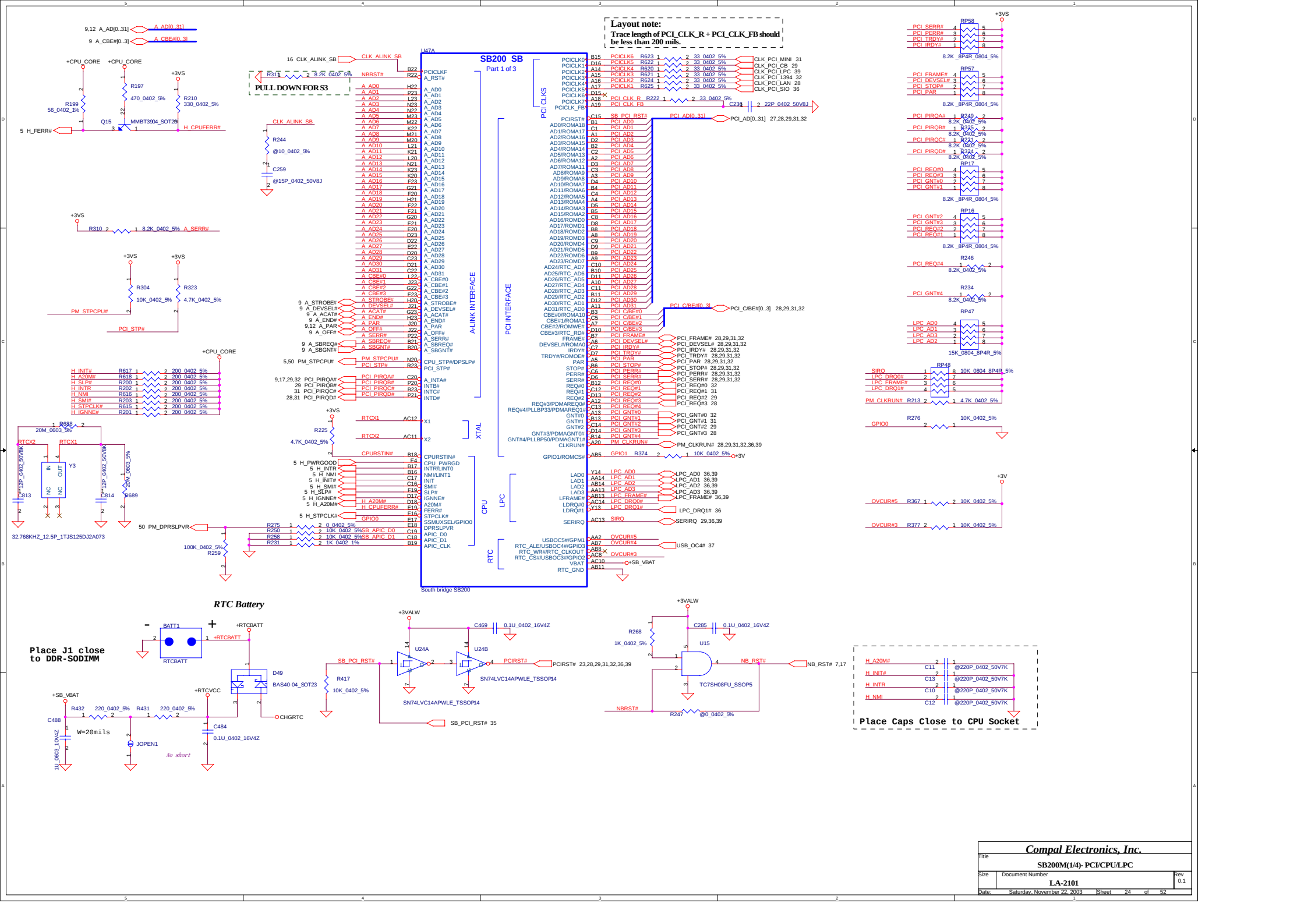
Compal Electronics, Inc.
Title
CRT,TV-OUT & LVDS Connector
Size C
Document Number
LA-2101
Rev 0.1
Date: Saturday, November 22, 2003
Sheet 23 of 52



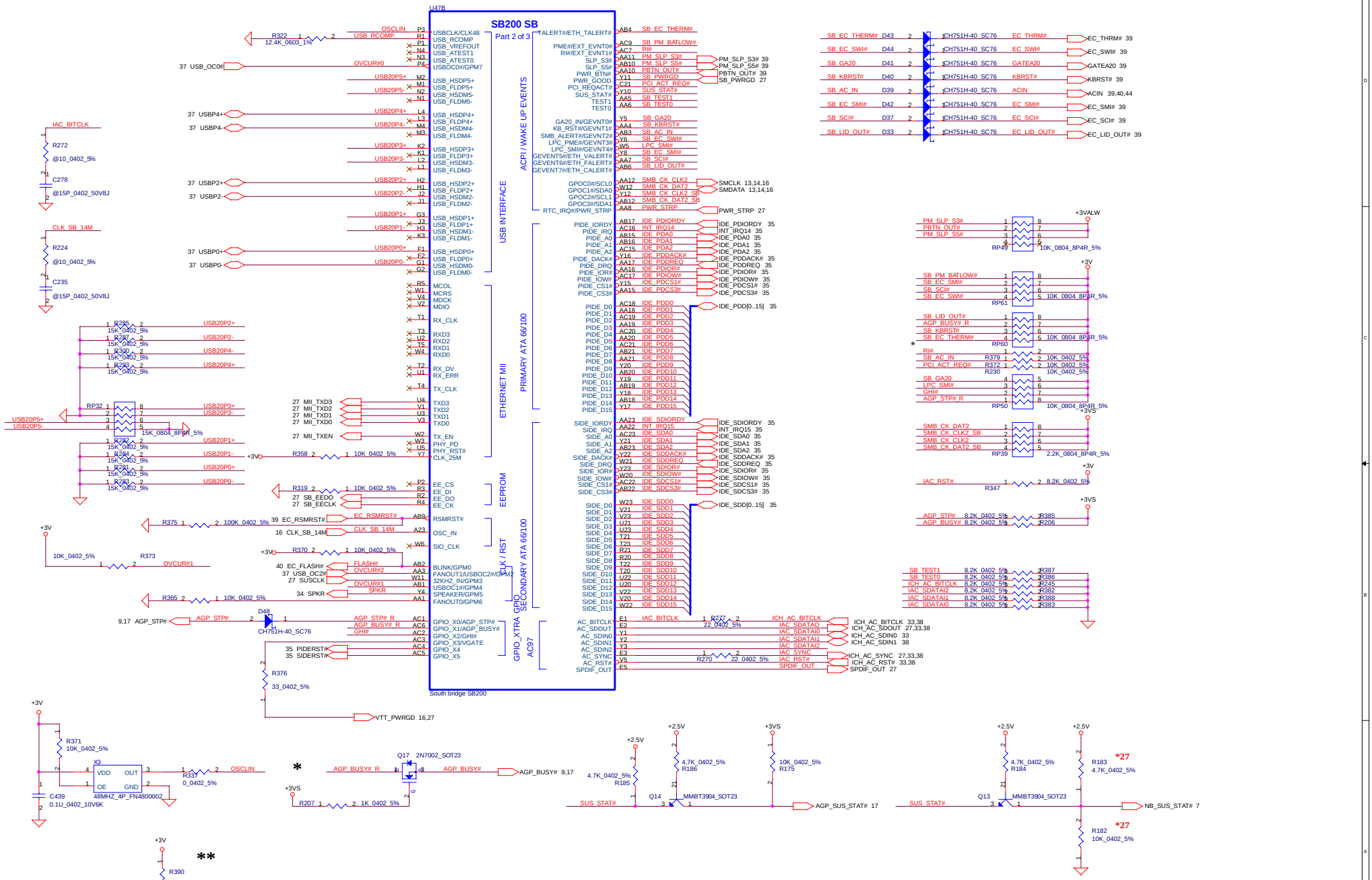
Title: SB200M(1/4)- PCI/CPU/LPC

Compal Electronics, Inc.

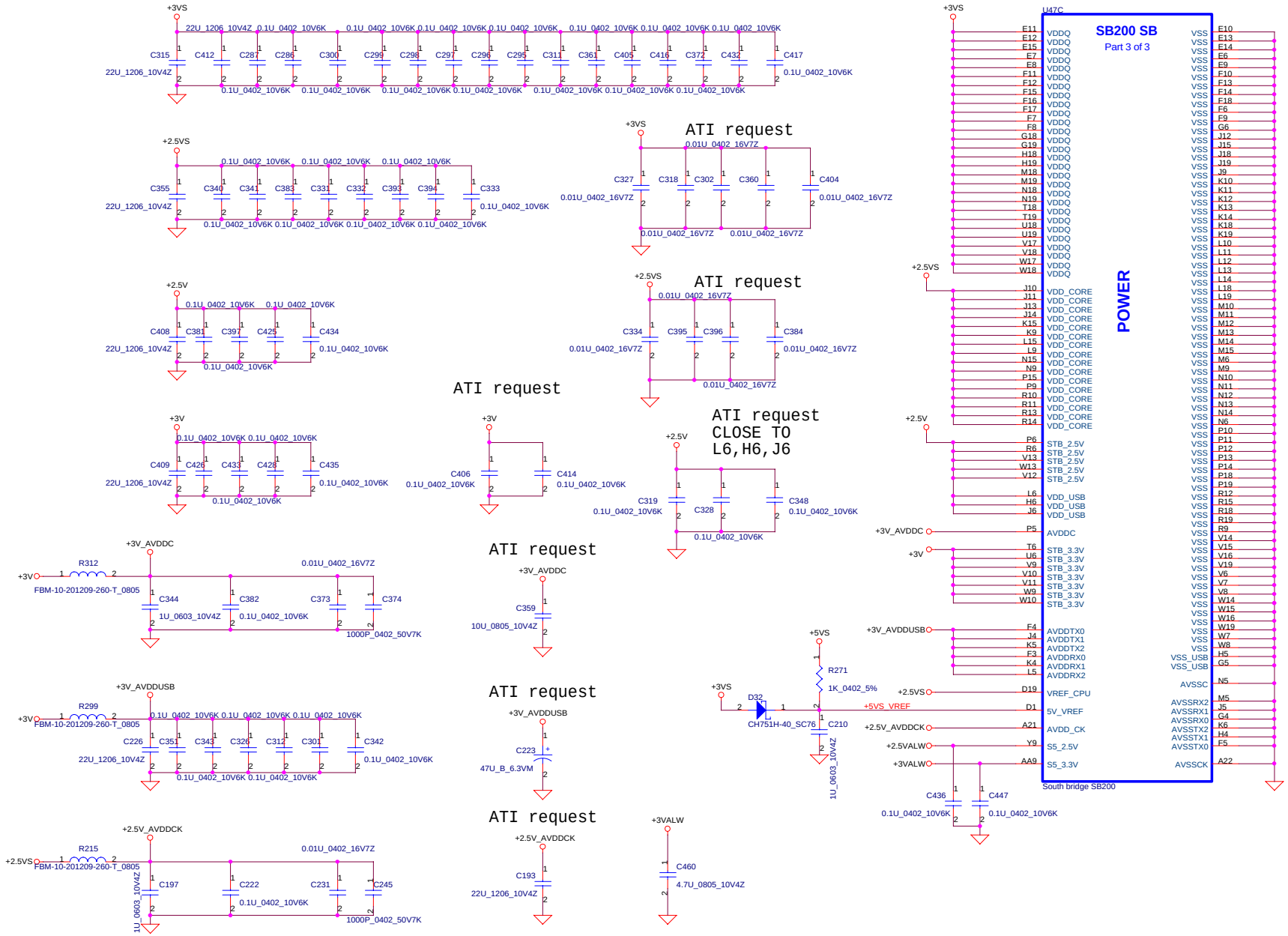
Document Number: LA-2101

Rev: 0.1

Date: Saturday, November 22, 2003 Sheet 24 of 52



Compal Electronics, Inc.	
Title	SB200M(2/4) - IDE/USB/MII
Size	Document Number: LA-2101 — Rev 0.1
Date: Saturday, November 22, 2003	Sheet 25 of 52



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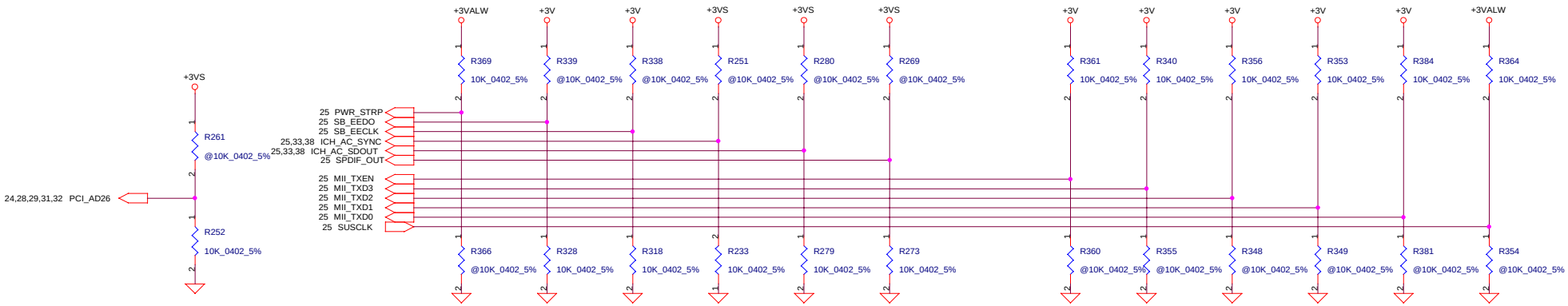
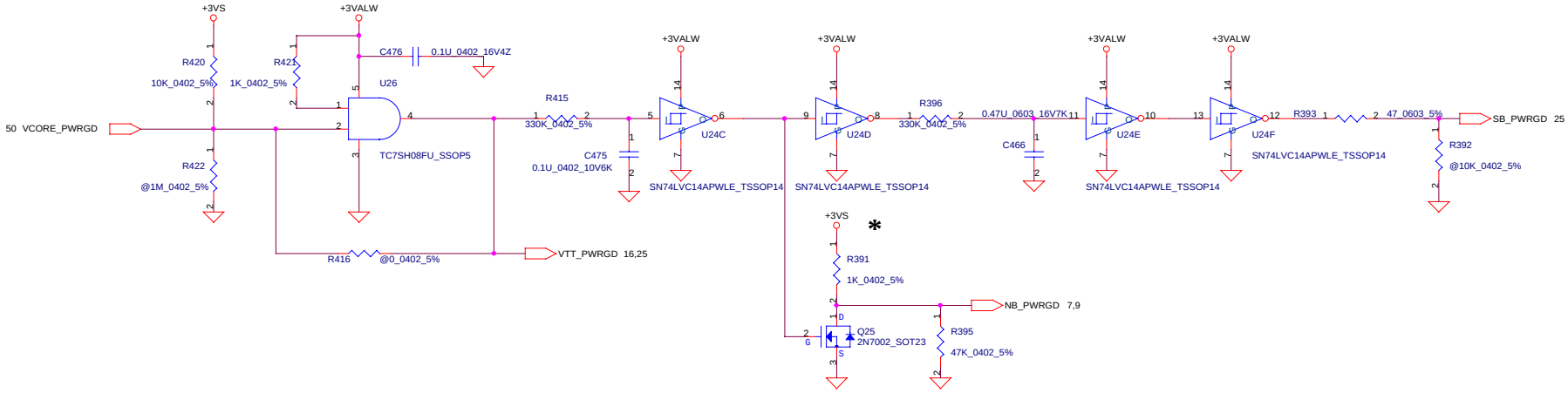
Compal Electronics, Inc.	
Title	SB200M(3/4) - PWR
Size	Document Number: LA-2101 — Rev: 0.1
Date: Tuesday, November 18, 2003	Sheet 26 of 52



REQUIRED SYSTEM STRAPS

	PWR_STRP	IGN DEBUG EEDO	EECK	AC_SYNC	AC_SDOUT	SPDIF_OUT	SPEEDSTEP CPU_STP#	FREQLTCH TX_EN	ETHERNET TXD[3:0]	32KHZ_S5
STRAP HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	ROM ON PCI BUS	INIT ACTIVE HIGH	33MHz NB BUS	SIO 24MHz	ENABLE SPEED STEP	DISABLE CPU FREQ SETTING DEFAULT	PROCESSOR FREQ MULTIPLIER	32KHZ OUTPUT FROM SB200 (INT RTC) DEFAULT
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	ROM ON LPC BUS DEFAULT	INIT ACTIVE LOW (PIII) DEFAULT	HI SPEED A-LINK DEFAULT	SIO 48MHz DEFAULT	DISABLE SPEED STEP DEFAULT	ENABLE CPU FREQSETTING		32KHZ INPUT TO SB200 (EXT RTC)



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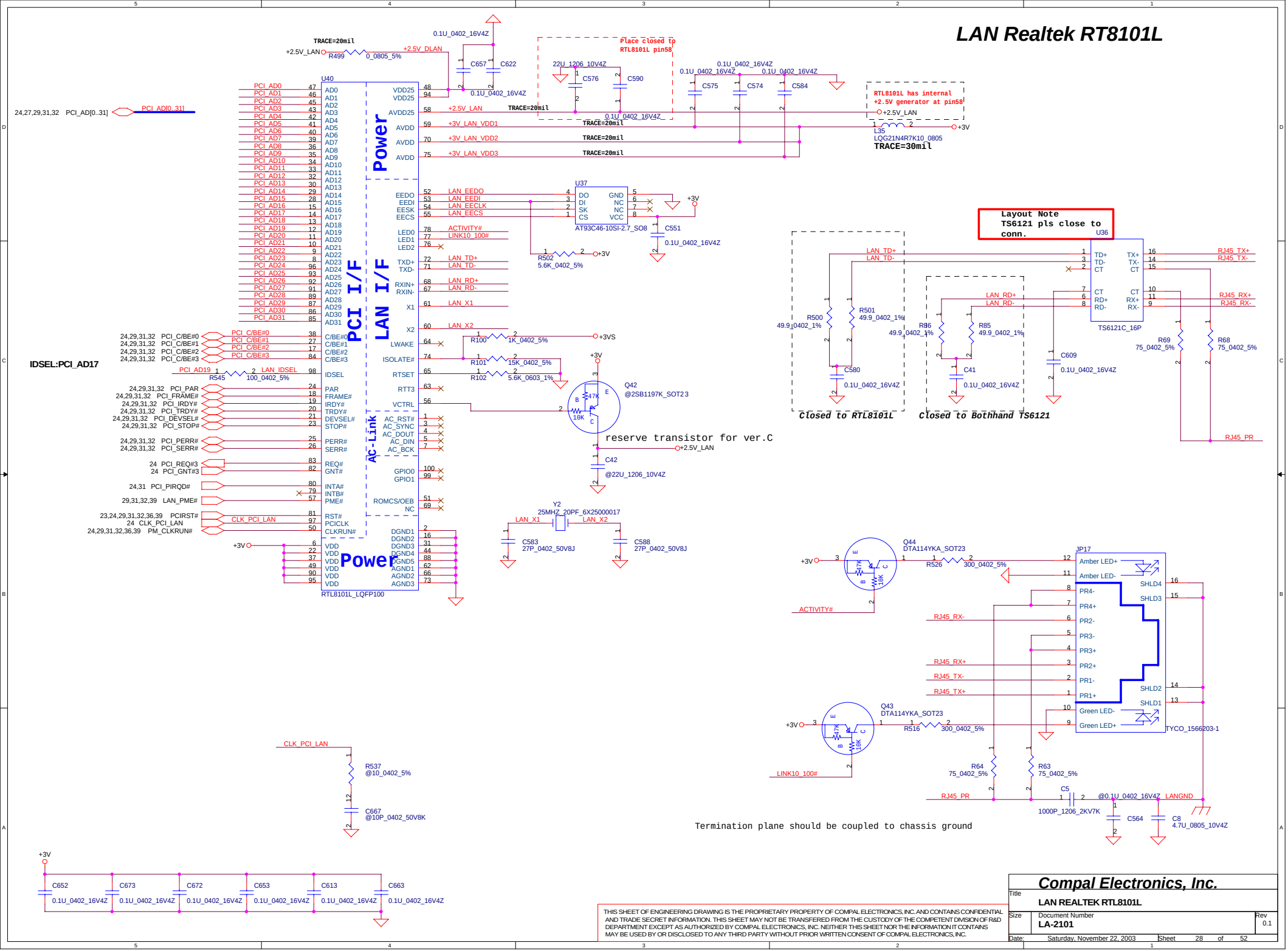
Compal Electronics, Inc.
Title: SB200M(4/4) - STRAPS
Size: Document Number: LA-2101 Rev: 0.1
Date: Saturday, November 22, 2003 Sheet 27 of 52

LAN Realtek RT8101L



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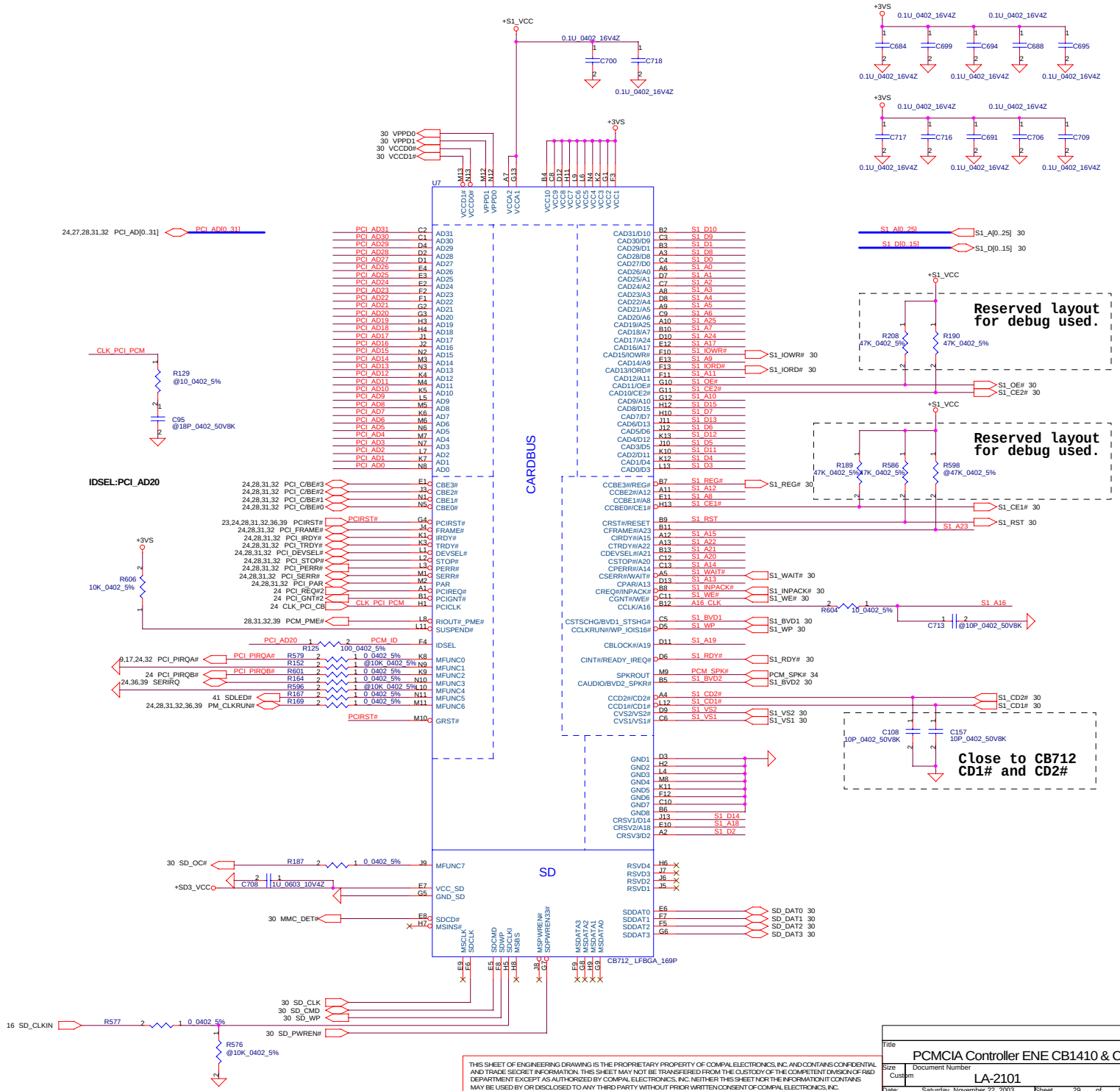
Compal Electronics, Inc.

Title	LAN REALTEK RTL8101L
Size	Document Number: LA-2101
Rev	0.1
Date:	Saturday, November 22, 2003
Sheet	28 of 52



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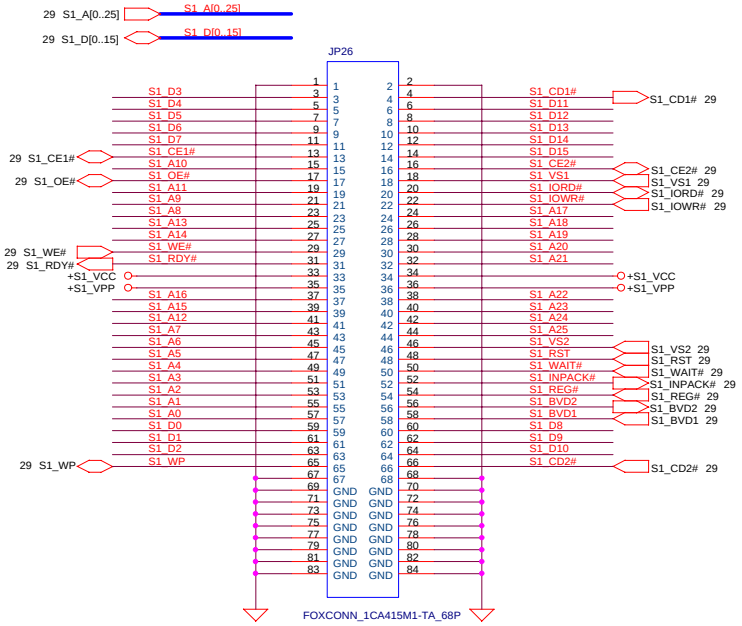
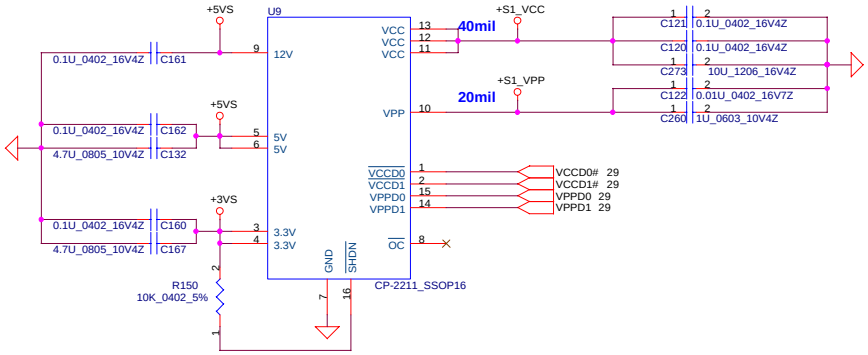
Title	PCMCIA Controller ENE CB1410 & CB712
Size	Custom
Document Number	LA-2101
Rev	0.1
Date:	Saturday, November 22, 2003
Sheet	29 of 52

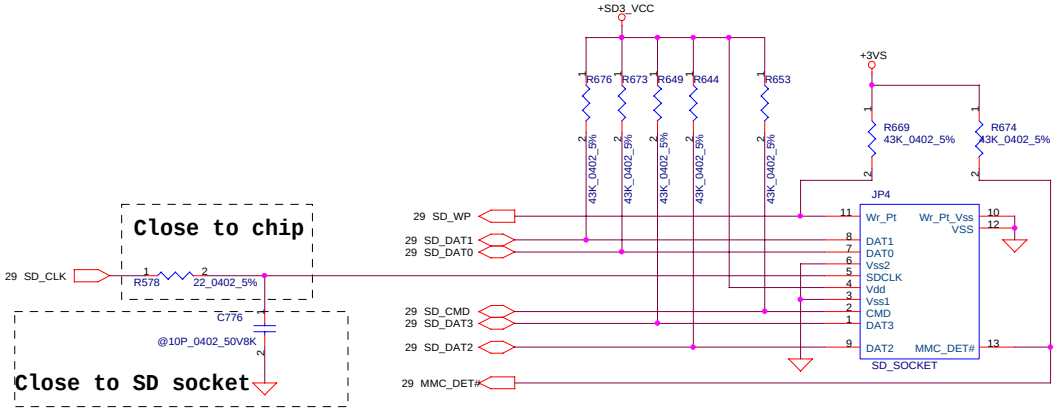
CARDBUS SOCKET

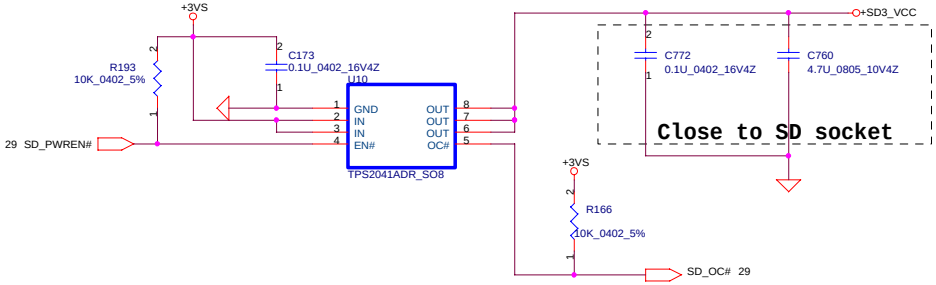


PCMCIA Power Controller



SD SOCKET





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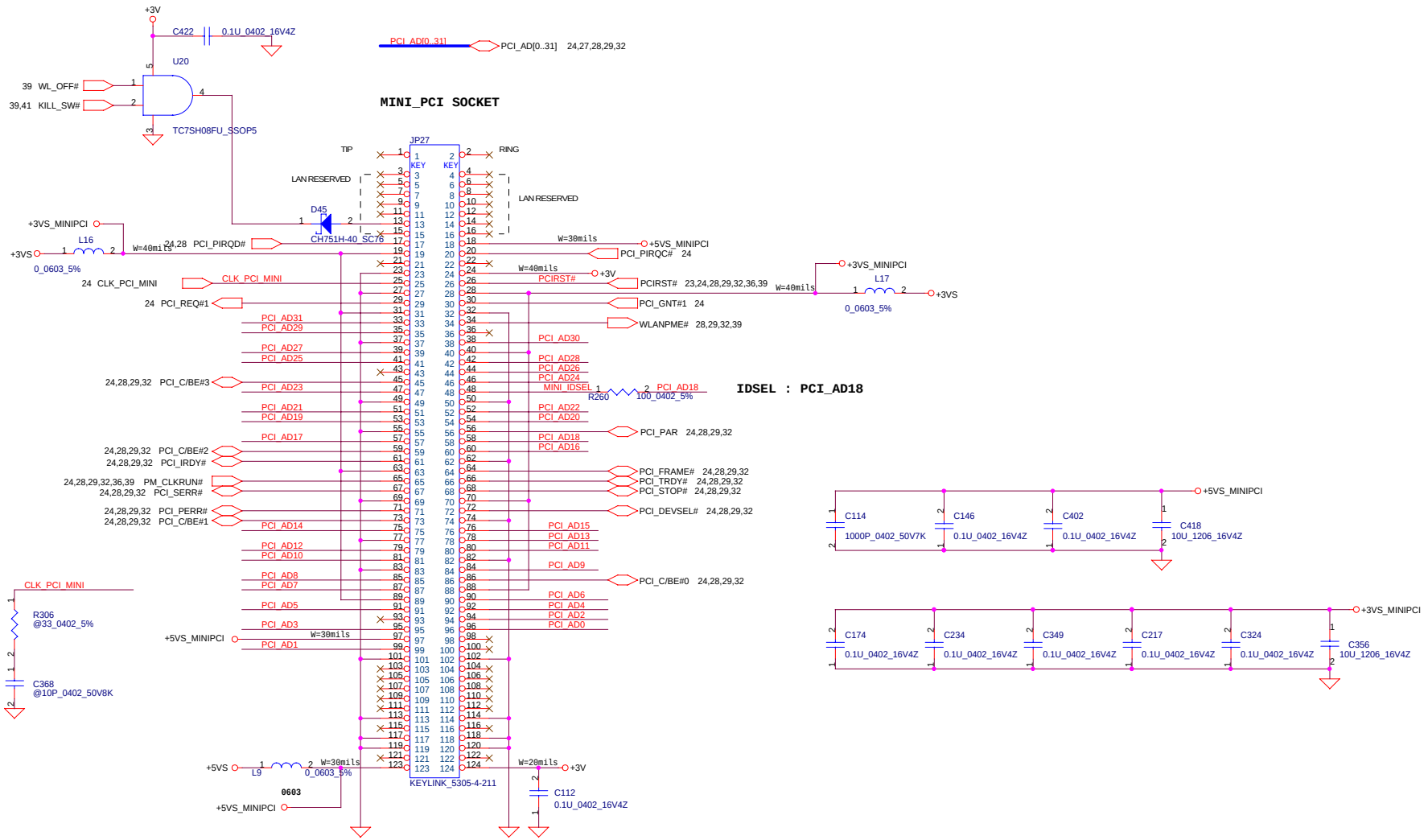
Compal Electronics, Inc.

Title	PCMCIA/SD SOCKET	
Size: Custom	Document Number: LA-2101	Rev: 0.1
Date: Saturday, November 22, 2003	Sheet 30 of 52	



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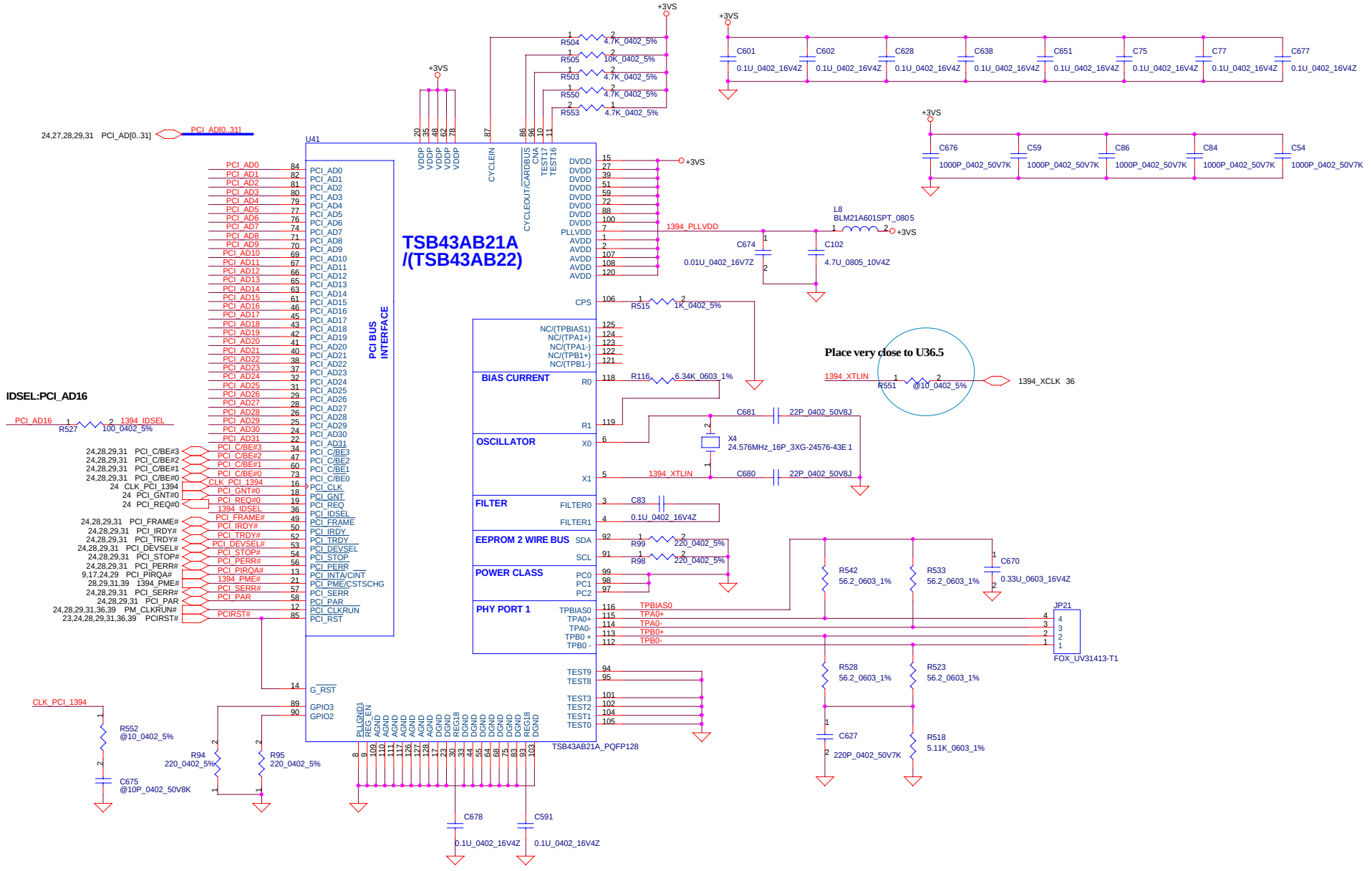
Compal Electronics, Inc.

Title	MINI_PCI	
Size: Custom	Document Number: LA-2101	Rev: 0.1
Date: Saturday, November 22, 2003	Sheet 31 of 52	



Compal Electronics, Inc.	
Title	1394 Interface
Size: Custom	Document Number: LA-2101
Rev	0.1
Date: Saturday, November 22, 2003	Sheet 32 of 52

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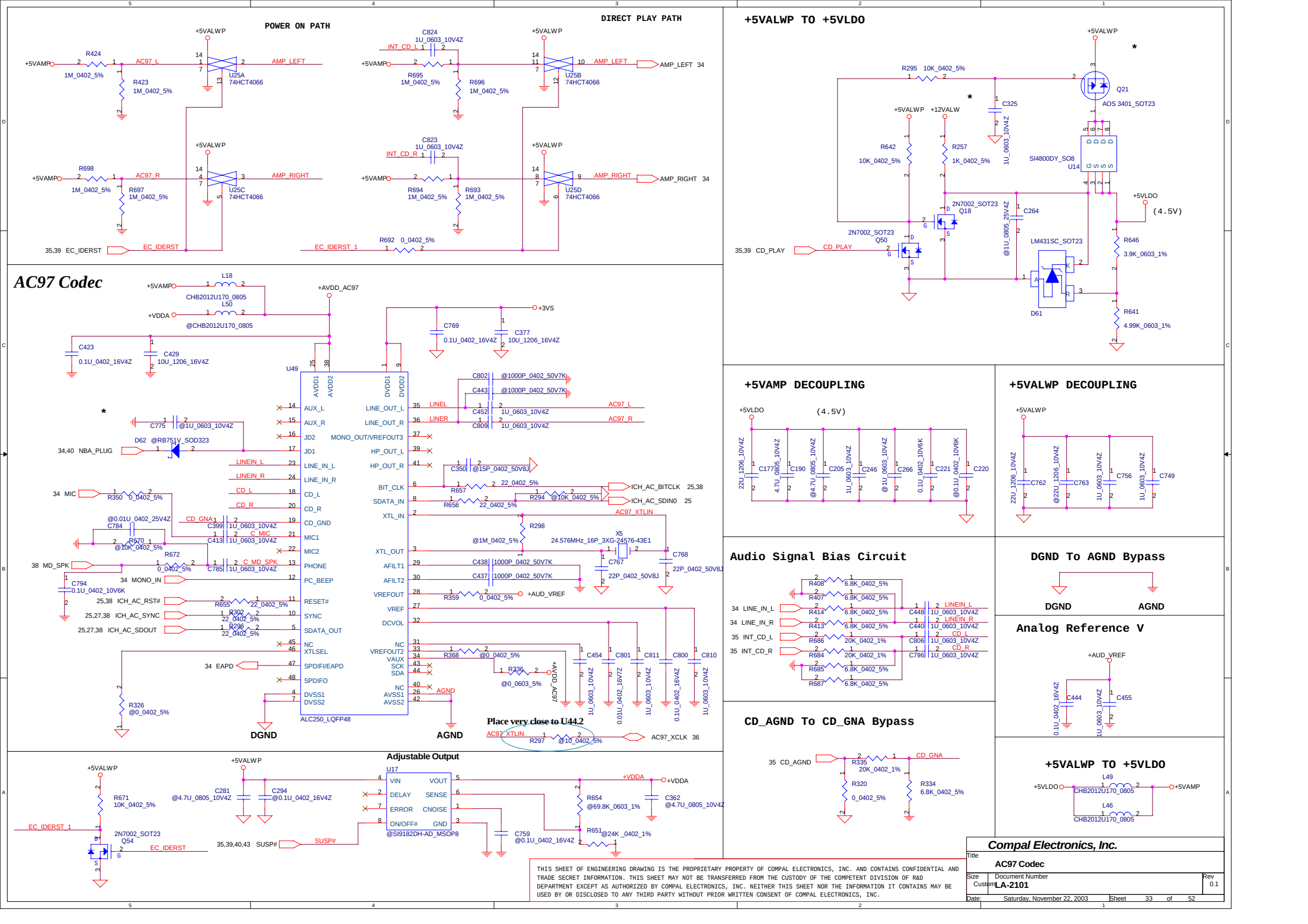
POWER ON PATH
DIRECT PLAY PATH
+5VALWP TO +5VLDO
AC97 Codec
+5VAMP DECOUPLING
+5VALWP DECOUPLING
Audio Signal Bias Circuit
DGND To AGND Bypass
Analog Reference V
CD_AGND To CD_GNA Bypass
+5VALWP TO +5VLDO
Adjustable Output
U25A 74HCT4066
U25B 74HCT4066
U25C 74HCT4066
U25D 74HCT4066
Q21 AOS 3401_SOT23
U14 SI4800DY_SO8
Q18 2N7002_SOT23
Q50 2N7002_SOT23
D61 LM431SC_SOT23
U49 ALC250_LQFP48
X5 24.576MHz_16P_3XG-24576-43E1
U17 @SI9182DH-AD_MSOP8
Q54 2N7002_SOT23
Place very close to U44.2
DGND
AGND
Compal Electronics, Inc.
Title AC97 Codec
Size Custom
Document Number LA-2101
Rev 0.1
Date: Saturday, November 22, 2003
Sheet 33 of 52
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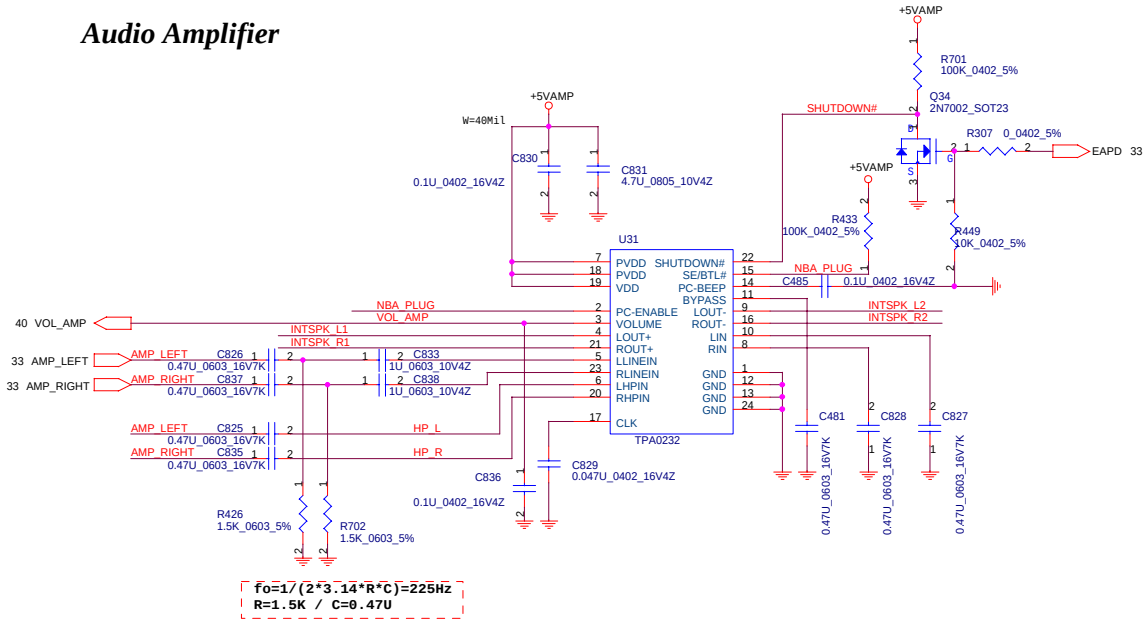
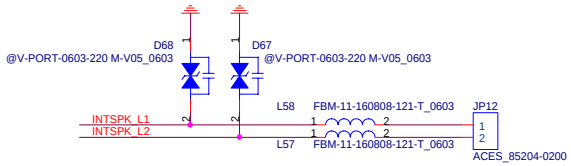
Audio Amplifier

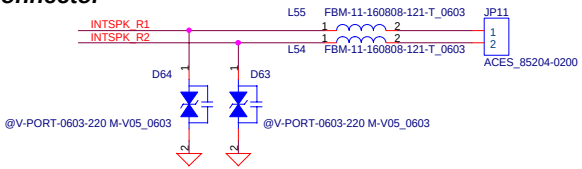


fo=1/(2*3.14*R*C)=225Hz
R=1.5K / C=0.47U

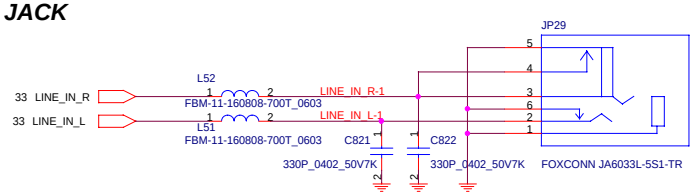
Left Speaker Connector



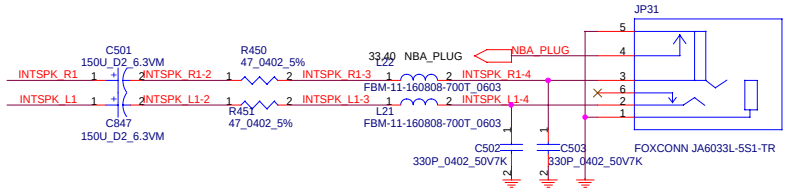
Right Speaker Connector



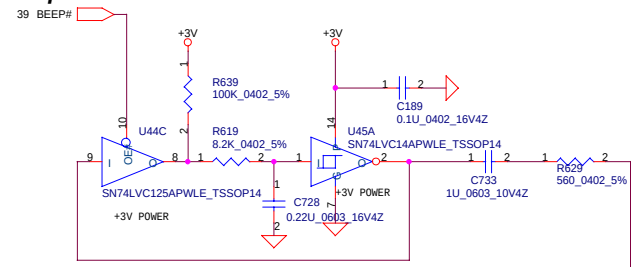
LINE IN JACK



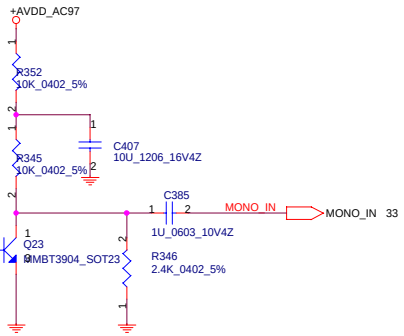
HEADPHONE OUT JACK



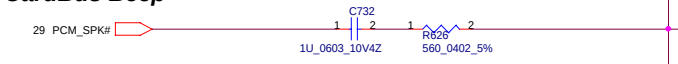
EC Beep



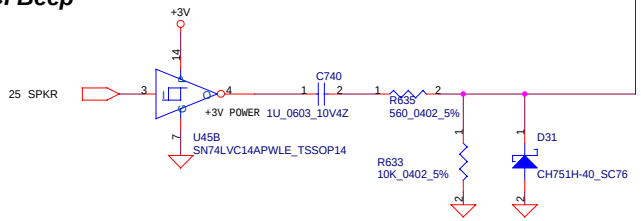
System Beep To AC97' Codec



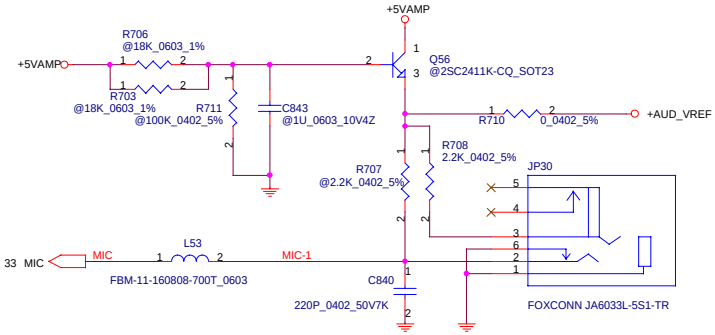
CardBus Beep



PCI Beep



MICROPHONE IN JACK



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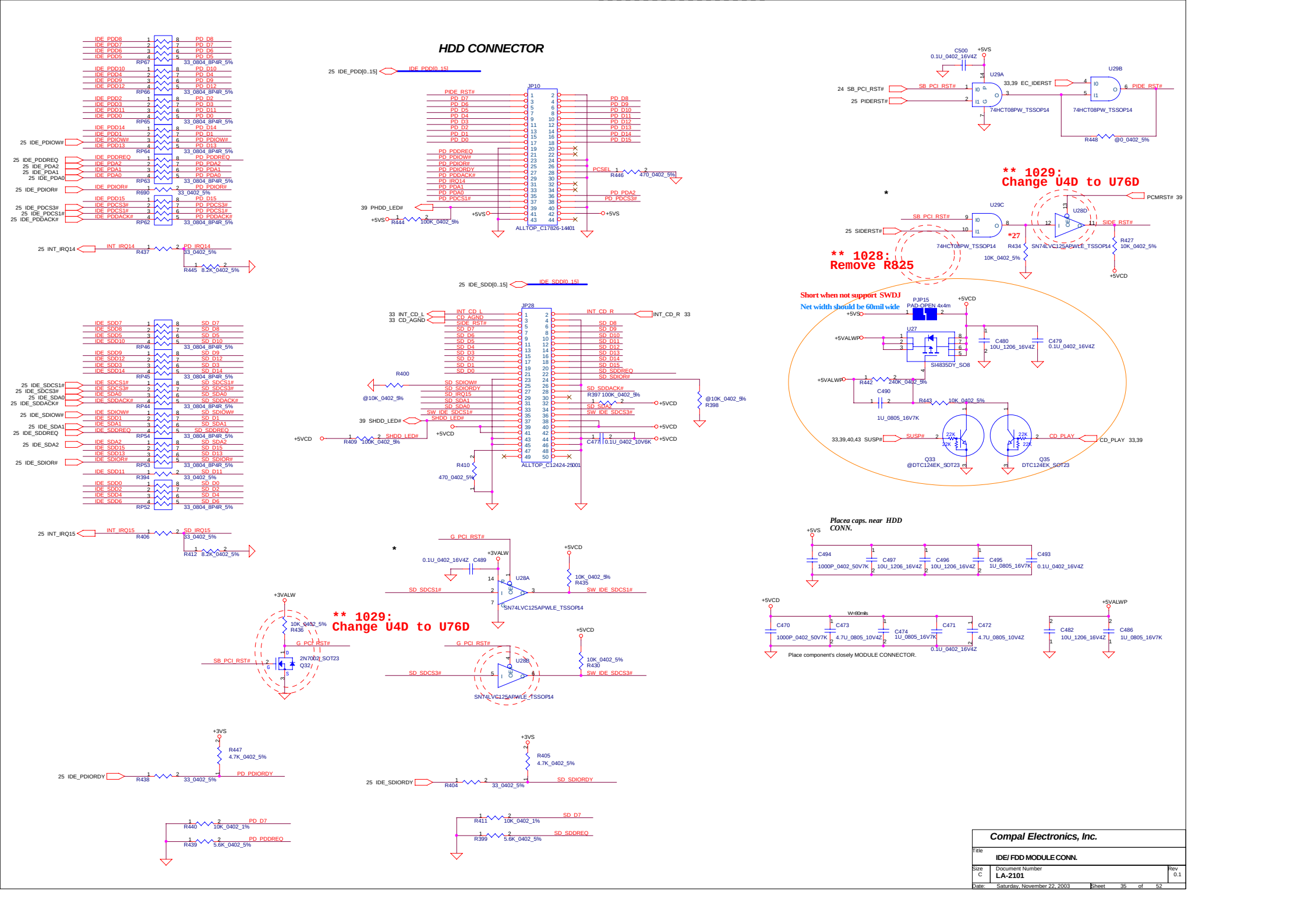
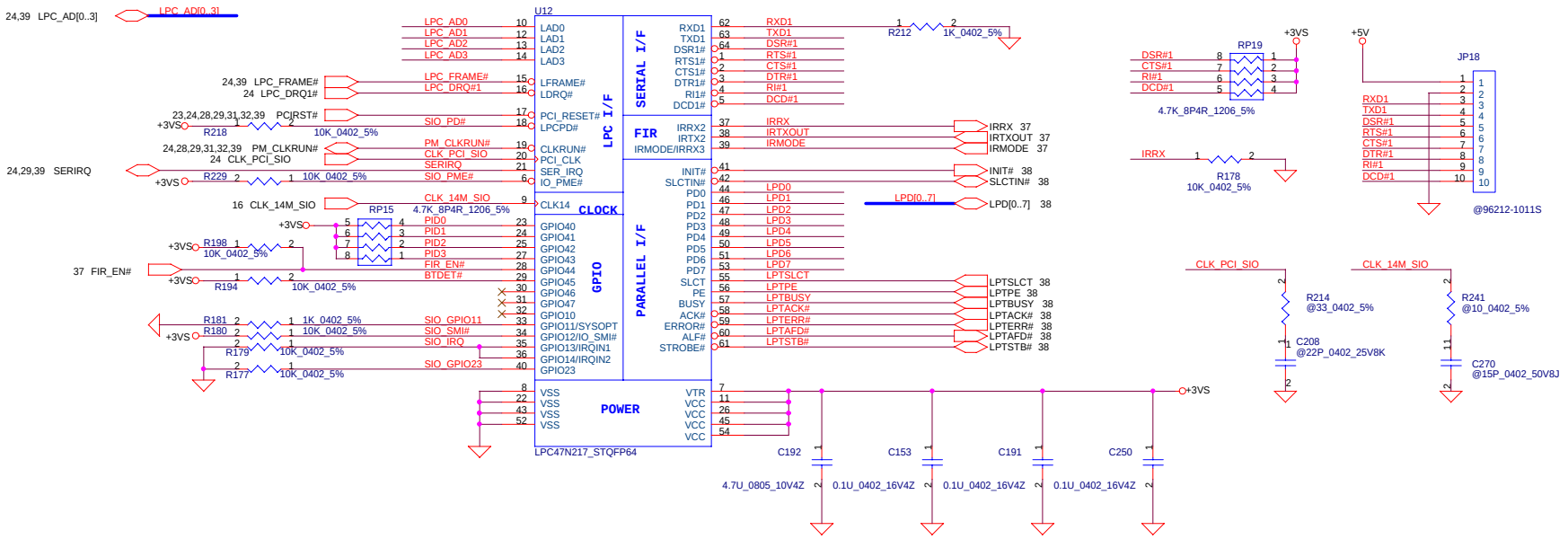
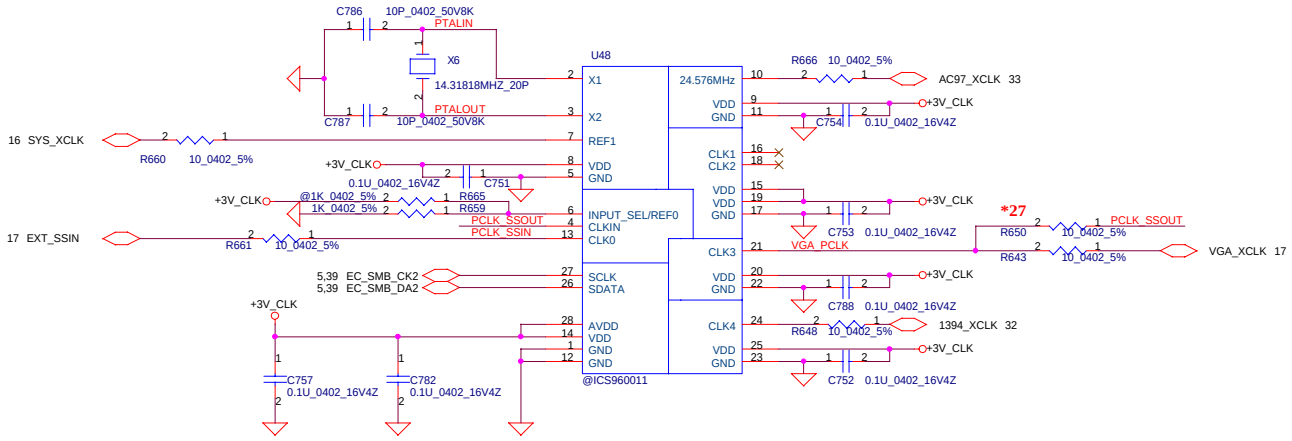
Compal Electronics, Inc.		
Title: AMP & Audio Jack		
Size: Custom	Document Number: LA-2101	Rev: 0.1
Date: Saturday, November 22, 2003	Sheet 34 of 52	


HDD CONNECTOR
JP10
ALLTOP_C17826-14401
JP28
ALLTOP_C12424-25001
** 1029: Change U4D to U76D
** 1028: Remove R825
Short when not support SWDJ
Net width should be 60mil wide
PJP15
PAD-OPEN 4x4m
U27
SI4835DY_SO8
U28A
U28B
SN74LVC125APWLE_TSSOP14
2N7002_SOT23
Q32
U29A
U29B
74HCT08PW_TSSOP14
U29C
U28D
Q33
@DTC124EK_SOT23
Q35
DTC124EK_SOT23
Placea caps. near HDD CONN.
Place component's closely MODULE CONNECTOR.
Compal Electronics, Inc.
IDE/ FDD MODULE CONN.
Size C
Document Number LA-2101
Rev 0.1
Date: Saturday, November 22, 2003
Sheet 35 of 52

SUPER I/O SMsC FDC47N217

*





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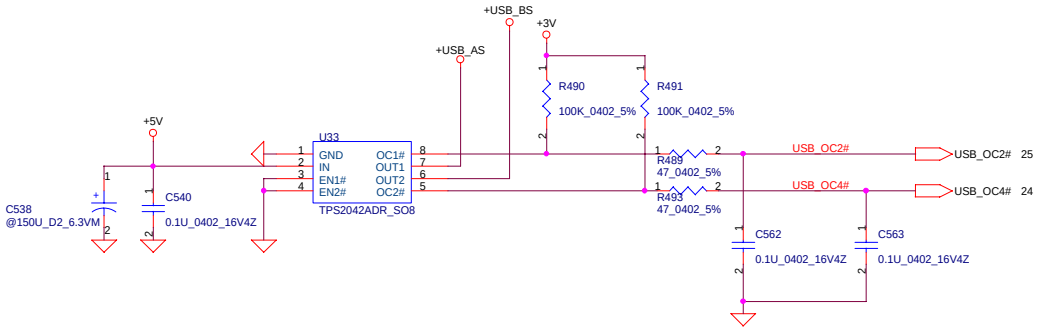
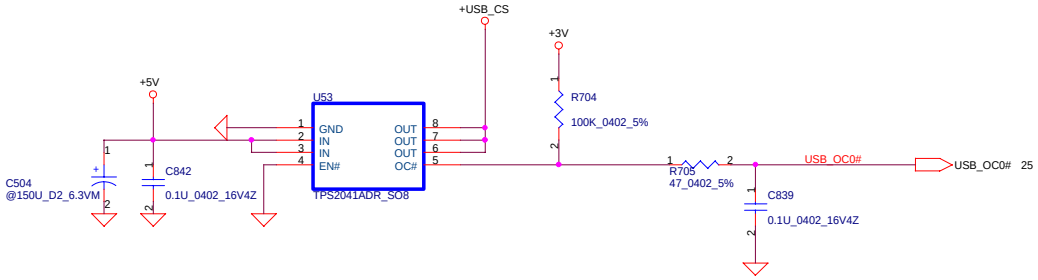
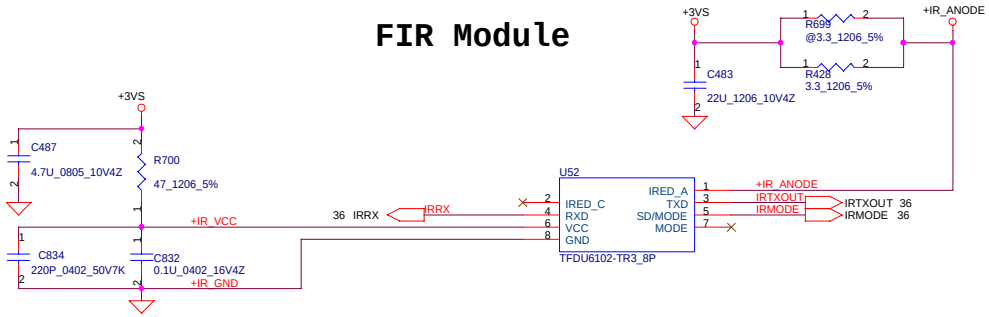
Compal Electronics, Inc.

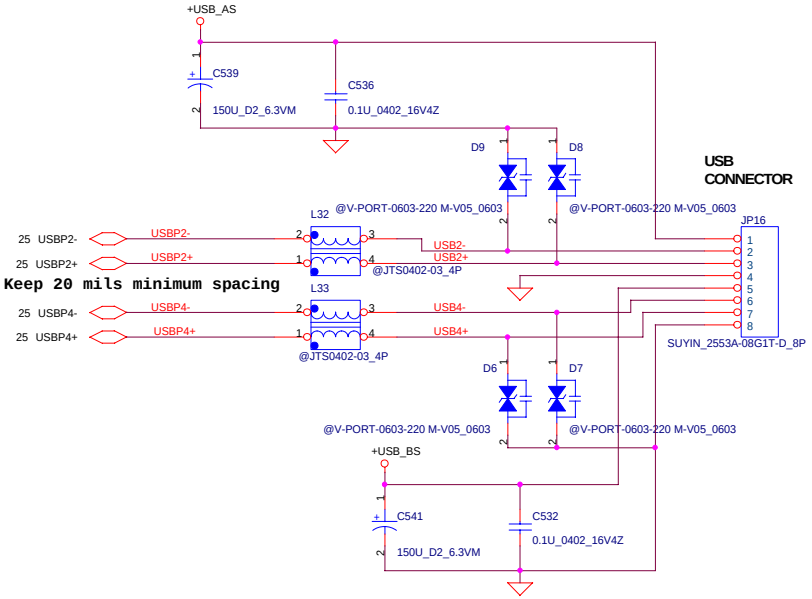
Title	SUPER I/O	
Size Custom	Document Number LA-2101	Rev 0.1
Date: Saturday, November 22, 2003	Sheet 36 of 52	

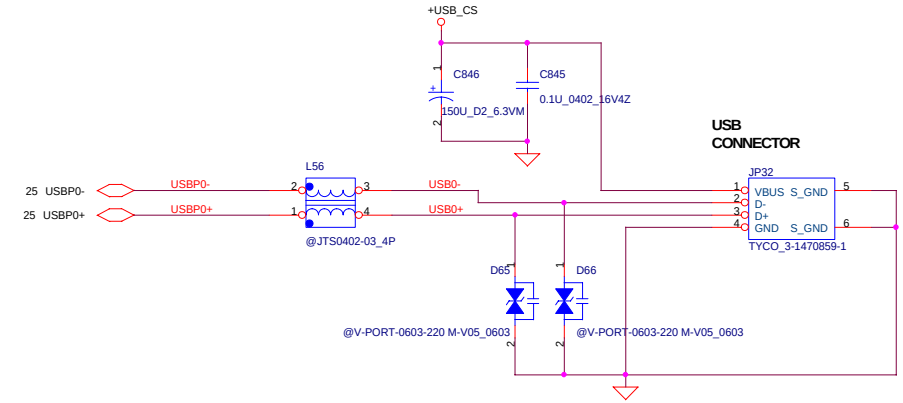


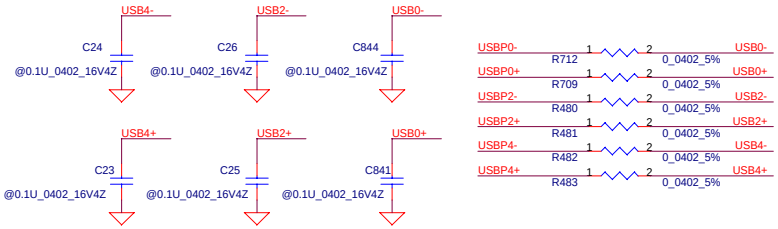


FIR Module

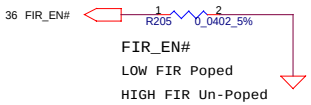








The component's most place cloely IRDA MODULE.



FIR_EN#
LOW FIR Poped
HIGH FIR Un-Poped

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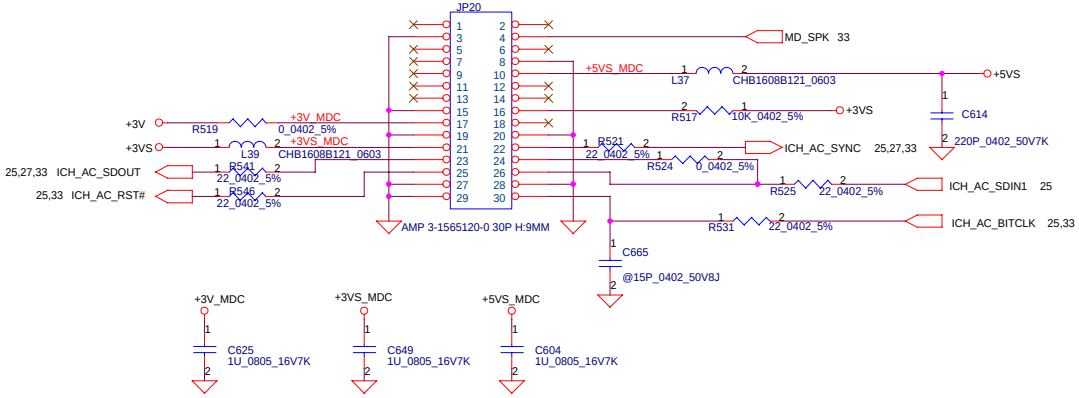
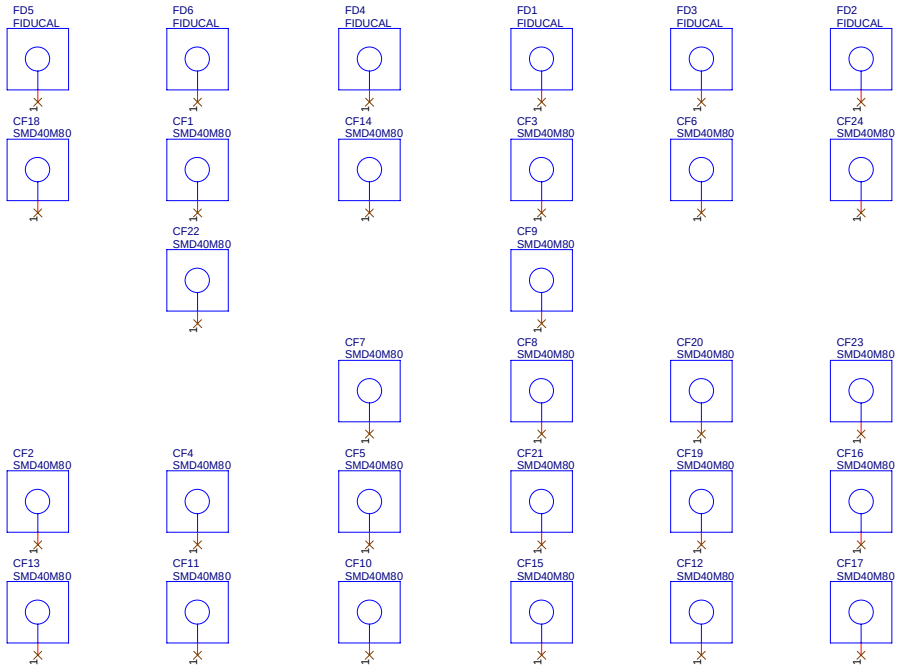
Compal Electronics, Inc.

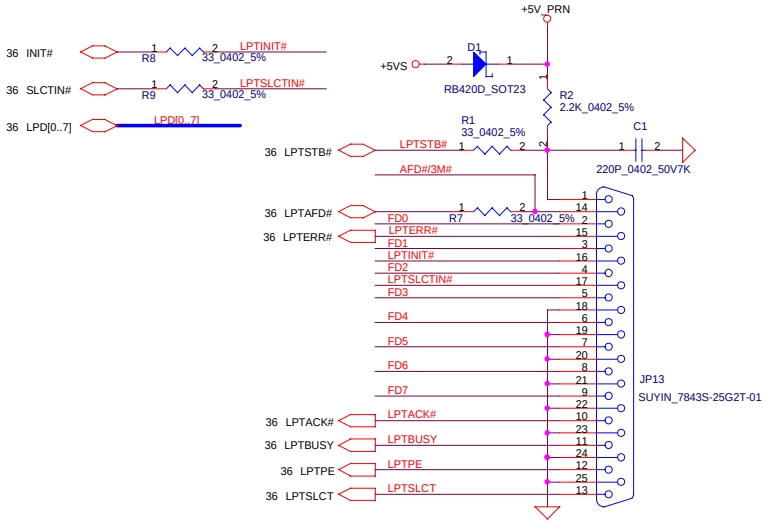
Title	USB Conn.	
Size: Custom	Document Number: LA-2101	Rev: 0.1
Date: Saturday, November 22, 2003	Sheet 37 of 52	

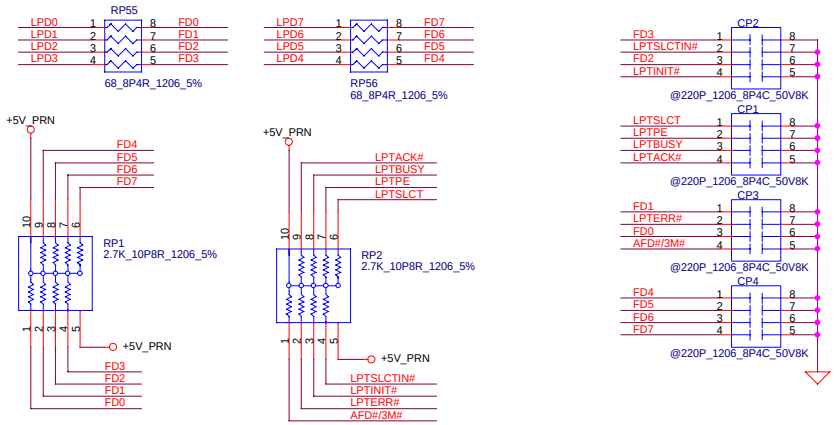
MDC CONN.





PARALLEL PORT





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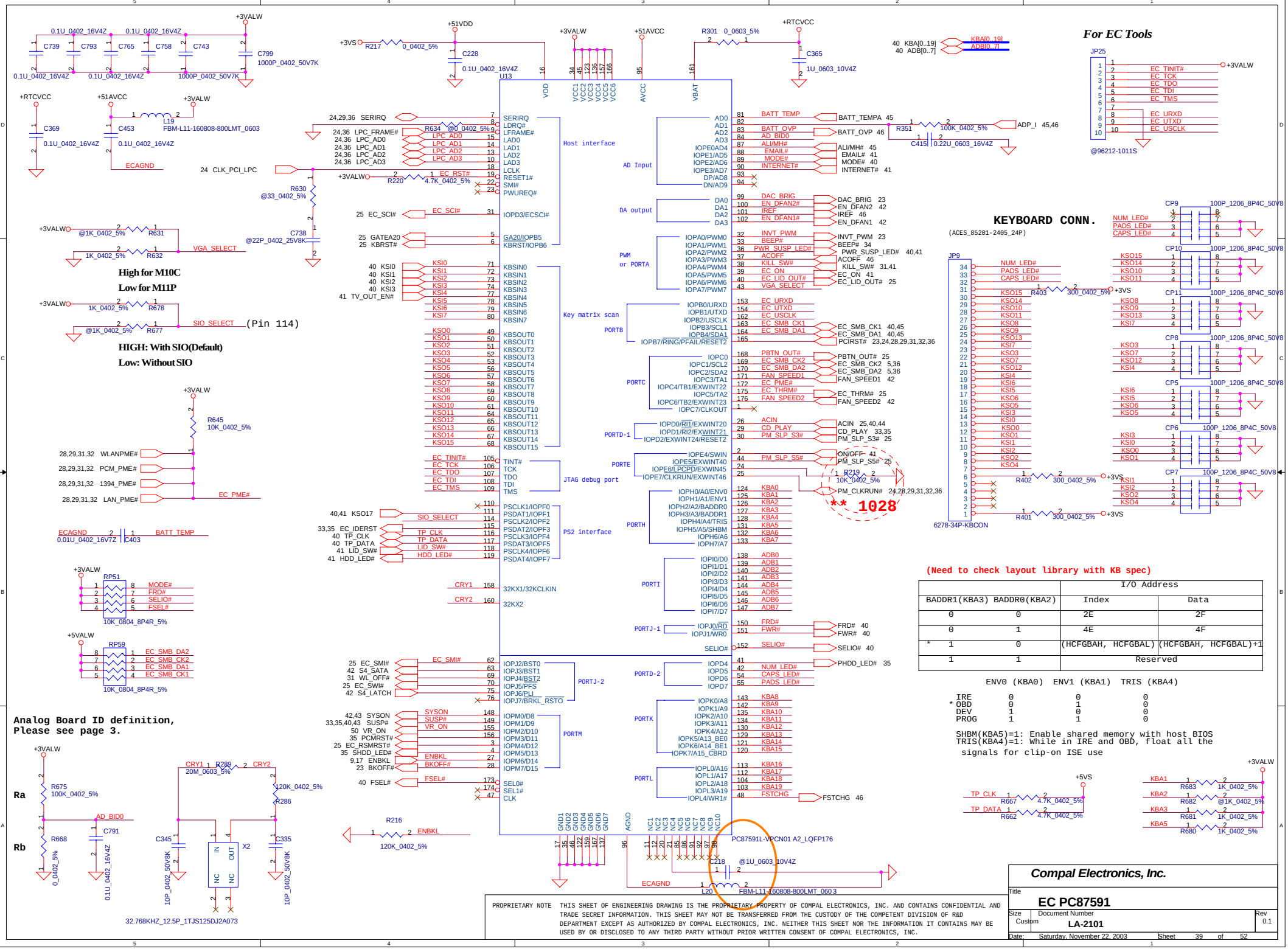
Compal Electronics, Inc.

Title	PARALLEL/MDC PORT	
Size	Document Number LA-2101	Rev 0.1
Date: Saturday, November 22, 2003	Sheet 38 of 52	



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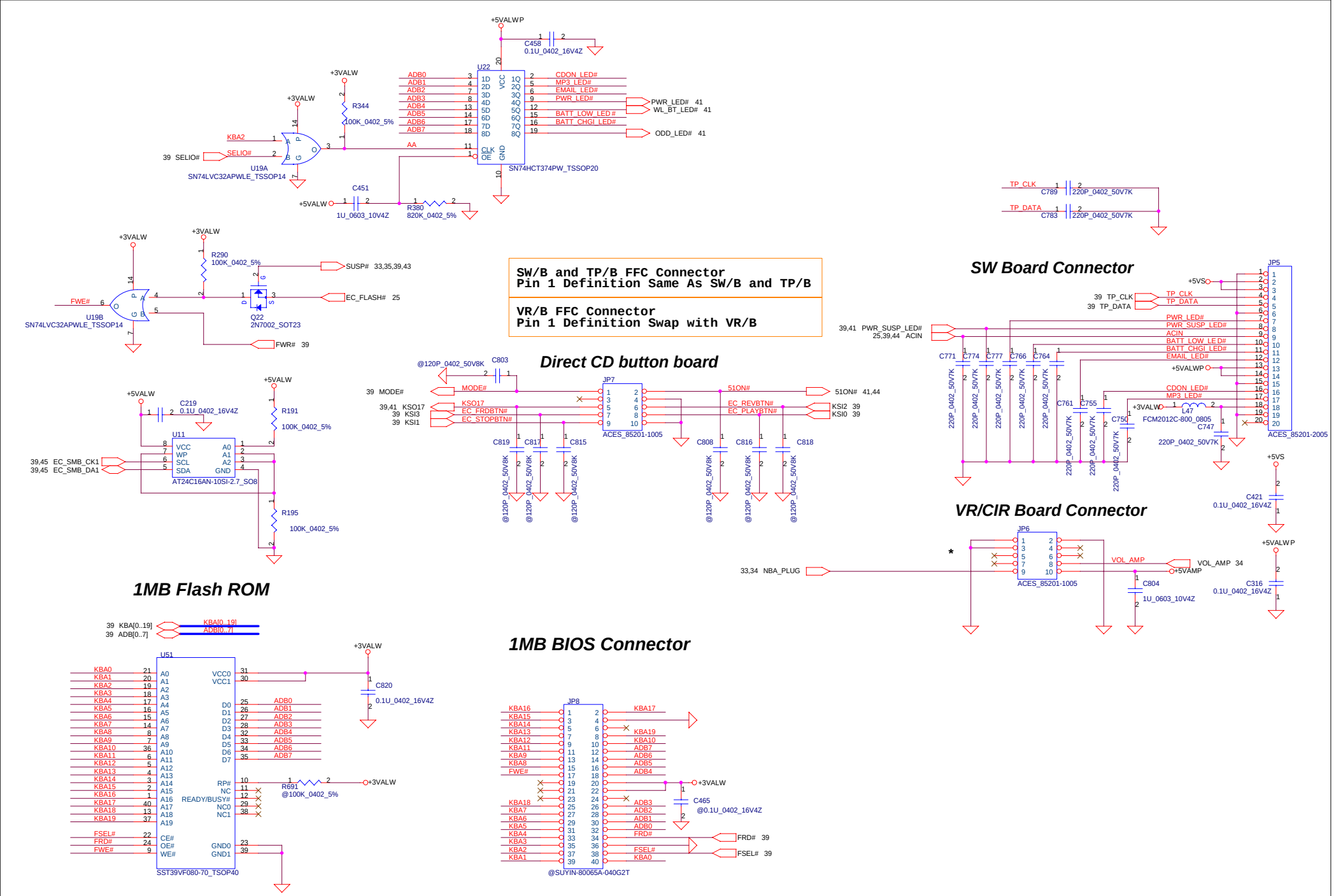

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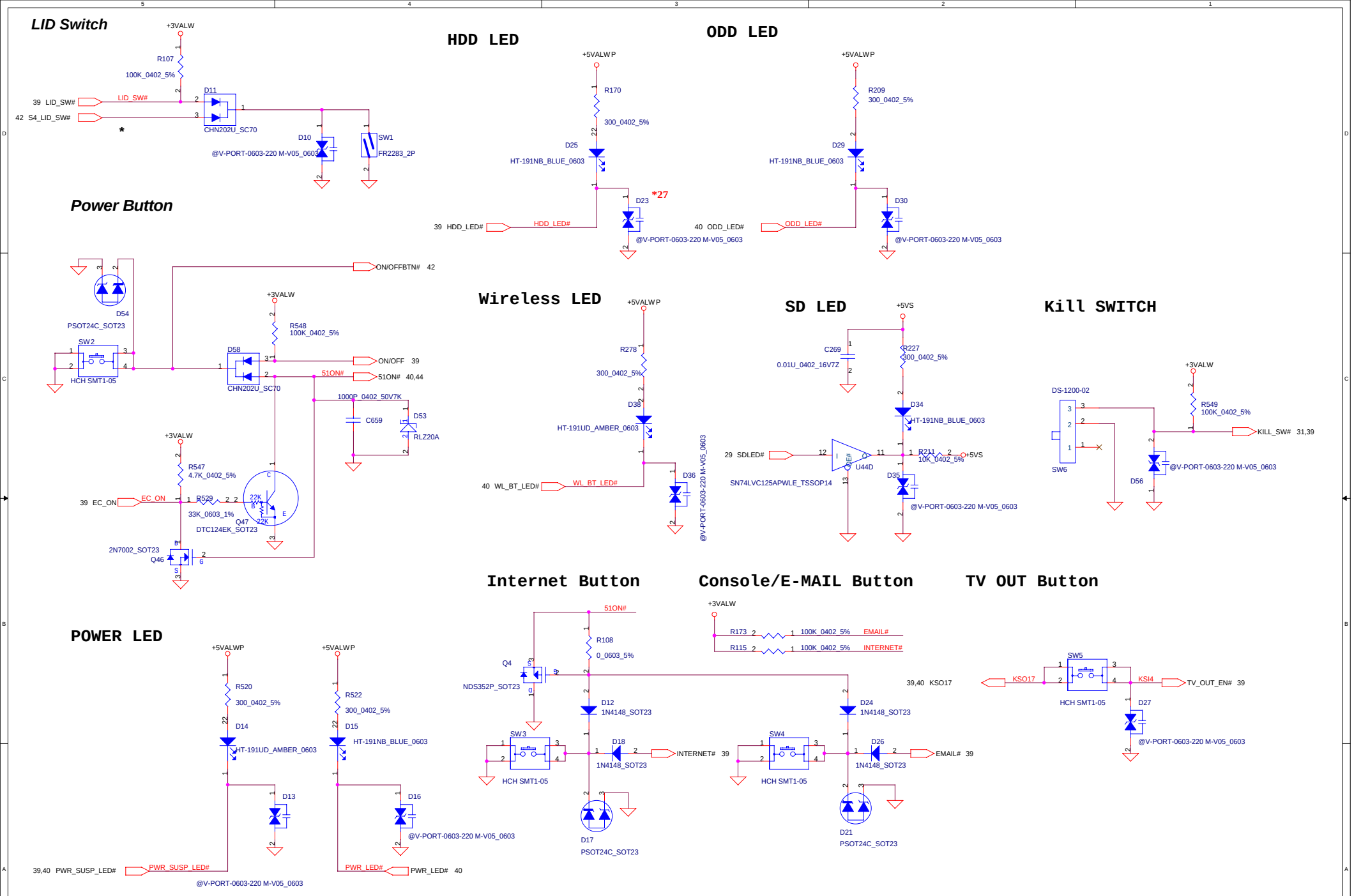
Compal Electronics, Inc.

Title	BIOS & EXT. I/O PORT	
Size: Custom	Document Number: LA-2101	Rev: 0.1
Date: Saturday, November 22, 2003	Sheet 40 of 52	



Compal Electronics, Inc.	
Title	Switchs & Connectors
Size: Custom	Document Number: LA-2101
Rev	0.1
Date: Saturday, November 22, 2003	Sheet 41 of 52

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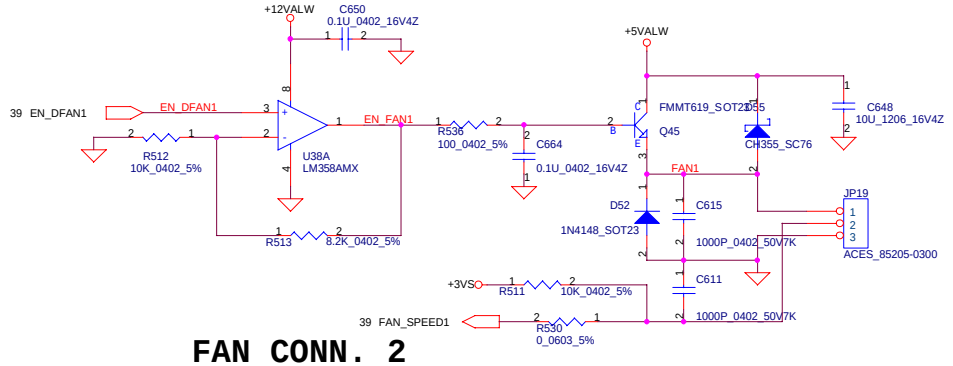
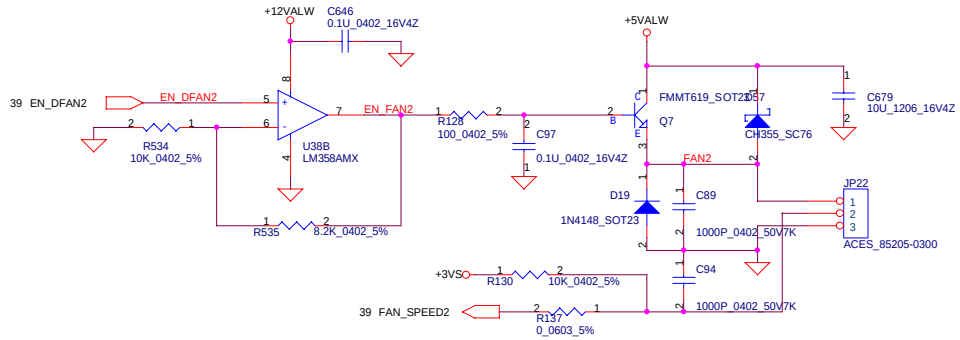
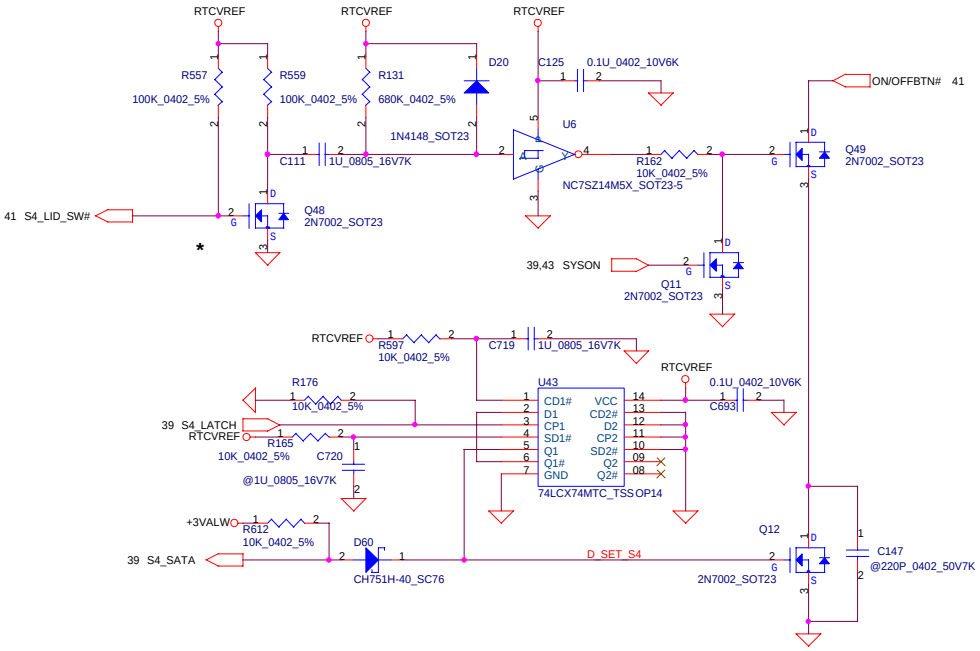
FAN CONN. 1



FAN CONN. 2



Battery mode Hibernation



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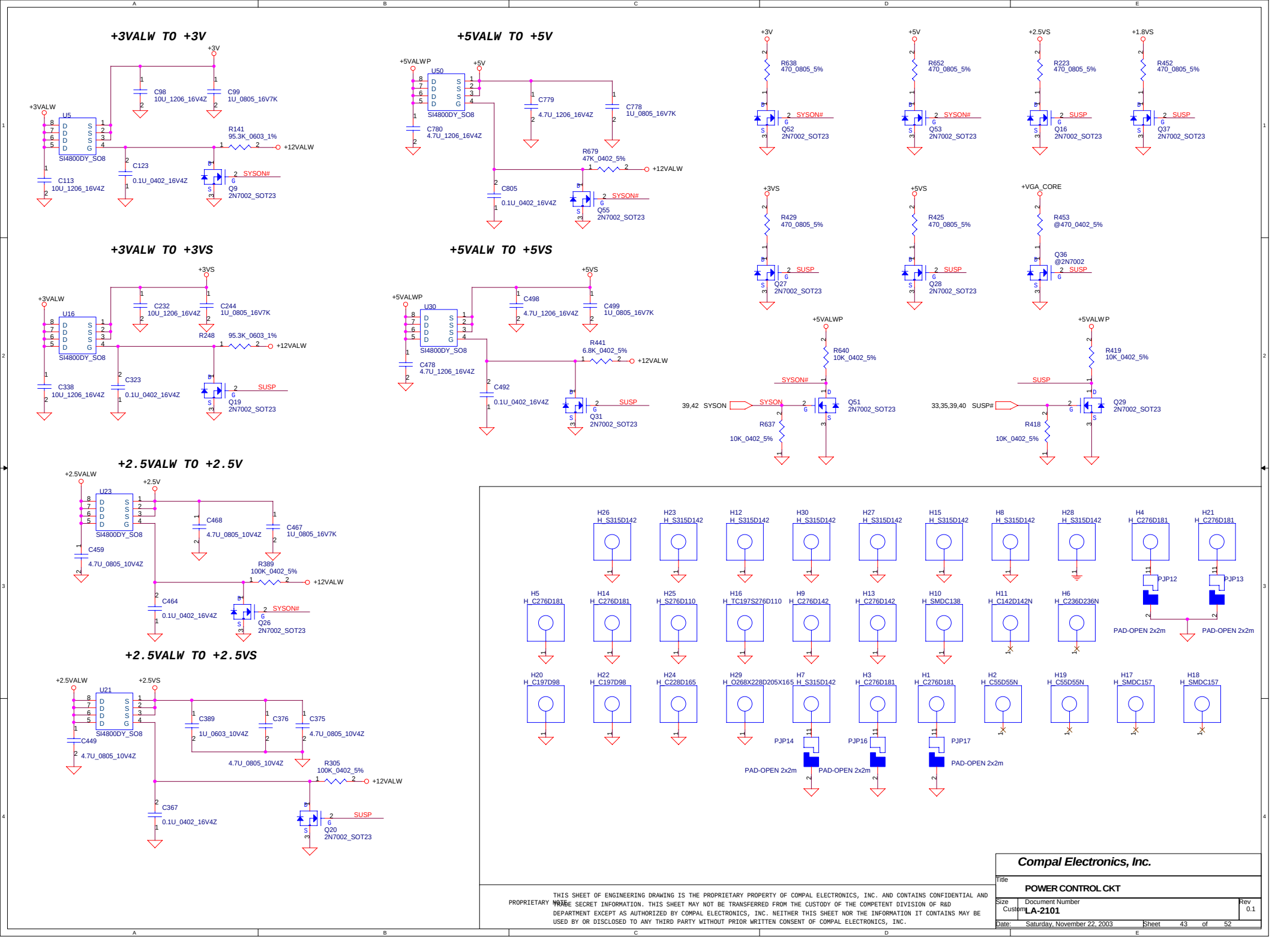
Compal Electronics, Inc.		
Title: Power OK/Reset/RTC battery/Lid Switch/Int. KB		
Size	Document Number: LA-2101	Rev: 0.1
Date: Saturday, November 22, 2003	Sheet 42 of 52	



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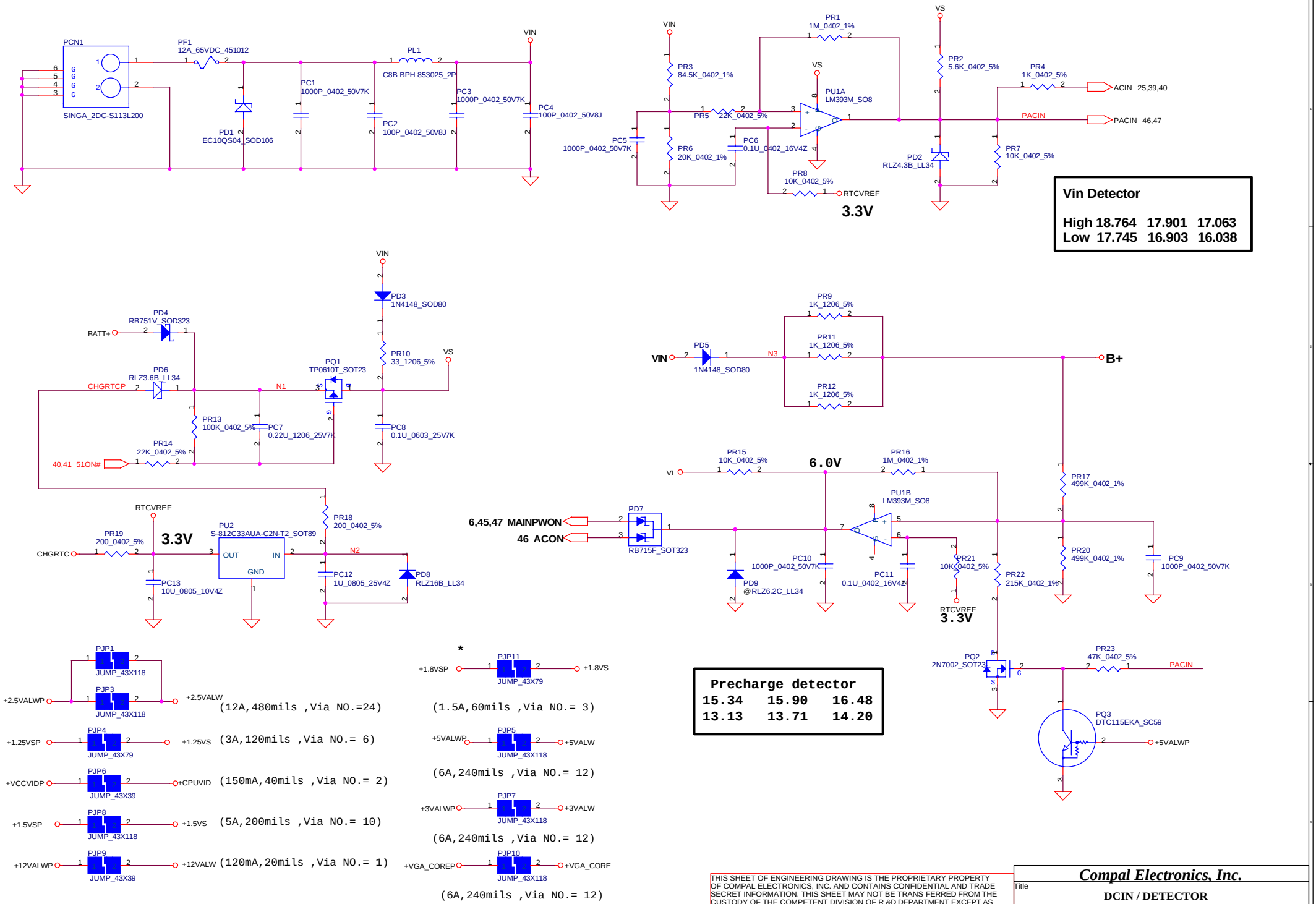
Compal Electronics, Inc.

Title	POWER CONTROL CKT
Size: Custom	Document Number: LA-2101
Rev	0.1
Date: Saturday, November 22, 2003	Sheet 43 of 52



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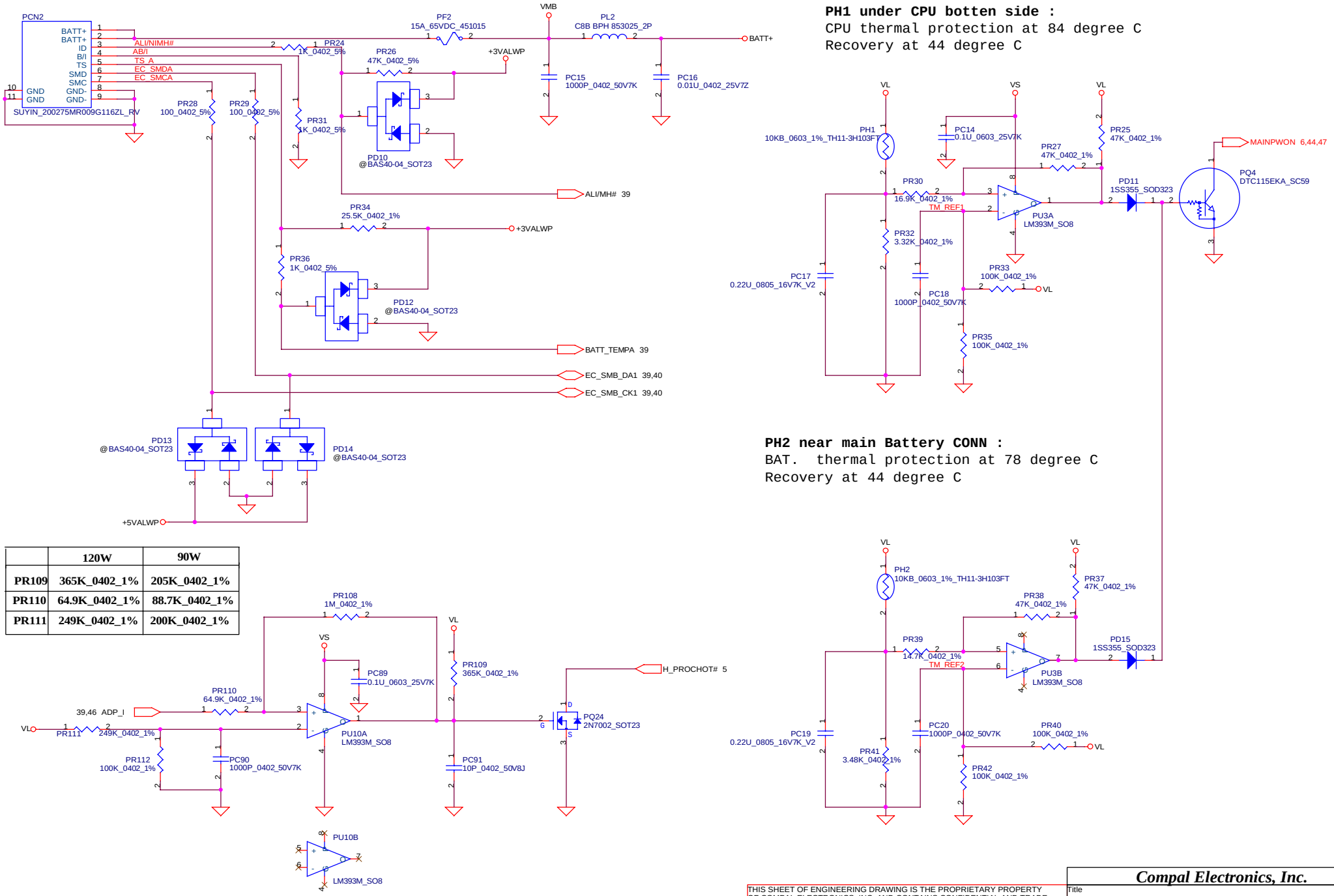
Compal Electronics, Inc.

Title: DCIN / DETECTOR

Size | Document Number: LA-2101 | Rev: 0.1

Date: Saturday, November 22, 2003 | Sheet 44 of 52



PH1 under CPU botten side :
CPU thermal protection at 84 degree C
Recovery at 44 degree C

PH2 near main Battery CONN :
BAT. thermal protection at 78 degree C
Recovery at 44 degree C

	120W	90W
PR109	365K_0402_1%	205K_0402_1%
PR110	64.9K_0402_1%	88.7K_0402_1%
PR111	249K_0402_1%	200K_0402_1%

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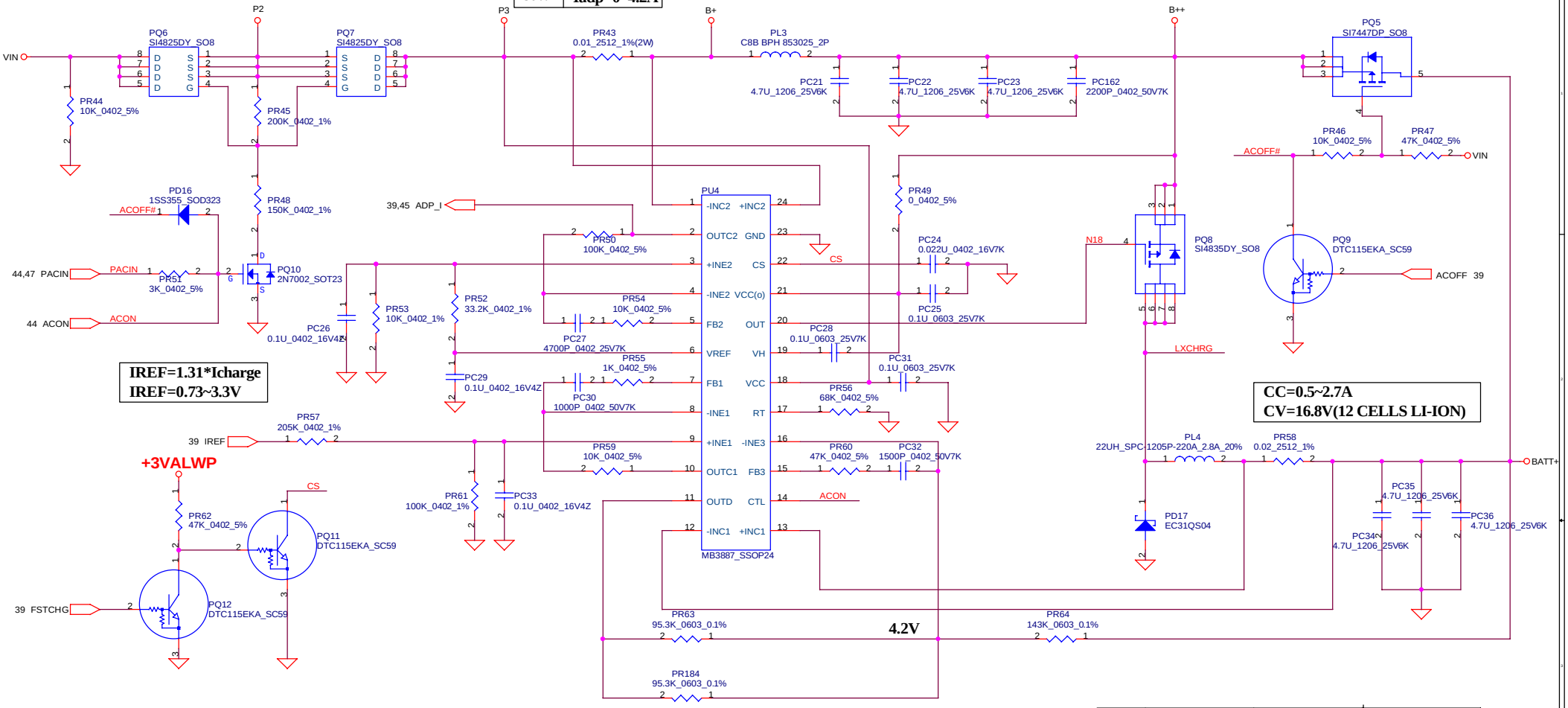
Compal Electronics, Inc.

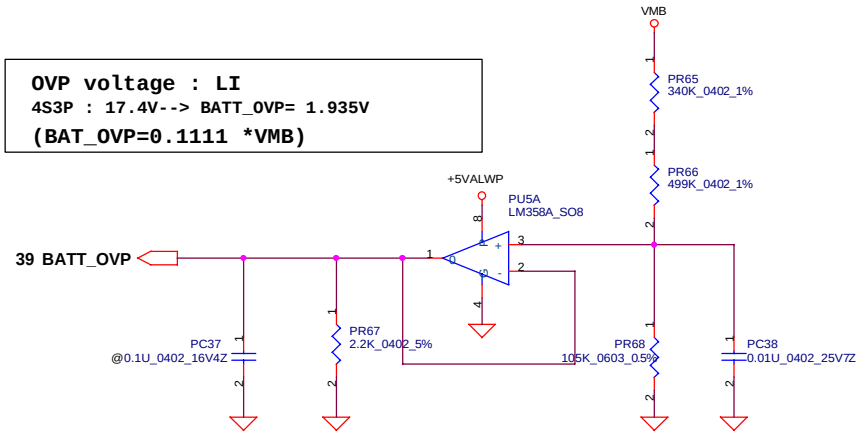
Title	BATTERY CONN / OTP /Throttling
Size	
Document Number	LA-2101
Rev	0.1
Date: Saturday, November 22, 2003	Sheet 45 of 52

120W	Iadp=0~5.8A
90W	Iadp=0~4.2A



	PR43	PR52	PQ5
120W	0.01_2512_1%	33.2K_0402_1%	SI7447DP_SO8
90W	0.015_2512_1%	29.4K_0402_1%	SI4825DY_SO8

OVP voltage : LI
4S3P : 17.4V--> BATT_OVP= 1.935V
(BAT_OVP=0.1111 *VMB)



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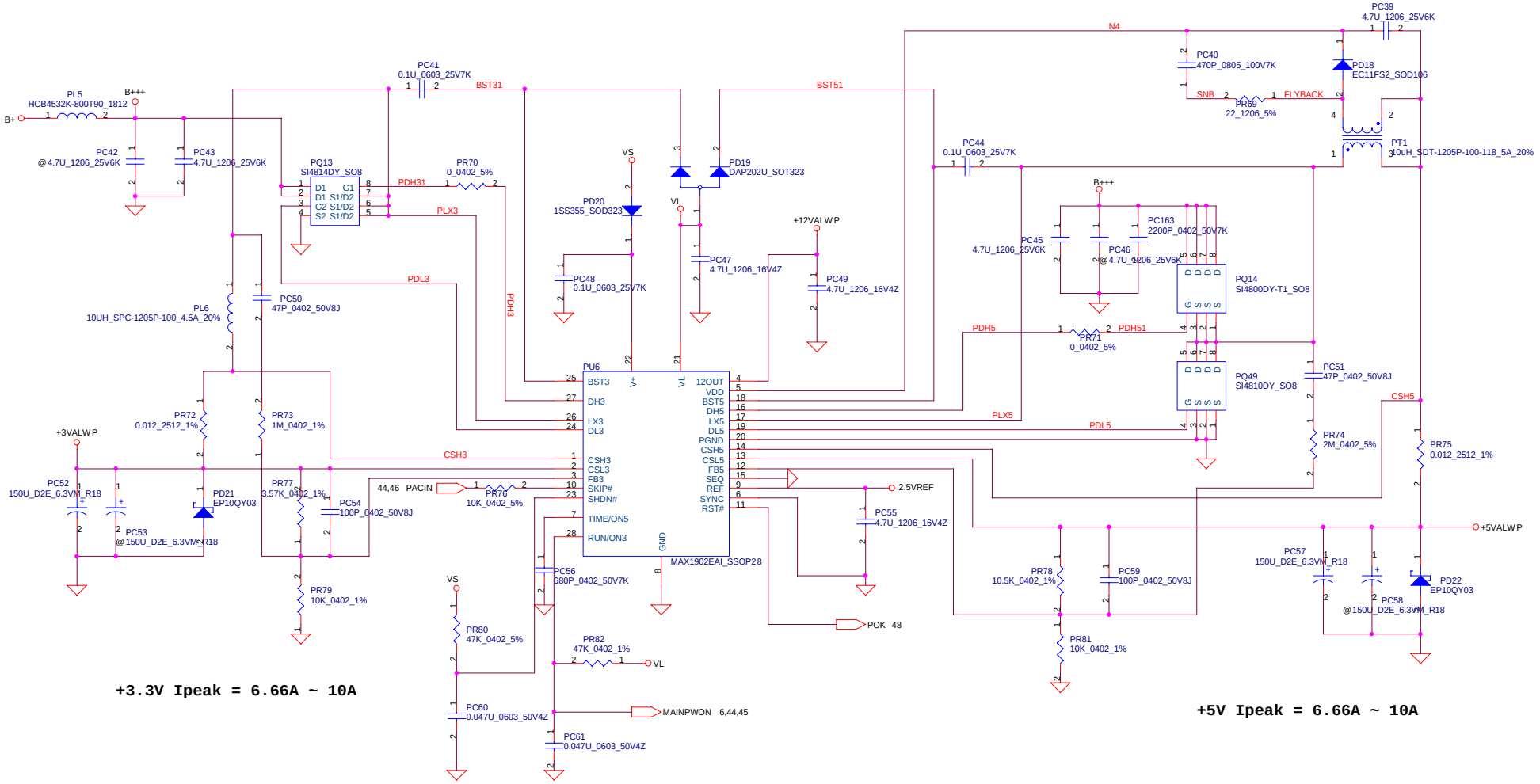
Compal Electronics, Inc.

Title	CHARGER	
Size	Document Number LA-2101	Rev 0.1
Date: Saturday, November 22, 2003	Sheet 46 of 52	



+3.3V Ipeak = 6.66A ~ 10A

+5V Ipeak = 6.66A ~ 10A

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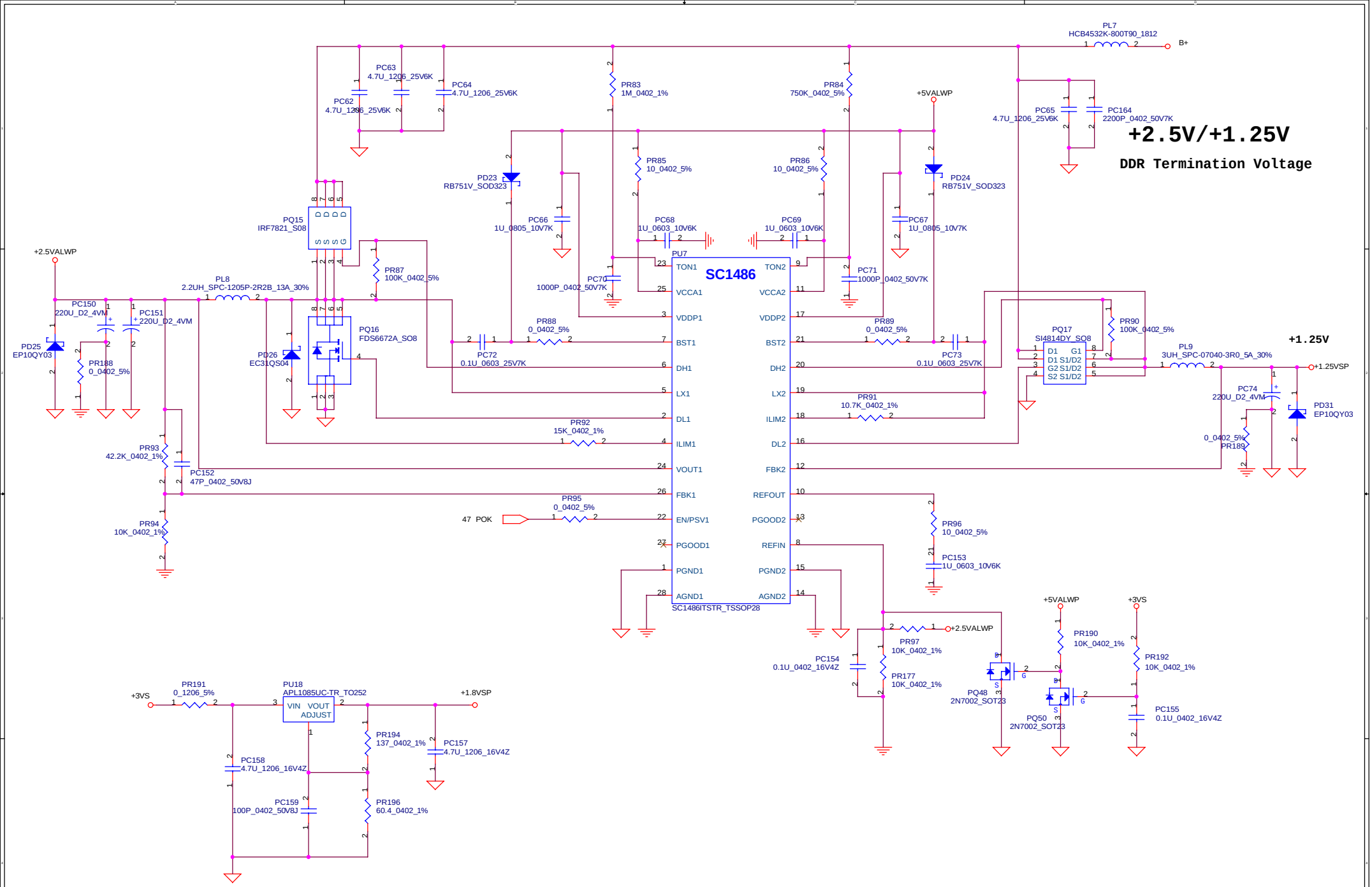
Compal Electronics, Inc.

Title	5V/3.3V/12V	
Size	Document Number: LA-2101	Rev 0.1
Date: Saturday, November 22, 2003	Sheet 47 of 52	



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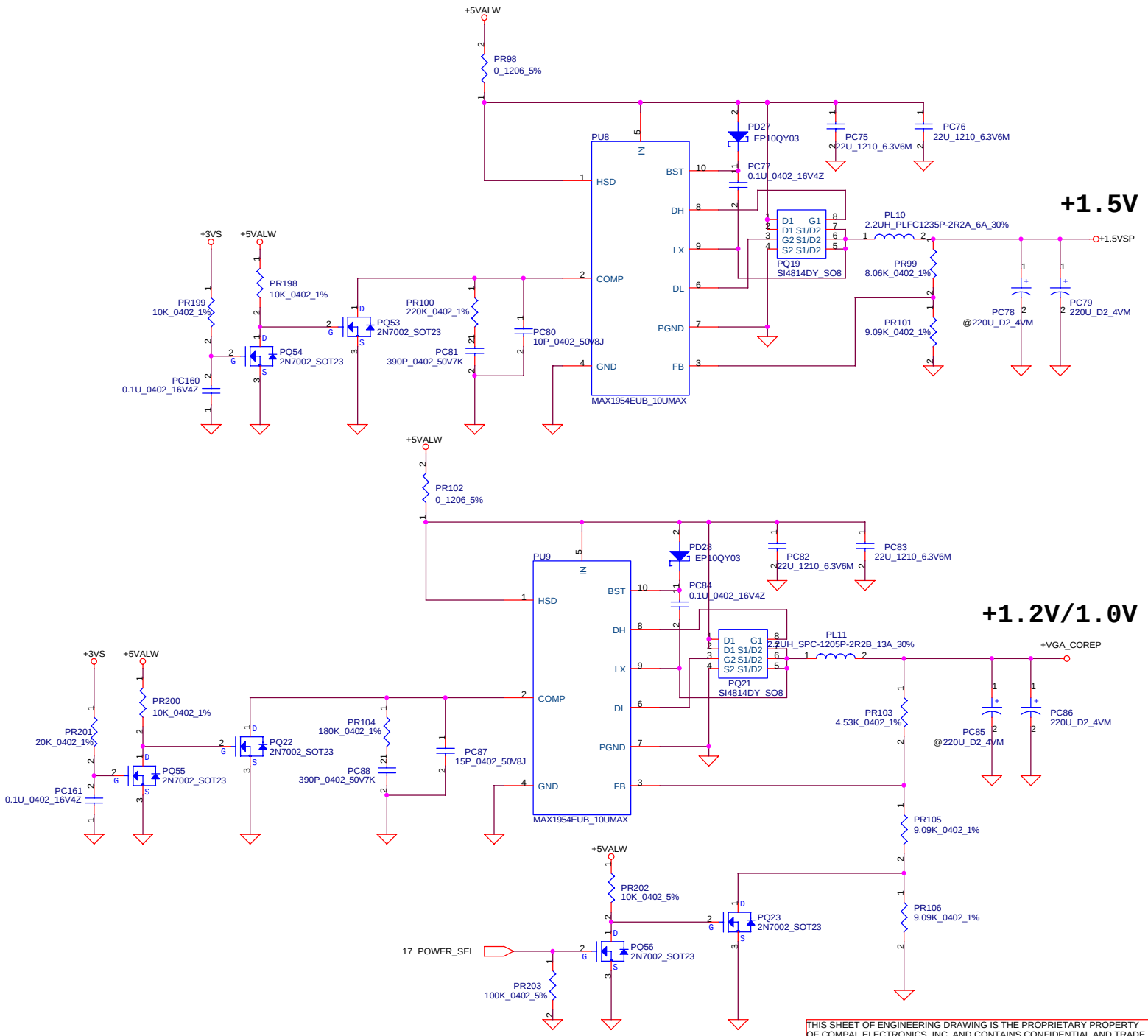
Compal Electronics, Inc.	
Title	DDR_2.5V/1.25V/1.8V
Size	Document Number: LA-2101 — Rev 0.1
Date: Saturday, November 22, 2003	Sheet 48 of 52



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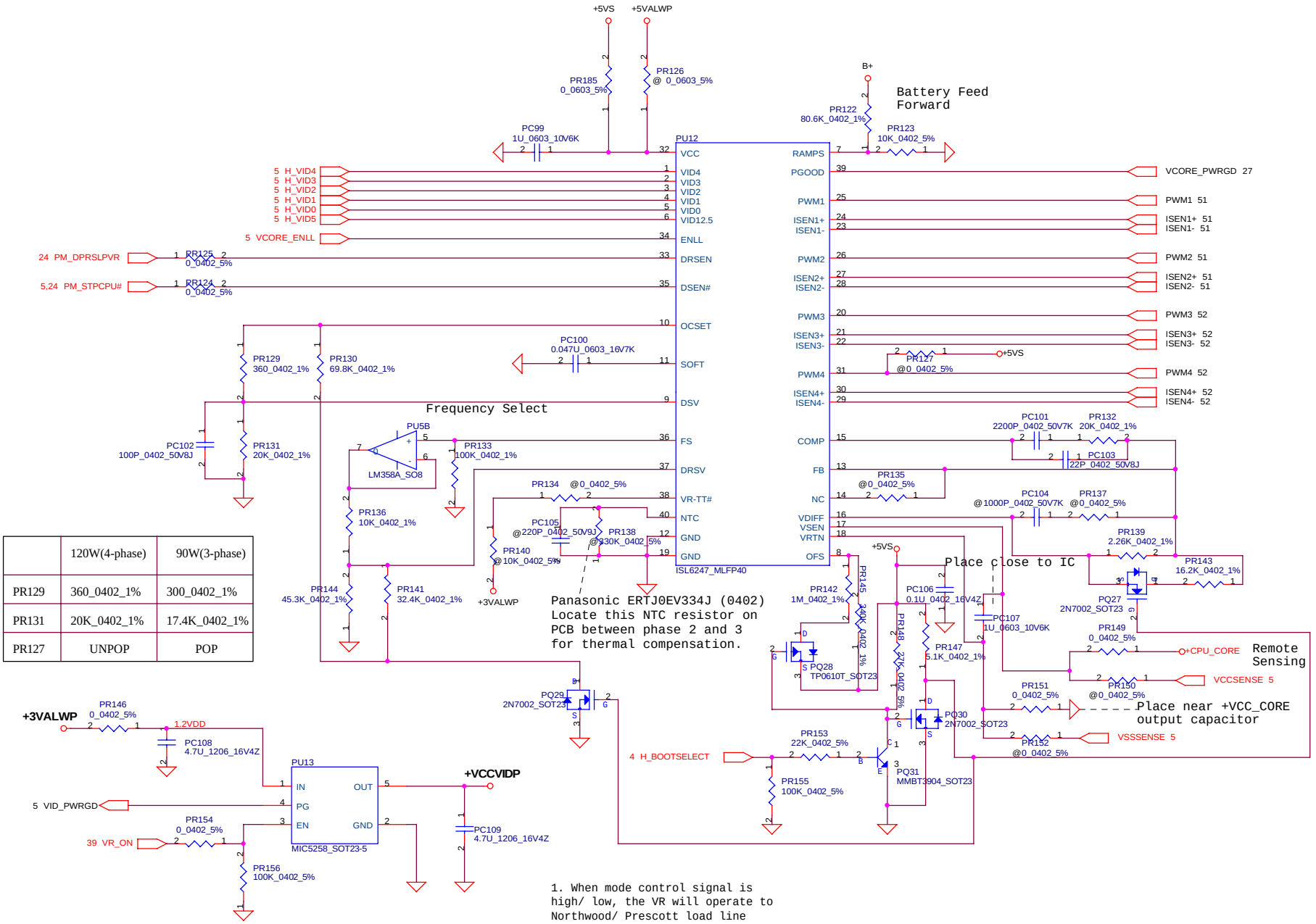
Compal Electronics, Inc.

Title	1.5V/VGA_CORE
Size	
Document Number	LA-2101
Rev	0.1
Date:	Saturday, November 22, 2003
Sheet	49 of 52



	120W(4-phase)	90W(3-phase)
PR129	360_0402_1%	300_0402_1%
PR131	20K_0402_1%	17.4K_0402_1%
PR127	UNPOP	POP

1. When mode control signal is high/ low, the VR will operate to Northwood/ Prescott load line (Northwood="0",Prescott="1")
2. VID5(12.5) should be pulled high, when the VR operates to Nothwood load line.

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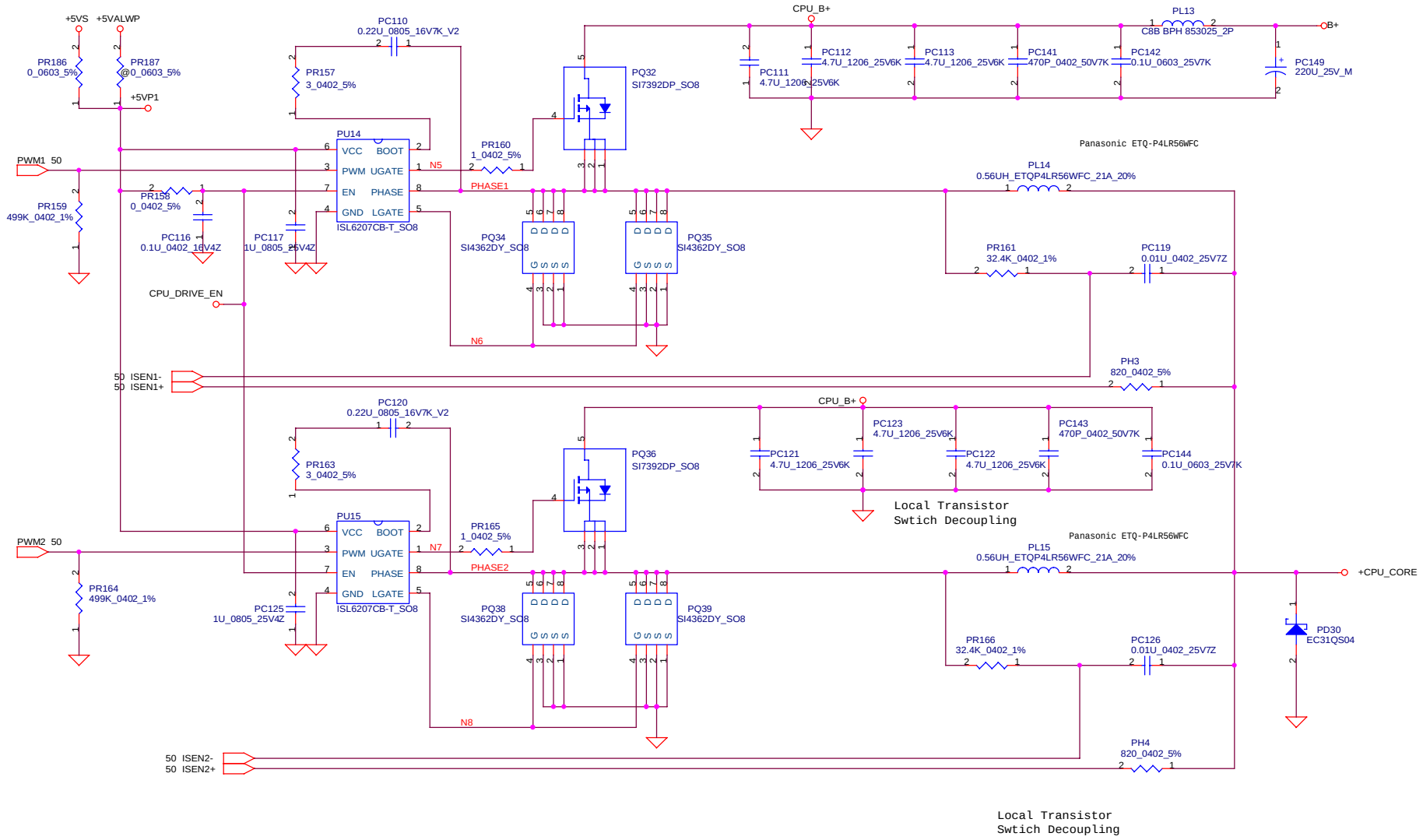
Compal Electronics, Inc.

Title: **CPU_CORE_Controller**

Size | Document Number: **LA-2101** | Rev: 0.1

Date: Saturday, November 22, 2003 | Sheet 50 of 52



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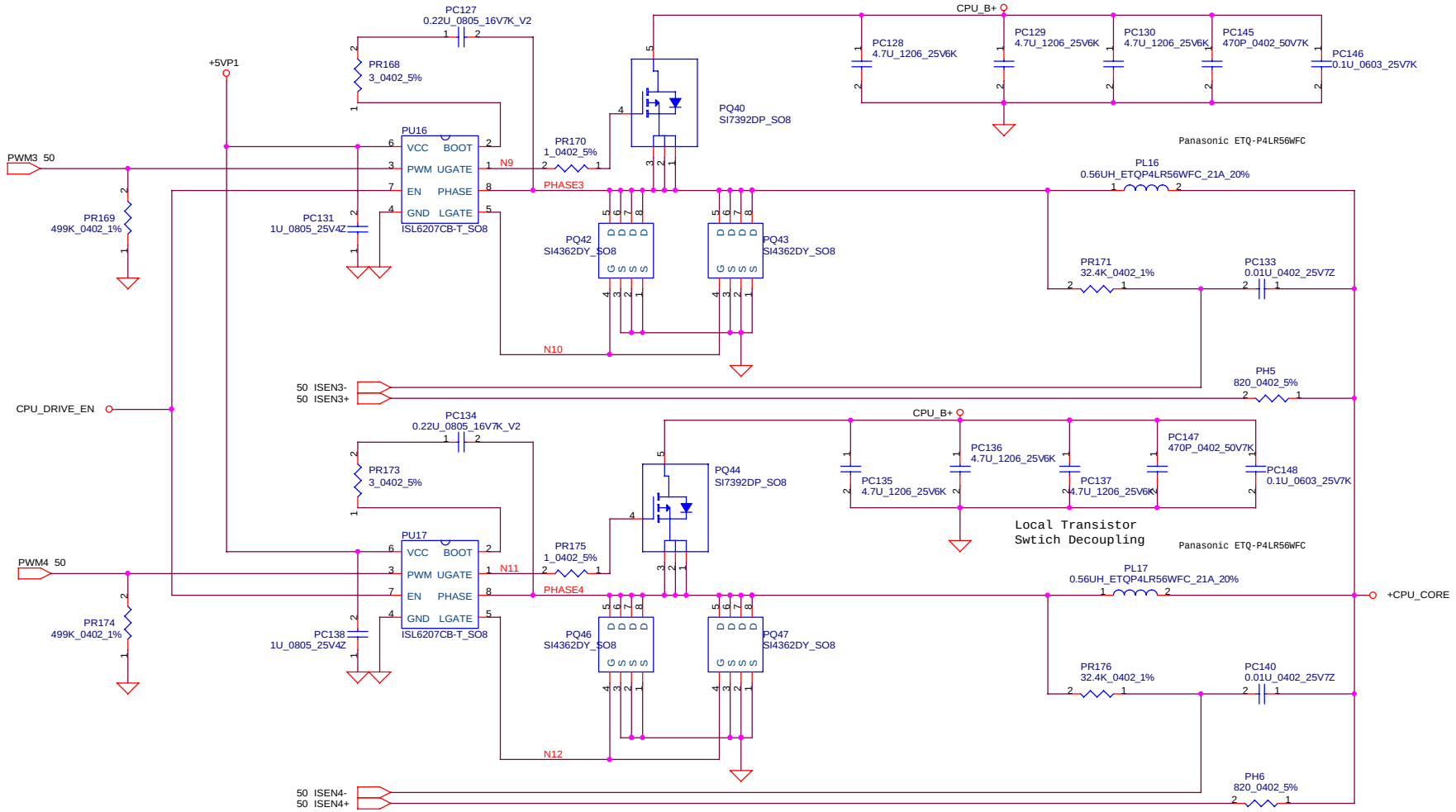
Compal Electronics, Inc.

Title	CPU_CORE_Power stage 1	
Size	Document Number LA-2101	Rev 0.1
Date: Saturday, November 22, 2003	Sheet 51 of 52	



	PC134,PC135,PC136,PC137,PC138,PC140, PC147,PC148,PR173,PR174,PR175,PR176, PQ44,PQ46,PQ47,PU17,PL17,PH6
120W(4-phase)	POP
90W(3-phase)	UNPOP

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Compal Electronics, Inc.

Title: CPU_CORE_Power stage 2

Size | Document Number: LA-2101 | Rev: 0.1

Date: Saturday, November 22, 2003 | Sheet 52 of 52