

Compal Confidential

ISRAE LA-3711P Schematics Document

Intel Yonah/Merom with 945GM/943GML/940GML+ DDRII + ICH7M

2007-02-02

REV: 1.0

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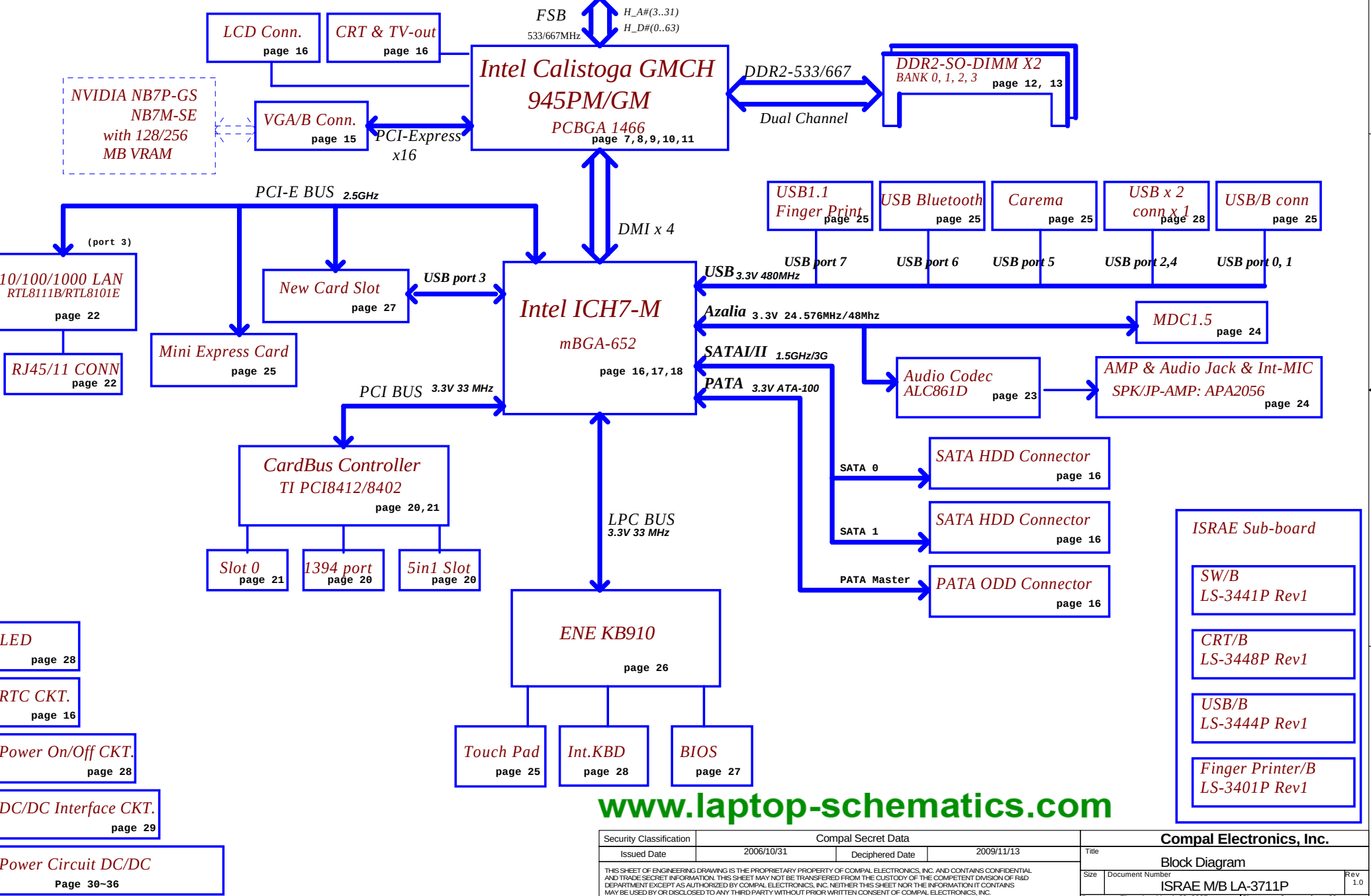
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Compal confidential

Model : ISRAE

File Name : LA-3711P

NAPA Platform



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	+VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
1394	D0	AD20	2	A,B,C
CARD BUS	D4	AD20	2	A,B,C
5IN1	D4	AD20	2	A,B,C

KB910 I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
SM1 24C16	A0H	1 0 1 0 0 0 0 X b
SM1 SMART BATTERY	16H	0 0 1 0 1 1 X b
SM2 ADM0132	98H	1 0 0 1 1 0 0 X b
CPU THERMAL MONITOR		

ICH7-M SM Bus address

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

SKU ID Table

SKU ID	SKU
0	10 (10E)(10M)
1	10C
2	10G(10MG)
3	10GC
4	10J(10EJ) (10MJ)
5	10CJ
6	10G(10MG)J
7	10GC(10MGC)J

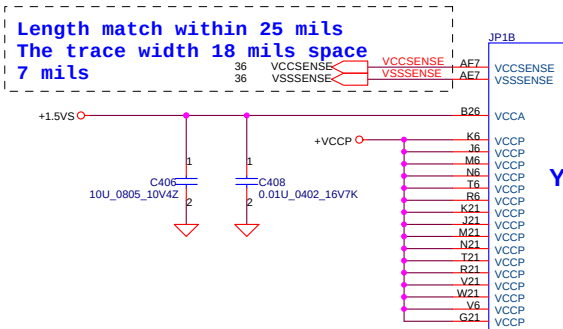
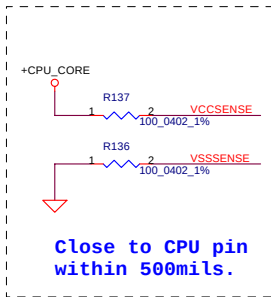
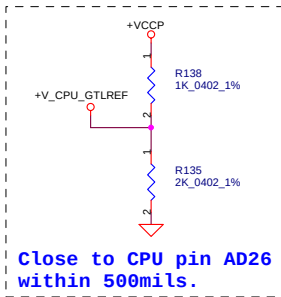
BTO Option Table

BTO Item	BOM Structure
45 level	45@
2ND HDD	2HDD@
LAN	100M@/1000M@
WLAN	KS@
MDC	MDC@
Blue tooth	BT@
Card ctrller	8412@/8402@/4512@
FINGER PRINT	FP@
5IN1	5IN1@, NON5IN1@
Express card	NEWCARD@
PCMCIA	PCMCIA@
Carema+MIC	CAREMA@
VGA FAN	FAN2@
CHIPSET (R3)	GMLR3@, GM@, ICH7R3@
change R3 to R1 for FRU	GMR3@, GM@, ICH7R3@
CIR	PMR3@, PM@, ICH7R3@
CIR	CIR@
Energy Star	ENG@

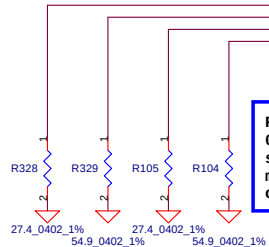
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Security Classification		Compal Secret Data		Compal Electronics, Inc. Yonah CPU in mFCPGA479							
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CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1



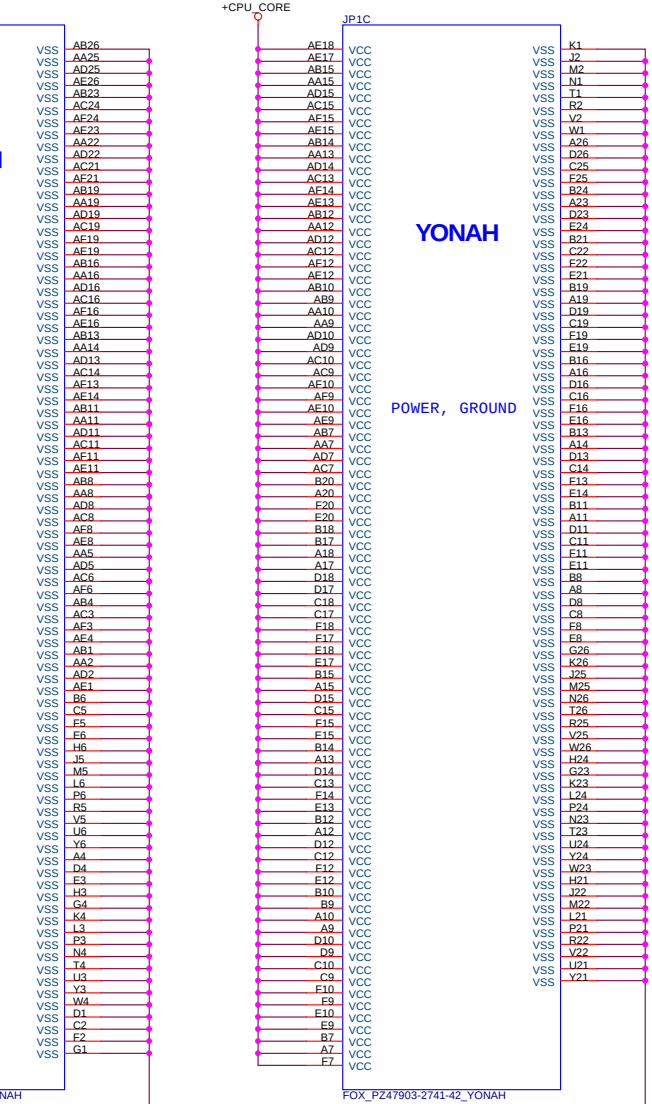
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal.

YONAH

YONAH

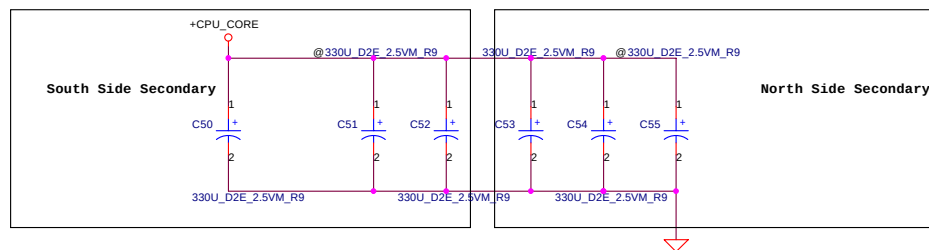
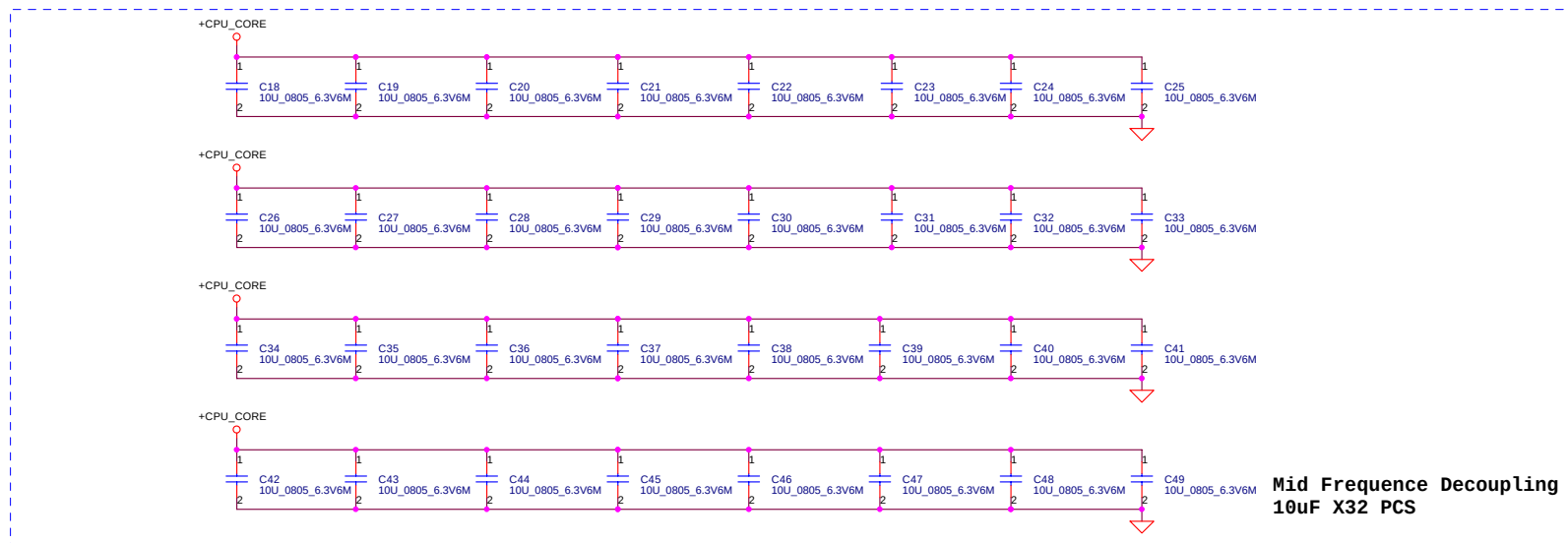
POWER, GROUND

POWER, GROUND, RESERVED SIGNALS AND NC



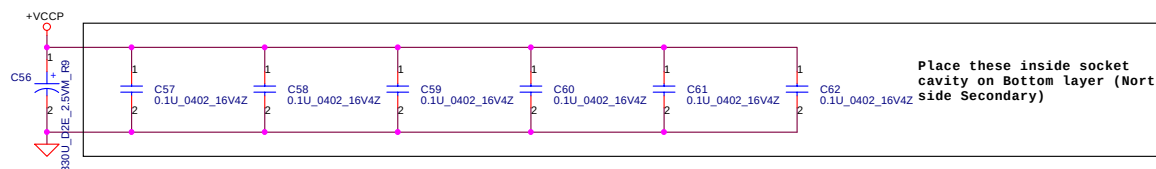
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ESR <= 1.5m ohm
Capacitor > 1980uF

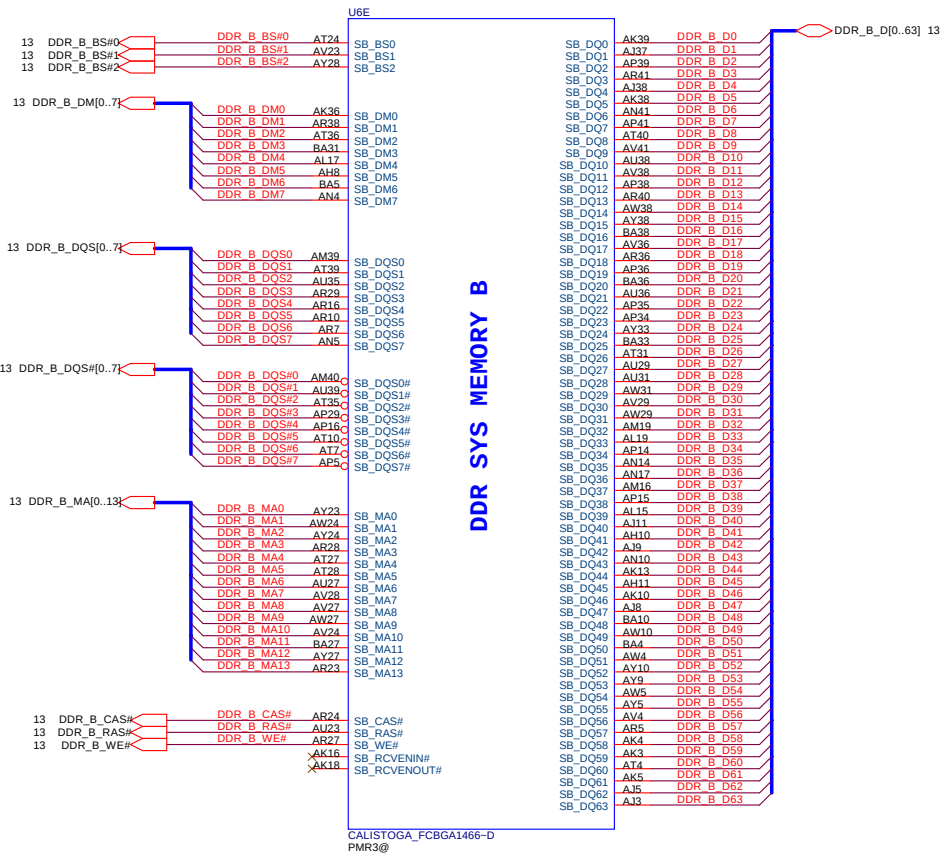
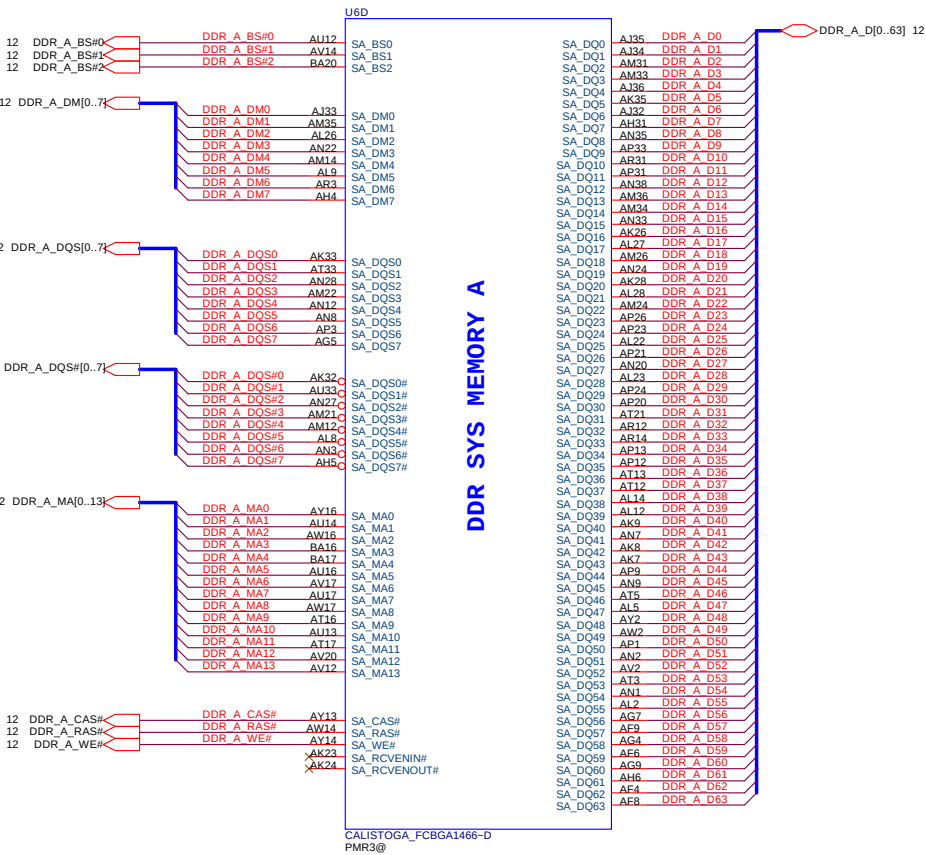
330uF ESR 9m ohm X 6 PCS



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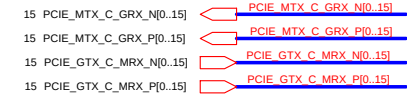
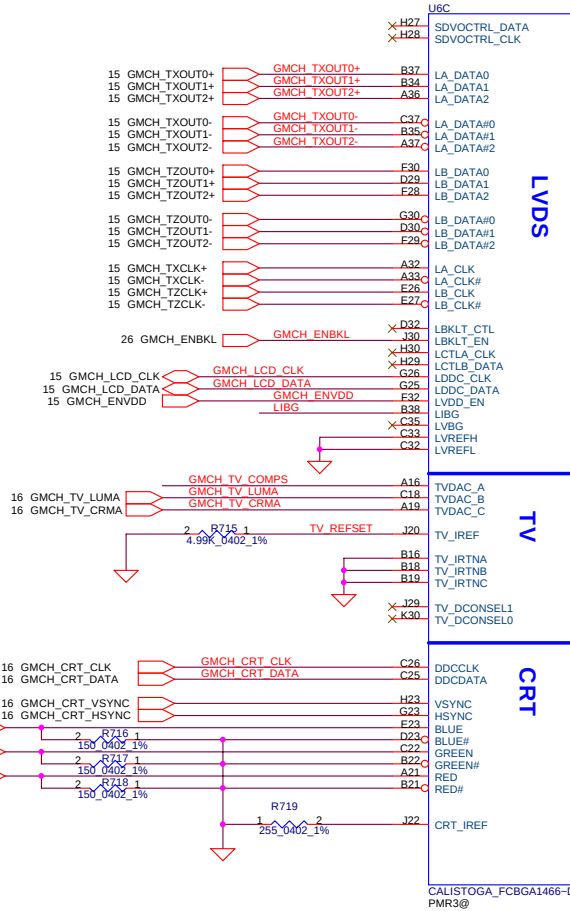
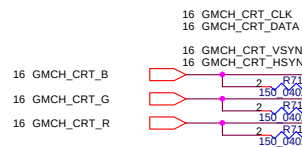
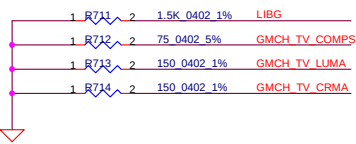
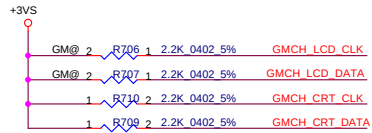
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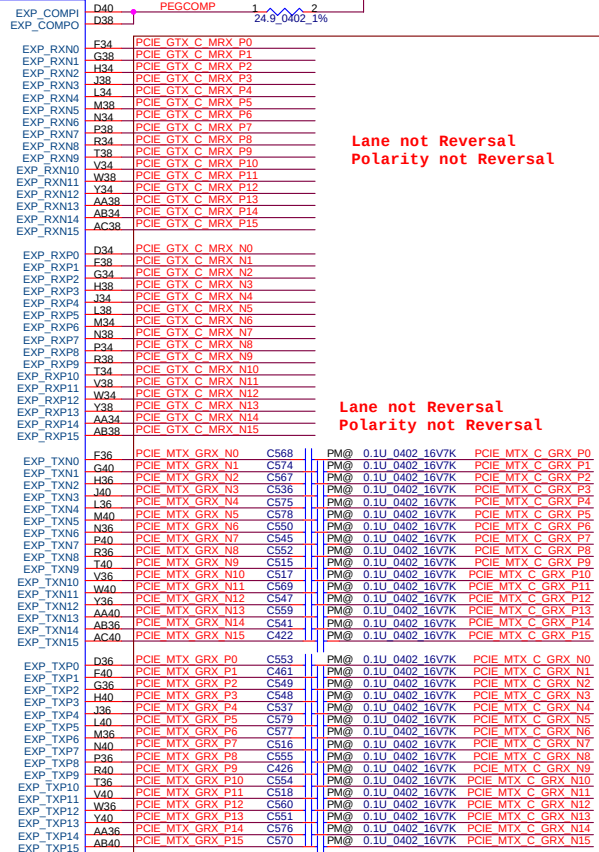


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PEGCOMP trace width and spacing is 18/25 mils.



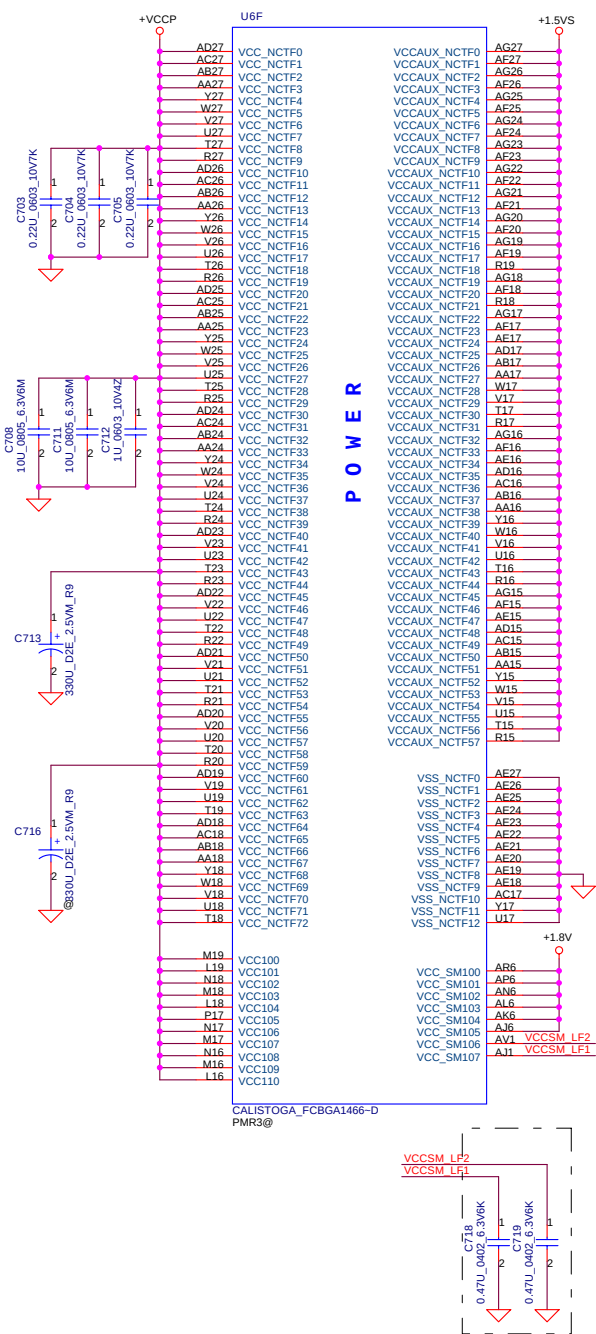
Lane not Reversal
Polarity not Reversal

Lane not Reversal
Polarity not Reversal

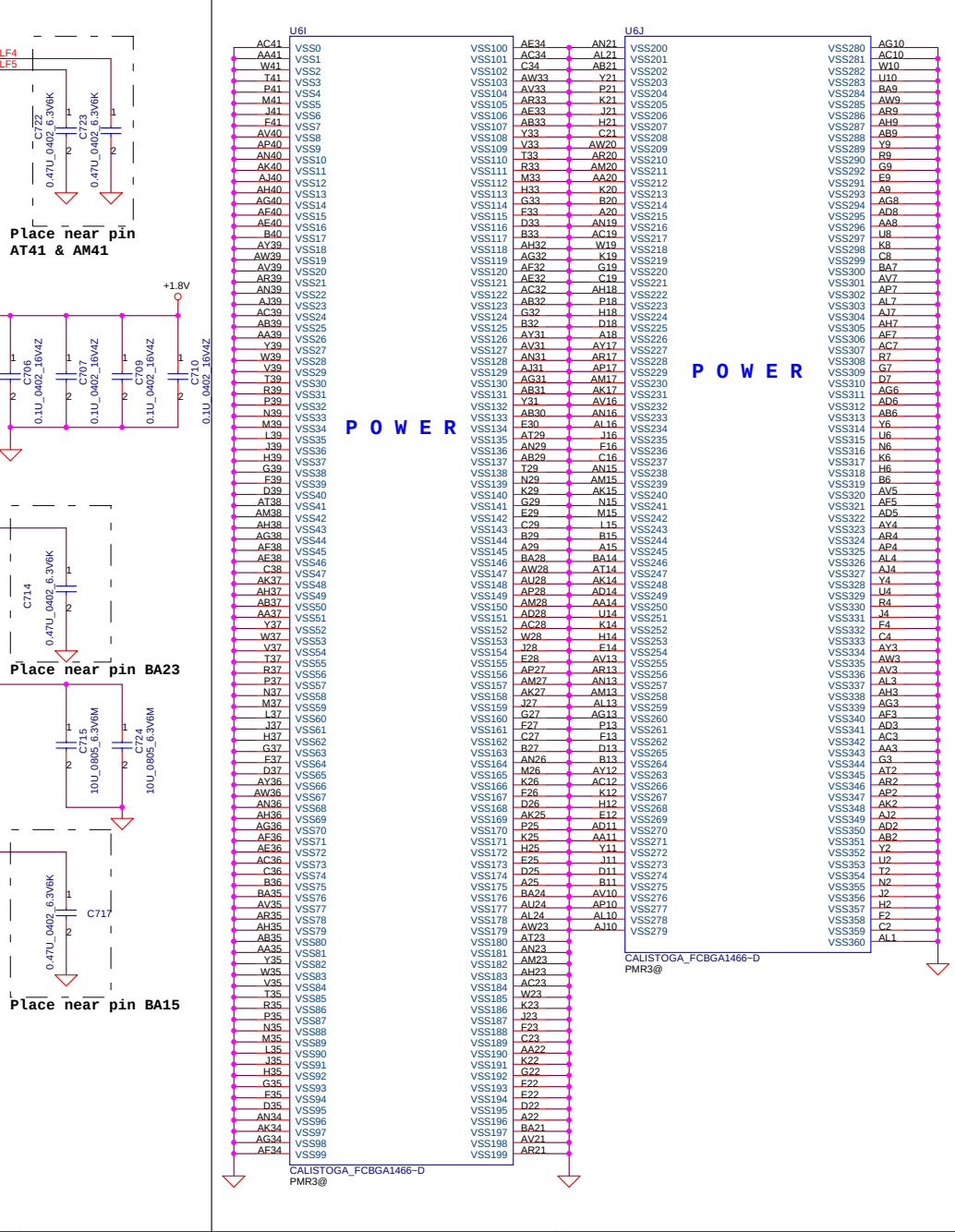
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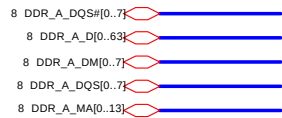
POWER



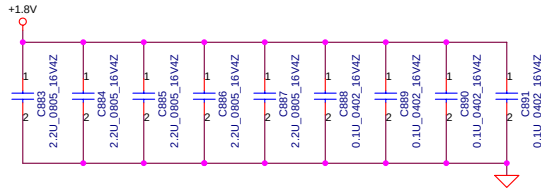
GND



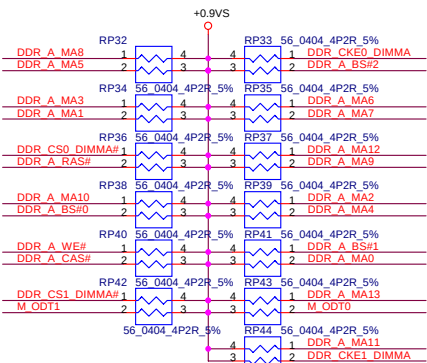
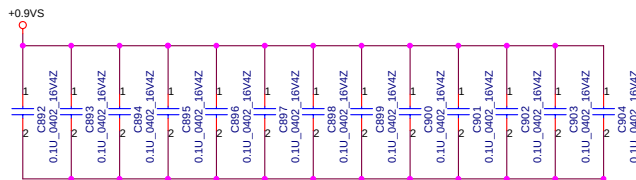
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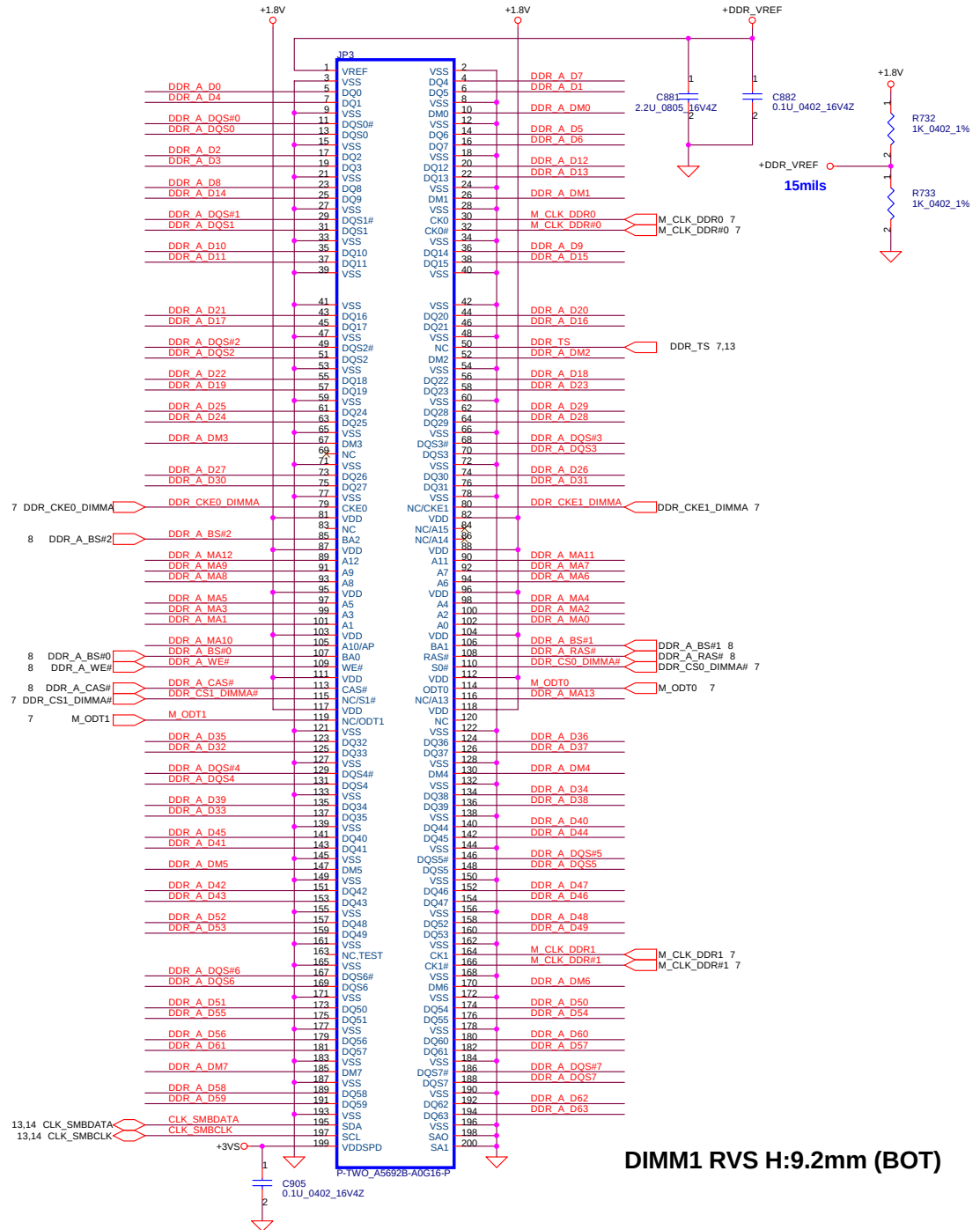
Layout Note:
Place near JP27

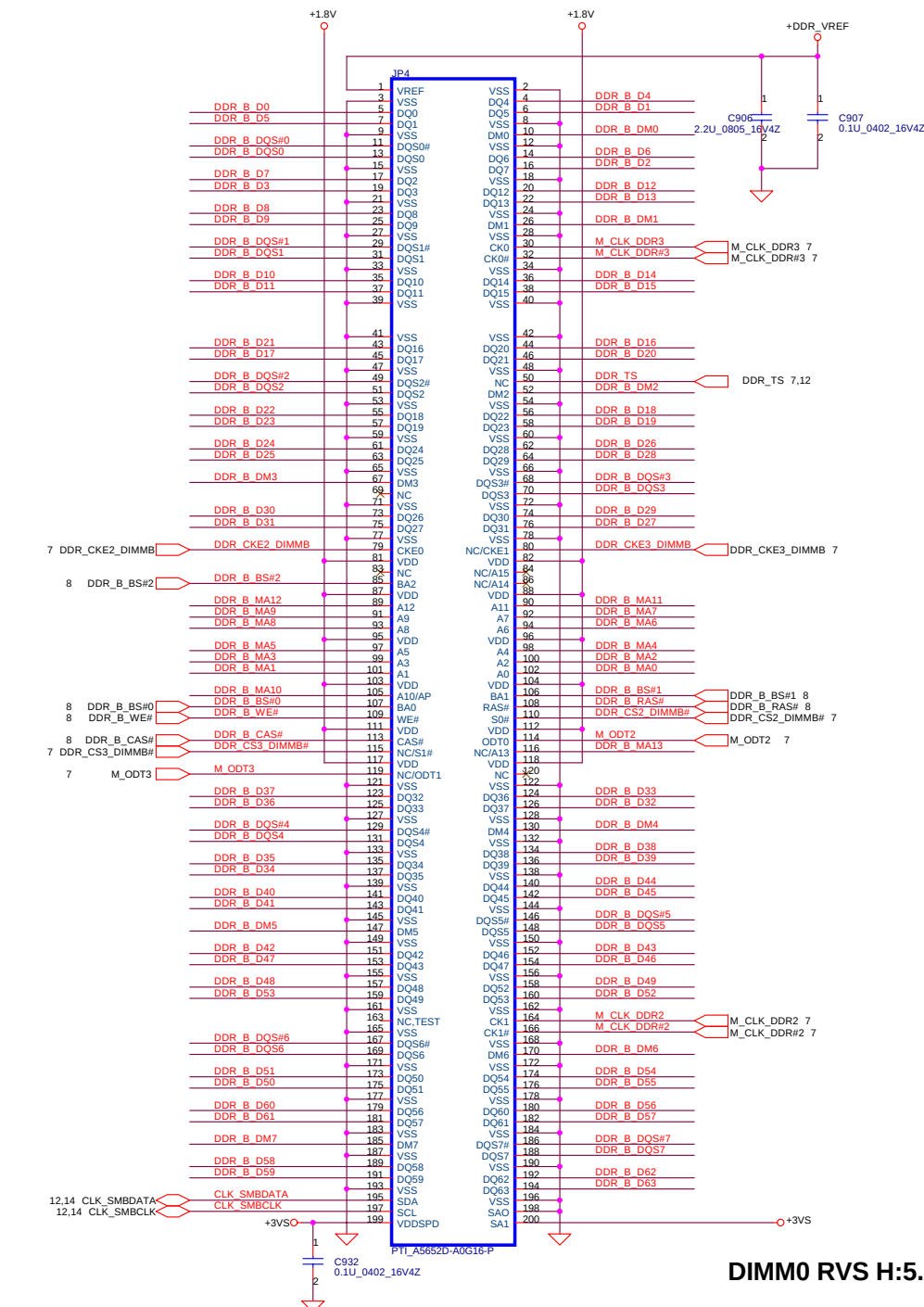
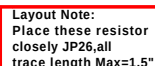
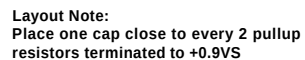
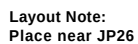


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



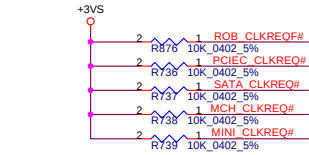
Layout Note:
Place these resistor closely JP27, all trace length Max=1.5"





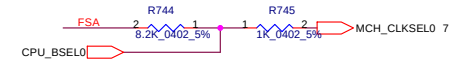
DIMM0 RVS H:5.2mm (BOT)

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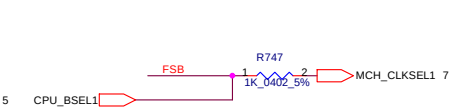


FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHZ	SRC MHZ	PCI MHZ
0	0	1	133	100	33.3
0	1	1	166	100	33.3

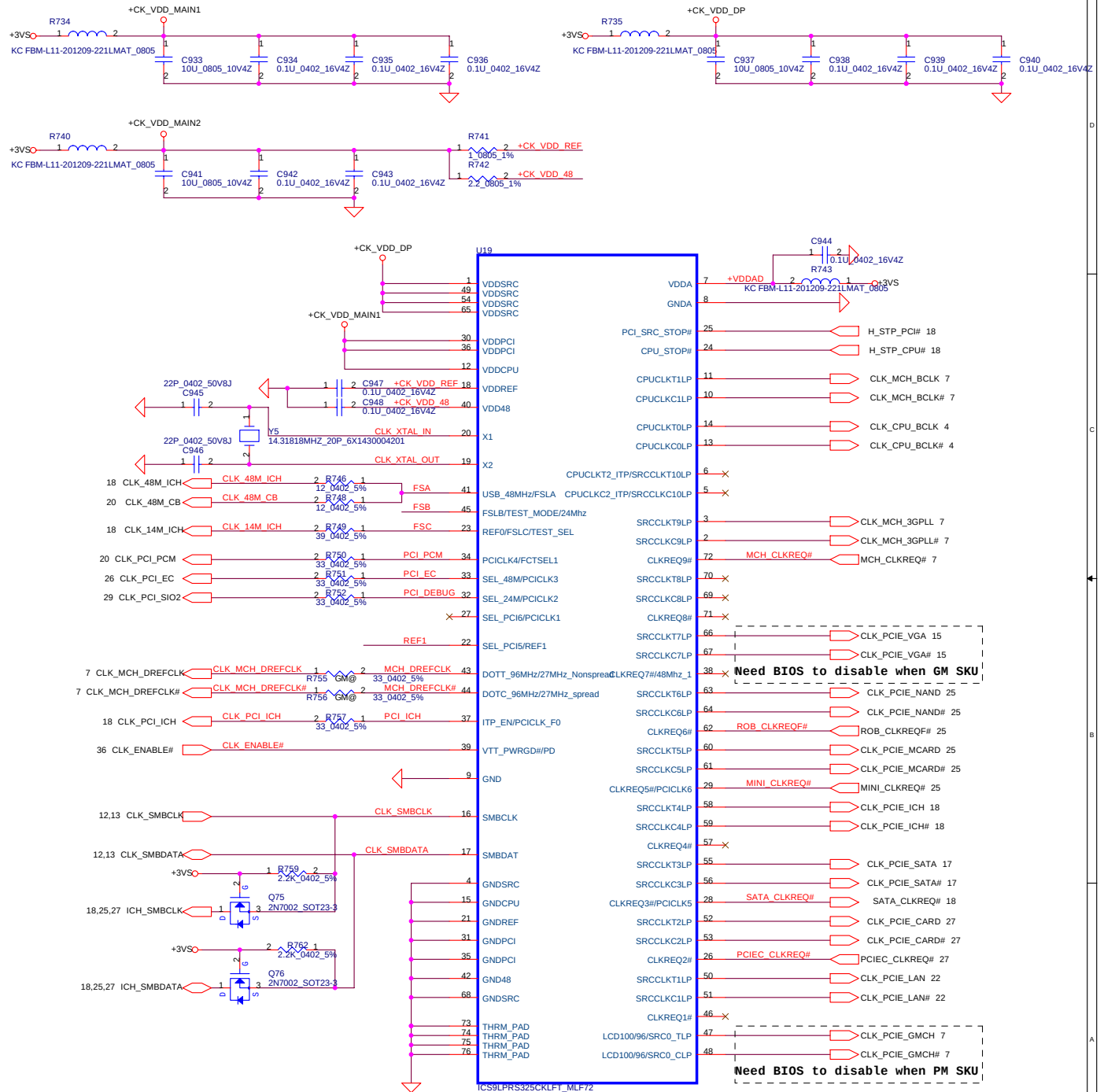
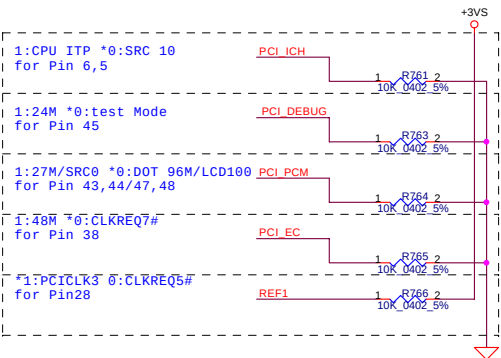
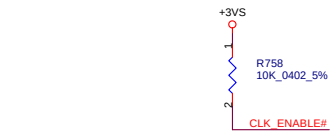
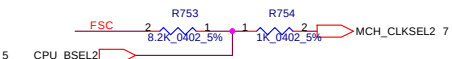
FSA



FSB

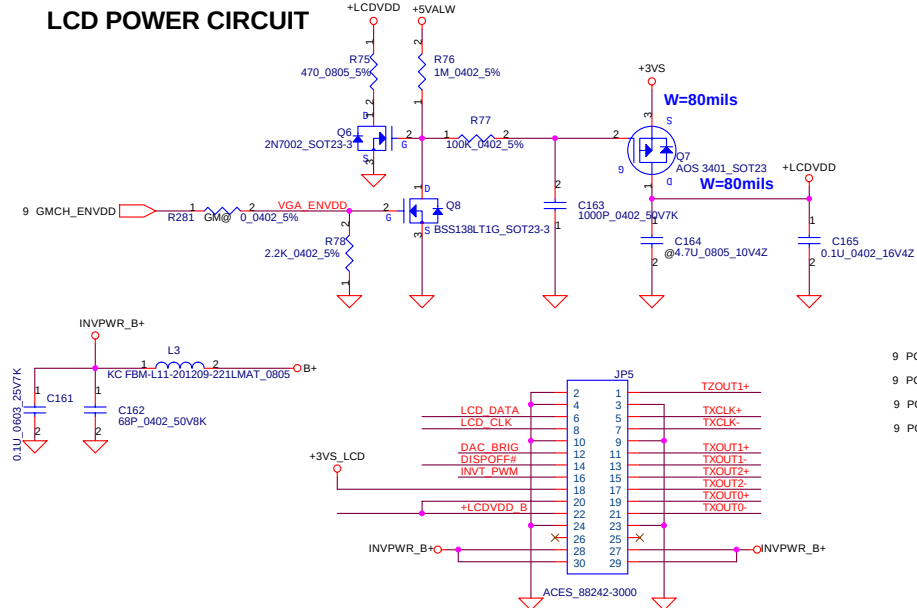


FSC (Fixed at low)

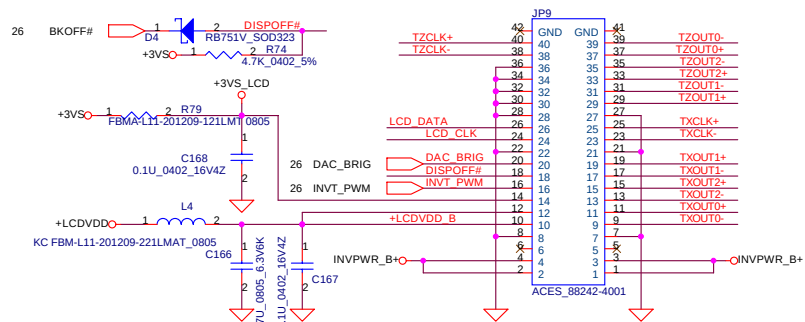


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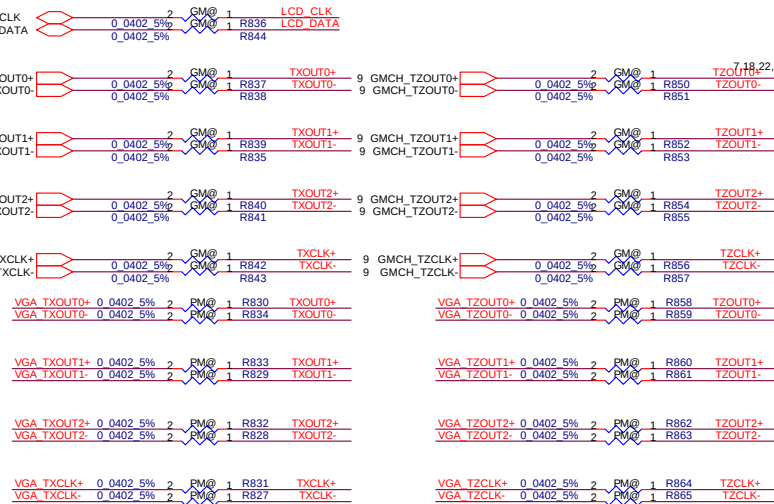
LCD POWER CIRCUIT



LCD/PANEL BD. Conn.



ALL R CLOSE LVDS CONNECTOR



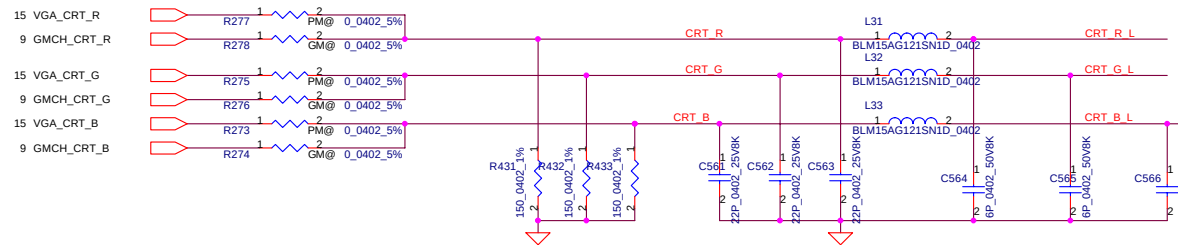
VGA BOARD Conn. VGA BOARD Conn.



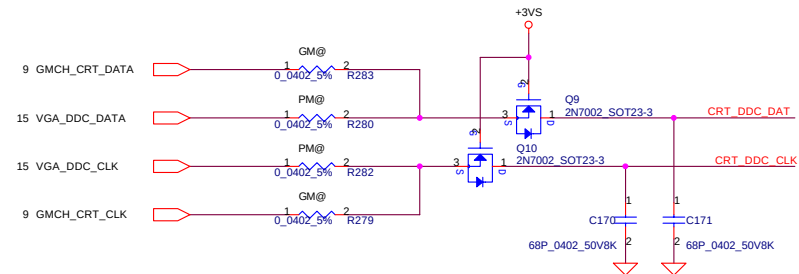
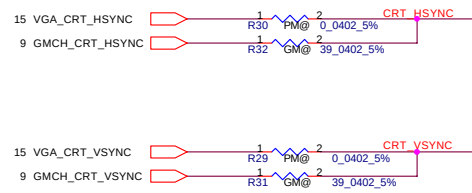
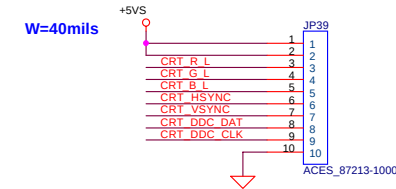
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							ISRAE M/B LA-3711P				1.0	
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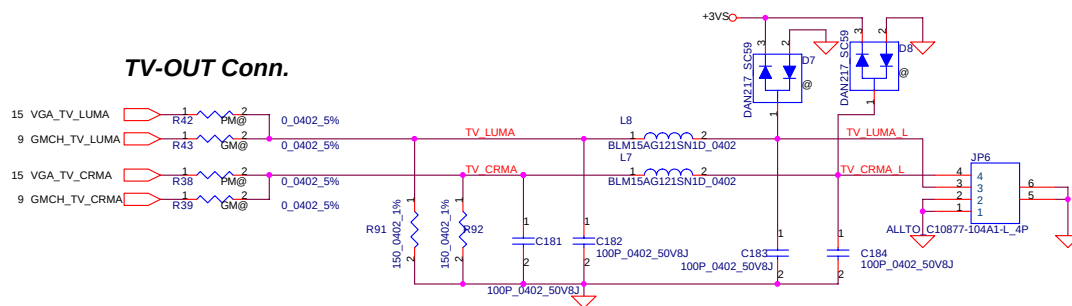
CRT CONNECTOR



CRT Conn.



TV-OUT Conn.



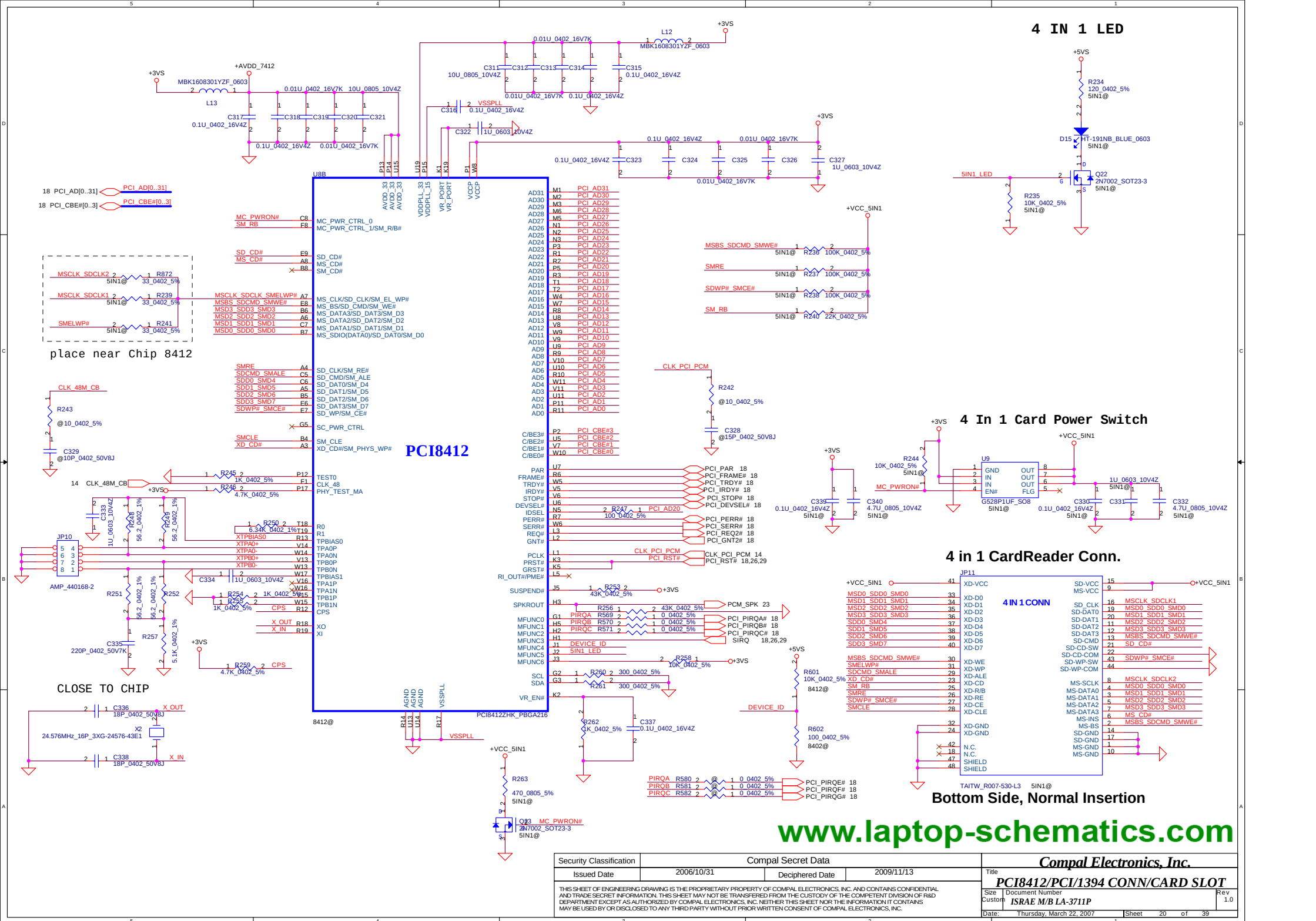
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Issued Date				2006/10/31				Deciphered Date			
				2009/11/13				Title			
								Display Interface Connector			
								Size			
								Document Number			
								ISRAE M/B LA-3711P			
								Rev			
								1.0			
								Date			
								Thursday, March 22, 2007			
								Sheet			
								16 of 39			

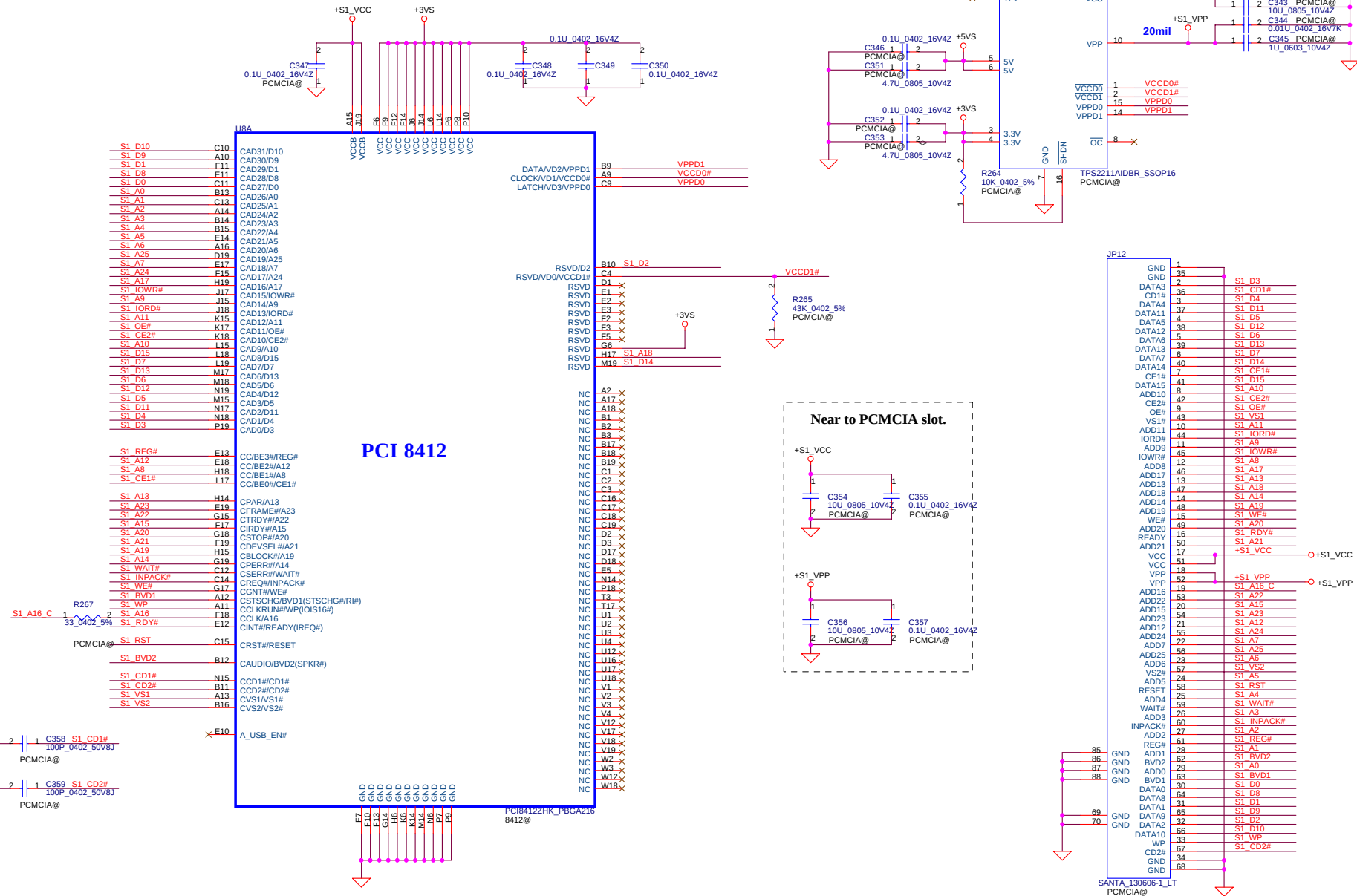
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				ISRAE M/B LA-3711P		1.0
Date:				Thursday, March 22, 2007	Sheet	18 of 39

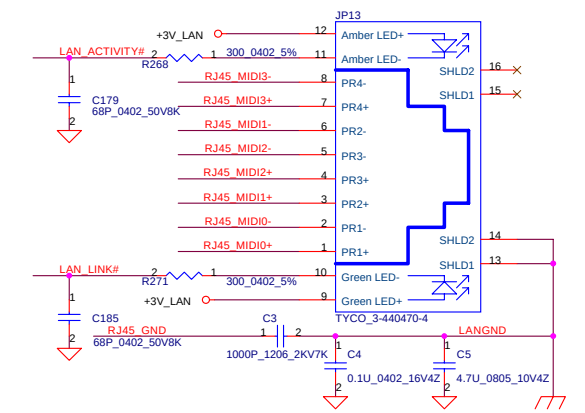
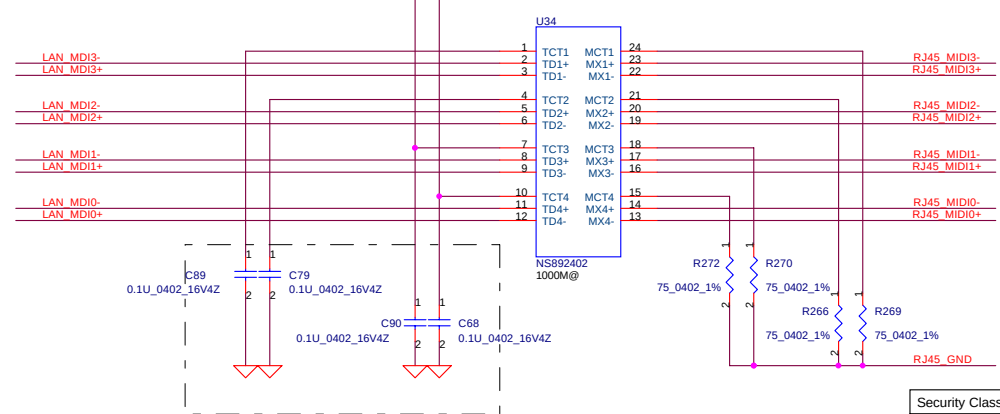
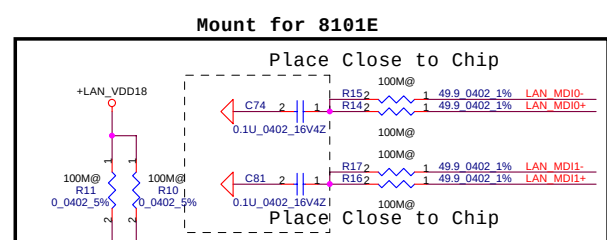
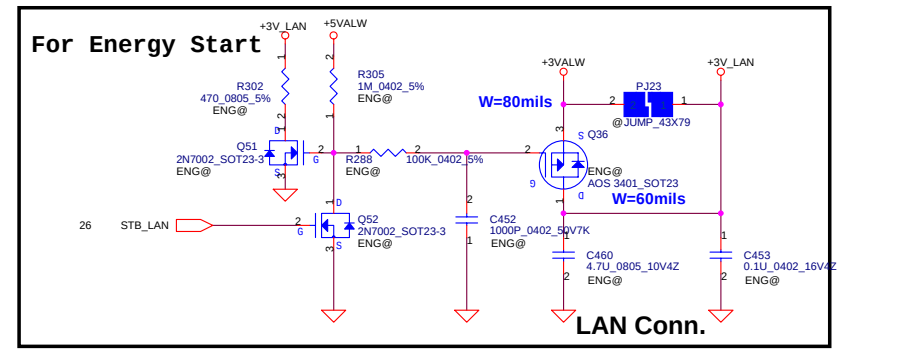
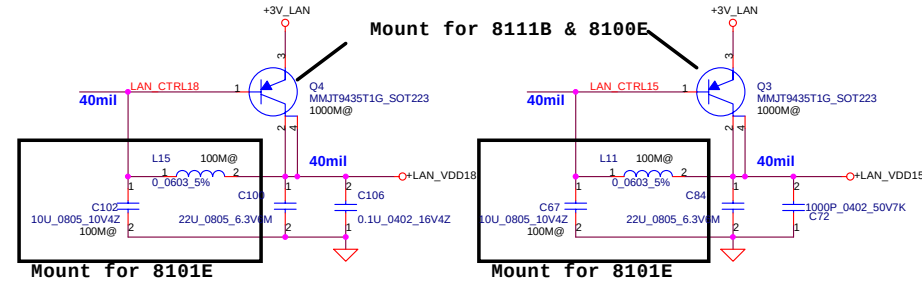
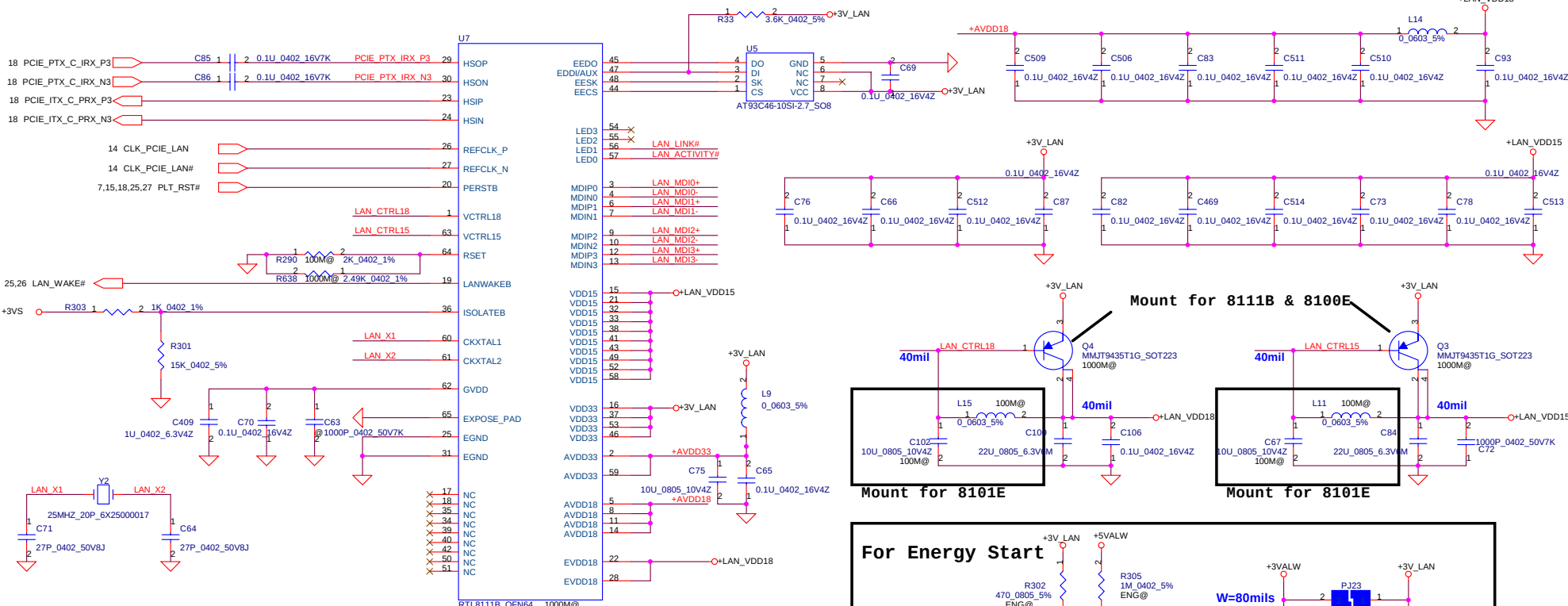


CardBus Power Switch



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Security Classification		Compal Secret Data		Compal Electronics, Inc. PCI7412/CB/CB SLOT	
Issued Date	2006/10/31	Deciphered Date	2009/11/13	Title	PCI7412/CB/CB SLOT ISRAE M/B LA-3711P
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				Date:	Thursday, March 22, 2007 Sheet 21 of 39



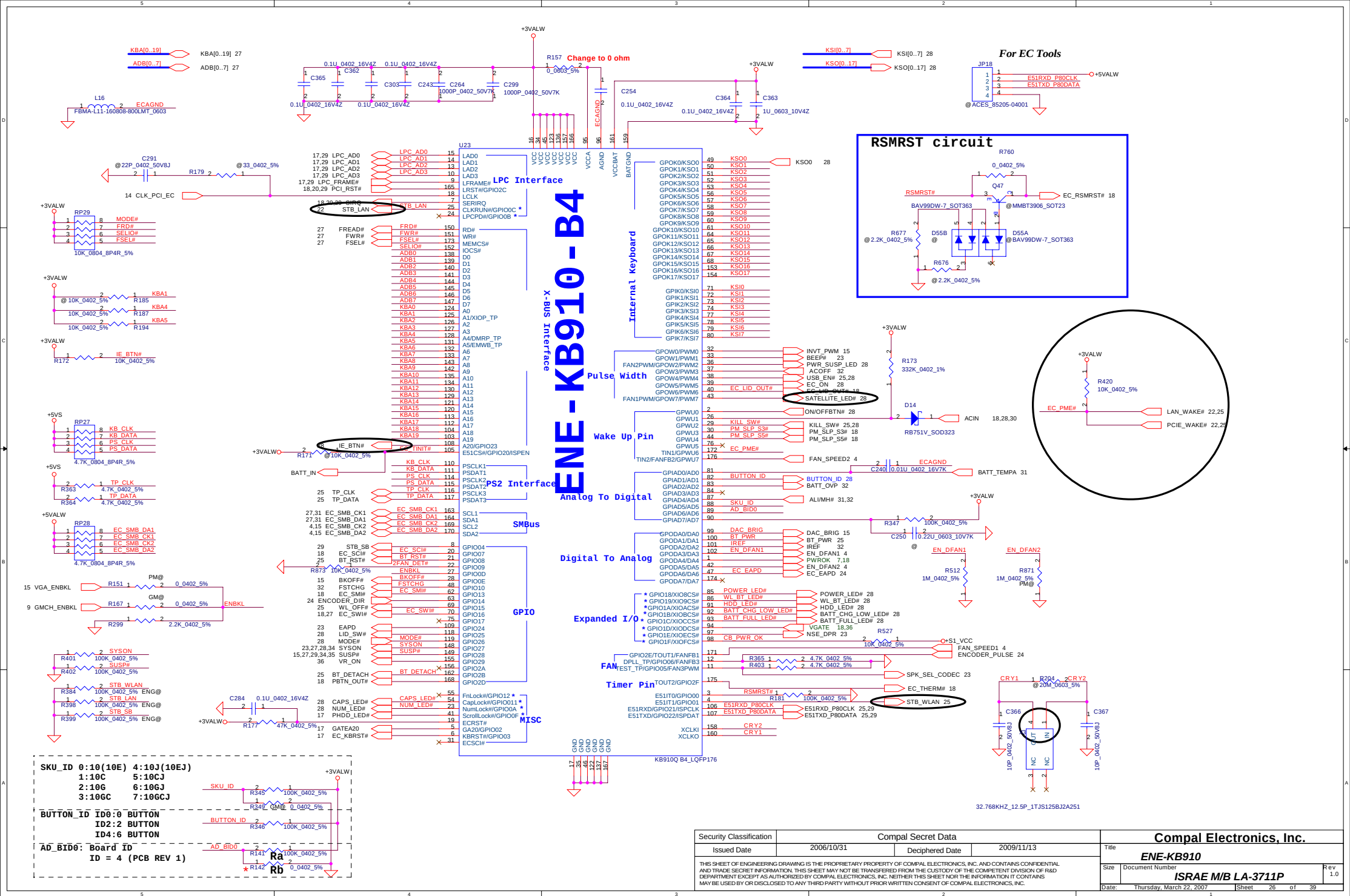
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Issued Date	2006/10/31	Deciphered Date	2009/11/13	RTL8100CL	
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				Custom	SRAE M/B LA-3711P
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+AVDD_HD +3VS_DVDD

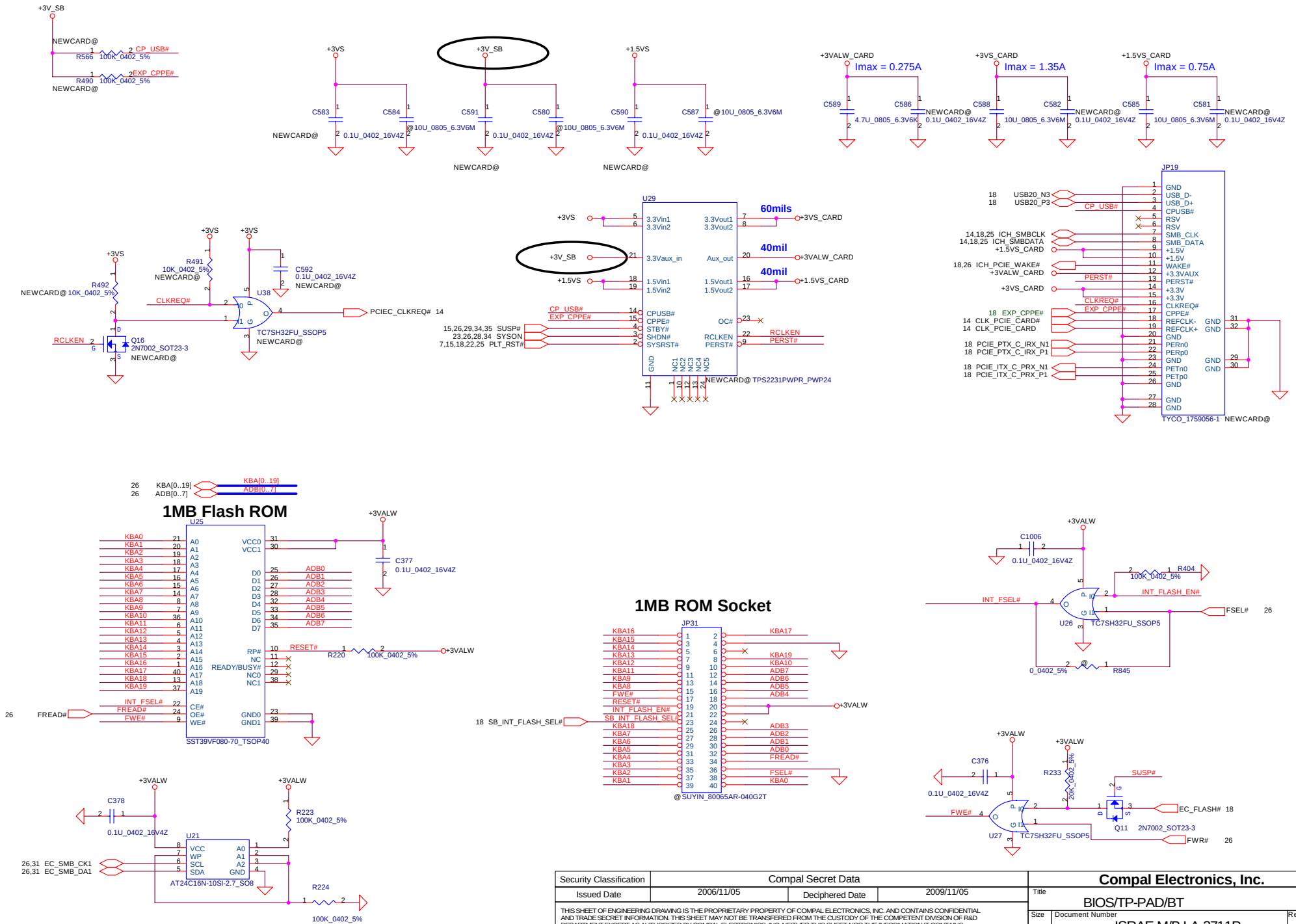


cs.com

Security Class
Issued Date
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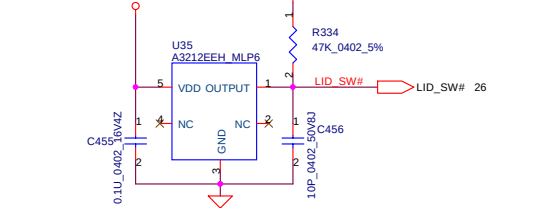


New Card

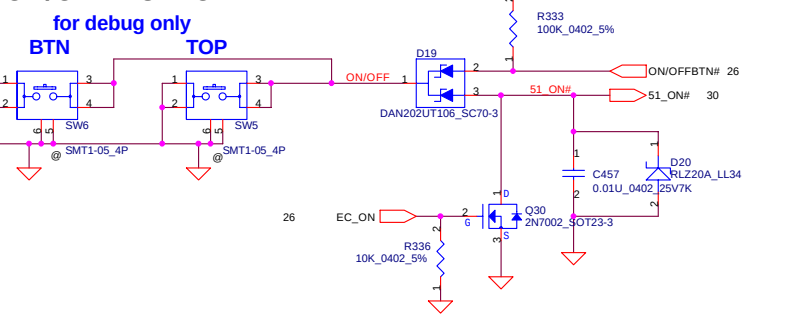


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Size		Document Number		Rev	
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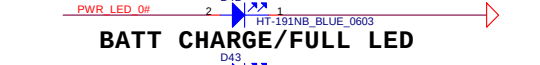
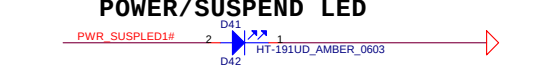
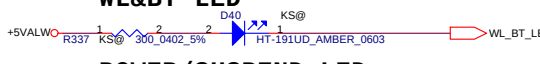
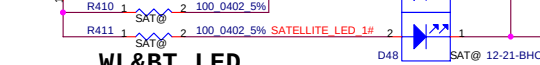
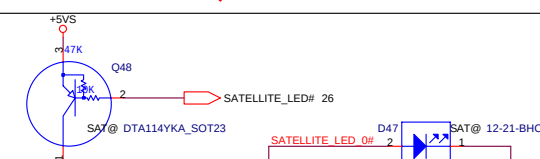
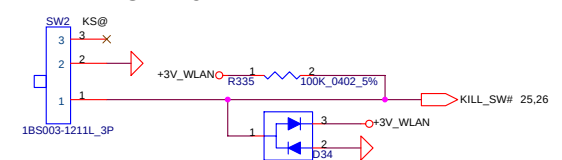
Lid SW



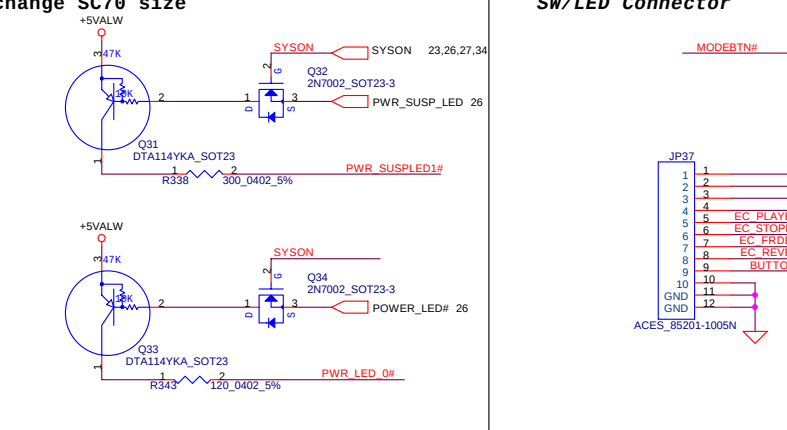
ON/OFF BUTTON



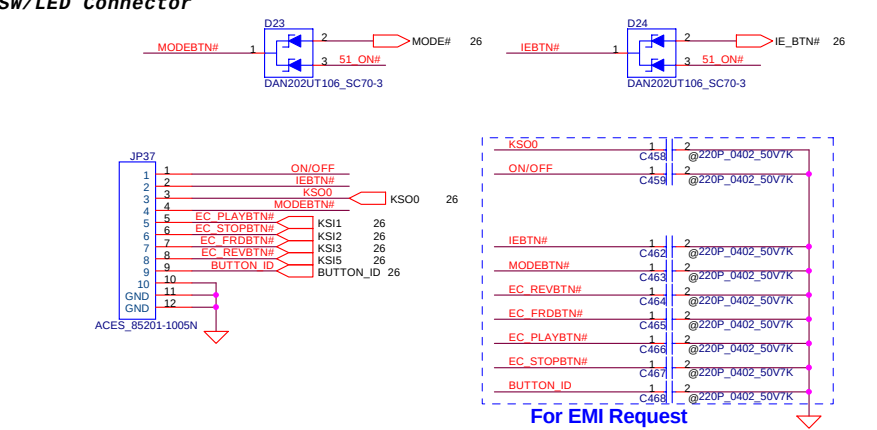
Kill SWITCH



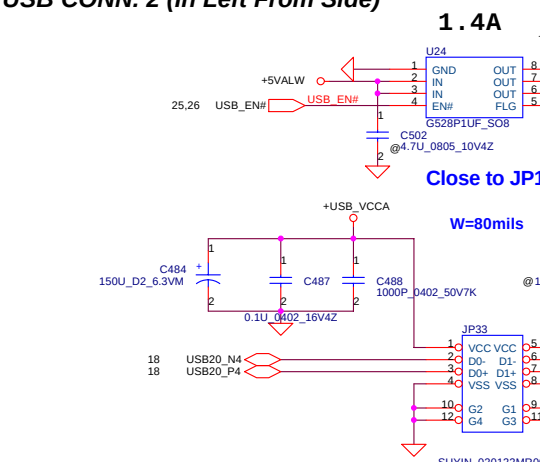
change SC70 size



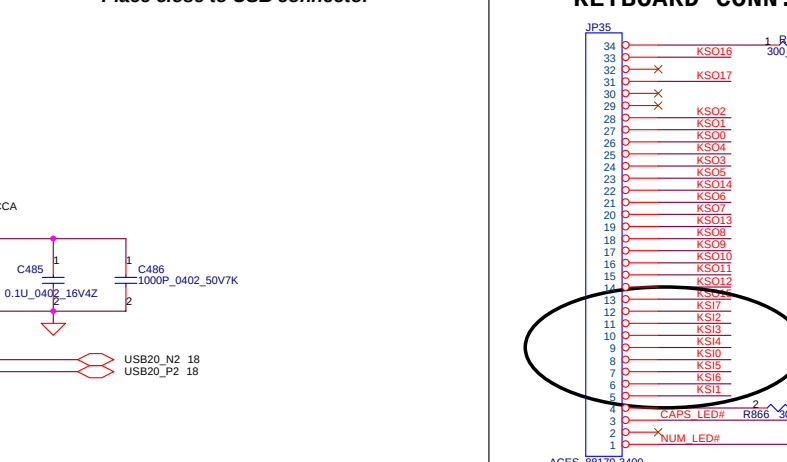
SW/LED Connector



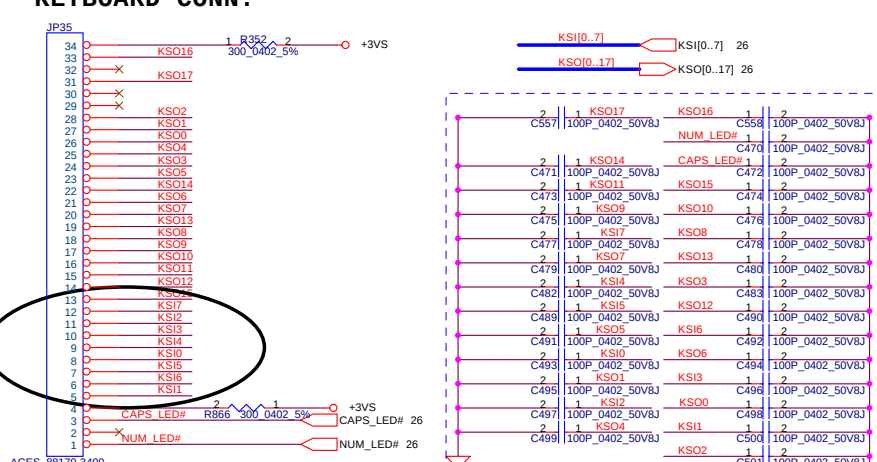
USB CONN. 2 (In Left From Side)



Place close to USB connector



KEYBOARD CONN.

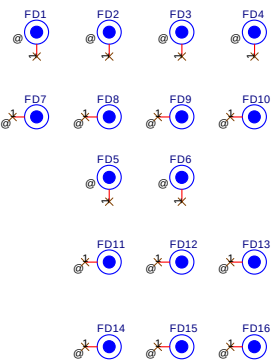
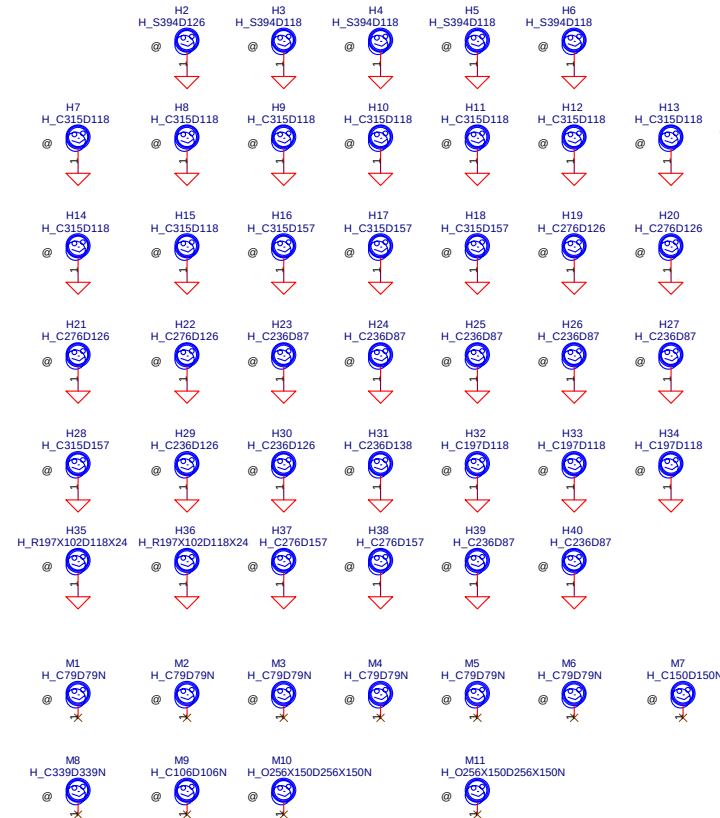
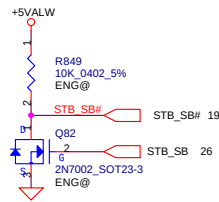
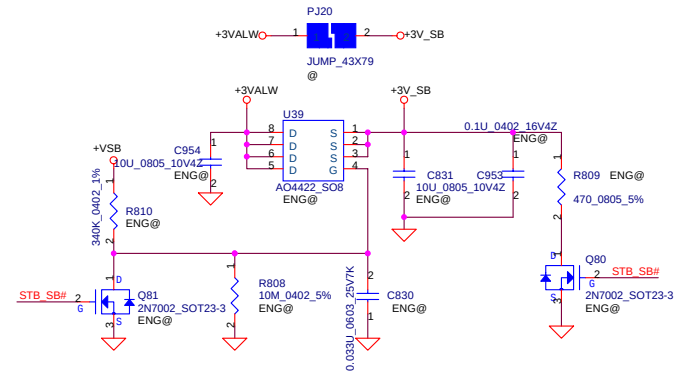
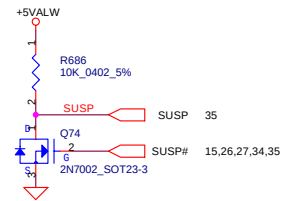


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The diagram illustrates the Under DDR ME Assignment Area. It features a central component with pins D_PAD1, D_PAD0, and @DEBUG_PAD. The following signals are connected to these pins:

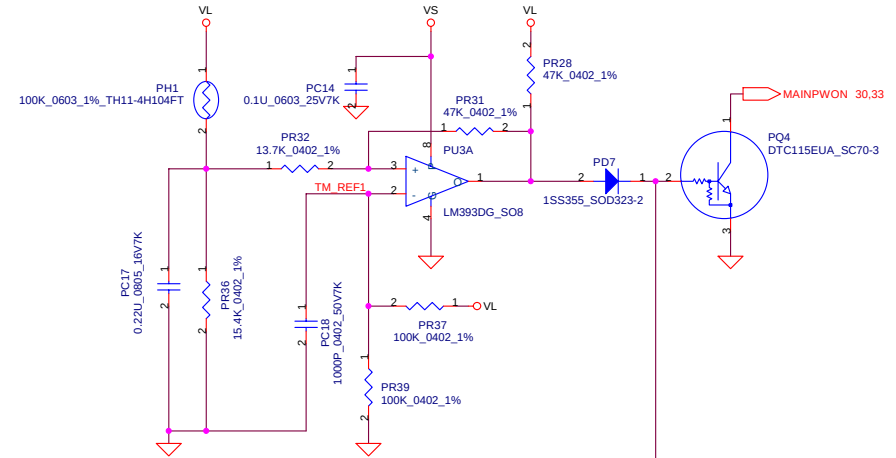
- D_PAD1** (Pin 6): Connected to E51RXD_P80CLK (18,20,26 SIRQ) via resistor R392 (0_0402_5%).
- D_PAD1** (Pin 7): Connected to SIRO (18,20,26 SIRQ) via resistor R394 (0_0402_5%).
- D_PAD1** (Pin 8): Connected to LPC_AD3 (17,26 LPC_AD3).
- D_PAD1** (Pin 9): Connected to LPC_AD1 (17,26 LPC_AD1).
- D_PAD1** (Pin 10): Connected to LPC_FRAME# (17,26 LPC_FRAME#).
- D_PAD0** (Pin 5): Connected to E51TXD_P80DATA (25,26) via resistor R391 (0_0402_5%).
- D_PAD0** (Pin 4): Connected to LPC_DRQ#1 (17) via resistor R393 (0_0402_5%).
- D_PAD0** (Pin 3): Connected to PCI_RST# (18,20,26) via resistor R393 (0_0402_5%).
- D_PAD0** (Pin 2): Connected to LPC_AD2 (17,26) via resistor R393 (0_0402_5%).
- D_PAD0** (Pin 1): Connected to LPC_AD0 (17,26) via resistor R393 (0_0402_5%).
- @DEBUG_PAD** (Pin 0): Connected to CLK_PCI_SIO2 (14) via resistor R395 (10_0402_5%) and capacitor C544 (10P_0402_50V8J).

Keep Resistor near Debug Pad and in the same side
Reverse side DIMM ---- Pin 1 keep away DIMM

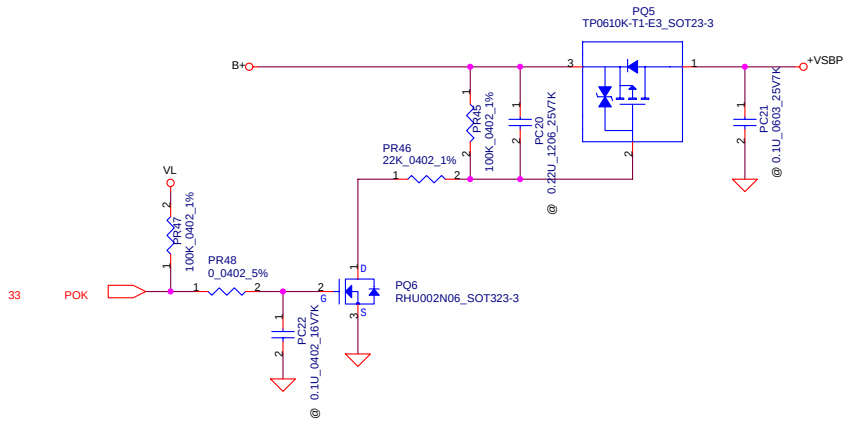
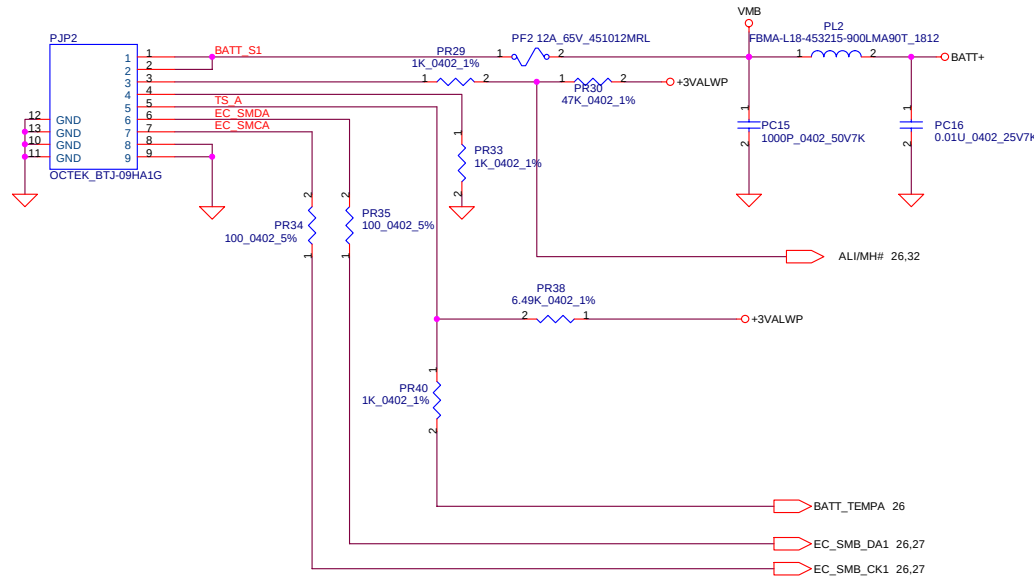
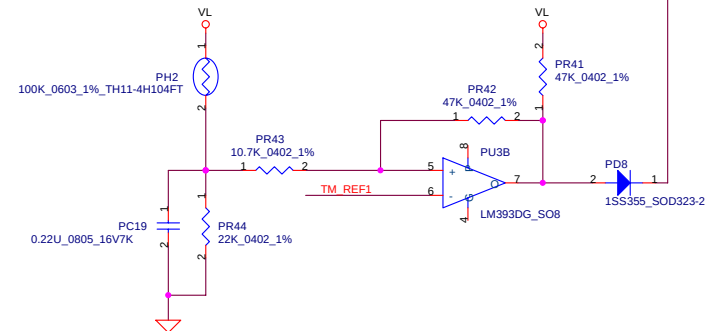
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						Size	Document Number				Rev 1.0
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PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C

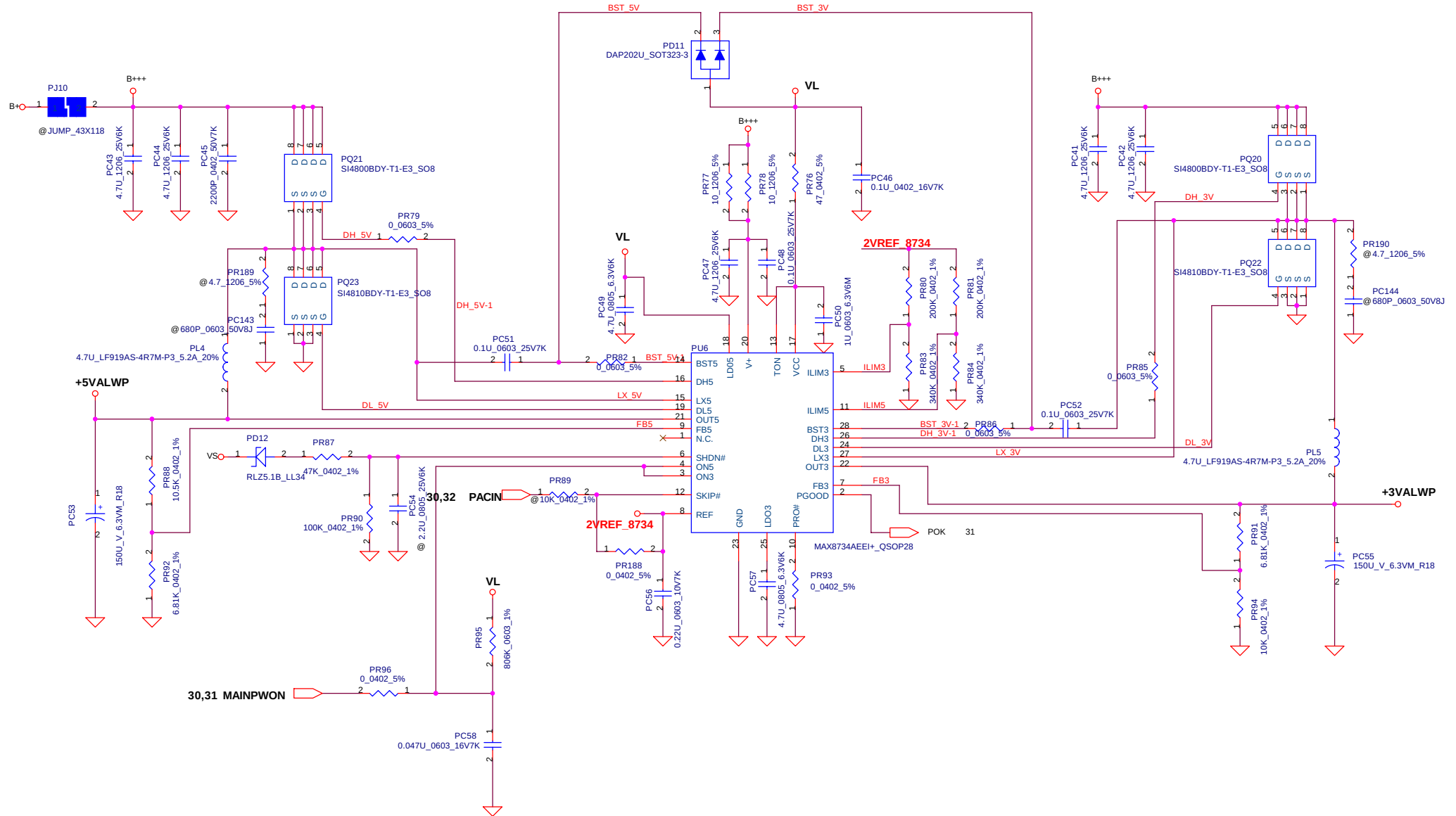


PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 45 degree C



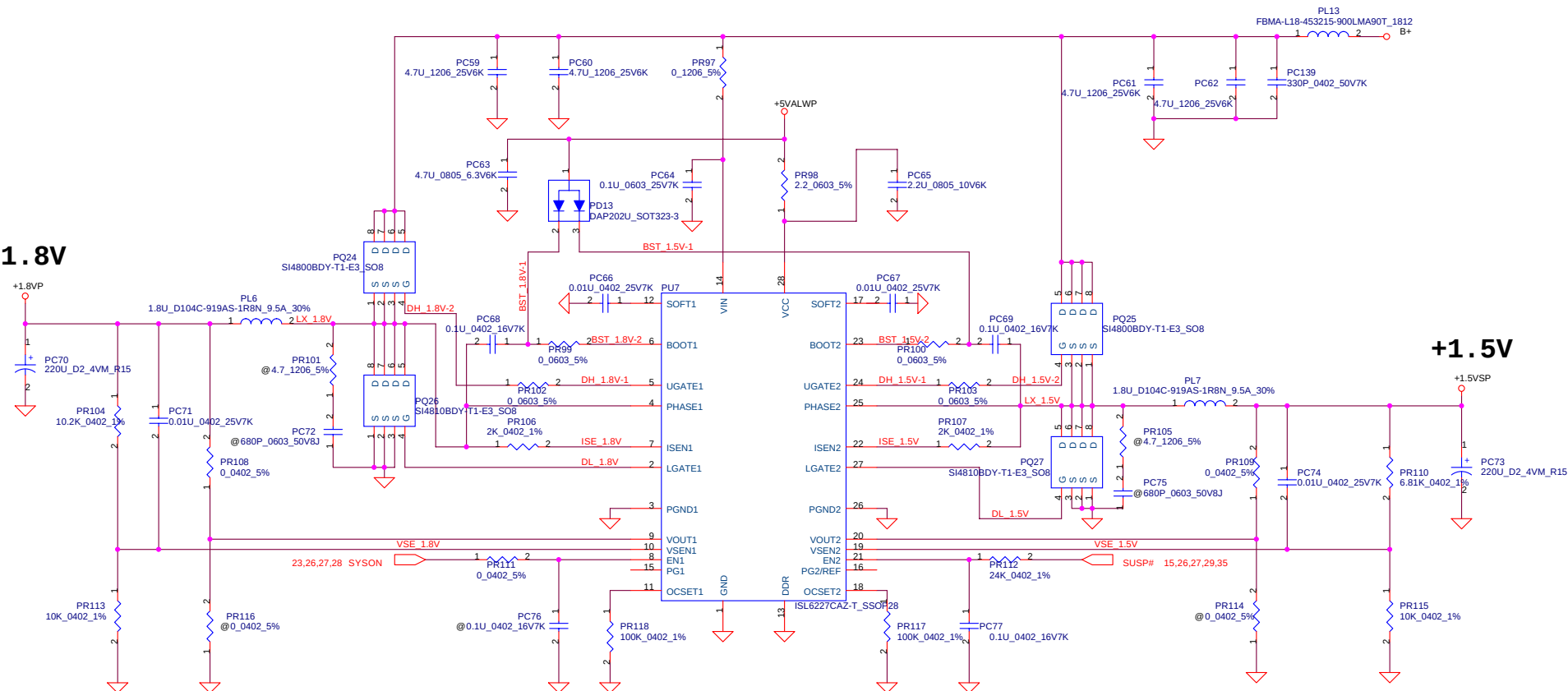
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				1.0	
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+3.3VALWP/+5VALWP



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				+5V/+3V	
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				IAKAA M/BLA-3401P	
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+1.8V



+1.5V

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Size		Document Number			Rev
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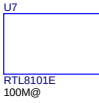
HW4 Product Improvement Record (P.I.R.)

Phase: B to C		Date: 2007/01/24			Writer: Timo Teng		
Page#	Action Plan (add; del; change)	Location or Net_List	Before value (Attached file)	After value (Attached file)	Detail Discretion and Root Cause	Rev.	DL/DM Check
P17	Change Connector	JP24	SUYIN_06802-TK102	SUYIN_127043FB 022G345ZR_NR	Change layout footprint	0.2	
P18	Delete Component	R873 R874	100K_0402_5%	NC	All sku keep 5 in 1 and 1394 functions		
P22	Delete Component	R820	10K_0402_5%	NC	No need more than one pull-high resistor on the net		
P25	Delete Component	R195	10K_0402_5%	NC	No need more than one pull-high resistor on the net		
P26	Delete Component	Q65/Q77 R821/R822	MMBT3904/10K_0402_5%	NC	No engine start, so follow Dallas project.		
P20	Change net	R234	Connects to +3VS	Connects to +5VS	Blue LED needs to connect 5V		
P24	Modify footprint	JP14/JP15	SINGA_2SJ-S351	SINGA_2SJ-T820	For solving SMT soldering poor issue		
P25	Delete Component	U38/R503/C630	CIR/100_0805/4.7U	NC	No CIR support on spec.		
P26	Add Component	R873/2FAN_DET#	NC	10K_0402/2FAN_DET#	For separate ISRAE&ISKAE EC BIOS		
P28	Modify component	R410/R411	200_0402_5%	100_0402_5%	Emonoto-san request, the LEDs increase brigtness		
P28	Modify BOM Select	Q48/R410/R411/D47/D48	NC	SAT@	Reserve Satelliate LED BOM select		
P29	Modify R Value	R613	820K_0402_1%	910K_0402_5%	For delaying and adjusting 1.8VS power sequence		
P22	Change Value	C89, C79, C90 C68, C74, C81	0.01uF_0402	0.1uF_0402	For solving EMI noise		
Phase: C to PreMP		Date: 2007/02/02			Writer: Timo Teng		
Page#	Action Plan (add; del; change)	Location or Net_List	Before value (Attached file)	After value (Attached file)	Detail Discretion and Root Cause		
P18	Add Component	R874/R875	NC	@1K_0402/@100K_0402	Reserve Satellite LDE detected	1.0	
P27	Modify component	C584/C580/C587	10uF_0805_6.3V	@10uF_0805_6.3V	For Cost reduce (PVT cut-in)		
P11	Modify component	C716	330uF_D2E_2.5V	@330uF_D2E_2.5V	For Cost reduce (PVT cut-in)		
P23	Modify component	C425	4.7uF_0805_10V	@4.7uF_0805_10V	For Cost reduce (PVT cut-in)		

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LAN



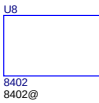
TRANSFORMER



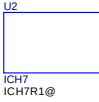
PCB



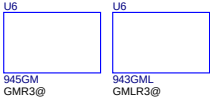
Card BUS



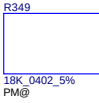
SB



NB



SKU ID



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POWER PIR LIST

page Reason for change Modify list

DVT

35	Change +1.05V PWM IC	Change PU8 to ISL6269A(SA00000GU80), add PR122 (0ohm, SD013000080)
36	For EMI team request to add snubber and gate resistor Modify the CUP CORE load line and compensation	Add snuber PR155,PR165(6.8ohm_SD011680880), PC109,PC118(680p_SE024681J80) and gate resistor PR154,PR162(1ohm_SD013100B80) Change PC103 to 0.022u(SE076223K80), PC104 to 2.2u(SE107225K80), PR185 to 4.42K(SD000004J80), PC129 to 0.1u(SE076104K80, add PC126 (0.018U_SE025183J80), delete PC105 and PC106
31	Modify the CPU OTP point from 84 degC to 87 degC for thermal team request	Change PR36 from 22K to 20K(SD034200280)

PVT

32,34, 35,36	For EMI team request to add bead to reduce board band	Add PL12,PL13,PL14(SM010020720);PC137,PC138,PC139(330p_SE074331K80);PC140(680p_SE074681K80);PC141(3300p_SE074332K80)
33	Reduce the power consumption on S3/S4	Add PR188(0_0402_5%) and unpop PR89
36	Solve the high frequency noise.	Change PC99 from 100U to 220U(SF22004M210)

Pre-MP

36	For EMI solution	Add PC142 (0.01u_0402)
36	PC99 was interfere with logic low so change to small size	Change PC99 from 220U to 100U and add PC143,PC144(68U_25V).

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