

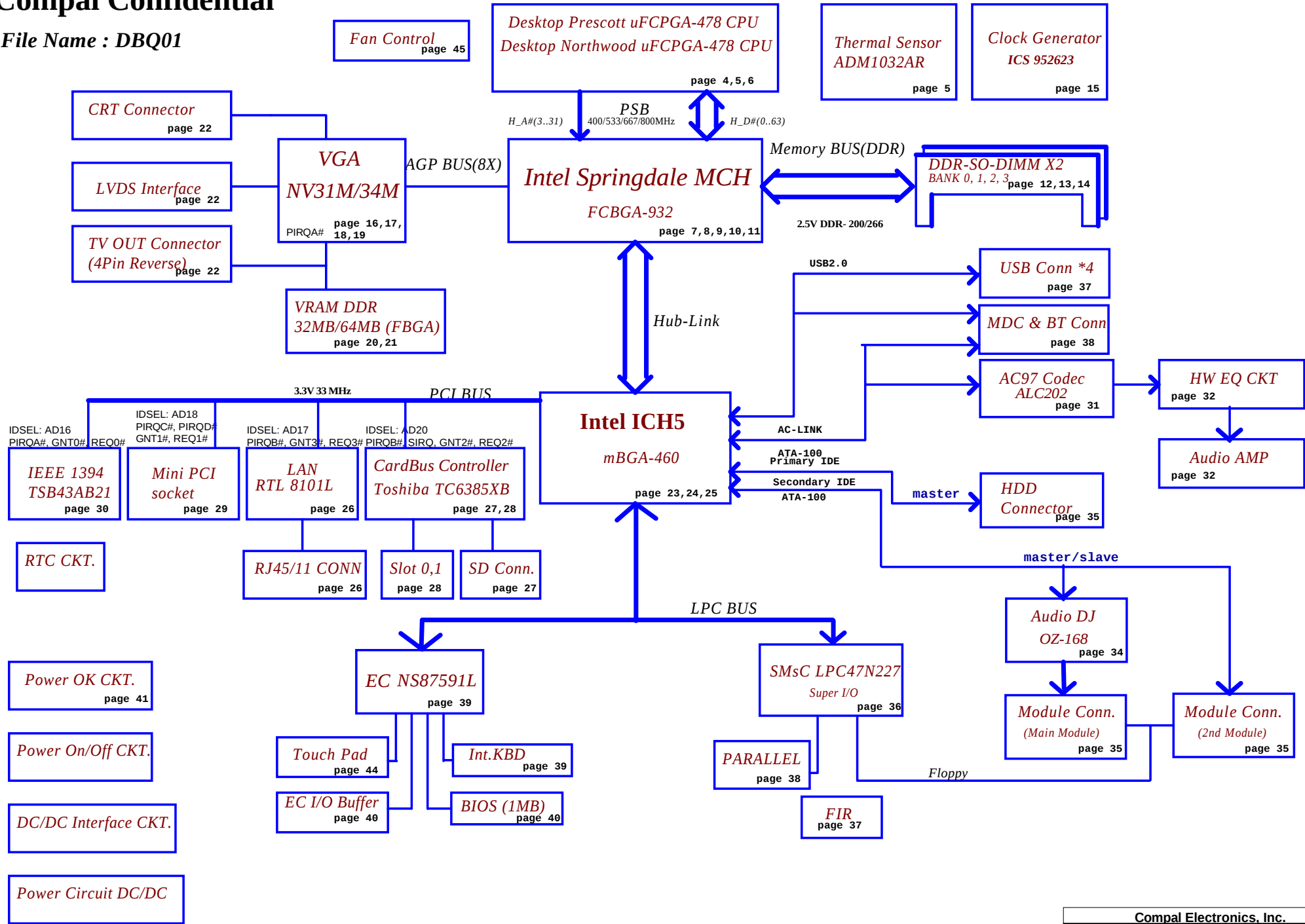
DBQ01 Rev0.1 Schematics Document

Intel Prescott uFCPGA-478 / P4 Northwood

with Springdale / ICH5 / nVIDIA NV34M/31M chipset

2003/07/01

Compal Electronics, Inc.			
Title			
Cover Sheet			
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_VID	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+VTT_GMCH	+1.225V (Prescott) / +1.45V (Northwood)	ON	OFF	OFF
+VGA_CORE	1.3V switched power rail for VGA chip	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	AGP 4X/8X	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
VGA			PIRQA
CardBus	AD20	2	PIRQA/PIRQB
LAN	AD17	3	PIRQB
Mini-PCI	AD18	1/4	PIRQC/PIRQD
1394	AD16	0	PIRQA
SD	AD22		

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02)	1010 000X b	OZ168	0011 0100 b
(24C04)	1011 000Xb		

EC SM Bus2 address

ICH5 SM Bus address

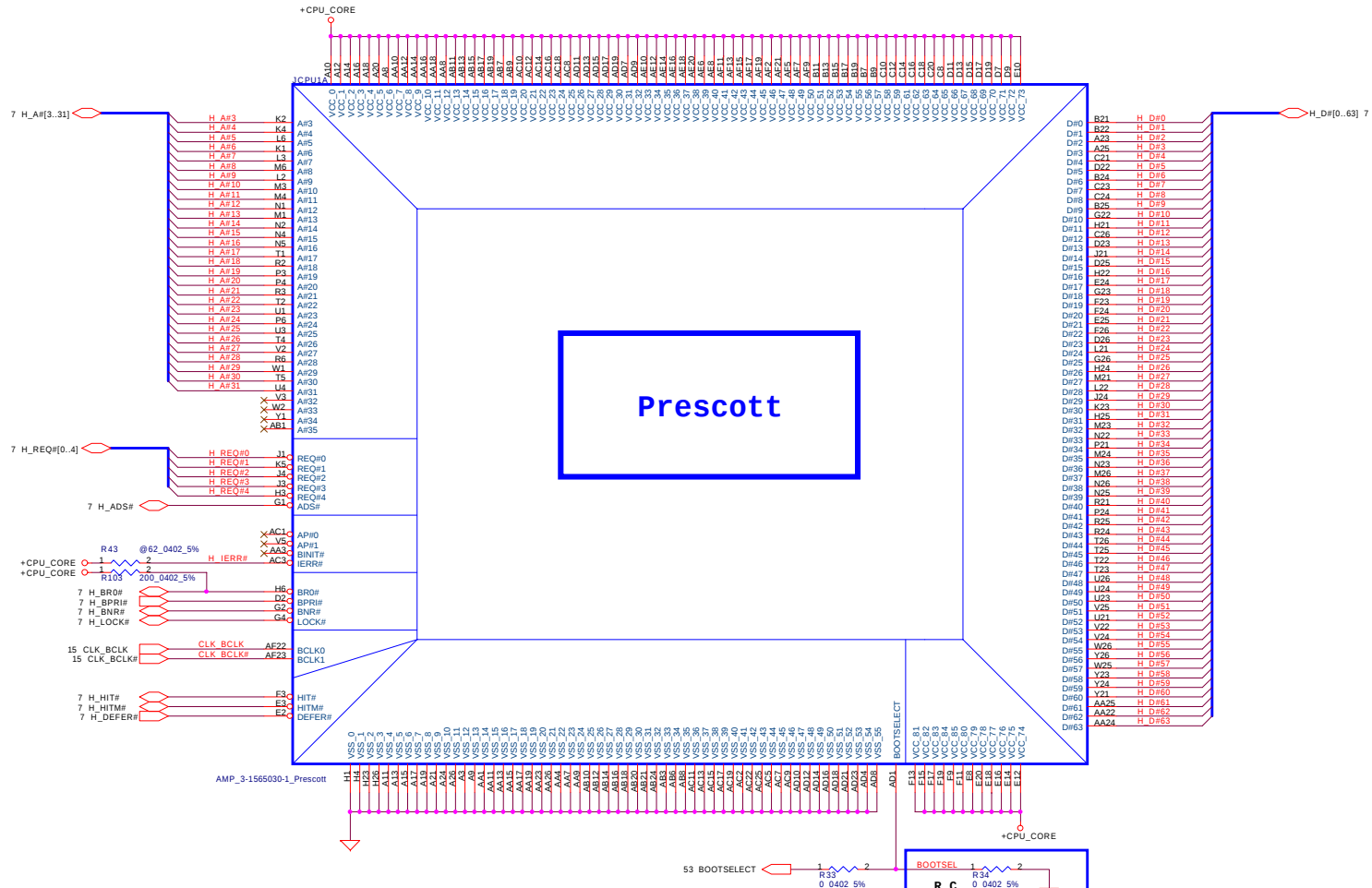
Device	Address
Clock Generator (ICS 952623)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 001Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

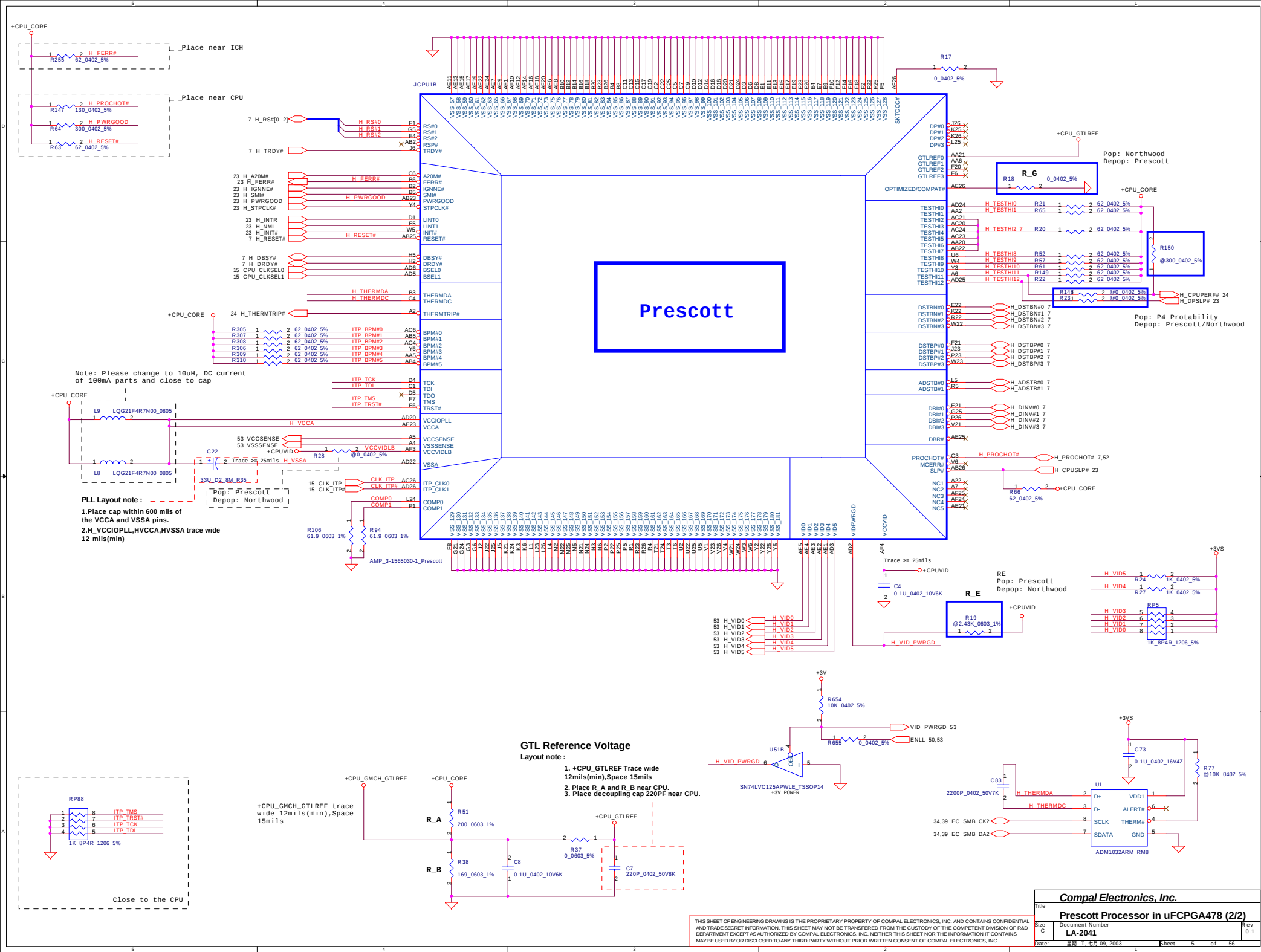
Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

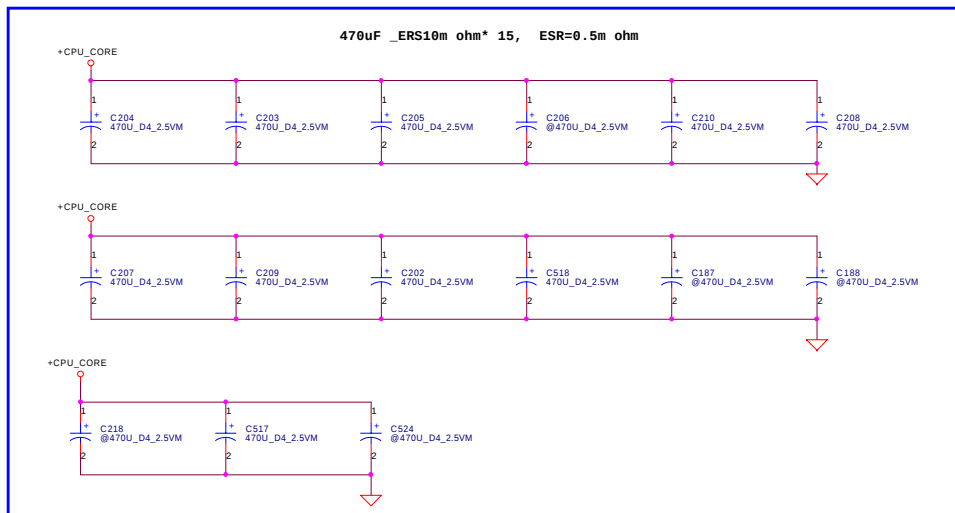
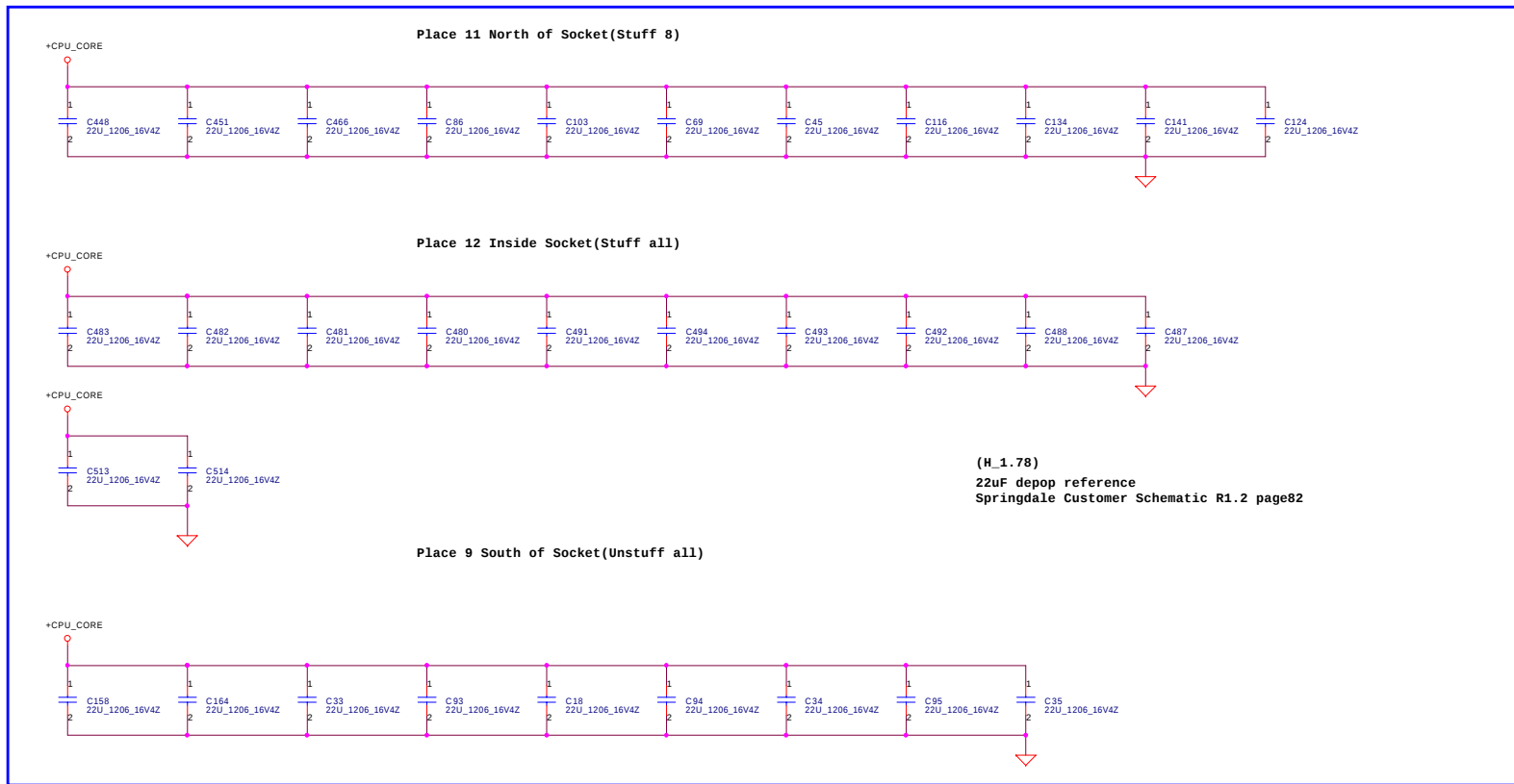
Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	



Reference Intel document Desktop P4 Spec.: 10988 P4 0.13u 512KB L2 EMTS Rev.2.0 Desktop Prescott Spec.: 11910 Prescott EMTS Rev.0.5						
Pin number	Northwood Pin name	Comment	Prescott Pin name	Comment	Northwood	Prescott
B6	FERR#	Pull-up 62ohm to +VCC_CORE	FERR#/PBE#	Pull-up 62ohm to +VCC_CORE	Pop	Pop
AA20	ITPCLKOUT0	Pull-up 62ohm to +VCC_CORE	TESTHI6	Pull-up 62ohm to +VCC_CORE	Pop	Pop
AB22	ITPCLKOUT1	Pull-up 62ohm to +VCC_CORE	TESTHI7	Pull-up 62ohm to +VCC_CORE	Pop	Pop
AD2	NC	float	VIDPWRGD	Pull-up 8.2Kohm to +VCCVID	Depop	Pop
AD3	NC	float	VID5	Pull-up 1Kohm to +3VRUN & connect to PWRIC	Depop	Pop
AF3	NC	float	VCCVIDLB	Connect to +VCCVID	Depop	Pop
AD20	VCCA	Connect to CPU Filter	VCCIOPLL	Connect to CPU Filter		
AF23	VCCIOPLL	Connect to CPU Filter	VCCA	Connect to CPU Filter		
AD1	VSS	Connect to GND	BOOTSELECT	CPU determine	Pop	Depop
AE26	VSS	Connect to GND	OPTIMIZED/ COMPAT#	float	Pop	Depop

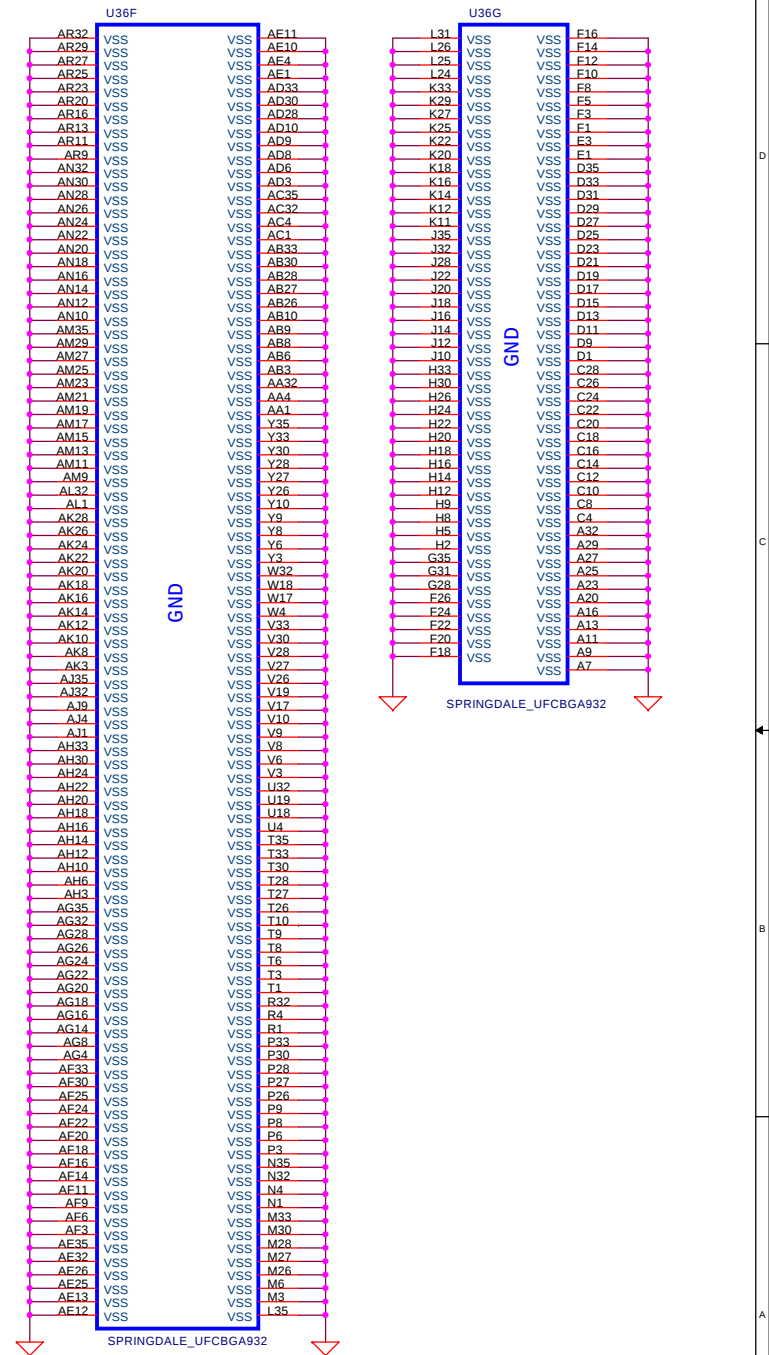
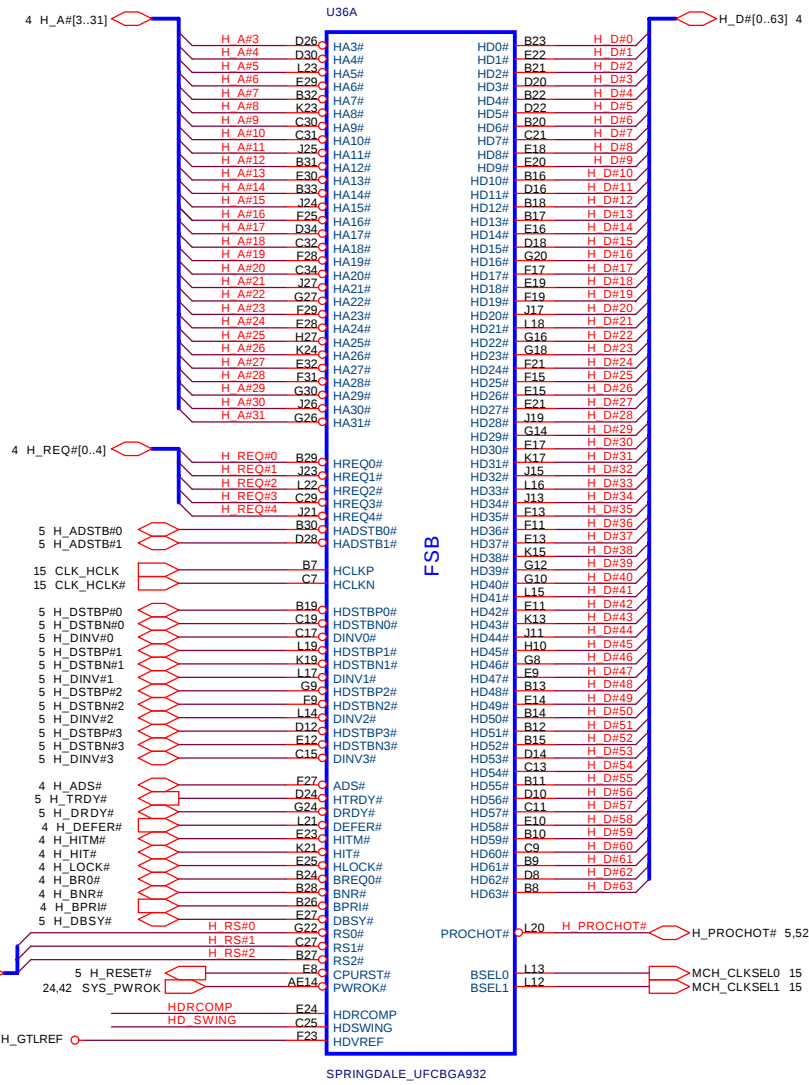
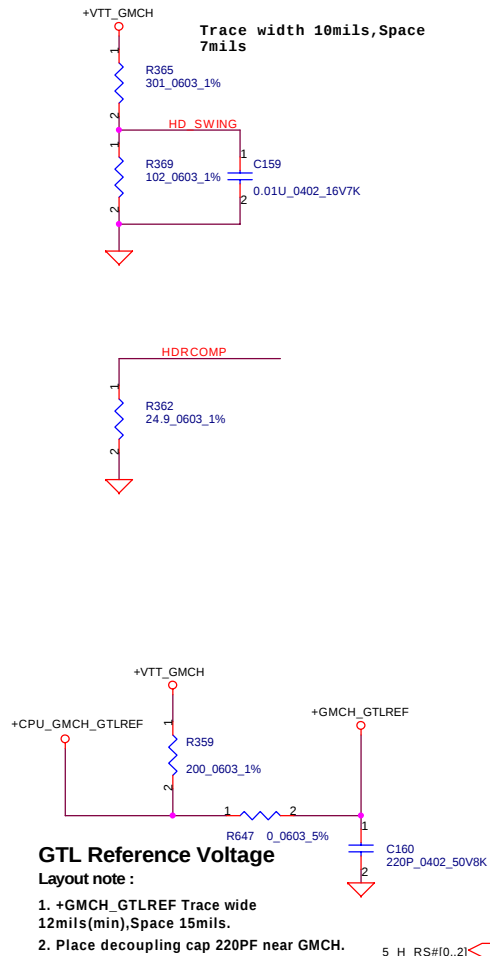
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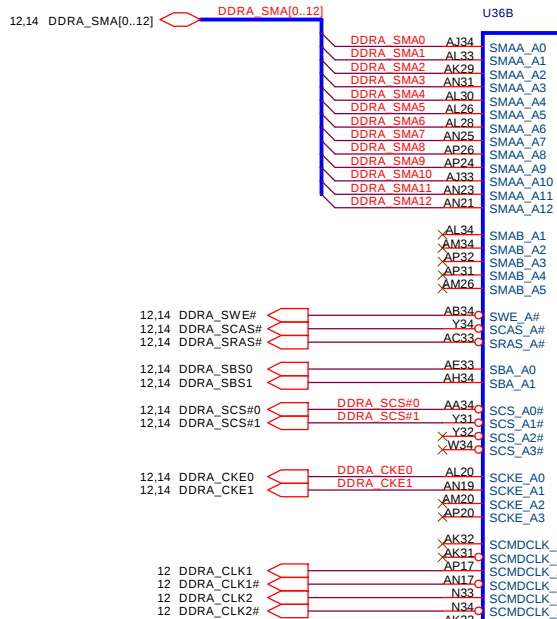




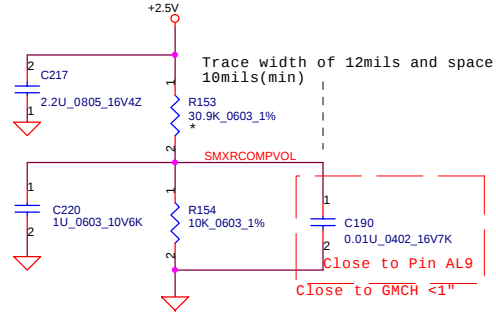
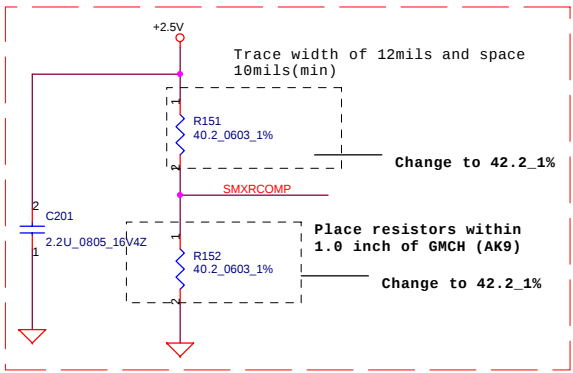
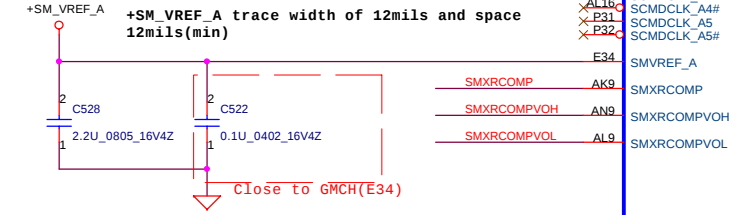
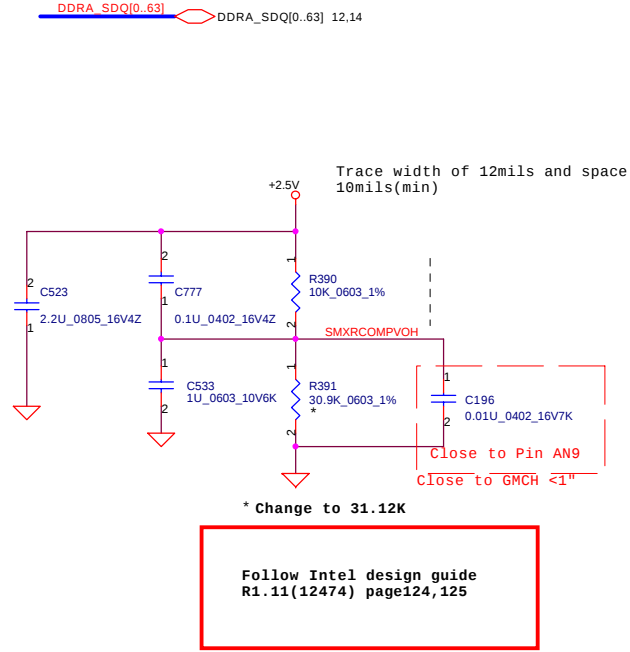
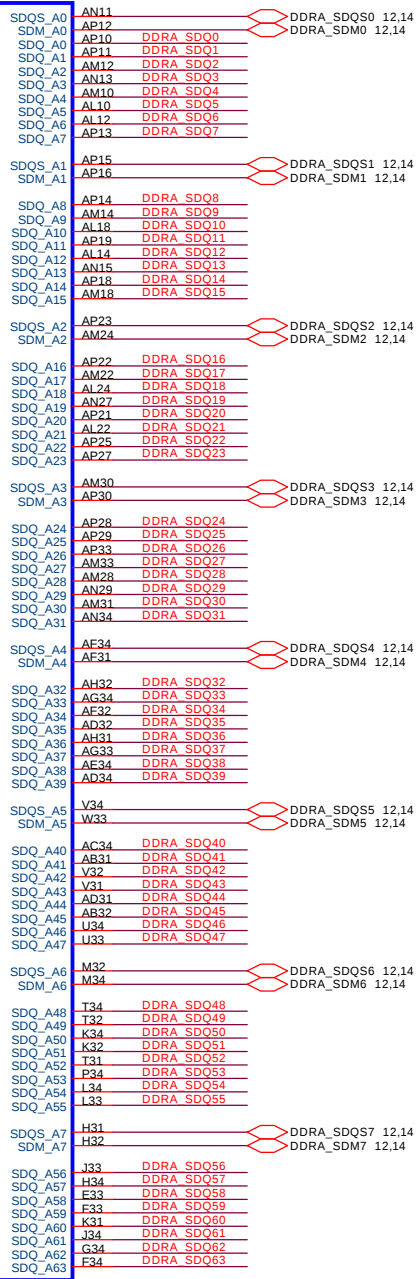
Decoupling Reference Document:
Springdale Chipset Platform Design guide Rev1.11
(12474)page239

Decoupling Reference Requirement:
560uF Polymer, ESR:5m ohm(each) * 10
22uF X5R * 32



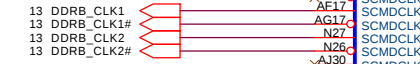
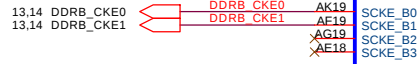
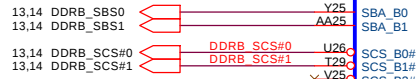
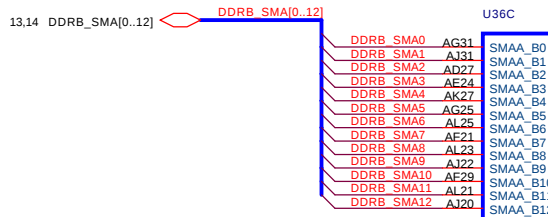


DDR Channel A

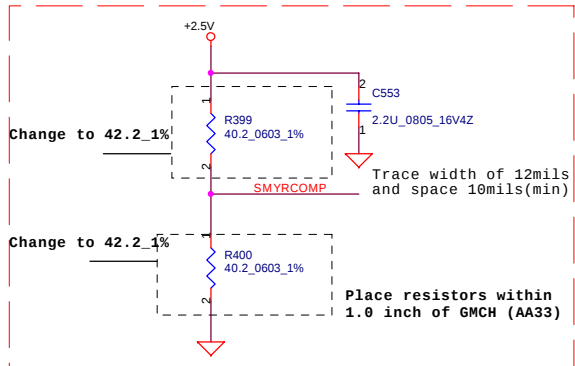
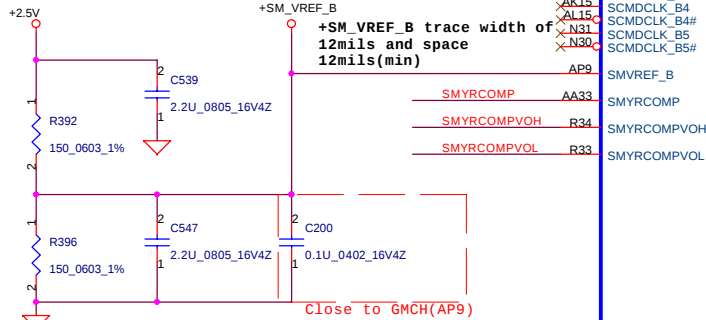


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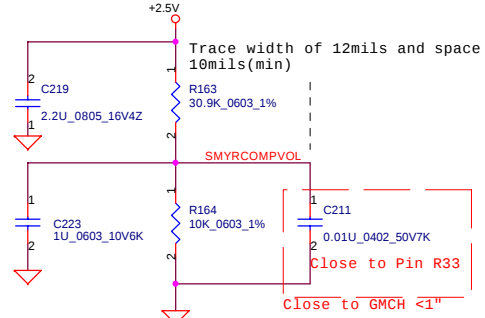
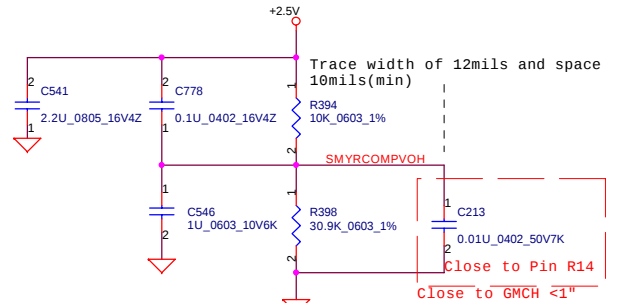
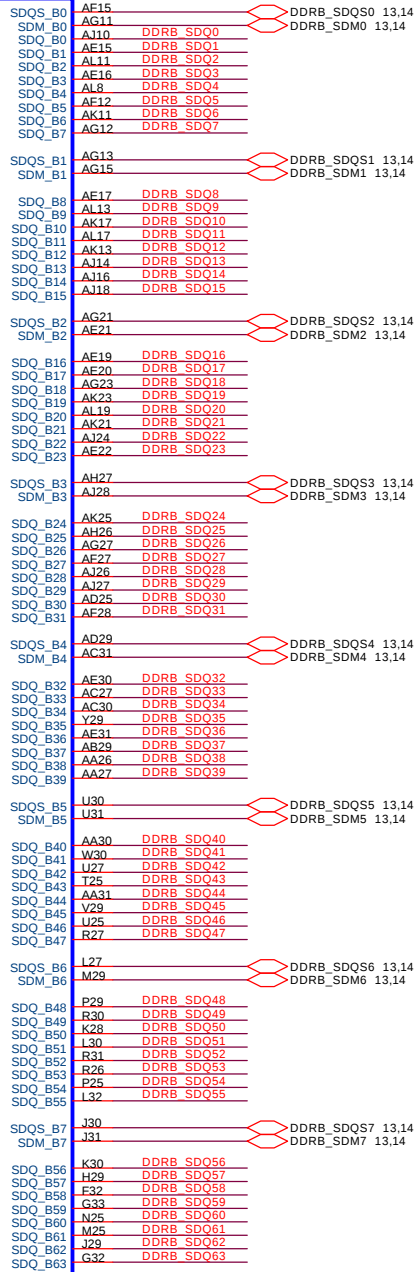
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Springdale-DDR Interface-A(2/5)			
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SM_VREF_B and SM_VREF_A
are connected inside GMCH.

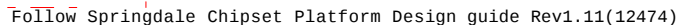
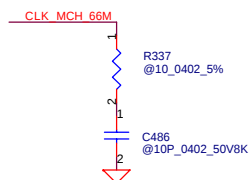
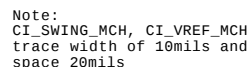
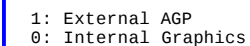


DDR Channel B

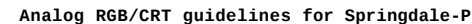


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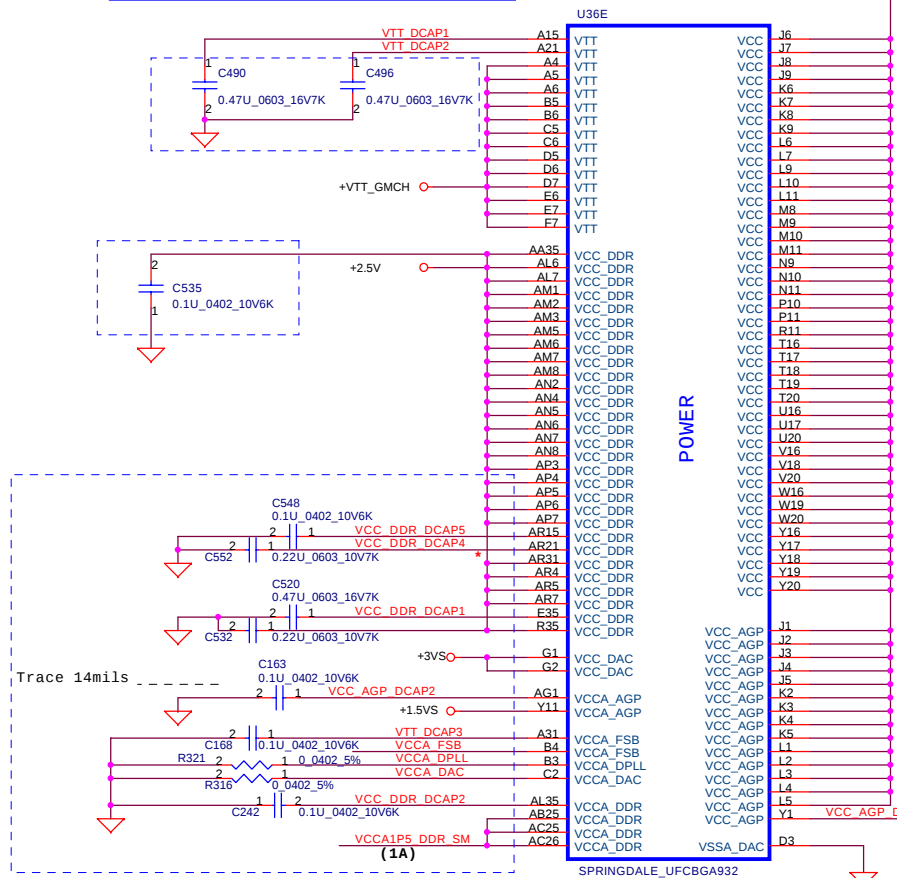
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Title		
Springdale-DDR Interface-B(3/5)		
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Note:
Springdale Customer Schematic R1.2 page18
AGP_SWING only had 0.1u cap ; But Springdale
Chipset Platform Design guide Rev1.11(12474)
page138 had a 0.01uf cap. need confirm with
Intel.



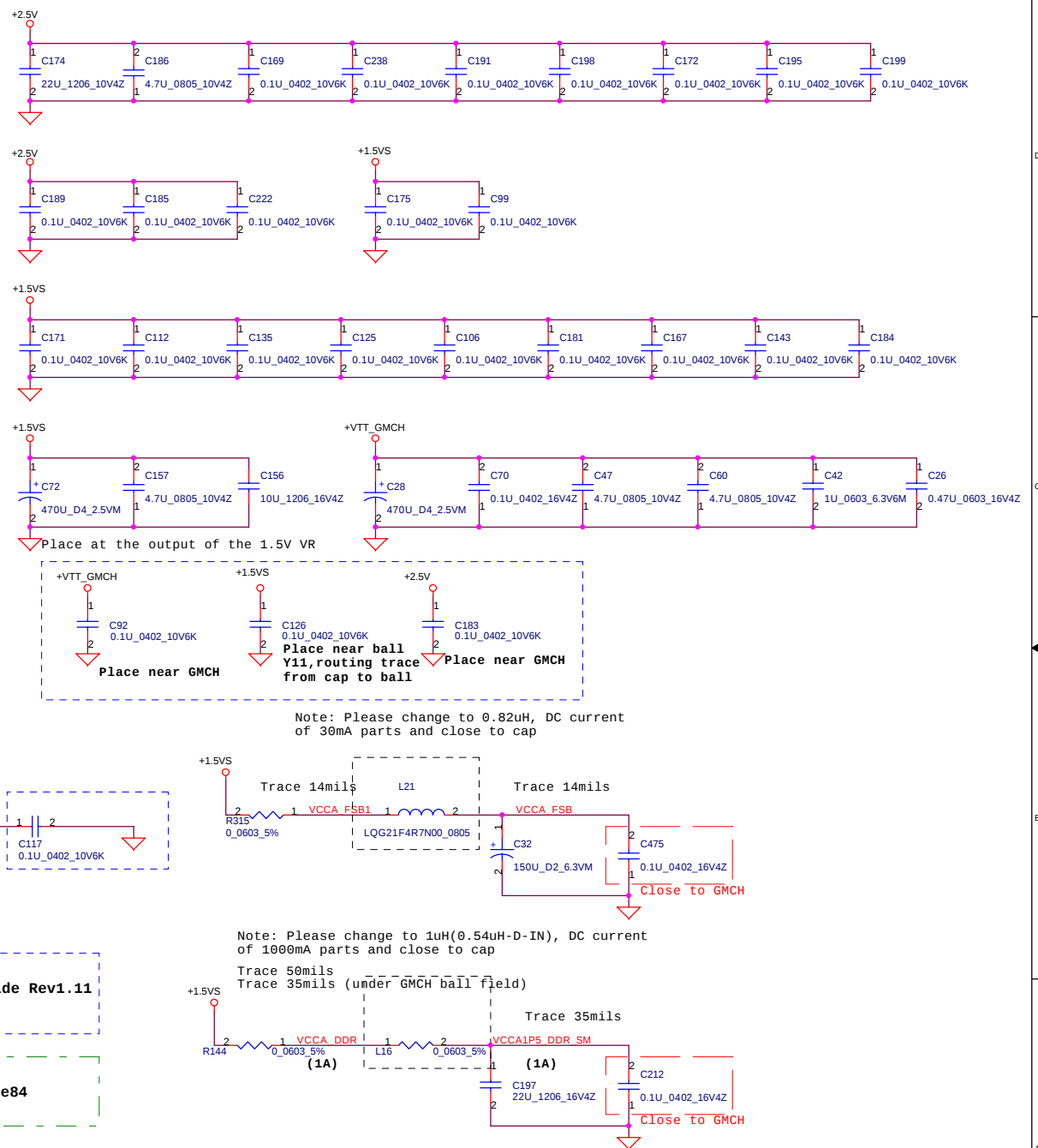
Note:
Placed less than 100 mils from ball
Route to GMCH ball without via



Note:
Placed less than 100 mils from ball
Route to GMCH ball without via

Decoupling Reference Document:
Springdale Chipset Platform Design guide Rev1.11
(12474)page246,248

Decoupling Reference Document:
Springdale Customer Schematic R1.2 page84



Compal Electronics, Inc.

Springdale-Decoupling (5/5)

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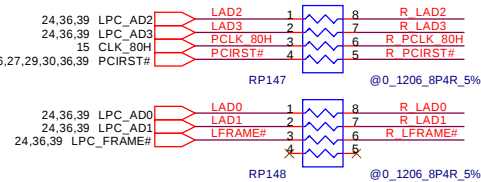
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DDR_B_VREF trace width of
12mils and space 12mils(min)

9,14 DDRB_SDQ[0..63] < DDRB_SDQ[0..63]
9,14 DDRB_SDQS[0..7] < DDRB_SDQS[0..7]
9,14 DDRB_SMA[0..12] < DDRB_SMA[0..12]
9,14 DDRB_SDM[0..7] < DDRB_SDM[0..7]

System Memory Decoupling caps

Decoupling Reference Document:
Springdale Customer Schematic R1.2 page26
each Channel(two DIMMs) requirement 0.1uF*24



DEBUG PORT

Compal Electronics, Inc.

DDR-SODIMM SLOT2

LA-2041

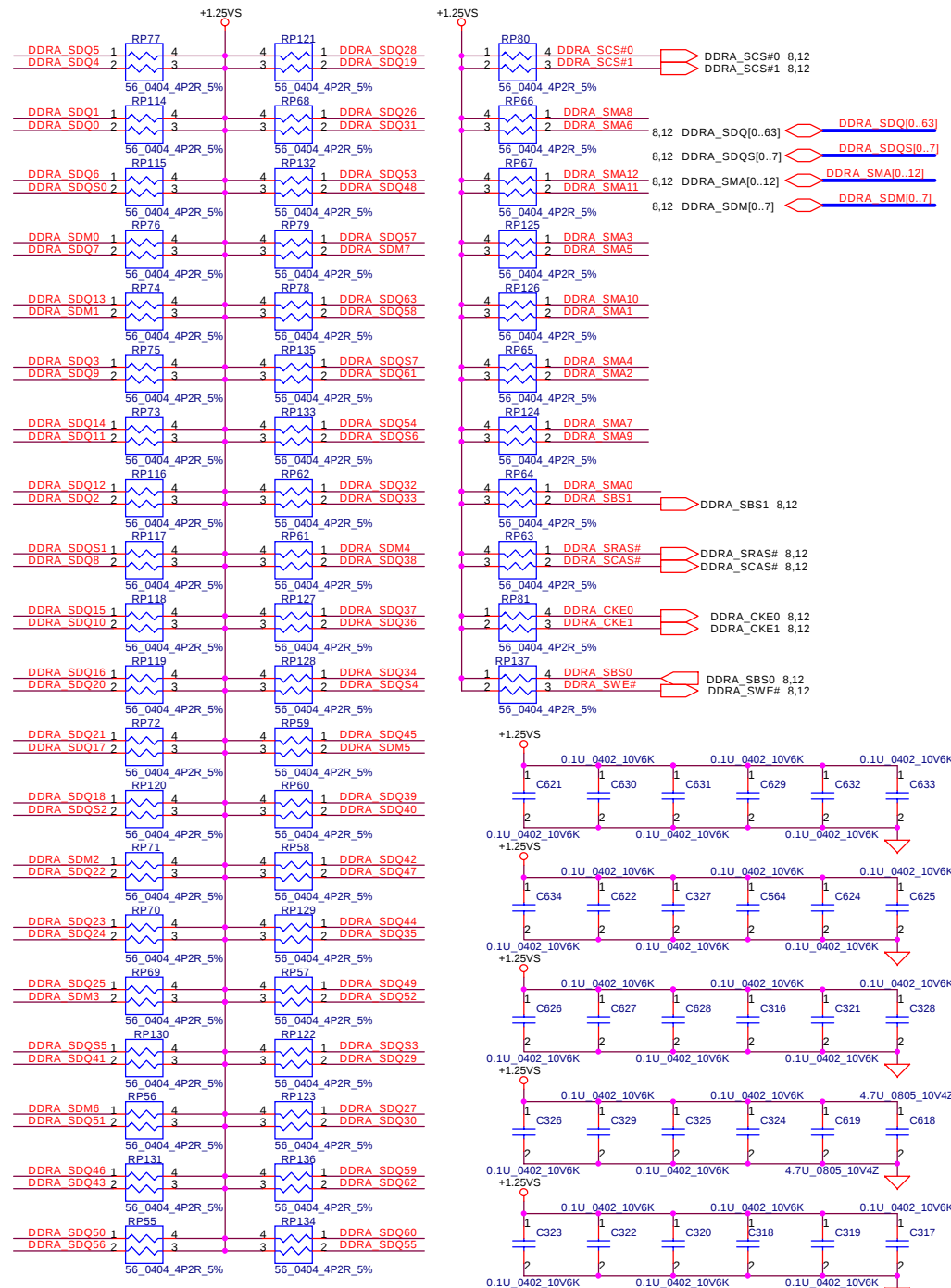
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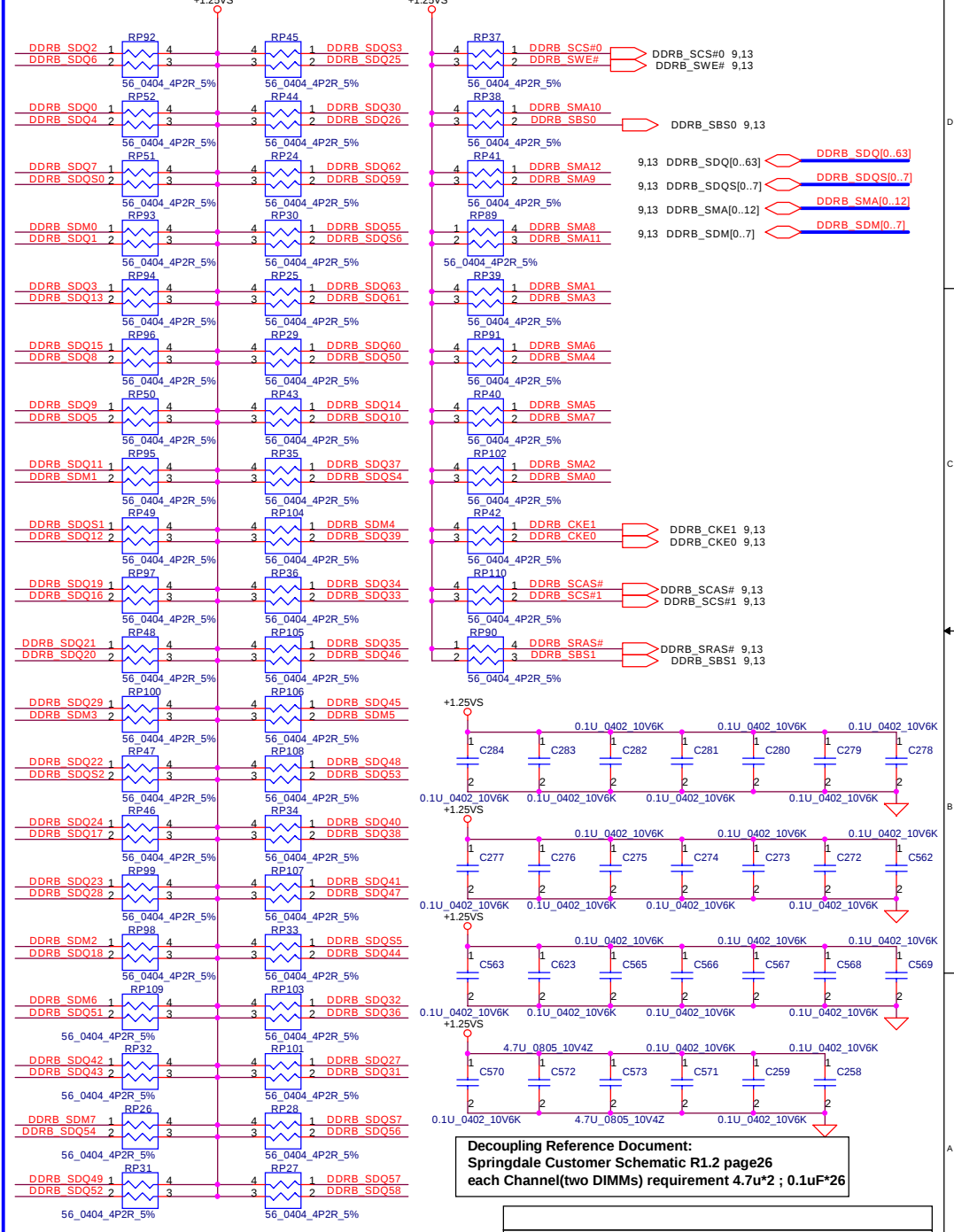
SO-DIMM 2 REVERSE

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Channel A(DIMM0) Termination resistors & Decoupling caps



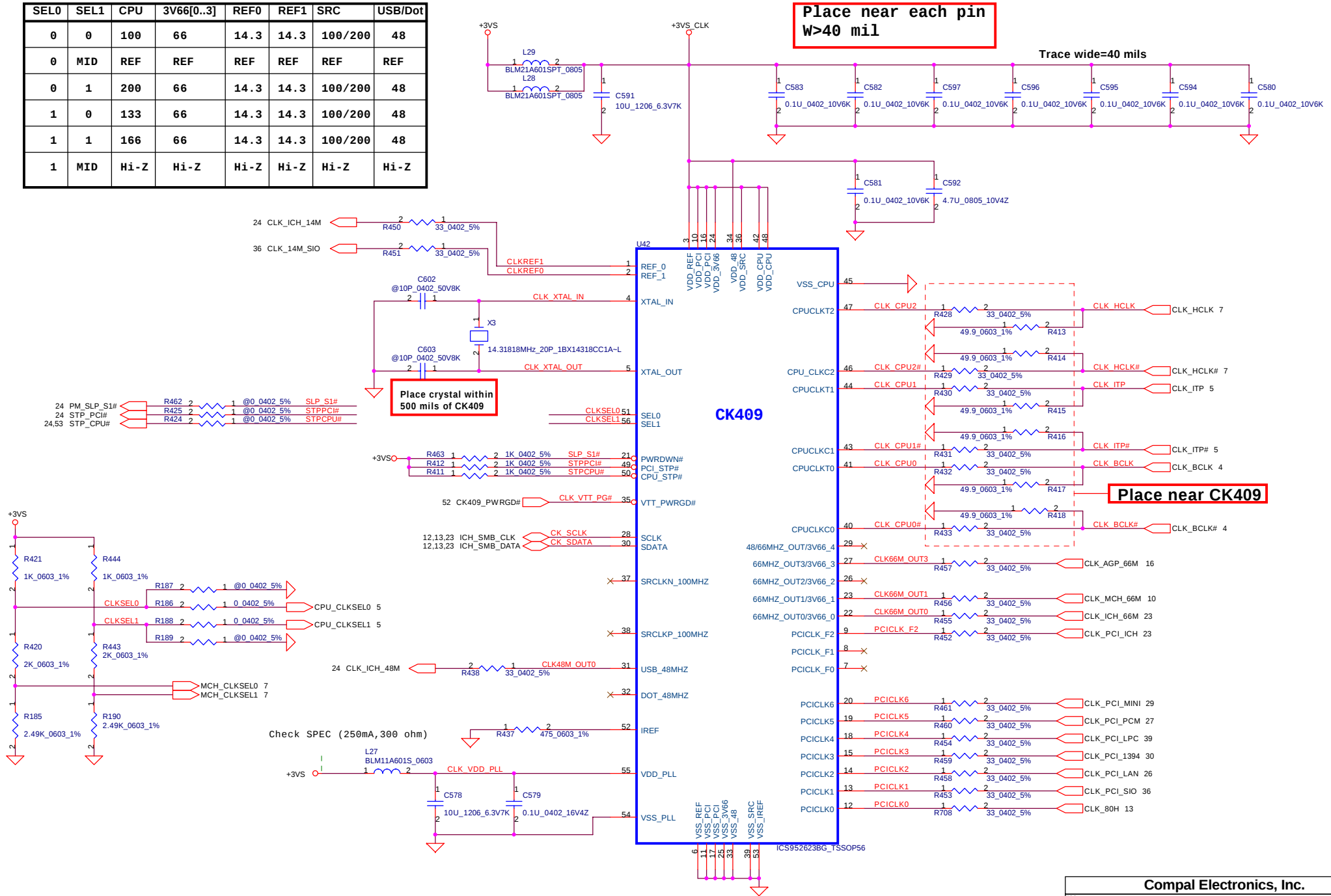
Channel B(DIMM1) Termination resistors & Decoupling caps



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Title		
DDR Termination Resistors		
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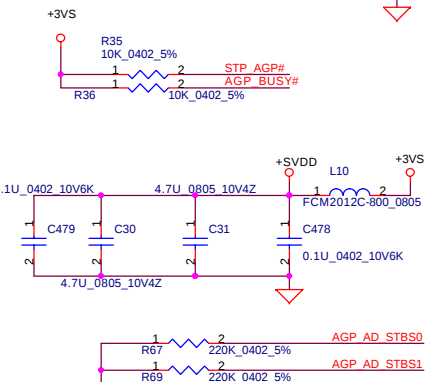
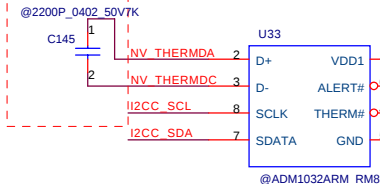
SEL0	SEL1	CPU	3V66[0..3]	REF0	REF1	SRC	USB/Dot
0	0	100	66	14.3	14.3	100/200	48
0	MID	REF	REF	REF	REF	REF	REF
0	1	200	66	14.3	14.3	100/200	48
1	0	133	66	14.3	14.3	100/200	48
1	1	166	66	14.3	14.3	100/200	48
1	MID	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z



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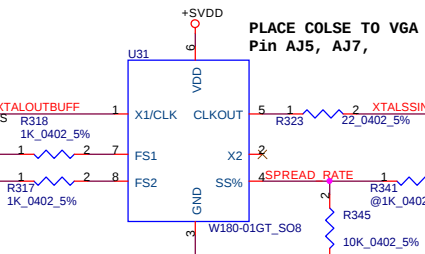
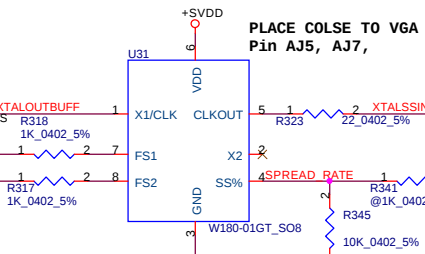
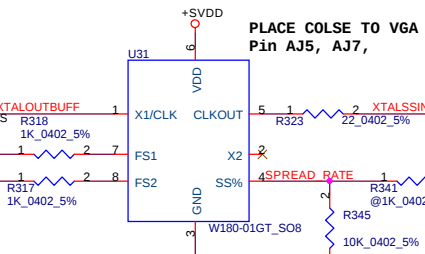
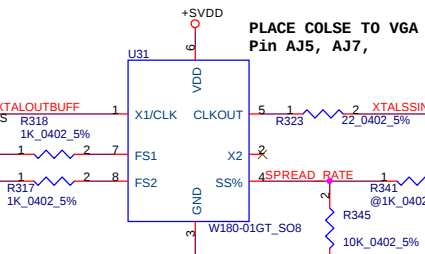
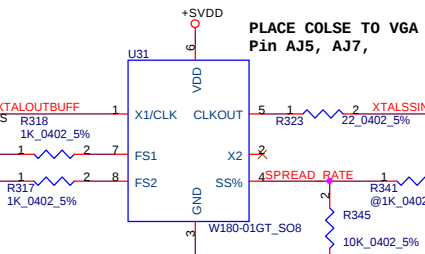
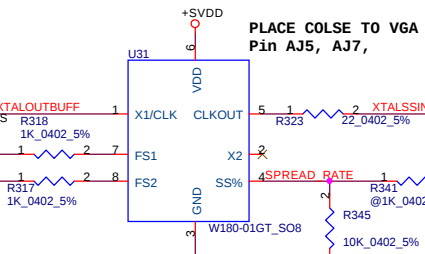
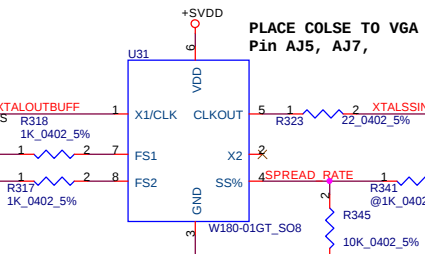
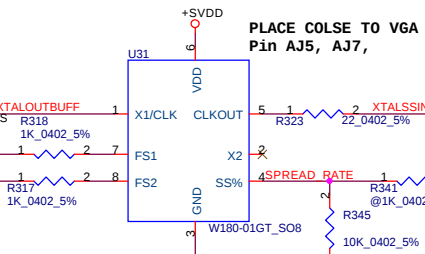
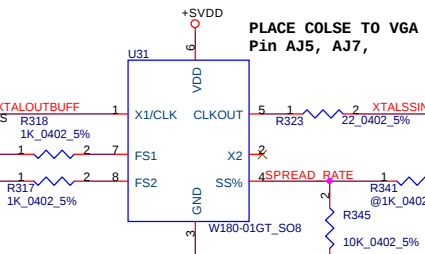
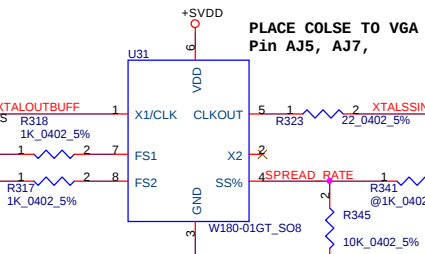
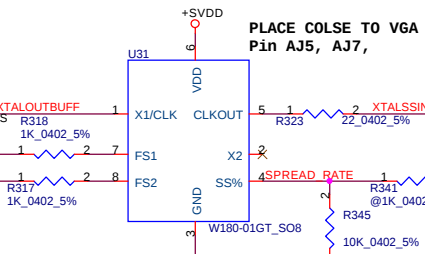
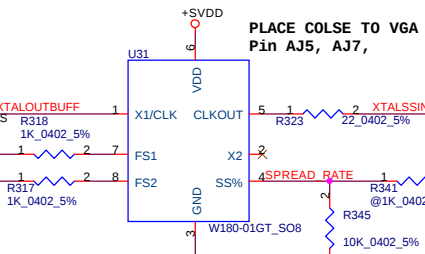
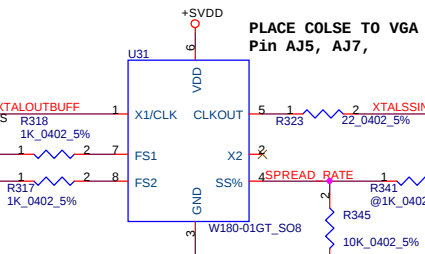
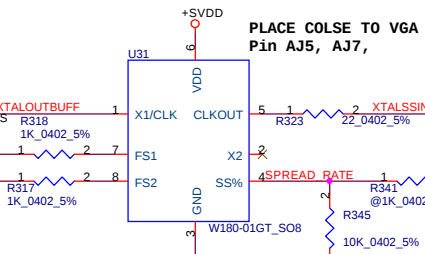
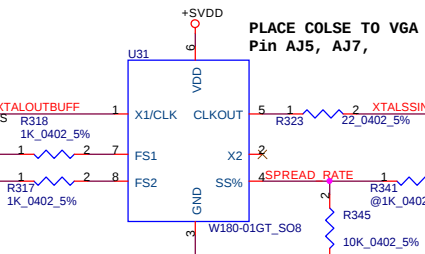
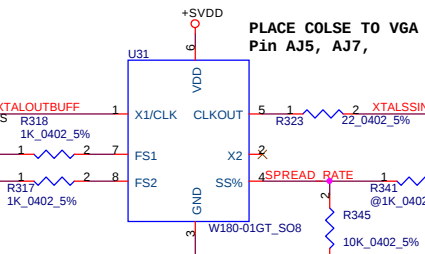
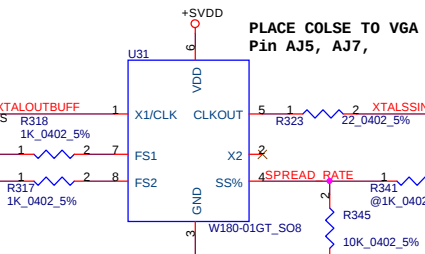
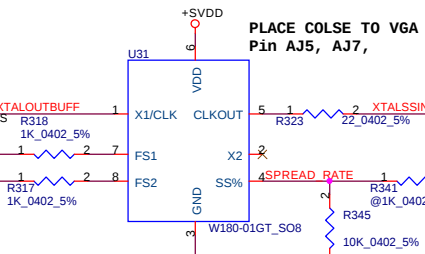
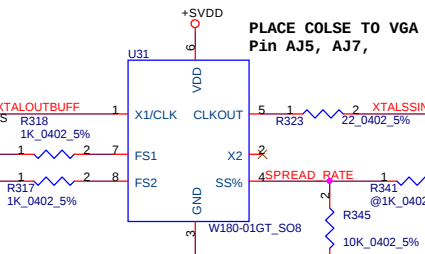
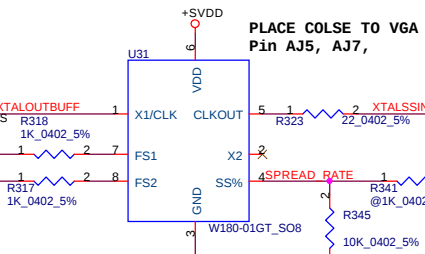
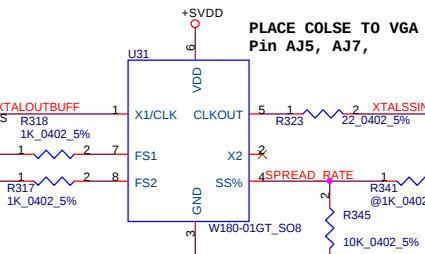
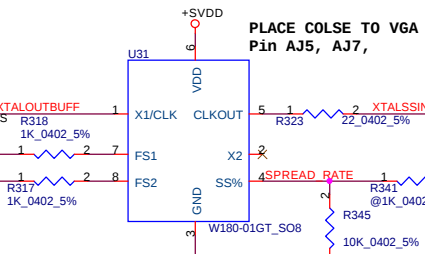
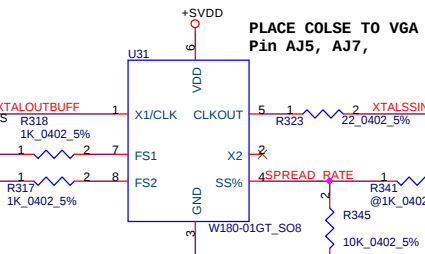
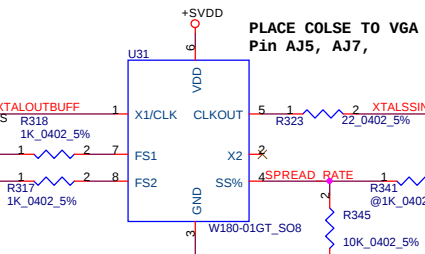
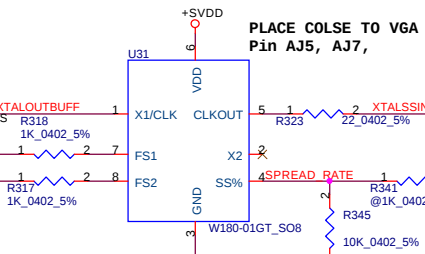
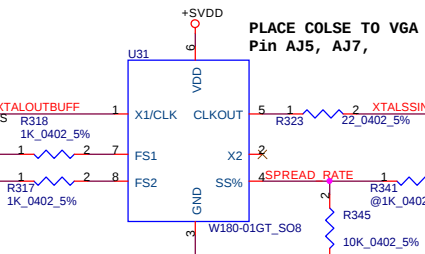
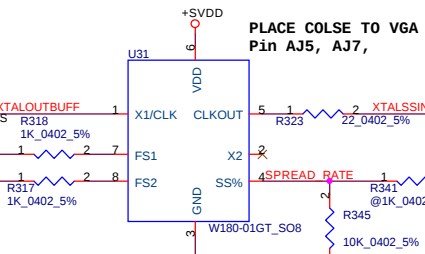
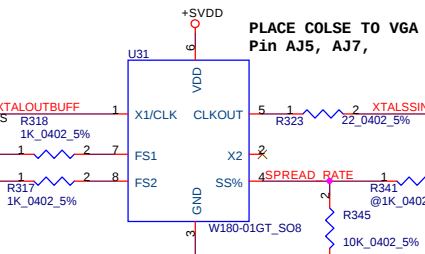
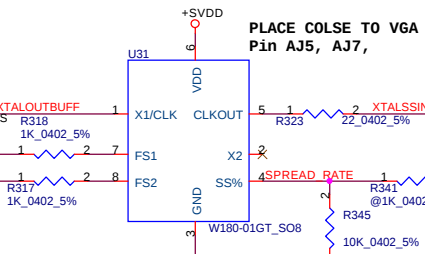
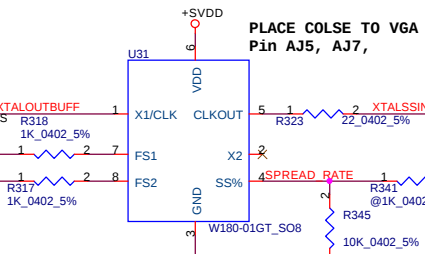
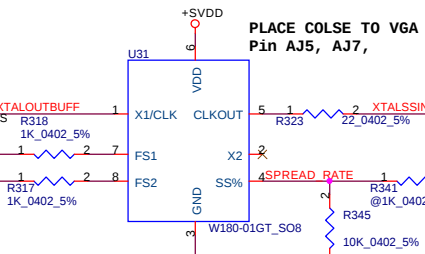
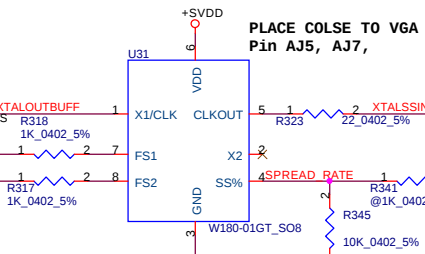
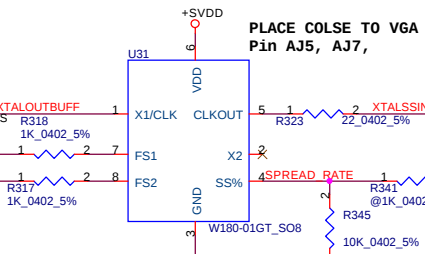
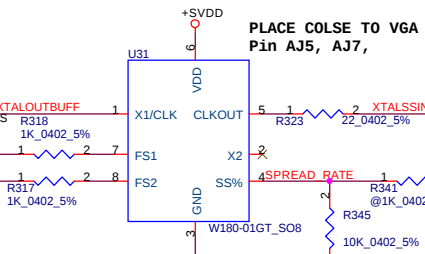
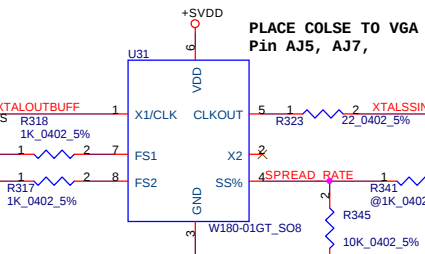
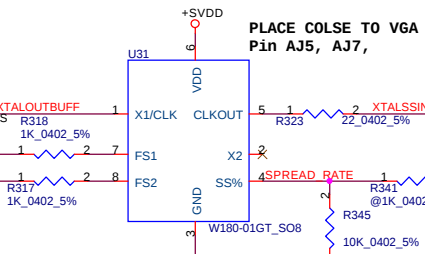
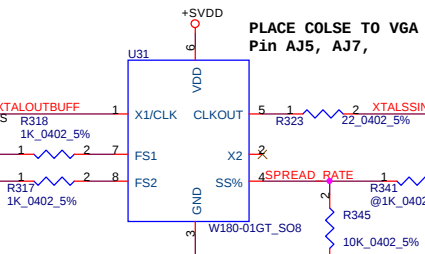
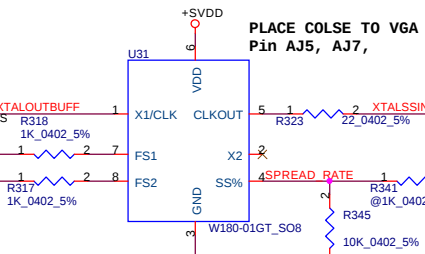
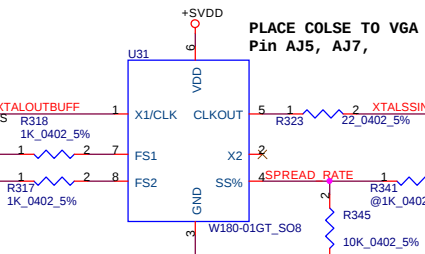
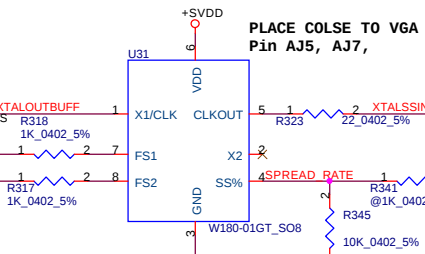
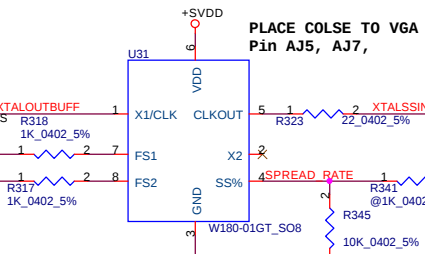
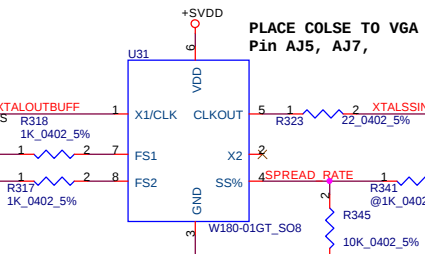
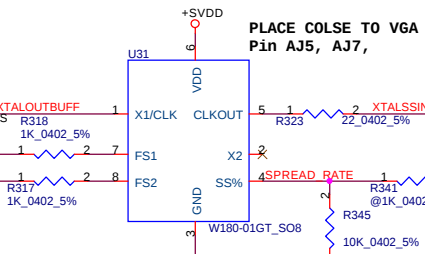
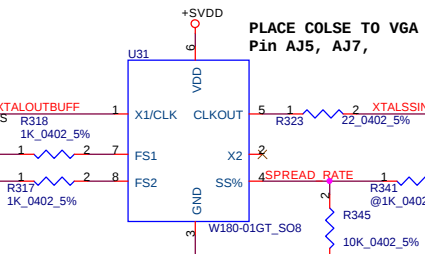
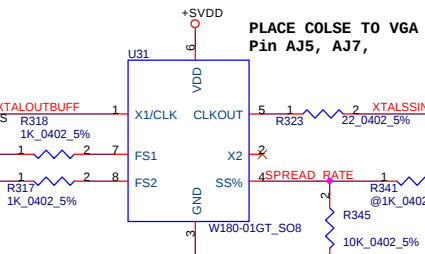
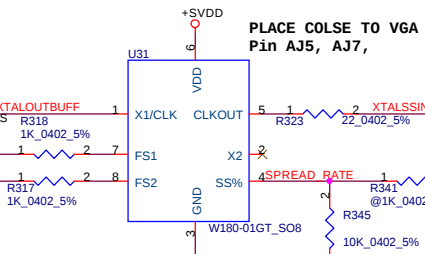
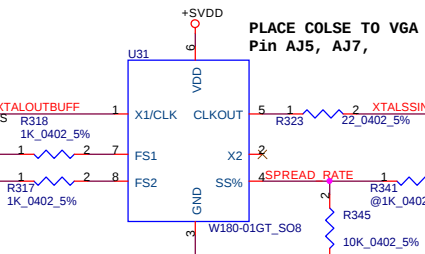
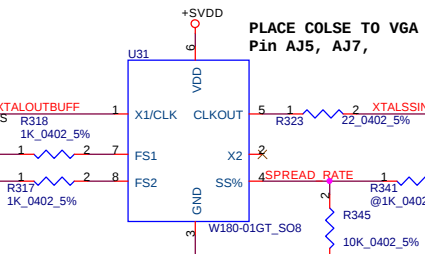
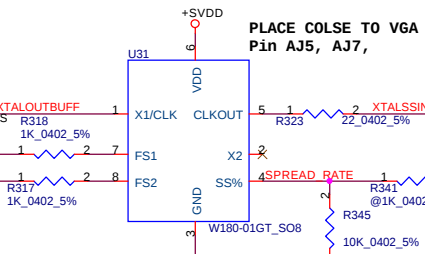
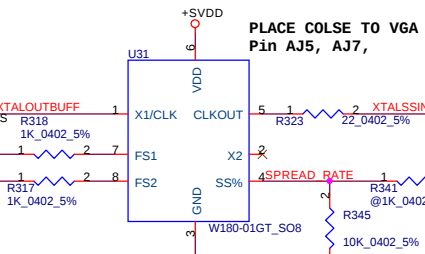
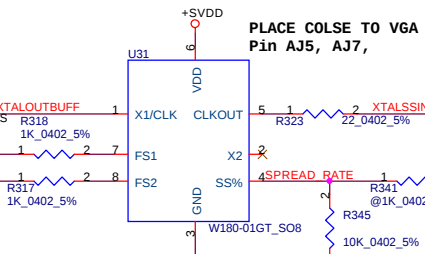
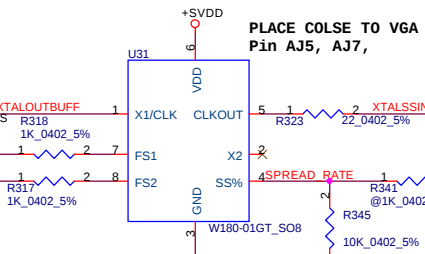
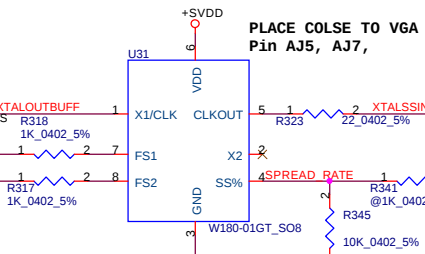
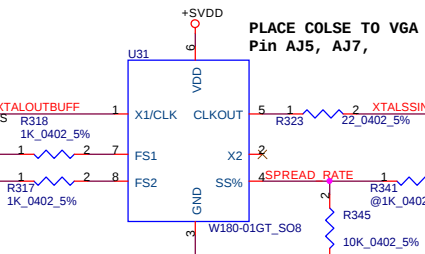
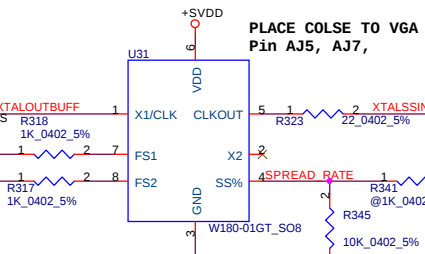
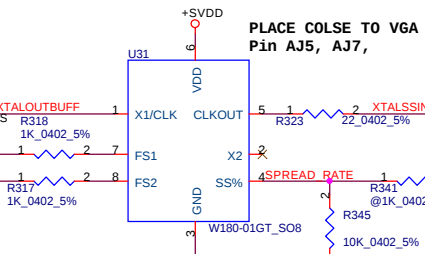
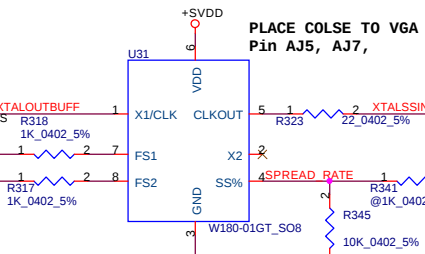
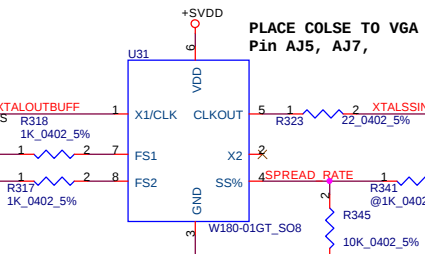
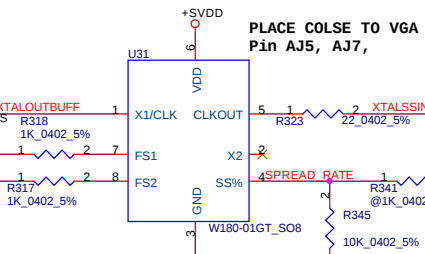
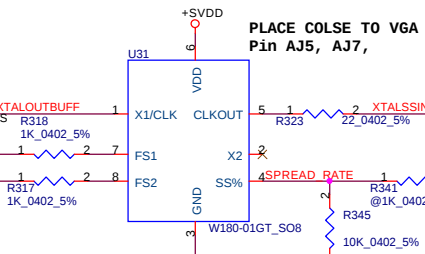
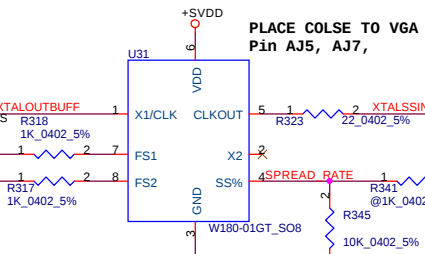
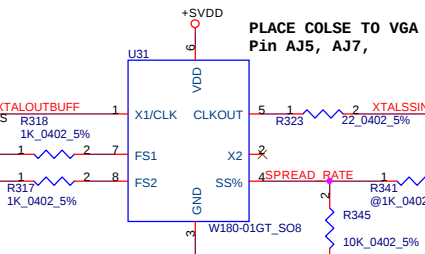
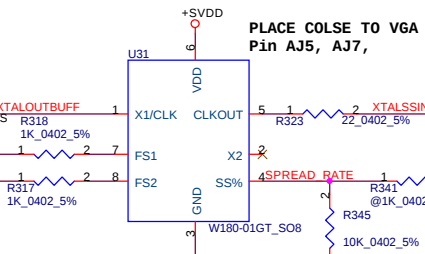
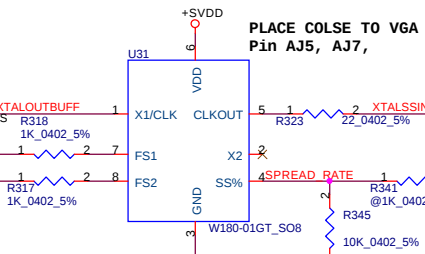
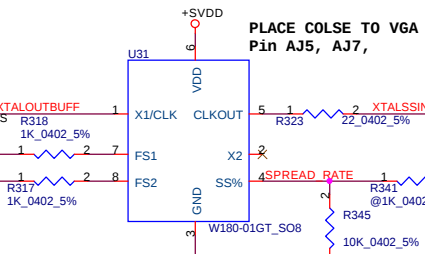
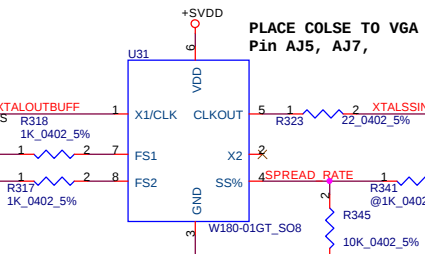
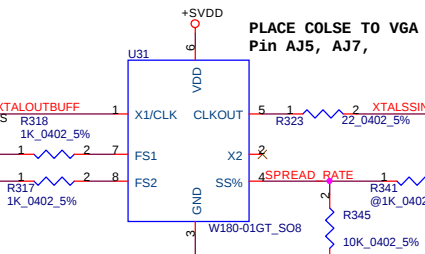
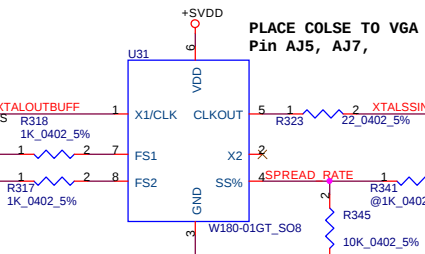
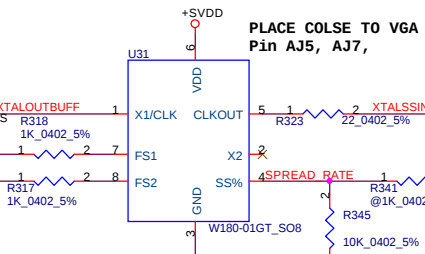
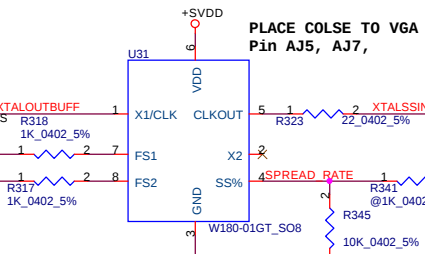
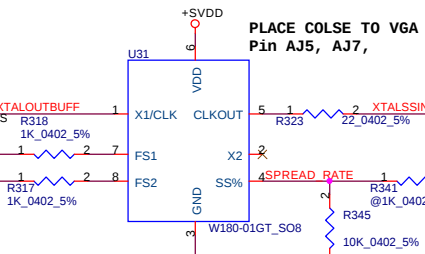
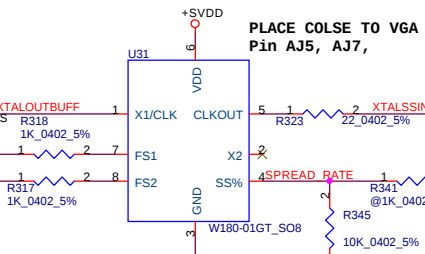
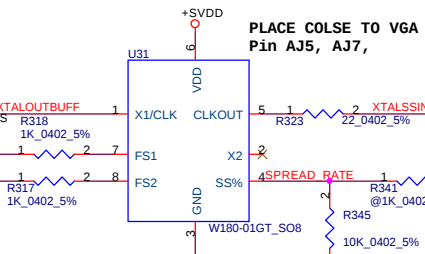
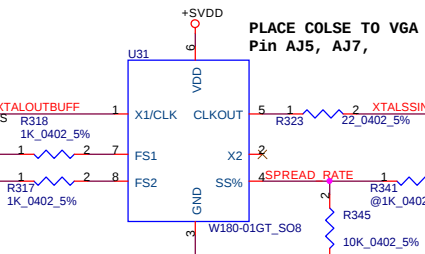
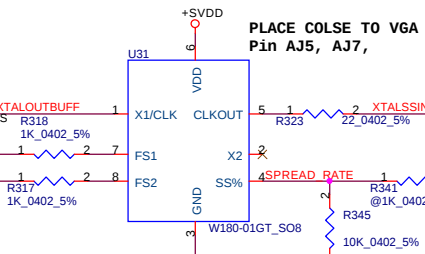
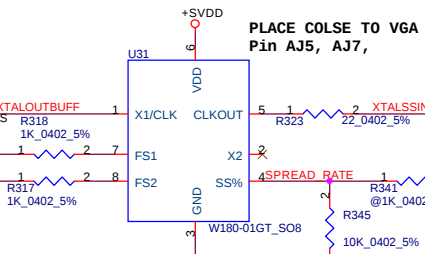
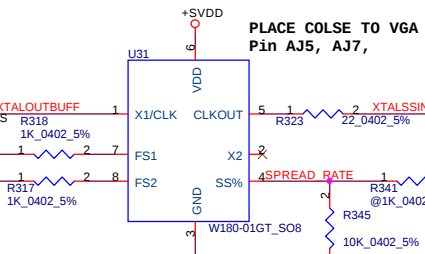
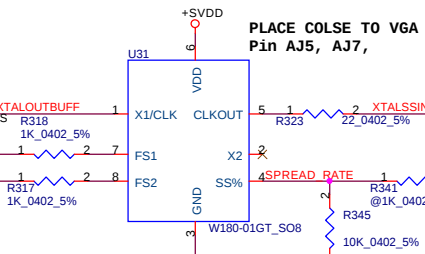
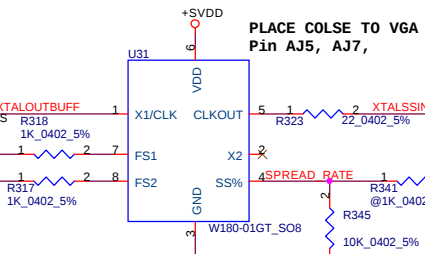
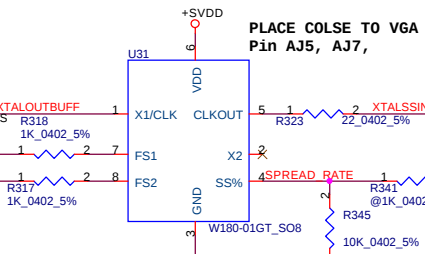
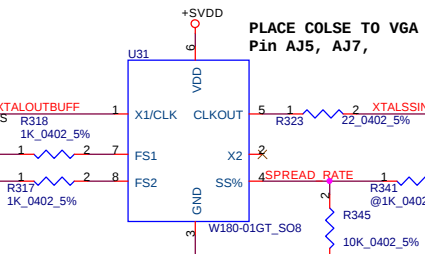
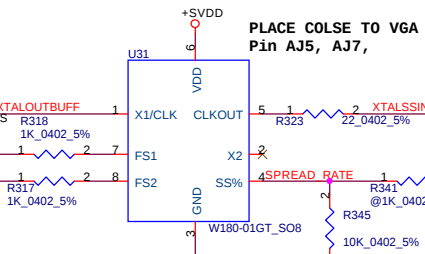
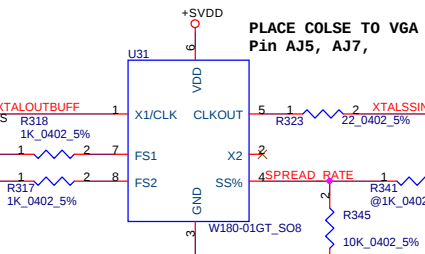
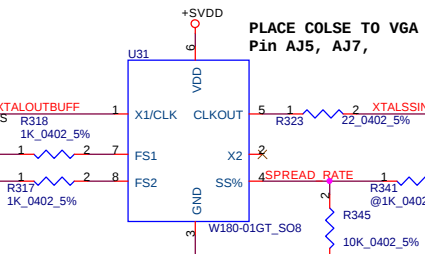
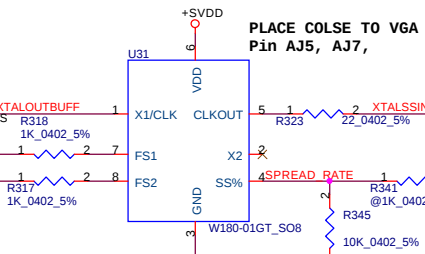
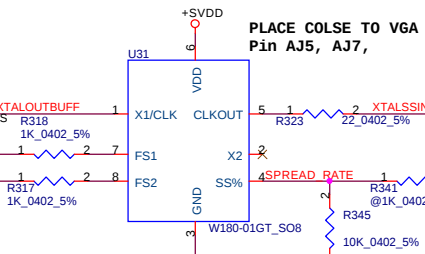
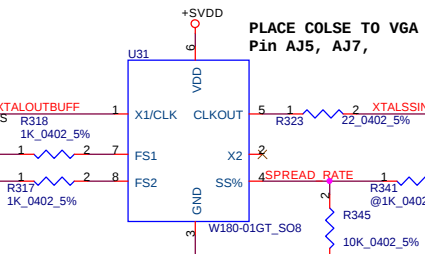
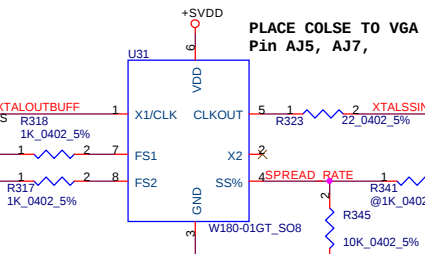
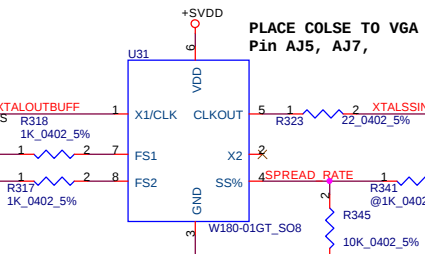
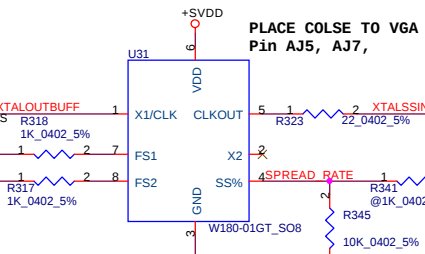
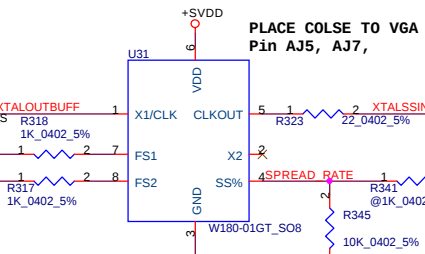
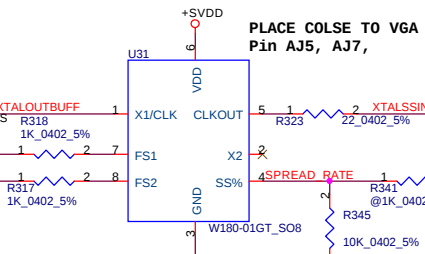
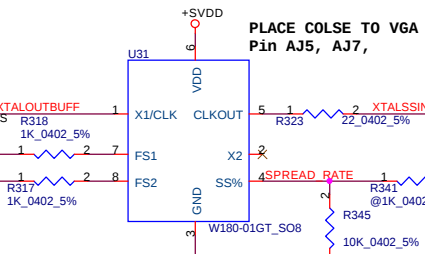
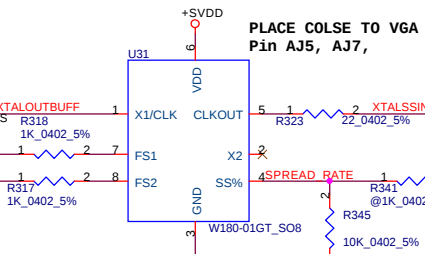
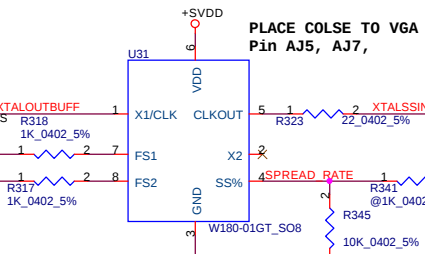
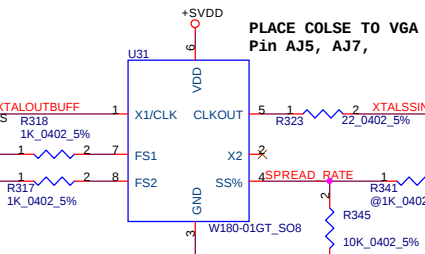
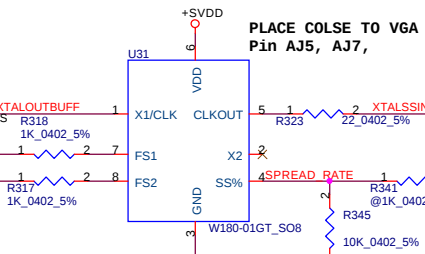
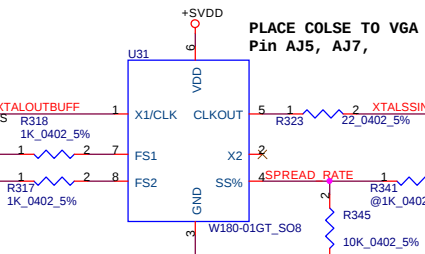
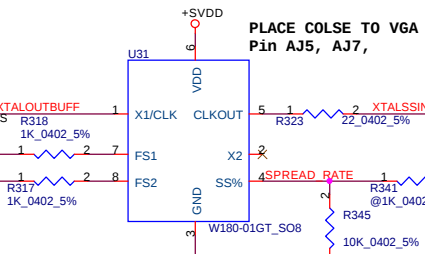
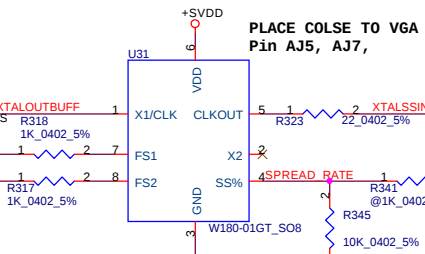
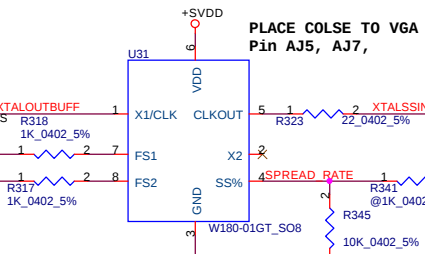
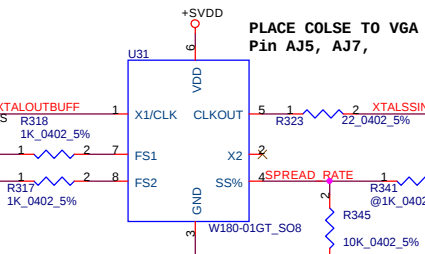
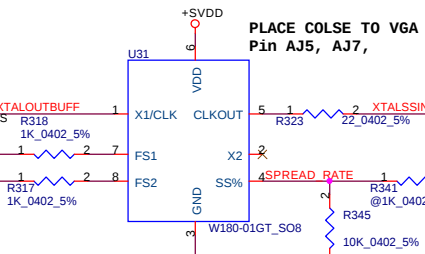
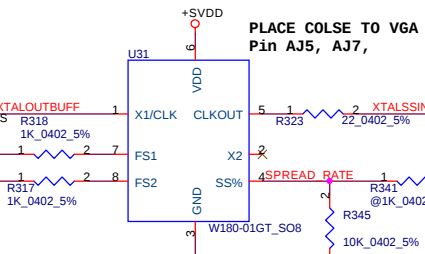
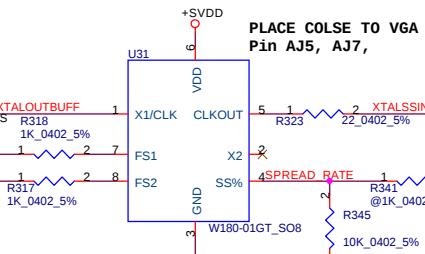
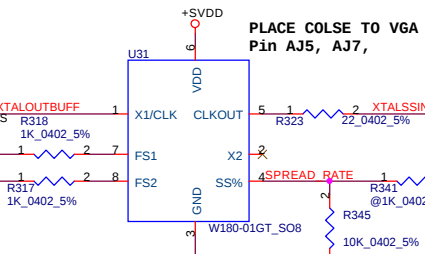
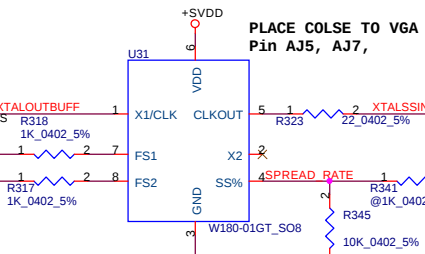
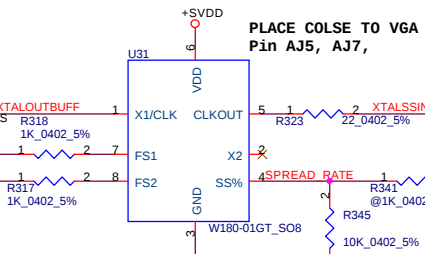
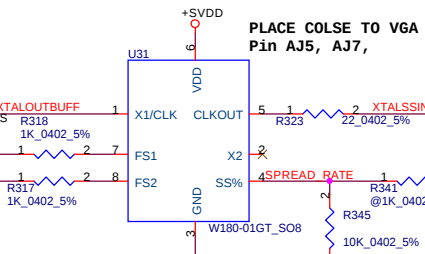
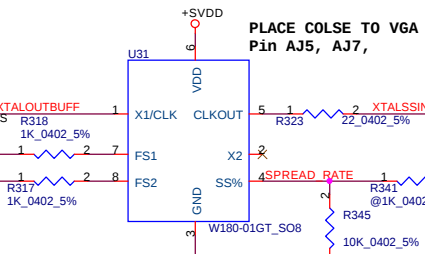
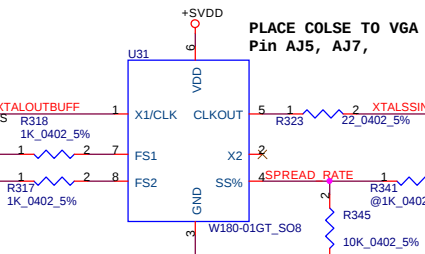
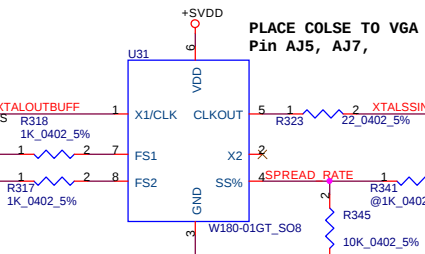
Compal Electronics, Inc.		
Clock Generator		
Title	Document Number	Rev
	LA-2041	0.1
Date: ~P 星期三, 七月 09, 2003	Sheet 15 of 56	

Place close
to pin
H2 & H3



Selection Table For W180

Modulation Setting	SST Ratio
SS%	
0	1.25%
1	3.75%

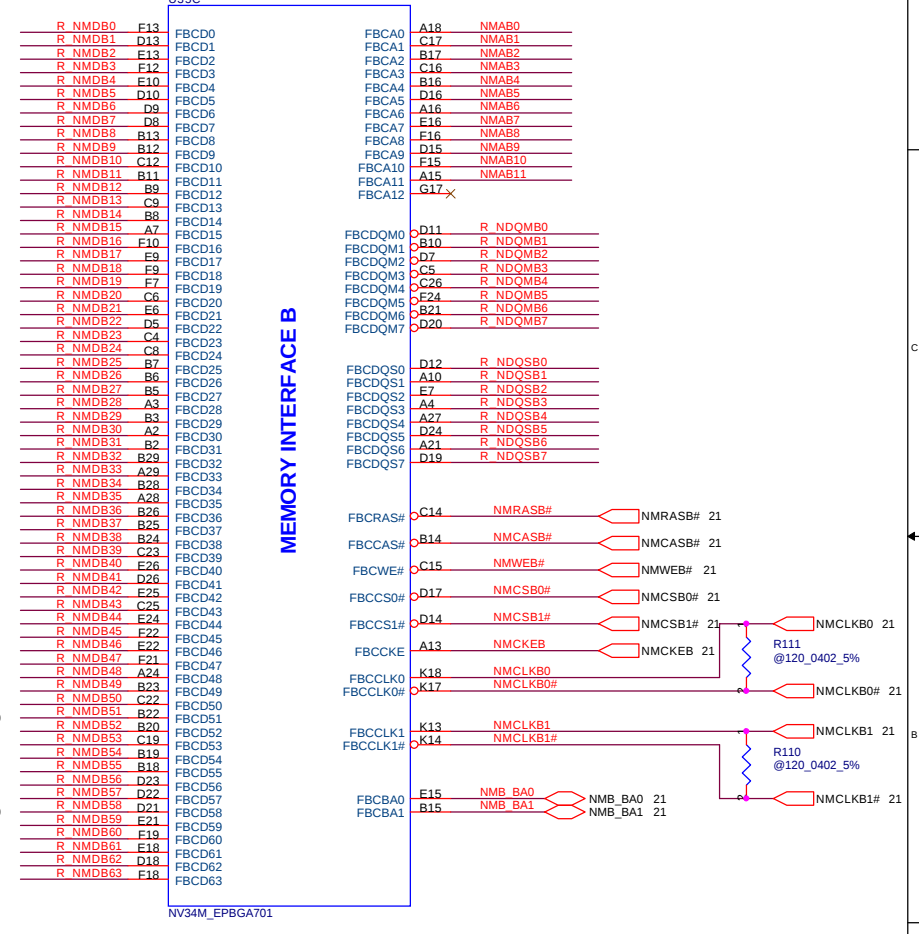


20 R_NDQMA[0..7]  R_NDQMA[0..7]
20 R_NDQSA[0..7]  R_NDQSA[0..7]
20 NMAA[0..11]  NMAA[0..11]
20 R_NMDA[0..63]  R_NMDA[0..63]

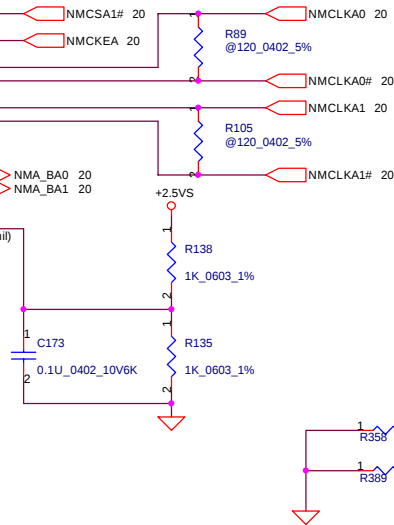
21 R_NDQMB[0..7]  R_NDQMB[0..7]
21 R_NDQSB[0..7]  R_NDQSB[0..7]
21 NMAB[0..11]  NMAB[0..11]
21 R_NMDB[0..63]  R_NMDB[0..63]



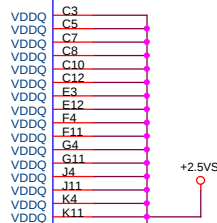
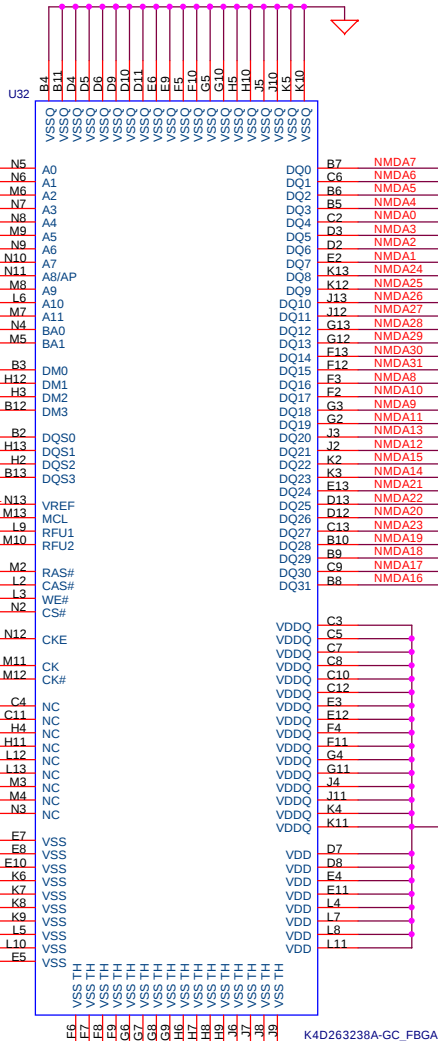
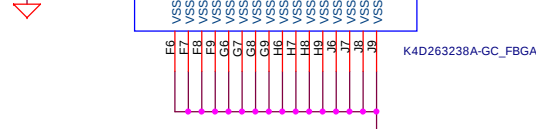
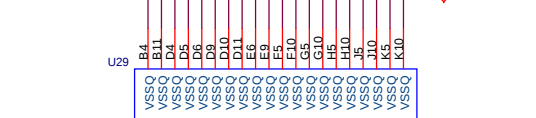
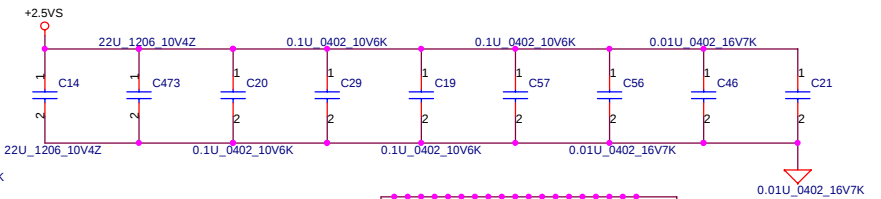
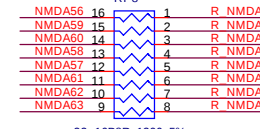
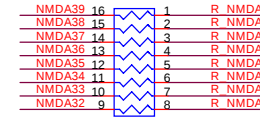
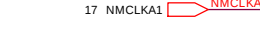
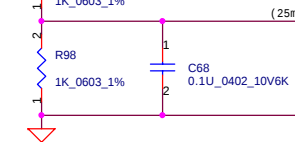
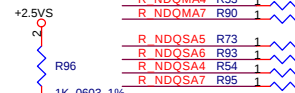
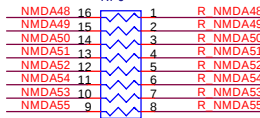
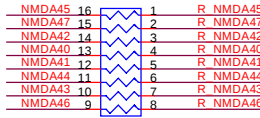
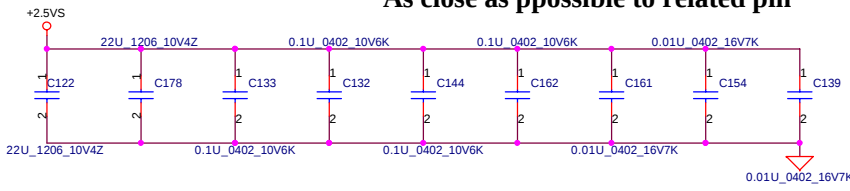
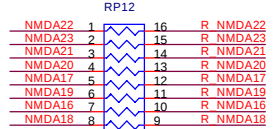
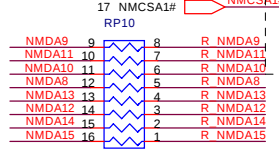
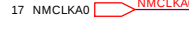
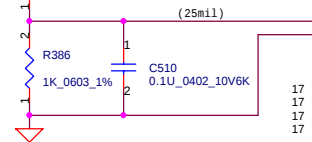
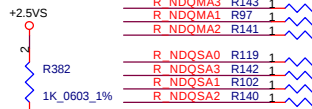
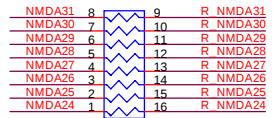
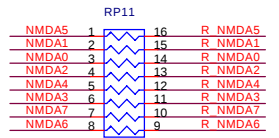
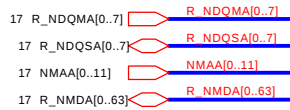
MEMORY INTERFACE A



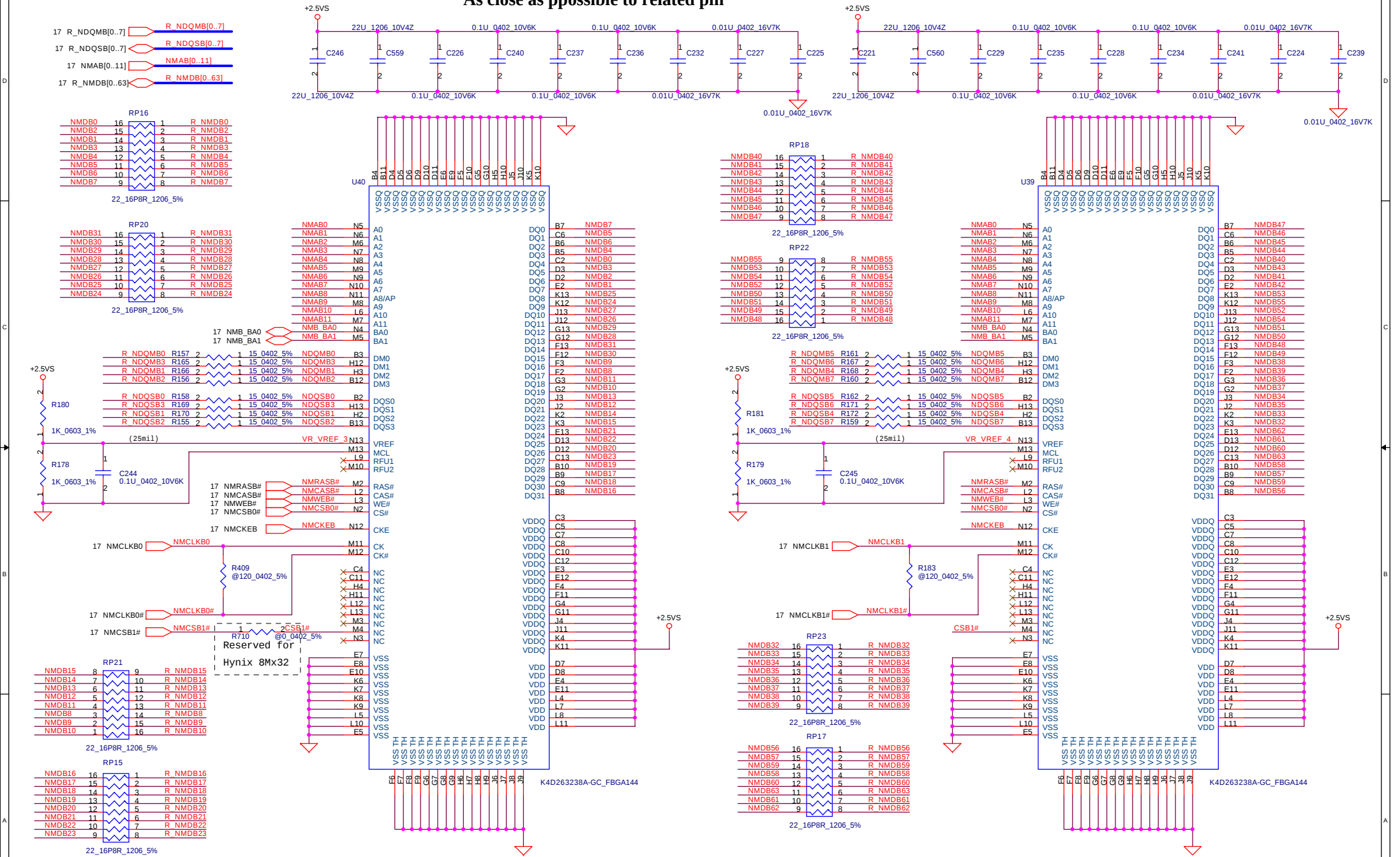
MEMORY INTERFACE B



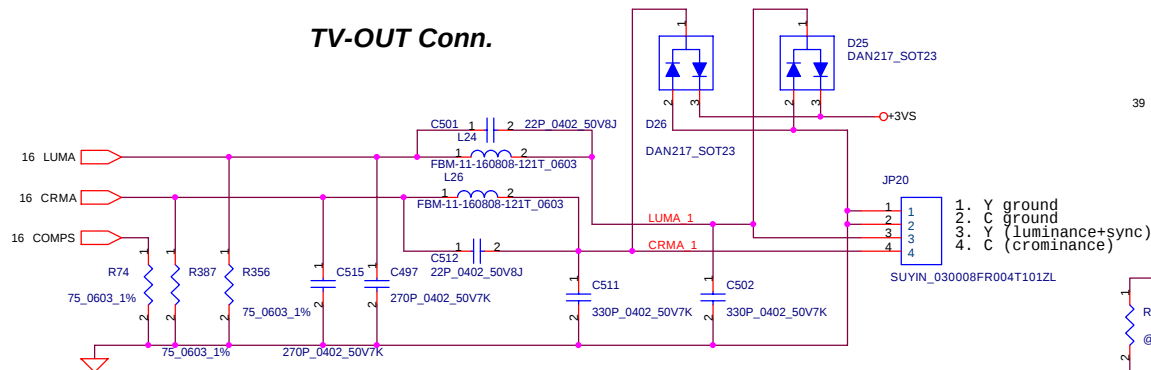
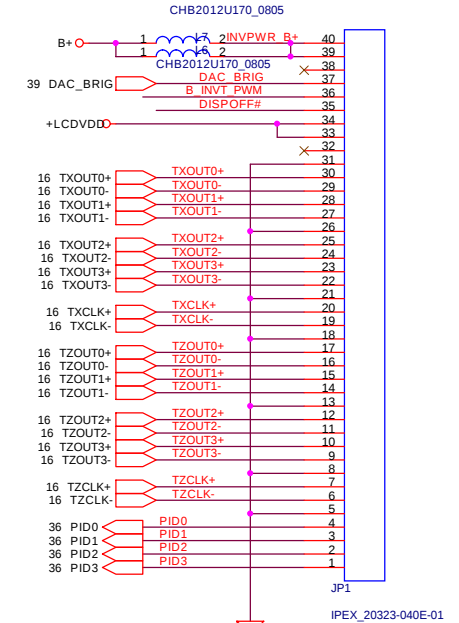
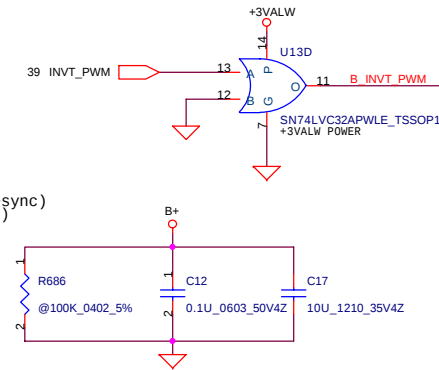
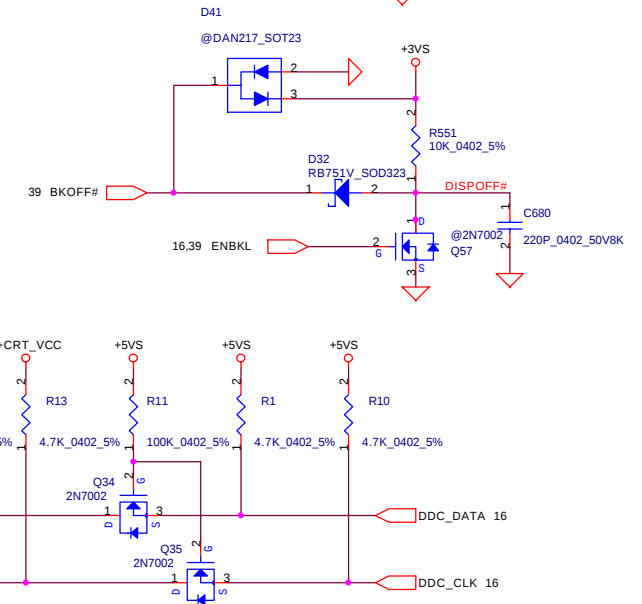
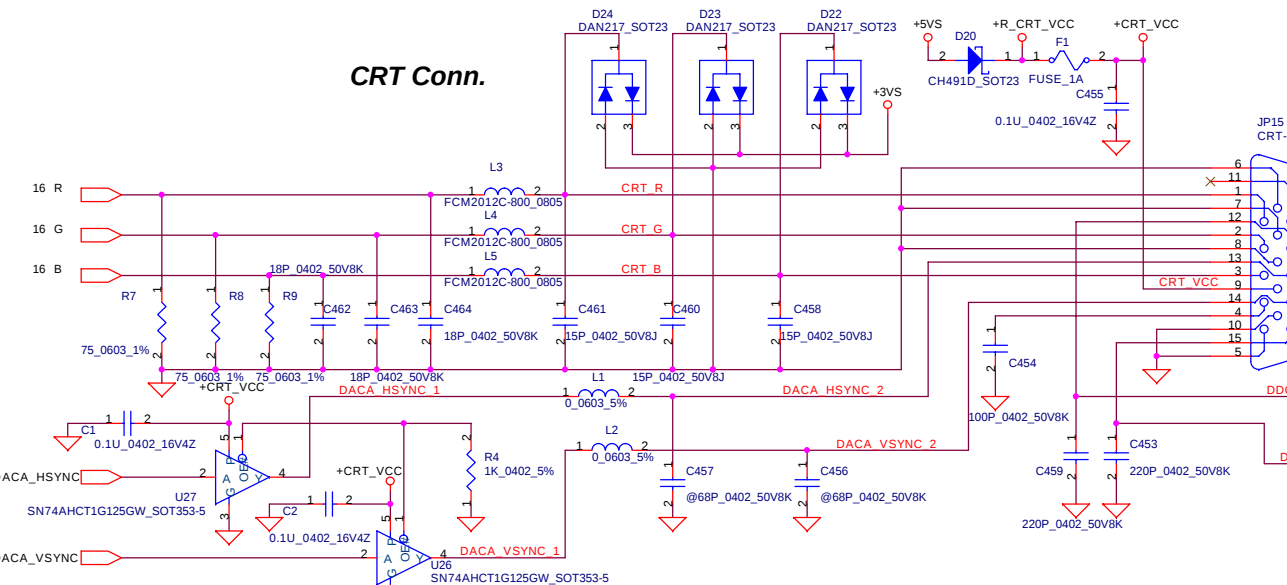
As close as ppossible to related pin



As close as ppossible to related pin



CRT, TV-OUT & LVDS CONNECTOR

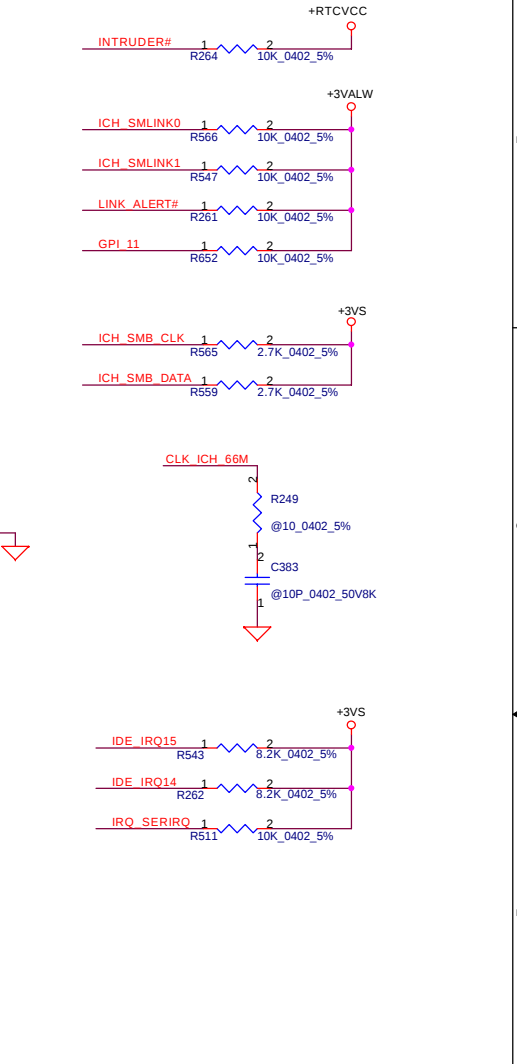
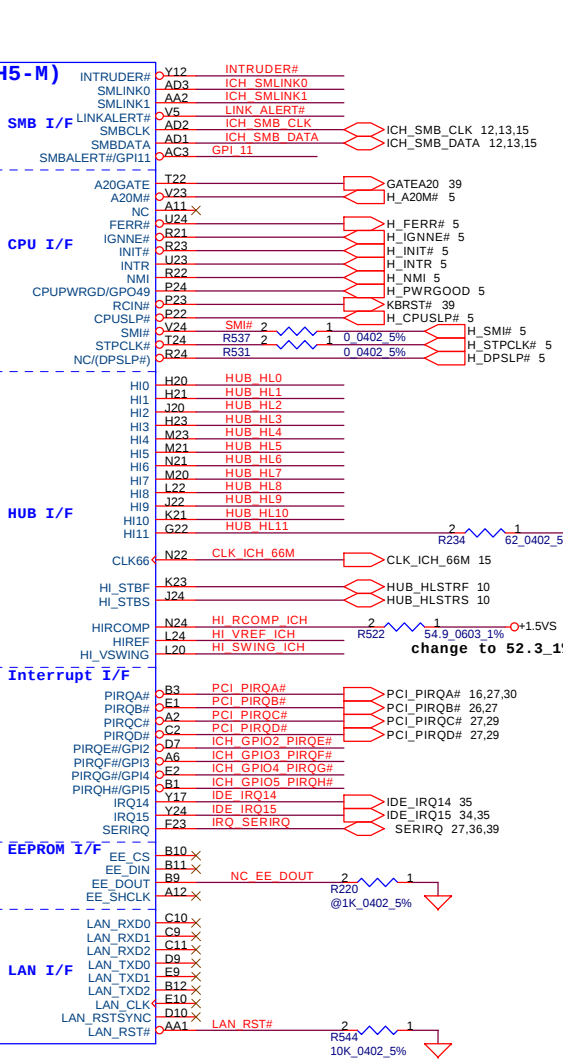
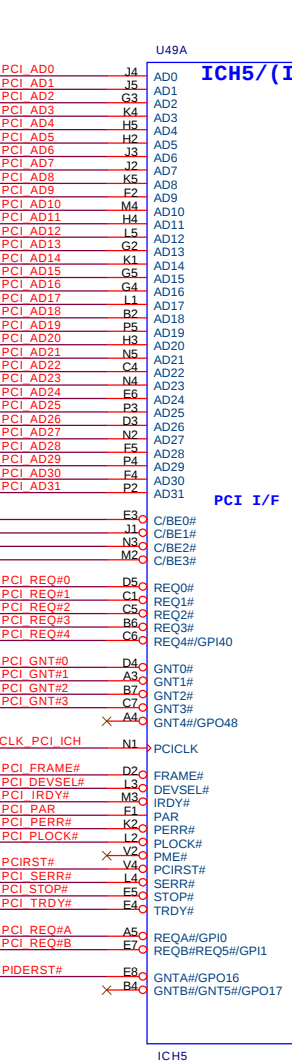
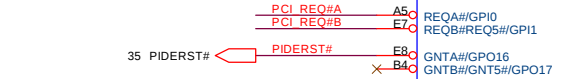
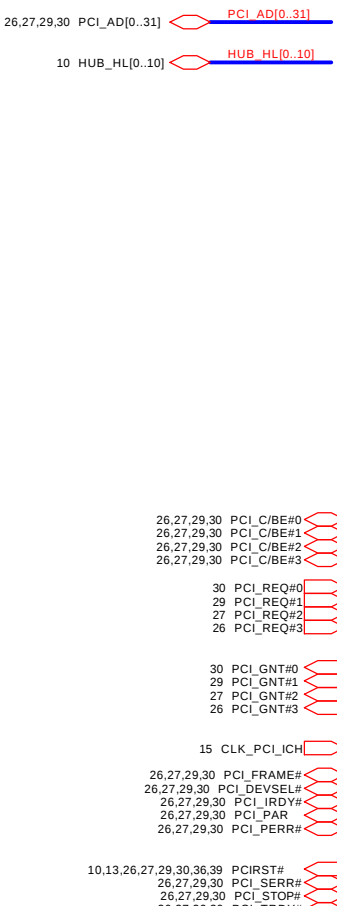
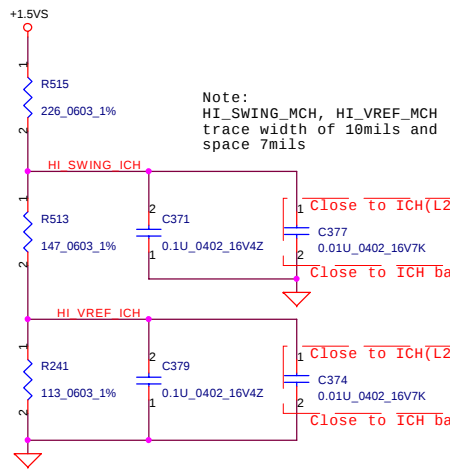
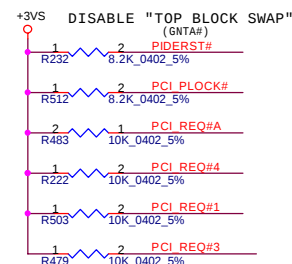
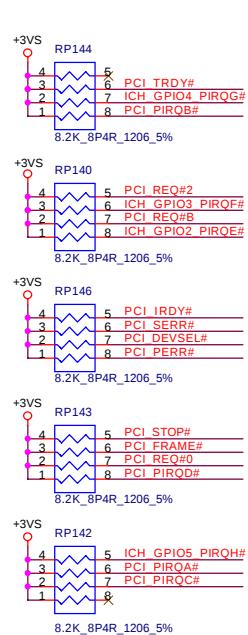
TV-OUT Conn.**LVDS Conn.****CRT Conn.**

Compal Electronics, Inc.

Title	CRT,TV-OUT & LVDS Connector
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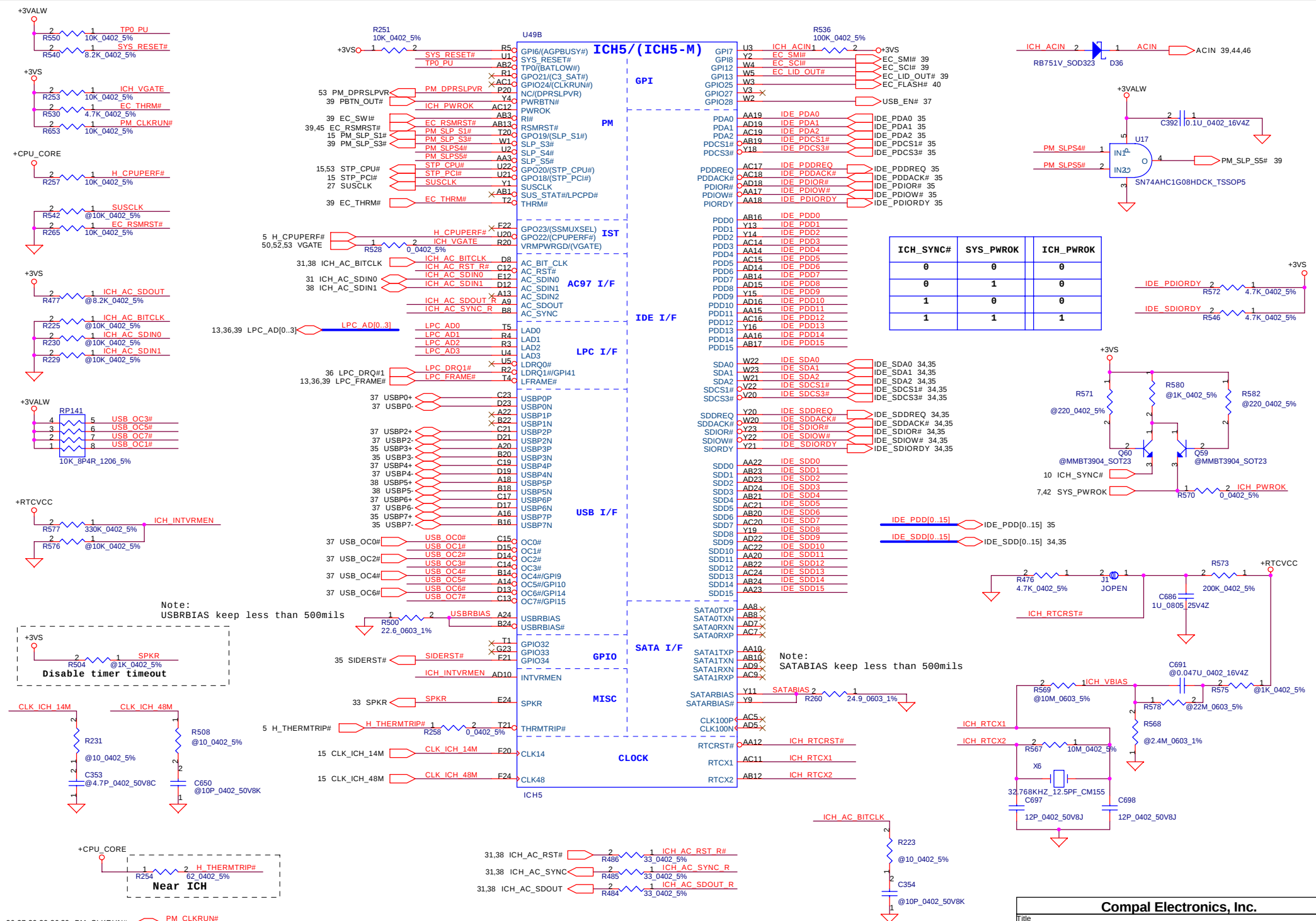
Size B	Document Number LA-2041	Rev 0.1
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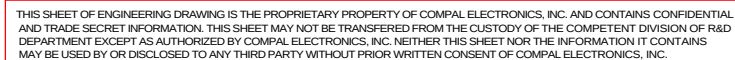
Compal Electronics, Inc.		
Title ICH5-PCI/HUB/LAN		
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ICH_SYNC#	SYS_PWROK	ICH_PWROK
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0	1	0
1	0	0
1	1	1

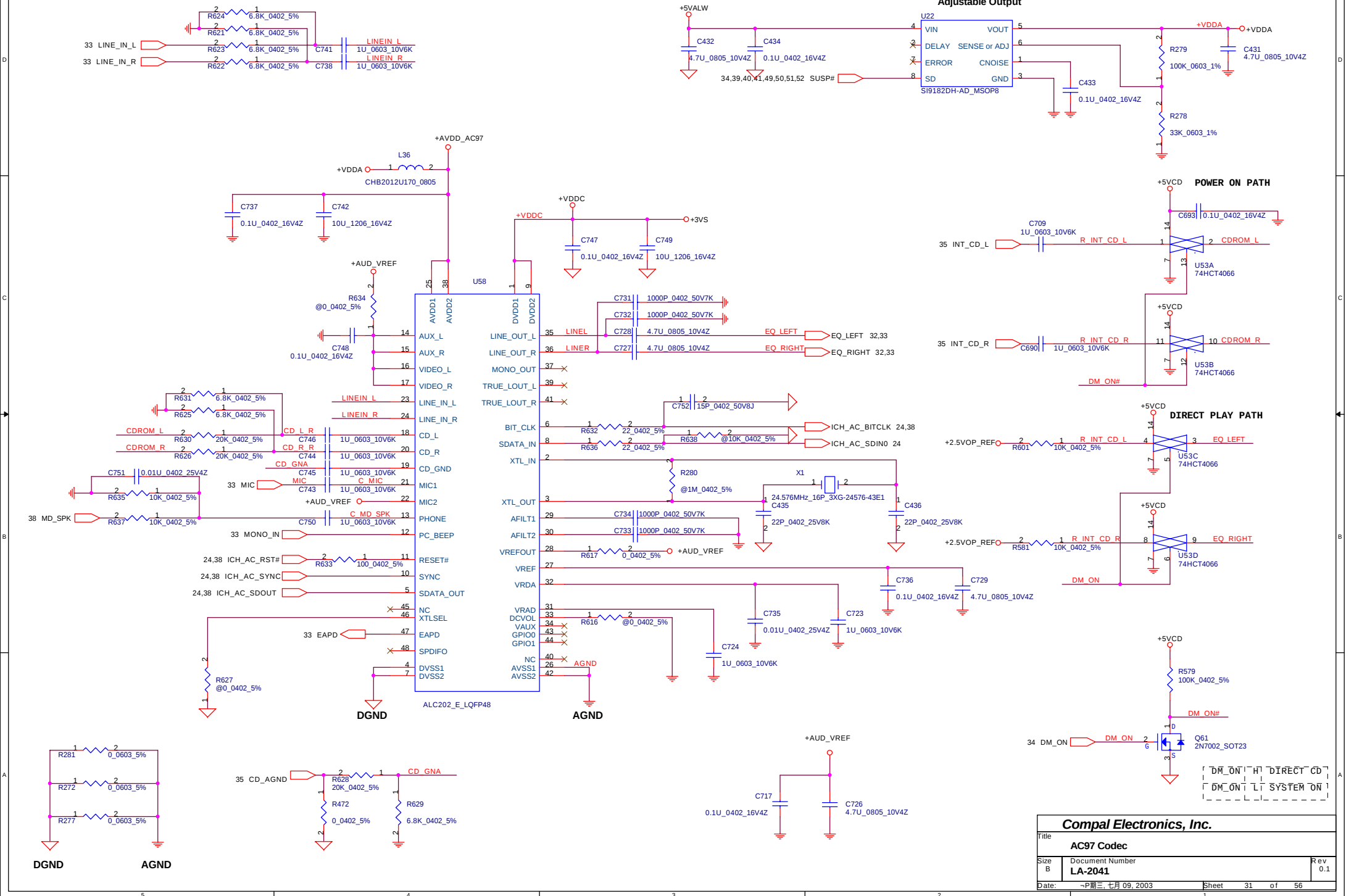
Compal Electronics, Inc.		
Title ICH5-IDE/LPC/PM/GPIO/USB		
Size	Document Number	Rev 0.1
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Date	~P 星期三, 七月 09, 2003	Sheet 24 of 56

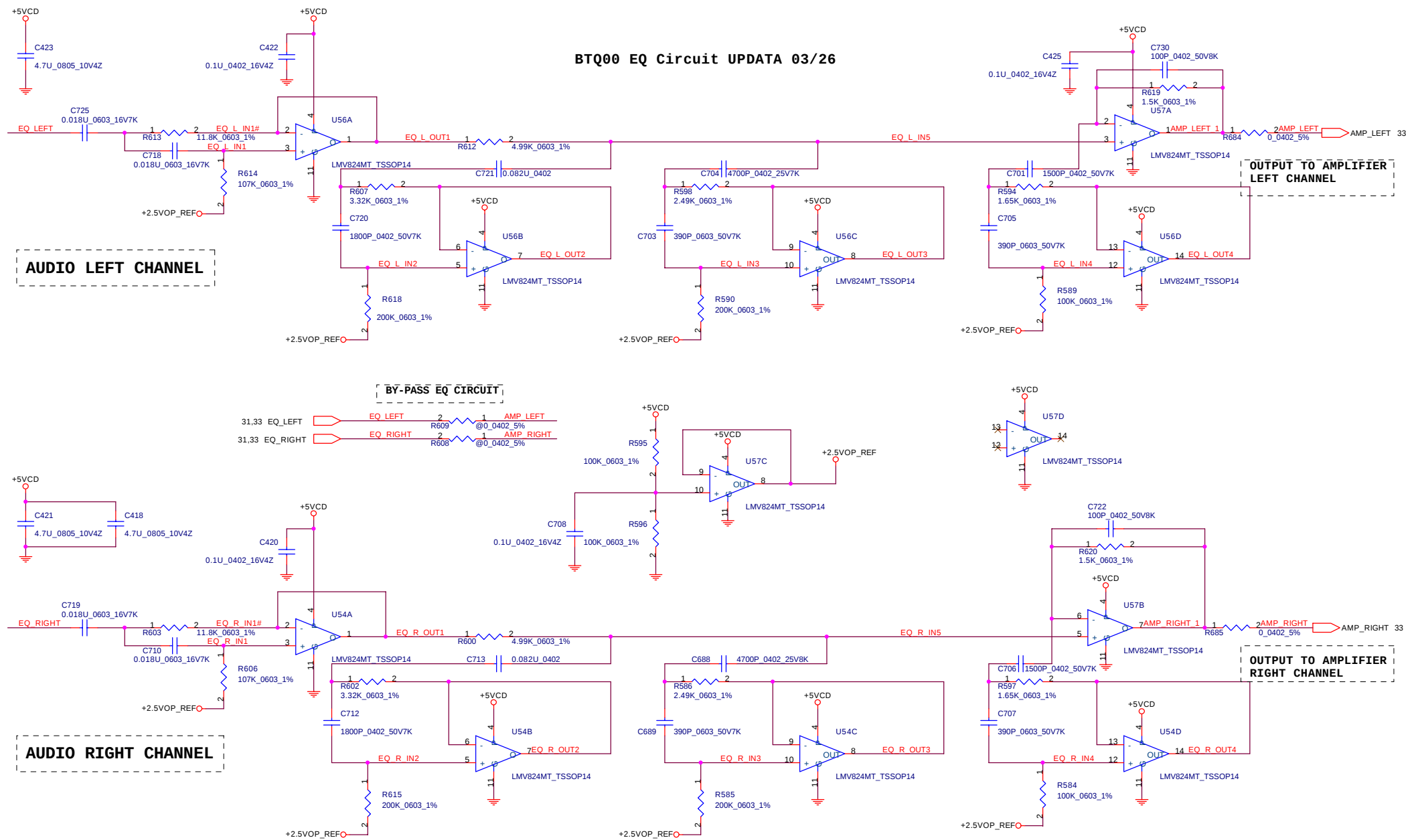
Compal Electronics, Inc.



AC97 Codec

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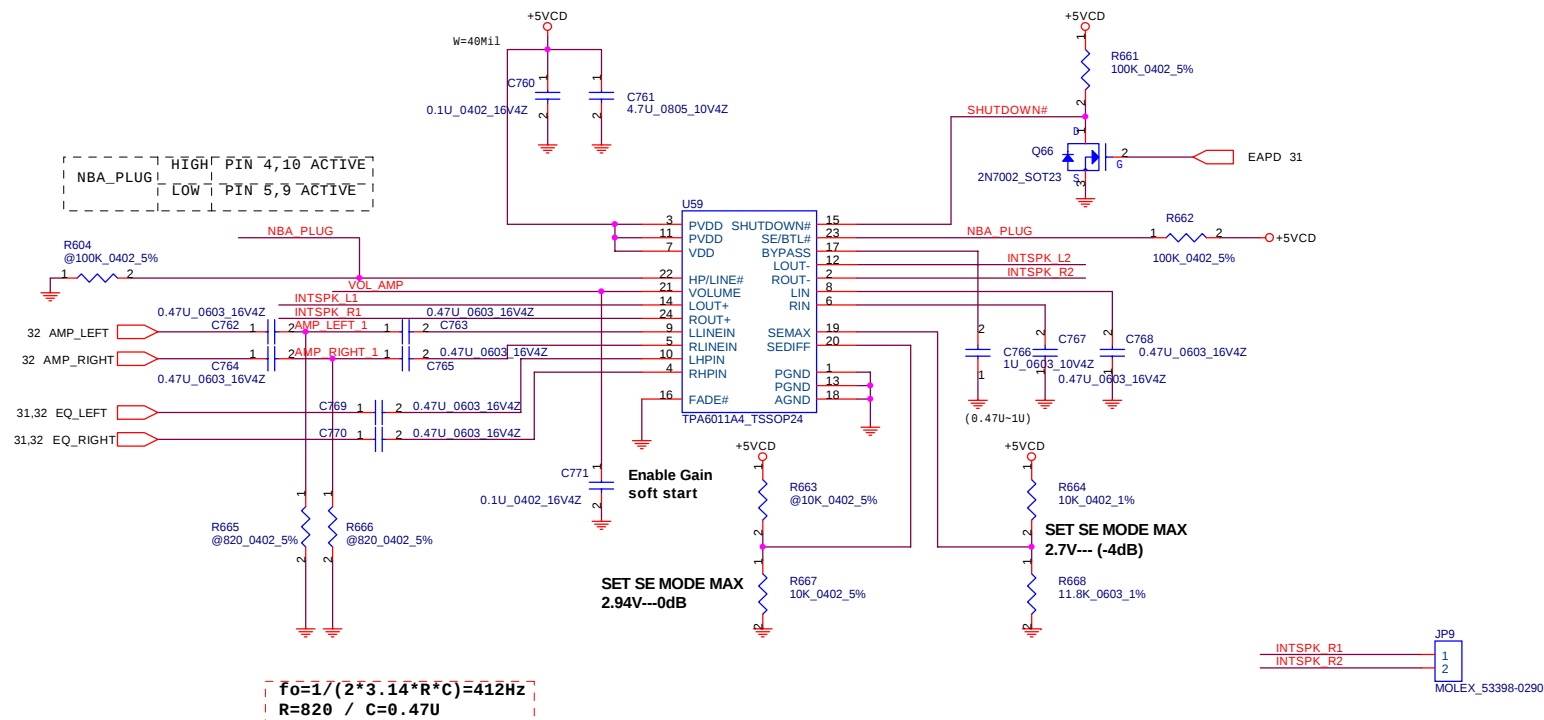




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Title			
HAREWARE EQ			
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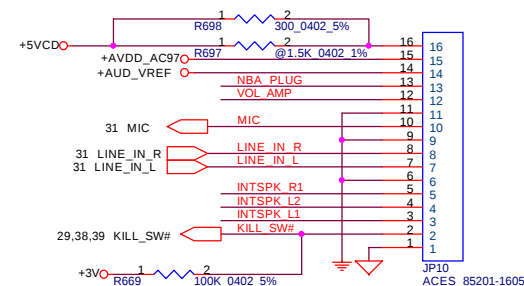
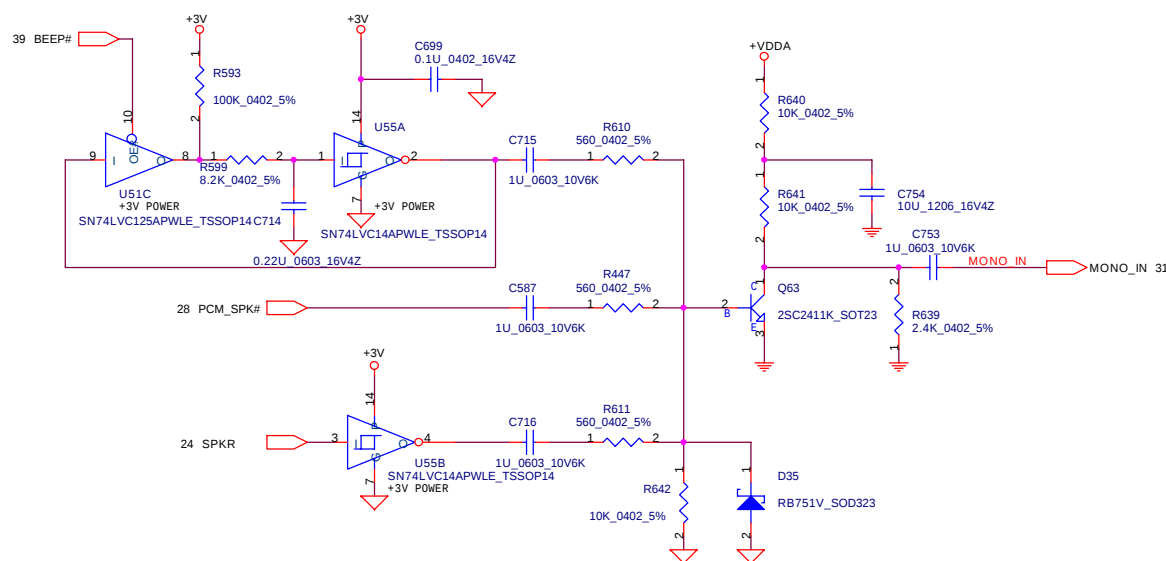
Audio AMP



AUDIO Board Conn.

R697(1.5K)-----10dB

R698(300)-----14dB



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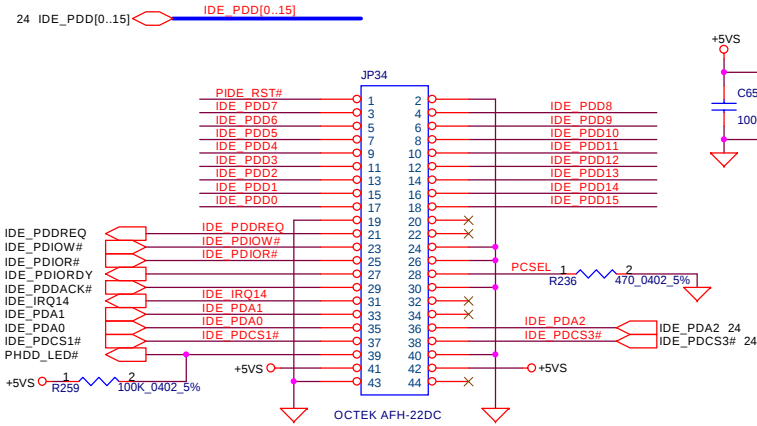
AMP & Audio Jack

Document Number	LA-2041
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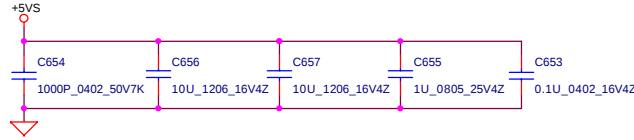
Rev	0.1
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HDD CONNECTOR



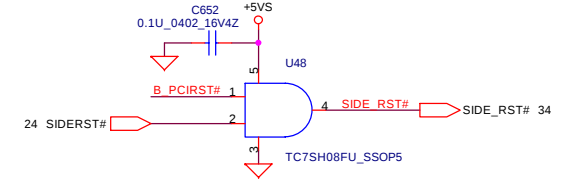
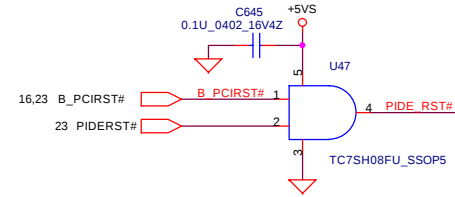
Place caps. near HDD CONN.



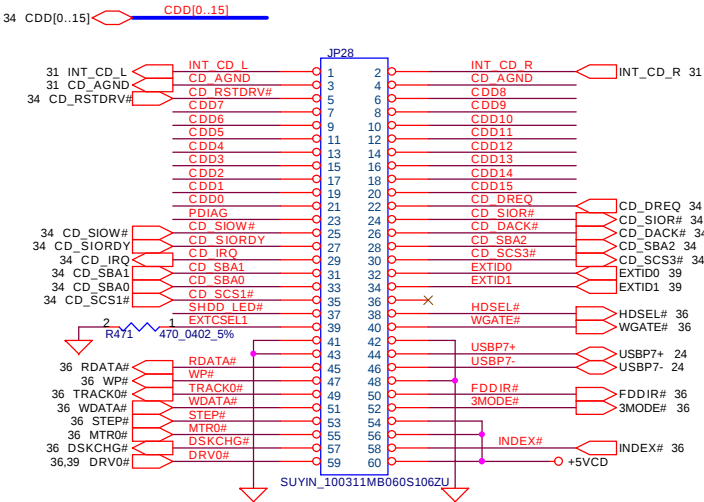
EXTID1	EXTID0	Module
0	0	CDROM
0	1	FDD
1	0	HDD
1	1	TV Tuner/No Module

EXTID3	EXTID2	Module
0	0	CDROM
0	1	FDD
1	0	HDD
1	1	TV Tuner/No Module

IDE,CD-ROM Module CONN.

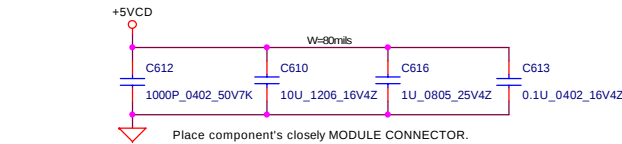
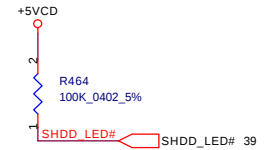
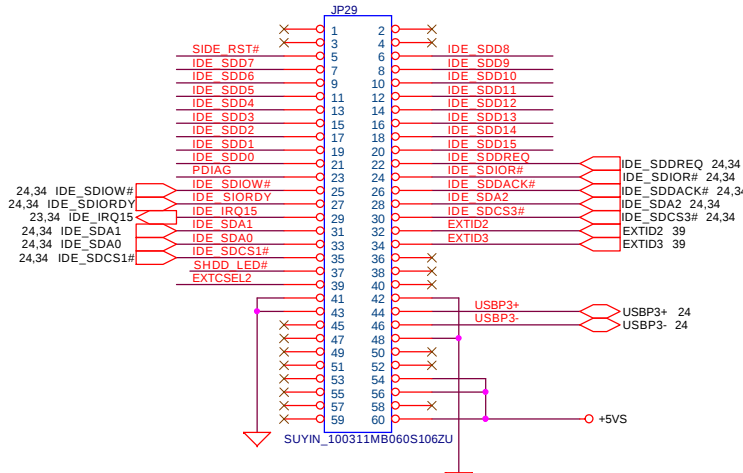


Main Module Conn. (Master)

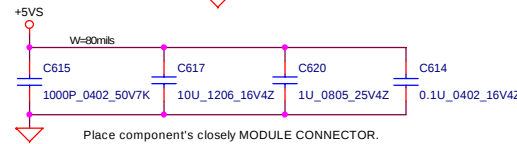
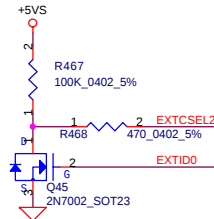
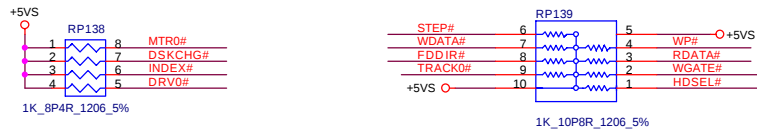


24,34 IDE_SDD[0..15] IDE_SDD[0..15]

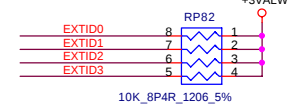
2nd Module Conn. (Slave)



Place component's closely MODULE CONNECTOR.



Place component's closely MODULE CONNECTOR.

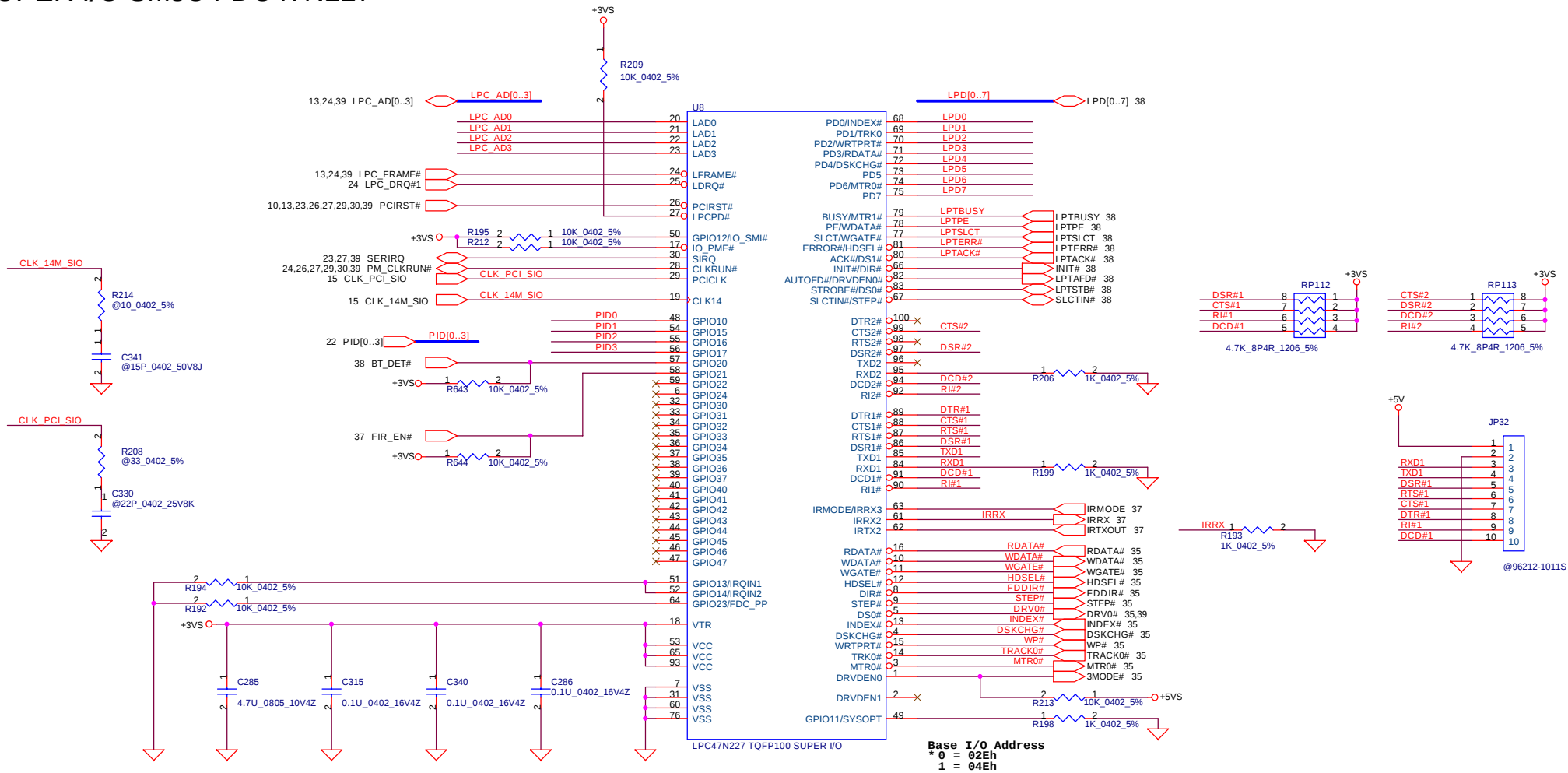


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IDE/FDD MODULE CONN.			
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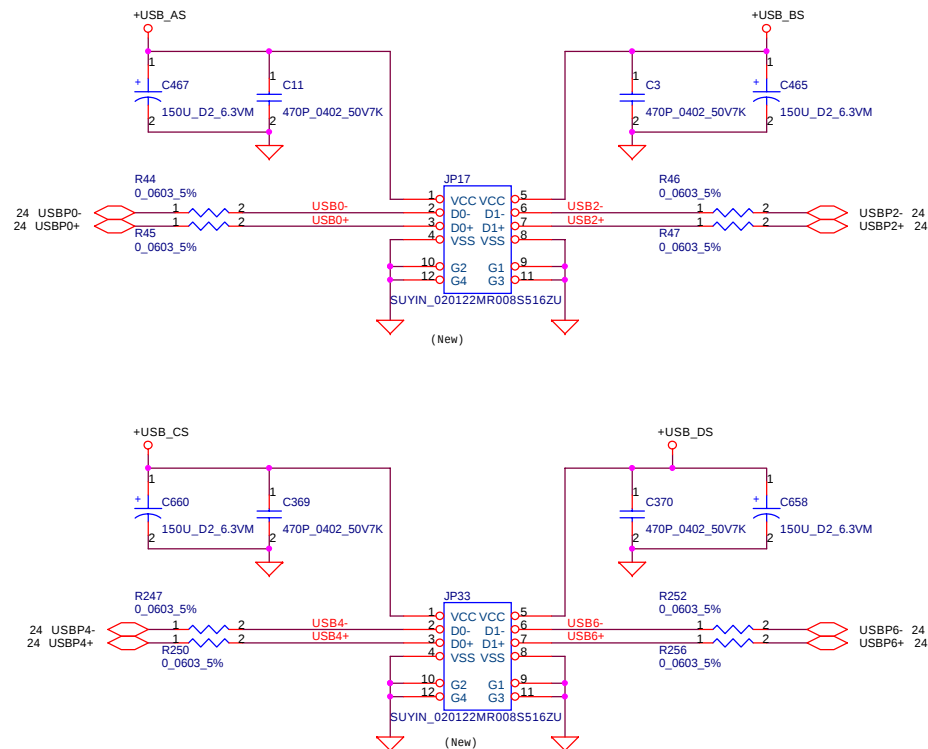
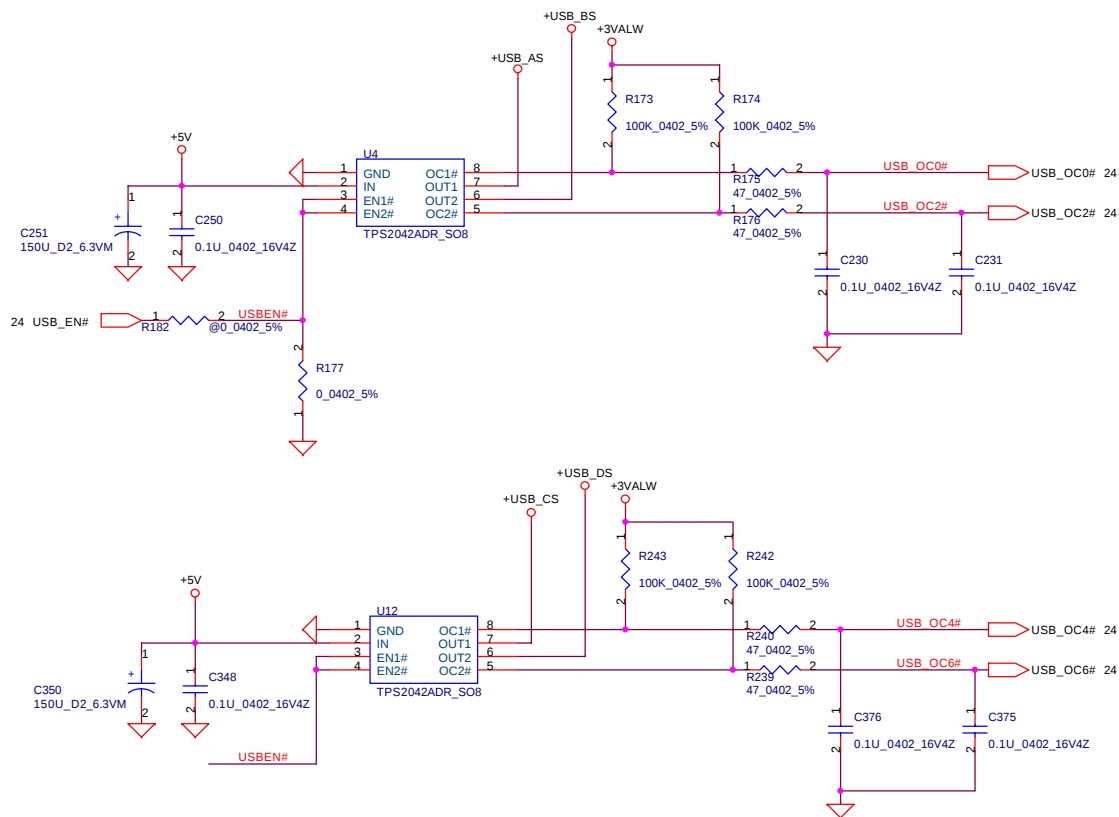
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SUPER I/O SMC FDC47N227

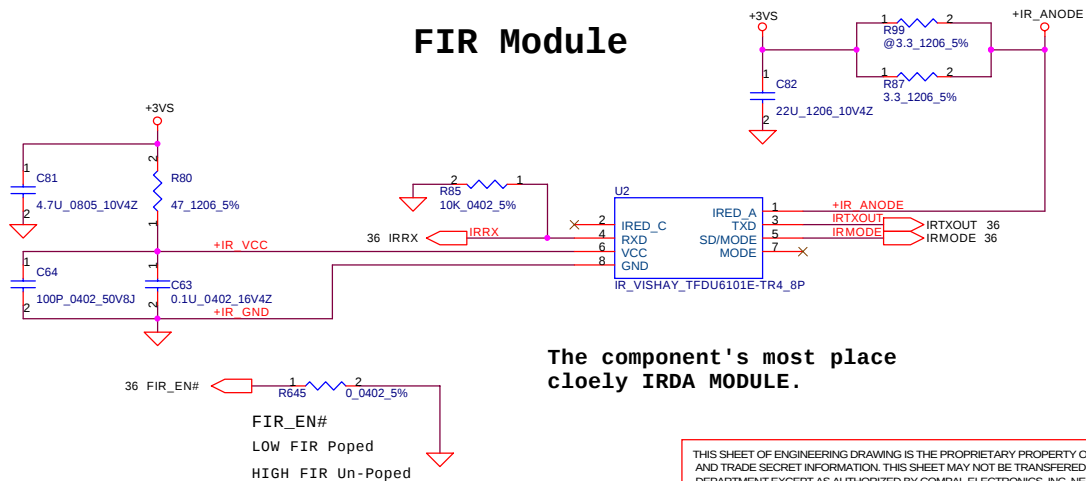


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SUPER I/O			
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FIR Module



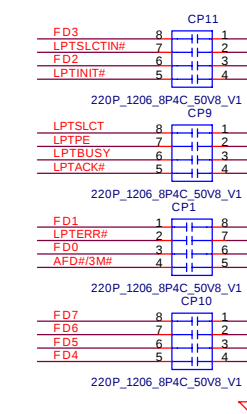
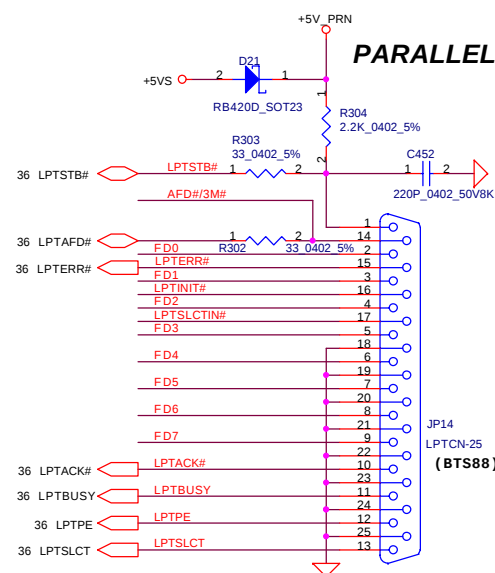
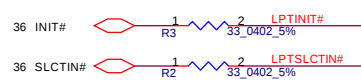
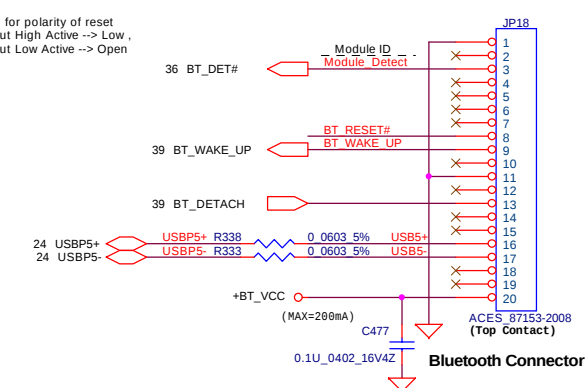
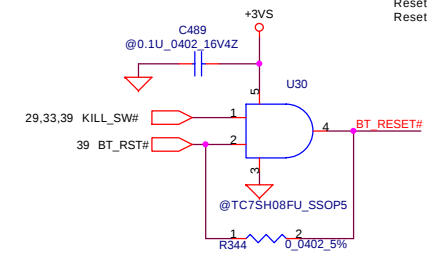
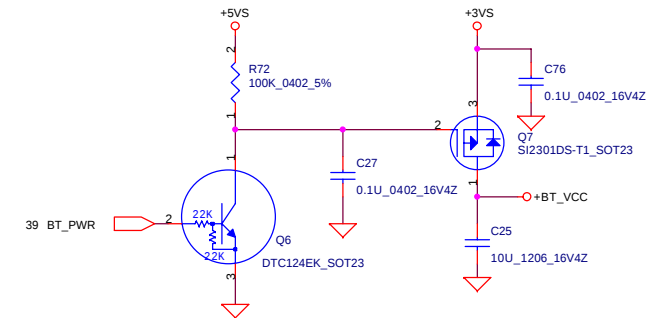
The component's most place
cloely IRDA MODULE.

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Title			
USB Conn.			
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BlueTooth Interface



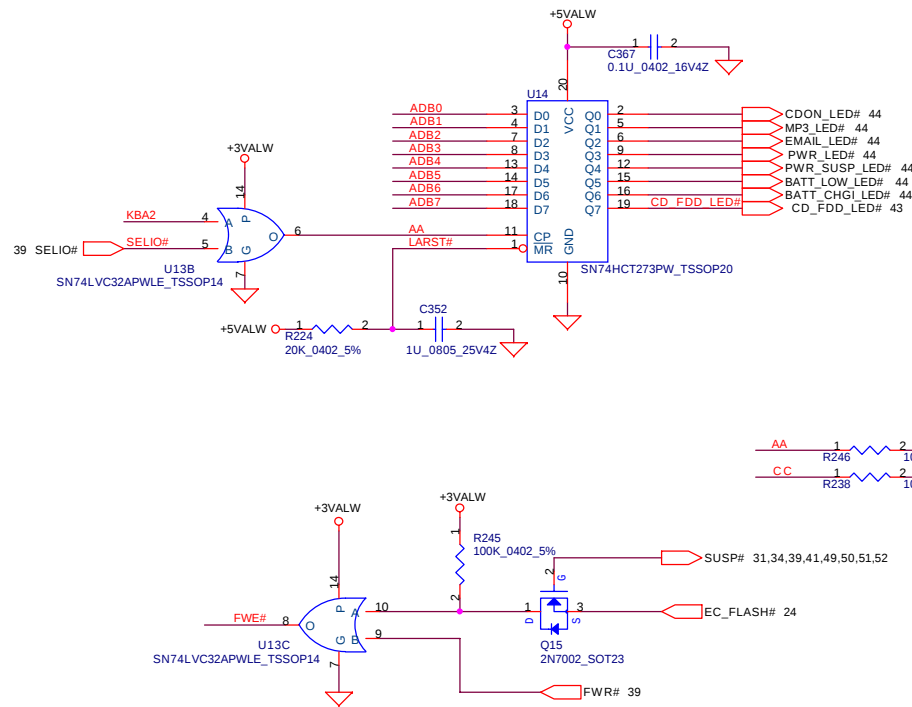
PARALLEL PORT

Bluetooth Connector

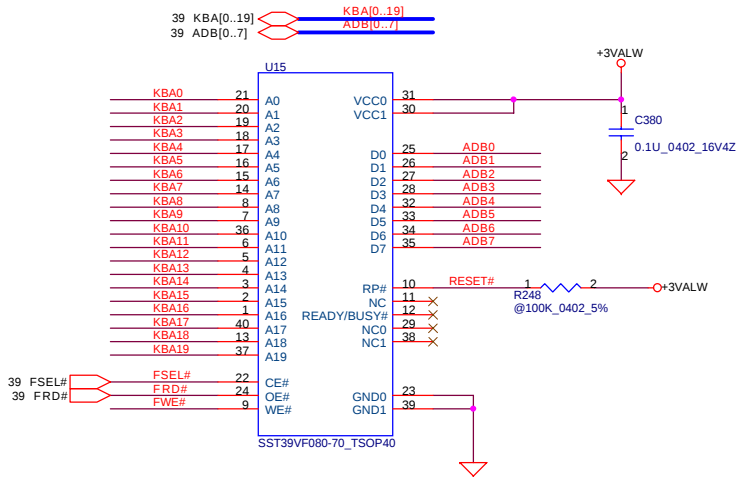
Compal Electronics, Inc.

Title	PARALLEL/MDC PORT		
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Date:	平成三、七月 09, 2003	Sheet	38 of 56

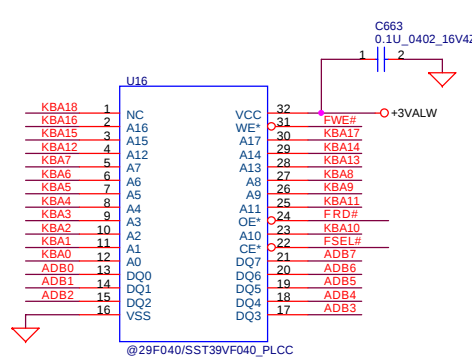




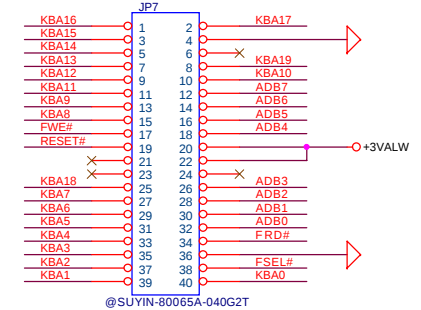
1MB Flash ROM



512KB Flash ROM



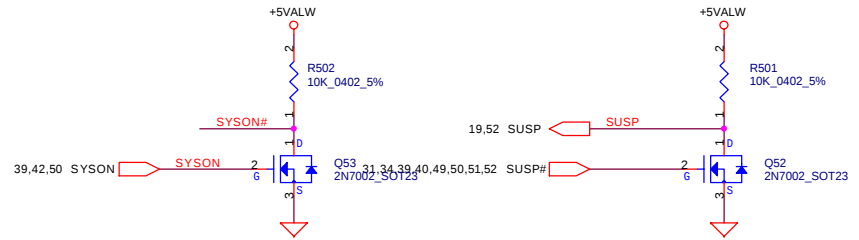
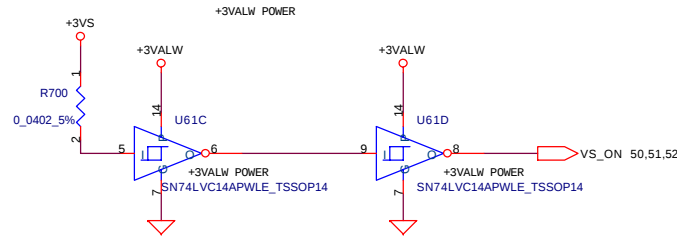
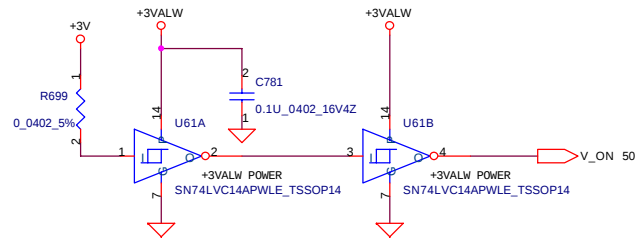
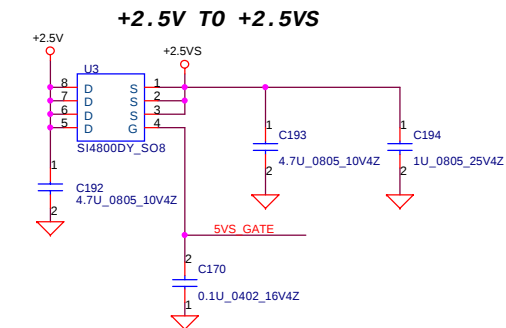
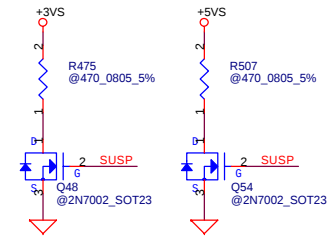
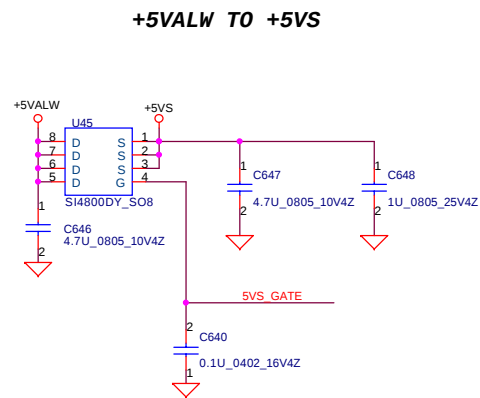
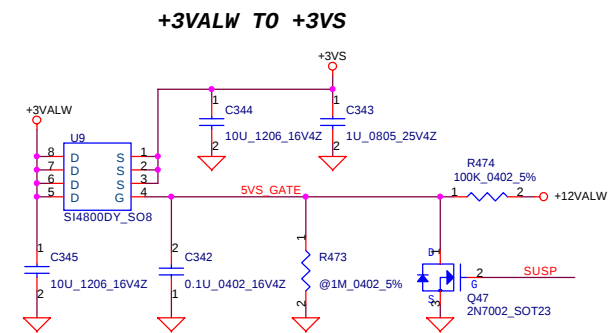
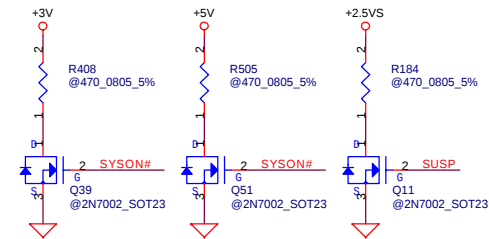
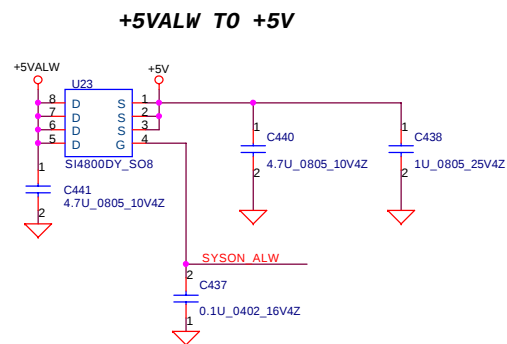
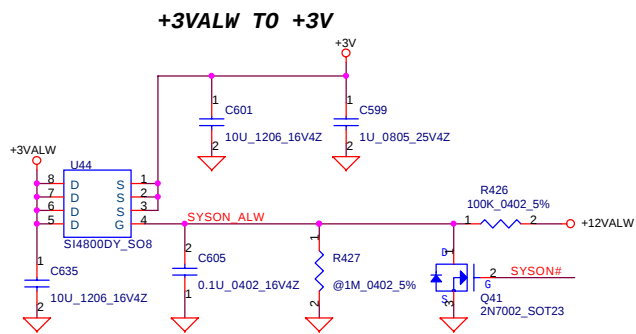
Flash ROM Socket Conn.



Compal Electronics, Inc.

Title			
BIOS & EXT. I/O PORT			
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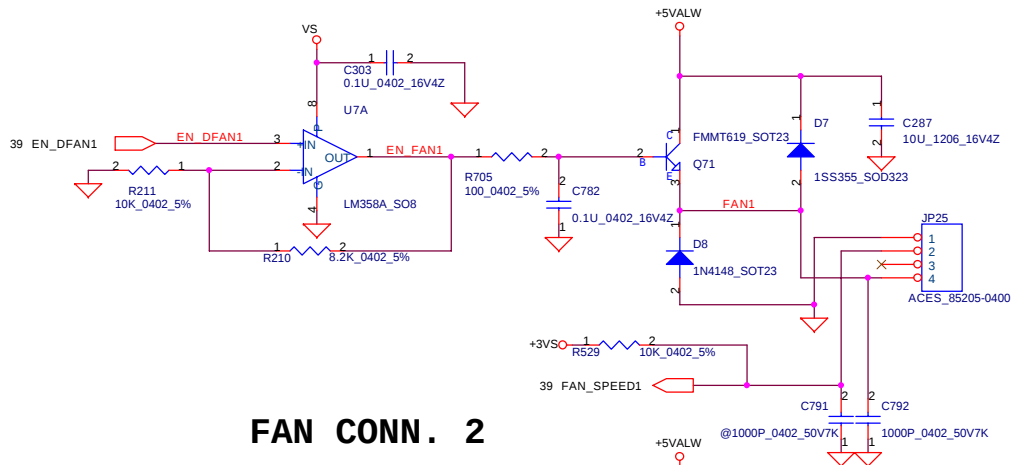
POWER CONTROL CKT

Document Number LA-2041

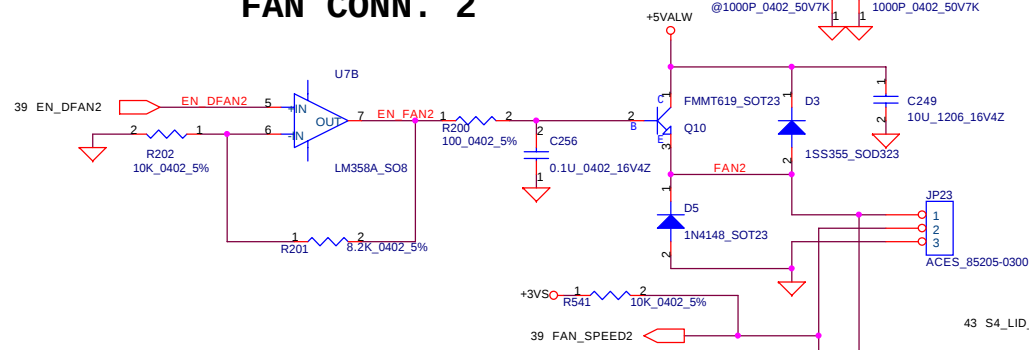
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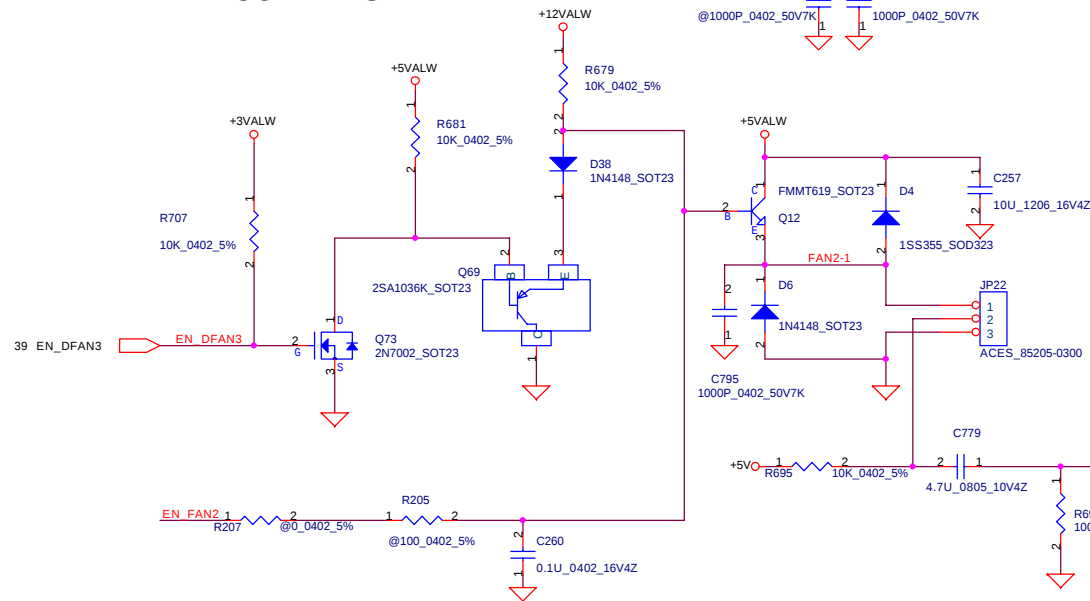
FAN CONN. 1



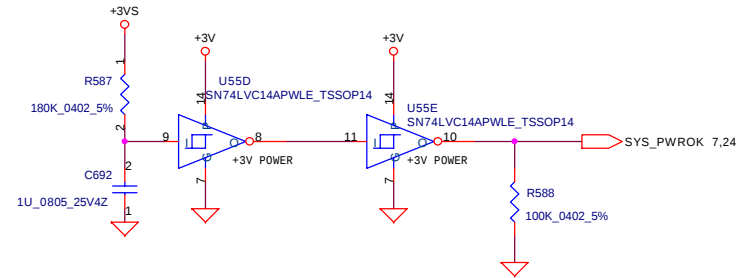
FAN CONN. 2



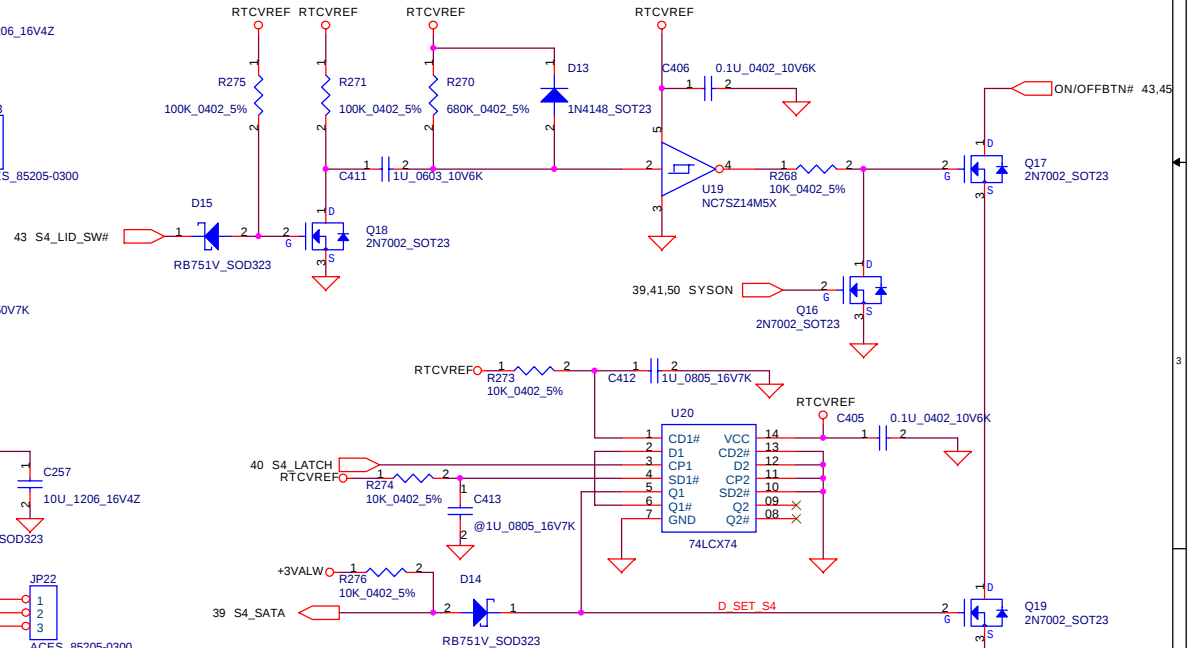
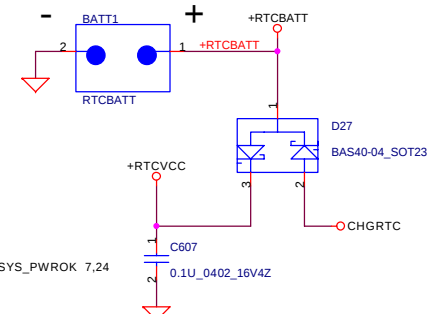
FAN CONN. 3



Power ON Circuit

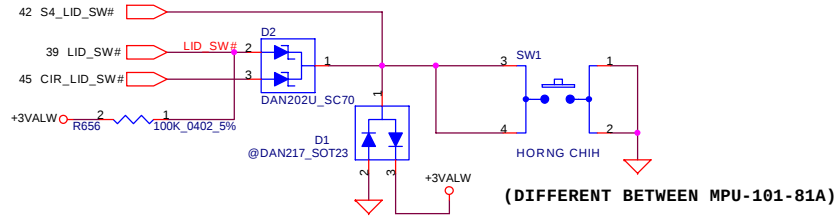


RTC Battery

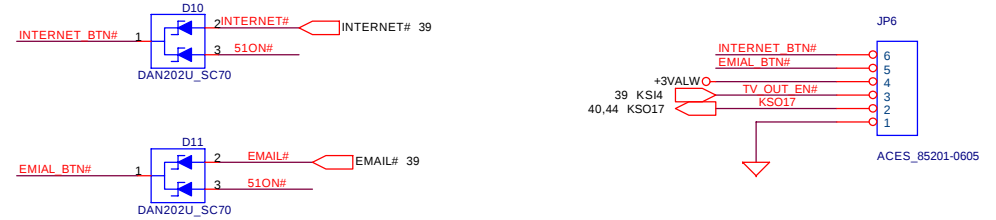


Compal Electronics, Inc.			
Title			
Power OK/Reset/RTC battery/Lid Switch/Int. KB			
Size	Document Number		Rev
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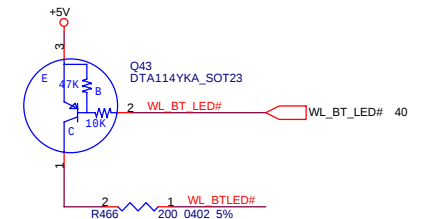
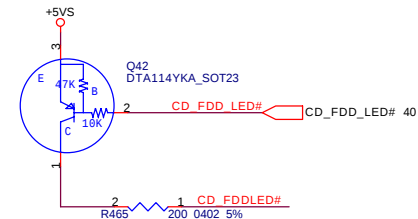
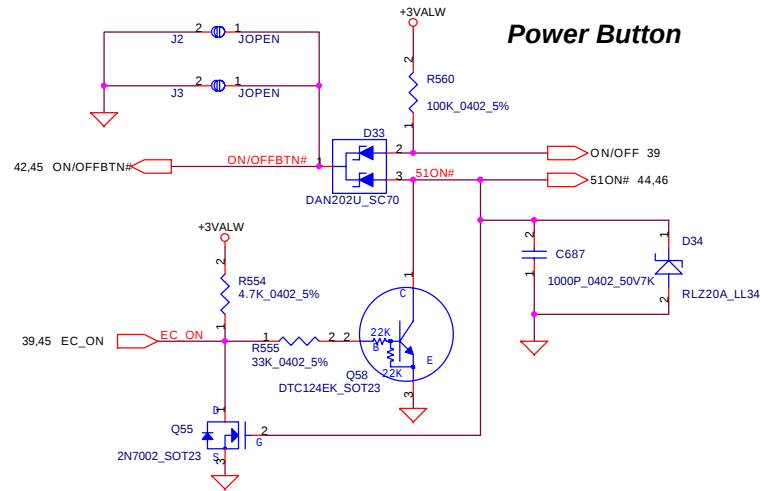
LID Switch



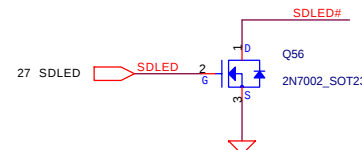
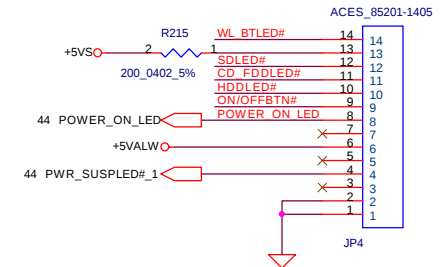
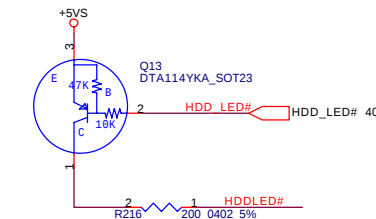
Button FPC Conn.



Power Button



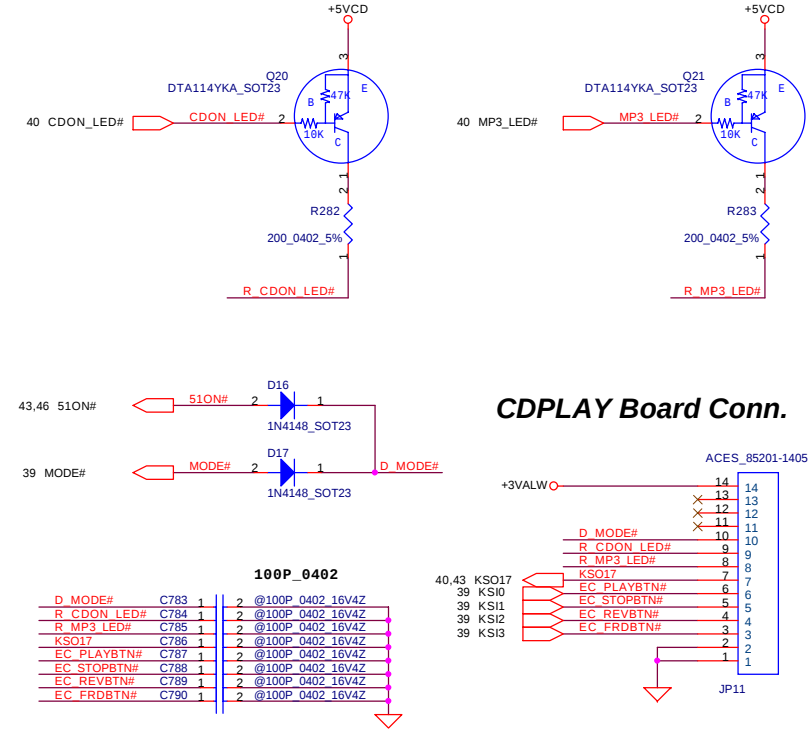
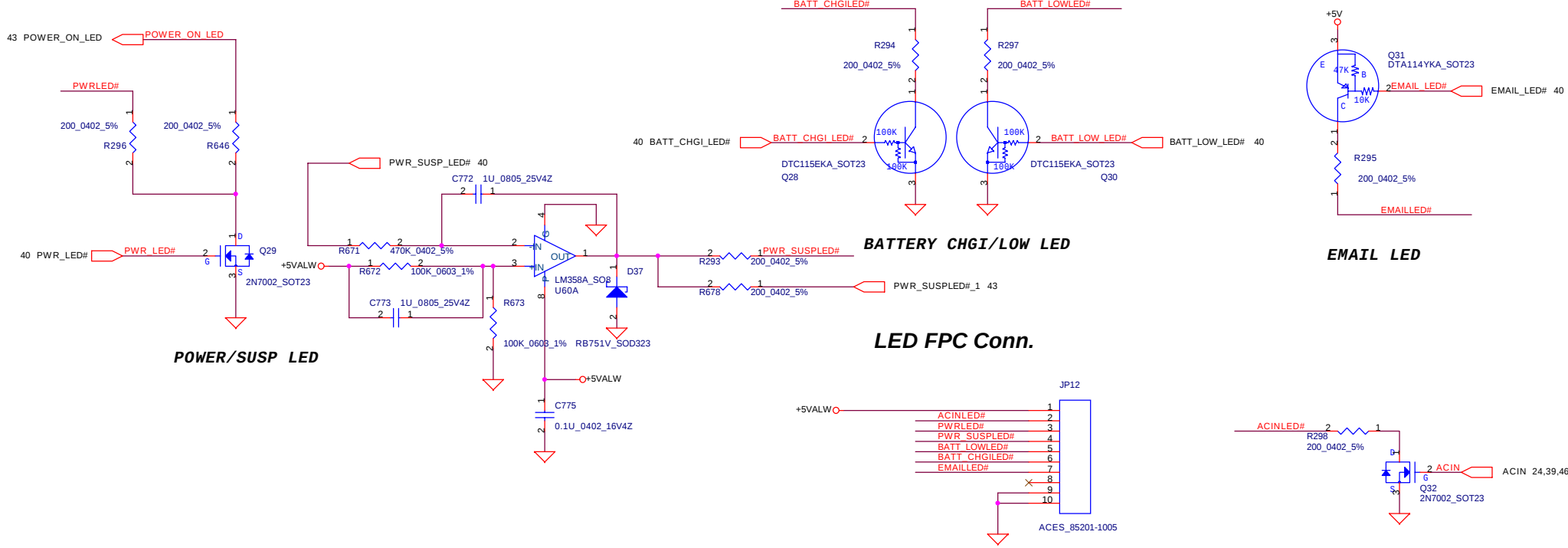
Power FPC Conn.



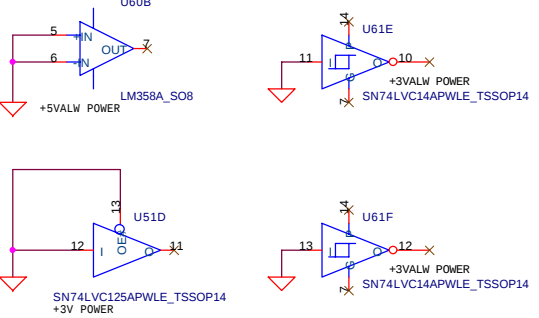
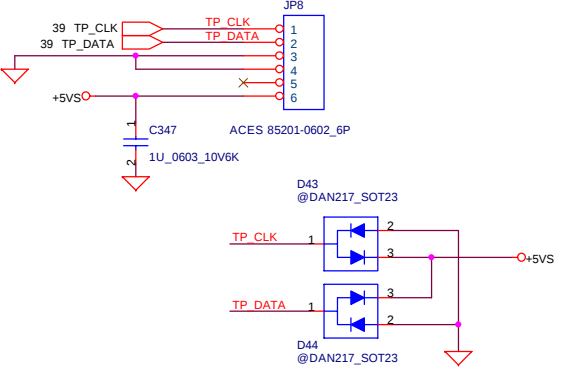
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Title		
Switches & Connectors		
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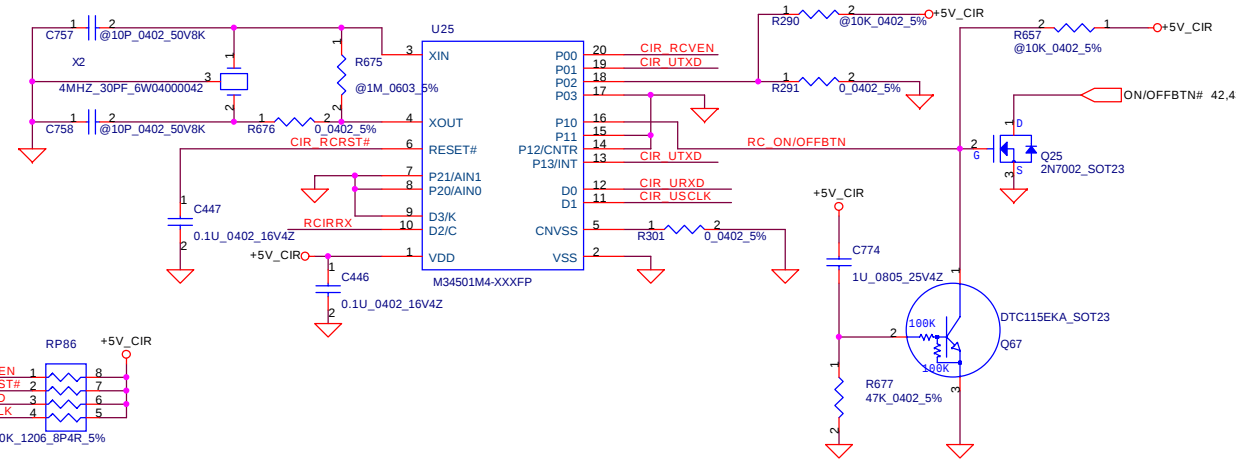
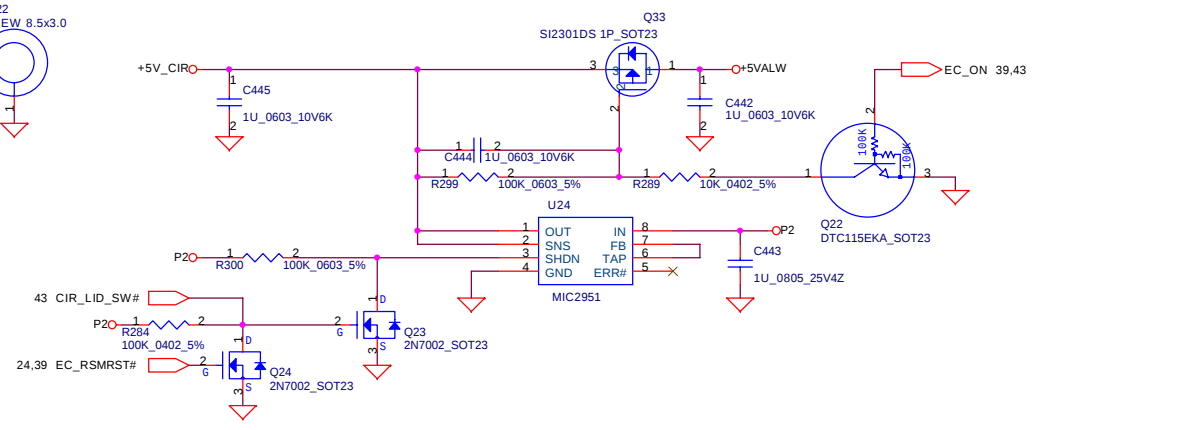
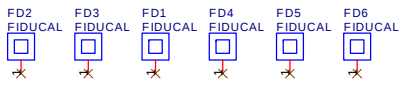
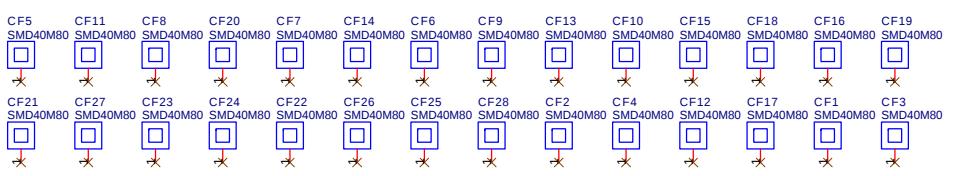
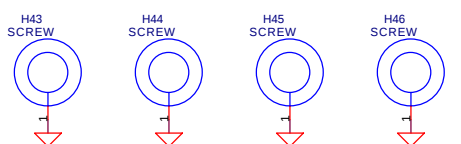
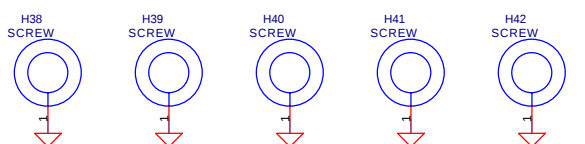
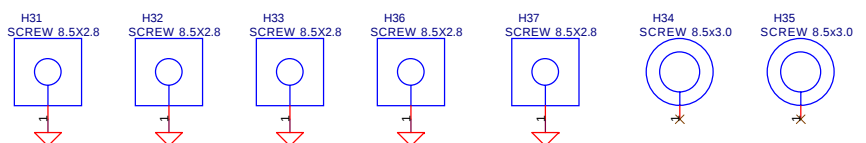
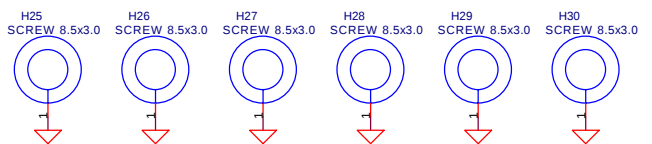
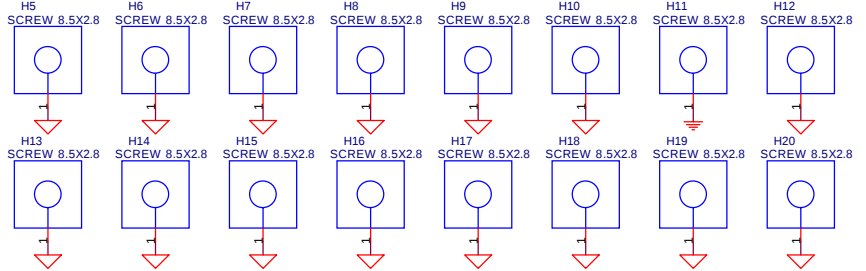
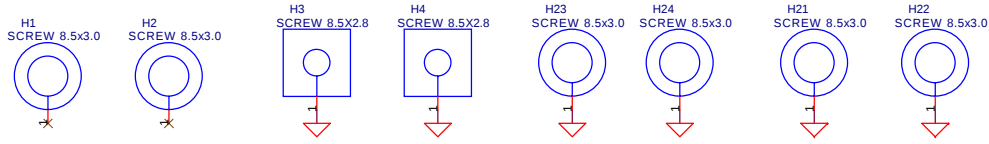


Touch Pad Connector

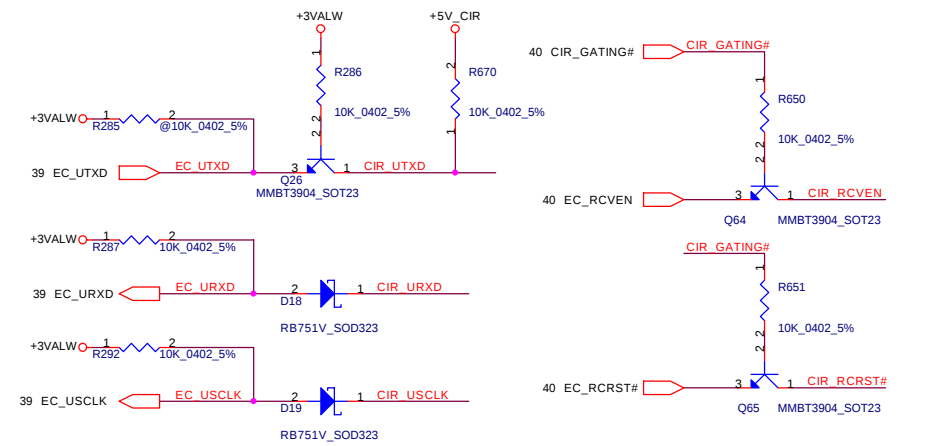
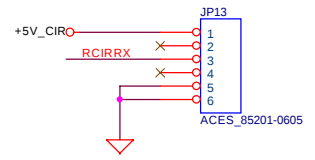


Compal Electronics, Inc.			
Switches & Connectors			
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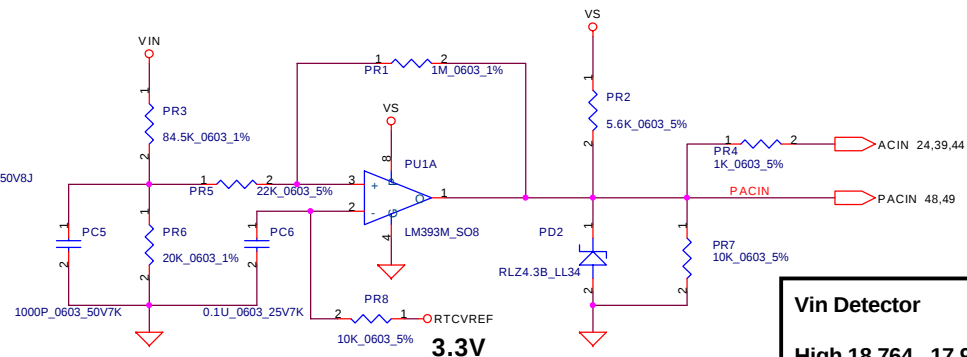
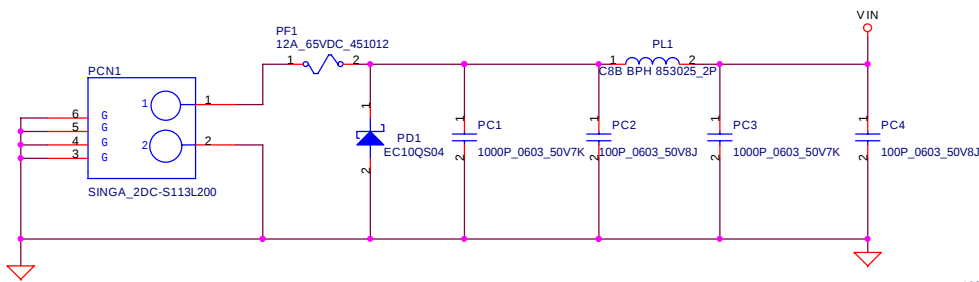


CIR Reciever Board Conn.

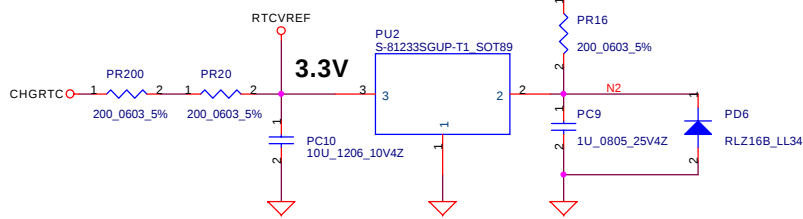
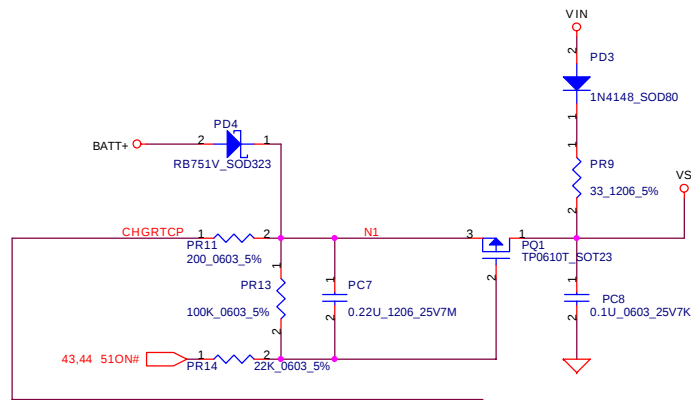


Compal Electronics, Inc.		
Title	CIR & Screws	
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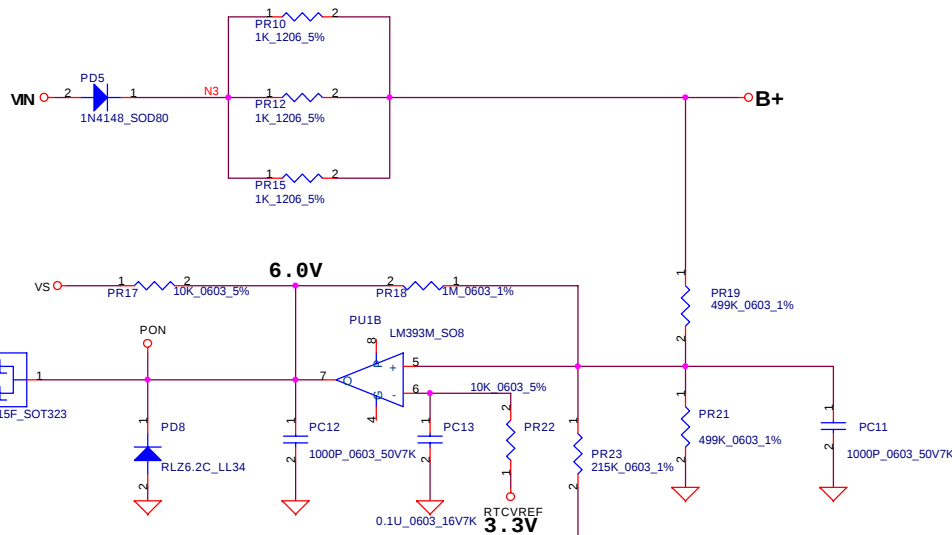
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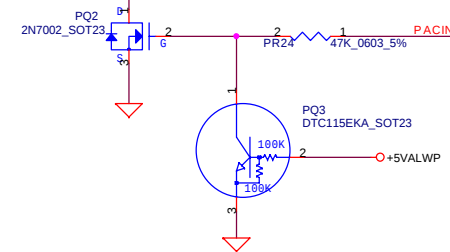
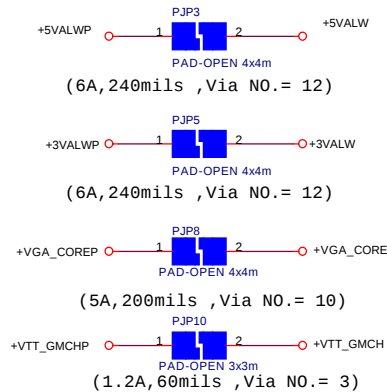
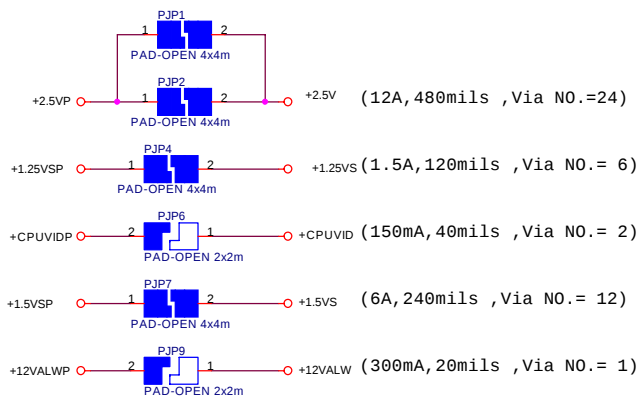
Vin Detector		
High	18.764	17.901
Low	17.745	16.038



47.49 MAINPWON
48 ACON



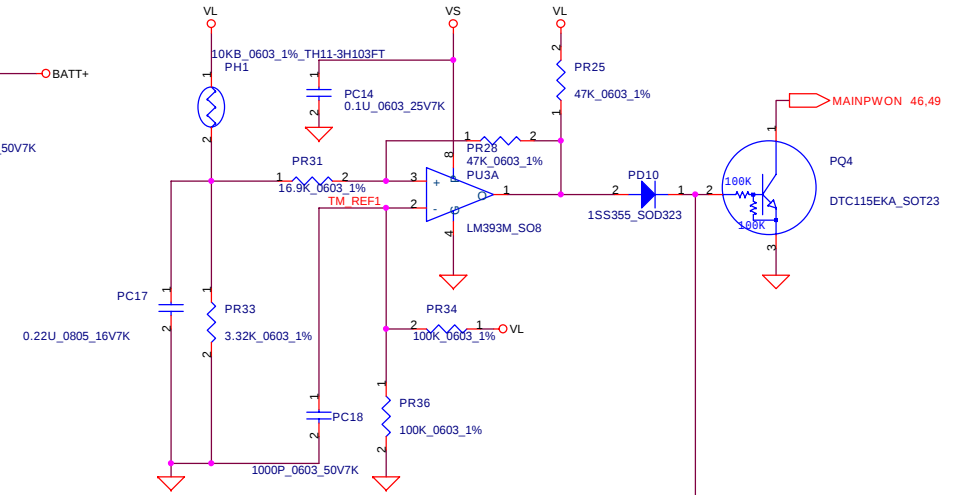
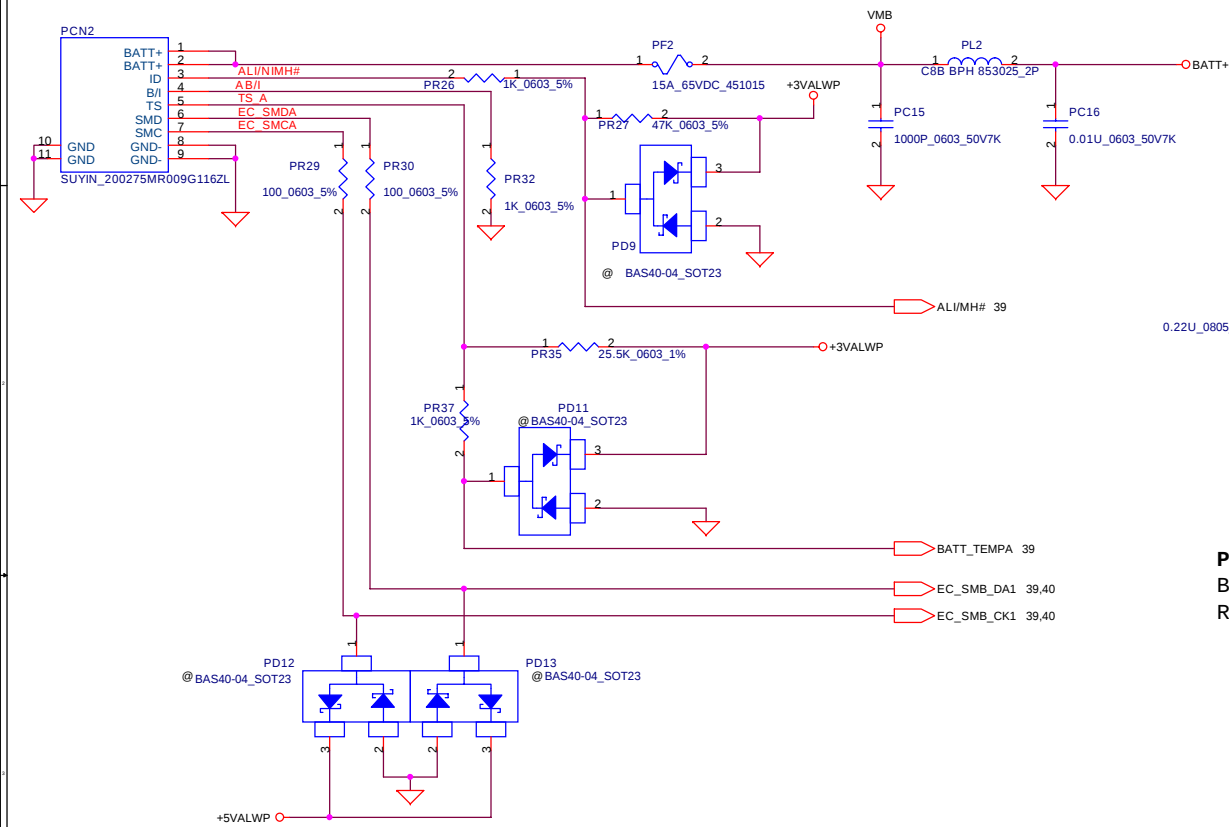
Precharge detector		
15.34	15.90	16.48
13.13	13.71	14.20



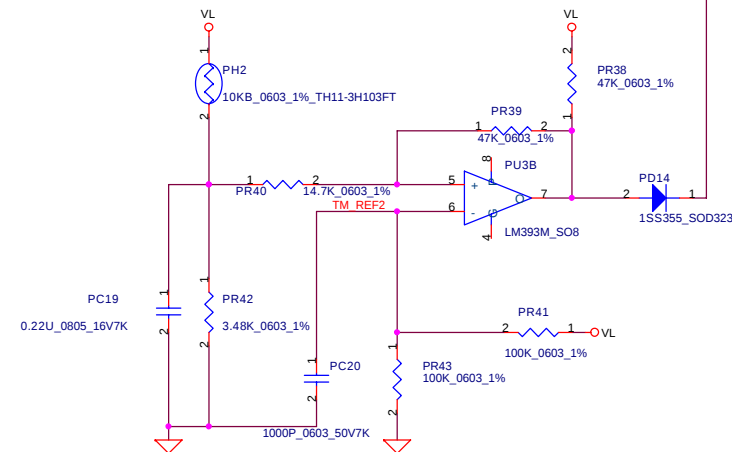
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Compal Electronics, Inc.		
Title		
DCIN & DETECTOR		
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PH1 under CPU botten side :
CPU thermal protection at 84 degree C
Recovery at 45 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 45 degree C



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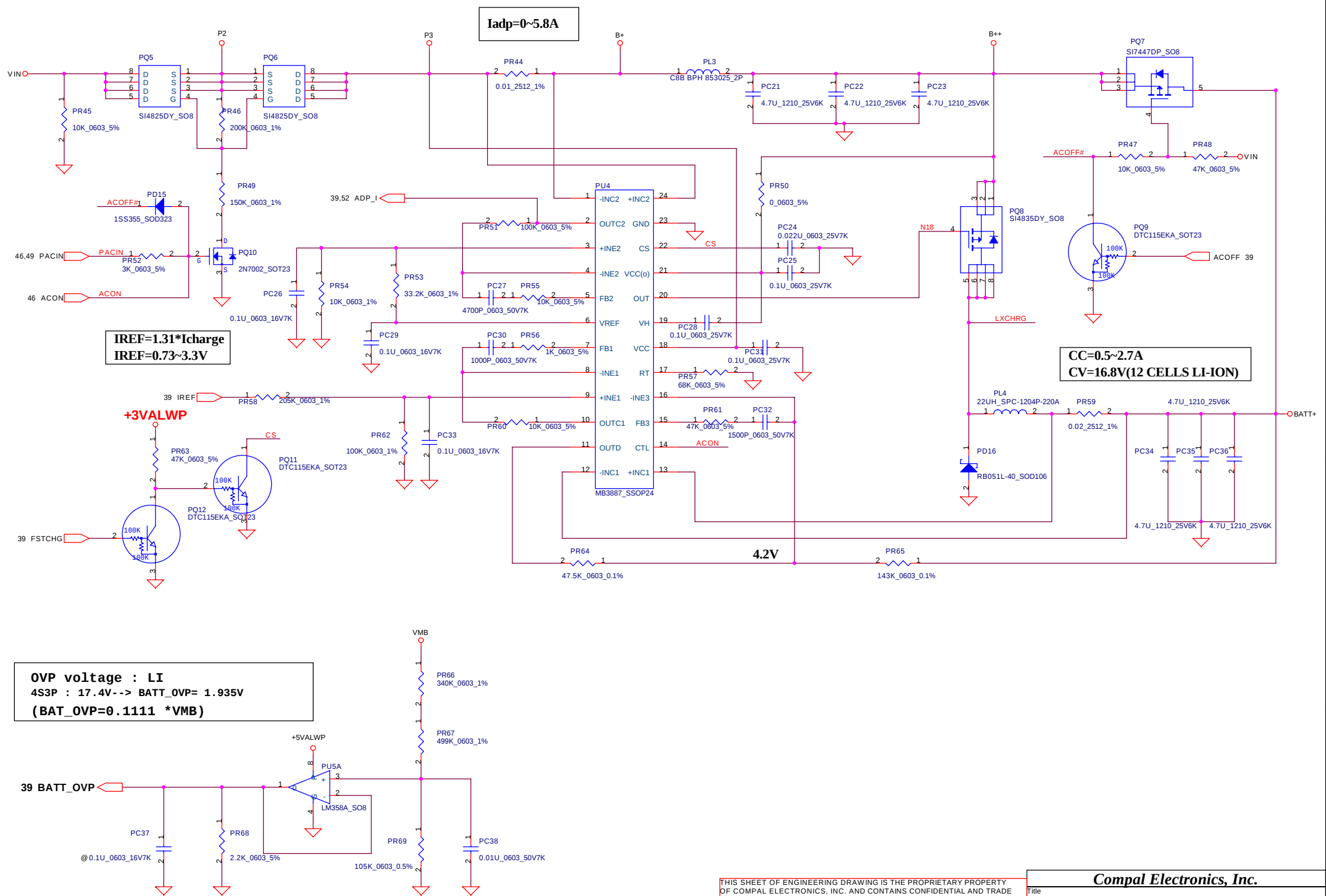
Compal Electronics, Inc.

Title **BATTERY CONN/OTP**

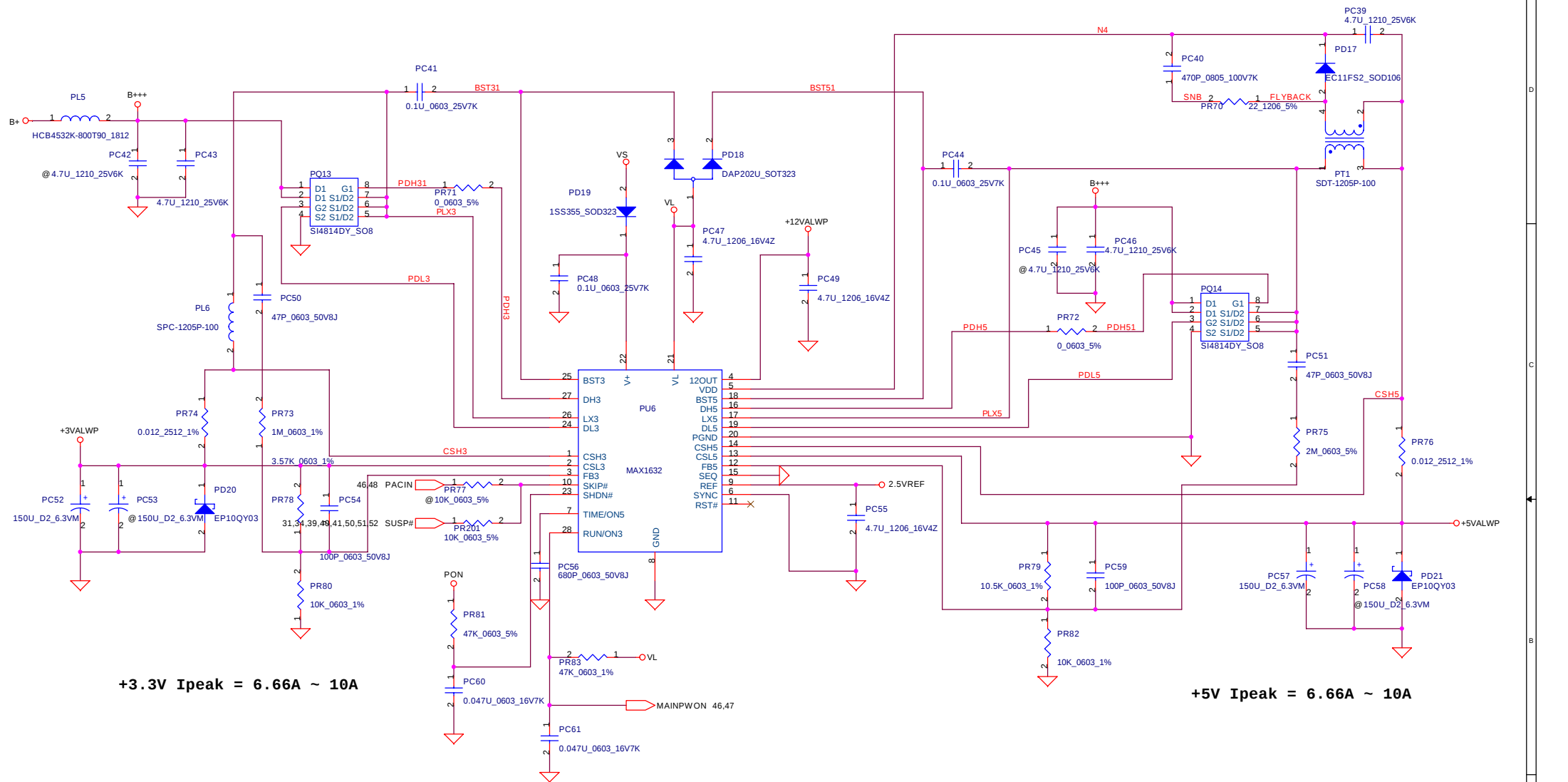
Size	Document Number
	LA-2041

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0.1	

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+3.3V Ipeak = 6.66A ~ 10A

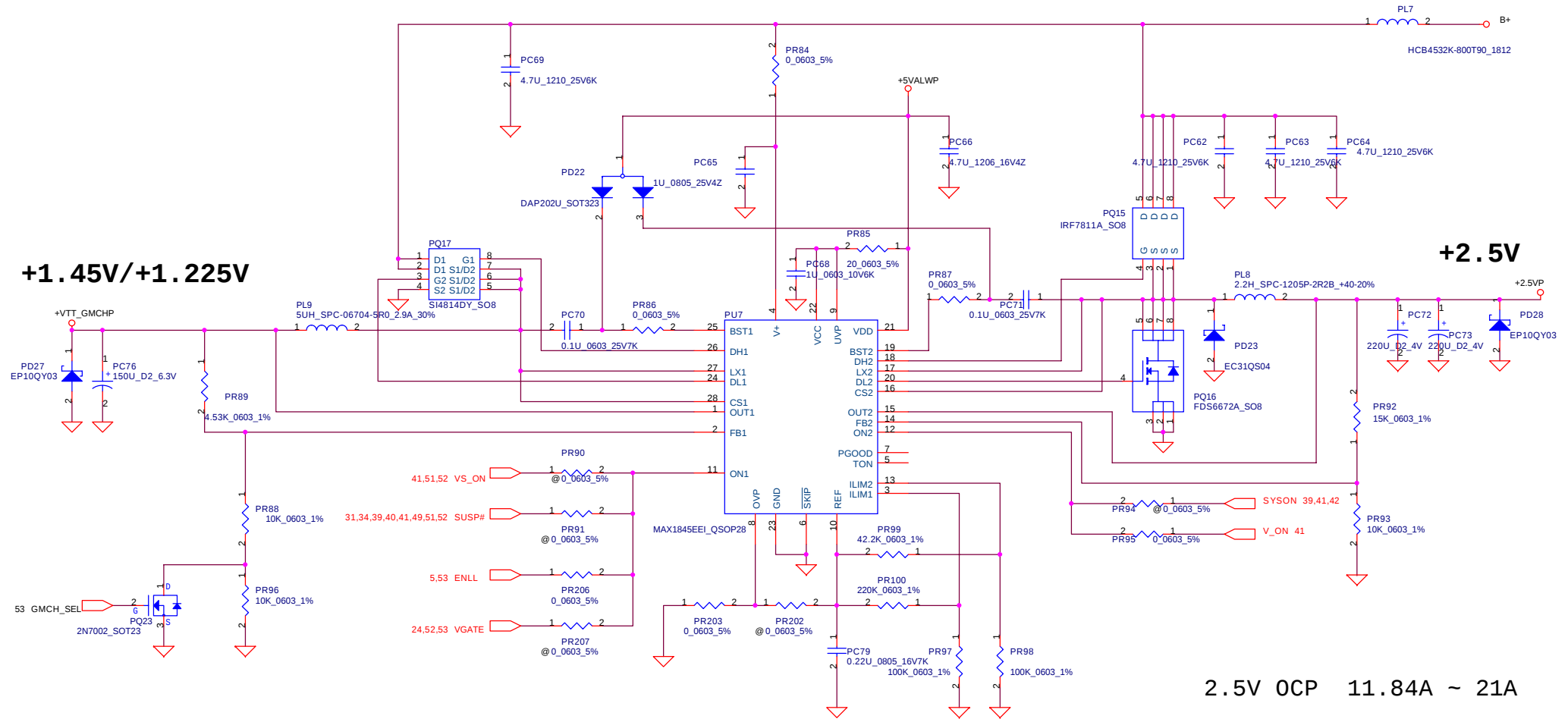
+5V Ipeak = 6.66A ~ 10A

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Compal Electronics, Inc.		
Title 5V/3.3V/12V		
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+2.5V/+VTT_GMCHP

+1.45V/+1.225V



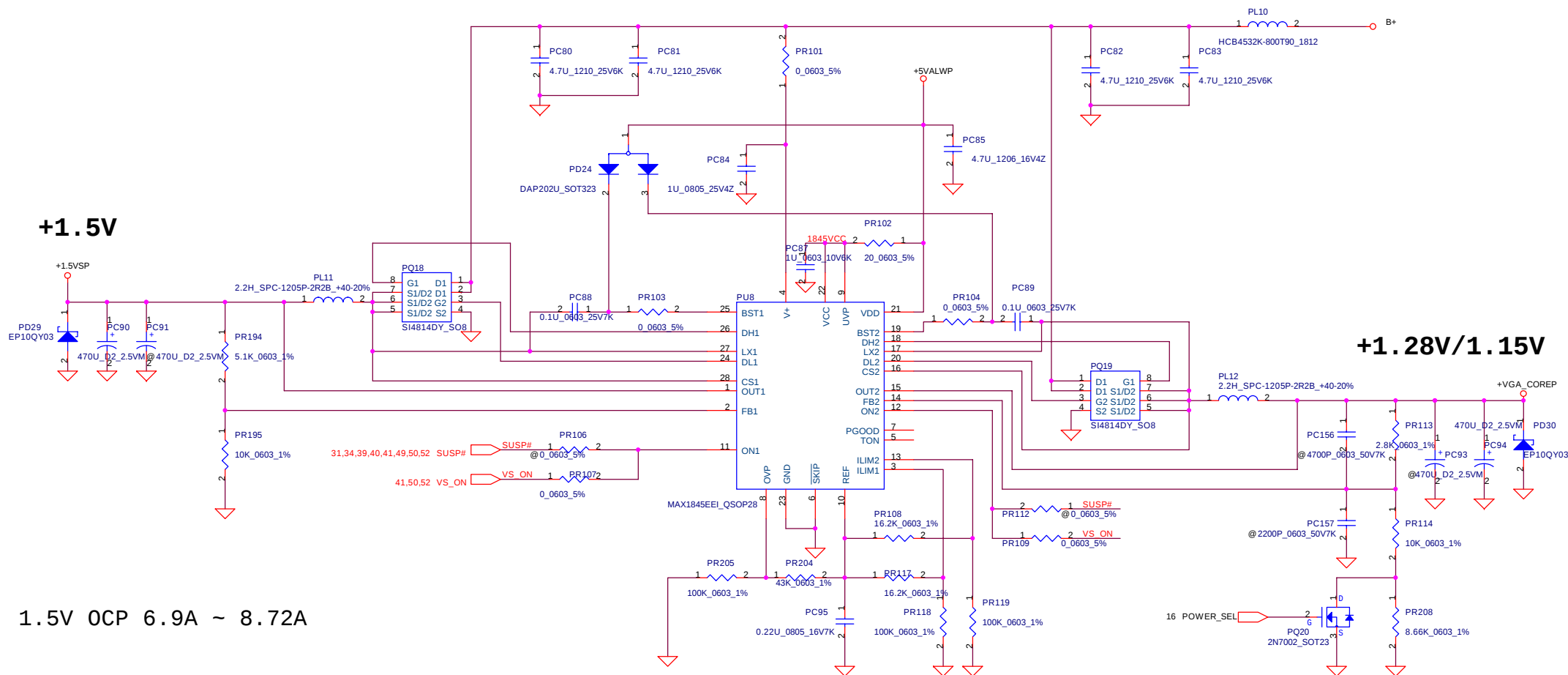
2.5V OCP 11.84A ~ 21A

GMCH_SEL=0 PRESCOTT VTT_GMCH=1.225V OCP 1.92A ~ 3.71A

GMCH_SEL=1 NORTHWOOD VTT_GMCH=1.45V OCP 1.98A ~ 3.78A

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Compal Electronics, Inc.			
Title		DDR_25V/VTT_GMCH	
Size		Document Number	
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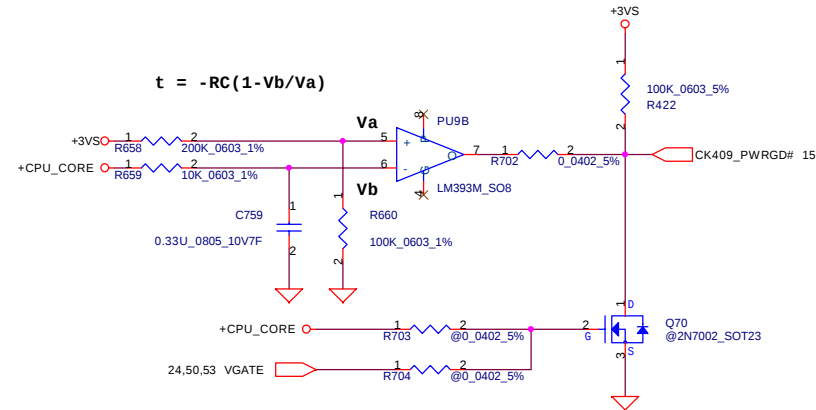
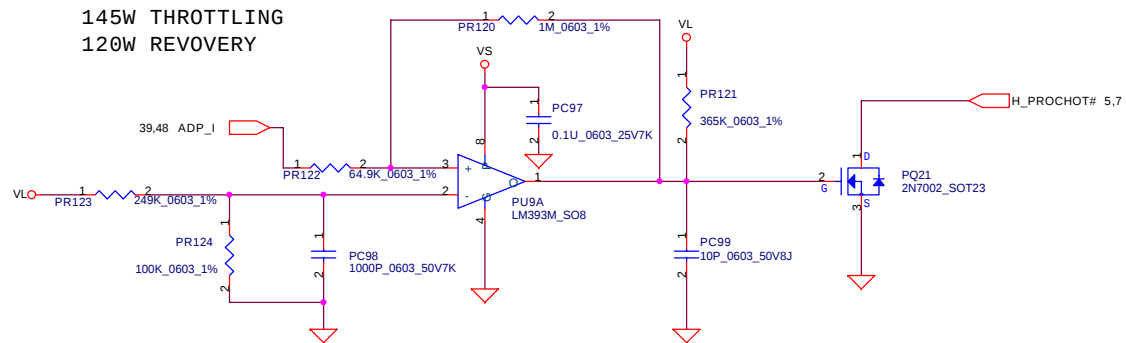
NV34M Ultra			
POWER_SEL=1	VOUT=1.28V	OCP 7.1A ~ 8.9A	PR113=2.8K_0603_1%
POWER_SEL=0	VOUT=1.15V	OCP 6.85A ~ 8.7A	PR208=8.66K_0603_1%

NV31			
POWER_SEL=1	VOUT=1.27V	OCP 7.1A ~ 8.9A	PR113=2.7K_0603_1%
POWER_SEL=0	VOUT=1V	OCP 6.85A ~ 8.7A	Unpop PR208

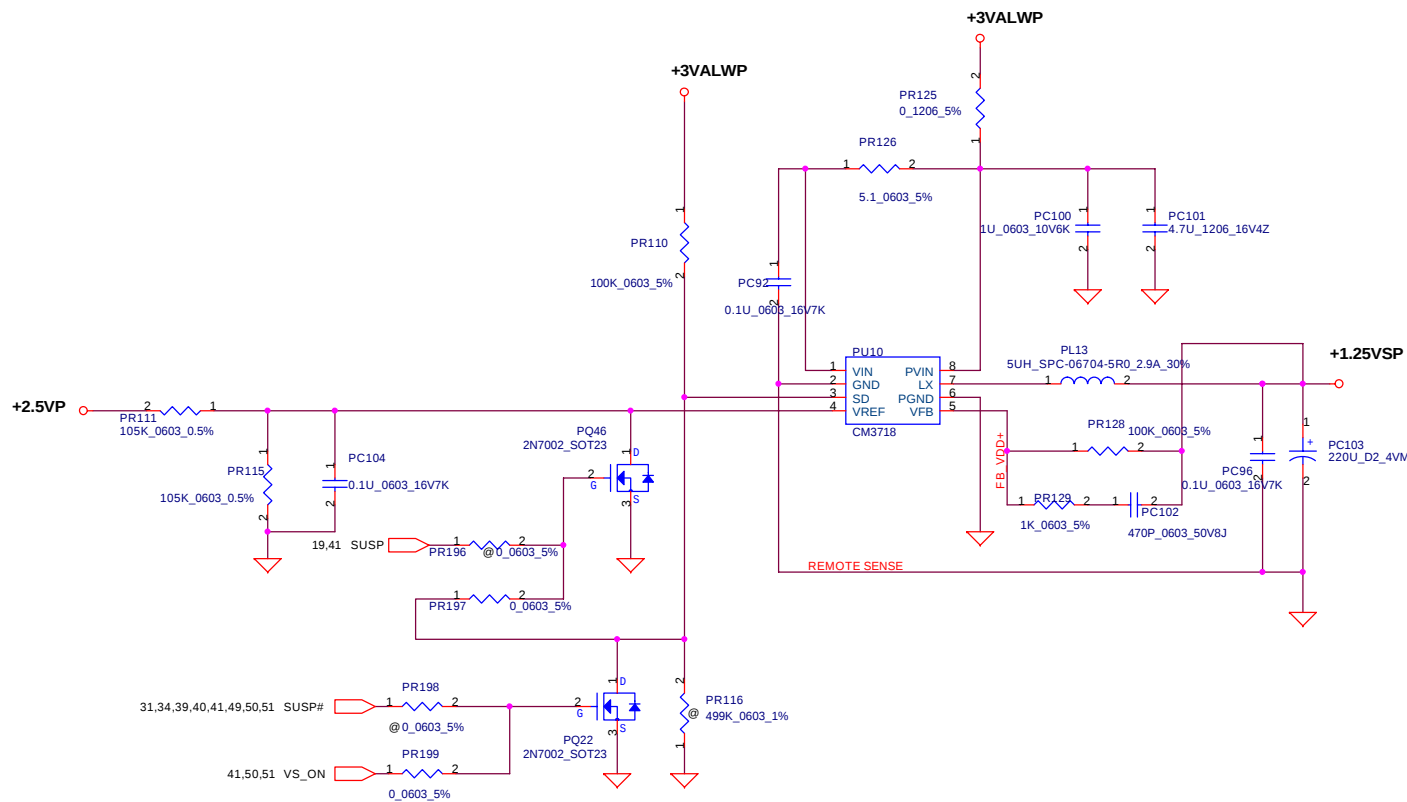
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Compal Electronics, Inc.			
Title VGA_CORE/1.5V			
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145W THROTTLING 120W RECOVERY



$$t = -RC(1 - V_b/V_a)$$

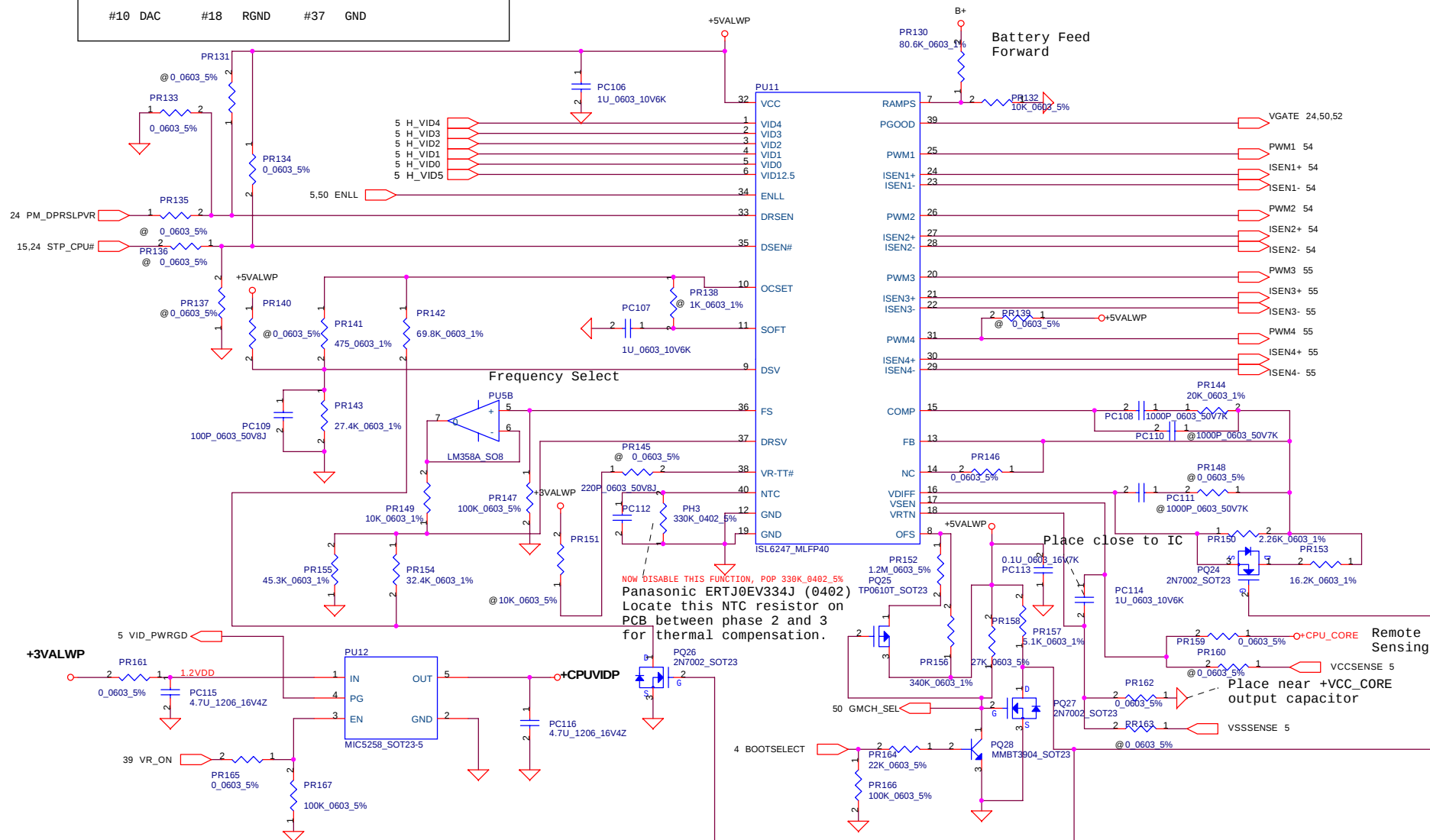


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Compal Electronics, Inc.			
Title			
DDR_1.25V/CLOCK THROTTLING			
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Different Pin Definition for ISL6561 in PU9

#7	GND	#11	REF	#33	EN	#38	OVP
#9	TCOMP	#14	IDROOP	#35	GND	#40	GND
#10	DAC	#18	RGND	#37	GND		



1. When mode control signal is high/ low, the VR will operate to Northwood/ Prescott load line.
2. VID5(12.5) should be pulled high, when the VR operates to Northwood load line.

BOOTSELECT=1 PRESCOTT

BOOTSELECT=0 NORTHWOOD

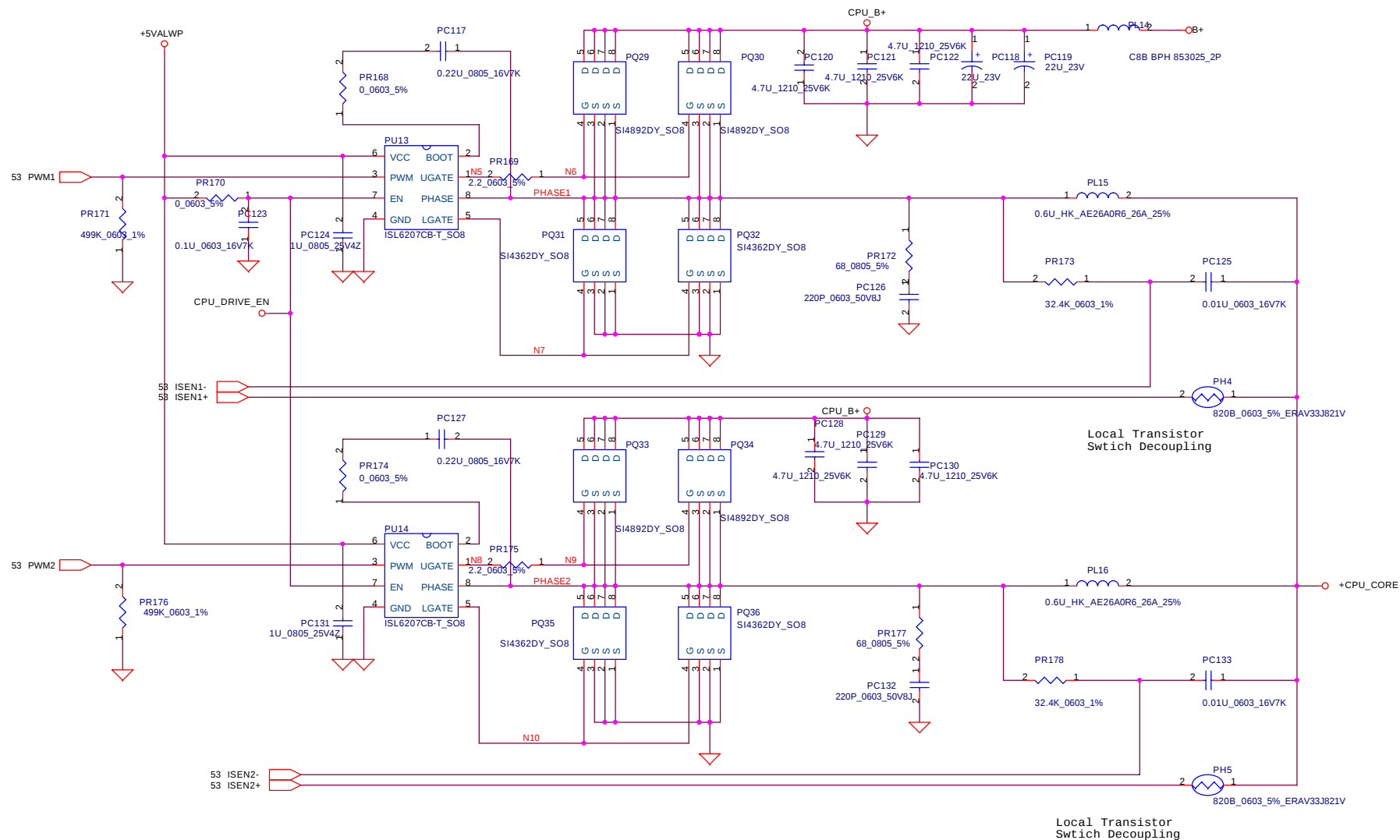
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Compal Electronics, Inc.

CPU_CORE Controller

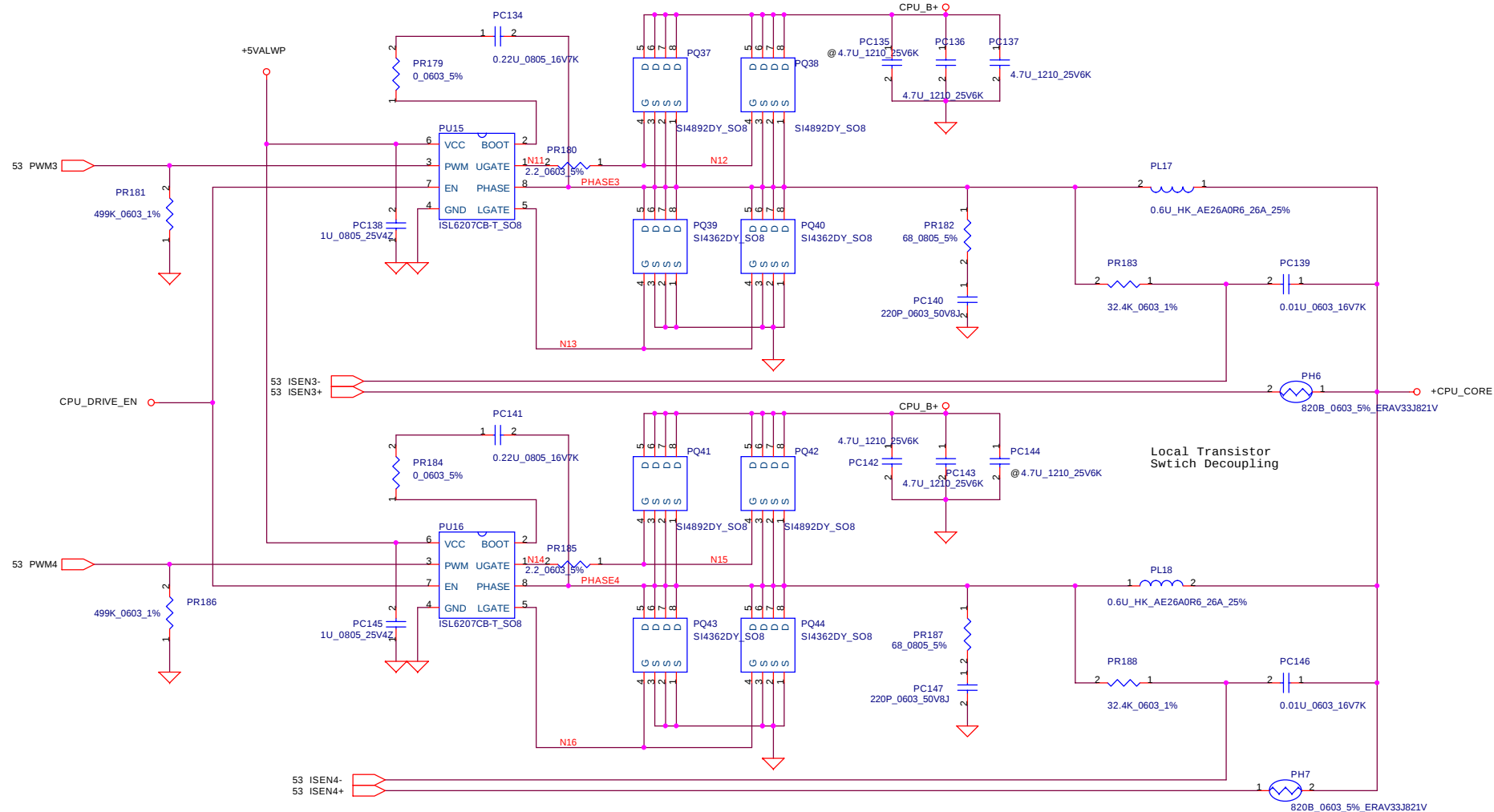
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Title			
CPU_CORE_Power stage 1			
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Title			
CPU_CORE Power stage 2			
Size			
Document Number			Rev
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***** Rev0.1 PIR List *****

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Title		
DBQ01 PIR LIST		
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B	LA-2041	0.1
Date: 二期三, 七月 09, 2003		Sheet 56 of 56