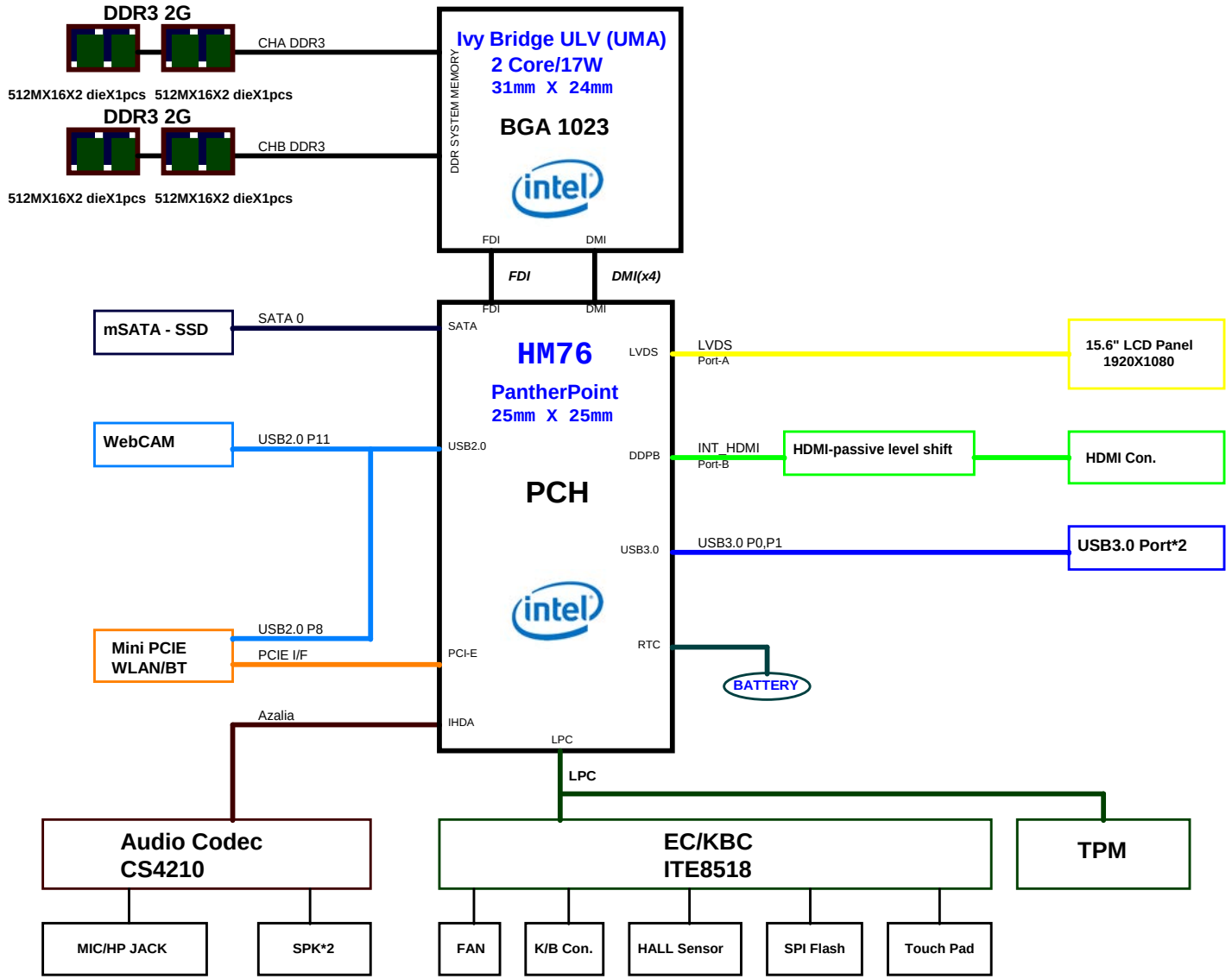
PCB HDI Stackups

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : SVCC
- LAYER 6 : IN3
- LAYER 7 : GND1
- LAYER 8 : BOT

VZ3 Block Diagram



Quanta Computer Inc.
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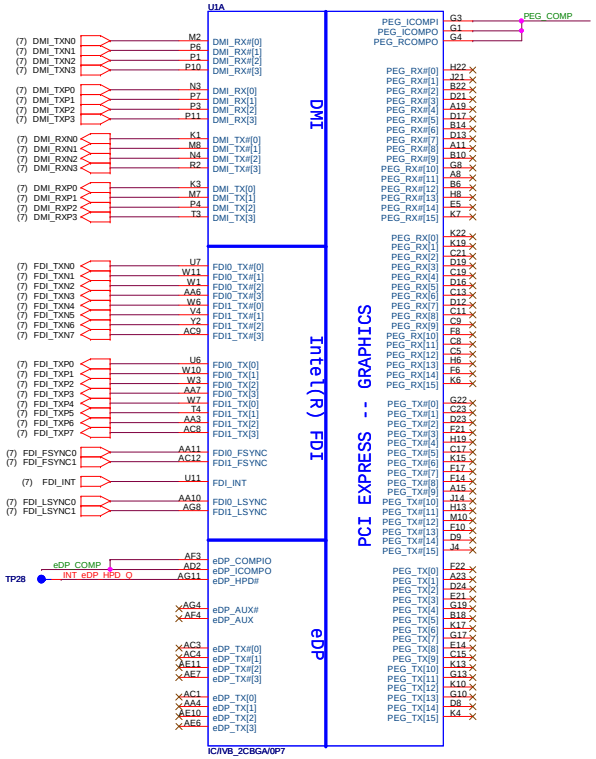
Table of Contents

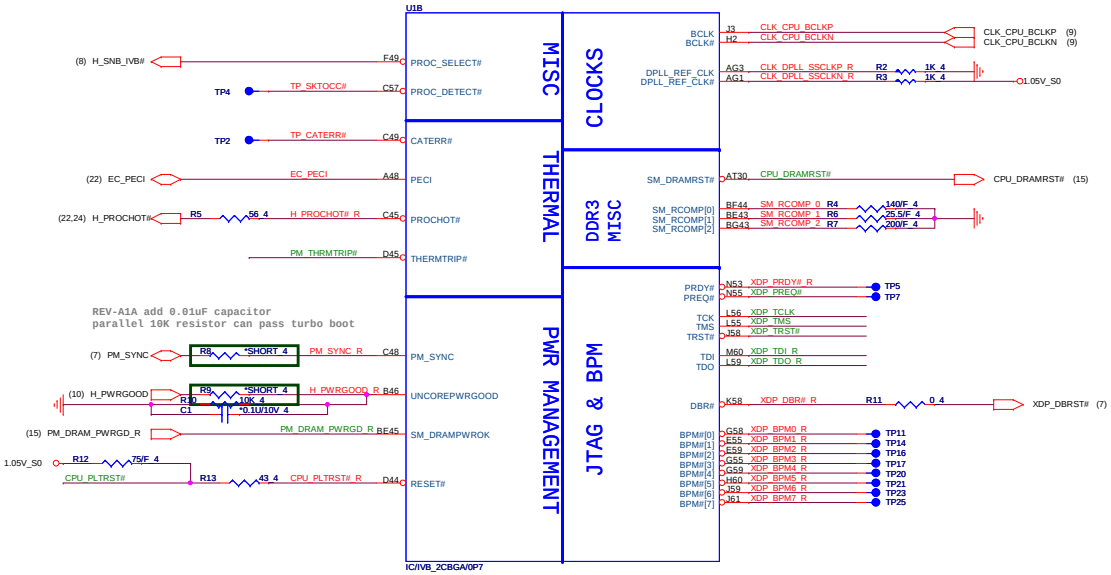
Voltage Rails

Power	Voltage	S0	S3	S4	S5	G3	Ctl Signal
VCCRTC	3V	ON	ON	ON	ON	ON	
VIN	19.5V	ON	ON	ON	ON	OFF	Adaptor in
5V_AUX	5V	ON	ON	ON	ON	OFF	Adaptor in
3V_AUX	3.3V	ON	ON	ON	ON	OFF	Adaptor in
12V_S5	12V	ON	ON	ON	OFF	OFF	S5_ON
5V_S5	5V	ON	ON	ON	OFF	OFF	S5_ON
3V_S5	3.3V	ON	ON	ON	OFF	OFF	S5_ON
5V_S3	5V	ON	ON	OFF	OFF	OFF	S3_ON
1.5V_S3	1.5V	ON	ON	OFF	OFF	OFF	S3_ON
1.5V_CPU	1.5V	ON	OFF	OFF	OFF	OFF	S0_ON1
5V_S0	5V	ON	OFF	OFF	OFF	OFF	S0_ON1
3V_S0	3V	ON	OFF	OFF	OFF	OFF	S0_ON1
1.8V_SFR	1.8V	ON	OFF	OFF	OFF	OFF	S0_ON2
1.05V_S0	1.05V	ON	OFF	OFF	OFF	OFF	S0_ON2
DDR_VTERM	0.75V	ON	OFF	OFF	OFF	OFF	S0_ON2
VCCSA	0.65~0.9V	ON	OFF	OFF	OFF	OFF	S0_ON2
1.5V_S0	1.5V	ON	OFF	OFF	OFF	OFF	S0_ON2
VCC_GFX	By VID	ON	OFF	OFF	OFF	OFF	VRON
VCC_CORE	By VID	ON	OFF	OFF	OFF	OFF	VRON

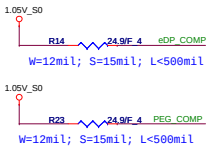
Ivy Bridge Processor (DMI,PEG,FDI)



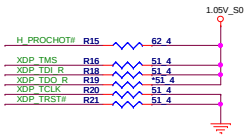
Ivy Bridge Processor (CLK,MISC,JTAG)



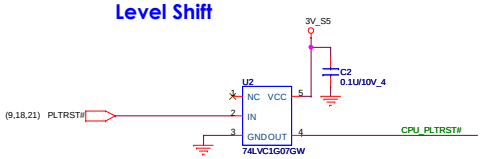
DP & PEG Compensation



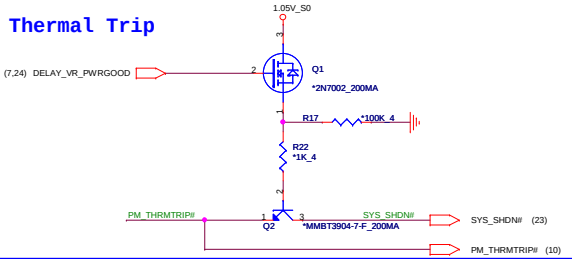
Processor pull-up



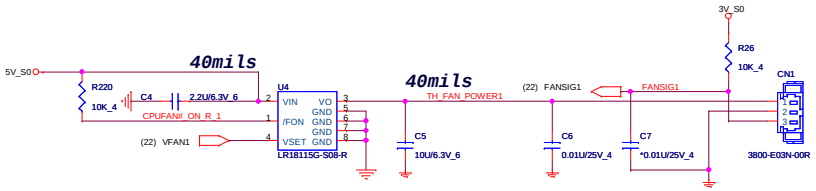
Level Shift



Thermal Trip



FAN Control-->For one FAN solution



Quanta Computer Inc.		
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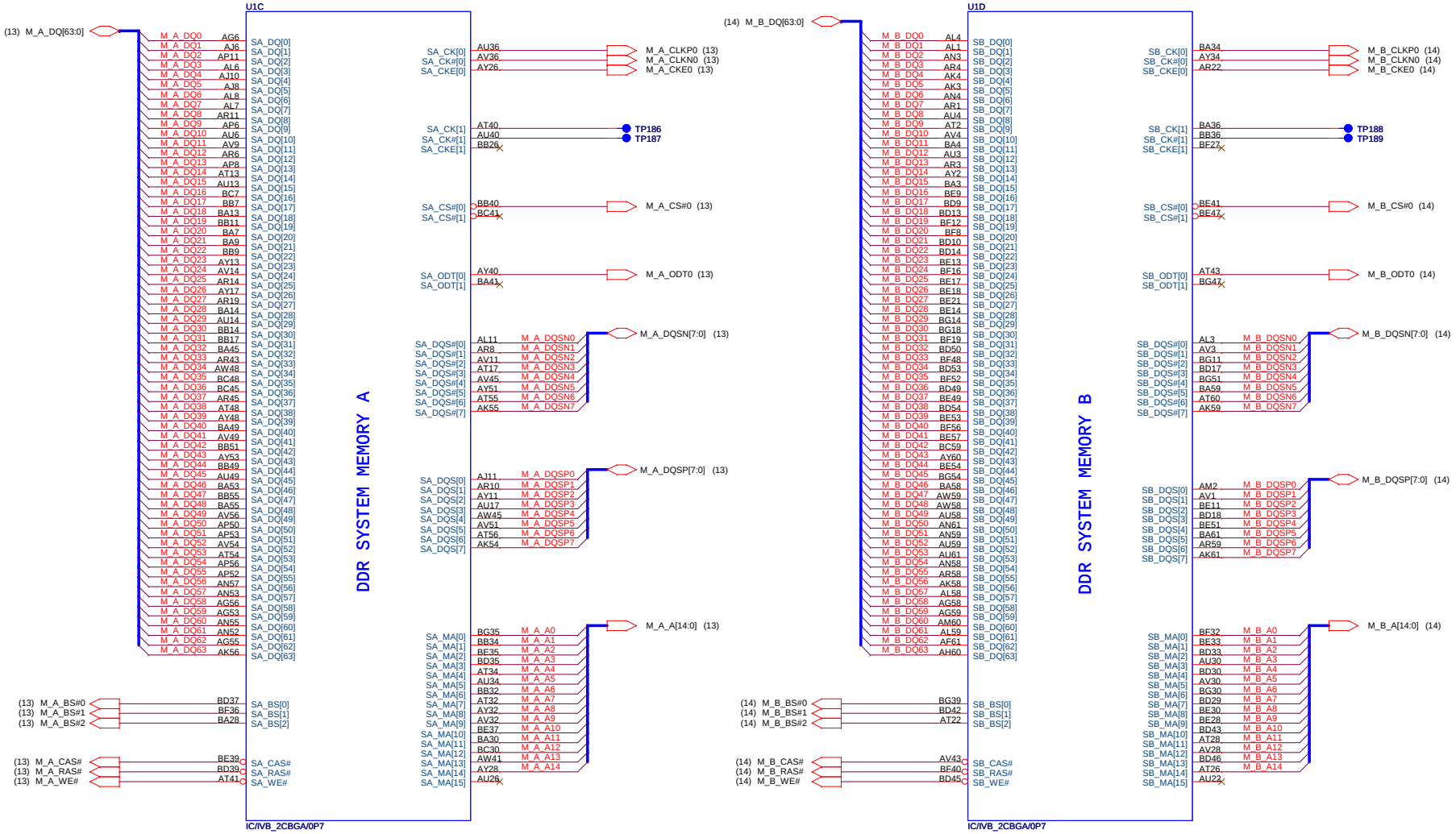
Ivy Bridge Processor (DDR3)



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PROJECT : VZ3			
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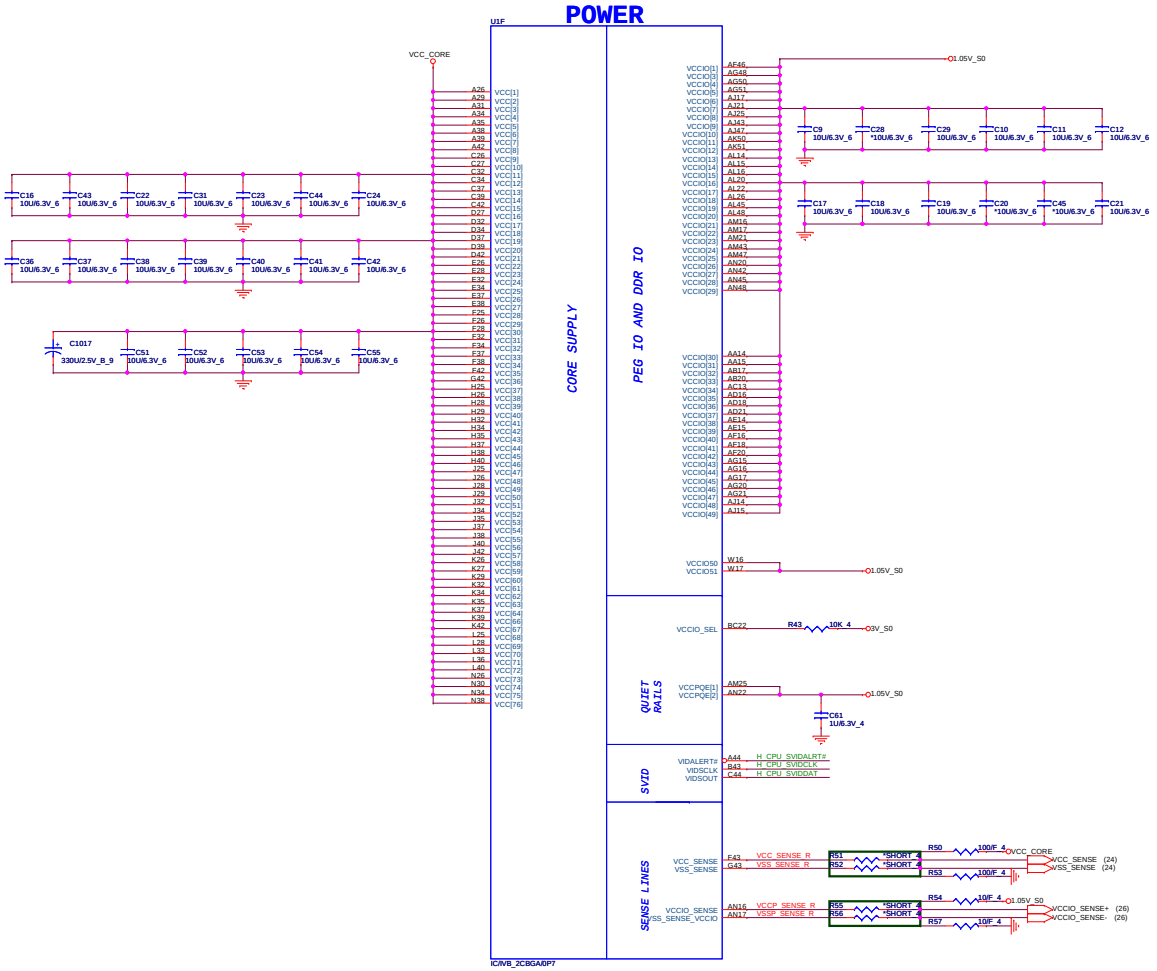
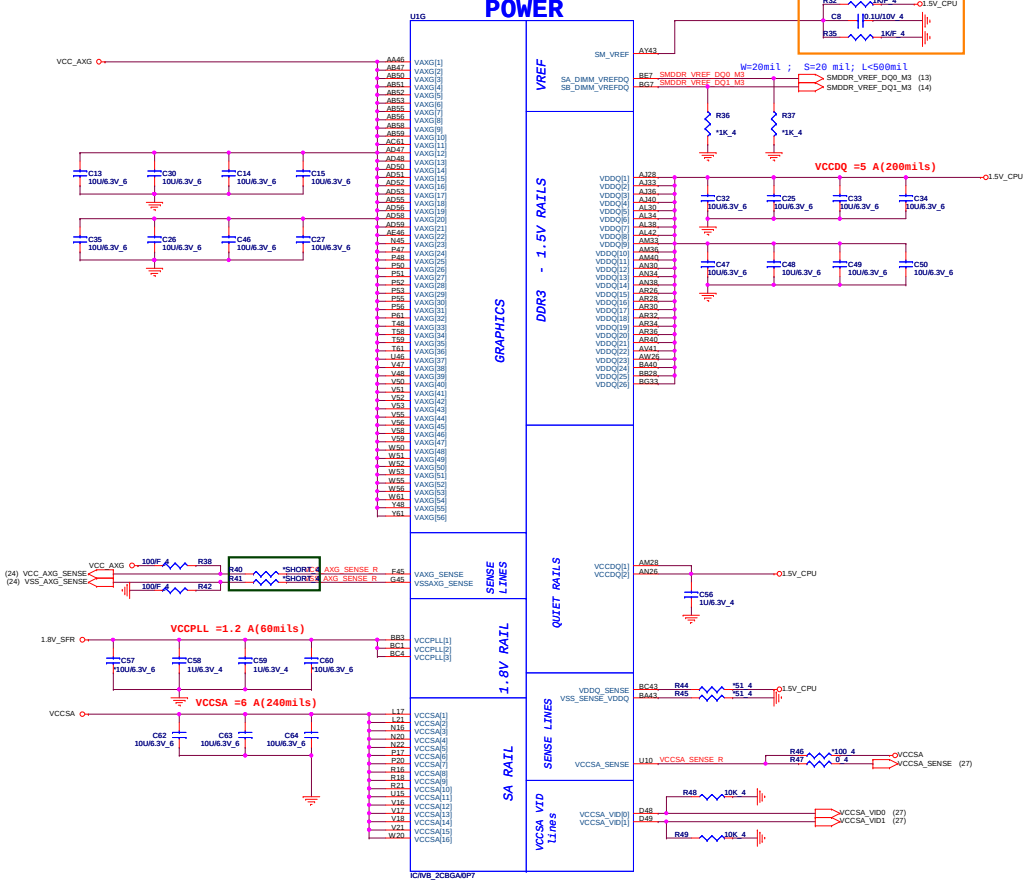
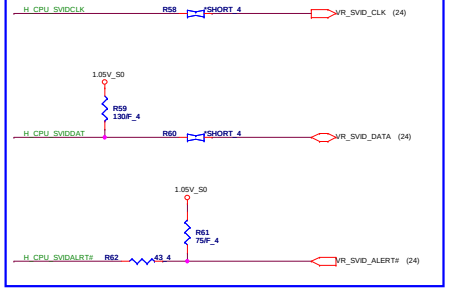
Ivy Bridge Processor (POWER)



Ivy Bridge Processor (GRAPHIC POWER)



Layout note: need routing together and ALERT need between CLK and DATA



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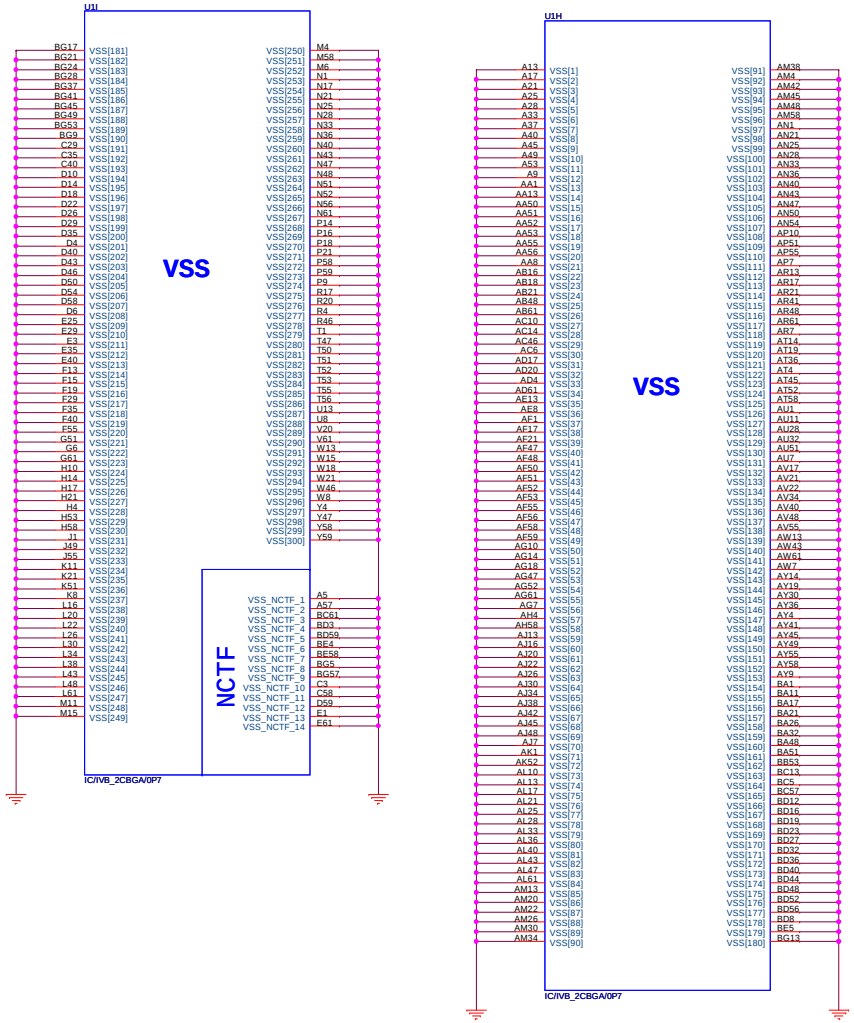
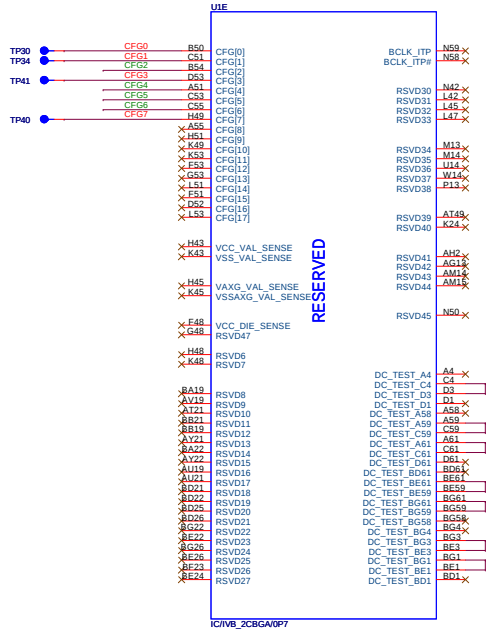
Ivy Bridge Processor (GND)

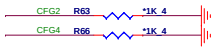


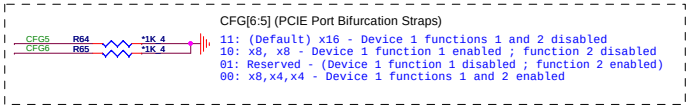
Ivy Bridge Processor (RESERVED, CFG)



Processor Strapping

CFG2	0	PCIe X16 LANE Reversed
	1	Normal Operation
CFG3	0	PCIe X4 LANE Reversed
	1	Normal Operation
CFG4	0	Enable; An ext DP device is connected to eDP
	1	Disable; No physical DP attached to eDP
CFG(5:6)	00	1 x 8 , 2 x 4 PCIe
	01	Reserve
	10	2 x 8 PCIe
	11	1 x 16 PCIe
CFG7	0	PEG Wait for BIOS for training
	1	PEG Train immediately following PLT_RST#





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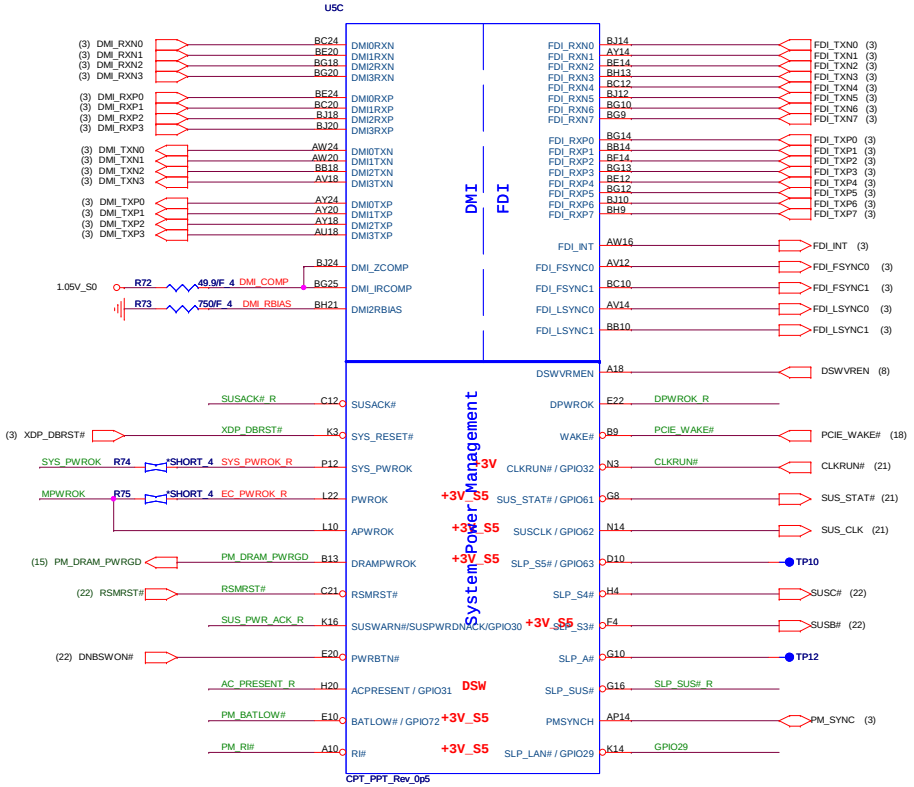
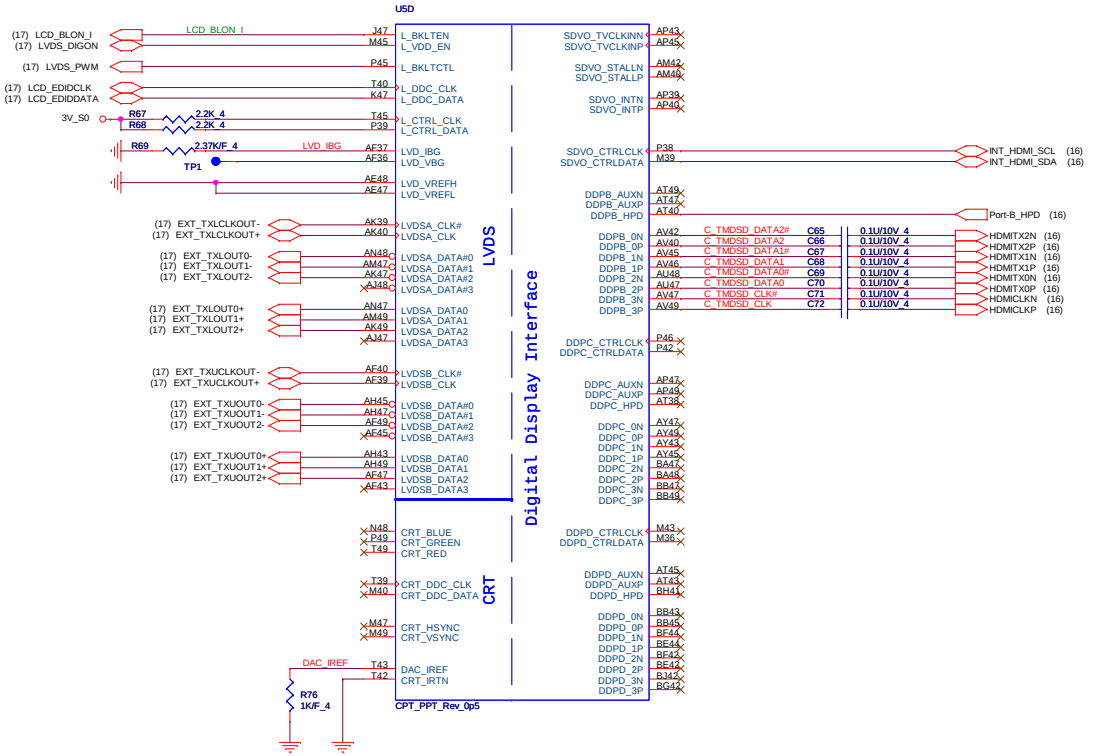
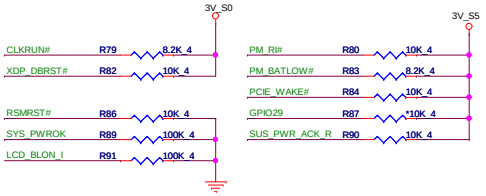
Panther Point (DMI,FDI,PM)



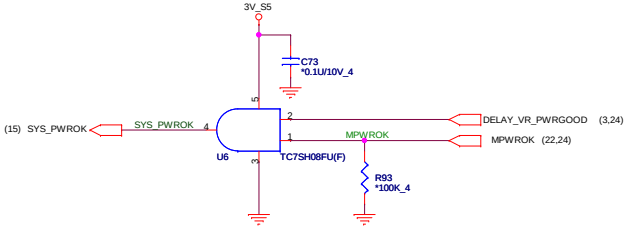
Panther Point (LVDS,DDI)



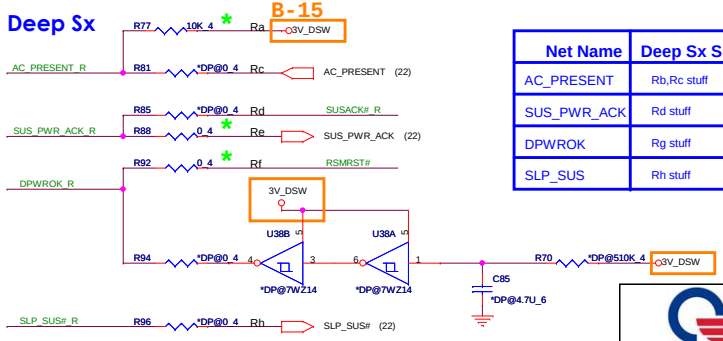
PCH Pull-high/low



System PWR_OK



Deep Sx



Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	Rb,Rc stuff	Ra stuff
SUS_PWR_ACK	Rd stuff	Re stuff
DPWROK	Rg stuff	Rf stuff
SLP_SUS	Rh stuff	Rh No stuff

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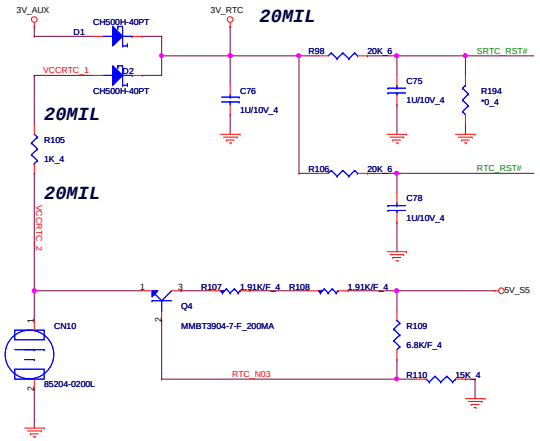
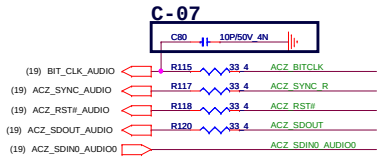
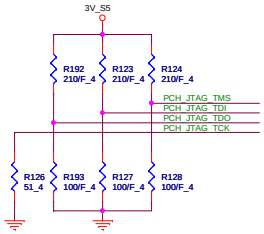
RTC Circuit



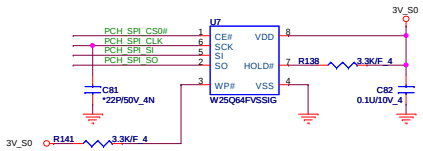
HDA Bus



PCH JTAG Debug



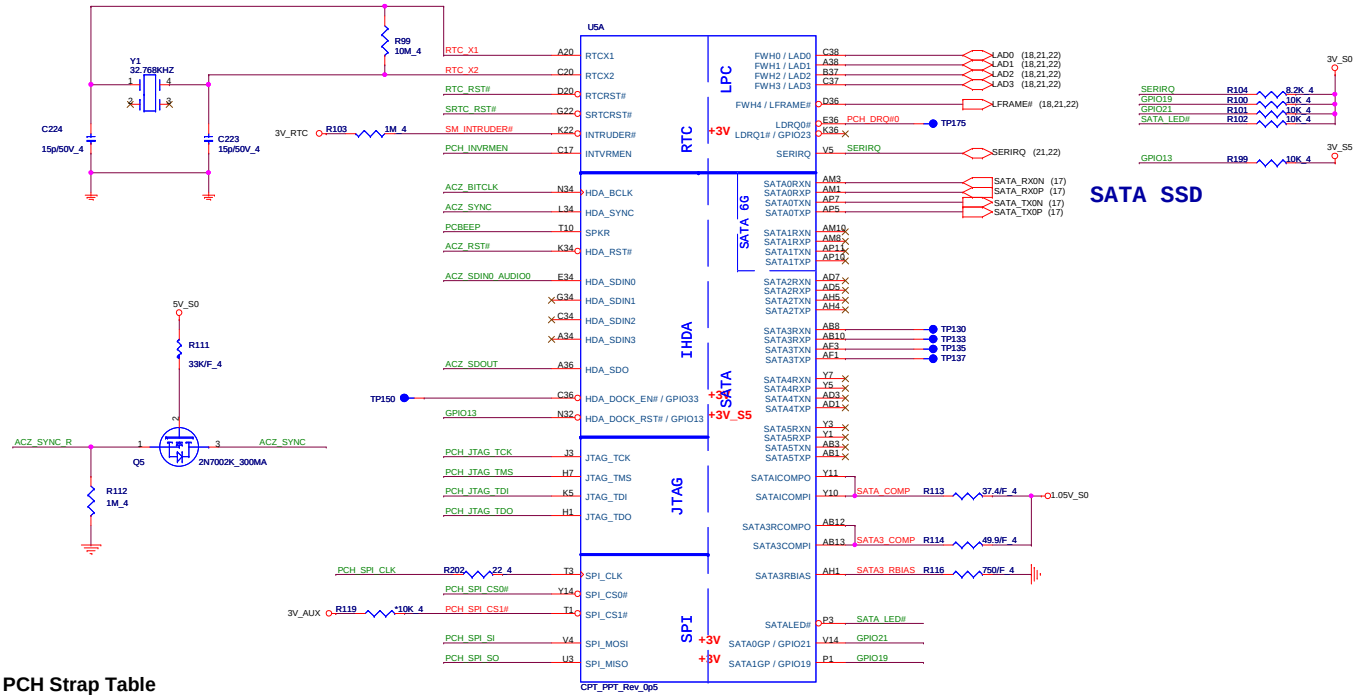
PCH Dual SPI BIOS & ME F/W ROM 8MB



PCH2

Panther Point (HDA,JTAG,SATA)

08



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	3V_S0 R121 *1K_4 PCBEEP
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R122 *1K_4 PCI_GNT3# (9)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	3V_RTC R125 330K_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GPIO19 / Boot Location: 1 / 1 / SPI * 0 / 0 / LPC	R129 *1K_4 GNT1# (9) R130 *1K_4 GPIO19
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SDO	Flash Descriptor Security	**RSMRST**	0 = Default (weak pull-down) 1 = Override	3V_S0 R131 *1K_4 ACZ_SDOUT ACZ_SDOUT (22)
DF_TVS	**DMI/FDI Termination voltage**	**PWROK**	**0 = Set to Vss** **1 = Set to Vcc (weak pull-down 20K)**	R132 2.2K_4 R133 1K_4 1.8V_SFR DF_TVS (10) H_SNB_IVB# (3)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	3V_AUX R134 *10K_4 R135 *1K_4 PLL_ODVR_EN (10)
HDA_SYNC	**On-Die PLL VR Voltage Select**	**RSMRST**	**0 = Support by 1.8V (weak pull-down)** **1 = Support by 1.5V**	3V_S5 R136 1K_4 ACZ_SYNC
GPIO15	TLS Confidentiality	RSMRST	0 = Default. TLS no Confidentiality 1 = TLS Confidentiality	3V_S5 R137 *1K_4 GPIO15 (10)
DSWVRMEN	Deep S4/S5 Well On -Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	DSWVREN (7) 3V_RTC R139 330K_4 R140 *330K_4
INIT3_3V#	**Reserved**	PWROK	1 = Default (weak pull-up 20K)	**Should not pull low. leave as No Connect**
GNT2#/ GPIO53	**ESI Strap (Server Only)**	PWROK	1 = Default. Should not be pulled low for desktop and mobile	**Should not pull low for desktop and mobile**
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
DDPD_CTRLDATA	Port D Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
SATA3GP/ GPIO37	**Reserved**	PWROK	0 = Default	**Should not be pulled high when strap is sampled**
SATA2GP/ GPIO36	**Reserved**	PWROK	0 = Default	**Should not be pulled high when strap is sampled**

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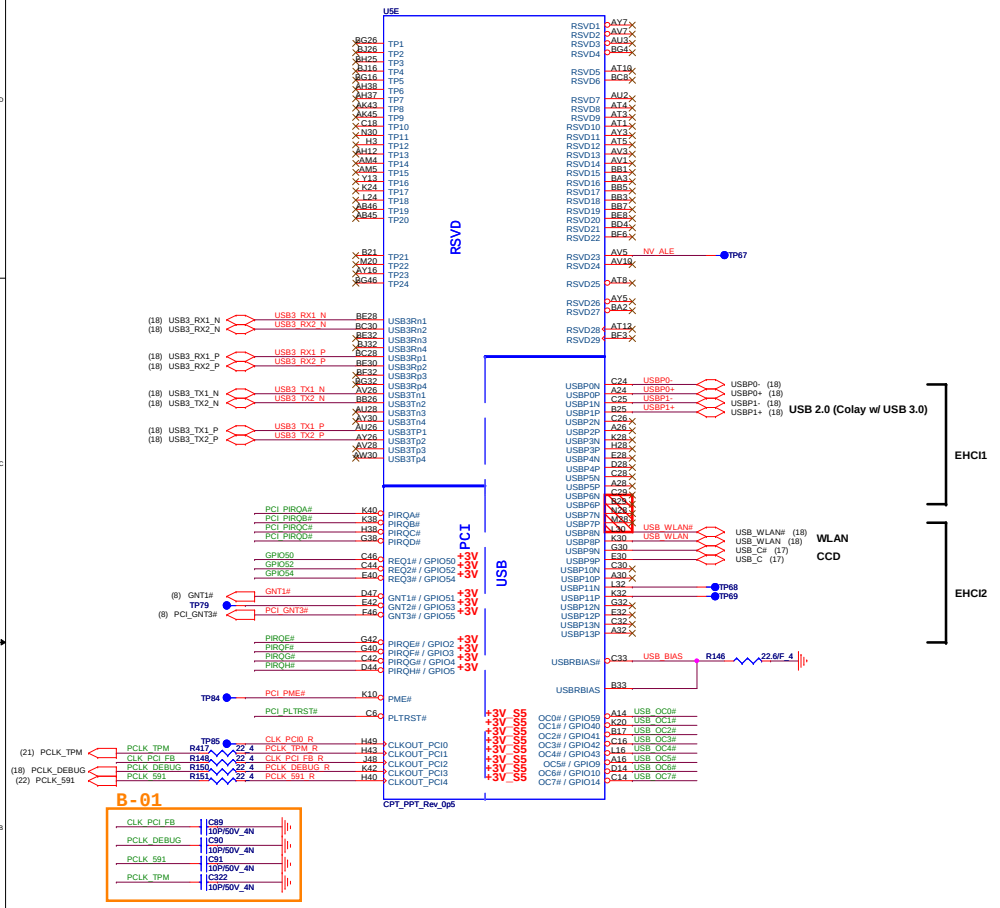
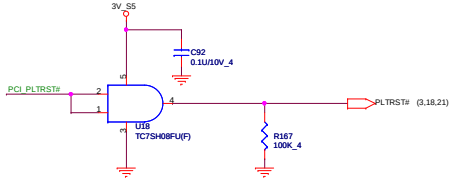
Panther Point-M (PCI,USB,NVRAM)

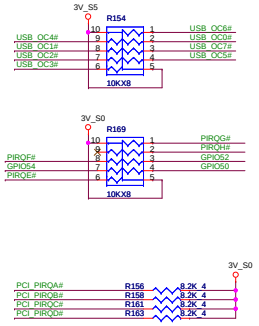


Panther Point-M (PCI-E,SMBUS,CLK)

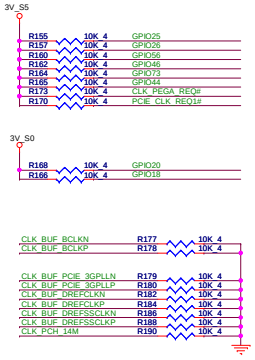
PLTRST#



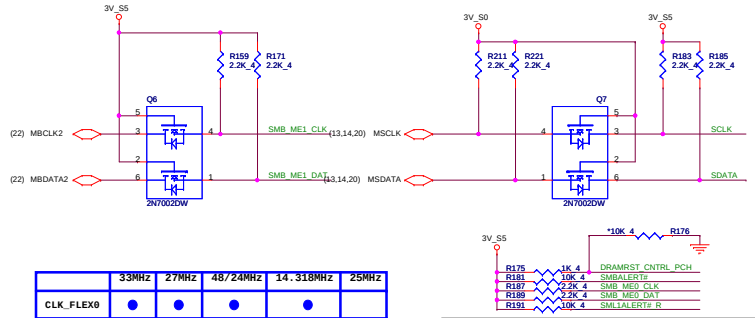
PCI/USBOC# Pull-up



CLK_REQ/Strap Pin



SMBus/Pull-up



	33MHz	27MHz	48/24MHz	14.318MHz	25MHz
CLK_FLEX0	●	●	●	●	
CLK_FLEX1		●	●	●	
CLK_FLEX2	●	●	●	●	●
CLK_FLEX3		●	●	●	

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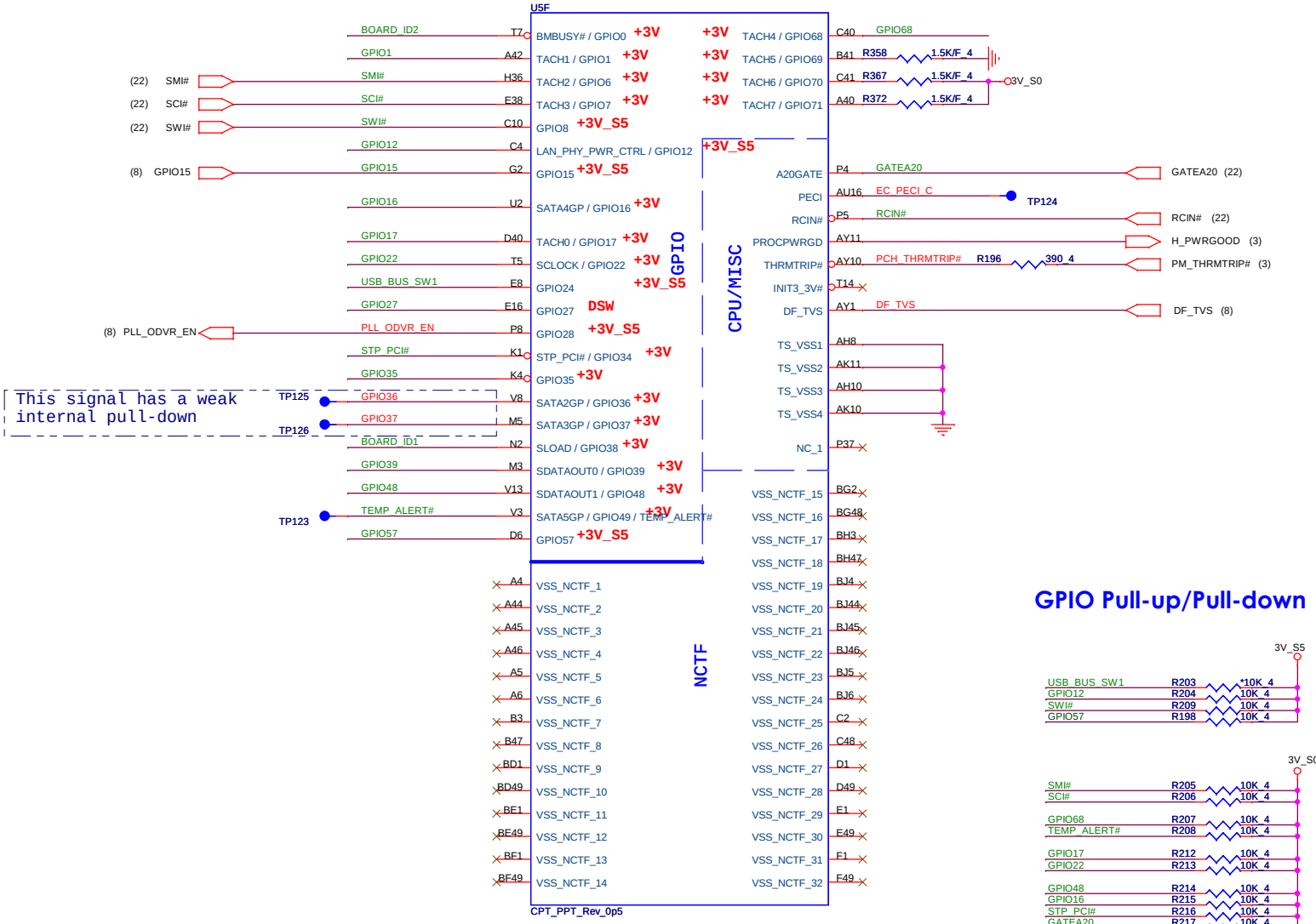
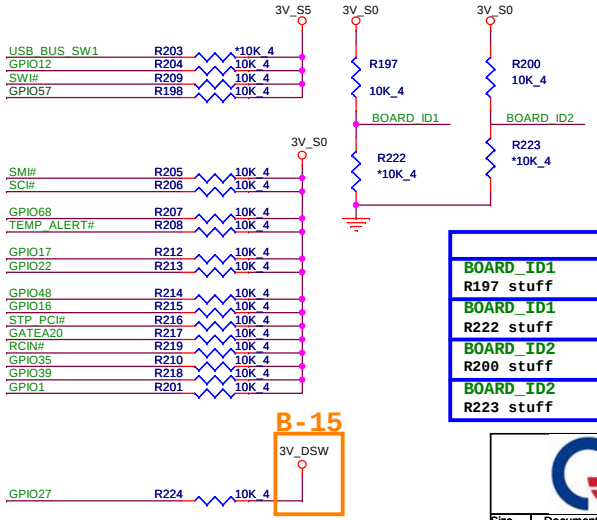
Panther Point (GPIO,VSS_NCTF,RSVD)



GPIO Pull-up/Pull-down



	VZ1	VZ3
BOARD_ID1 R197 stuff	● (Hi)	
BOARD_ID1 R222 stuff		● (Lo)
BOARD_ID2 R200 stuff	● (Hi)	● (Hi)
BOARD_ID2 R223 stuff		

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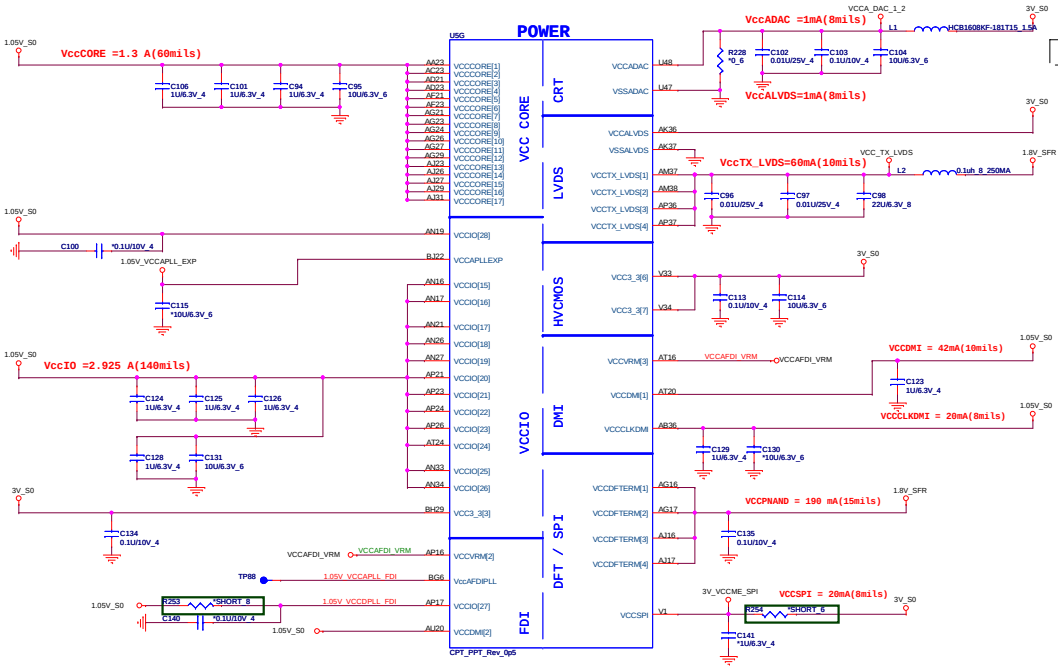
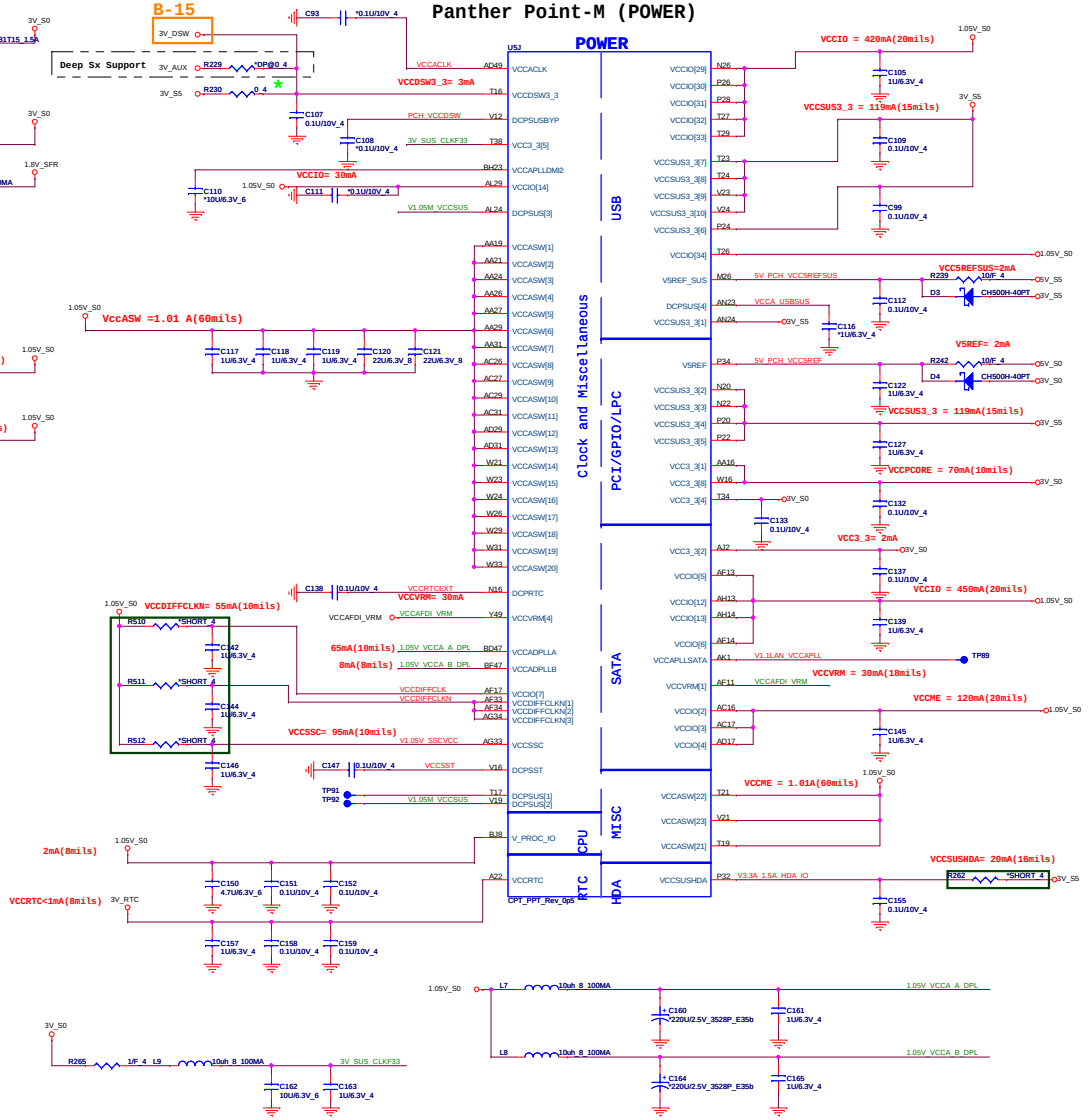
Panther Point (POWER)



Panther Point-M (POWER)



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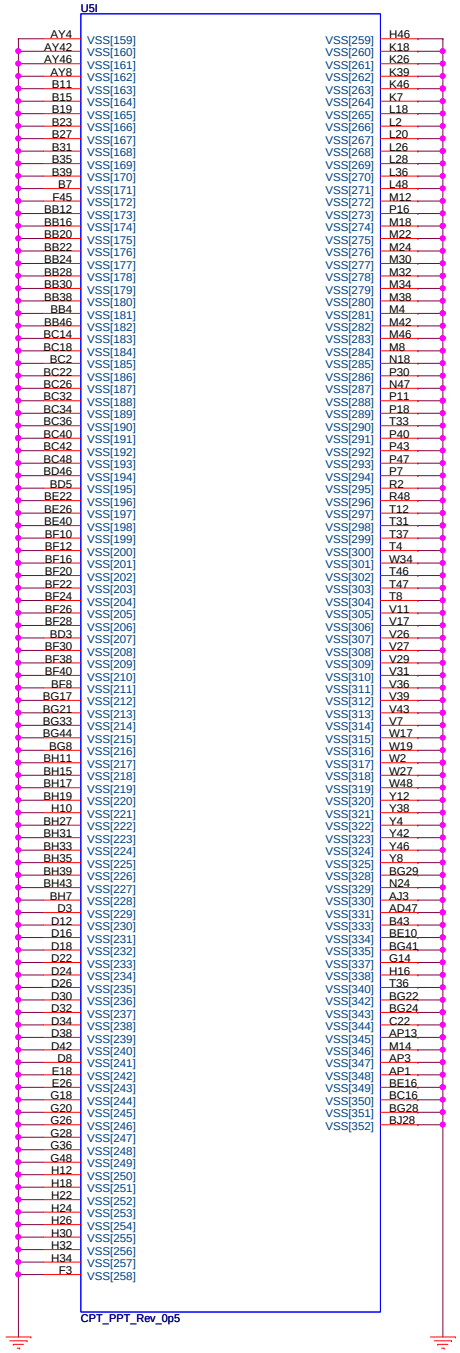
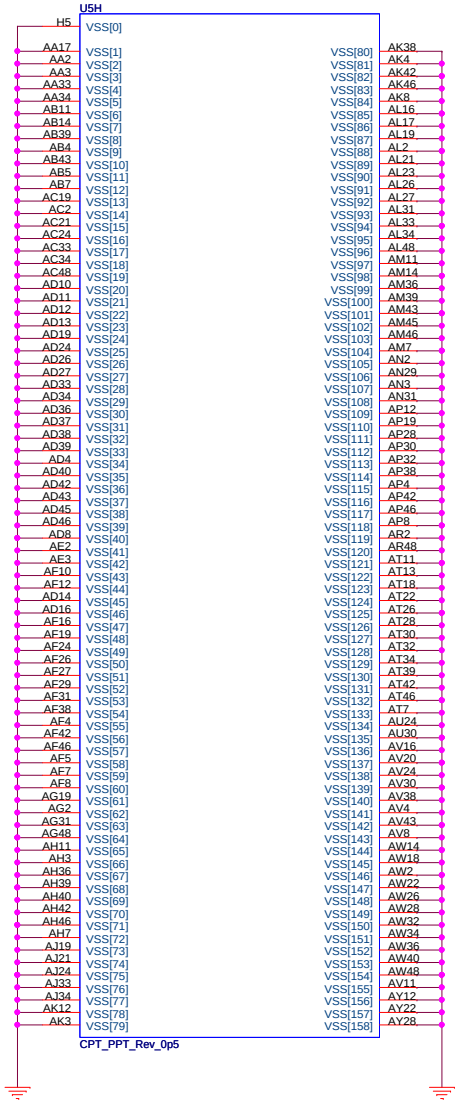
IBEX PEAK-M (GND)





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(4) M_A_DQSP[7:0]
(4) M_A_DQSN[7:0]
(4) M_A_DQ[63:0]

U10

M_A_DQ8 M_A_DQ9 M_A_DQ10 M_A_DQ11 M_A_DQ12 M_A_DQ13 M_A_DQ14 M_A_DQ15
M_A_DQ16 M_A_DQ17 M_A_DQ18 M_A_DQ19 M_A_DQ20 M_A_DQ21 M_A_DQ22 M_A_DQ23
M_A_DQ24 M_A_DQ25 M_A_DQ26 M_A_DQ27 M_A_DQ28 M_A_DQ29 M_A_DQ30 M_A_DQ31
M_A_DQ0 M_A_DQ1 M_A_DQ2 M_A_DQ3 M_A_DQ4 M_A_DQ5 M_A_DQ6 M_A_DQ7

(4) M_A_A[14:0]
M_A_A0 M_A_A1 M_A_A2 M_A_A3 M_A_A4 M_A_A5 M_A_A6 M_A_A7 M_A_A8 M_A_A9 M_A_A10 M_A_A11 M_A_A12 M_A_A13 M_A_A14

(4) M_A_BS#0
(4) M_A_BS#1
(4) M_A_BS#2

M_A_DQSP1 M_A_DQSN1 M_A_DQSP2 M_A_DQSN2 M_A_DQSP3 M_A_DQSN3 M_A_DQSP0 M_A_DQSN0

Should be 240 Ohms +-1%
R270 240/F_4
R275 240/F_4

1.5V_S3

M_A_CLKP0 (4)
M_A_CLKN0 (4)
M_A_CKE0 (4)
M_A_ODT0 (4)
M_A_CS#0 (4)
M_A_RAS# (4)
M_A_CAS# (4)
M_A_WE# (4)
DDR3_DRAMRST# (14,15)
SMDDR_VREF_DQ0 *0_4
R266
SMDDR_VREF_DQ0_M3 (5)

DDR3_EDJ8232B5MB

U11

M_A_DQ40 M_A_DQ41 M_A_DQ42 M_A_DQ43 M_A_DQ44 M_A_DQ45 M_A_DQ46 M_A_DQ47
M_A_DQ48 M_A_DQ49 M_A_DQ50 M_A_DQ51 M_A_DQ52 M_A_DQ53 M_A_DQ54 M_A_DQ55
M_A_DQ56 M_A_DQ57 M_A_DQ58 M_A_DQ59 M_A_DQ60 M_A_DQ61 M_A_DQ62 M_A_DQ63
M_A_DQ32 M_A_DQ33 M_A_DQ34 M_A_DQ35 M_A_DQ36 M_A_DQ37 M_A_DQ38 M_A_DQ39

M_A_A0 M_A_A1 M_A_A2 M_A_A3 M_A_A4 M_A_A5 M_A_A6 M_A_A7 M_A_A8 M_A_A9 M_A_A10 M_A_A11 M_A_A12 M_A_A13 M_A_A14

M_A_BS#0 M_A_BS#1 M_A_BS#2

M_A_DQSP5 M_A_DQSN5 M_A_DQSP6 M_A_DQSN6 M_A_DQSP7 M_A_DQSN7 M_A_DQSP4 M_A_DQSN4

Should be 240 Ohms +-1%
R271 240/F_4
R375 240/F_4

1.5V_S3

M_A_CLKP0
M_A_CLKN0
M_A_CKE0
M_A_ODT0
M_A_CS#0
M_A_RAS#
M_A_CAS#
M_A_WE#
DDR3_DRAMRST#
SMDDR_VREF_DMM
SMDDR_VREF_DQ0

DDR3_EDJ8232B5MB

CAD Note:Cterm=1.5pF should be kept near feeding point of first SDRAM

M_A_CLKP0 R276 30/F_4
C166 1.5P/50V_4
M_A_CLKN0 R284 30/F_4
C171 0.1U/10V_4

Place these Caps near Memory Down-1

1.5V_S3
C169 4.7U/6.3V_6
C174 4.7U/6.3V_6
C177 4.7U/6.3V_6
C180 4.7U/6.3V_6
C181 4.7U/6.3V_6
C182 4.7U/6.3V_6
C183 0.1U/10V_4
C185 0.1U/10V_4
C188 0.1U/10V_4
C191 0.1U/10V_4

SMDDR_VREF_DQ0
C167 0.1U/10V_4
C172 2.2U/6.3V_6
C175 0.1U/10V_4
C178 2.2U/6.3V_6

SMDDR_VREF_DMM
C184 0.1U/10V_4
C186 2.2U/6.3V_6
C189 0.1U/10V_4
C192 2.2U/6.3V_6

DDR_VTERM
C168 1U/6.3V_4
C173 1U/6.3V_4
C176 1U/6.3V_4
C179 1U/6.3V_4

C170 470P/50V_4
R285 1K/F_4
R286 1K/F_4
SMDDR_VREF_DMM
SMDDR_VREF_DMM (14)
1.5V_S3

1.5V_S3
R294 1K/F_4
SMDDR_VREF_DQ0
R301 1K/F_4
C193 0.1U/10V_4
C194 *0.047U/10V_4

DDR_VTERM
R280 36/F_4 M_A_CKE0
R281 36/F_4 M_A_ODT0
R283 36/F_4 M_A_CS#0
R287 36/F_4 M_A_RAS#
R288 36/F_4 M_A_CAS#
R289 36/F_4 M_A_WE#
R291 36/F_4 M_A_BS#0
R292 36/F_4 M_A_BS#1
R293 36/F_4 M_A_BS#2
R295 36/F_4 M_A_A0
R296 36/F_4 M_A_A1
R298 36/F_4 M_A_A2
R299 36/F_4 M_A_A3
R300 36/F_4 M_A_A4
R302 36/F_4 M_A_A5
R303 36/F_4 M_A_A6
R304 36/F_4 M_A_A7
R305 36/F_4 M_A_A8
R306 36/F_4 M_A_A9
R307 36/F_4 M_A_A10
R308 36/F_4 M_A_A11
R309 36/F_4 M_A_A12
R310 36/F_4 M_A_A13
R311 36/F_4 M_A_A14

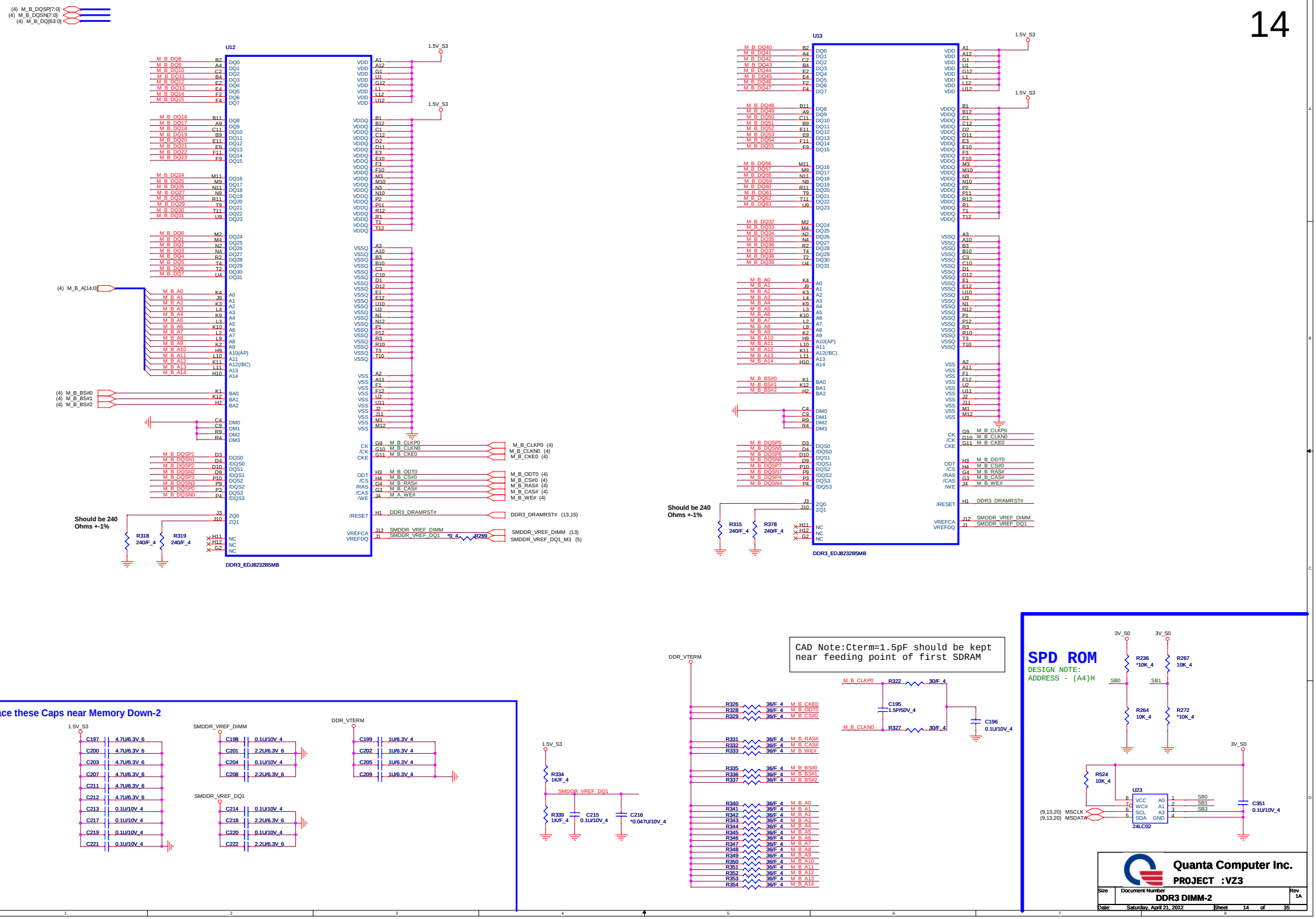
SPD ROM

DESIGN NOTE:
ADDRESS - (A0)H

3V_S0
R237 *10K_4
R278 *10K_4
SA0
SA1
R277 10K_4
R279 10K_4
R444 10K_4
U24
VCC WC# SCL SDA A0 A1 A3 GND
SA0 SA1 SA3
(9,14,20) MSCLK
(9,14,20) MSDATA
24LC02
C350 0.1U/10V_4

Quanta Computer Inc.
PROJECT :VZ3

Size	Document Number	Rev
	DDR3 DIMM-1	1A
Date: Saturday, April 21, 2012	Sheet 13 of 35	



Place these Caps near Memory Down-2

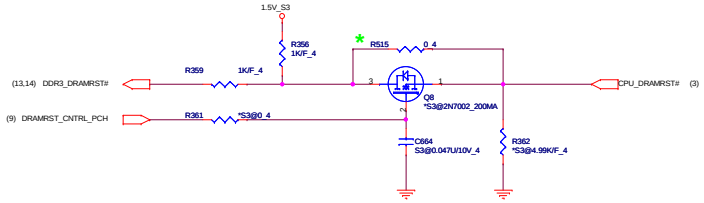
CAD Note:Cterm=1.5pF should be kept near feeding point of first SDRAM

SPD ROM

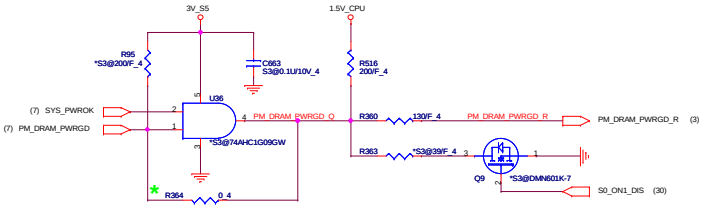
DESIGN NOTE:
ADDRESS - (A4)H

Quanta Computer Inc.		
PROJECT :VZ3		
Size	Document Number: DDR3 DIMM-2	Rev: 1A
Date: Saturday, April 21, 2012	Sheet 14 of 35	

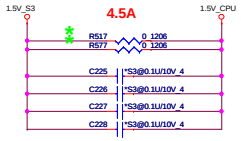
S3 power Reduction (SM_DRAMRST#)



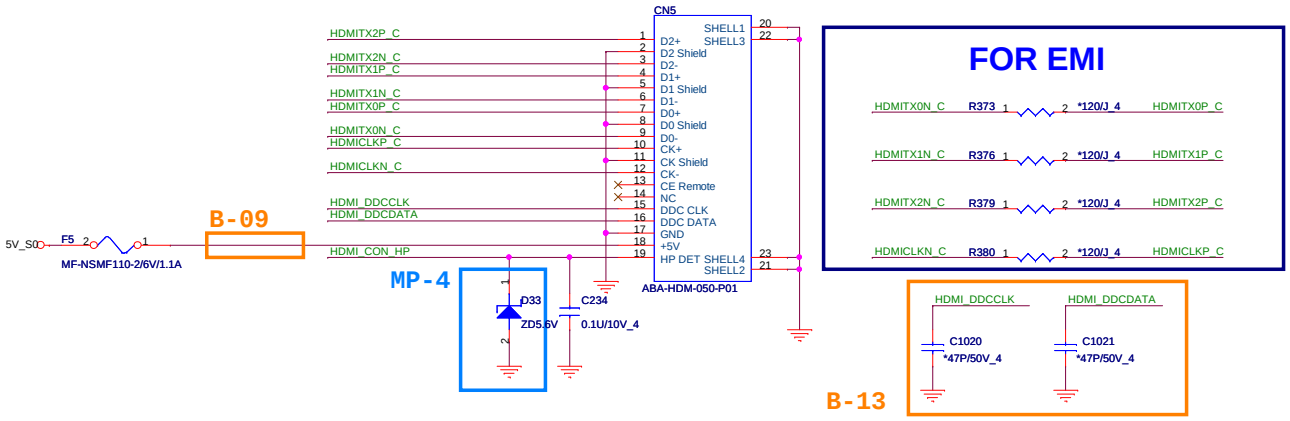
S3 power Reduction (SM_DRAMPWROK)

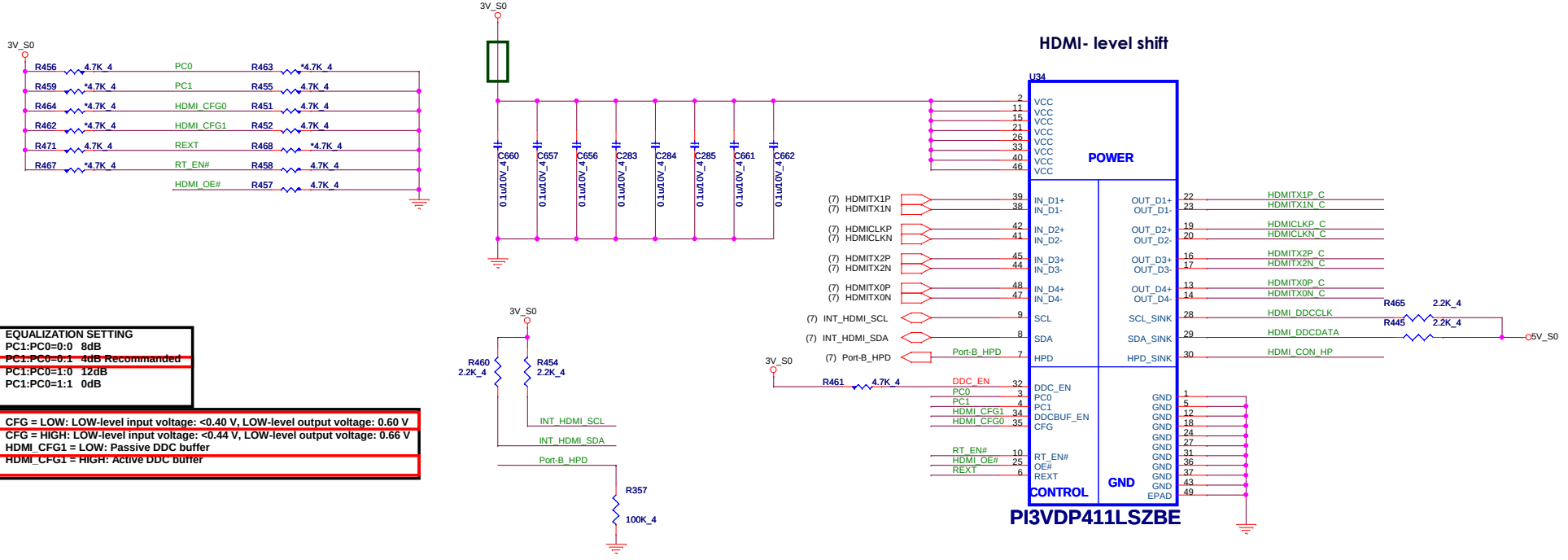


S3 power Reduction (CPU Power)



Quanta Computer Inc.		
PROJECT : VZ3		
Size	Document Number: S3 power Reduction	Rev: 1A
Date: Saturday, April 21, 2012	Sheet 15 of 36	





Quanta Computer Inc.

PROJECT : VZ3

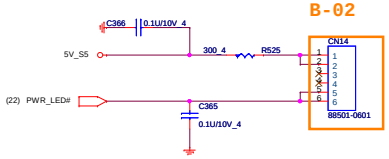
Size	Document Number	Rev
	HDMI CONN	1A

Date: Saturday, April 21, 2012 Sheet 16 of 36

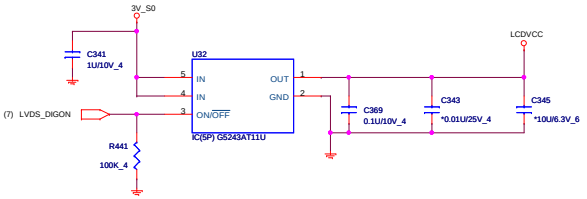
LED

0.2A(20mils)

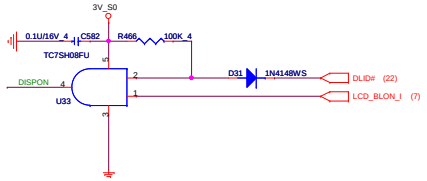
B-02



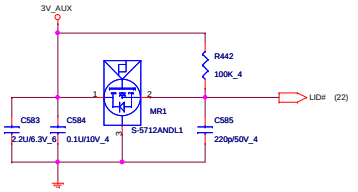
LCD POWER SWITCH



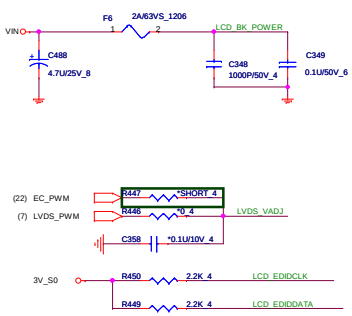
PANEL BACKLIGHT CONTROL

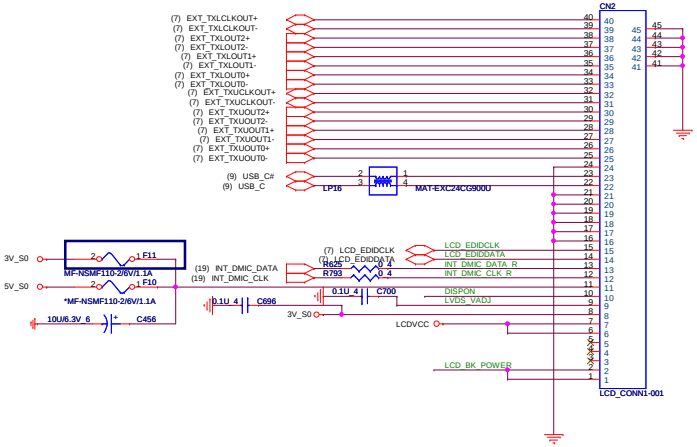


HALL SENSOR&BACK LIGHT SWITCH

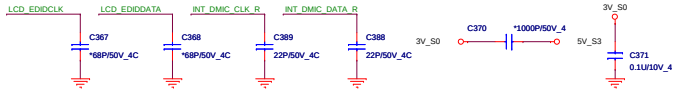


LCD Panel Module





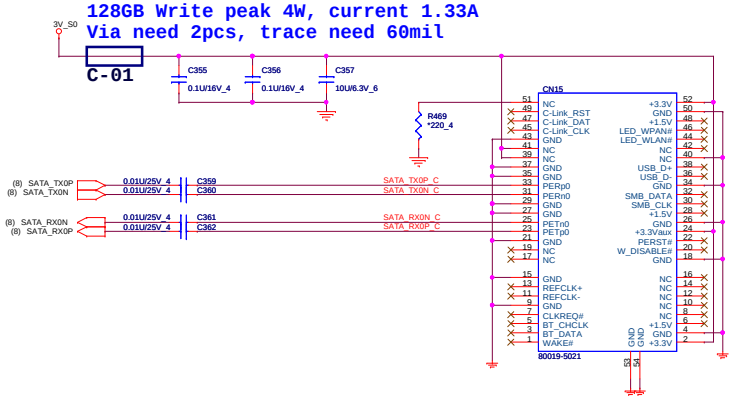
For EMI close to connector



mSATA (SATA over mini PCIe)

128GB Write peak 4W, current 1.33A
Via need 2pcs, trace need 60mil

C-01



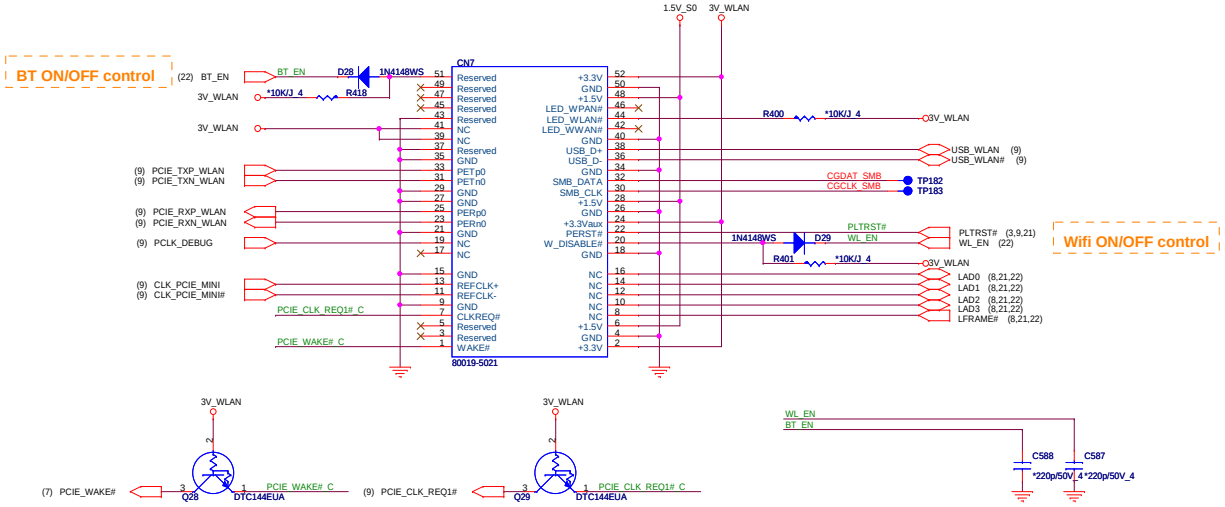
Quanta Computer Inc.

PROJECT : VZ3

Size	Document Number	Rev
	LCD/CCD/mSATA	1A

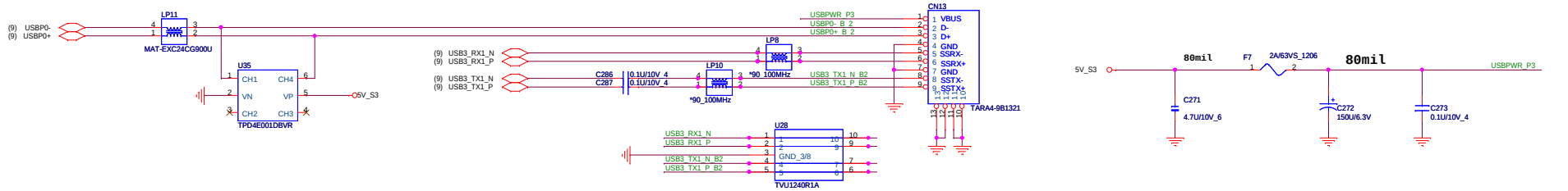
Date: Saturday, April 21, 2012 Sheet 17 of 38

Wireless + BT

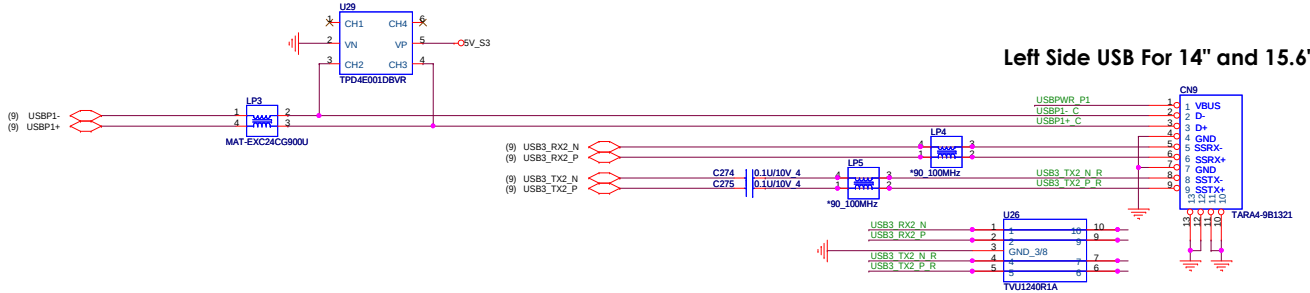


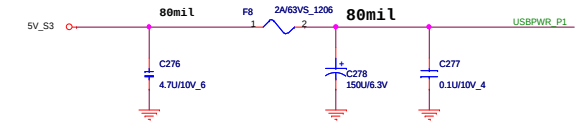
USB 3.0

Right Side for 15.6 only



Left Side USB For 14" and 15.6"





Quanta Computer Inc.
PROJECT : VZ3

Size	Document Number	Rev
	USB3.0/WLBT	3A

Date: Saturday, April 21, 2012 Sheet 18 of 36

AUDIO Cirrus Logic CS4210

C-08

AUDIO return path 1 | AUDIO return path 2 | AUDIO return path 3 | AJK1 EMI path | ACON1 EMI path

1	ALG_HP_L
2	ALG_HP_R
6	MIC_BIAS
3	GND
5	ALG_HP_SENSE
4	GND

LAYOUT NOTICE

DGND | AGND

B-16

CIRRUS LOGIC CS4210

AGND

DGND

B-12

Put the RC close EE mainland side

Put the RC close EE mainland side

Headset remote control circuit (PCBA side)

Jack type	Sense A value
Non-jack	3.3 V
Normal jack	1.72 V
Combo jack	1.33 V

HP & MIC COMBO

C-06

MP-5

B-10

Internal SPK

ACON1

ACS-88266-04001-06

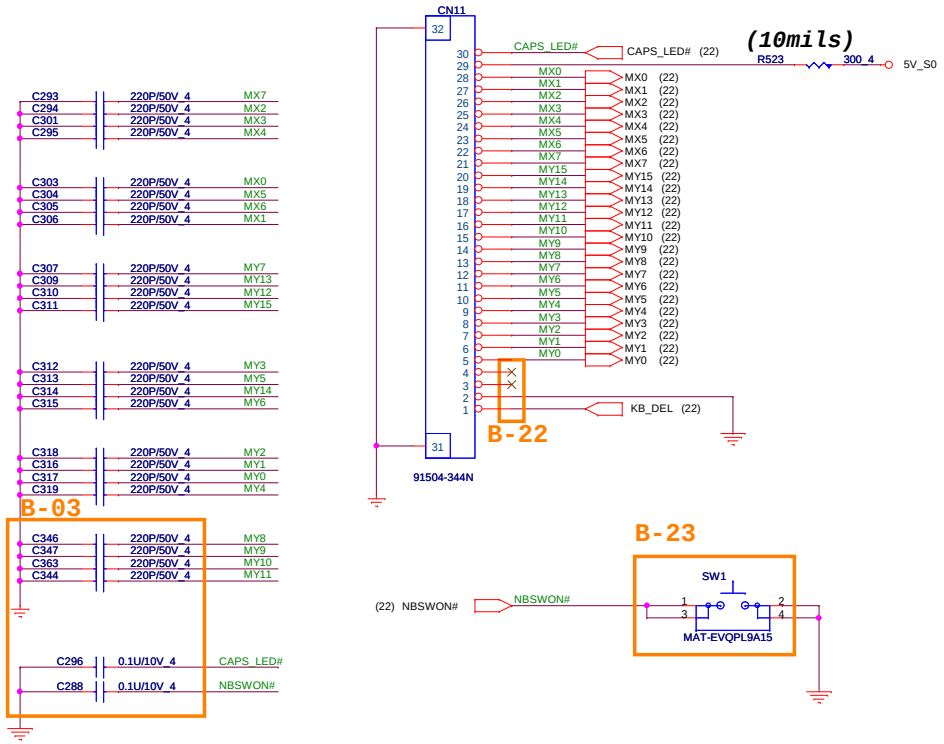
MP-1

B-11

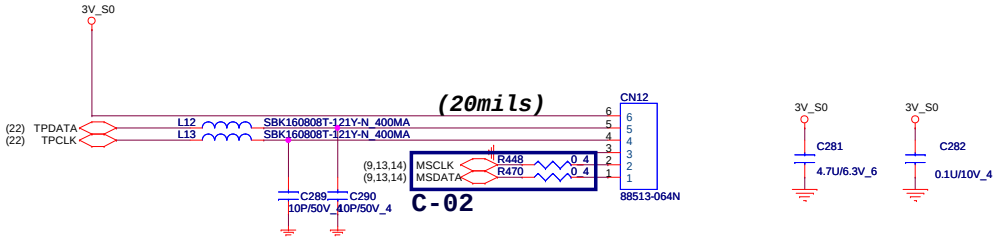
To EC ADC pin

Quanta Computer Inc.	
PROJECT : VZ3	
Size	Document Number: AUDIO CIRRUS LOGIC CS4210 — Rev: 1A
Date: Wednesday, April 25, 2012	Sheet 19 of 36

INT KeyBoard

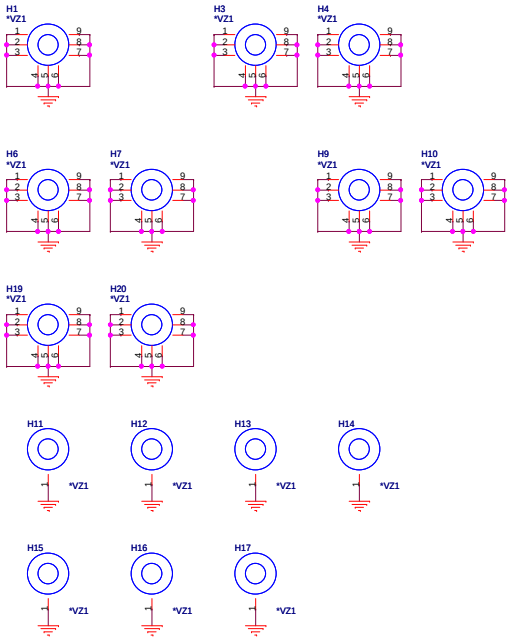


TP board

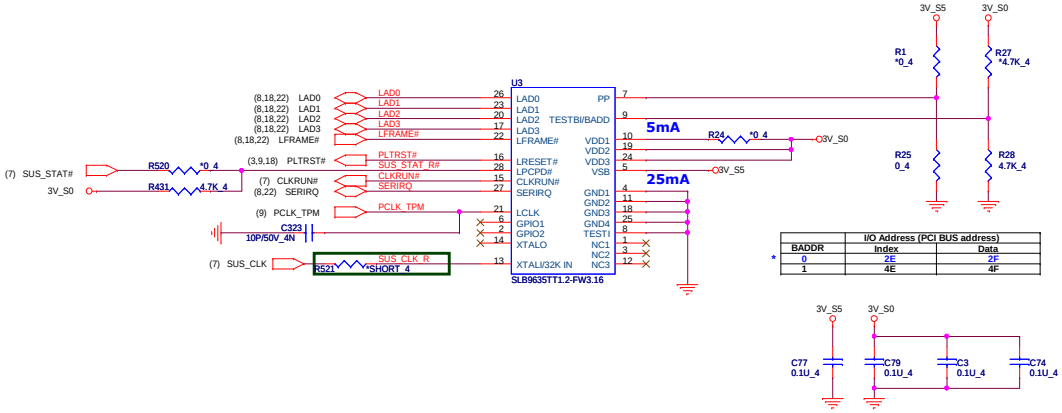


Quanta Computer Inc.		
PROJECT : VZ3		
Size	Document Number: TP/KB	Rev: 1A
Date: Saturday, April 21, 2012	Sheet 20 of 36	

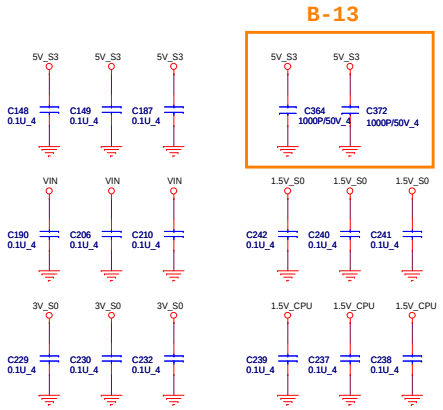
HOLE



TPM



EMI



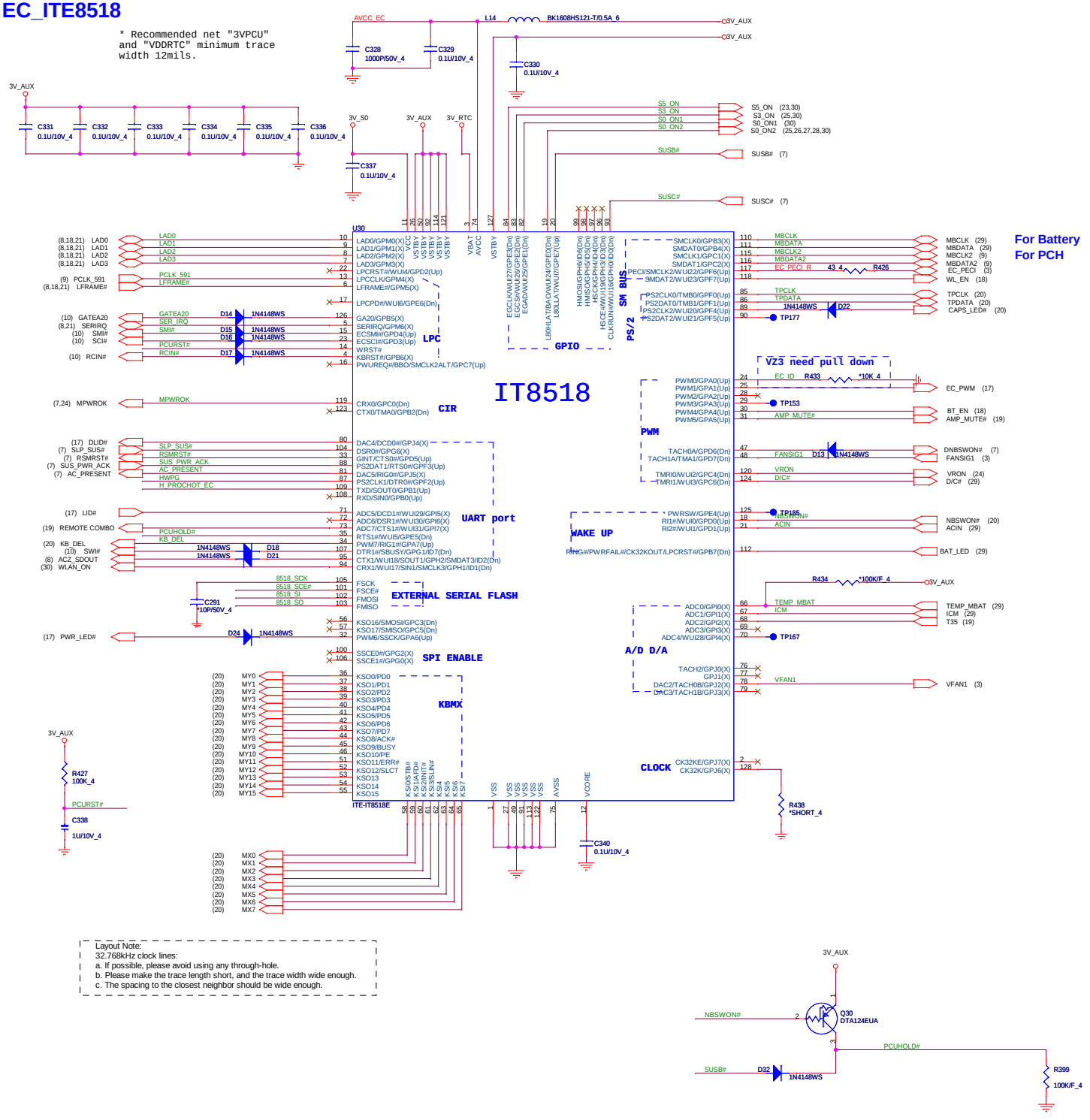
Quanta Computer Inc.
PROJECT : VZ3

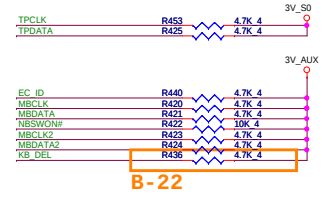
Size	Document Number	Rev
	HOLE/TPM	1A

Date: Saturday, April 21, 2012 Sheet 21 of 36

EC_ITE8518

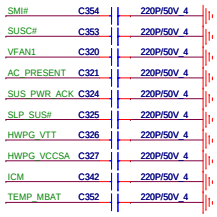
* Recommended net "3VPCU" and "VDDRTC" minimum trace width 12mils.



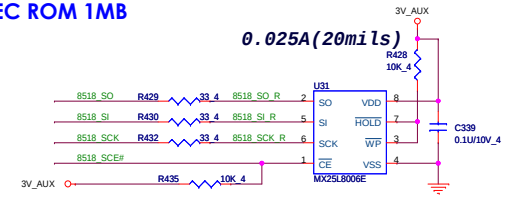


VZ1	R440	Hi
VZ3	R433	Lo

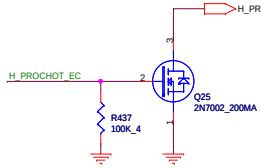
EMI



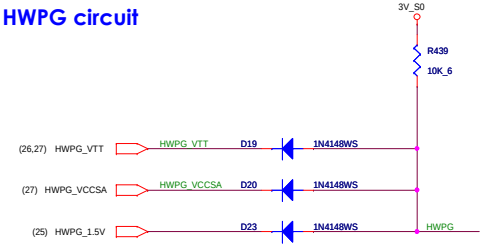
EC ROM 1MB



For throttleing

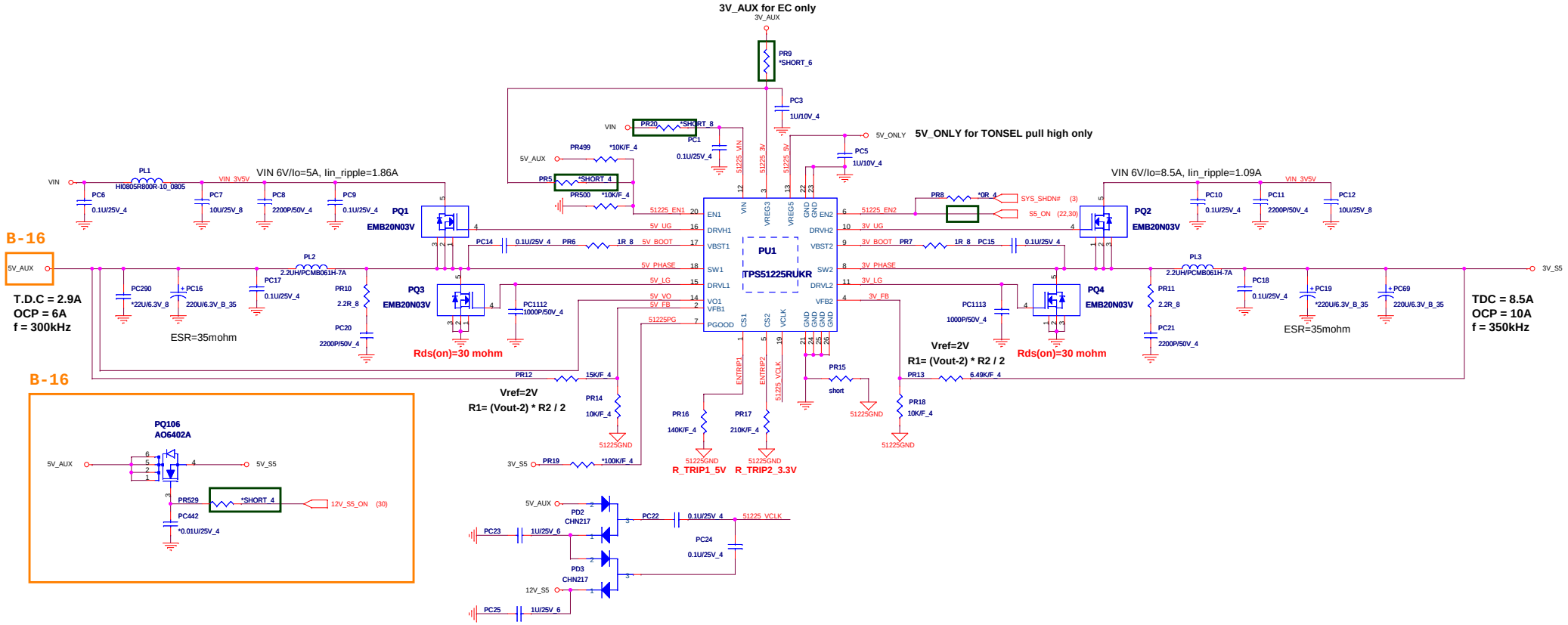


HWPG circuit



Quanta Computer Inc.	
PROJECT : VZ3	
Size	Document Number: EC_ITE8519 — Rev: 1A
Date: Saturday, April 21, 2012	Sheet 22 of 36

System 3V_S5 and 5V_S5 (TPS51225RUKR)



Iripple=(Vin-Vout)*Vout/(Vin*L*f)

O.C.P setup information

Output	Mos Rds_on	I_OCP	OC_ΔIL(A)	Freq(KHz)	Inductor	R_TRIP
5V	17.5m_Max	9	3.68	365	2.5uH	215K
3.3V	17.5m_Max	7.5	2.18	460	2.5uH	196K

L/S Mosfet parameter

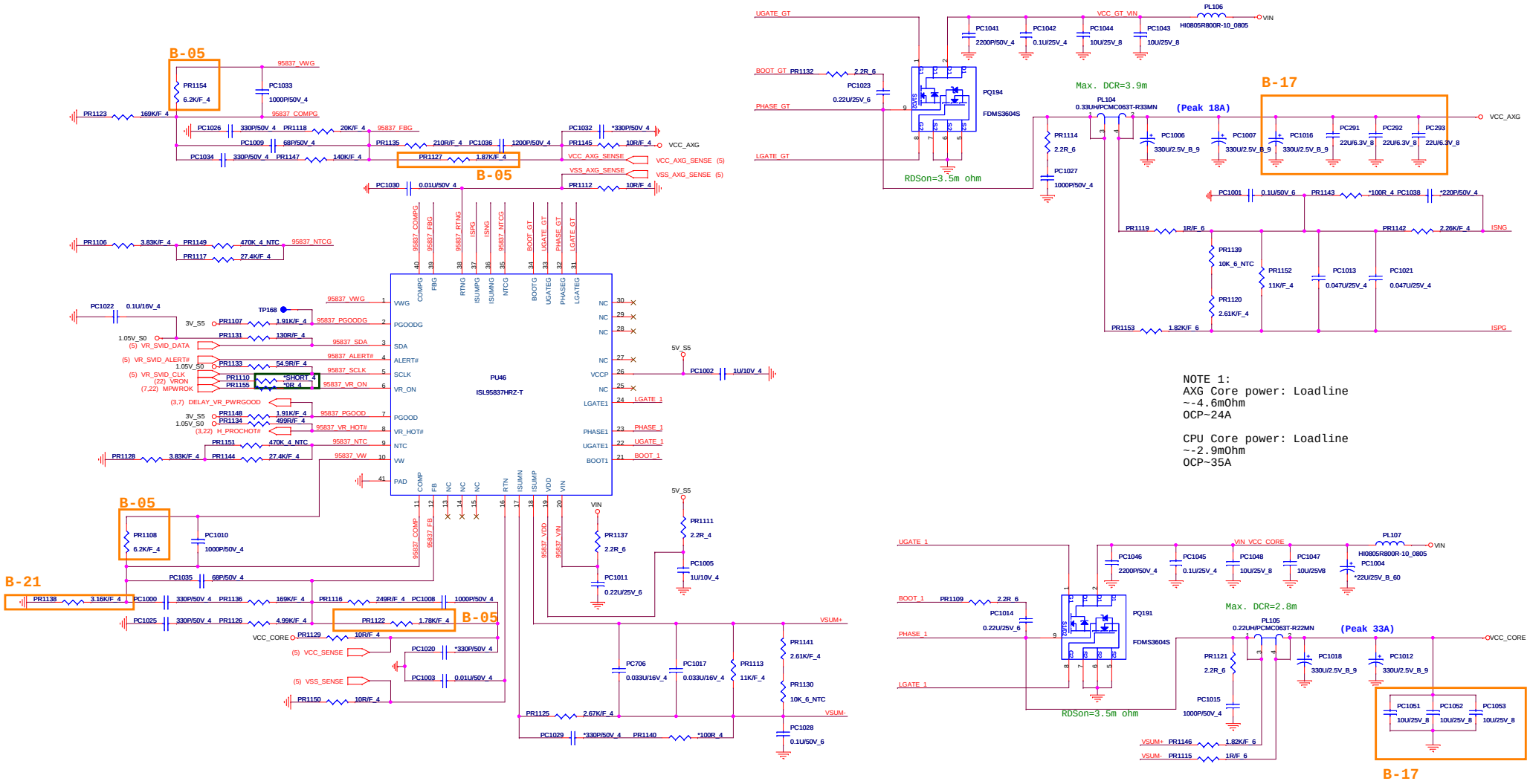
MOSFET	Package	ID (Ta=25C)	Rds_on_max
AP4438GM-HF	SO-8	11.8A	18m
EMB12N03G	SO-8	12A	15m
SI4134DY	SO-8	14A	17.5m
EMB20N03V	DFN3x3	12A	30m
MDV1525	DFN3x3	24A	14m
TPCC8065-H	DFN3x3	13A	14.5m

Power On sequencing

EN0	ENC	REF	VREG3	VREG5	SMPS1	SMPS2
LOW	LOW	OFF	OFF	OFF	OFF	OFF
> 2.4V	LOW	ON	ON	ON	OFF	OFF
> 2.4V	> 2.4V	ON	ON	ON	ON	ON

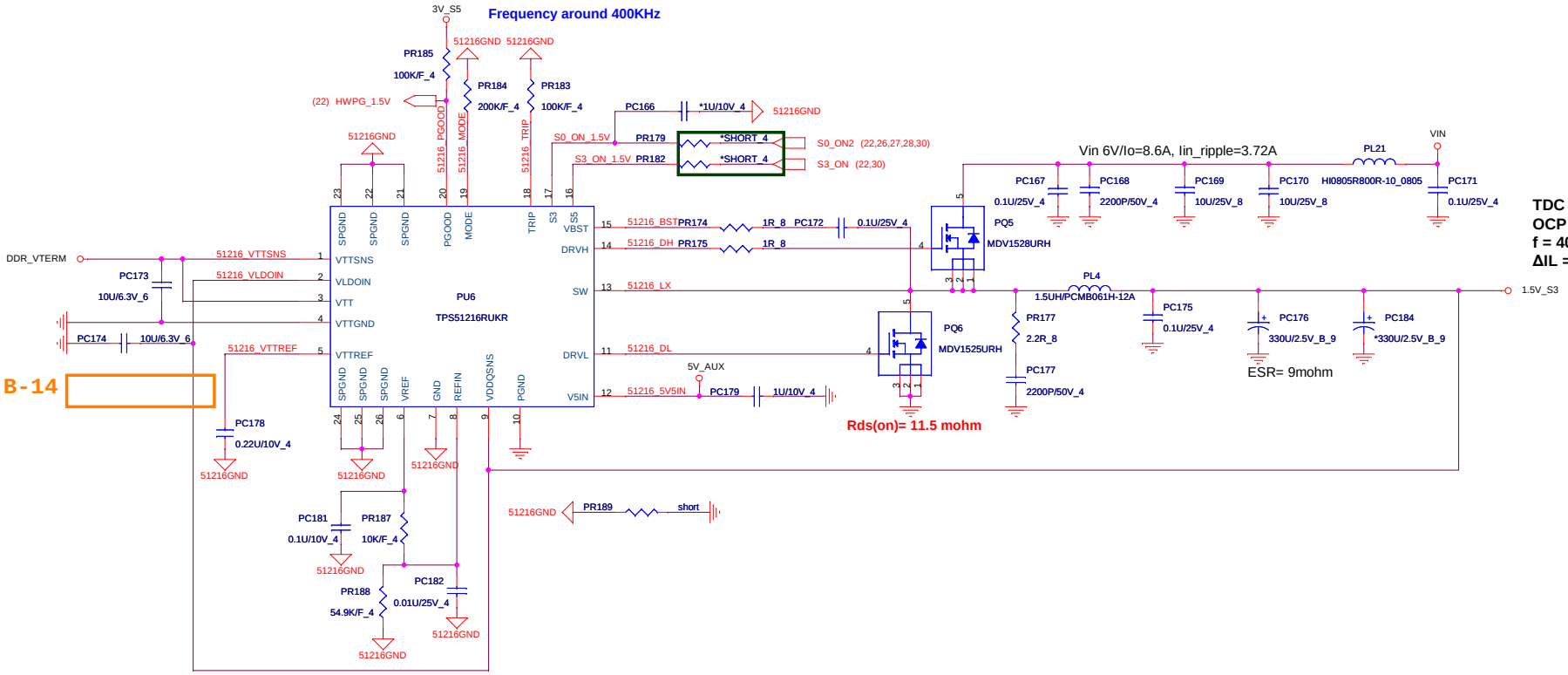
Quanta Computer Inc.
PROJECT : VZ3
Size | Document Number: SYSTEM 3V/5V (TPS51225RUKR) | Rev 1A
Date: Saturday, April 21, 2012 | Sheet 23 of 36

CPU_CORE (ISL95837HRZ-T)



Quanta Computer Inc.
PROJECT : VZ3
Size
Document Number
SYSTEM 3V/5V (TPS51225RUKR)
Rev 1A
Date: Saturday, April 21, 2012
Sheet 24 of 36

DDR3 1.5V_S3 (TPS51216RUKR)



Iripple=(Vin-Vout)*Vout/(Vin*L*f)

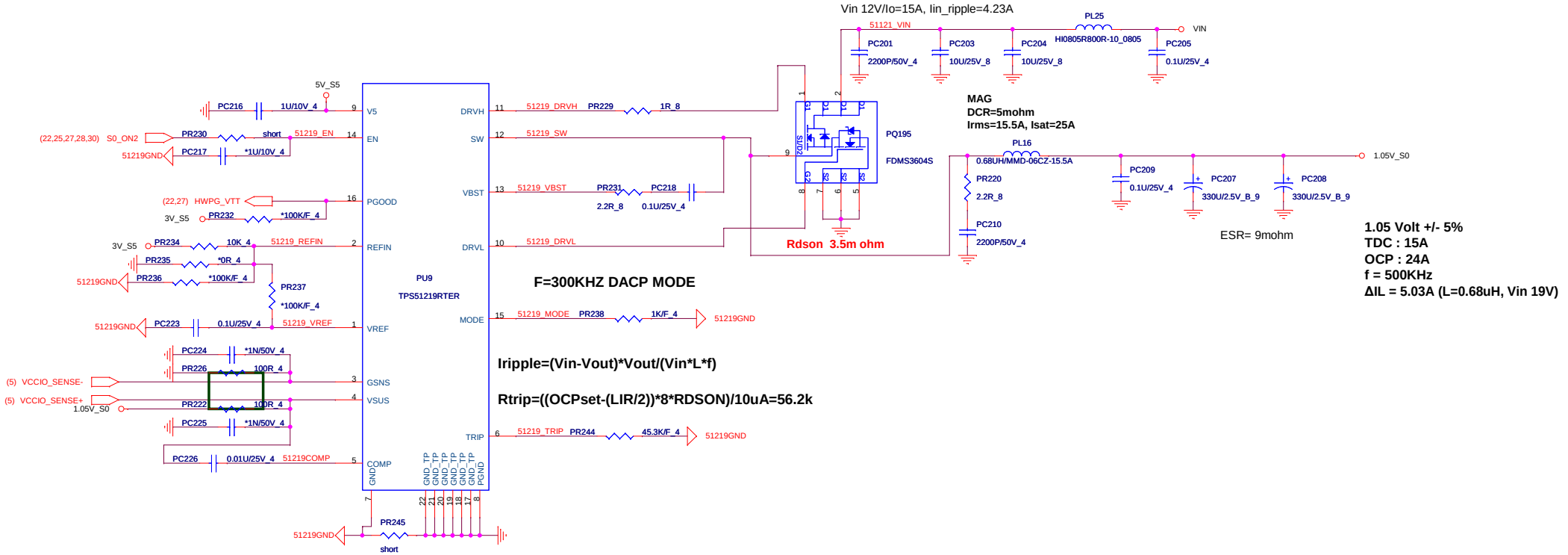
O.C.P setup information

Output	Mos Rds_on	I_OCP	OC_ΔIL(A)	Freq(KHz)	Inductor	R_TRIP
1.5V	12m_Max	10.5	2.3	400	1.5uH	11.5K

L/S Mosfet parameter

Mosfet	Package	ID (Ta=25C)	Rds_on_max
FDMC7692S	DFN 3*3	12.5A/18A	12m
AON7702	DFN 3*3	13.5A/20A	14m

VCCIO and 1.05V_PCH (TPS51219RTER)



VCCIO_SENSE- connect to the GND sense point of the load
VCCIO_SENSE+ connect to the load voltage sense point.

Output Voltage Selection

RFIN=3.3V	output voltage=1.05V
RFIN=GND	output voltage=1.00V
Resister Divider	Adjutable from VREF

Inductor information

Value	Vendor	QCI P/N	Irms(A)	Isat(A)	Rdc (ohm)	Size
1uH 20%	CYN	CV-10I0MZ04	18	28	3.3m Max.	11X10X4
1uH 20%	MAG Layer	CV-10L0MZ28	21	30	3.1m Max.	11X10X4

O.C.P setup information

Output	Mos Rds_on	I_OCP	OC_ΔIL(A)	Freq(KHz)	Inductor	R_TRIP
1.05V	4.3m_Max	18	3.306	300	1uH	56.2K

Quanta Computer Inc.
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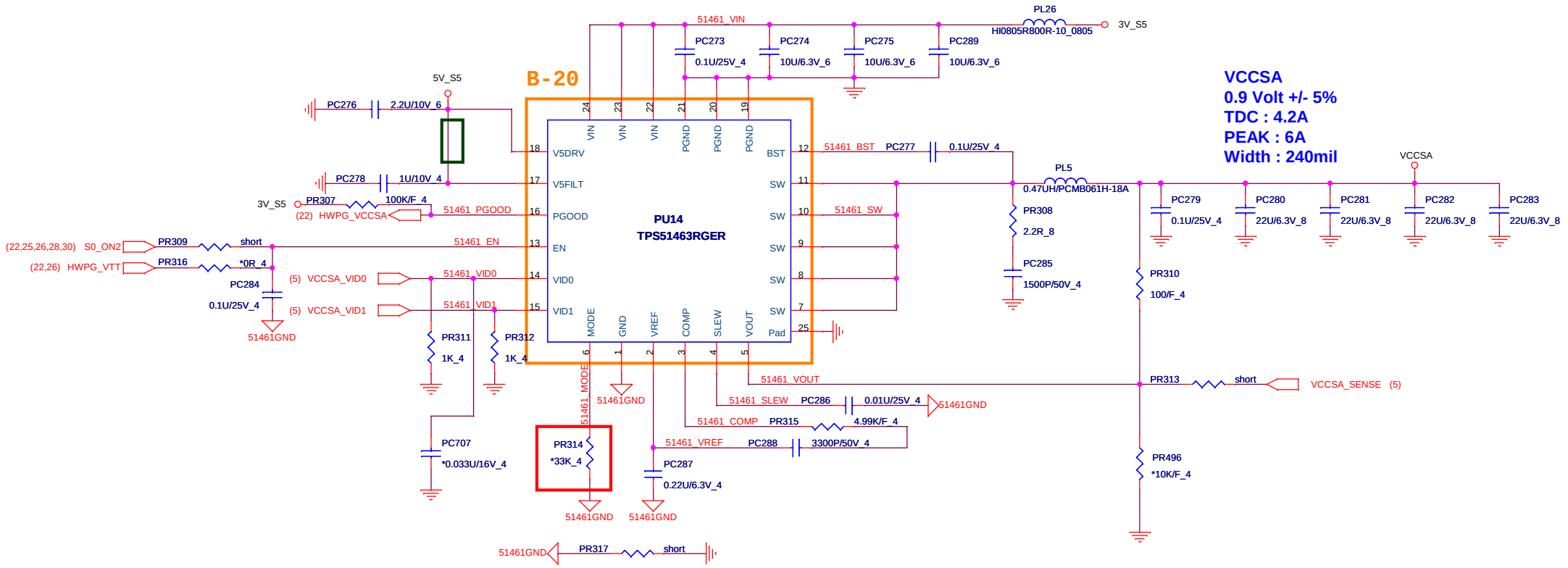
VCCSA (TPS51463RGER)



VCCSA PWM IC(PU14) Controller

CPU	Vendor P/N	QCI P/N	PR314	QCI P/N
Sandy Bridge	TPS51461RGER	AL051461000	33K	CS33302FB14
IVY Bridge	TPS51463RGER	AL051463000	NA	

IVY Bridge Table

VID0	VID1	VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.750V

Sandy Bridge Table

VID0	VID1	VCCSA
0	0	0.9V
0	1	0.85V
1	0	Note
1	1	Note

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	VCCSA (TPS51463RGER)	1A

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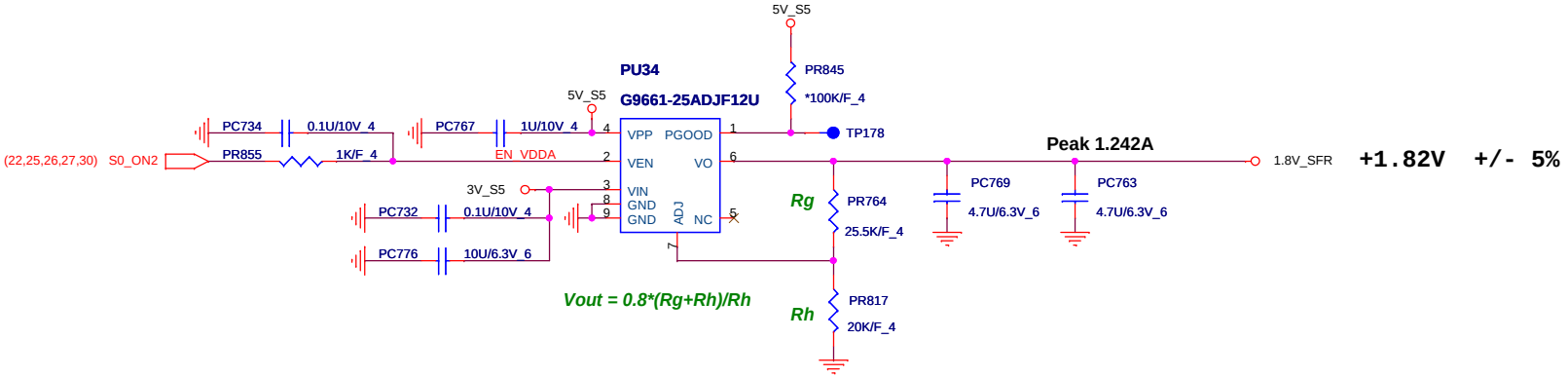
1.8V_SFR (G9661-25ADJF12U)



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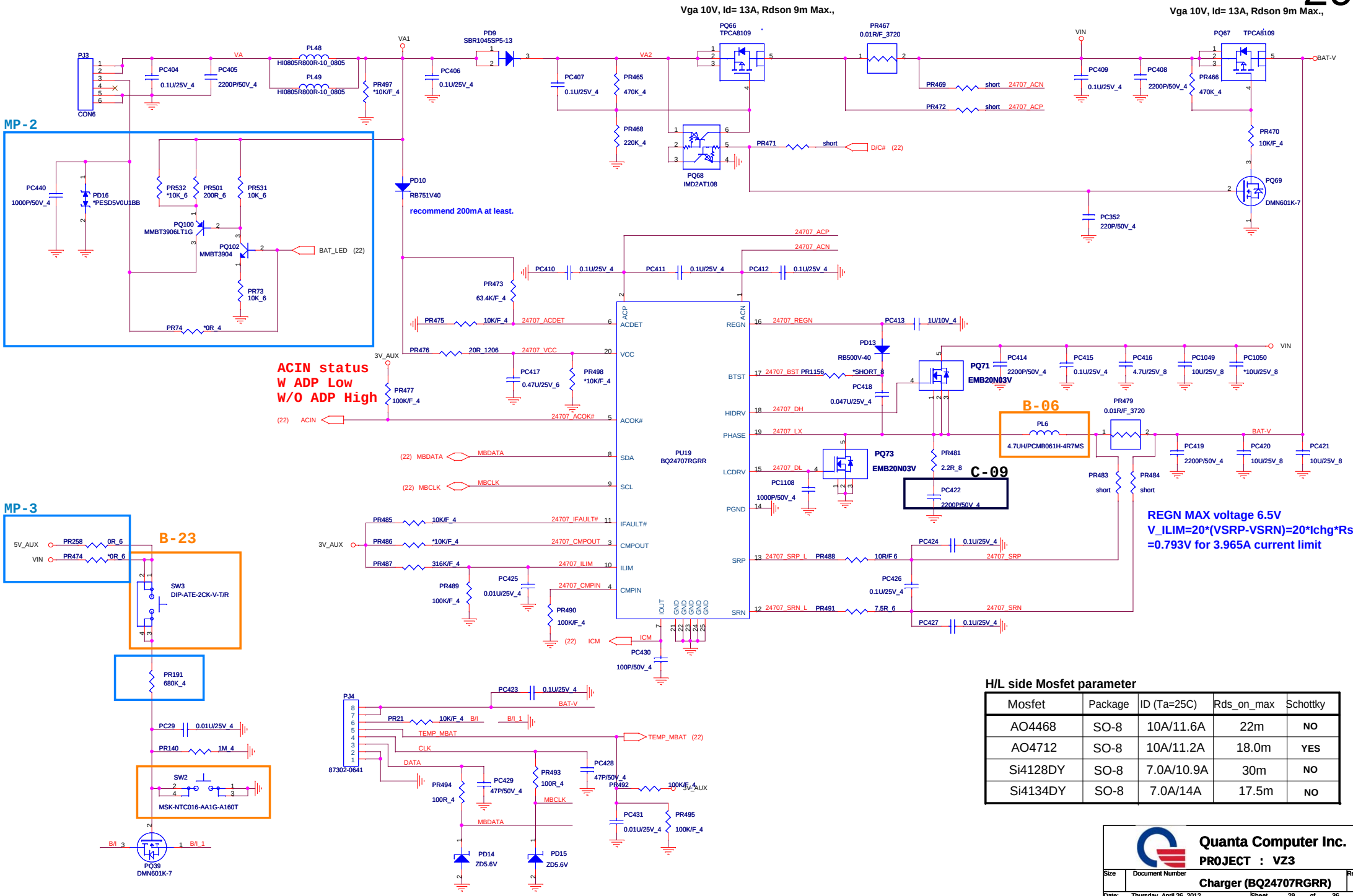
Adapter/Battery input & Charger



H/L side Mosfet parameter

Mosfet	Package	ID (Ta=25C)	Rds_on_max	Schottky
AO4468	SO-8	10A/11.6A	22m	NO
AO4712	SO-8	10A/11.2A	18.0m	YES
Si4128DY	SO-8	7.0A/10.9A	30m	NO
Si4134DY	SO-8	7.0A/14A	17.5m	NO

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Charger (BQ24707RGRR)
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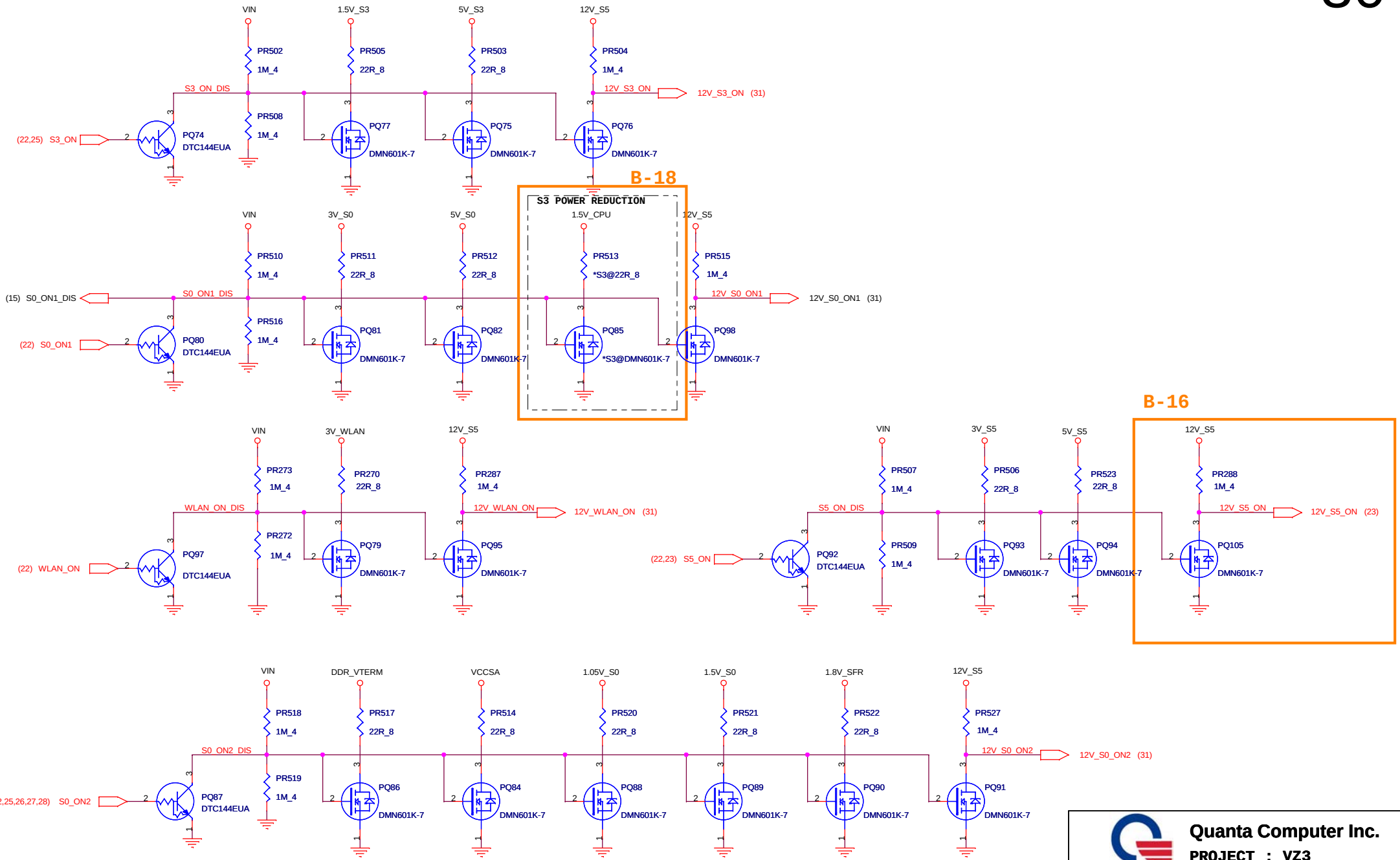
Power rail discharge



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	Power rail discharge	3A
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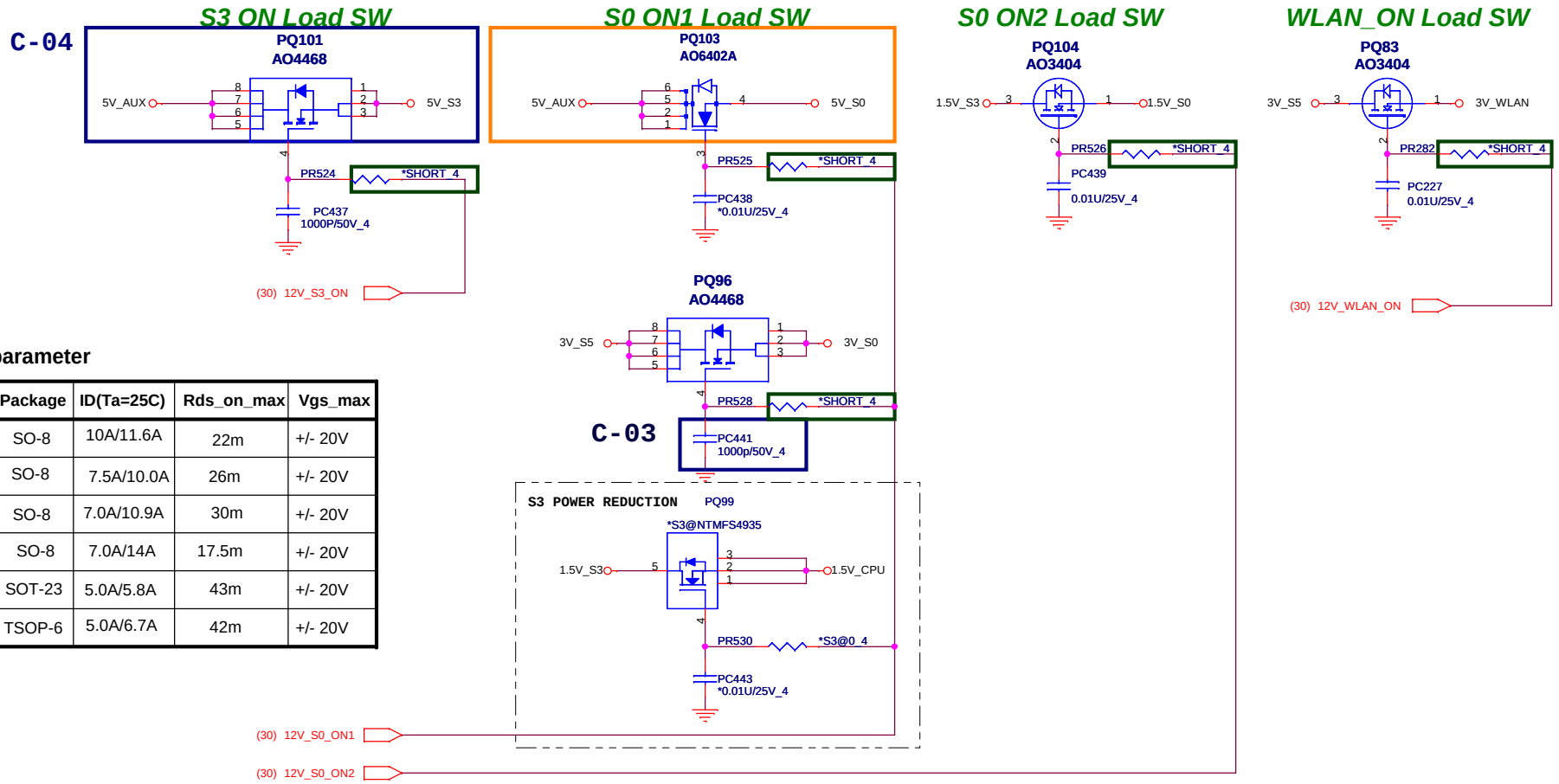
Load Switch



Mosfet parameter

Mosfet	Package	ID(Ta=25C)	Rds_on_max	Vgs_max
AO4468	SO-8	10A/11.6A	22m	+/- 20V
AO4496	SO-8	7.5A/10.0A	26m	+/- 20V
Si4128DY	SO-8	7.0A/10.9A	30m	+/- 20V
Si4134DY	SO-8	7.0A/14A	17.5m	+/- 20V
AO3404	SOT-23	5.0A/5.8A	43m	+/- 20V
ME3424D	TSOP-6	5.0A/6.7A	42m	+/- 20V

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	Load SW	1A
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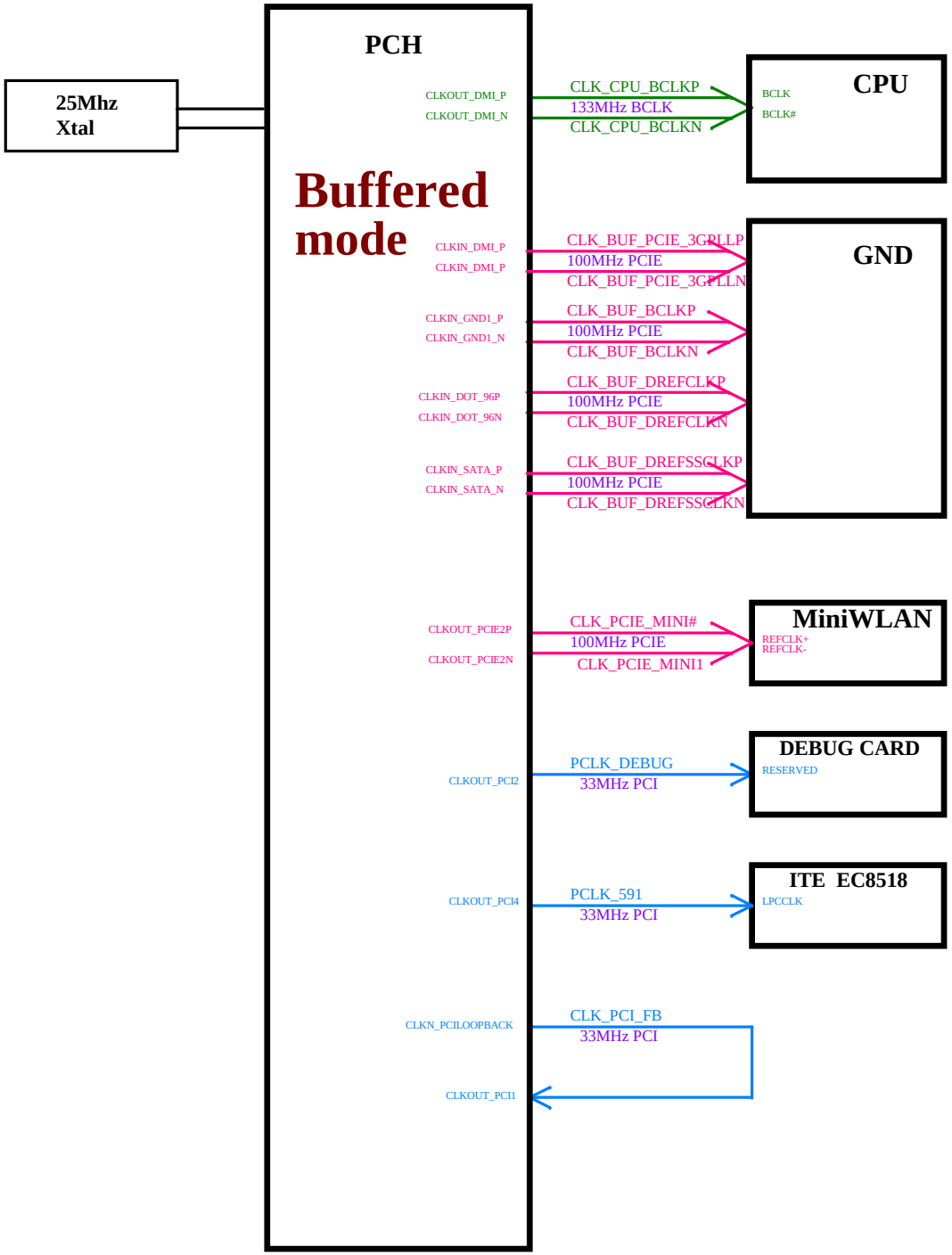

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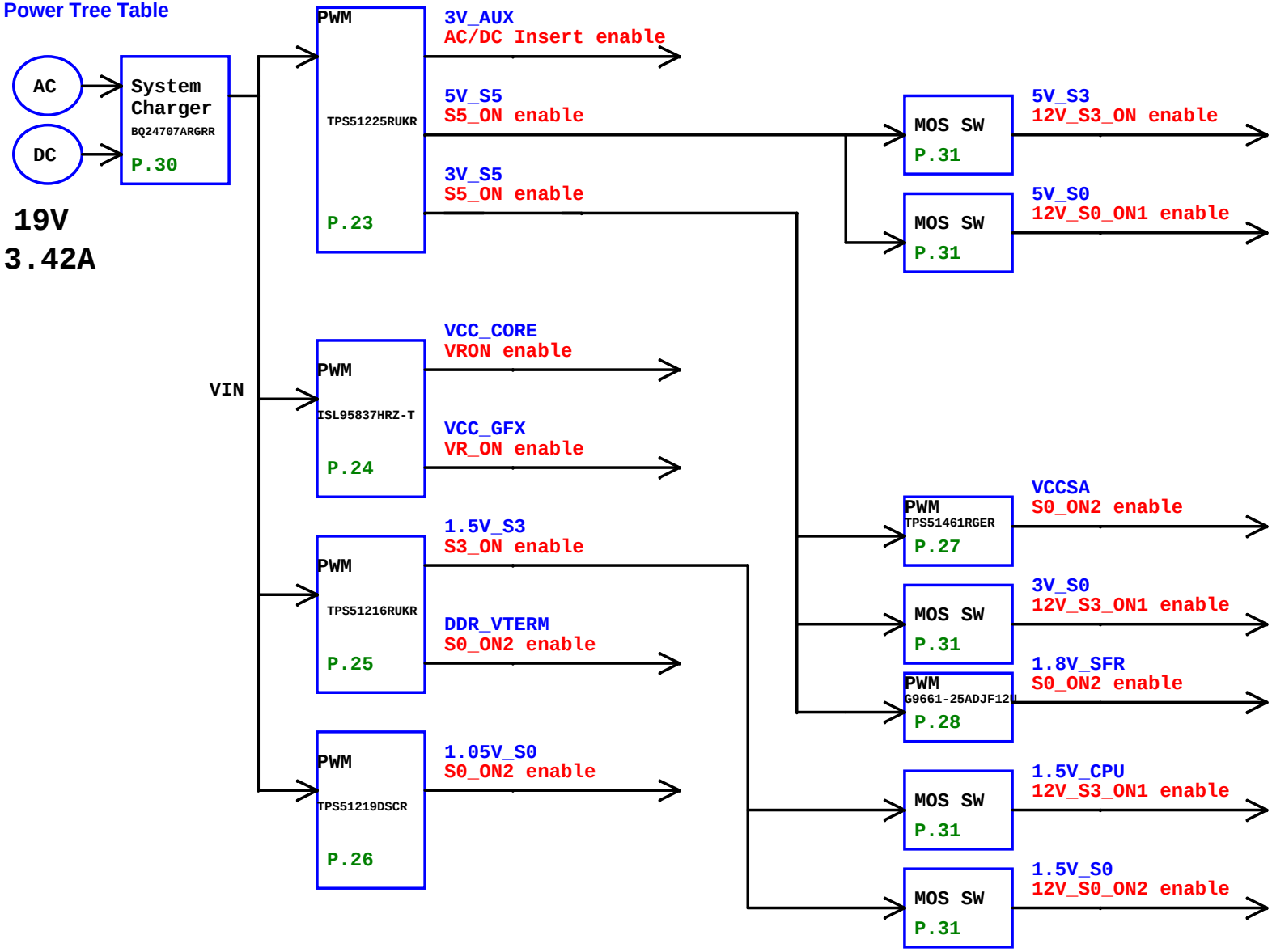
Power Tree Table



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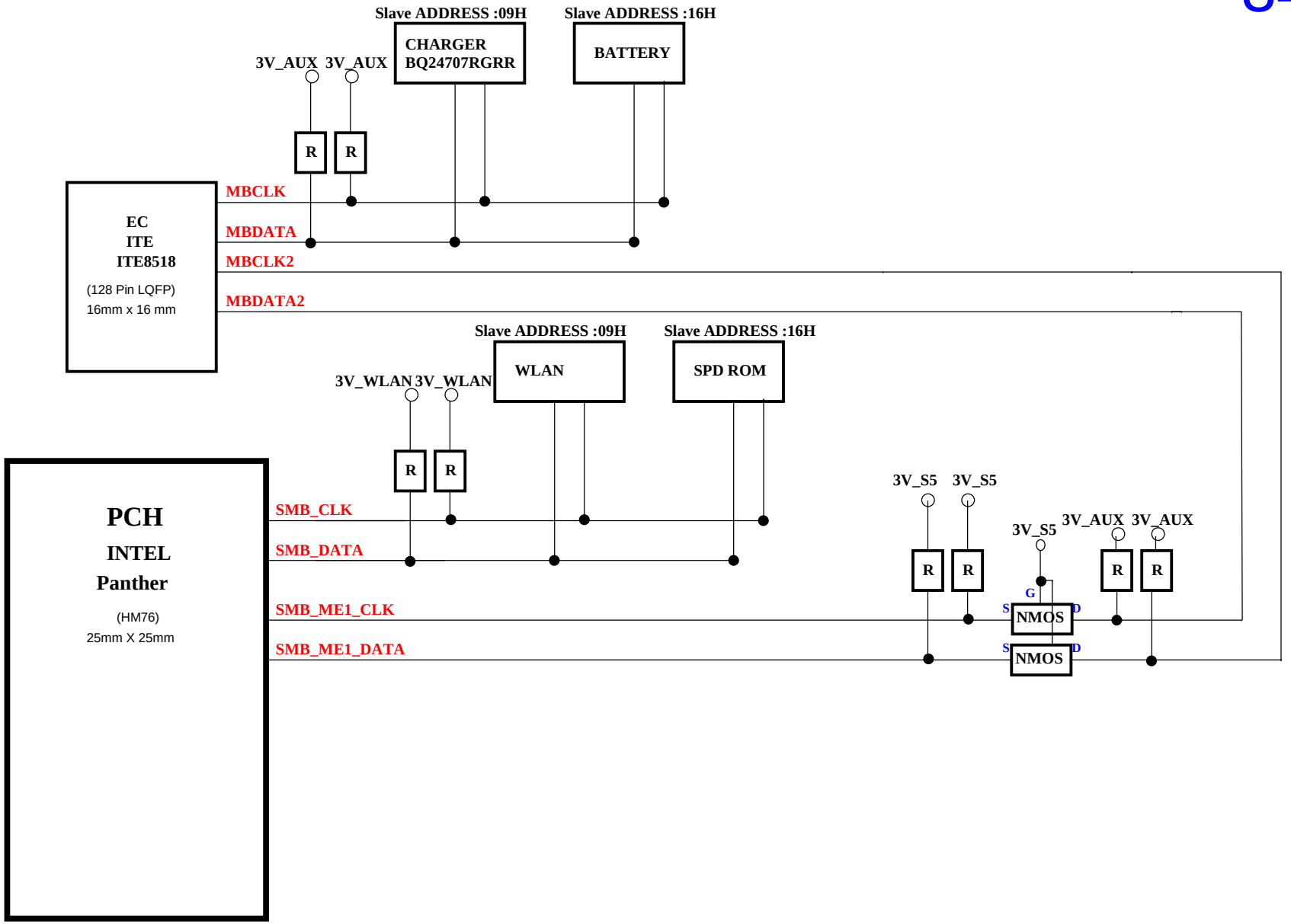

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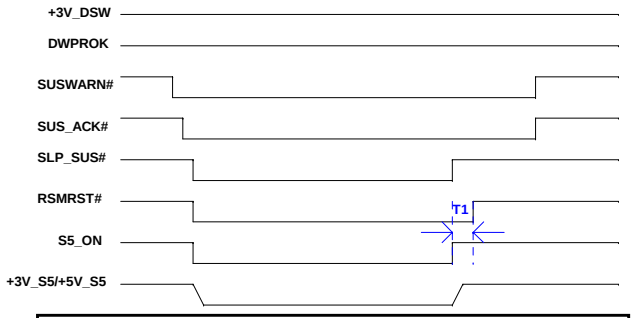
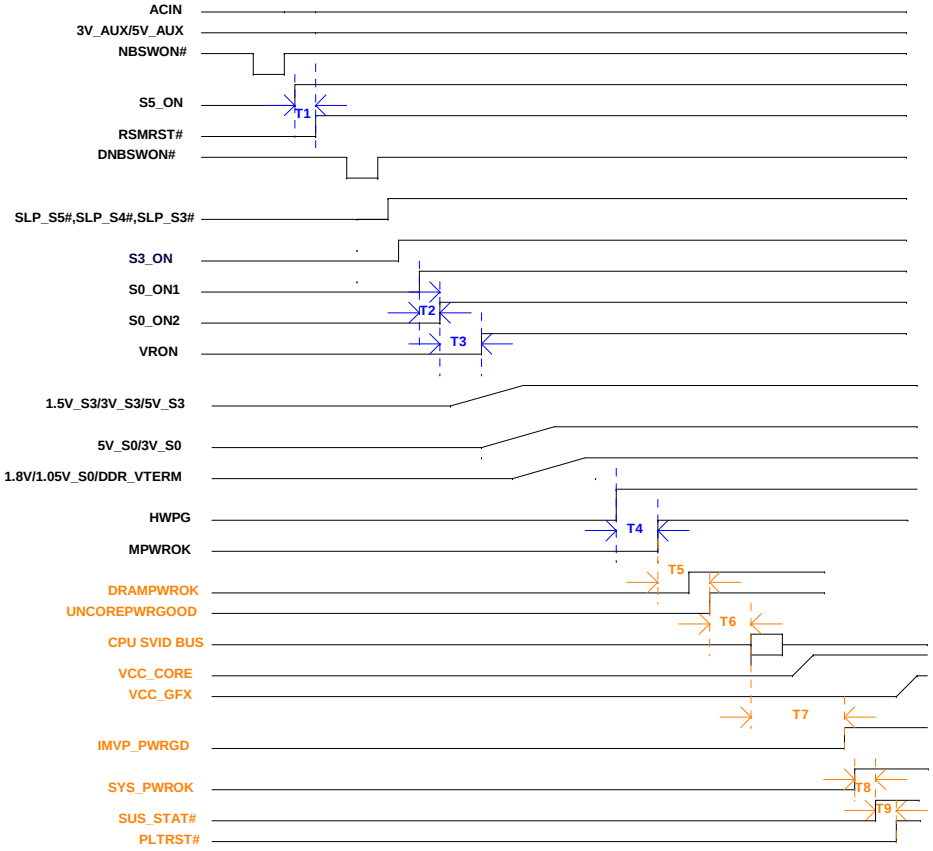
Deep S4/S5 off-on Sequence



Deep S4/S5 Sequence
T1: S5_ON TO RSMRST# = 30ms (spec:mini 10ms)

System Power-ON Sequence



System Power Sequence

EC Control:
T1: S5_ON TO RSMRST# = 20ms (spec:mini 10ms)
T2: S0_ON1 TO S0_ON2 = 500us
T3: S0_ON2 TO VRON = 10ms
T4: HWPG TO MPWROK = 110ms (spec:mini 99ms)
Note:HWPG NEED TO BE HIGH at that time

System:
T5: MPWROK to UNCOREPWRGOOD =2ms(Min)
T6: UNCOREPWRGOOD to SVID Packet =500us(Max)
T7: SVID Packet to IMVP_PWRGD =5ms(Max)
T8: SYS_PWROK to SUS_STAT# =1ms(Min)
T9:SUS_STAT# to PLTRST# =60us(Min)

Model	REV	CHANGE LIST
VZ1 MB	B	B-01.Add EMI solution B-02.Change CN14 LED connector B-03.Add keyboard EMI solution B-04.Add AR16 pull high B-05.PR1127 CHANGE FROM 1.82K TO 1.87K,PR1122 CHANGE FROM 1.87K TO 1.78K,PR1108, PR1154 CHANGE FROM 6.98KTO 6.2K for VCC_CORE loline B-06.PL6 CHANGE FROM 6.8UH TO 4.7UH for charge current change to 0.5C. B-07.JS7 CHANGE TO SWITCH , PR474 CHANGE FROM 680K TO 1M,PC88 , PR20 DELETE B-08.PQ101& PQ103 CHANGE FROM A03404 TO A06402A,PC437 CHANGE FROM 2200P TO 1000P B-09.Del D6 for HDMI power issue B-10.NA AC37 , AC40 , ADD AC31,AC32,AC35,AC38 100P , AL5,AL6,AL7,AL8 CHANGE FROM 0OHM TO BEAD for SPK CIRCUIT. B-11.ADD U39 for TO EC ADC PIN B-12.ADD AL9 , AL10 bead for EMI . B-13.ADD C364 , C372, C1018, C1019, C1020, C1021 cap for EMI request B-14.Del PR181 SMDDR_VREF power source B-15.Change power source to 3V_DSW B-16.Add 5V_AUX switch MOSFET & Discharger B-17.add pc1051,pc1052,pc1053,pc1016,pc291,pc292,pc293 for cpu loline B-18.add 1.5V_CPU Power rail discharge B-19.Change SM_VREF Power rail to 1.5V_CPU B-20.change from PR314 remove TPS51461RGER(AL051461000) to TPS51463RGER(AL051463000) B-21.PR1138 change from 2.37K(CS22372FB11) to 3.16K(CS23162FB04) B-22.Del R172,R504,C292 for KB remove POWER LED,Add R436 pull hi for KB_DEL B-23.Change POWER SWITCH SW1 to DHPPL9A1500,add SW2 & SW3
	C	C-01.Del R233 for cost down C-02.Add SMBus for touch pad vendor request C-03.Add PC441 to 1000P for SSD not found issue C-04.Change AO6402 to AO4468 for power noise issue C-05.Add PC440 for EMI request C-06.Change AL12 , AL13 to bead for EMI. C-07.Add C80 10P for EMI. C-08.Add AC1,AC2,AC3,AC5,AC11,AC12 to 1000P for EMI. C-09.Add PC422 to 2200P for EMI.
	MP-1	MP-1.add AU6(LMV331SN3T1G) , AR32(0OHM) , AR27(12K) , AR26(10K) , change AR66 to 6.8K . MP-2.Add PR532(10K) , PR501(10K) , PR531(10K) , PQ100(MMBT3906) , PQ102(MMBT3904) , PR73(10K) . MP-3.Add PR258(0OHM) , PR191(680K) , NA PR474(1M) . MP-4.Add D33 MP-5. change AJK1

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Size: Document Number: Change list Rev: 1A		PART NUMBER:	DRAWING BY:	REVISON:	2A
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