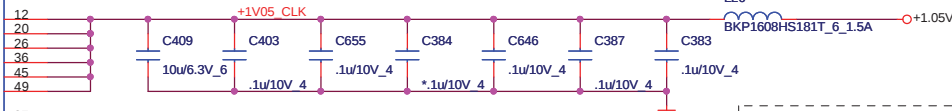
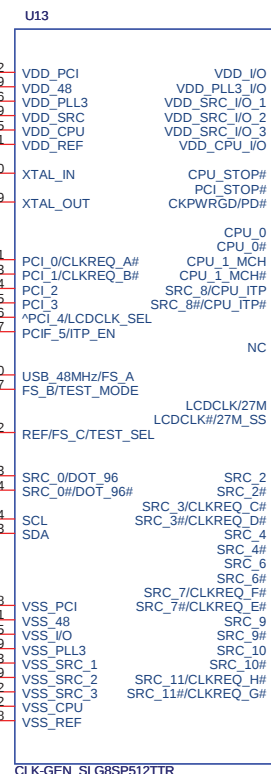
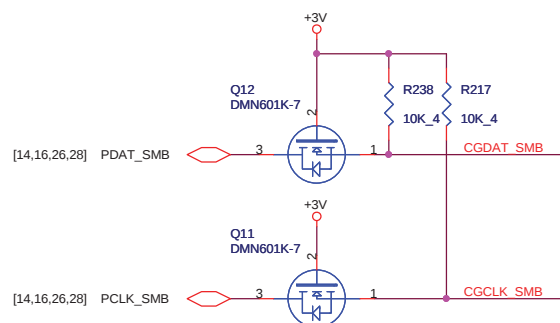
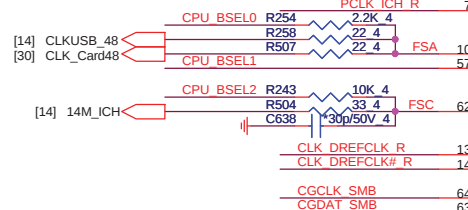
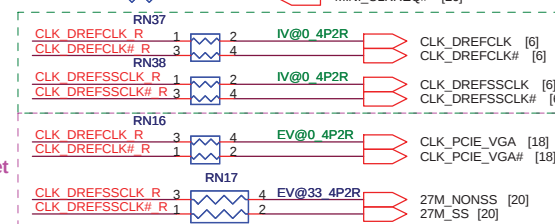
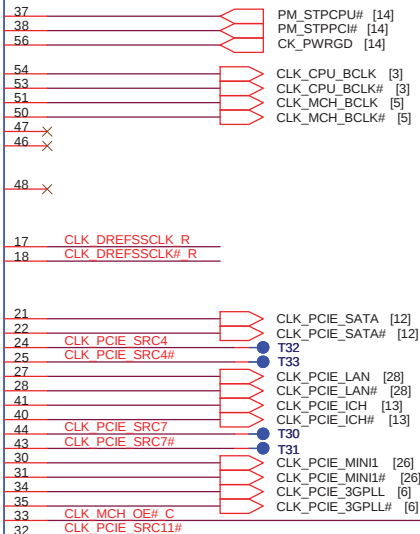


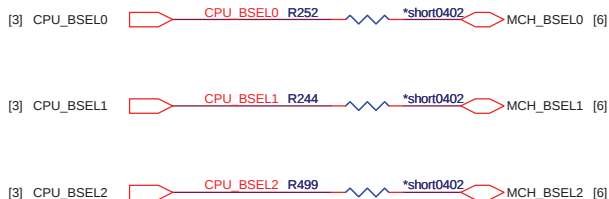
C647	*10p/50V 4	PCLK_DEBUG R
C371	*10p/50V 4	PCLK_591 R
C641	*10p/50V 4	PCLK_ICH R
C648	*10p/50V 4	FSA



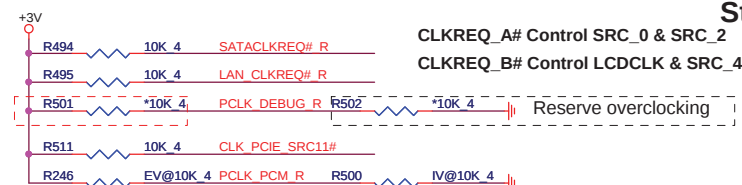
Pin 56 : It acts as a level sensitive strobe to latch the FS pins and other multiplexed inputs.



Pin 10/57/62 : For Pin CPU frequency selection



FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz



Pin 6 : For Pin 13/14 and 17/18 selection
0 = LCDCLK & DOT96 for internal graphic controller support
1 = 27M & 27M SS & SRC 0 for external graphic controller support

Pin 7 : For Pin 46/47 selection
1 = CPU_ITP
0 = SRC 8

Strap table



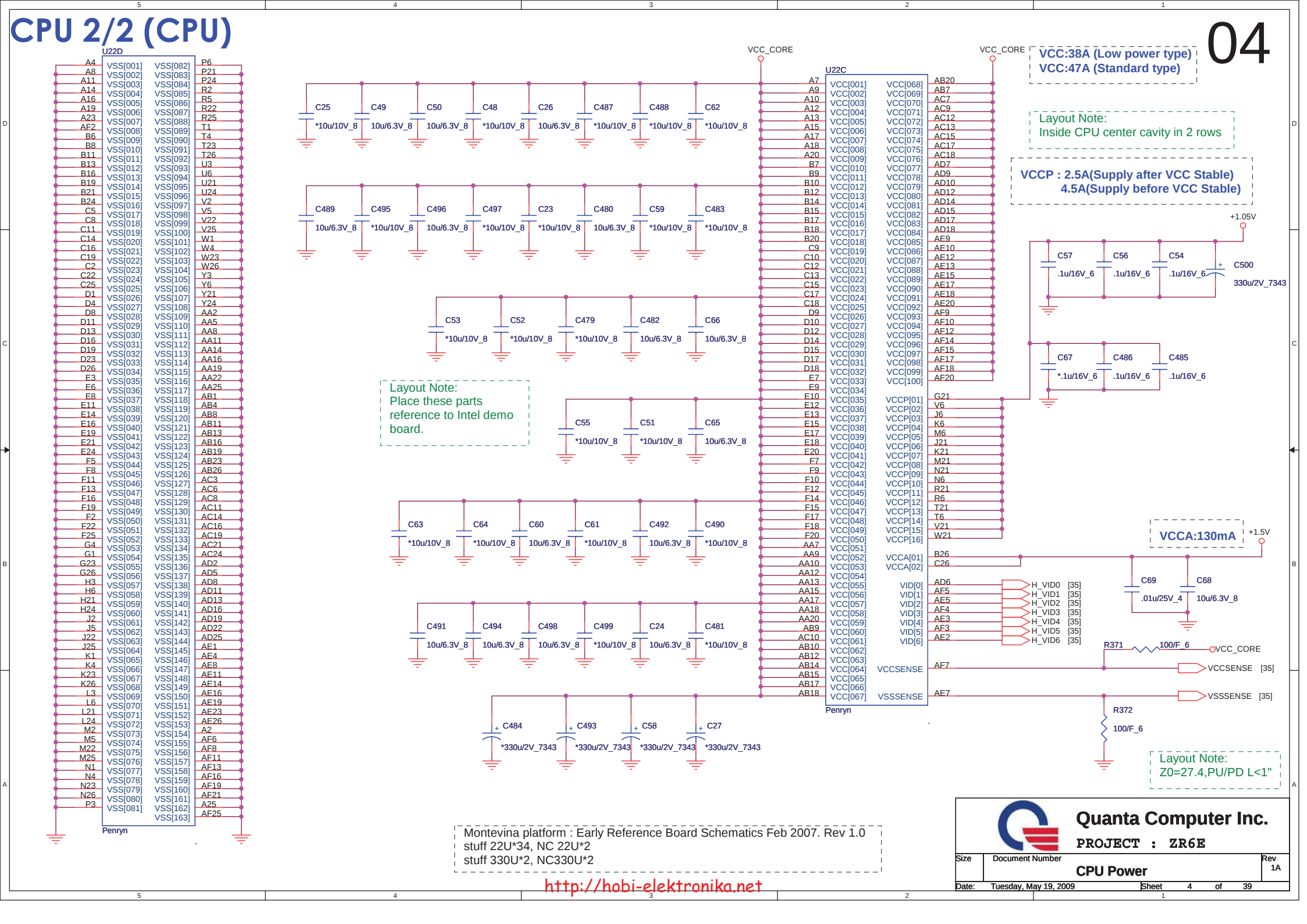
PROJECT : ZR6E

Size	Document Number	Rev
	CLOCK GENERATOR	1A
Date:	Tuesday, May 19, 2009	Sheet 2 of 39



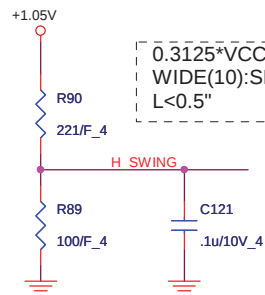
CPU Thermal monitor (THM)



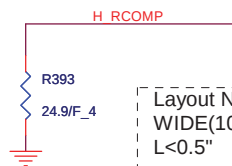


GMCH-CANTIGA(CLG)

	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06
Intel Cantiga (G)L A1	AJSLGGM0T04

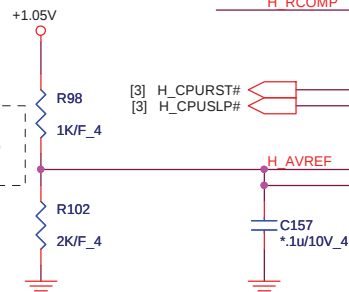


0.3125*VCCP
WIDE(10):SPACING(20) ,
L<0.5"



Layout Note:
WIDE(10):SPACING(20) ,
L<0.5"

2/3*VCCP
WIDE(10):SPACING(20),
L<0.5"



[3] H_CPURST#
[3] H_CPUSLP#

H SWING C5
H RCOMP E3

U28A

H D#0 F2
H D#1 G8
H D#2 F8
H D#3 E6
H D#4 G2
H D#5 H6
H D#6 H2
H D#7 F6
H D#8 D4
H D#9 H3
H D#10 M9
H D#11 M11
H D#12 J1
H D#13 J2
H D#14 N12
H D#15 J6
H D#16 P2
H D#17 L2
H D#18 R2
H D#19 N9
H D#20 L6
H D#21 M5
H D#22 J3
H D#23 N2
H D#24 R1
H D#25 N5
H D#26 N6
H D#27 P13
H D#28 N8
H D#29 L7
H D#30 N10
H D#31 M3
H D#32 Y3
H D#33 AD14
H D#34 Y6
H D#35 Y10
H D#36 Y12
H D#37 Y14
H D#38 Y7
H D#39 W2
H D#40 AA8
H D#41 Y9
H D#42 AA13
H D#43 AA9
H D#44 AA11
H D#45 AD11
H D#46 AD10
H D#47 AD13
H D#48 AE12
H D#49 AE9
H D#50 AA2
H D#51 AD8
H D#52 AA3
H D#53 AD3
H D#54 AD7
H D#55 AE14
H D#56 AF3
H D#57 AC1
H D#58 AE3
H D#59 AC3
H D#60 AE11
H D#61 AE8
H D#62 AG2
H D#63 AD6

H D#_0
H D#_1
H D#_2
H D#_3
H D#_4
H D#_5
H D#_6
H D#_7
H D#_8
H D#_9
H D#_10
H D#_11
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H D#_60
H D#_61
H D#_62
H D#_63

HOST

H_A#_3
H_A#_4
H_A#_5
H_A#_6
H_A#_7
H_A#_8
H_A#_9
H_A#_10
H_A#_11
H_A#_12
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H_A#_29
H_A#_30
H_A#_31
H_A#_32
H_A#_33
H_A#_34
H_A#_35

H_ADS#
H_ADSTB#_0
H_ADSTB#_1
H_BNR#
H_BPR#
H_BREQ#
H_DEFER#
H_DBSY#
HPLL_CLK
HPLL_CLK#
H_DPWR#
H_DRDY#
H_HIT#
H_HITM#
H_LOCK#
H_TRDY#

H_DINV#_0
H_DINV#_1
H_DINV#_2
H_DINV#_3

H_DSTBN#_0
H_DSTBN#_1
H_DSTBN#_2
H_DSTBN#_3

H_DSTBP#_0
H_DSTBP#_1
H_DSTBP#_2
H_DSTBP#_3

H_REQ#_0
H_REQ#_1
H_REQ#_2
H_REQ#_3
H_REQ#_4

H_RS#_0
H_RS#_1
H_RS#_2

A14
C15
F16
H13
C18
M16
J13
P16
R16
N17
M13
E17
P17
F17
G20
B19
J16
E20
H16
J20
L17
A17
B17
L16
C21
J17
H20
B18
K17
B20
F21
K21
L20

H12
B16
G17
A9
F11
G12
E9
B10
AH7
AH6
J11
F9
H9
E12
H11
C9

J8
L3
Y13
Y1

L10
M7
AA5
AE6

L9
M8
AA6
AE5

B15
K13
F13
B13
B14

B6
F12
C8



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Size	Document Number	Rev 1A
GMCH HOST		
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U28

ME JTAG

CFG

PM

ME GRAPHICS VID

ME

NC

MISC

HDA

CLK DIR CLK/ CONTROL/COMPENSATION

RSVD

SA_CK_0

SA_CK_1

SA_CK_0

SA_CK_1

SA_CK_0

SA_CK_1

SA_CK_0

SA_CK_1

SA_CKE_0

SA_CKE_1

SA_CKE_0

SA_CKE_1

SA_CS_0

SA_CS_1

SA_CS_0

SA_CS_1

SA_ODT_0

SA_ODT_1

SA_ODT_0

SA_ODT_1

SM_RCOMP

SM_RCOMP#

SM_RCOMP_VOH

SM_RCOMP_VOL

SM_VREF

SM_PWROK

SM_REXT

SM_DRAMRST

DPLL_REF_CLK

DPLL_REF_CLK#

DPLL_REF_SSCLK

DPLL_REF_SSCLK#

PEG_CLK

PEG_CLK#

AE41

AE42

AE43

AE44

AE45

AE46

AE47

AE48

AE49

AE50

AE51

AE52

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AE452

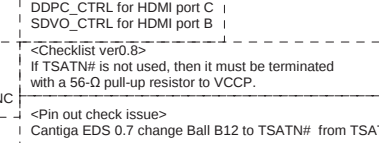
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AE455

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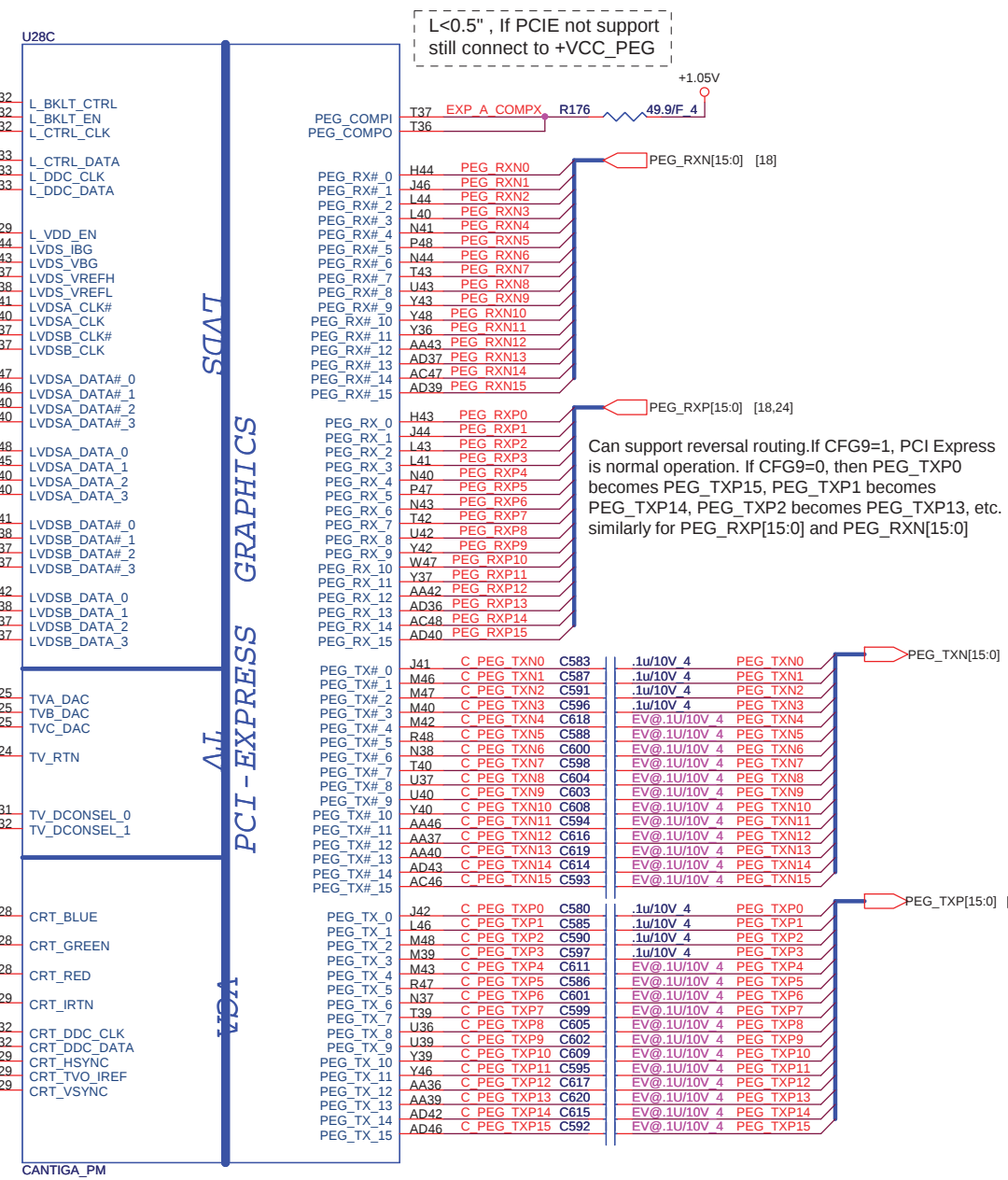
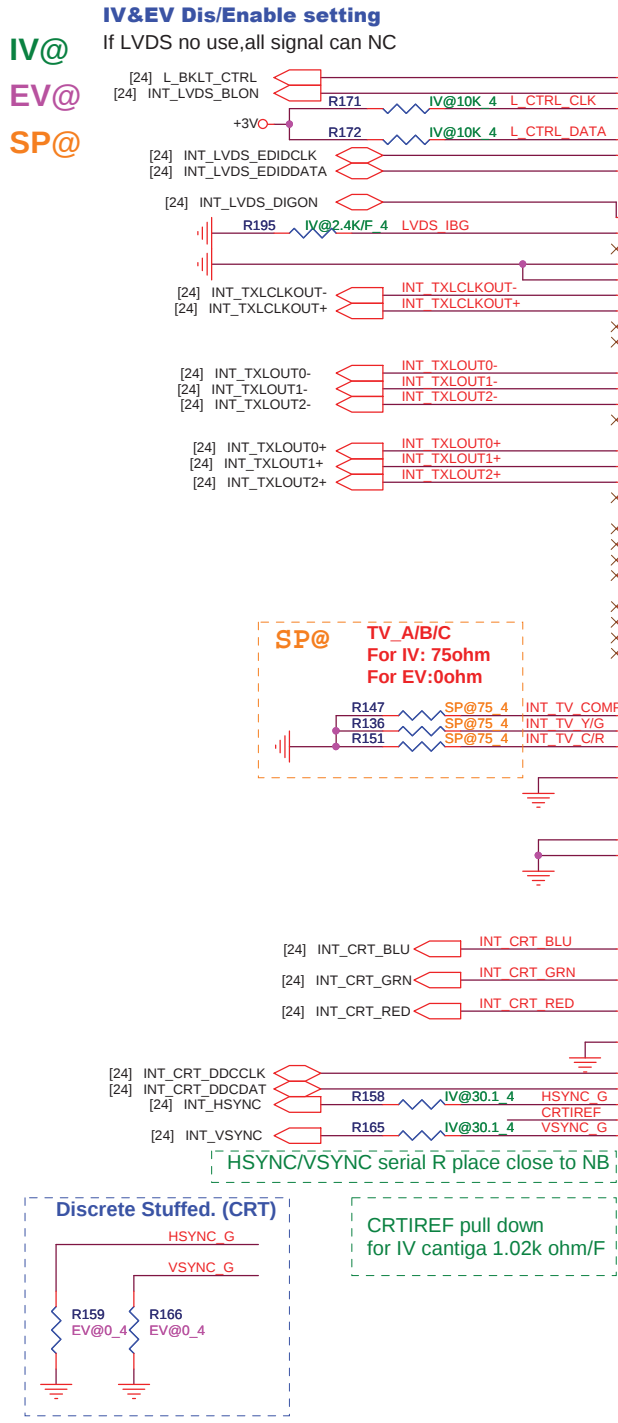
AE45



Impact ICH9M VCCHDA and VCCSUSDHDA supply 1.5V/3.3V

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSDHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

GMCH-CANTIGA(CLG)



IV&EV Dis/Enable setting
<5/31>Montevina_Schematics_Checklist_Rev0_8
a)For TVOUT Disabled, TV_DCONSEL[1:0] Connect to GND. But design guide Rev0.7 show NC.What is correct.
b)For CRT DAC Disable, CRT_DDC_CLK, CRT_DDC_DATA, CRT_HSYNC, CRT_VSYNCThese signals should be connected to GND. But design guide Rev0.7 show NC, Intel suggest follow Design guide.

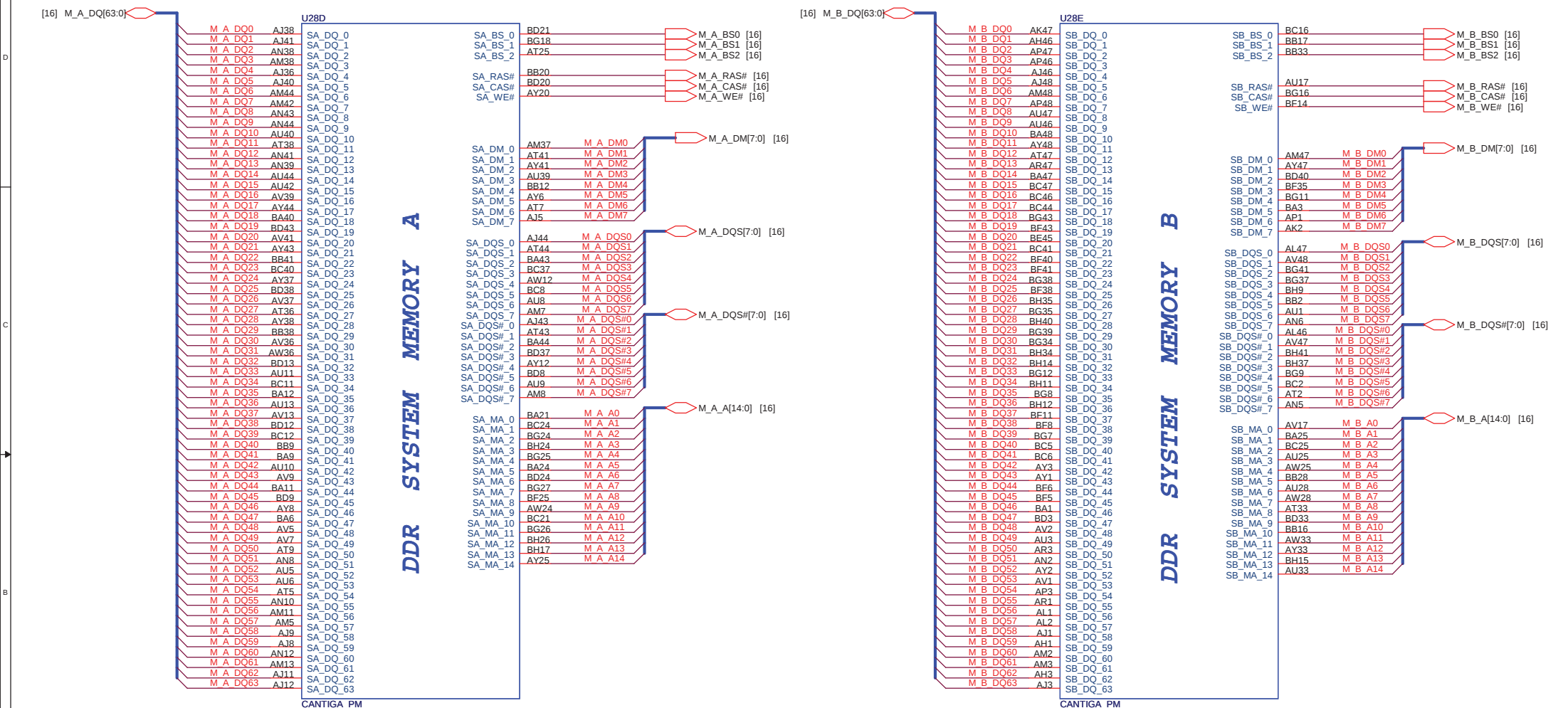
<check list>
For EV@
CRT R/G/B 0ohm to GND
CRTIREF 0ohm to GND

<check list>
For IV@
CRT R/G/B 150ohm to GND
CRTIREF 1Kohm to GND

For topology without the analog switch - if the total motherboard route length is less than 12", the recommended reference resistor value is 1 kΩ ±1%

CRTIREF
For IV: 1Kohm
For EV:0ohm

CRT R/G/B
For IV: 150ohm
For EV:0ohm



Quanta Computer Inc.

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	GMCH DDRII	
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Size Document Number **GMCH VCC,NCTF** Page 0 of 20

IV@
EV@
SP@

Power consumption reference to Intel Cantiga chipset EDS Volume1, Section 10

1210 10uH, 10%
0.45A DCR_max = 0.39

1.05V
64.8mA for DPLL A/B

1210 10uH, 10%
0.45A DCR_max = 0.39

1.05V
139.2mA

1210 0.1uH, 20%, 1A
DCR_max=0.078Ω

3.3V
24.15mA for VCCA_TV_DAC
39.48mA for VCCA_TV_DAC
24.15mA for VCCA_TV_DAC
Total 87.78mA

1.05V
157.2mA

1.5V
35mA

1.5V
48.363mA for CRT
5mA for IV

1.5V
157.2mA

1.5V
35mA

1.5V
48.363mA for CRT
5mA for IV

1.5V
157.2mA

1.5V
35mA

1.5V
48.363mA for CRT
5mA for IV

1.5V
157.2mA

1.5V
35mA

If CRT have Flicker issue
STUFF 5.6 ohm

IV&EV Dis/Enable setting

IV&EV Dis/Enable setting

SP@iNT use 0.01u
EXT use 0 ohm

SP@iNT use 0.1u
EXT use 0 ohm

SP@iNT use 0.01u
EXT use 0 ohm

SP@iNT use 0.1u
EXT use 0 ohm

SP@iNT use 0.01u
EXT use 0 ohm

SP@iNT use 0.1u
EXT use 0 ohm

SP@iNT use 0.01u
EXT use 0 ohm

SP@iNT use 0.1u
EXT use 0 ohm

SP@iNT use 0.01u
EXT use 0 ohm

SP@iNT use 0.1u
EXT use 0 ohm

SP@iNT use 0.01u
EXT use 0 ohm

SP@iNT use 0.1u
EXT use 0 ohm

SP@iNT use 0.01u
EXT use 0 ohm

SP@iNT use 0.1u
EXT use 0 ohm

SP@iNT use 0.01u
EXT use 0 ohm

SP@iNT use 0.1u
EXT use 0 ohm

SP@iNT use 0.01u
EXT use 0 ohm

VCCA_DPLLA always keep to +1.05V
(if no use IV dynamic core power)

USE same GND plane

1.8V
13.2mA

1.05V
50mA

1.05V
139.2mA

1.05V
157.2mA

1.05V
157.2mA

1.05V
157.2mA

1.05V
157.2mA

1.05V
157.2mA

1.05V
157.2mA

1.05V
157.2mA

1.05V
157.2mA

1.05V
157.2mA

1.05V
157.2mA

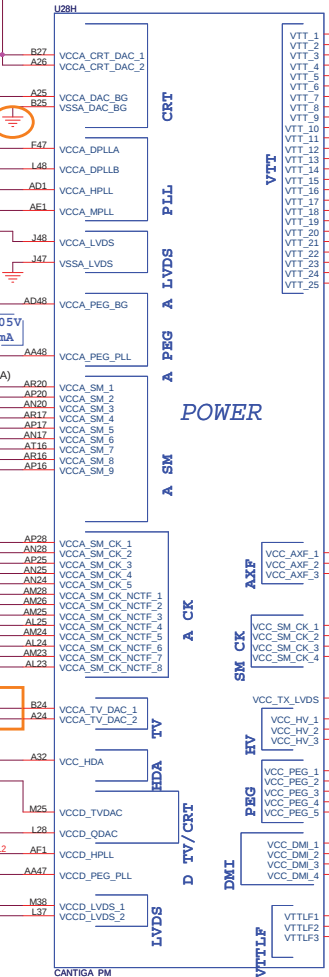
1.05V
157.2mA

1.05V
157.2mA

http://hobi-elektronika.net

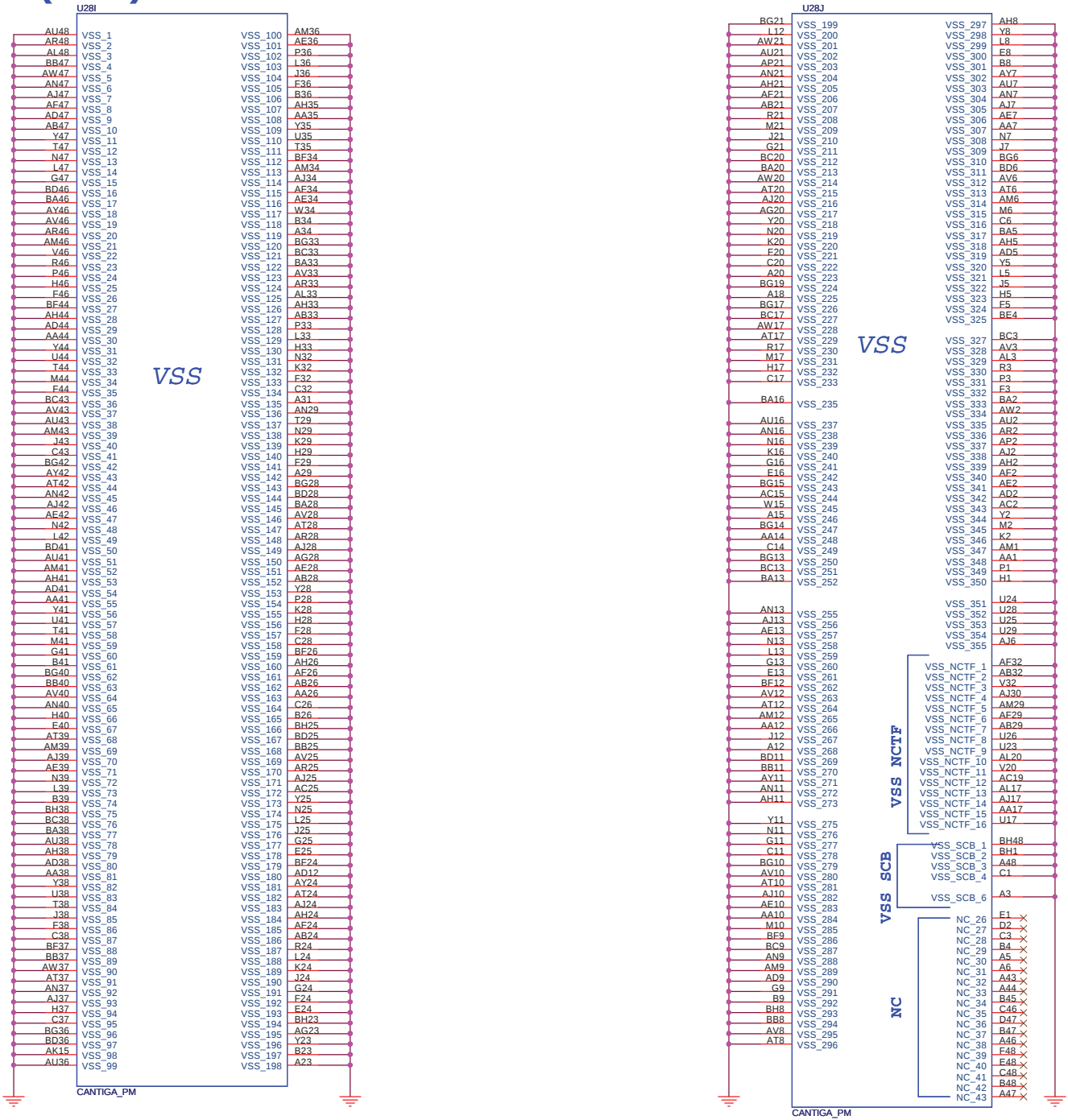
External Graphics
(GMCH Integrated Graphics Disable)

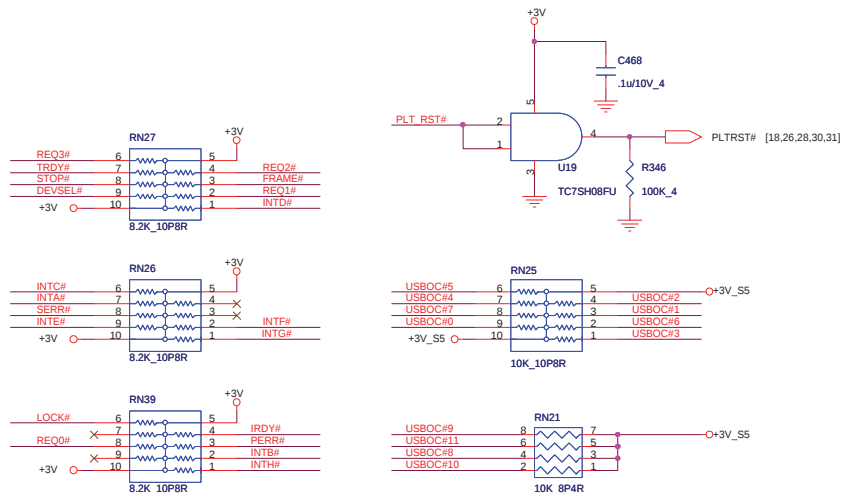
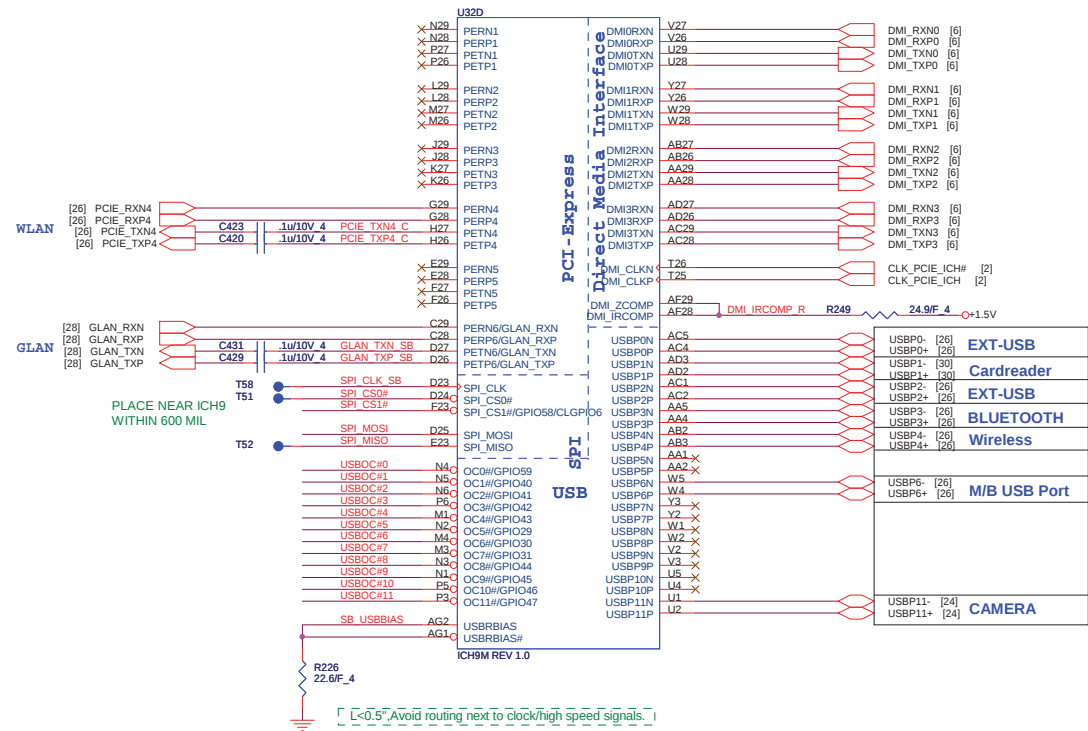
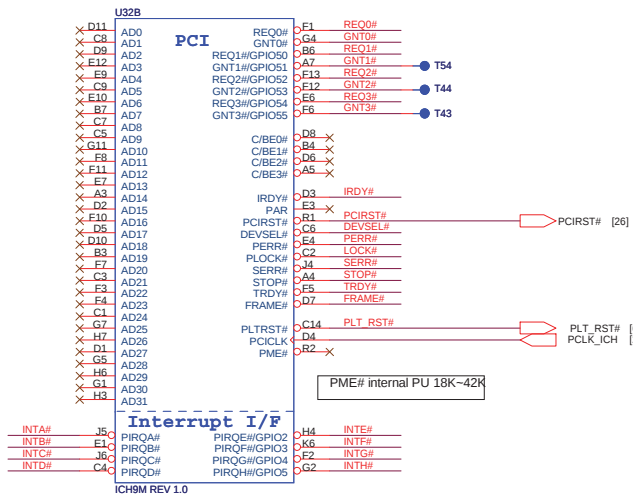
VCCSYNCR_CRT	GND
VCCA_CRT_DAC	GND
VCCD_LVDS	GND
VCCD_TX_LVDS	GND
VCCA_LVDS	GND
VCCA_TV_DAC	GND
VCCD_QDAC	GND
VCCA_DAC_BG	GND
VCC_AXG	GND
VCC_AXG_NCTF	GND



Power Net Name	Cantiga (V)
VCC_AXG_#	1.05V
VCC_AXG_NCTF_#	1.05V
VCCA_PEG_BG	1.5V
VCCA_DPLLA	1.05V
VCCA_DPLLB	1.05V
VCCA_SM_#	1.05V
VCCA_HPLL	1.05V
VCCA_MPLL	1.05V
VCCA_SM_CK_#	1.05V
VCCA_PEG_PLL	1.05V
VCCD_PEG_PLL	1.05V

GMCH-CANTIGA(CLG)

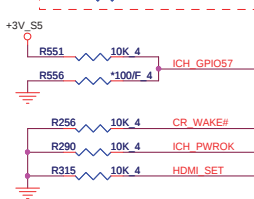
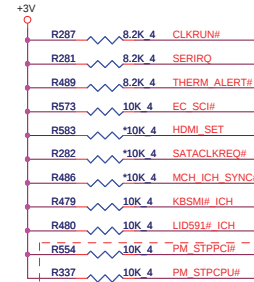
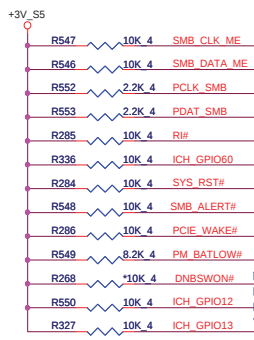




South Bridge Strap Pin (2/3)

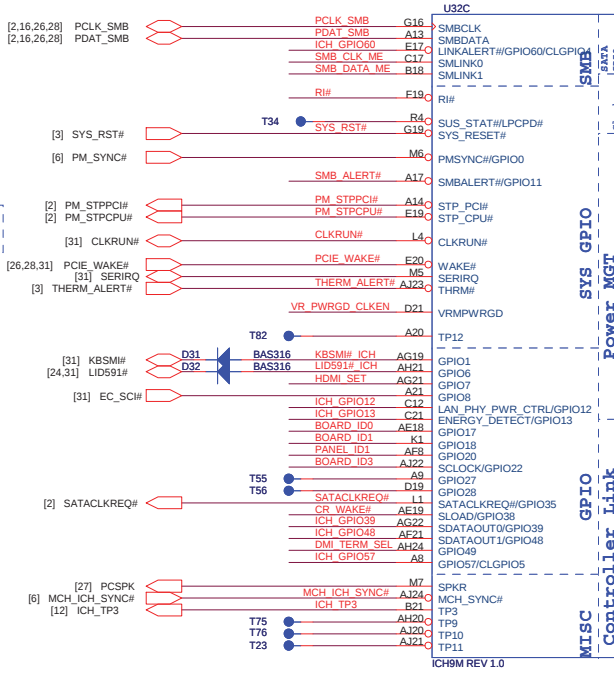
Pin Name	Strap description	Sampled	Configuration	PU/PD		
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0			
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default			
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default			
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default			
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable			
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0	SPI_CS#1	Boot Location	
			0	1	SPI	
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1	0	PCI	
			1	1	LPC(Default)	

ICH9M(CLG)

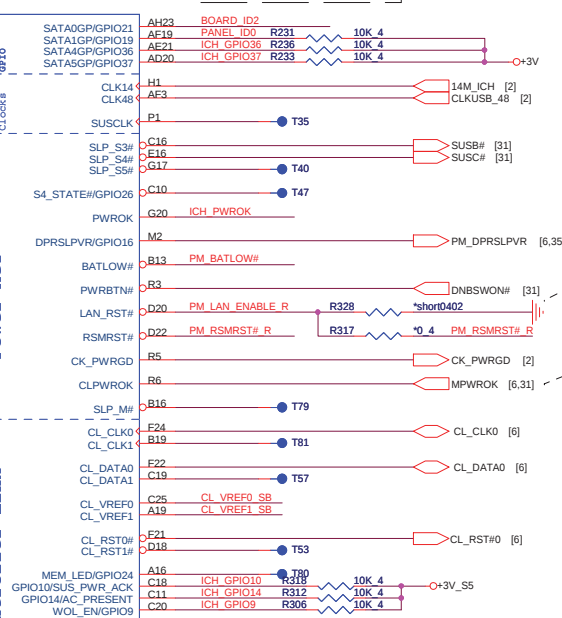


Stuﬀ	HDMI SET
R583	HDMI
R315	No HDMI

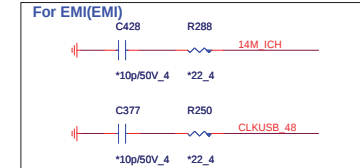
- D3A:(1/31) ASF issue:when iAMT is not implemented,
- ICH8M SMBus and SMLink should be connected together to support slave mode
- Connect SMLINK0 to SMBCLK and SMLINK1 to SMBDATA (Add R474,R475 for debug use)



SATA[x]GP pins if unused require
8.2-k to 10-k pull-up to Vcc3_3 or
8.2-k to 10-k pull-down to ground



ZS2 Default not
 support IAMS. So this
 interface follow
 CRB/Checklist PU
 only



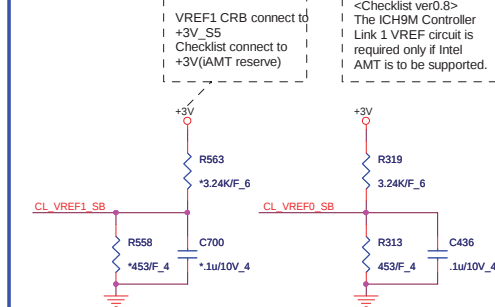
```

-----<Checklist ver0.8>-----
If integrated LAN is not used LAN_RST# tie it to GND.NC serial R from RSMRST#.
If Intel LAN is used with Wake On LAN, tie LAN_RST# to RSMRST# and NC 0ohm.

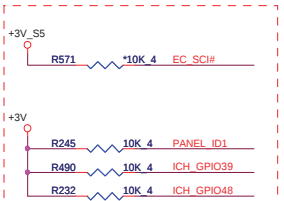
```

CL_PWROK must not assert after PWROK asserts for IAMT.
CL_PWROK to the NB and SB should be connected to existing PWROK inputs
on the NB and SB on a platform with no IAMT

CL VREF

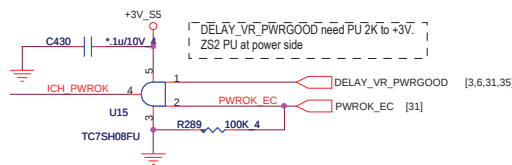


<Checklist ver0.8>
| The ICH9M Controller
| Link 1 VREF circuit is
| required only if Intel
| AMT is to be supported.

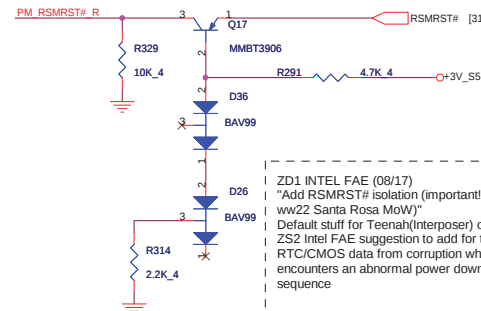


Follow CHECK LIST V1.5

ICH PWROK

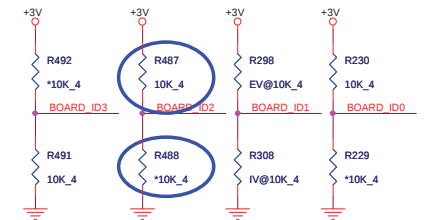


Resume RST



| ZD1 INTEL FAE (08/17)
 | "Add RSMRST# isolation (important!!! See
 | ww22 Santa Rosa MoW)"
 | Default stuff for Teenah(Interposer) chipset
 | ZS2 Intel FAE suggestion to add for to protect
 | RTC/CMOS data from corruption when system
 | encounters an abnormal power down
 | sequence

M/B ID ID0=0 -->ZK6 , ID0=1 -->ZR6
ID1=0 -->UMA , ID1=1 -->Discrete

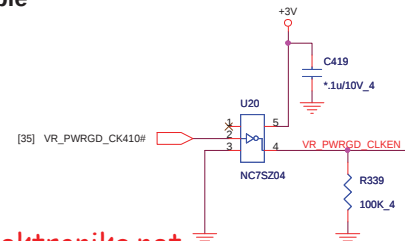


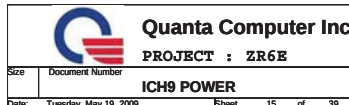
Board ID	ID3	ID2	ID1	ID0
A-SMT,ID1=0 -->UMA ,ID1=1 -->Discrete	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1

South Bridge Strap Pin (3/3)

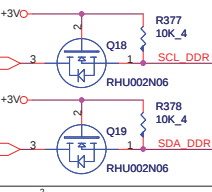
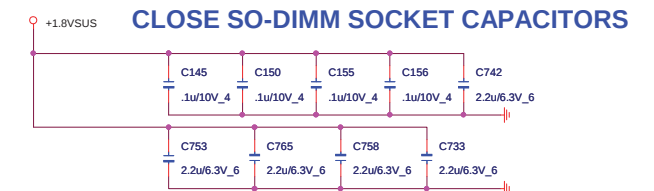
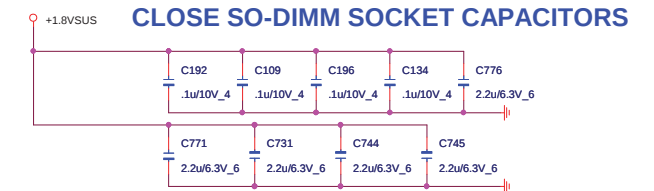
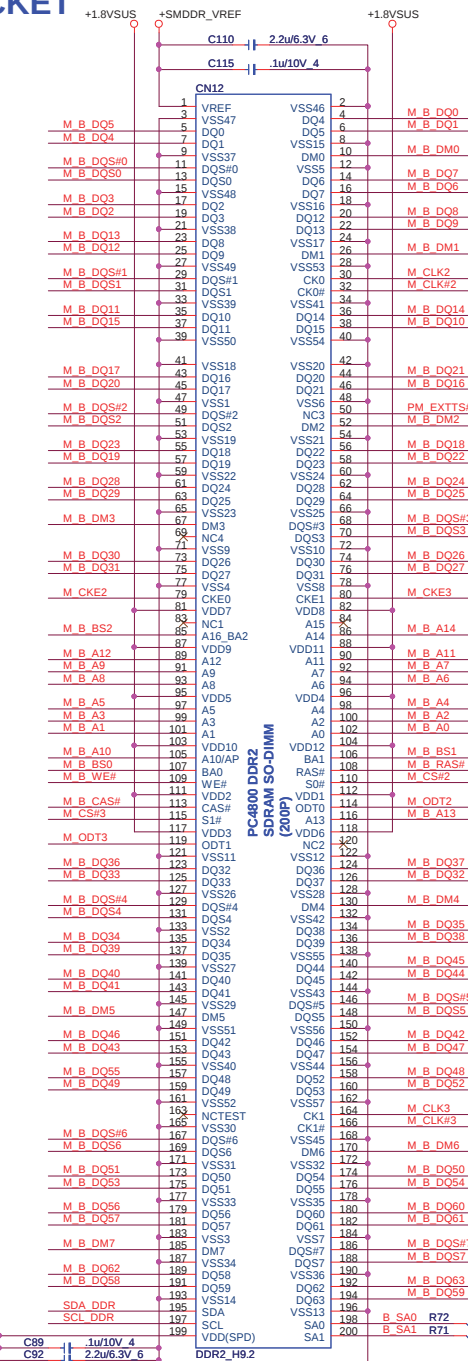
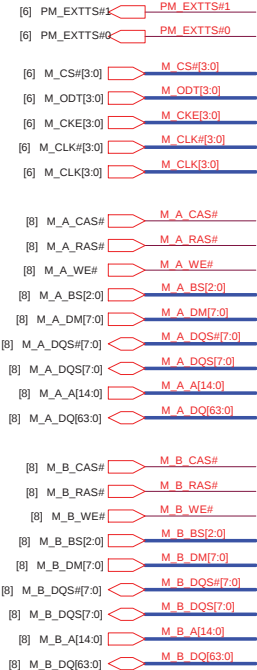
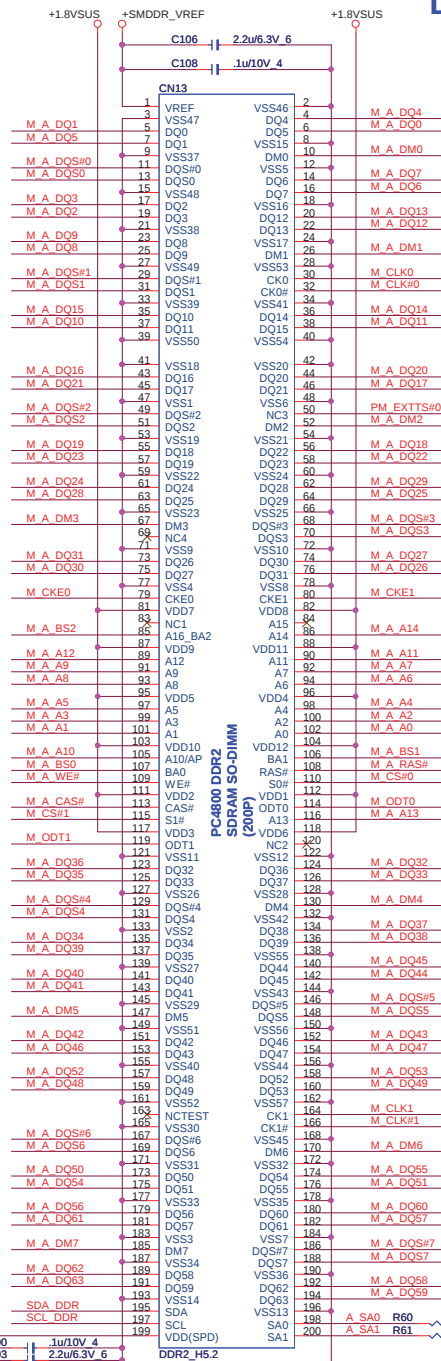
Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	

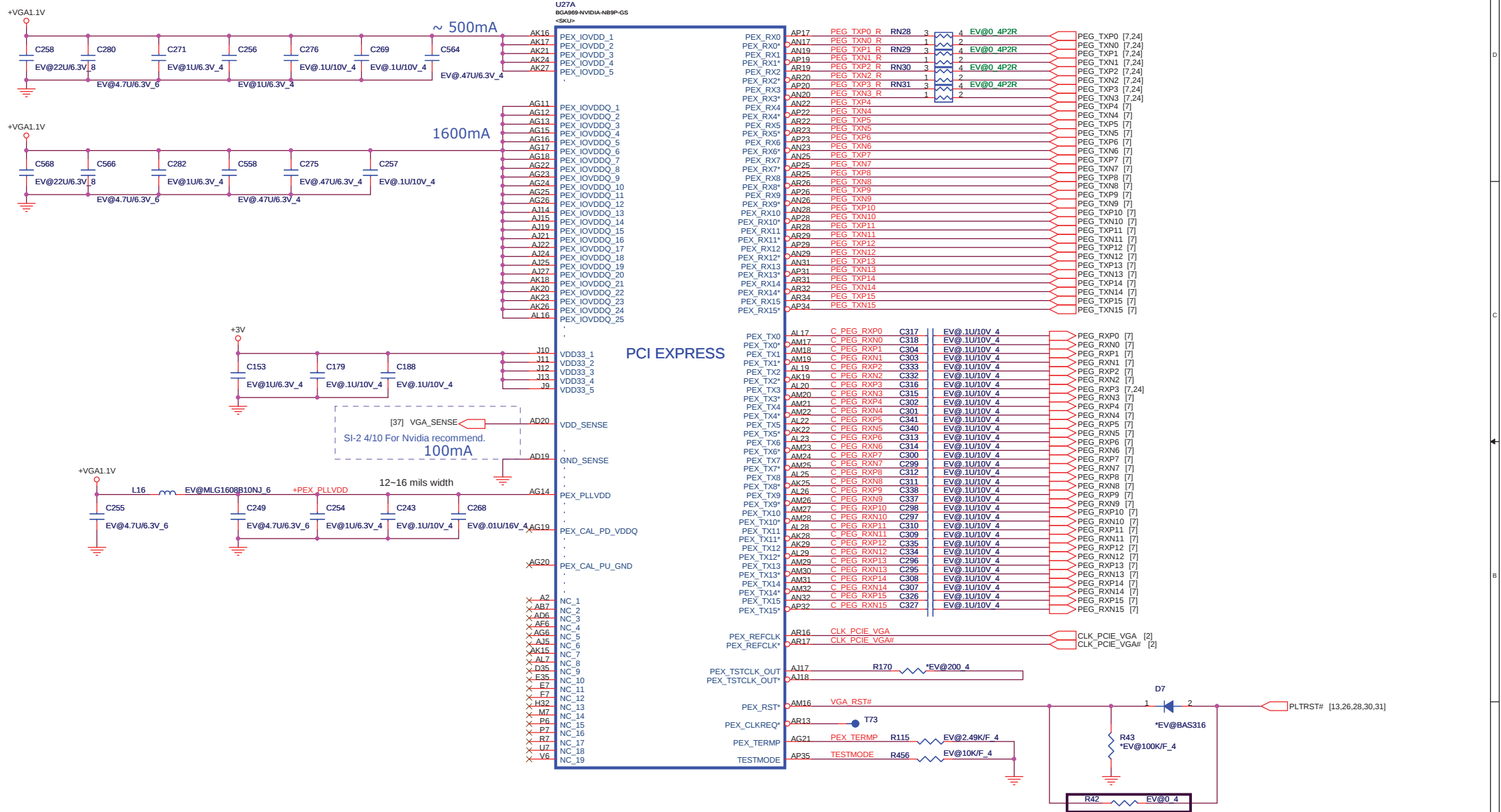
CLK Enable

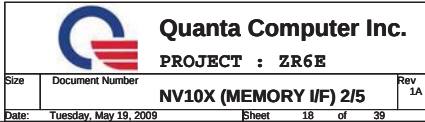


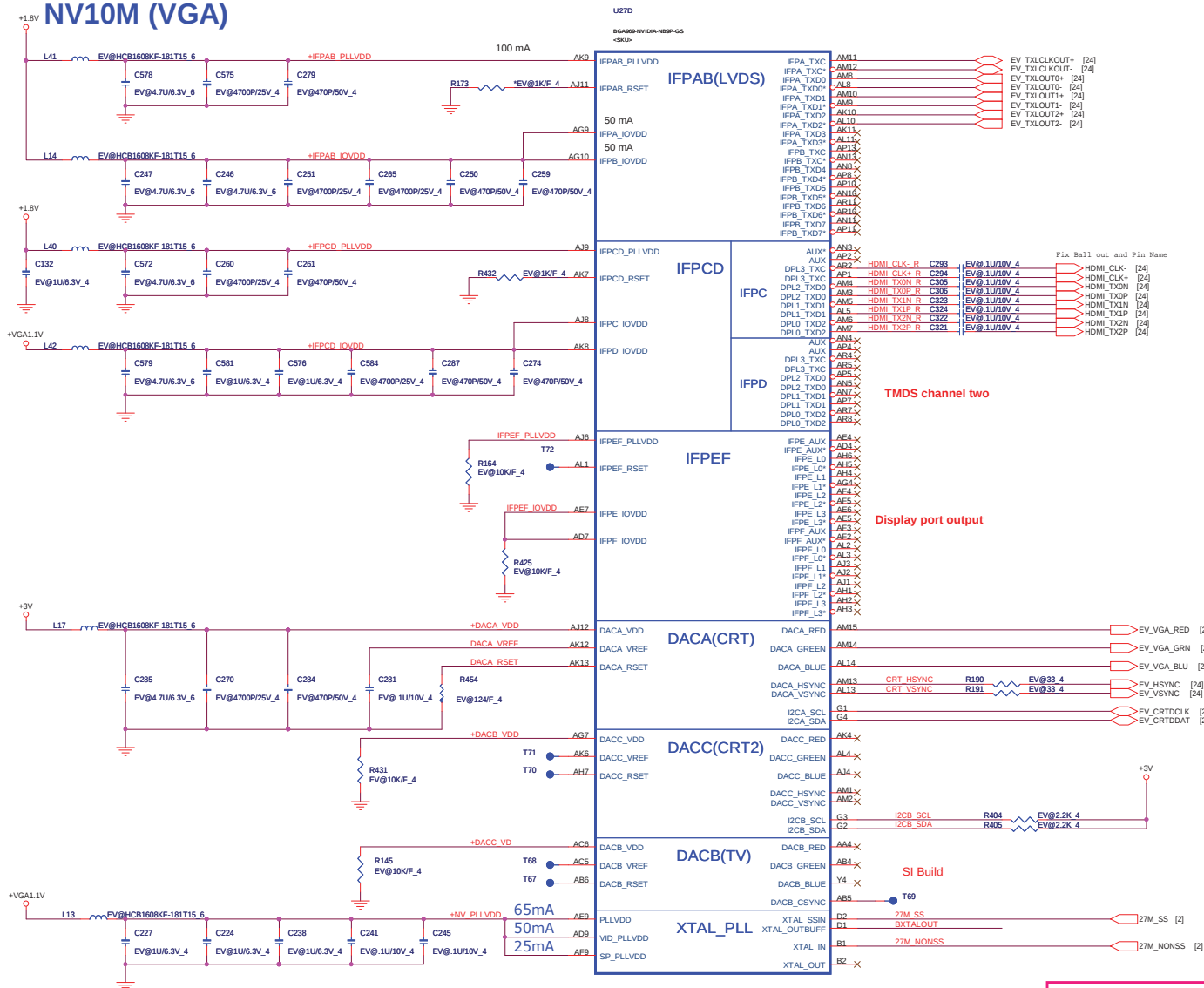


DDR2 SO-DIMM SOCKET







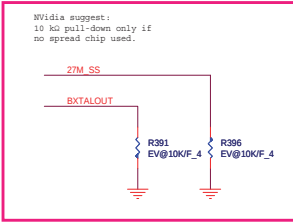
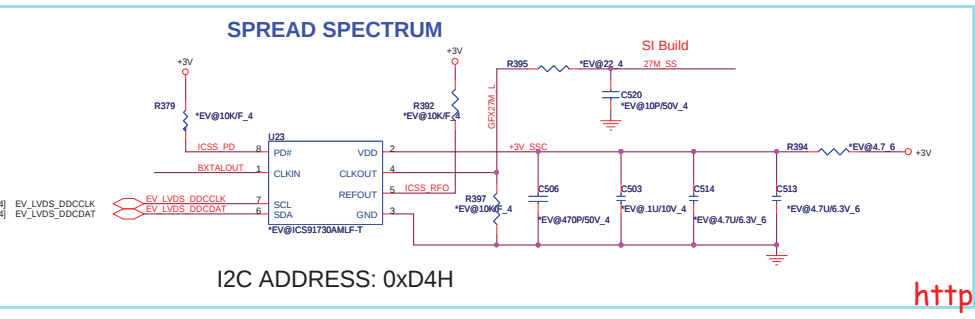


TMDs channel two

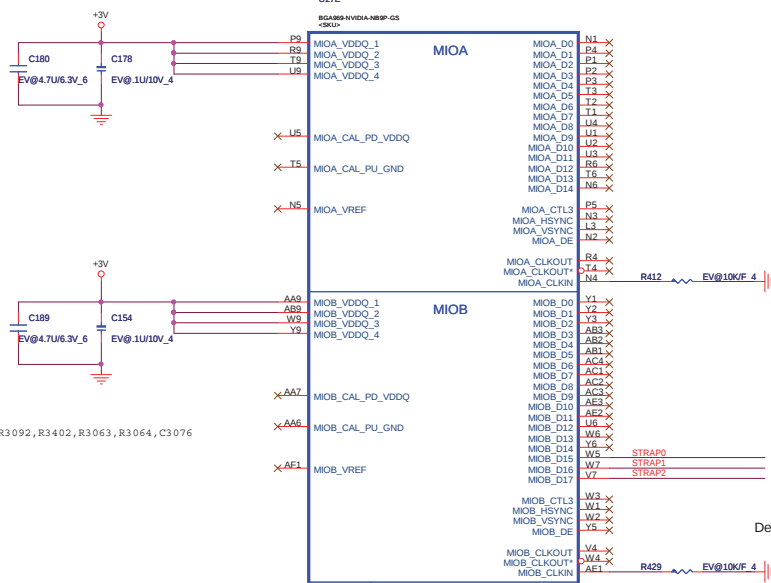
Display port output



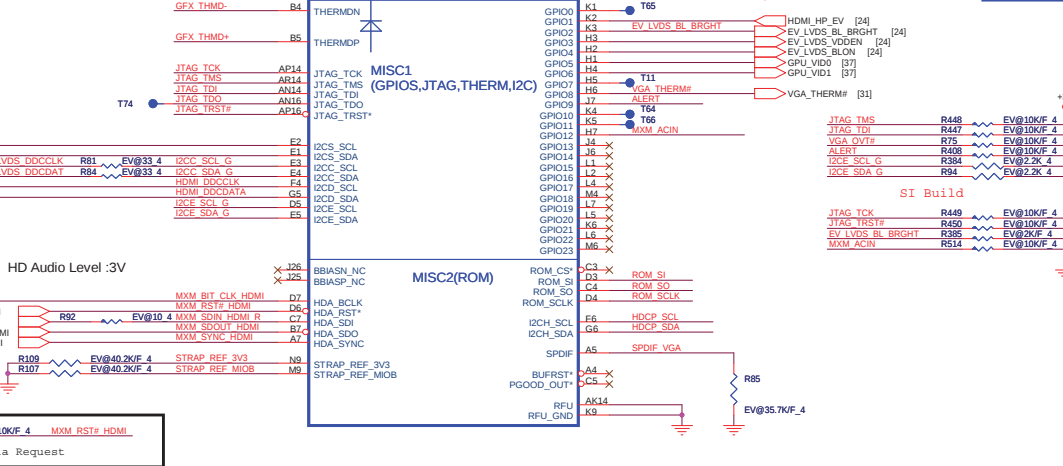
Close to GPU



NV10M (VGA)



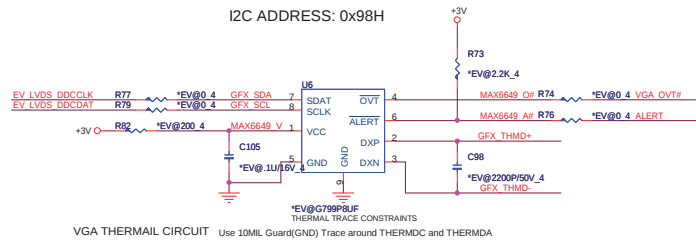
Nvidia Propose Remove C3134,C3681,R3092,R3402,R3063,R3064,C3076



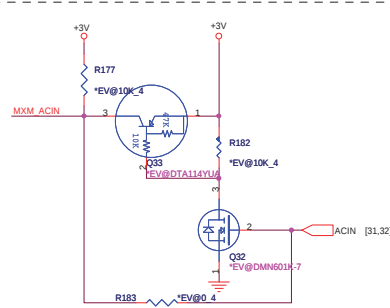
HD Audio Level :3V

Nvidia Request

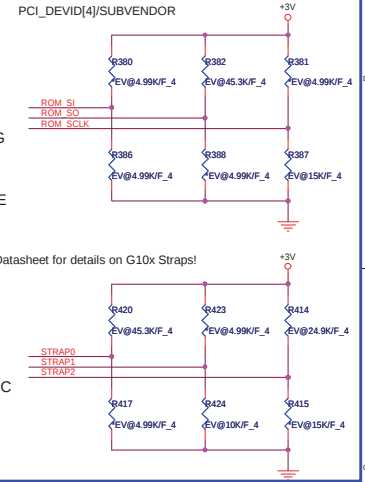
I2C ADDRESS: 0x98H



VGA THERMAIL CIRCUIT Use 10MIL Guard(GND) Trace around THERMOC and THERMDA

<http://hobi-elektronika.net>N10P-GE1 (G96) Straps
N10M-GE1 (G98) Straps
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVD0 VID0
6	OUT	N/A	NVVD1 VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL



SEE Datasheet for details on G10x Straps!

PCI_DEVID: STRAP2

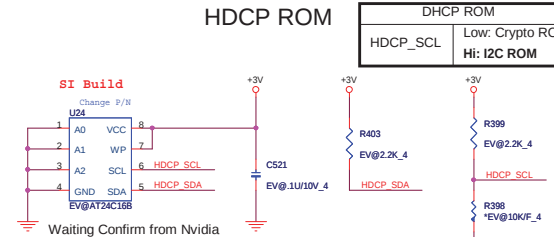
Strap	Value	Default
NB9M-GE	0x06E 8	1000
NB9M-GS	0x06E 9	1001
NB9P-GE2	0x064 8	1000
NB9P-GS	0x064 9	1001
N10P-GE1	0x065 2	0010
N10M-GE1	0x06E C	1100 default

Logical Strap Bit Mapping

R414	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

R386	Config	Definitions	Die
CS25102FB02 5K	64Mx16 DDR2	Hynix	E
CS31002FB26 10K	64Mx16 DDR2	Samsung	Q
CS32002FB29 20K	64Mx16 DDR2	Samsung	E

HDCP ROM

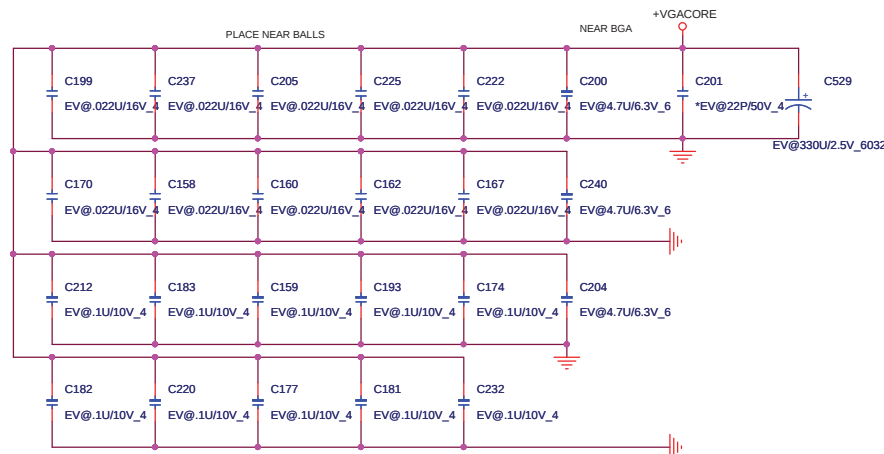


Waiting Confirm from Nvidia

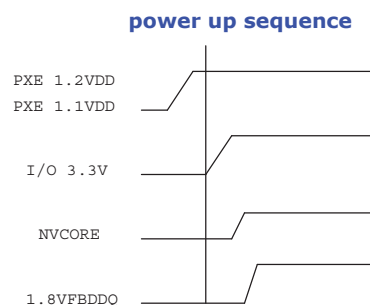
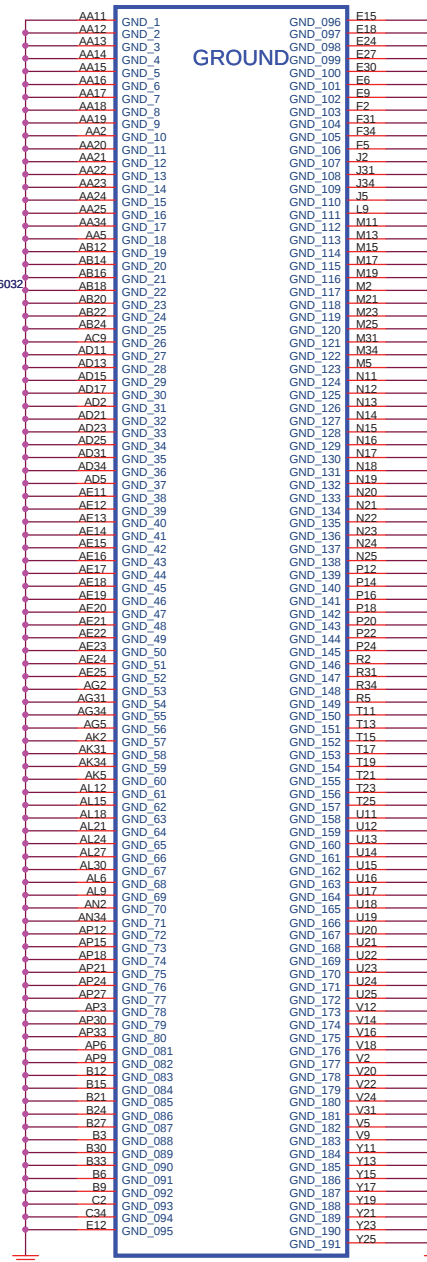
U27G

BGA969-NVIDIA-NB9P-GS

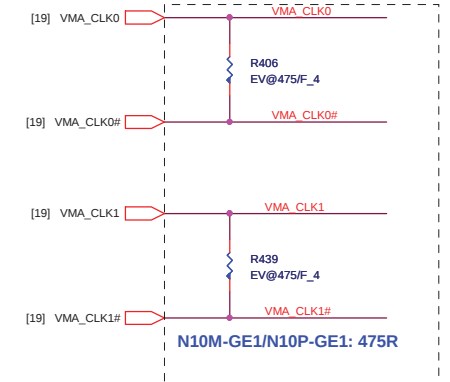
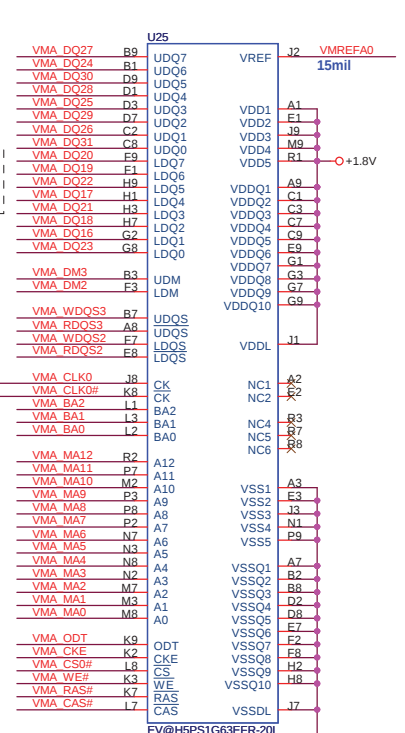
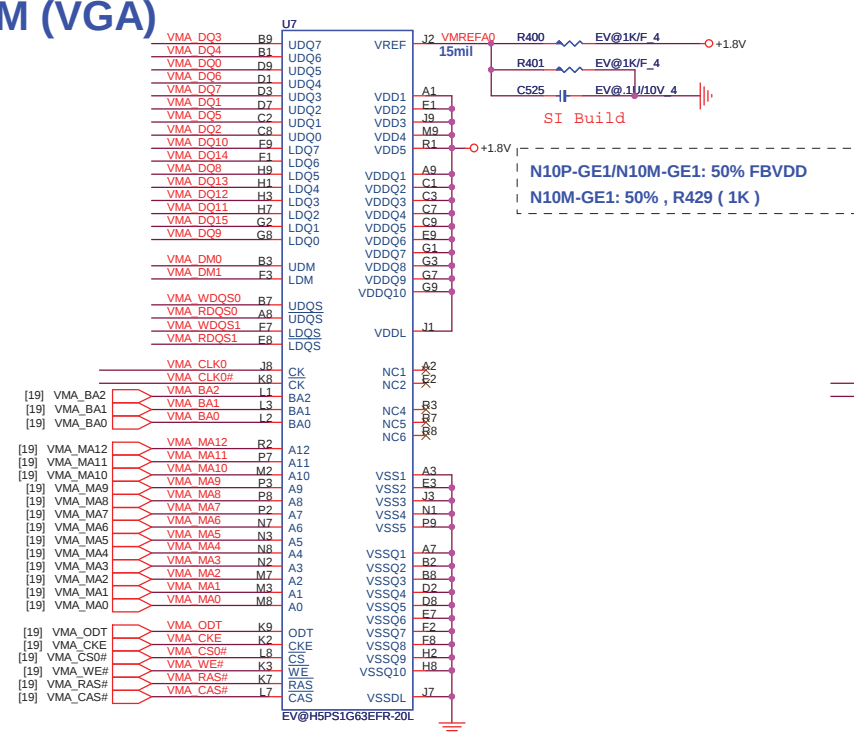
<SKU>



GROUND

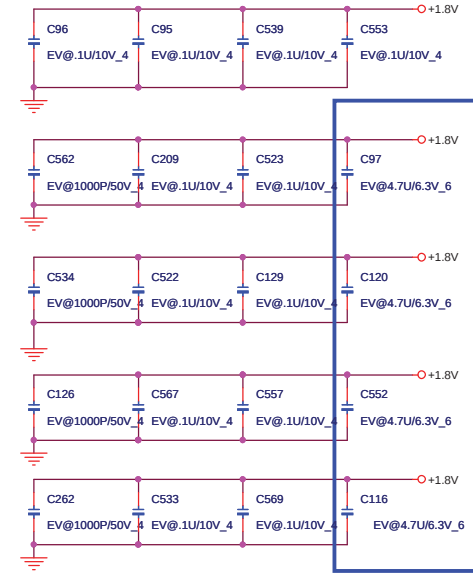


NV10M (VGA)

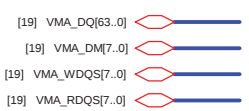
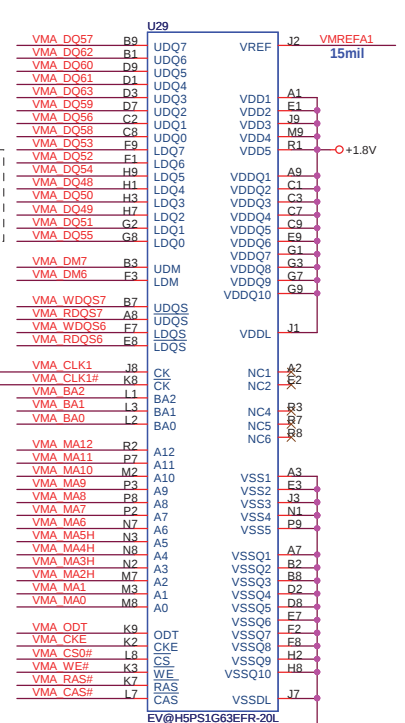
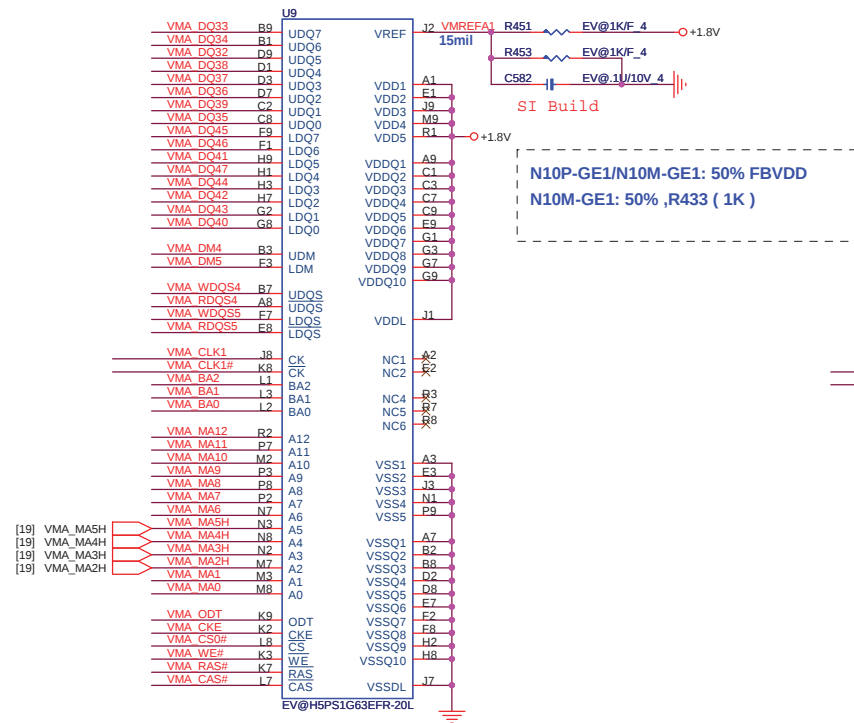


CS14752FB11 RES CHIP 475 1/16W +-1%(0402)

(By pass capacitor)



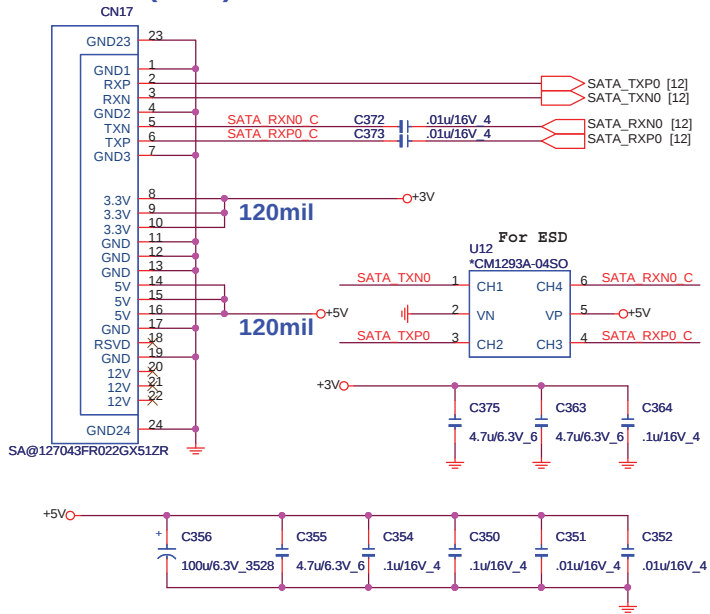
For DB:
 N10P/N10M : AKD5LG-T510(Samsung,64M*16)
 AKD5LG-TW02(Hynix,64M*16)



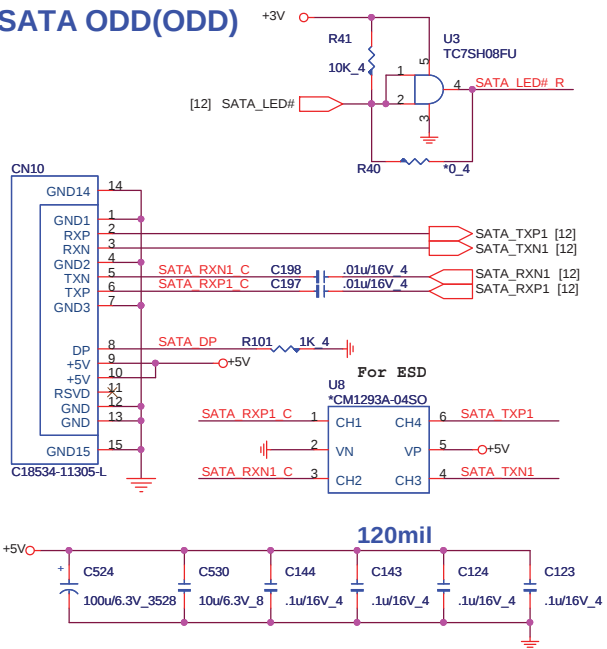
Quanta Computer Inc.
PROJECT : ZR6E

Size	Document Number	Rev
	NV10X VRAM-1(GDDR2 BGA84)	1A
Date:	Tuesday, May 19, 2009	Sheet 22 of 39

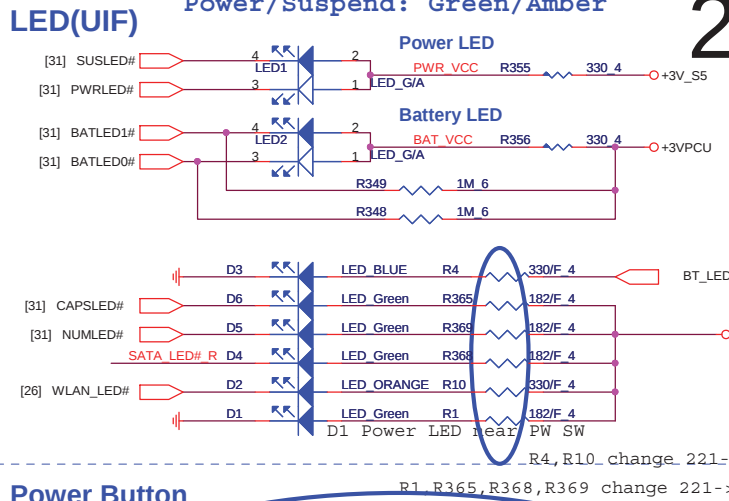
SATA HDD(HDD)



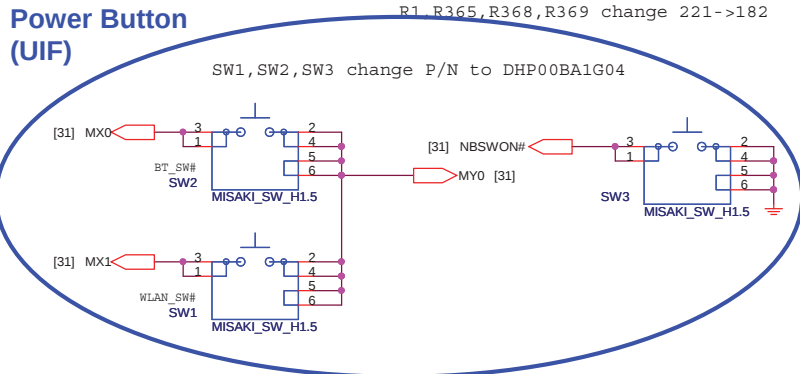
SATA ODD(ODD)



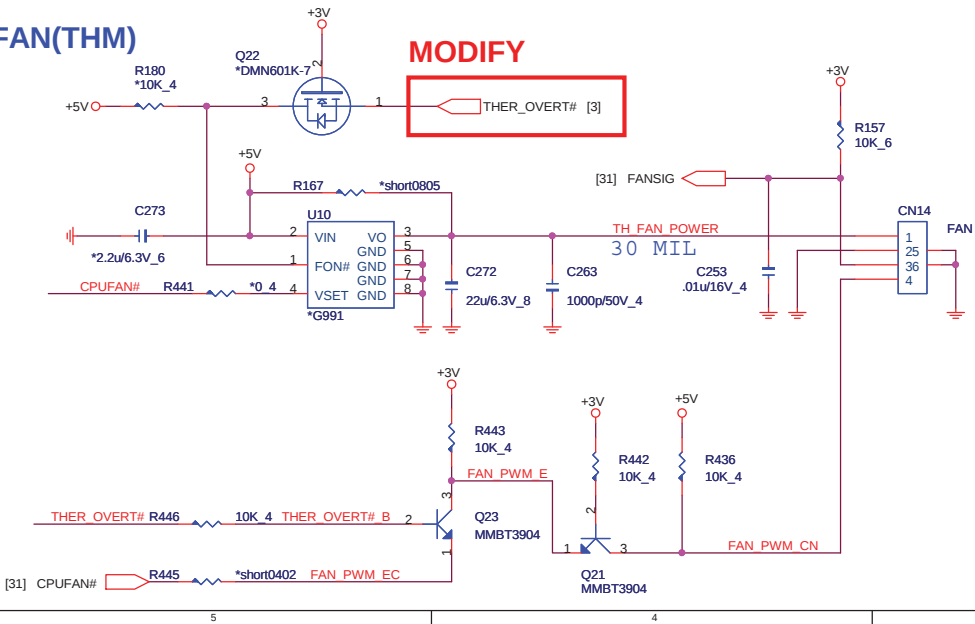
LED(UIF)



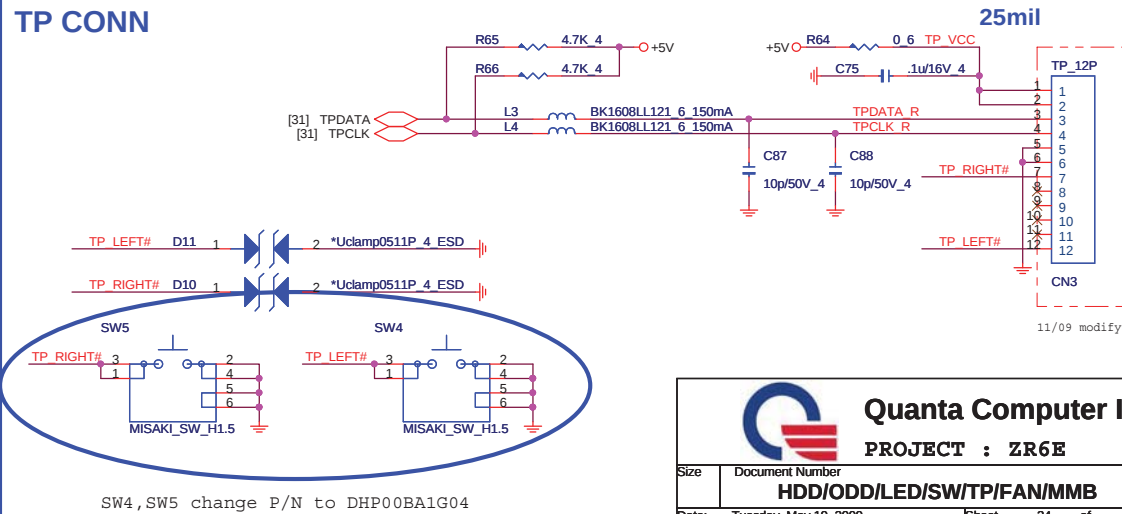
Power Button (UIF)



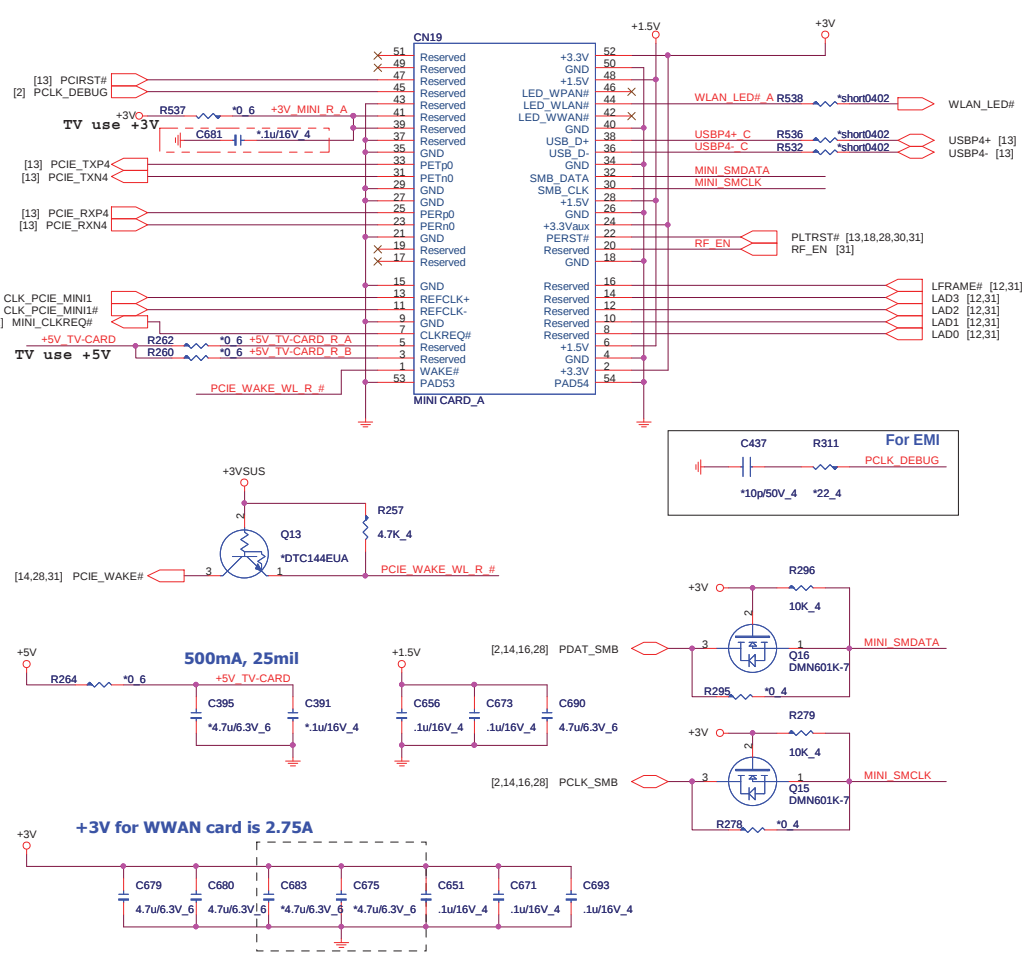
FAN(THM)



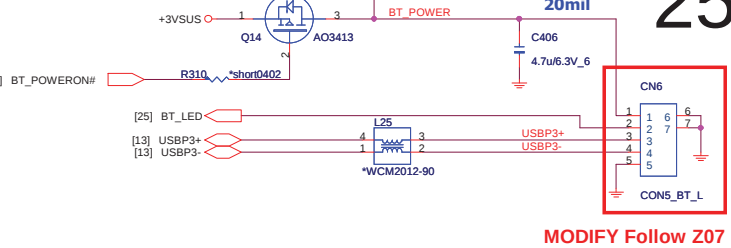
TP CONN



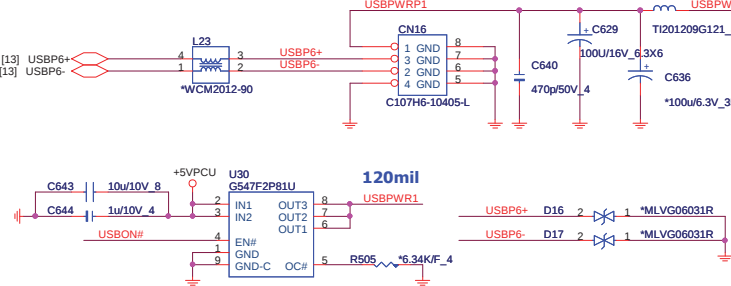
MINI-CARD(MPC)



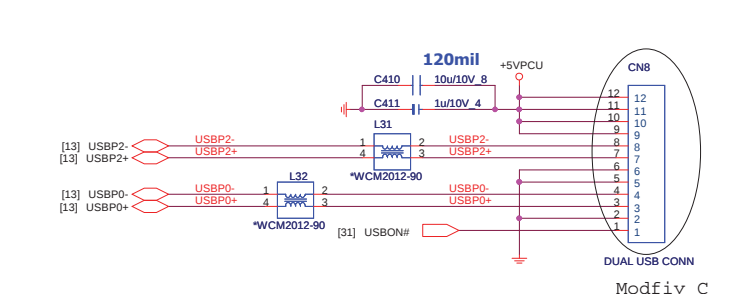
Bluetooth(BTM)



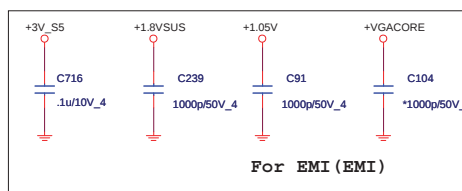
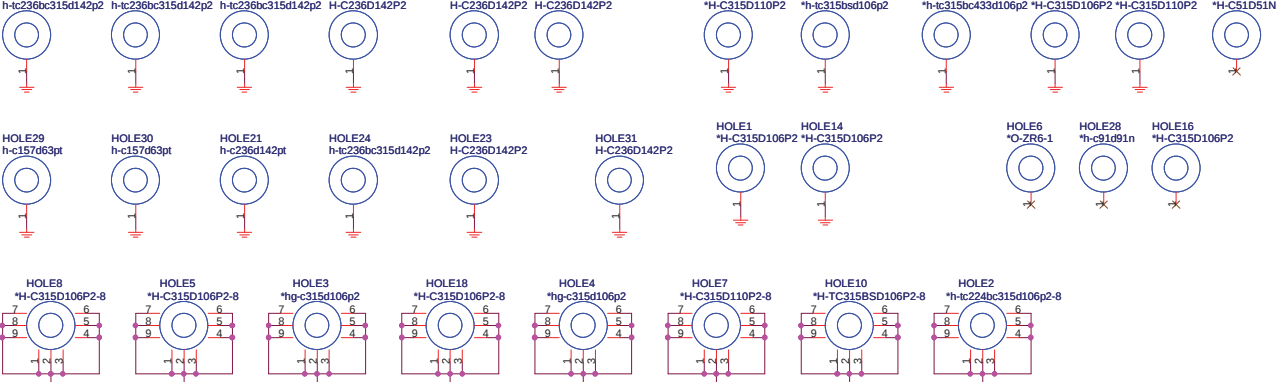
INT. USB(USB)



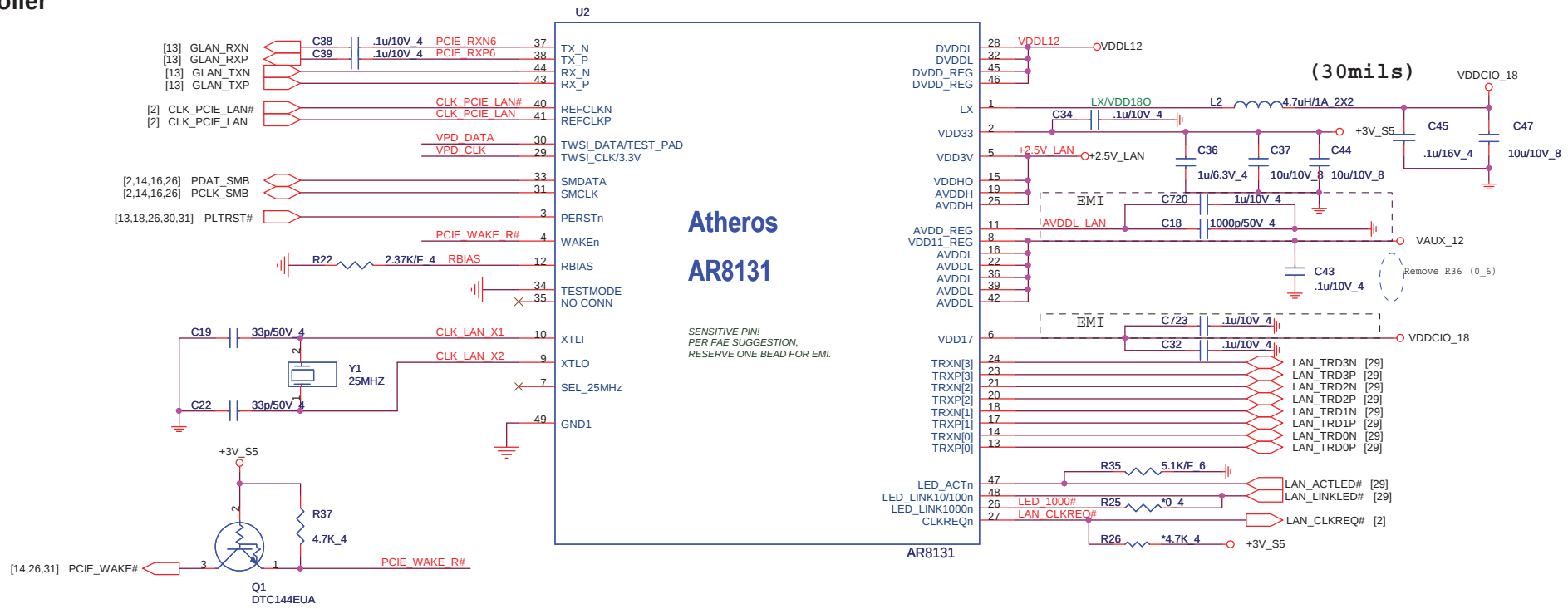
EXT. USB(USB)



(OTH)



LAN Controller



Decoupling CAP

PLACE NEAR IC SIDE

EEPROM

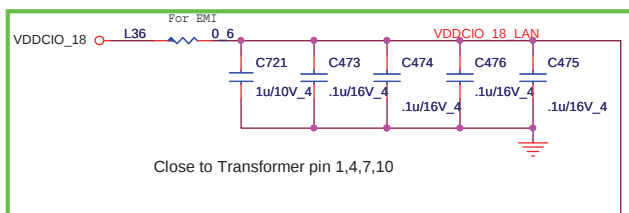


Quanta Computer Inc.

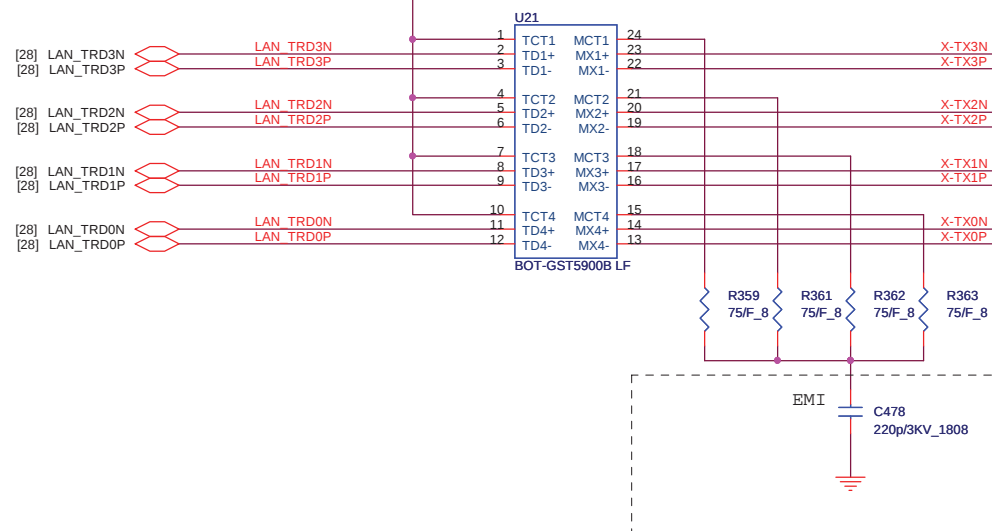
PROJECT : ZR6E

AR8131 GLAN

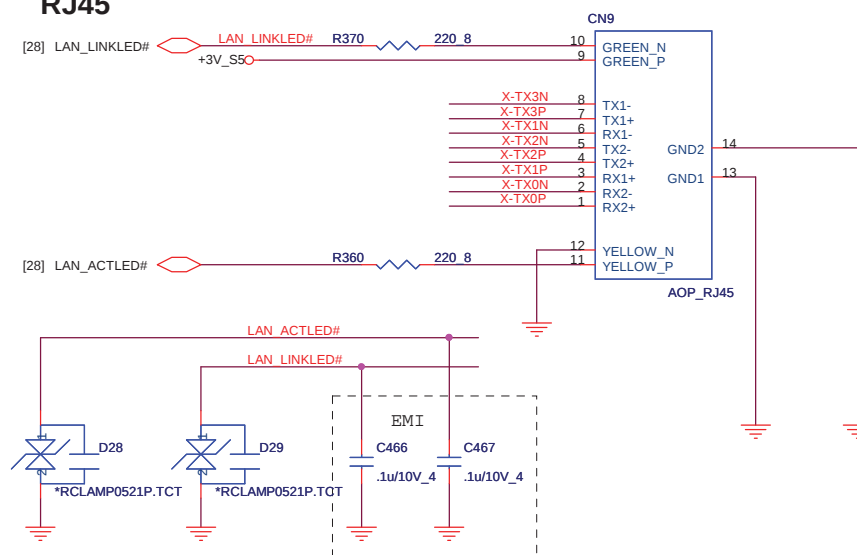
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Date:	Tuesday, May 19, 2009	Sheet 27 of 39



TRANSFORMER



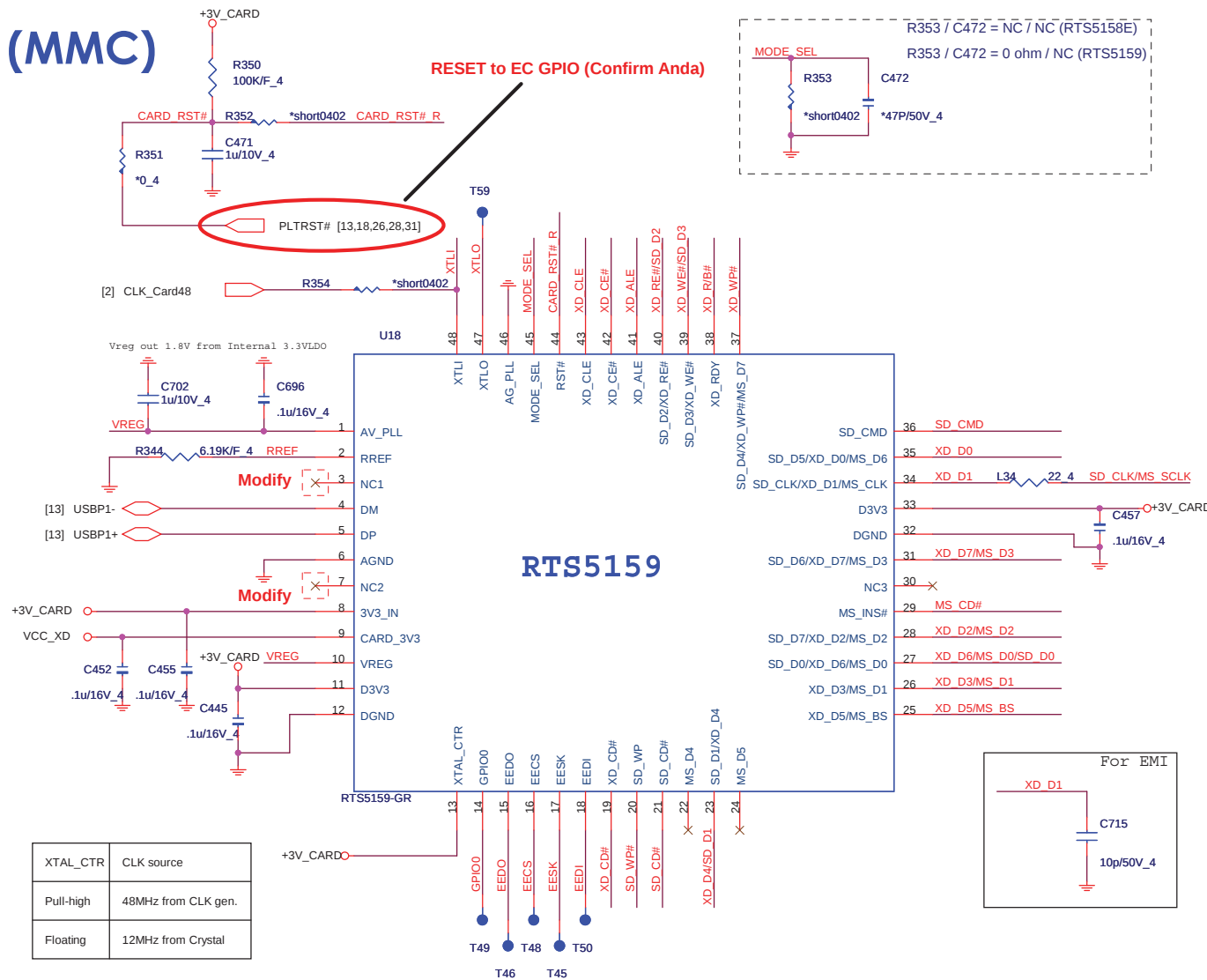
RJ45



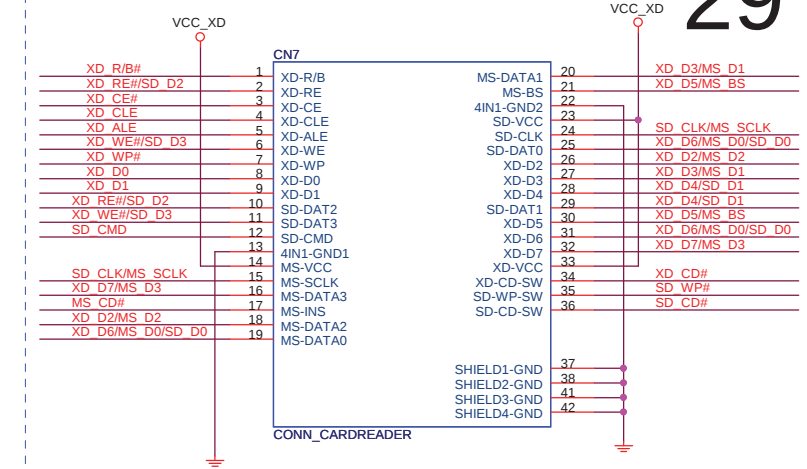
Quanta Computer Inc.
PROJECT : ZR6E

Size	Document Number	Rev
	LAN Transformer and RJ45/BT	1A
Date:	Tuesday, May 19, 2009	Sheet 28 of 39

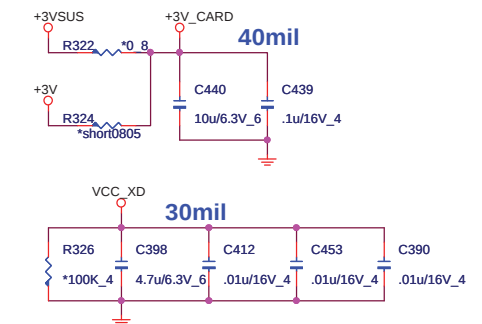
(MMC)



4 IN 1 CARD READER



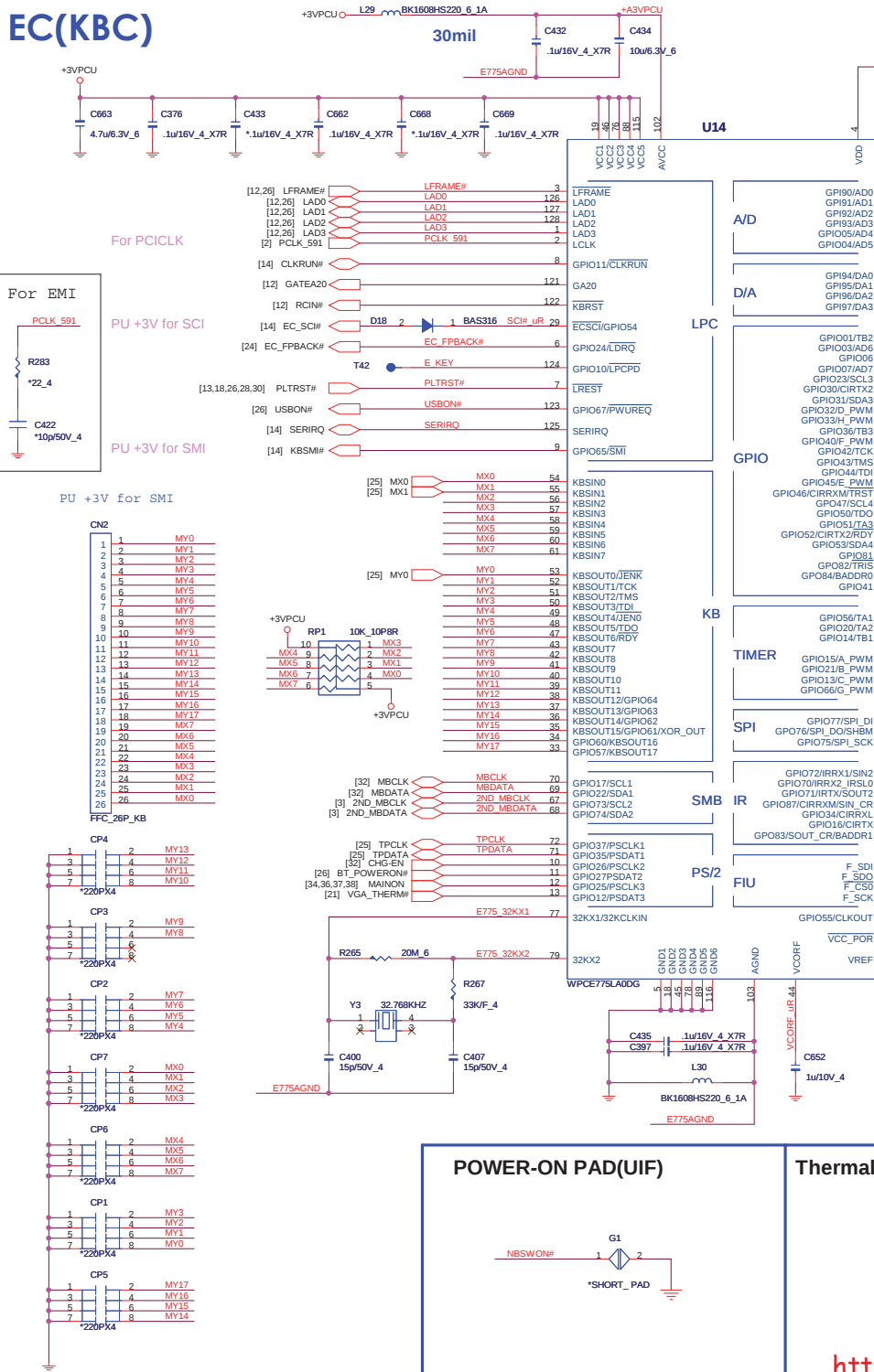
CARDREADER POWER



Quanta Computer Inc.

PROJECT : ZR6E

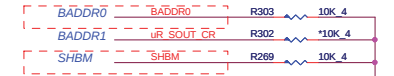
Size	Document Number	Rev
	CARD READER RTS5159	1A
Date:	Tuesday, May 19, 2009	Sheet 29 of 39



I/O ADDRESS SETTING

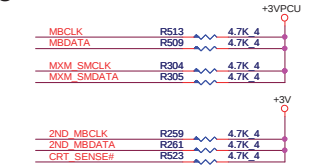
I/O Address		
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

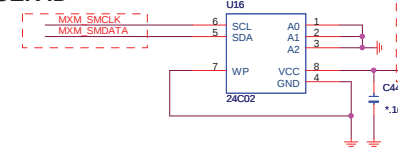


1/13 Confirm by vendor mail :
 Disabled ('1') if using FW device on LPC.
 Enabled ('0') if using SPI flash for both system BIOS and EC firmware

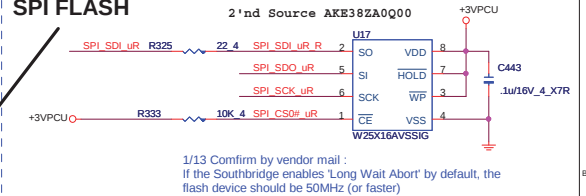
SM BUS PU



ACER ID

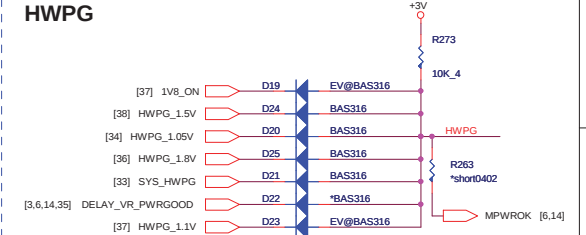


SPI FLASH



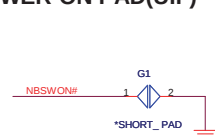
1/13 Confirm by vendor mail :
 If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

HWPG

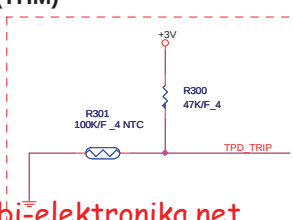


1'st AKE38ZP0N01 : Winbond W25X16AVSSIG
 2'nd AKE37FP0Z13 : MXIC MX25L1605AM2C-15G
 3'rd AKE38ZA0Q00 : EON EN25F16-100HIP
 4'rd AKE38ZN0800 : AMIC A25L016

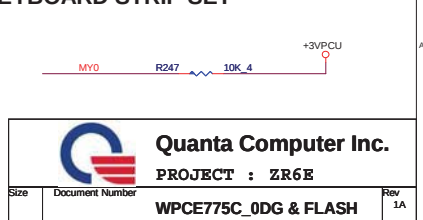
POWER-PAD (UIF)

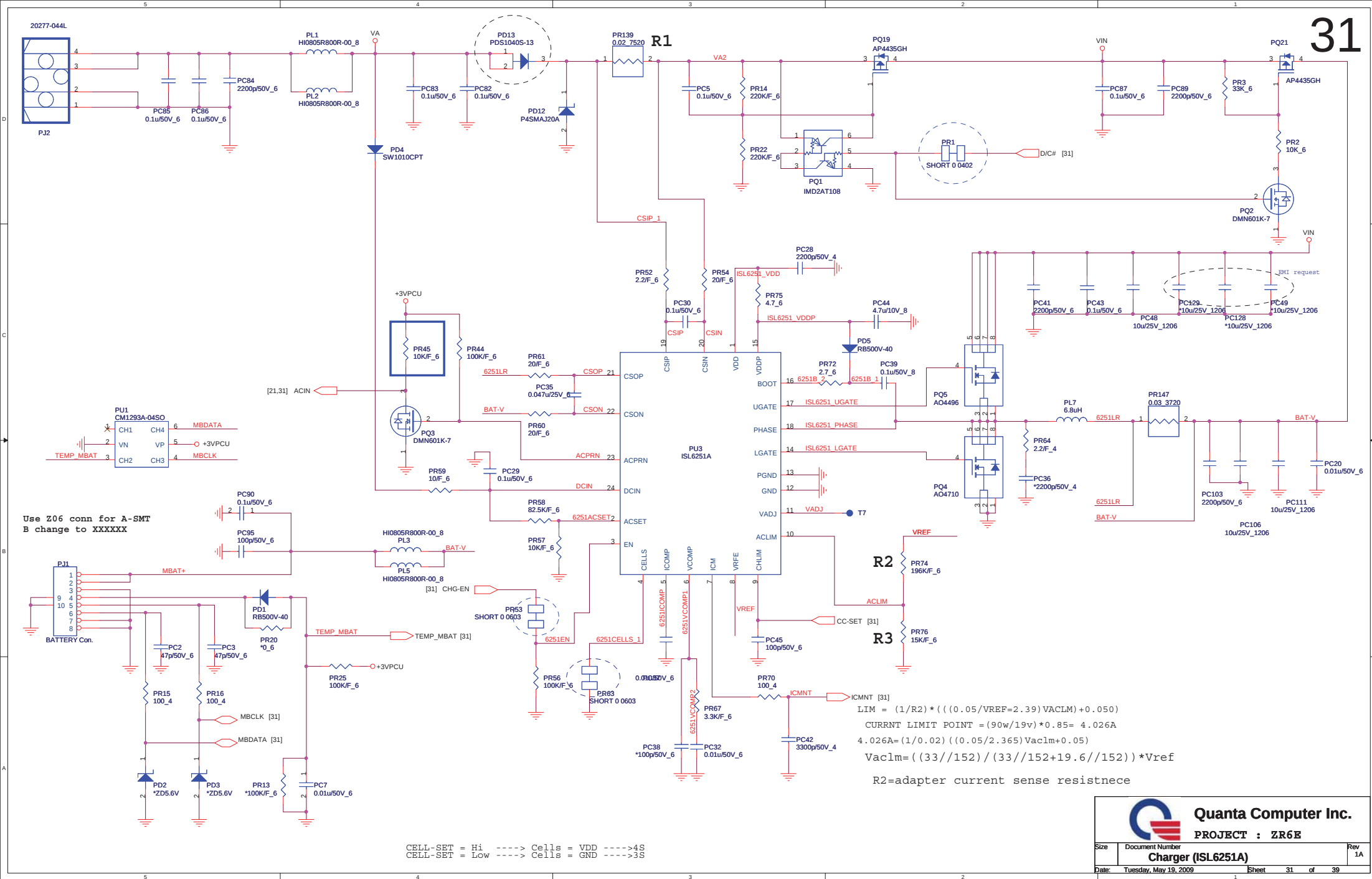


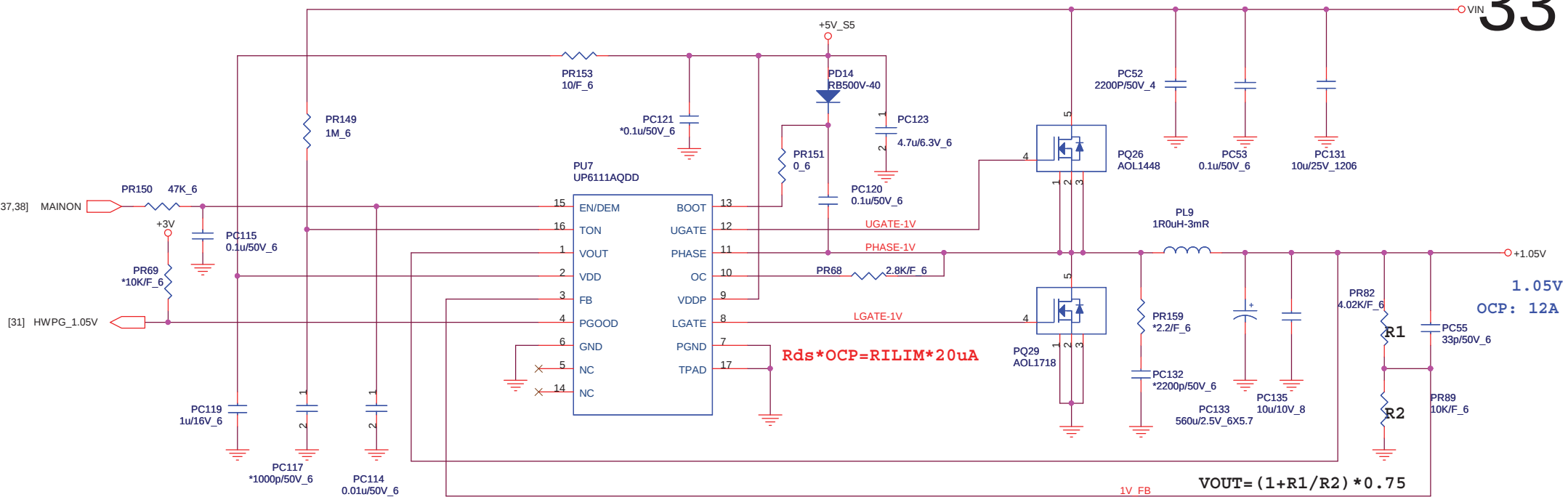
Thermal Sensor (THM)



INTERNAL KEYBOARD STRIP SET







$$TON = 3.85p * R_{TON} * V_{out} / (V_{in} - 0.5)$$

$$Frequency = V_{out} / (V_{in} * TON)$$

$$TON = 3.85p * 1M * 1 / (V_{in} - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

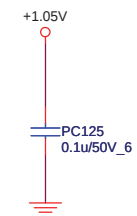
$$AOL1412 \quad R_{ds(on)} = 4.6m\Omega$$

$$OCP = 16 - 0.8A$$

$$L(\text{ripple current}) = (19 - 1.05) * 1.05 / (1\mu * 272k * 19) \sim 3.646A$$

$$4.6m * 12 = R_{ILIM} * 20\mu A$$

$$R_{ILIM} = 2.76K \text{ --- } 2.8K$$

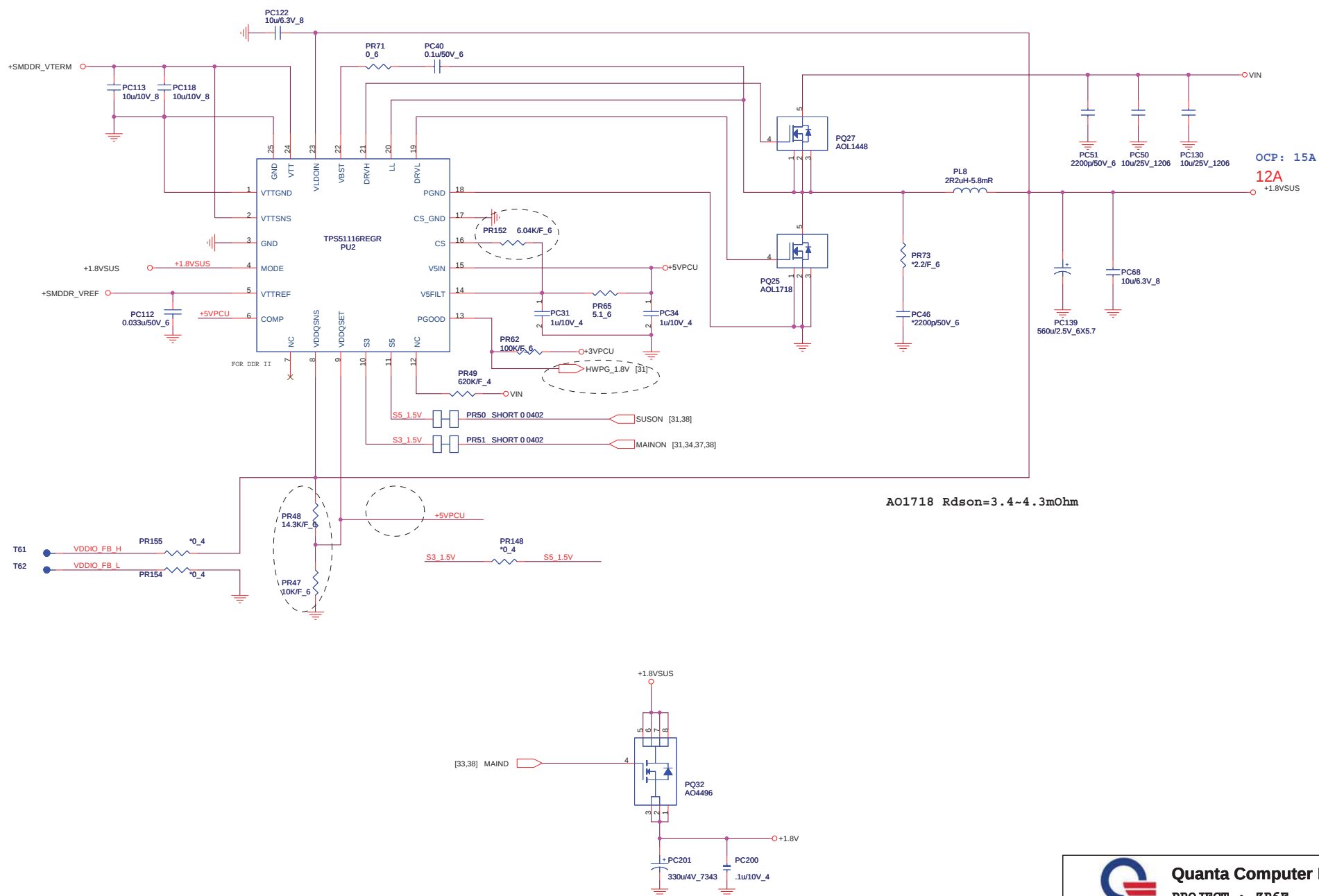


Quanta Computer Inc.

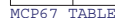
PROJECT : ZR6E

Size	Document Number	Rev
	VCCP 1.05V(UP6111A)	1A

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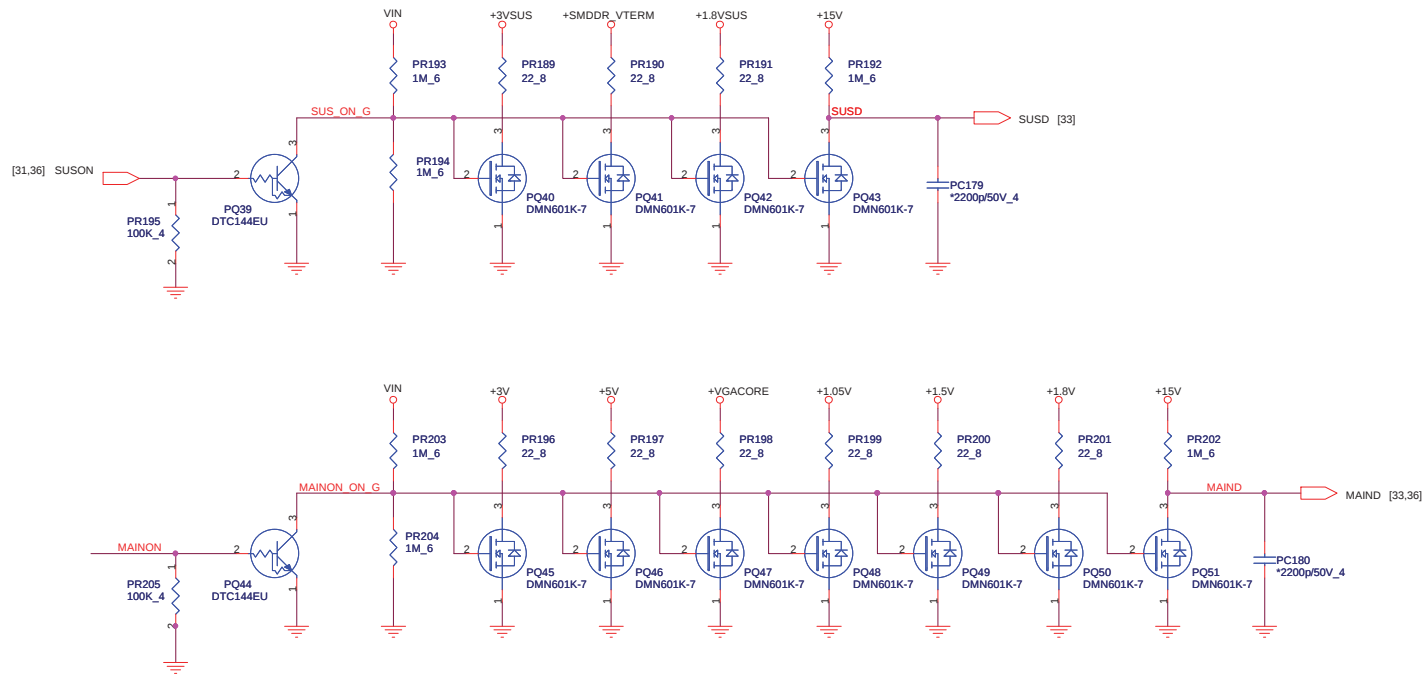
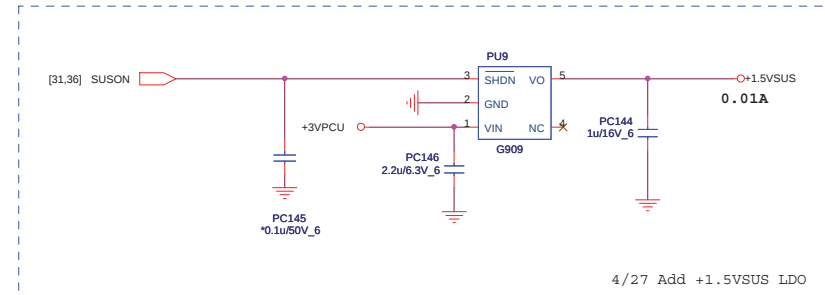
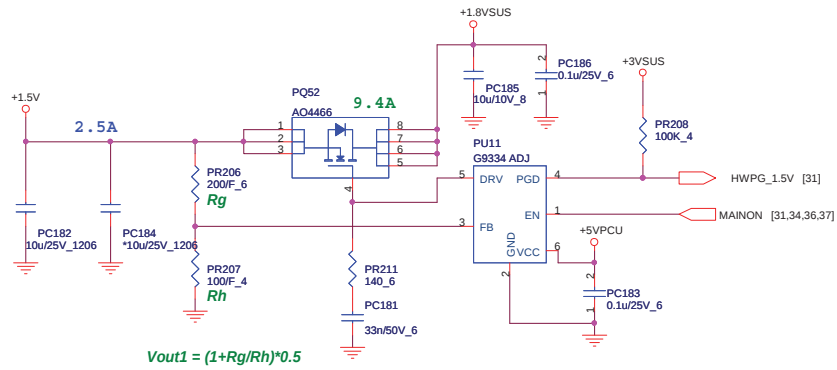
<http://hobi-elektronika.net>



VID[1:0]		
VID1	VID0	Set
0	0	1.2V
0	1	1.1V
1	0	1.0V
1	1	0.9V

INPUTS		OUTPUTS			VOUT1
G1	G0	OD1	OD2	OD3	
0	0	$2.75 * R2 / (R1 + R2) = 2.75 * 121 / (121 + 158) =$			1.192 (G0=0, G1=0)
0	1	$2.75 * (R2 R3) / [(R2 R3) + R1] =$			1.092 (G0=1, G1=0)
1	0	$2.75 * (R2 R4) / [(R2 R4) + R1] =$			0.99 (G0=0, G1=1)
1	1	$2.75 * (R2 R3 R4) / [(R2 R3 R4) + R1] =$			0.91 (G0=1, G1=1)

<http://hobi-elektronika.net>





For EC control thermal protection (output 3.3V)

[illegible]