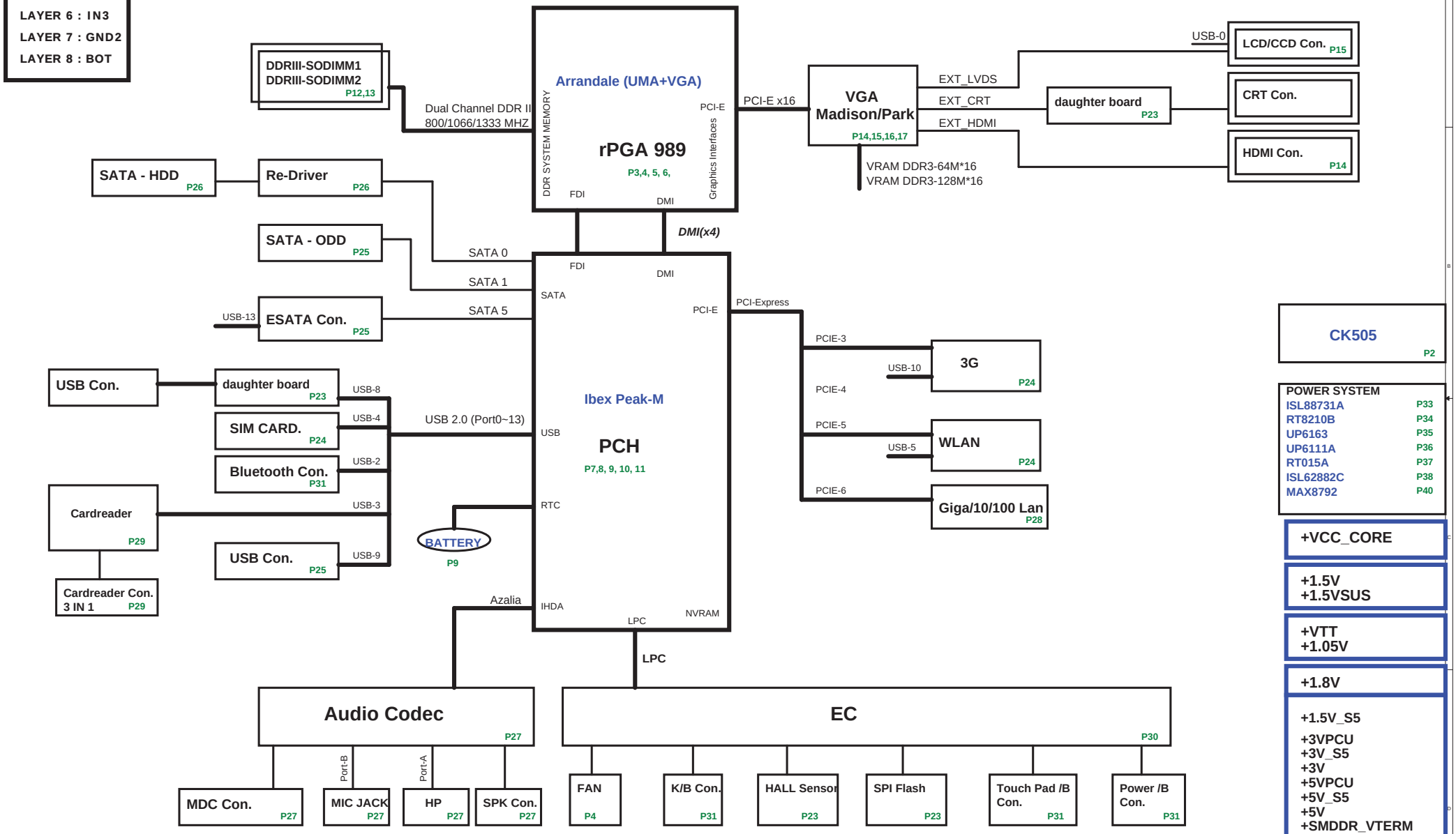
TE2D Block Diagram

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND1
- LAYER 3 : IN1
- LAYER 4 : VCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : GND2
- LAYER 8 : BOT



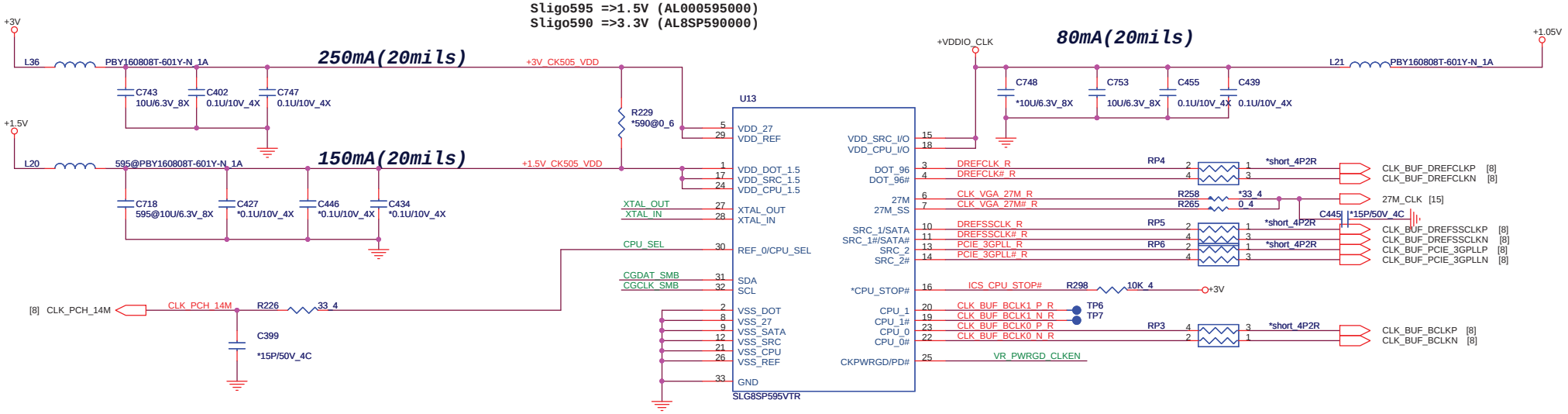
Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	Block Diagram	2A

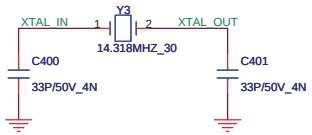
Date: Thursday, February 25, 2010 Sheet 1 of 43

CLOCK Gen [CLK]

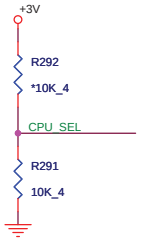
Pin1/17/24
Sligo595 =>1.5V (AL000595000)
Sligo590 =>3.3V (AL8SP590000)



CLK CRYSTAL

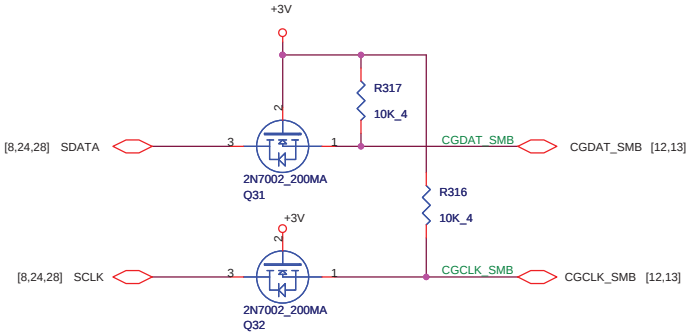


CLK CPU_SEL



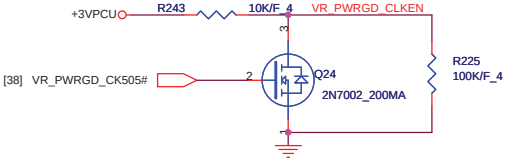
	0	1
CPU_SEL	CPU =133MHz (default)	CPU=100MHz

CLK I2C



CLK POWERGOOD

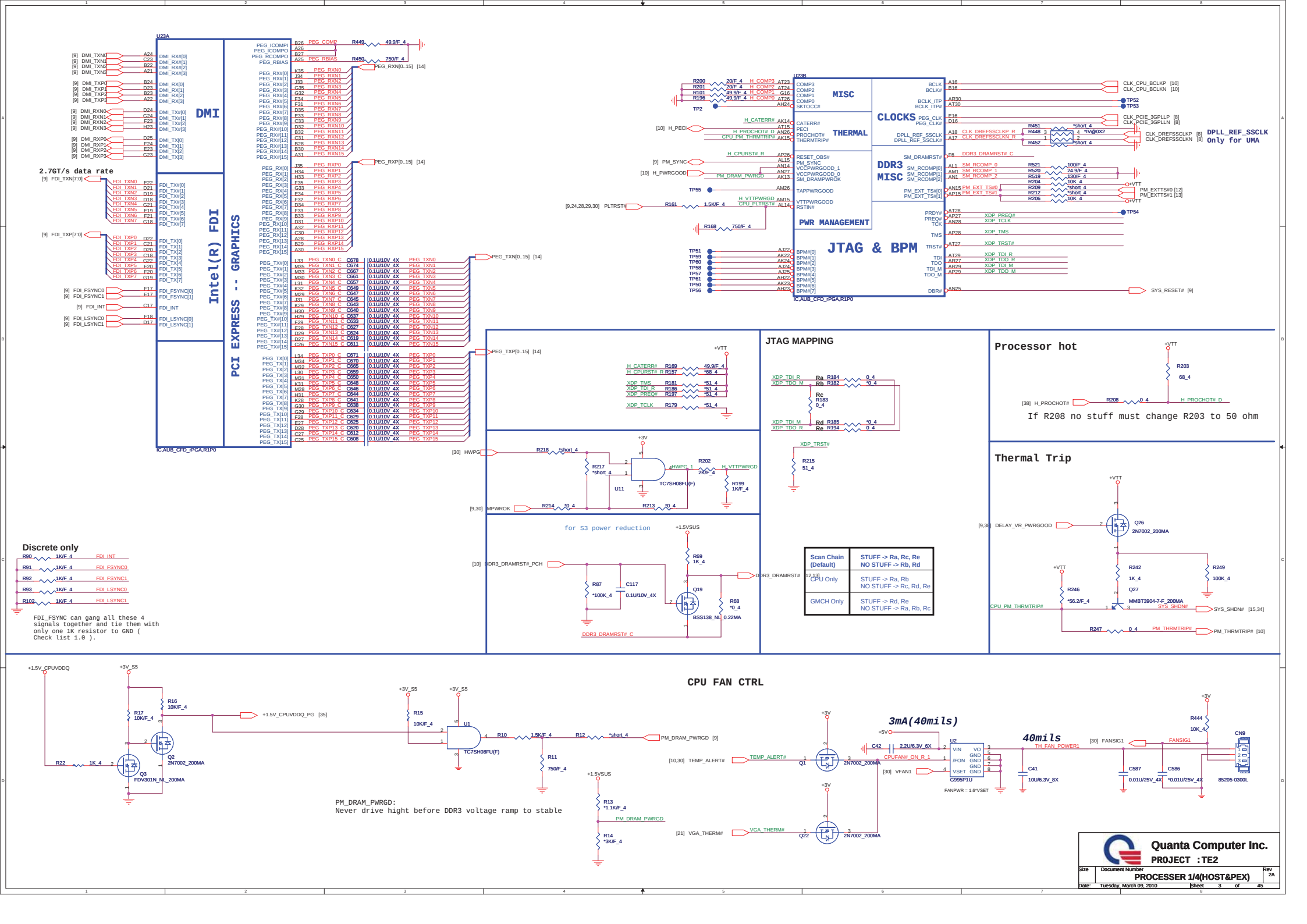
Change to +3VPCU
(follow CRB)



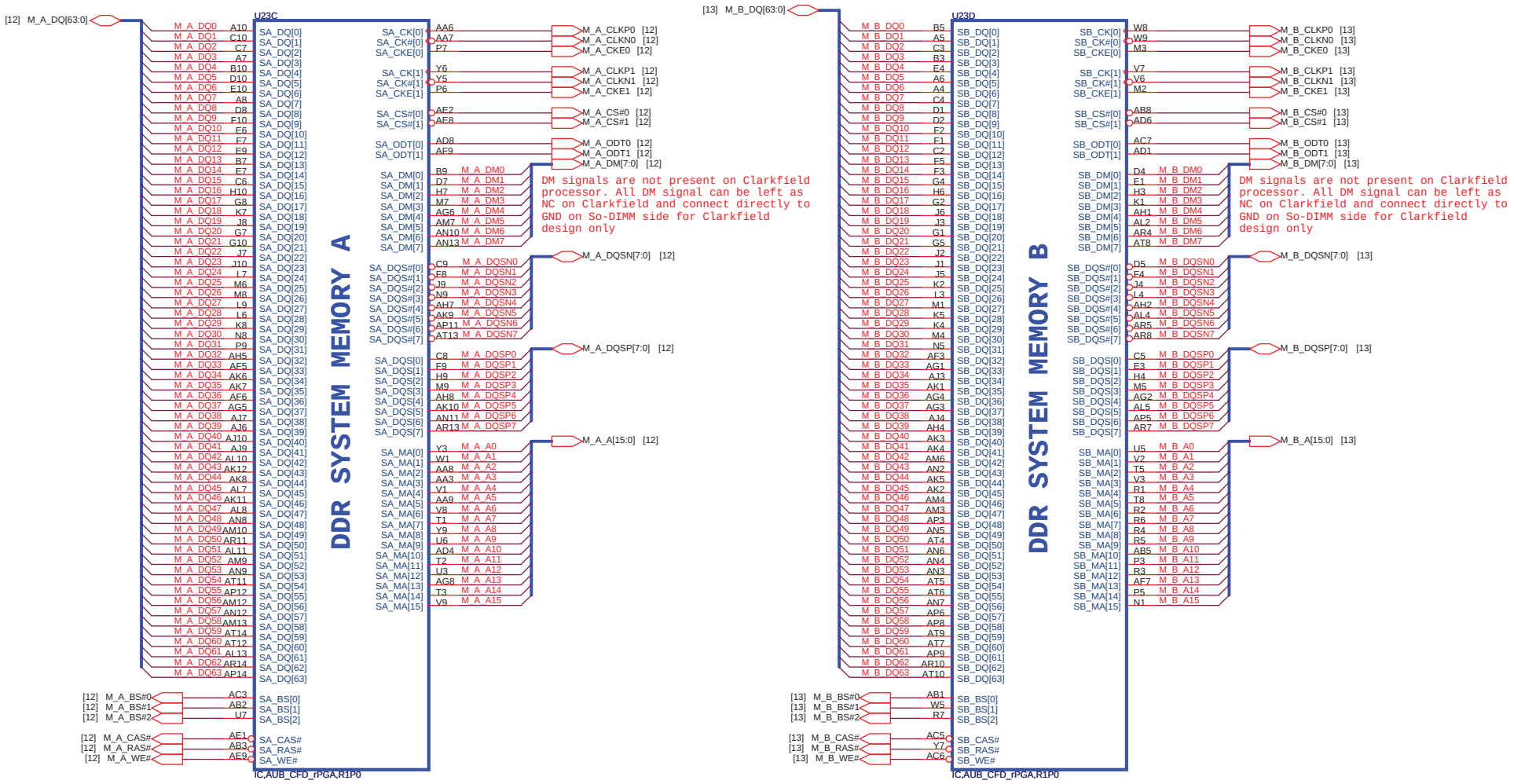
Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	CLOCK GENERATOR	2A

Date: Friday, March 19, 2010 Sheet 2 of 45


DMI
Intel(R) FDI
PCI EXPRESS -- GRAPHICS
MISC
THERMAL
CLOCKS
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
DPLL_REF_SSCLK
Only for UMA
2.7GT/s data rate
JTAG MAPPING
Processor hot
If R208 no stuff must change R203 to 50 ohm
Thermal Trip
Discrete only
FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (Check list 1.0).
for S3 power reduction
CPU FAN CTRL
3mA(40mils)
40mils
PM_DRAM_PWRGD:
Never drive hight before DDR3 voltage ramp to stable
Scan Chain (Default)
STUFF -> Ra, Rc, Re
NO STUFF -> Rb, Rd
CPU Only
STUFF -> Ra, Rb
NO STUFF -> Rc, Rd, Re
GMCH Only
STUFF -> Rd, Re
NO STUFF -> Ra, Rb, Rc
Quanta Computer Inc.
PROJECT :TE2
PROCESSER 1/4(HOST&PEX)
Rev 2A
Tuesday, March 09, 2010
Sheet 3 of 45

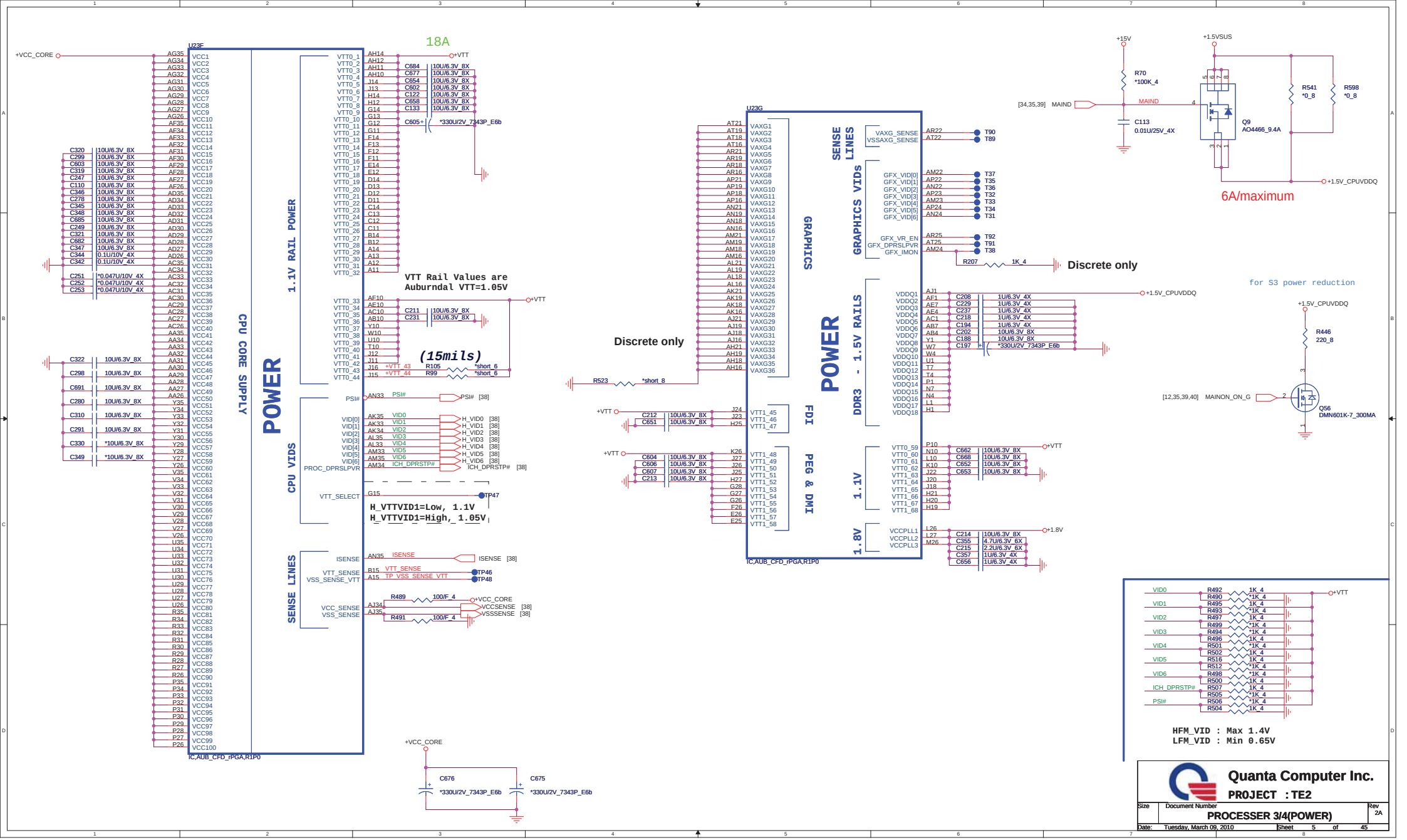
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



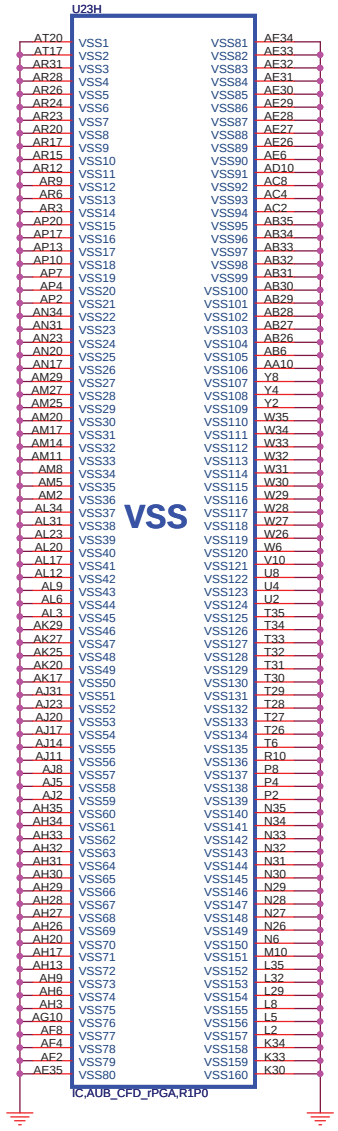
Quanta Computer Inc.

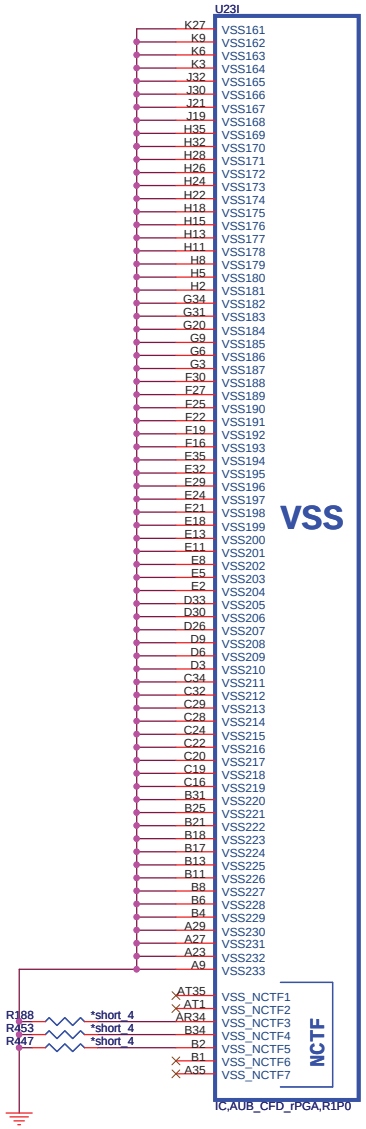
PROJECT : TE2

Size	Document Number	Rev
	PROCESSER 2/4(DDR)	2A
Date: Thursday, February 25, 2010	Sheet 4 of 45	

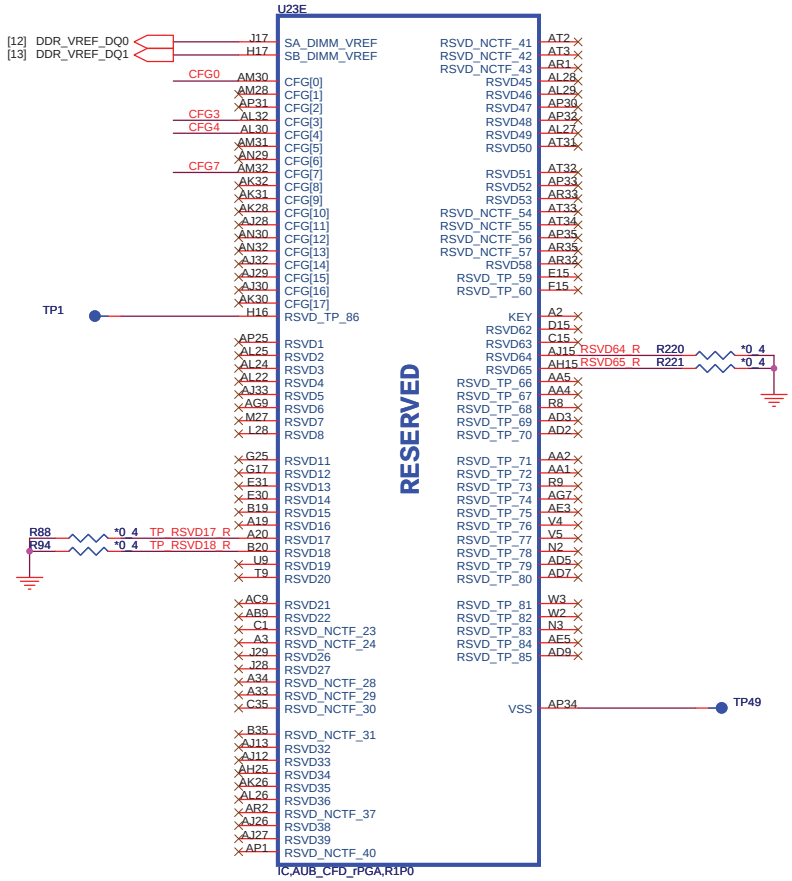

18A
U23F
POWER
CPU CORE SUPPLY
1.1V RAIL POWER
CPU VIDS
SENSE LINES
VTT Rail Values are
Auburndal VTT=1.05V
(15mils)
H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V
IC,AUB_CFD_rPGA,R1P0
U23G
POWER
GRAPHICS
SENSE LINES
GRAPHICS VIDs
DDR3 - 1.5V RAILS
1.1V
1.8V
FDI & PEG & DMI
Discrete only
Discrete only
for S3 power reduction
6A/maximum
HFM_VID : Max 1.4V
LFM_VID : Min 0.65V
Quanta Computer Inc.
PROJECT : TE2
PROCESSER 3/4(POWER)
Tuesday, March 09, 2010
Sheet 5 of 45

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)





AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

For Discrete only

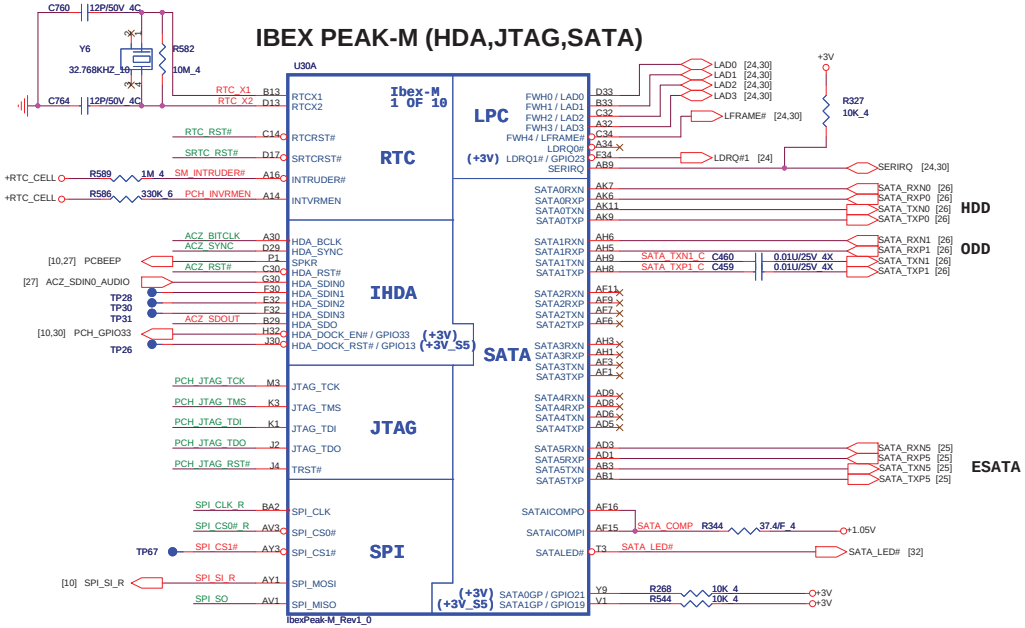
CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**

Quanta Computer Inc.
PROJECT : TE2

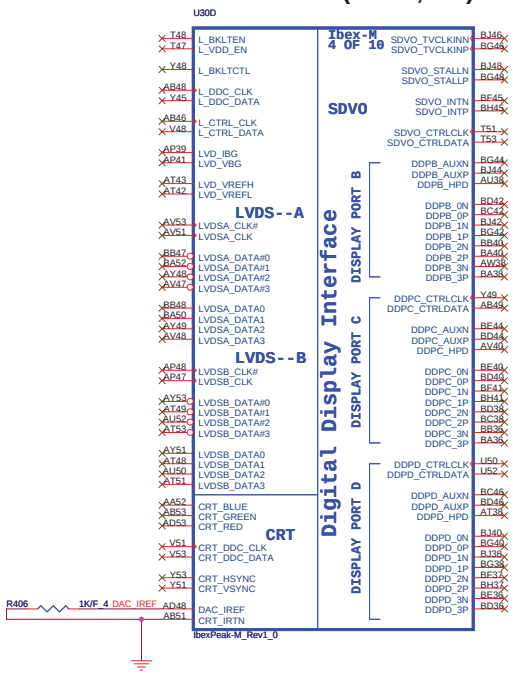
Size	Document Number	Rev
	PROCESSER 4/4 (GND)	2A
Date: Tuesday, March 09, 2010	Sheet 6 of 45	

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

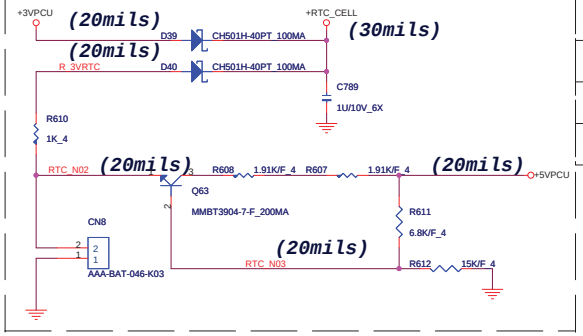


IBEX PEAK-M (LVDS,DDI)



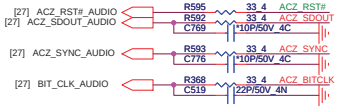
[RTC]

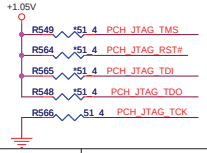
RTC BATTERY



Port	Strap	How to enable Port?	How to disable Port?
LVDS	L_DDC_DATA	PU to 3.3V with 2.2k+/- 5%	NC
Port B	SDVO_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port C	DDPC_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port D	DDPD_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
eDP	CFG[4]	PD to GND directly	NC

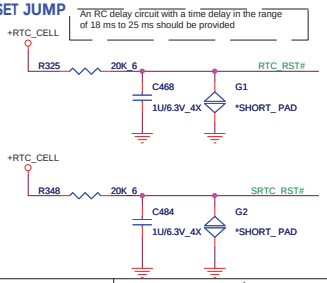
For AUDIO



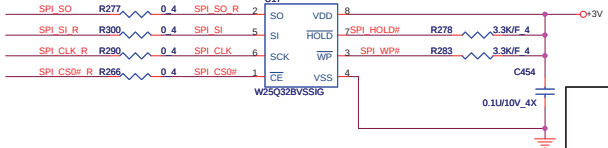


RESET JUMP

An RC delay circuit with a time delay in the range of 18 ms to 25 ms should be provided



4M byte SPI ROM

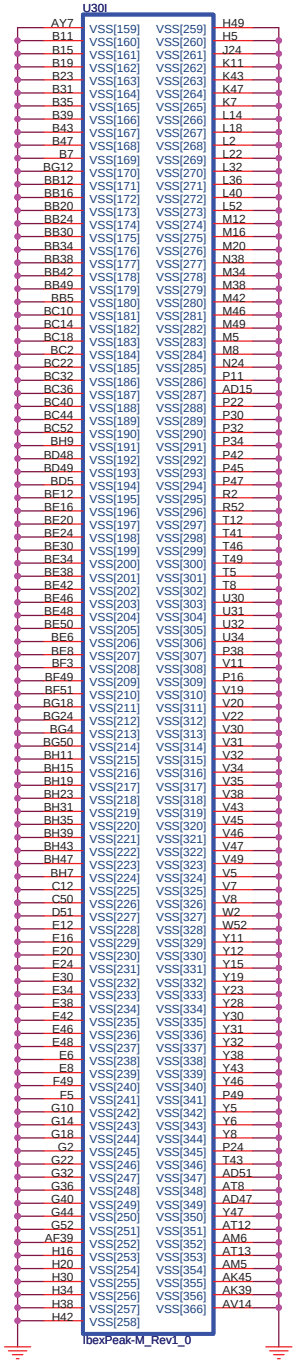


PCH	2MB	4MB	8MB
PM55	●		
HM55		●	
HM57/PM57		●	●
QM57/QS57			●

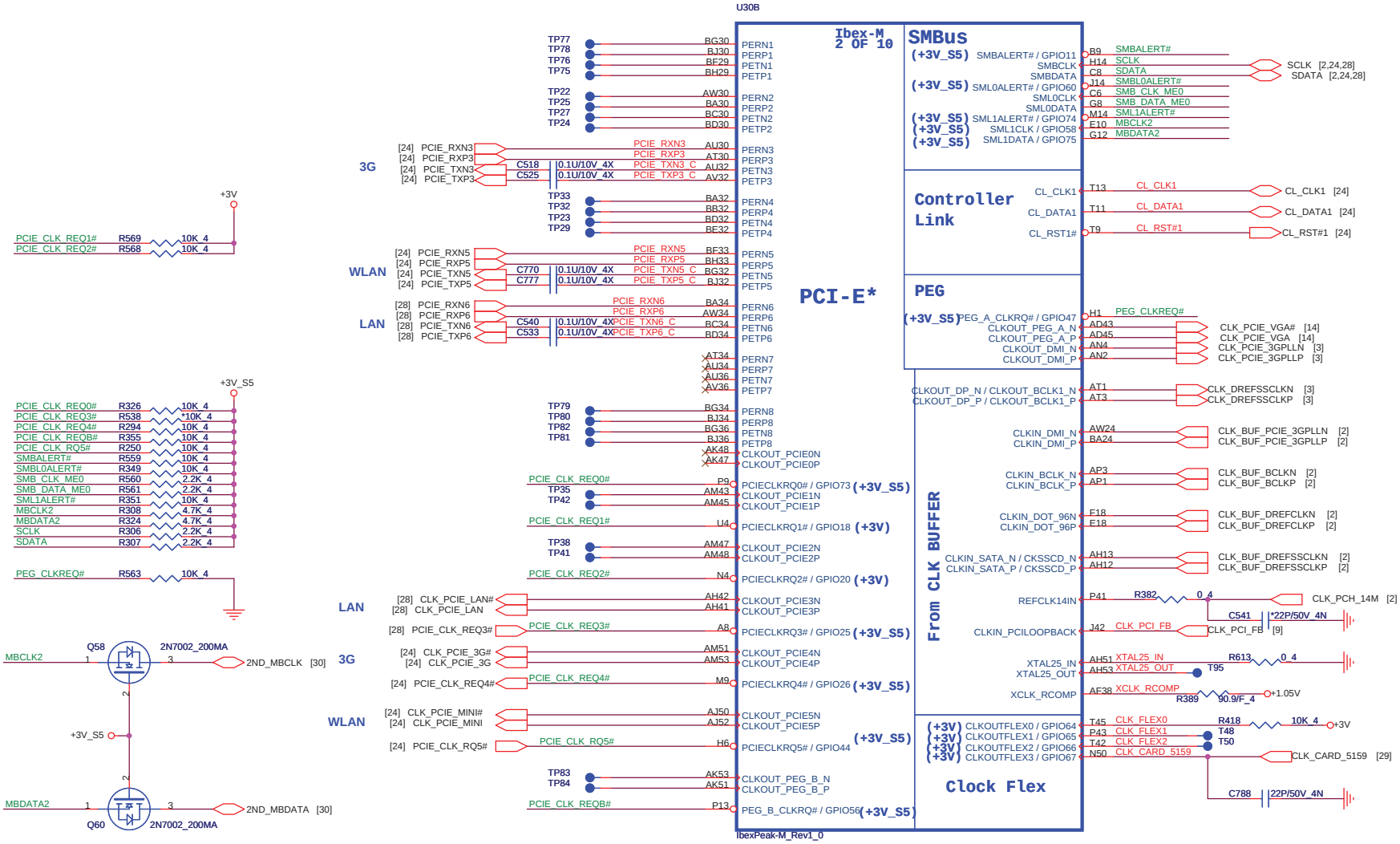
Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	PCH 1/5 (SATA,HDA,LPC)	2A
Date: Tuesday, March 09, 2010	Sheet 7 of 45	

IBEX PEAK-M (GND)

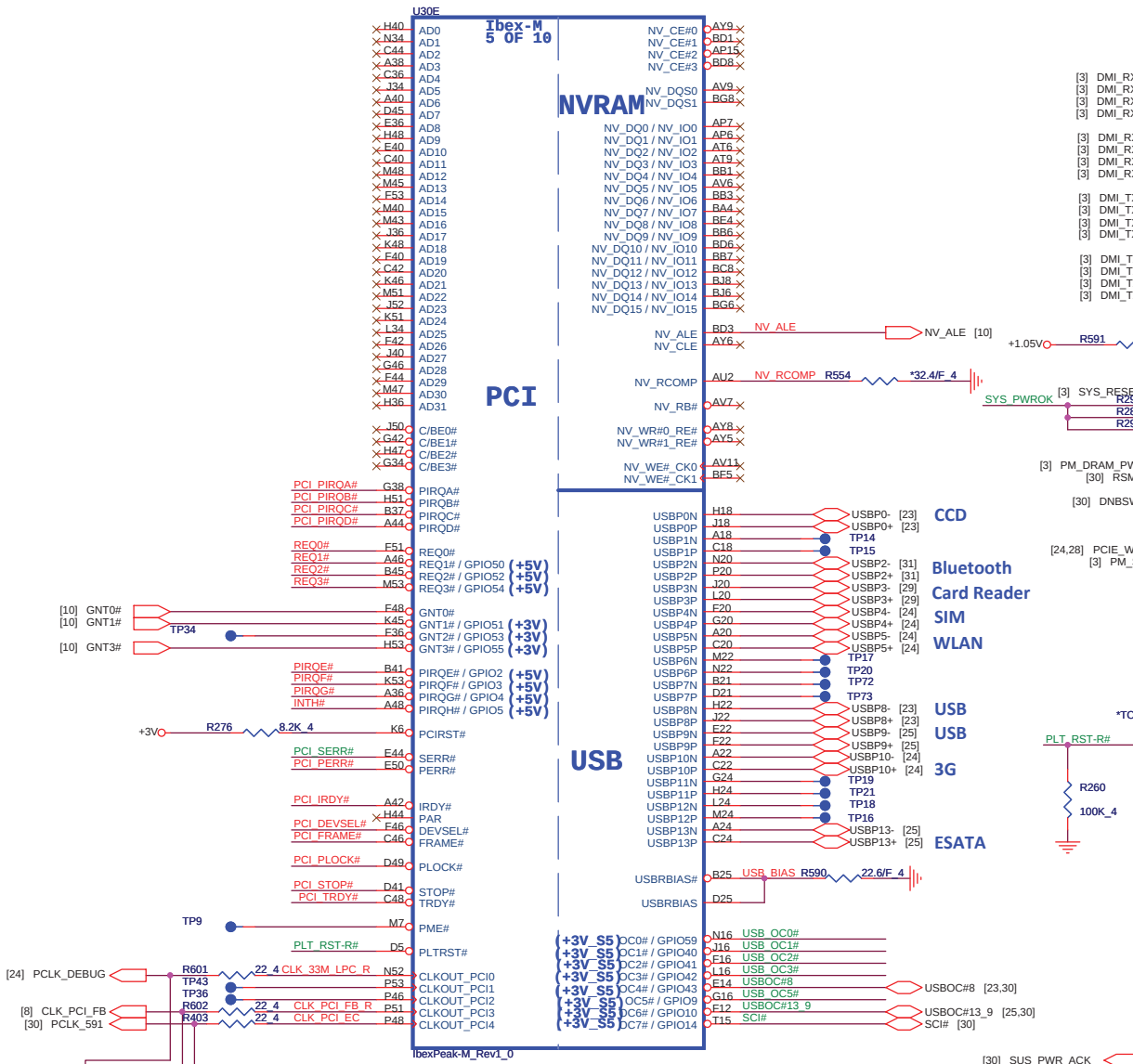


IBEX PEAK-M (PCI-E,SMBUS,CLK)

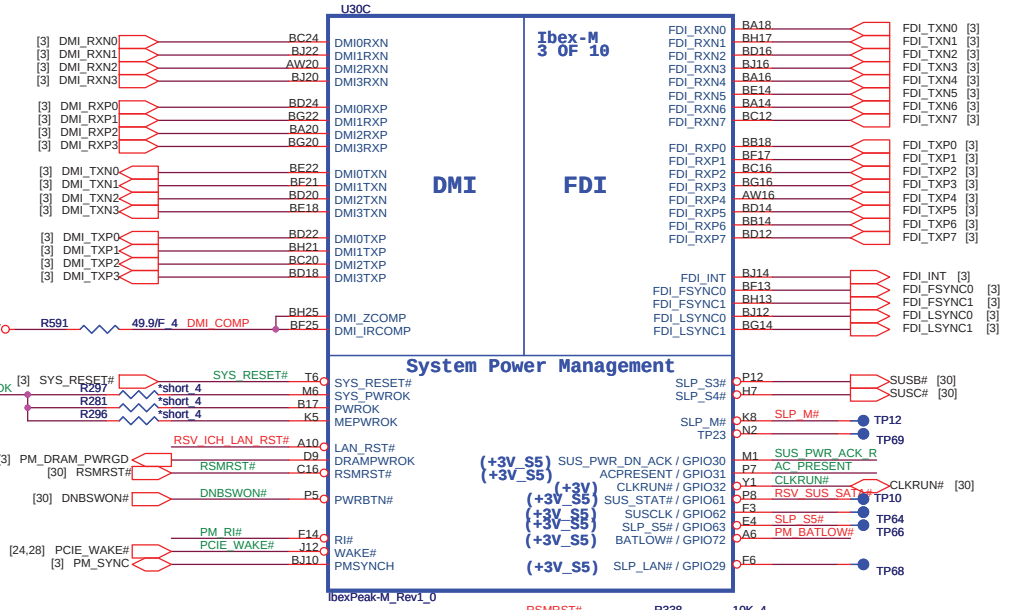


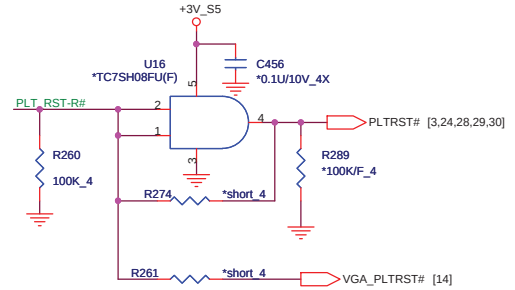
Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: PCH 2/5 (PCIE, SMBUS, CK)	Rev: 2A
Date: Tuesday, March 09, 2010	Sheet 8 of 45	

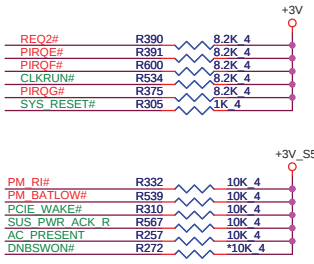
IBEX PEAK-M (PCI,USB,NVRAM)

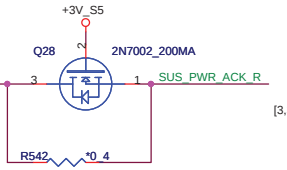


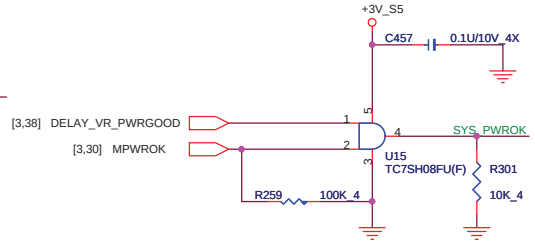
IBEX PEAK-M (DMI,FDI,GPIO)

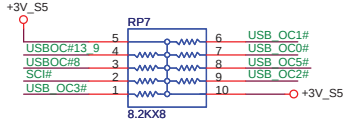


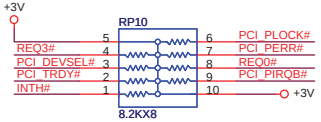


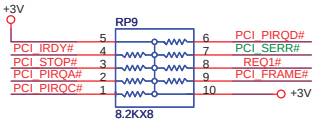










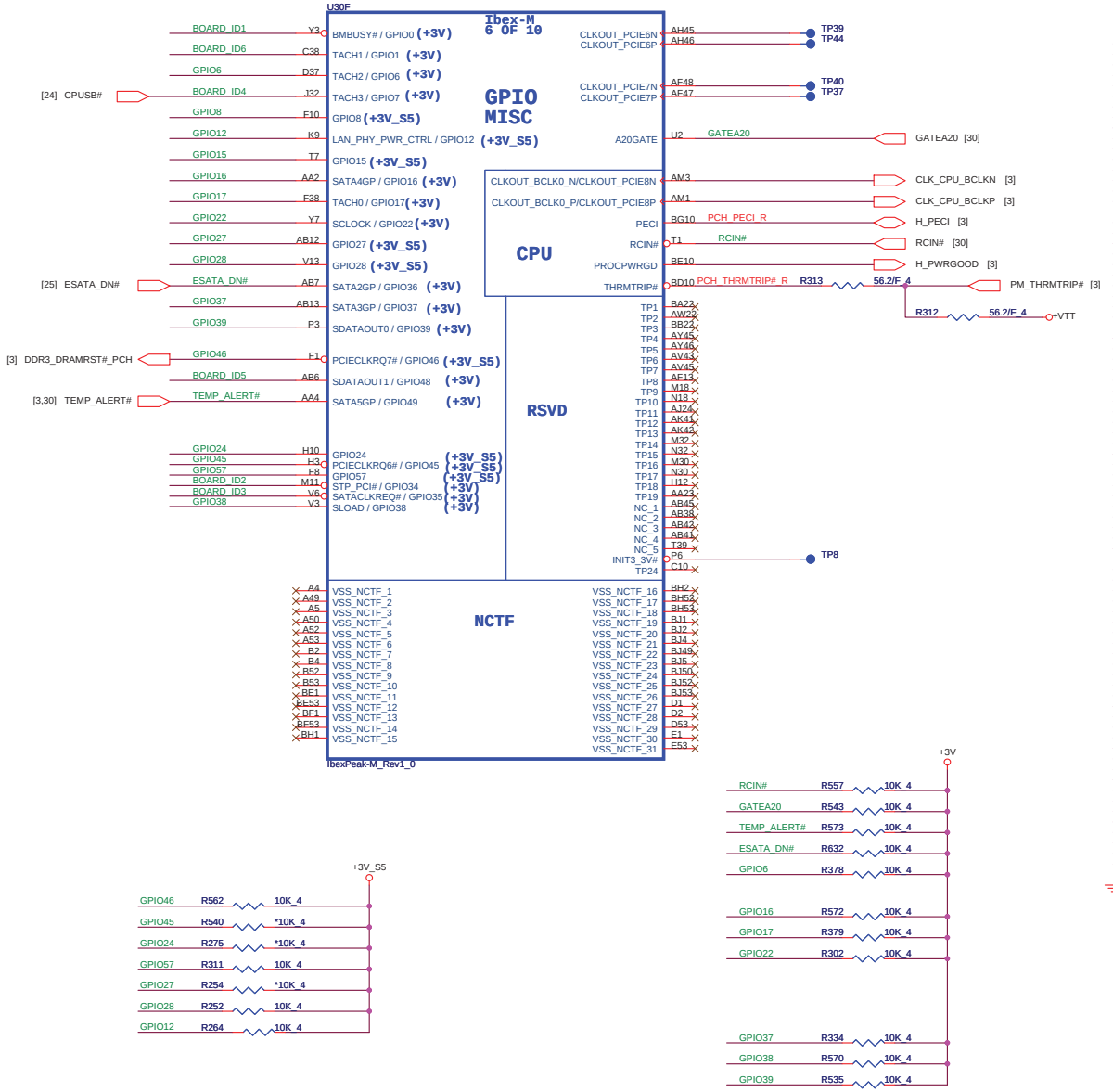


Quanta Computer Inc.

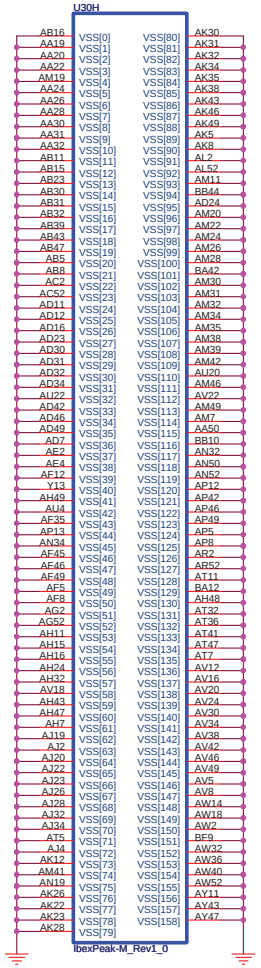
PROJECT : TE2

Size	Document Number	Rev
	PCH 3/5 (PCI,ONFI,USB,DMI)	2A
Date: Tuesday, March 09, 2010	Sheet 9 of 45	

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)



PCH Strap Pin Configuration Table

SPKR

[7,27] PCBEEP — *1K/F_4 — R556 — +3V

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

GNT3#/ GPIO55

[9] GNT3# — R603 — *10K/F_4

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

HDA_DOCK_EN #/GPIO33

[7,30] PCH_GPIO33 — R371 — 1K_4 — JP1 (2, 1) *SHORT PAD

0 = Top Block Swap Mode
1 = Default Mode (Internal pull-up)

GNT0#, GNT1#

[9] GNT0# — GNT0# R397 *1K/F_4
[9] GNT1# — GNT1# R599 *1K/F_4

Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

SPI_MOSI

[7] SPI_SI_R — R279 — *1K_4 — +3V

NV_ALE

[9] NV_ALE — R574 — *10K_4 — +1.8V

1 = Enabled
0 = Disabled (Default)

GPIO8

GPIO8 — R309 — 10K_4 — +3V_S5

This signal has a weak internal pull up.
NOTE: This signal should not be pulled low

GPIO15

GPIO15 — R267 — 1K_4 — +3V_S5

0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

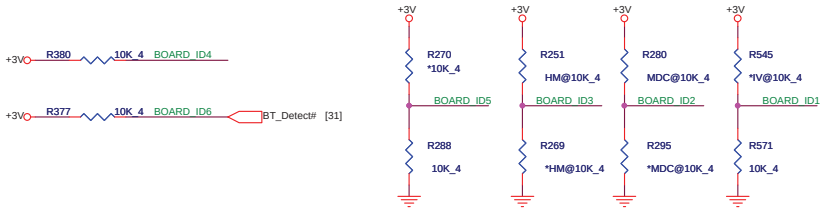
GPIO27

GPIO27 — R271 — *10K_4

0 = Disables the VccVRM. Need to use on-board filter circuits for analog rails.
1 = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit.
This signal has a weak internal pull-up.

BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6
UMA SKU VGA SKU	H L					
W/ MDC W/O MDC		H L				
W/ HDMI W/O HDMI			H L			
W/O 3G W/ 3G				H L		
15" 14"					H L	
W/O BT W/ BT						H L



Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	PCH 4/5 (GPIO & Strap)	2A
Date: Friday, March 19, 2010	Sheet 10 of 45	

+VCCA_DAC_1_2=69mA(15mils)

VCCCORE = 1.432A(80mils)

40mA(15mils)

VCCIO = 3.062A(150mils)

37mA(15mils)

VCCALVDS= 59mA(15mils)

VCCVRM= 196mA(15mils)

VCCPNAND= 156mA(15mils)

68mA(15mils)

VCCME3_3= 85mA(15mils)

VCCIO = 3.062A(150mils)

VCCSUS3_3 = 0.163A(20mils)

VCC3_3 = 0.357A(30mils)

V_CPU >1mA(15mils)

VCCRTC= 2mA(15mils)

VCCSUSHDA= 6mA(15mils)

VCCLAN = 0.32A(30mils)

VCCME = 1.849A(100mils)

VCC3_3 = 0.357A(30mils)

VCCDMI= 61mA(15mils)

V5REF_SUS< 1mA

V5REF< 1mA

VCCIO = 3.062A(150mils)

VCCME = 1.849A(100mils)

Reserve for clear CRT Power

C3A

POWER

Ibex-M 7 OF 10

Ibex-M 10 OF 10

U30G

U30J

CRT

LVDS

HVCMOS

DMI

NAND / SPI

VCC CORE

PCI E*

FDI

USB

SATA

PCI/GPIO/LPC

CPU

RTC

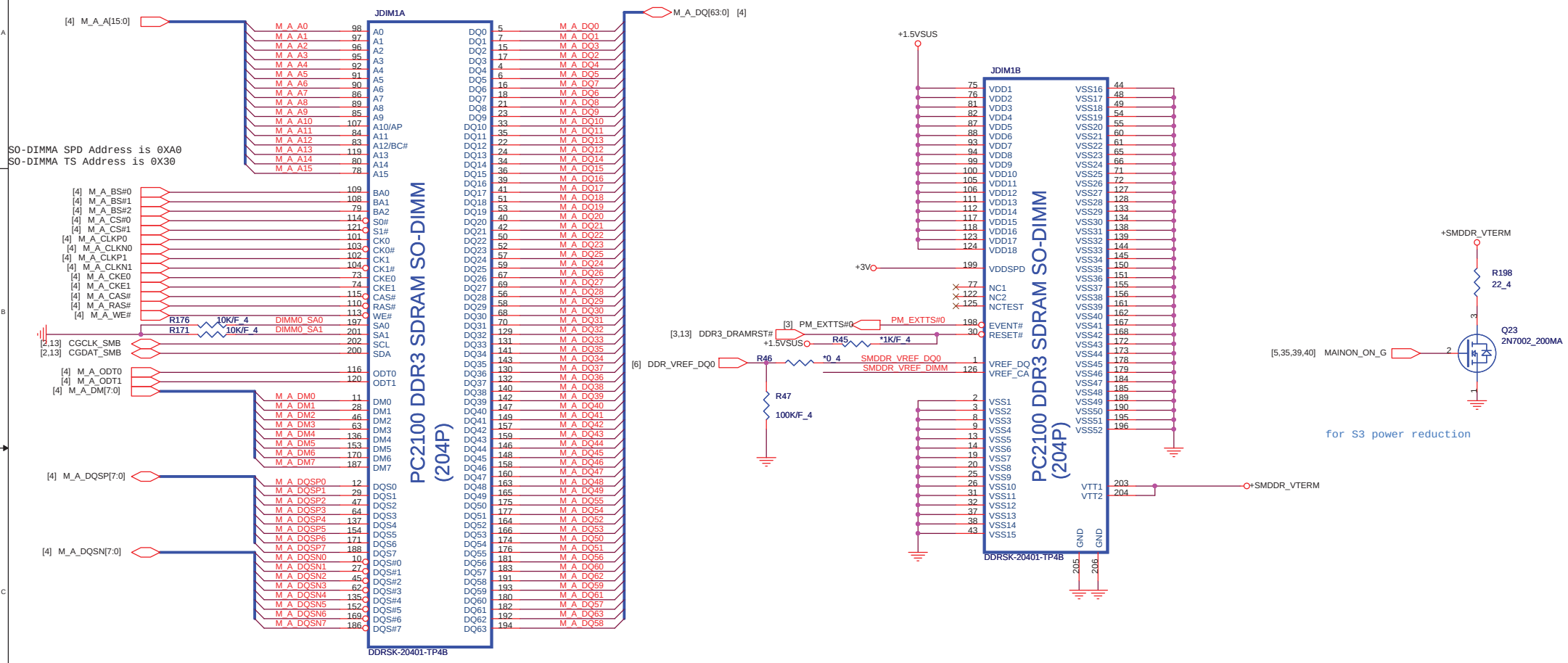
HDA

Clock and Miscellaneous

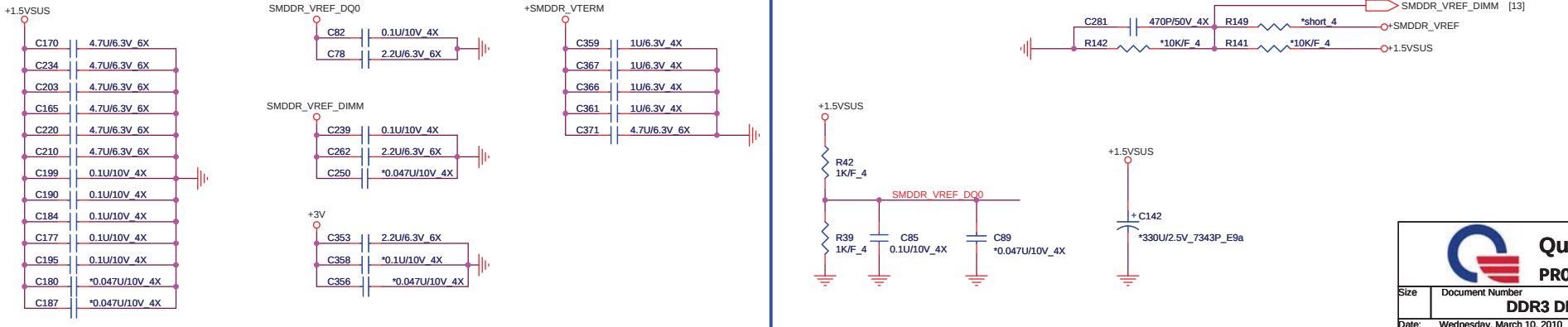
IbexPeak-M_Rev1_0

U21 *G913C

Quanta Computer Inc.	
PROJECT : TE2	
Size	Document Number: PCH 5/5 (POWER) — Rev: 2A
Date: Wednesday, March 10, 2010	Sheet 11 of 45



Place these Caps near So-Dimm0.



Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: DDR3 DIMM-0	Rev: 2A
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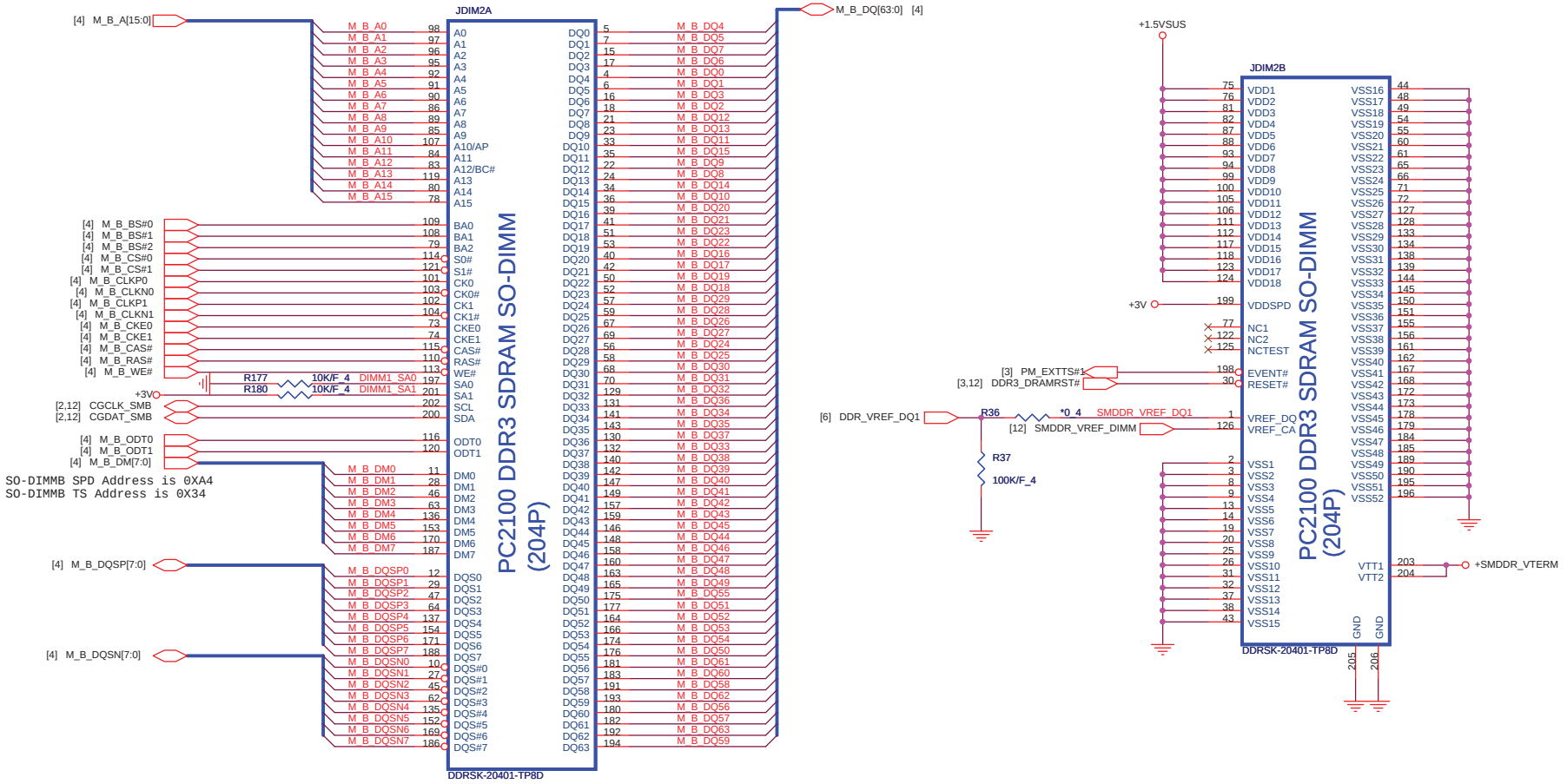
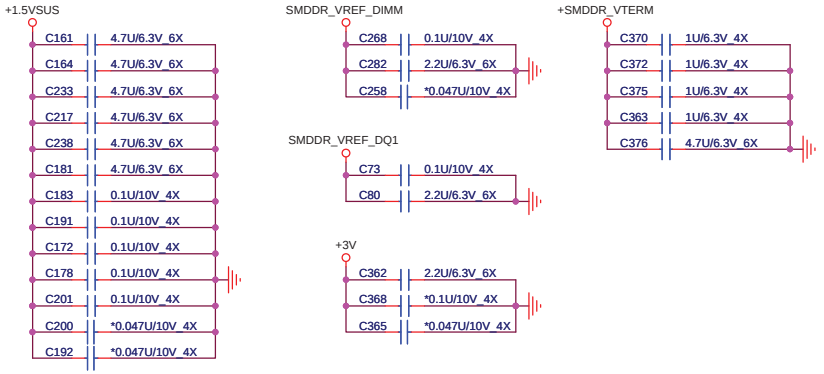
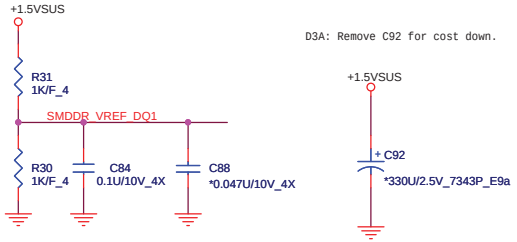


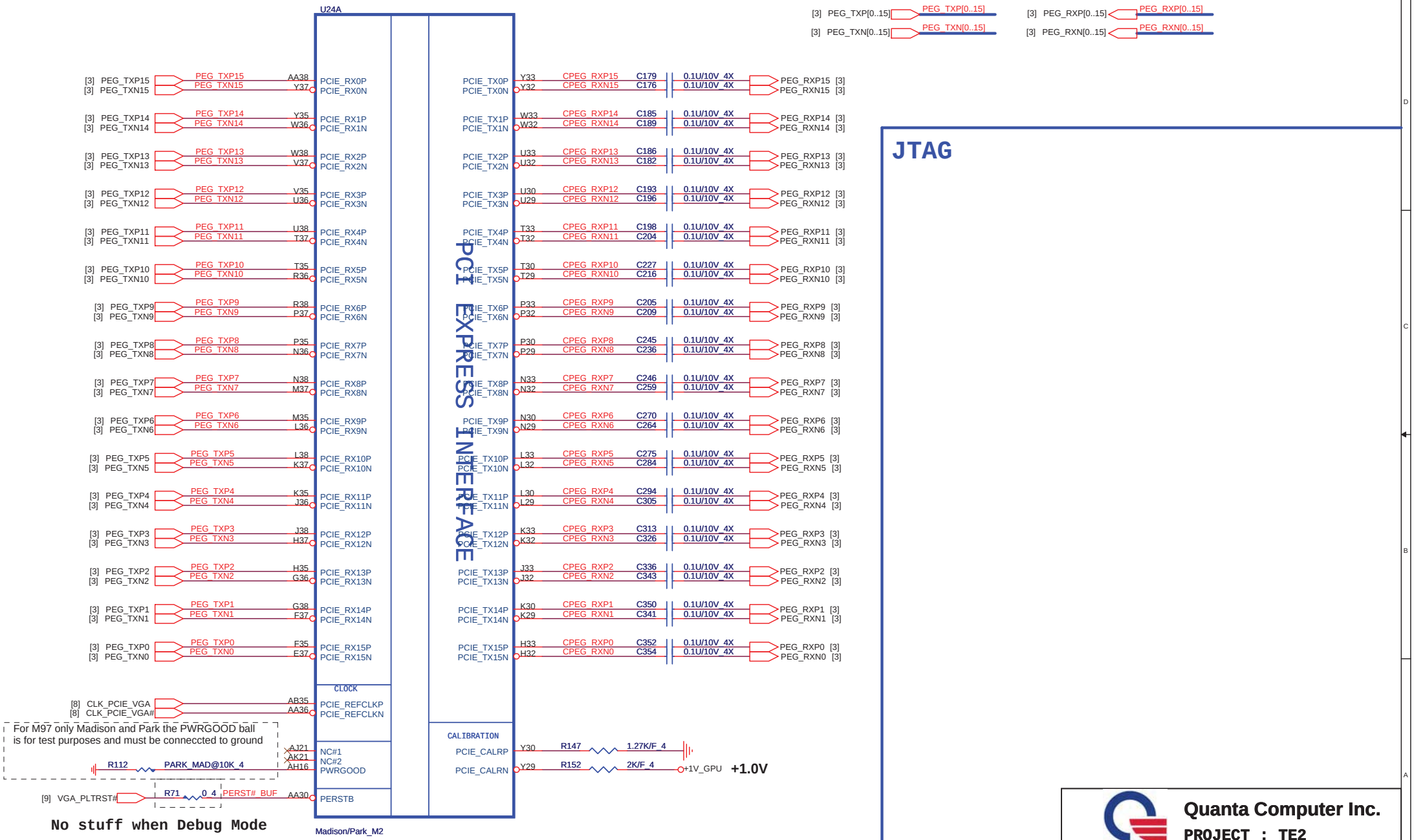
Place these Caps near So-Dimm1.





D3A: Remove C92 for cost down.

Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: DDR3 DIMM-1	Rev: 2A
Date: Wednesday, March 10, 2010	Sheet 13 of 43	



For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V

GPU Power-on sequence

1 => +VGPU_CORE
2 => +VGPU_IO
3 => +1V_GPU
4 => +1.5V_GPU
5 => +3V_D
6 => +1.8V_GPU
7 => +GPU_PWROK

JTAG SIGNAL STUFF OPTION FOR OPTION2

SIGNALS	NORMAL MODE	JTAG MODE (DEBUG
TESTEN	"1" (PU)	"1" (PU)
GPIO24_TRSTB	"0" (PD)	"1" (PU)
GPIO26_TCK	CLK	"1" (PU)
GPIO27_TMS	"1" (PU)	"1" (PU)

1.8V GPIO

NC on Park

SCL must be tied high if not used

DP

PLACE AC CAP CLOSE TO CONNECTOR

NC on Park

LVDS

HDMI DDC

HDMI

CRT

NC on Park

LVDS

NC on Park

Place close to Chip

+1.8V(20mA)

75mA (10mils)

125mA (10mils)

(1.8V@70mA AVDD)

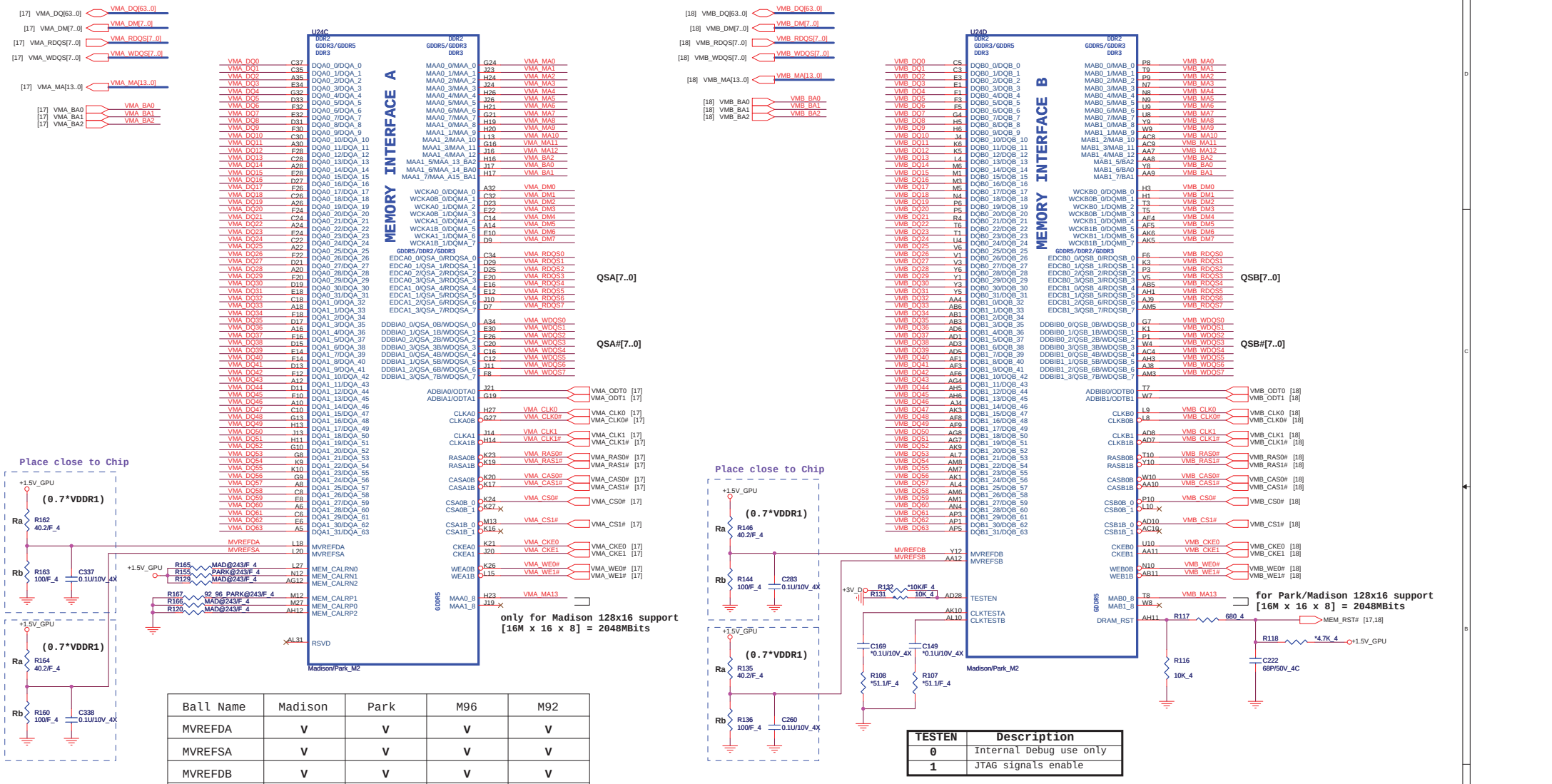
(1.8V@100mA VDD1DI)

(1.8V@2mA A2VDDQ)

Madison/Park_M2

Madison/Park_M2

Quanta Computer Inc.
PROJECT : TE2
Size: Document Number: Madison/Park-HOST I/F Rev: 2A
Date: Wednesday, March 10, 2010 Sheet 15 of 45

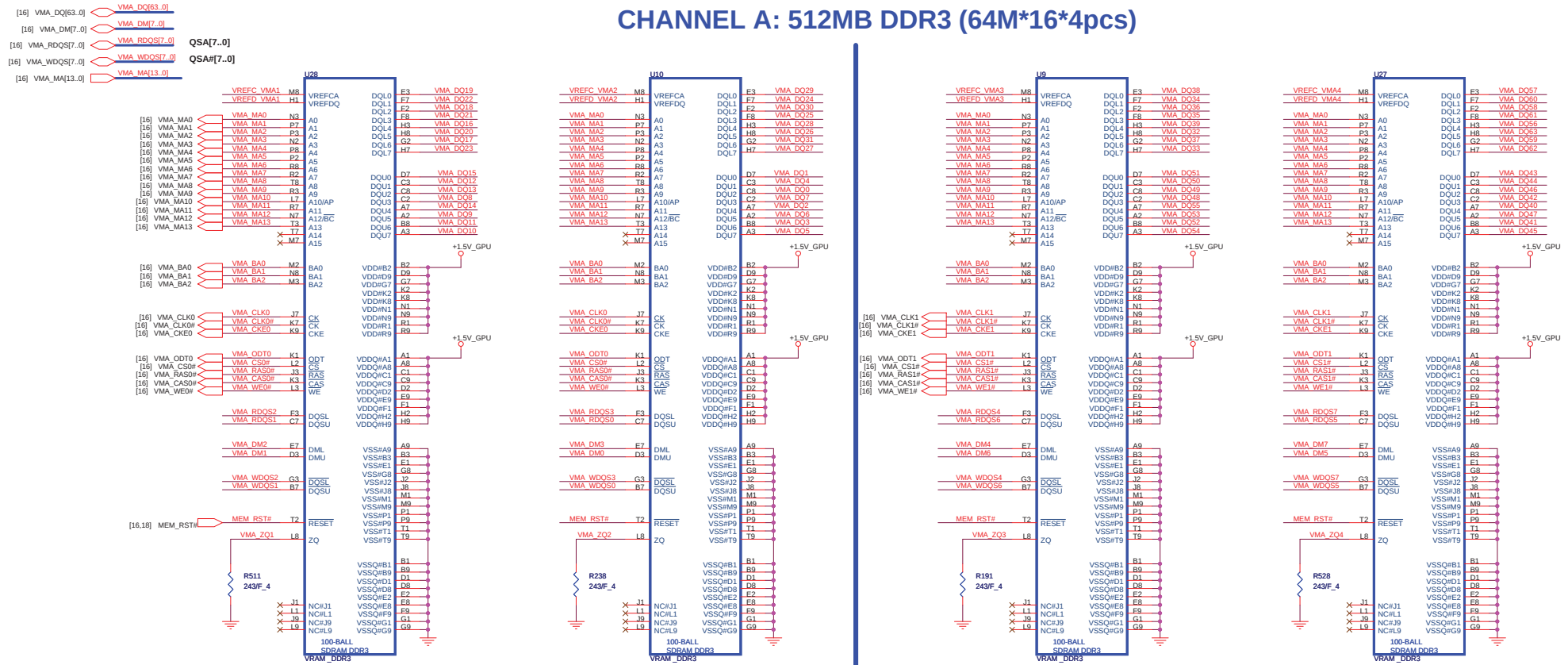


Ball Name	Madison	Park	M96	M92
MVREFDA	V	V	V	V
MVREFSA	V	V	V	V
MVREFDB	V	V	V	V
MVREFSB	V	V	V	V
MEM_CALRN0	V	V		
MEM_CALRN1	V	V		
MEM_CALRN2	V			
MEM_CALRP0	V	V		
MEM_CALRP1	V	V	V	V
MEM_CALRP2	V			

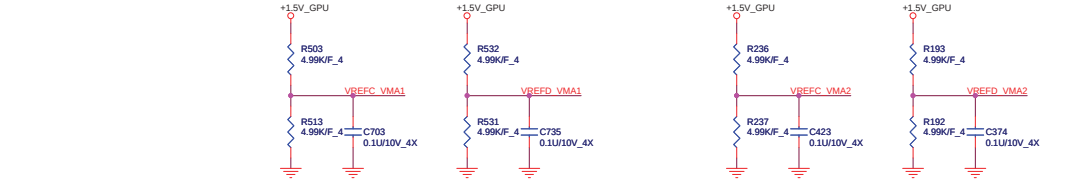
TESTEN	Description
0	Internal Debug use only
1	JTAG signals enable

Quanta Computer Inc.
PROJECT : TE2
Size | Document Number | Rev 2A
Madison/Park-MEM I/F
Date: Tuesday, March 09, 2010 | Sheet 16 of 45

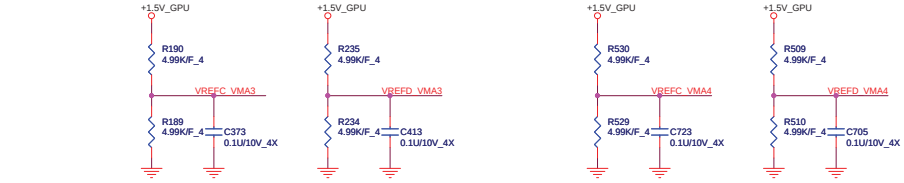
CHANNEL A: 512MB DDR3 (64M*16*4pcs)



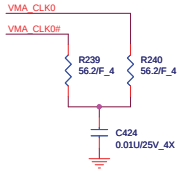
Group-A0 VREF



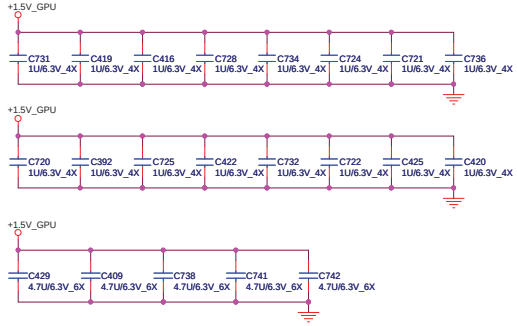
Group-A1 VREF



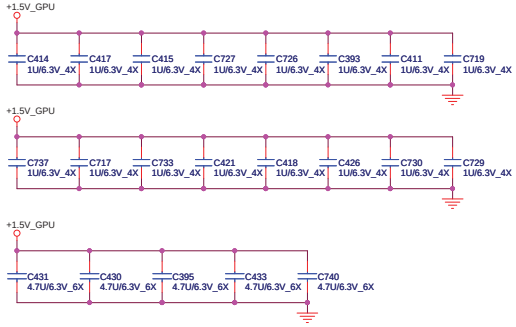
MEM_A0 CLK



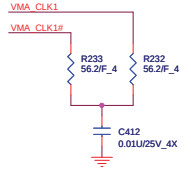
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK

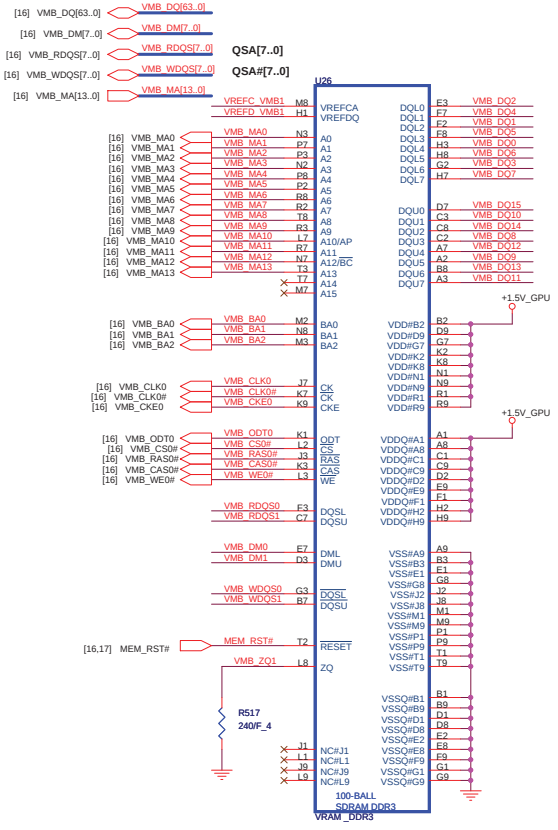


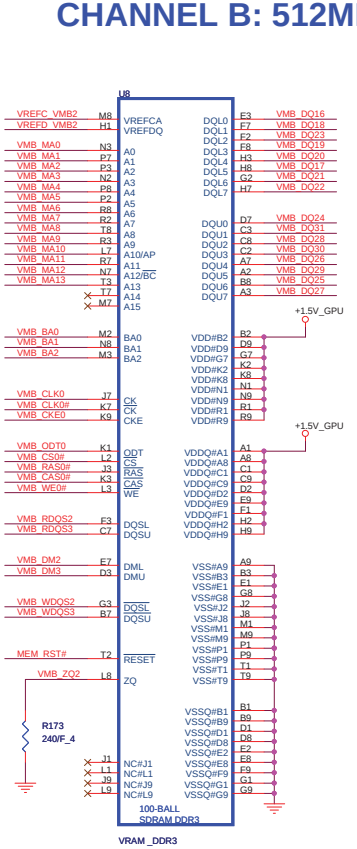
Quanta Computer Inc.

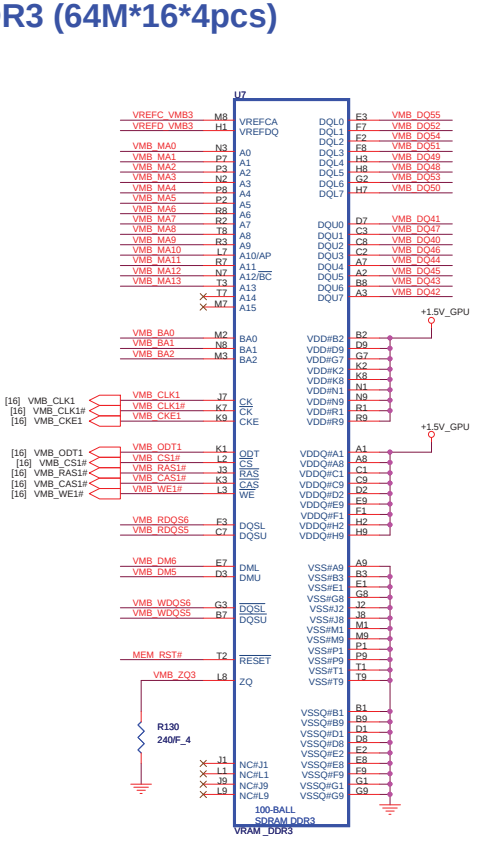
PROJECT : TE2

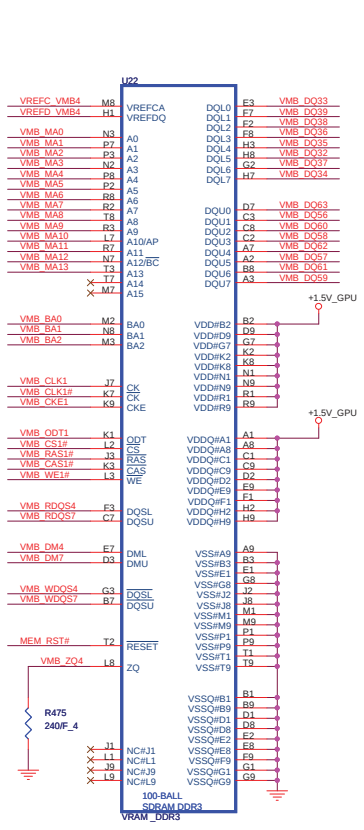
Size	Document Number	Rev
	VRAM_A: DDR3-64M*16*4PCS	2A
Date: Friday, March 19, 2010	Sheet 17 of 45	

CHANNEL B: 512MB DDR3 (64M*16*4pcs)

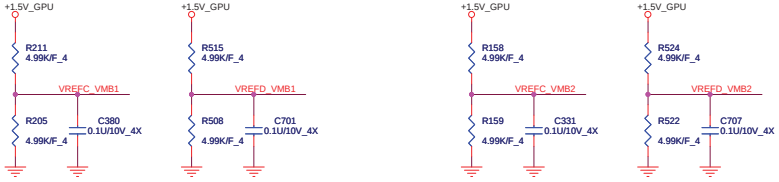




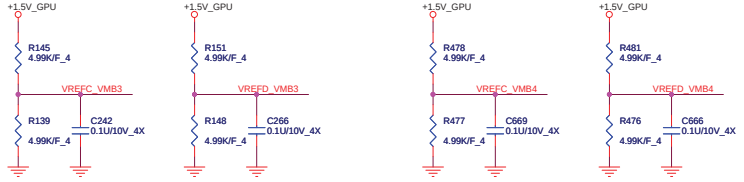




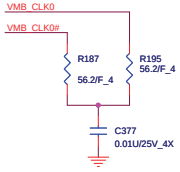
Group-B0 VREF



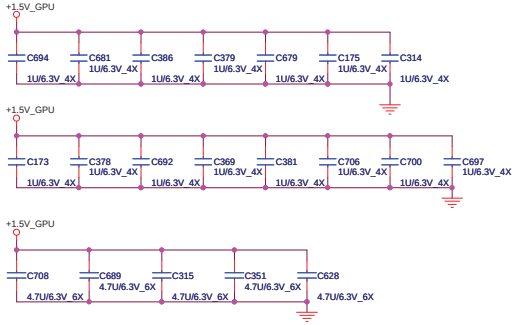
Group-B1 VREF



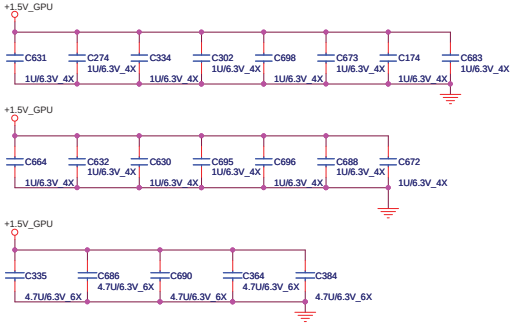
MEM_B0 CLK



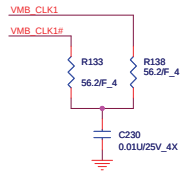
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: VRAM_B: DDR3-64M*16*4PCS	Rev: 2A
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For Madison and Park VDDCI and VDDC can share one common regulator

VDD/VDDQ =1.5V at 1333
VDD/VDDQ =1.8V at 1600 and 1800

U24E

MEM I/O

PCIE

CORE

POWER

LEVEL TRANSLATION

I/O

PLL

VOLTAGE SENESE

Madison/Park_M2

U24F

GND

(1.5V@5A_VDDR1)

(1.8V@400mA PCIE_VDDR)

(1.0V@2A PCIE_VDDC)

(30A or more)

(1.8V@110mA VDD_CT)

(3.3V@60mA)

(1.8V@170mA)

M96 ONLY

(1.8V@40mA PCIE_PVDD)

Park,Madison ONLY

(1.8V@150mA MPV18)

Park,Madison ONLY

(1.8V@75mA SPV18)

(1.0V@120mA SPV10)

(DDR3 1.12V@4A VDDCI) or more

PowerXpress control signal for Madsion and Park only
If not used, can be disconnected. (AL21 pin)

PX_EN = LOW, turn on
PX_EN = HIGH, turn off

Pin AL21 to Ground for Broadway

GPU all PWROK

Route as differential Pair

GPU +3V power

0.5A

Quanta Computer Inc.
PROJECT : TE2

Size: | Document Number: Madison/Park PWR_GND | Rev: 2A

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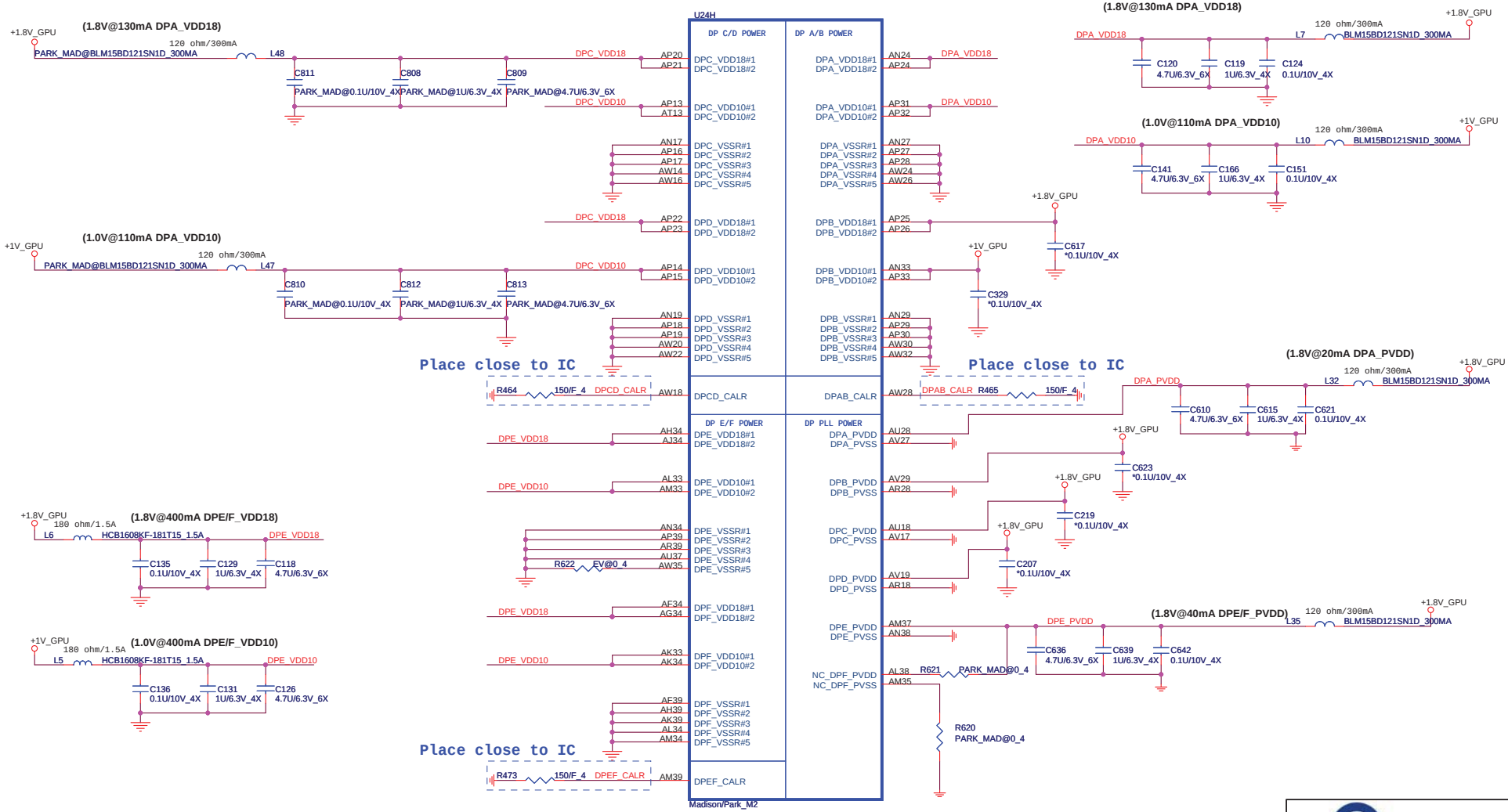
U24H
DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER
Madison/Park_M2
(1.8V@130mA DPA_VDD18)
(1.0V@110mA DPA_VDD10)
(1.8V@20mA DPA_PVDD)
(1.8V@40mA DPE/F_PVDD)
(1.8V@400mA DPE/F_VDD18)
(1.0V@400mA DPE/F_VDD10)
Place close to IC
Place close to IC
Place close to IC
DPF
M92,M96-->NC
Madison,Park-->1.8V and GND
Quanta Computer Inc.
PROJECT : TE2
Madison/Park DPPW_GND
Rev 2A
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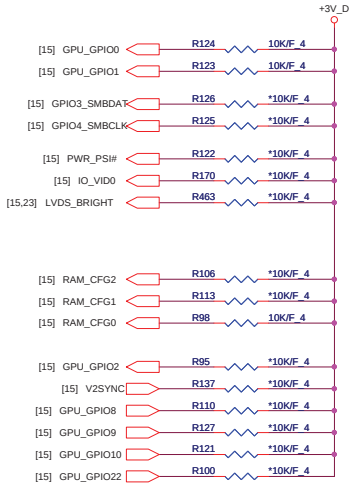
PIN STRAPS



Memory Aperture size	
RAM_CFG[2:0]	Size
000	128MB
001	256MB
010	64MB
011	32MB

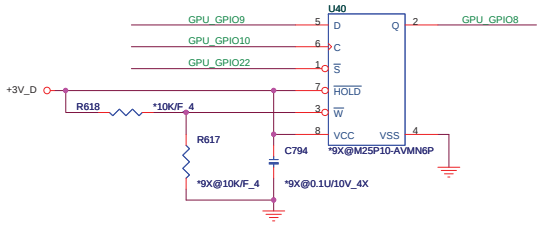
ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

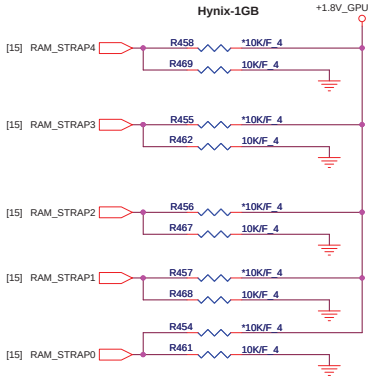
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM (Only for GDDR5) 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA VIP: Video Capture Port Interface	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

EEPROM

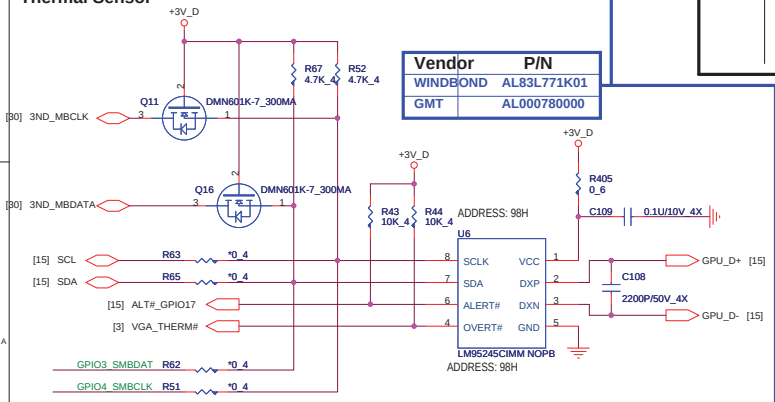


DDR3 Memory TYPE

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0	RAM_STRAP4 15"	RAM_STRAP4 14"
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW00 (64M*16)	512MB	0	1	0	0	0	1
			1GB	0	0	0	0	0	1
Samsung	K4W1G1646E-HC12	AKD5LGGT502 (64M*16)	512MB	0	1	0	1	0	1
			1GB	0	0	0	1	0	1
									1

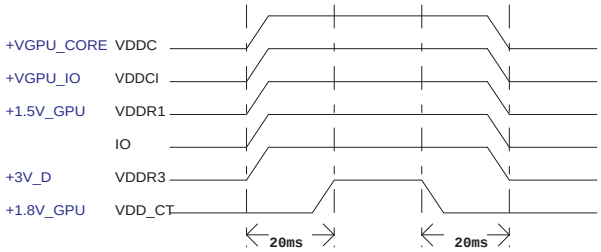


Thermal Sensor



Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

Power Up/Down Sequence



+1V

Quanta Computer Inc.
PROJECT : TE2
Size | Document Number: Memory strip/Thermal/HDCP | Rev 2A
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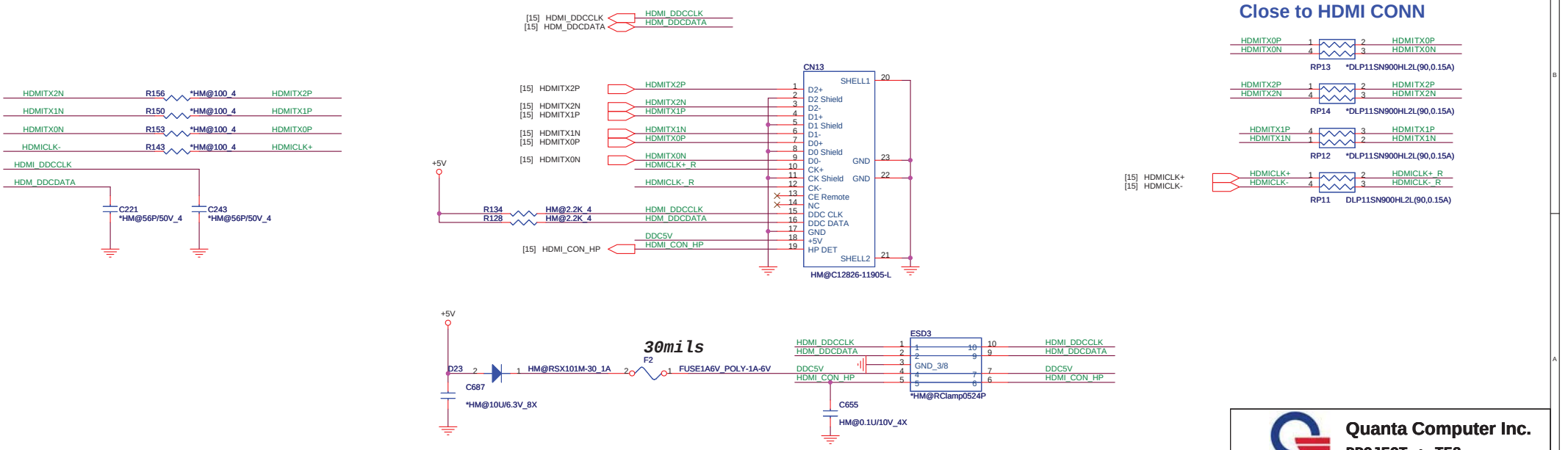
HDMI Conn



Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	HDMI CONN	2A

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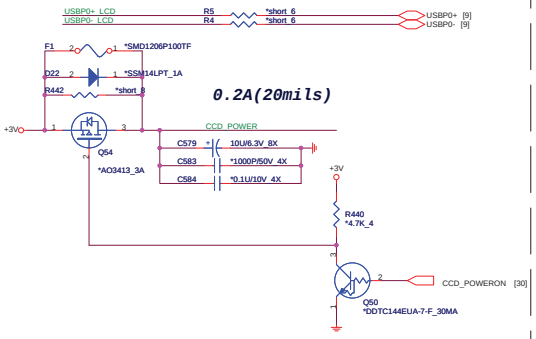
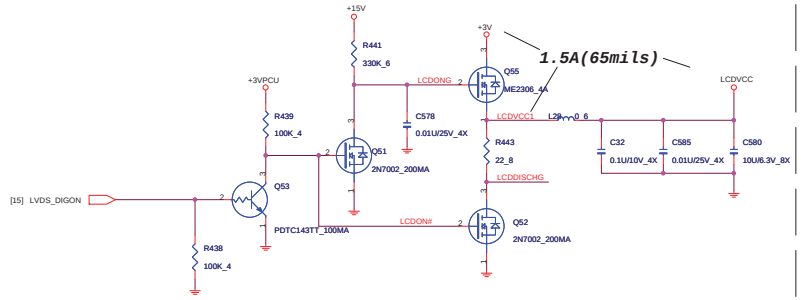
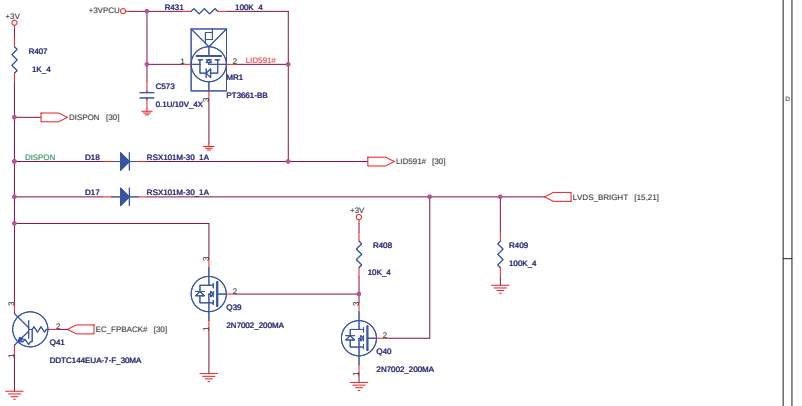
CCD [CCD]



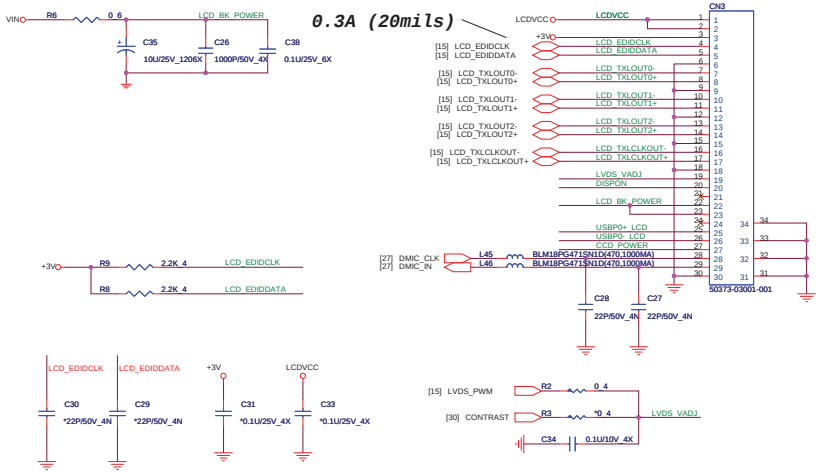
LCD POWER SWITCH [LDS]



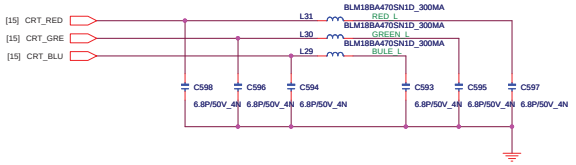
HALL SENSOR&BACK LIGHT SWITCH [HSR]

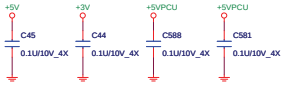


LCD Panel Module [LDS]

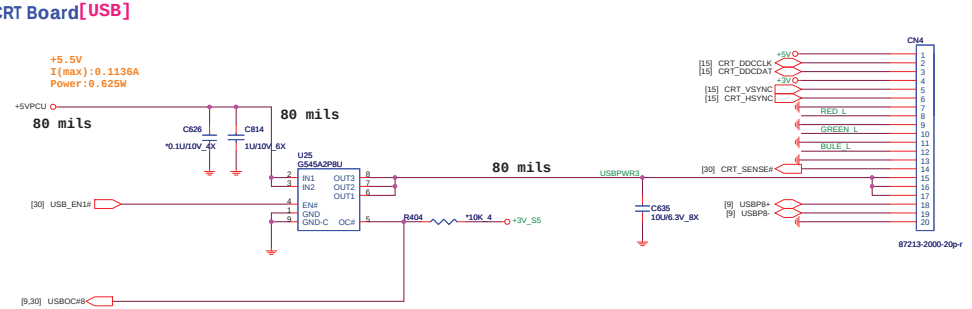


CRT [CRT]





USB To CRT Board[USB]



Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	LCD/LED Panel/CCD	2A
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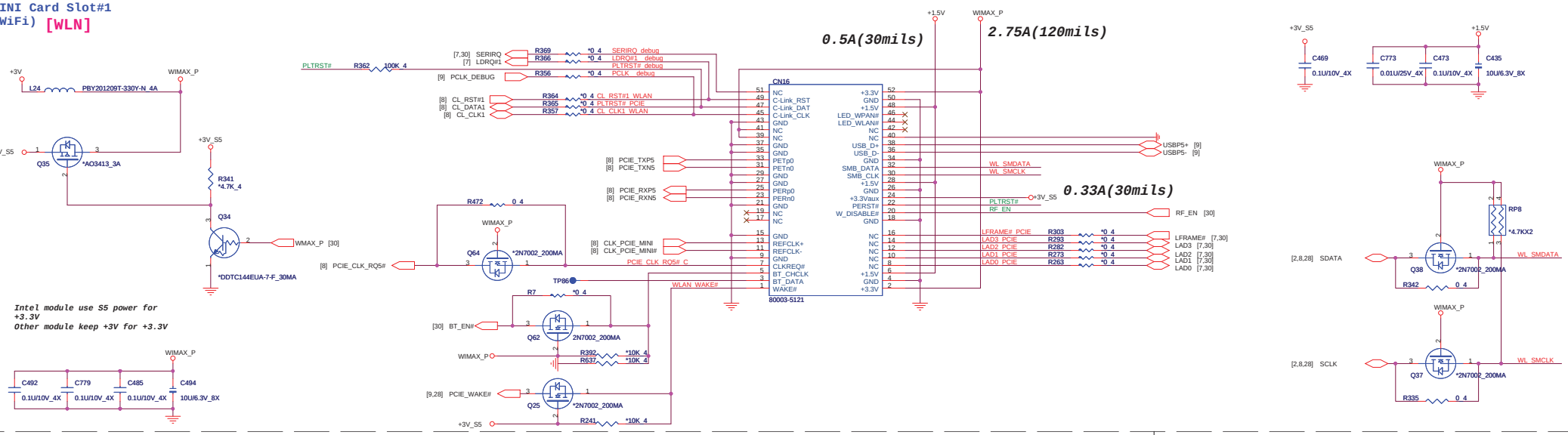
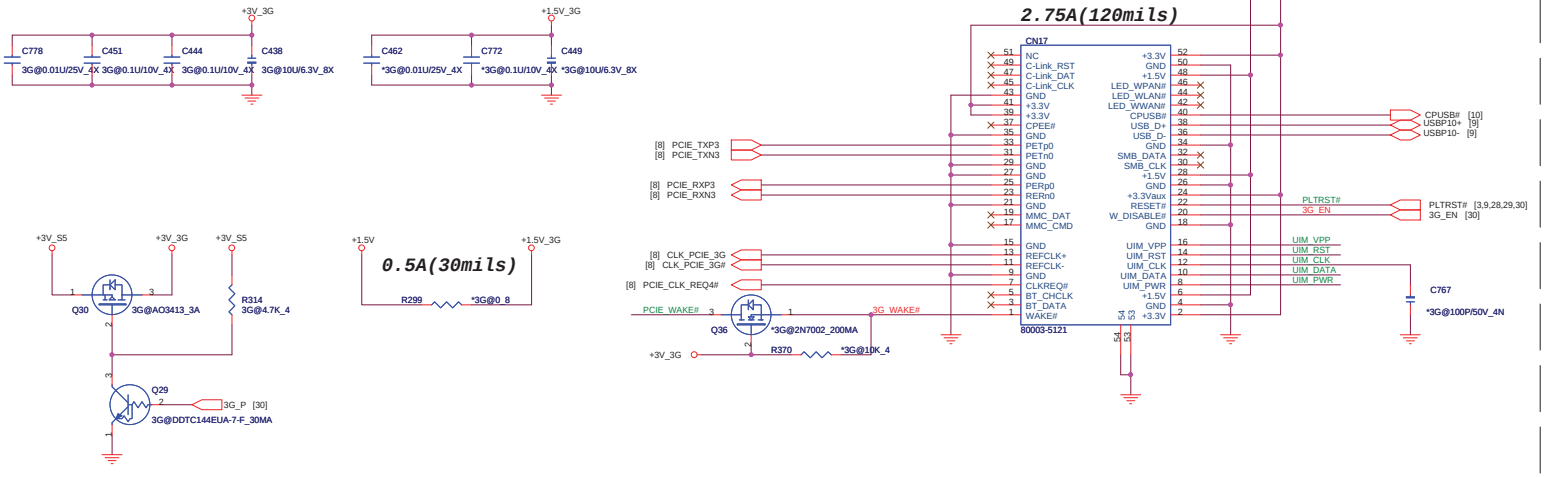
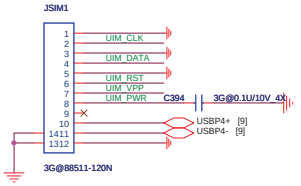
MINI Card Slot#1 (WiFi) [WLN]



MINI Card Slot#2 3G [M3G]



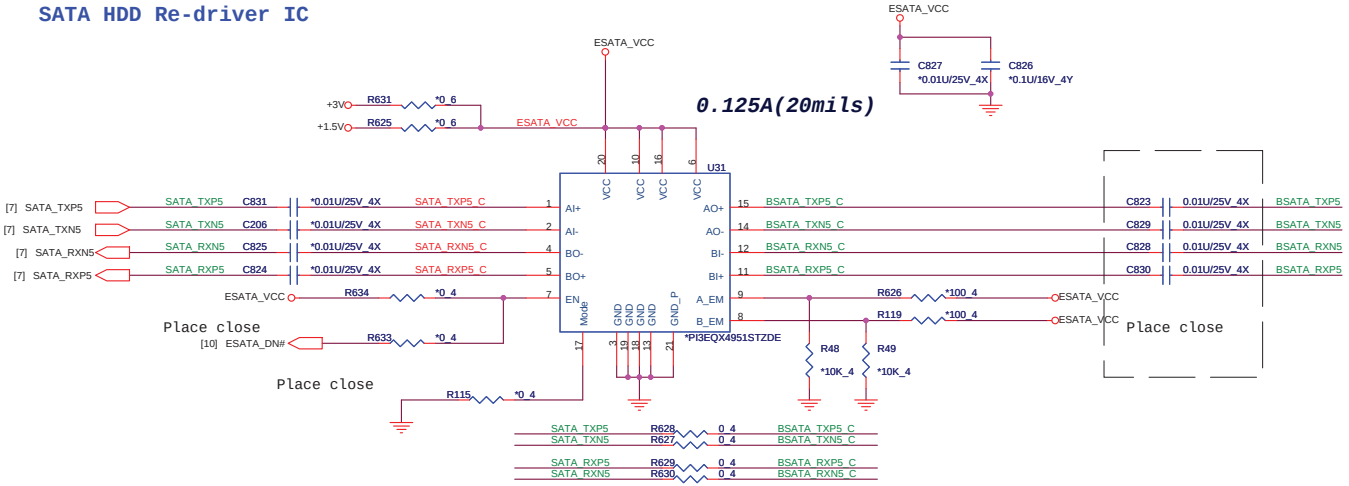
SIM CARD



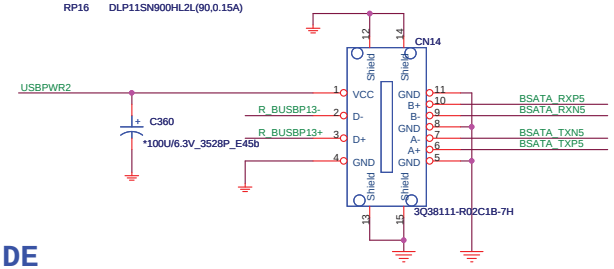
Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: MINI CARD(WLAN/3G/SIM Card)	Rev 2A
Date: Friday, March 19, 2010	Sheet 24 of 45	

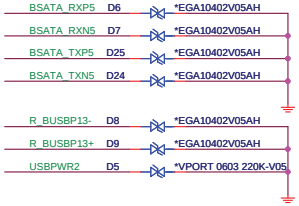
E-SATA [ESA]

SATA HDD Re-driver IC

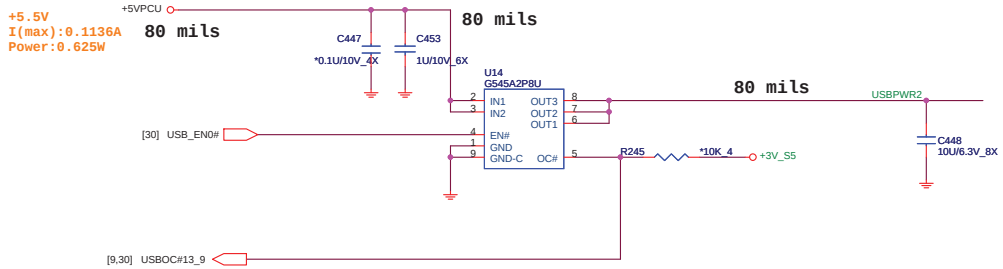


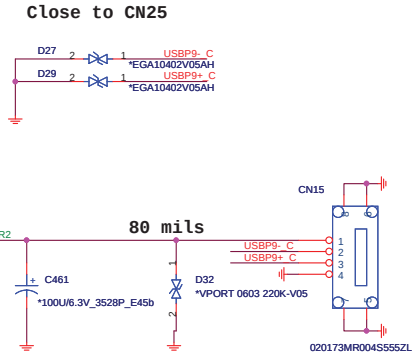
ESATA CONN

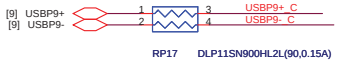




USB MB SIDE







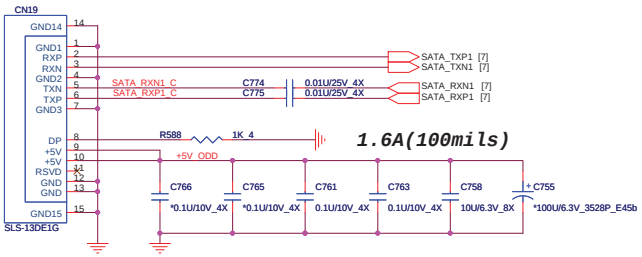
Quanta Computer Inc.
PROJECT : TE2

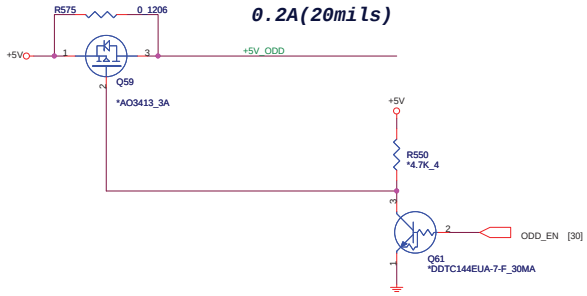
Size	Document Number	Rev
	TP/SW/ESATA/USB+Audio/LED	2A

Date: Tuesday, March 09, 2010 Sheet 25 of 45

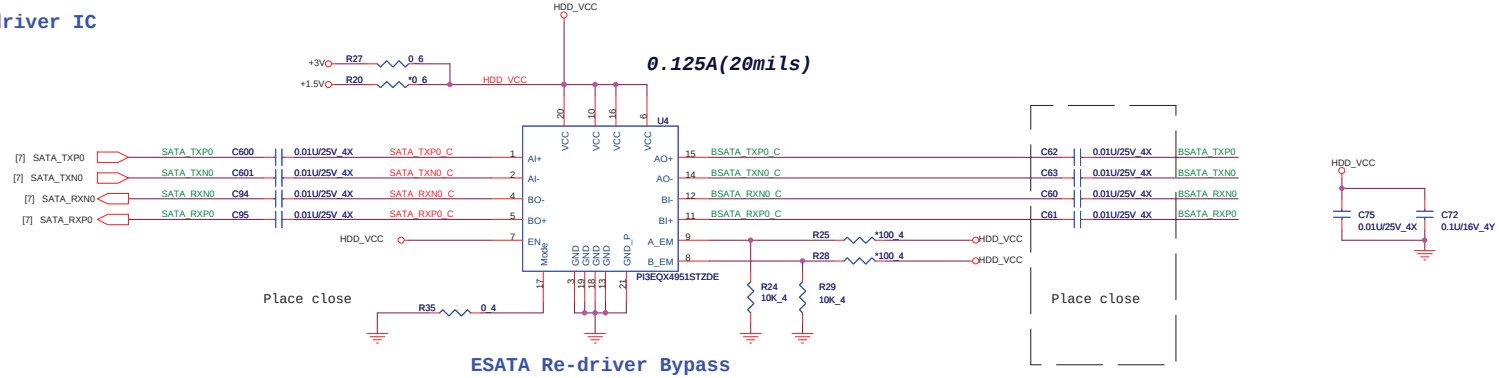
SATA ODD

[ODD]



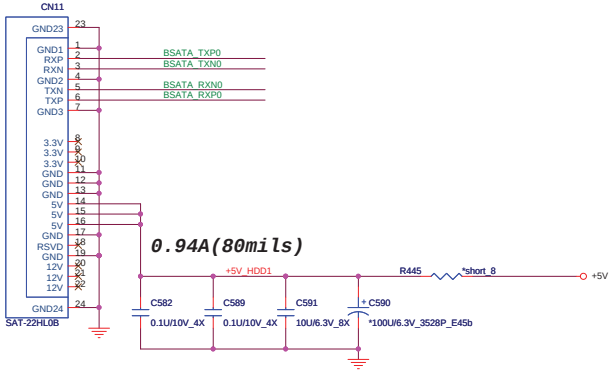


SATA HDD Re-driver IC



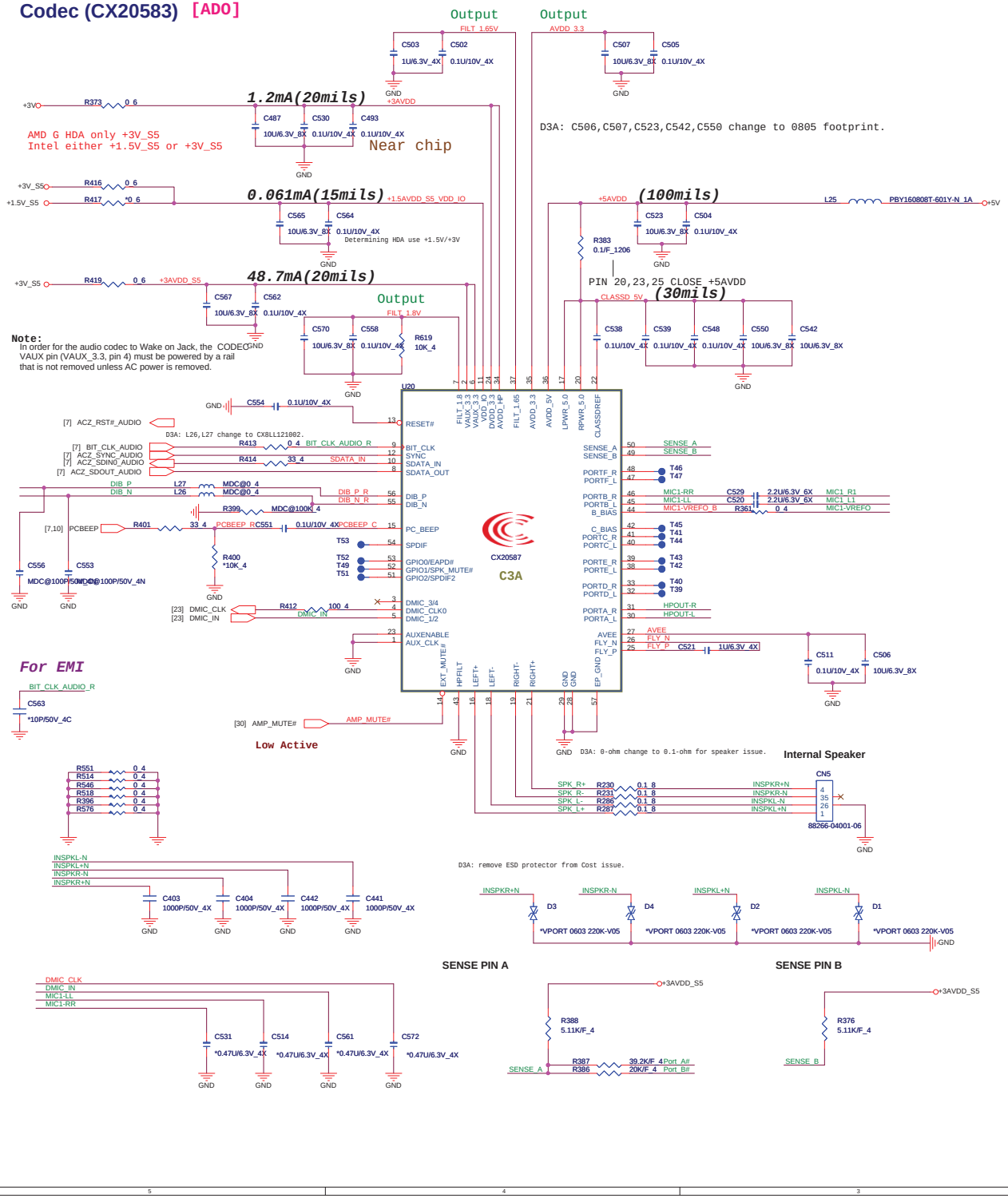
SATA HDD

[HDD]



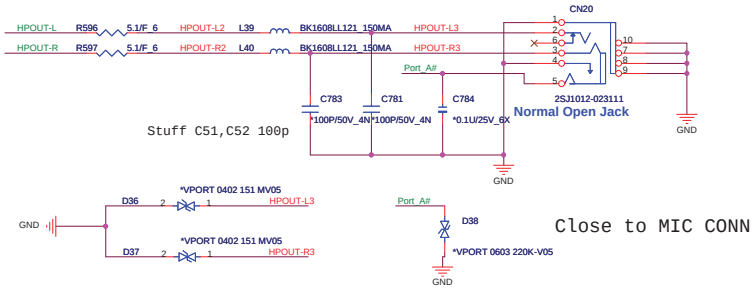
Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: HDD/ODD/MDC	Rev: 2A
Date: Tuesday, March 09, 2010	Sheet 26 of 45	

Codec (CX20583) [ADO]

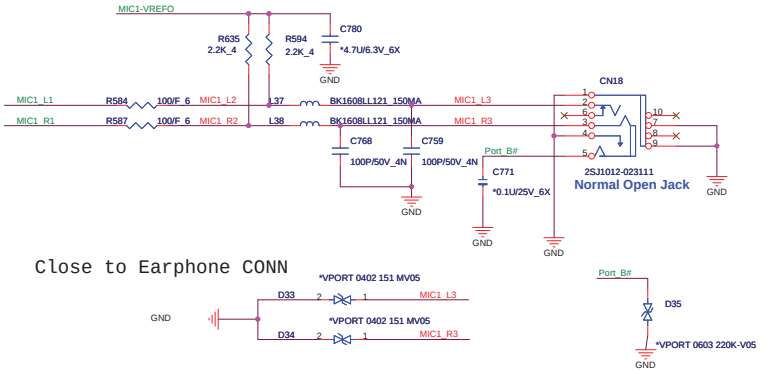


AUDIO JACK

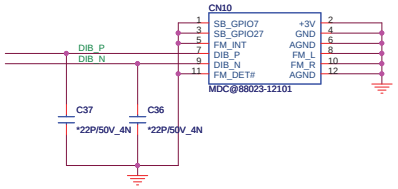
Earphone



External MIC



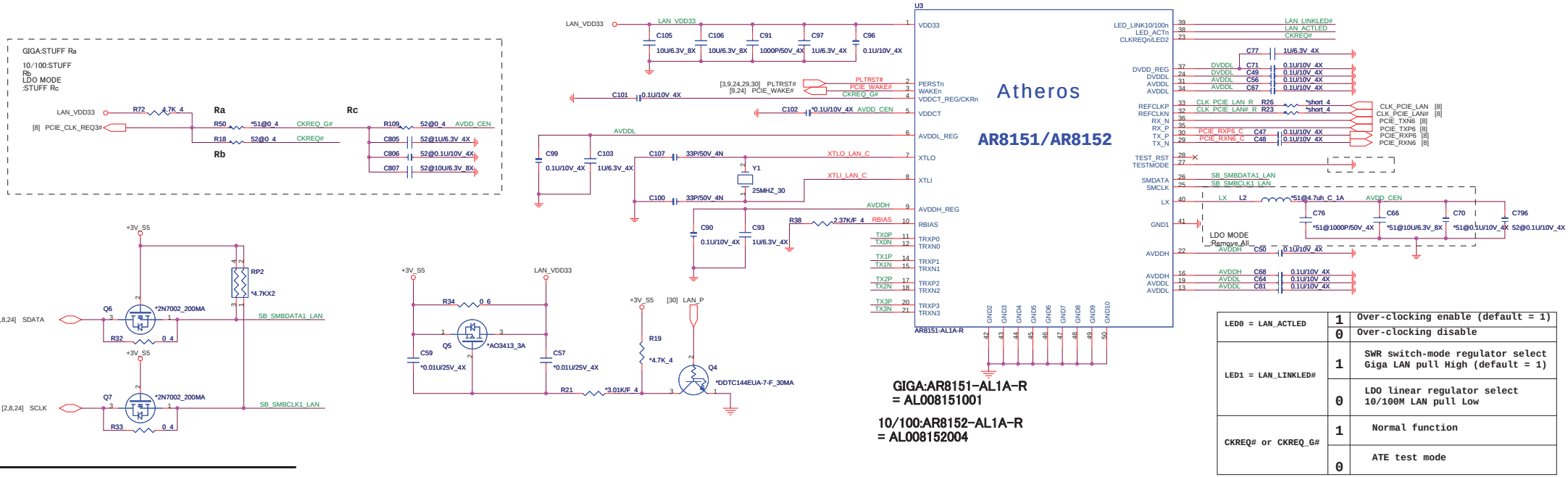
MDC



Quanta Computer Inc.
PROJECT : TE2

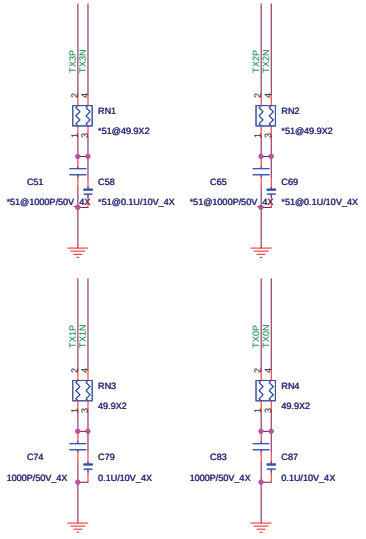
Size	Document Number	Rev
	Codec (CX20583)	2A
Date: Friday, March 19, 2010	Sheet 27 of 45	

Atheros Lan

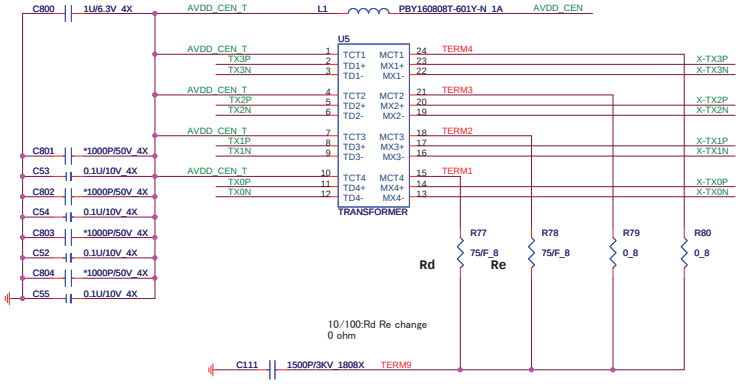


LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

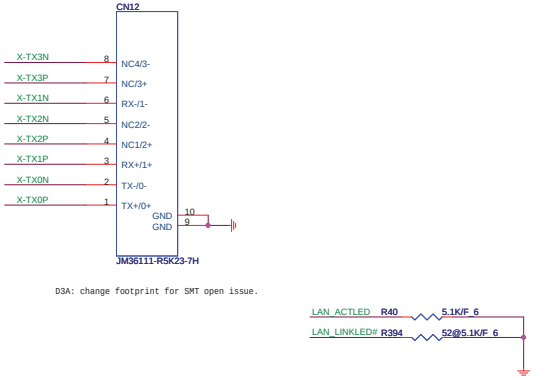
PLACE NEAR LAN IC SIDE



TRANSFORMER

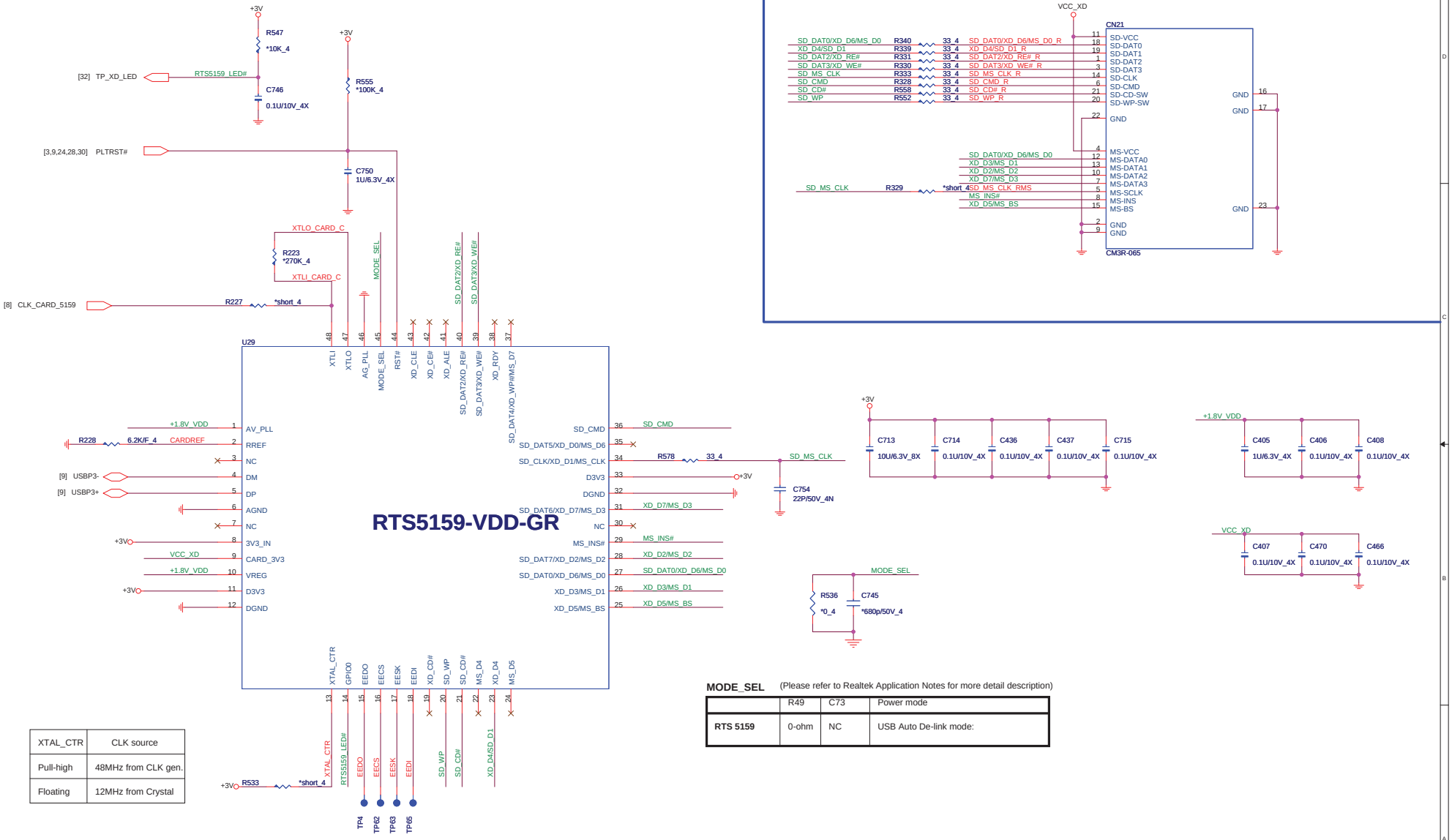


RJ45



Quanta Computer Inc.			
PROJECT : TE2			
Size	Document Number		Rev
	Atheros Lan		2A
Date:	Wednesday, March 10, 2010	Sheet 28 of 45	

3 IN 1 CARD READER



XTAL_CTR	CLK source
Pull-high	48MHz from CLK gen.
Floating	12MHz from Crystal

MODE_SEL (Please refer to Realtek Application Notes for more detail description)

	R49	C73	Power mode
RTS 5159	0-ohm	NC	USB Auto De-link mode:

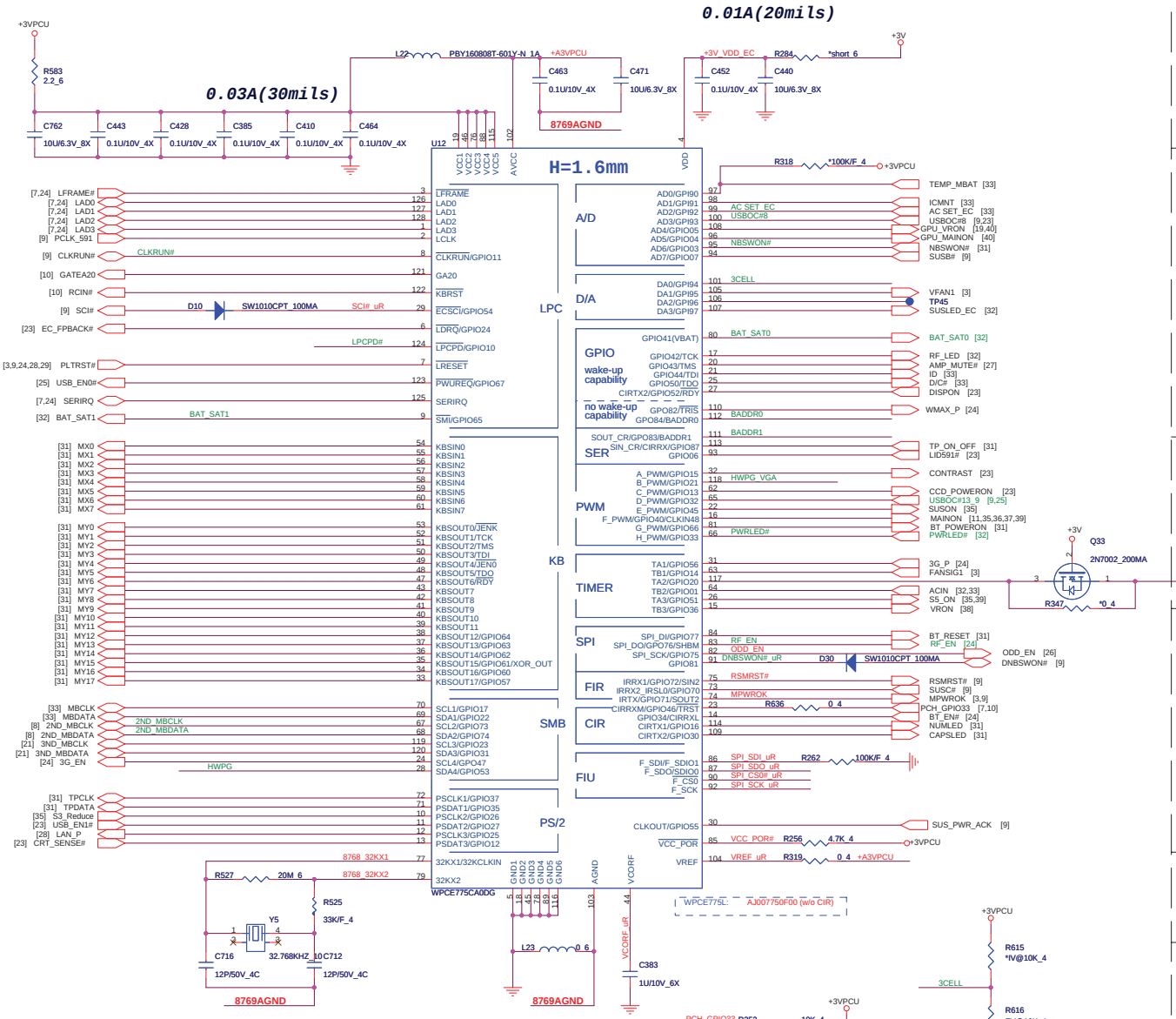
3 IN 1 CARD READER

Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	RTS5159 (Card Reader)	2A

Date: Tuesday, March 09, 2010 Sheet 29 of 45

EC [KBC]



SMBUS Table

SMBUS	Devices	Address
1	Battery	12H
2	CPU Board Thermal Sensor	98H
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H

SM BUS PU

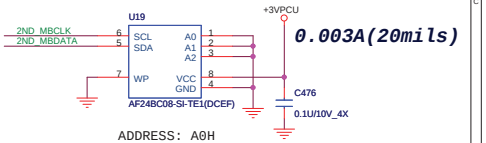
I/O Base Address

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

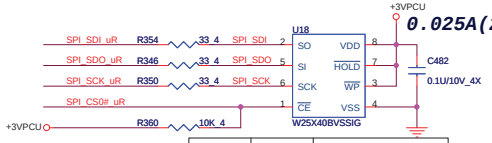
SHBM=0: Enable shared memory with host BIOS

Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

ID

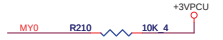


SPI FLASH

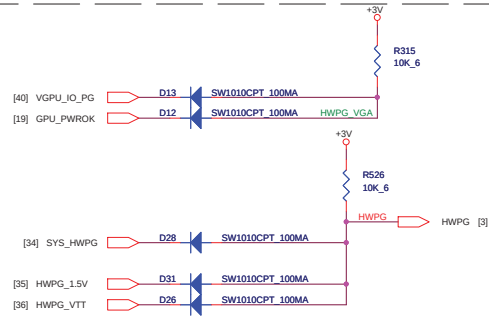


Intel	512KB	W25X40BVSSIG
AMD	2MB	W25Q16BVSSIG

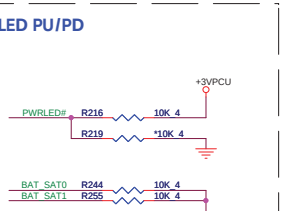
INTERNAL KEYBOARD STRIP SET



HWPG



LED PU/PD

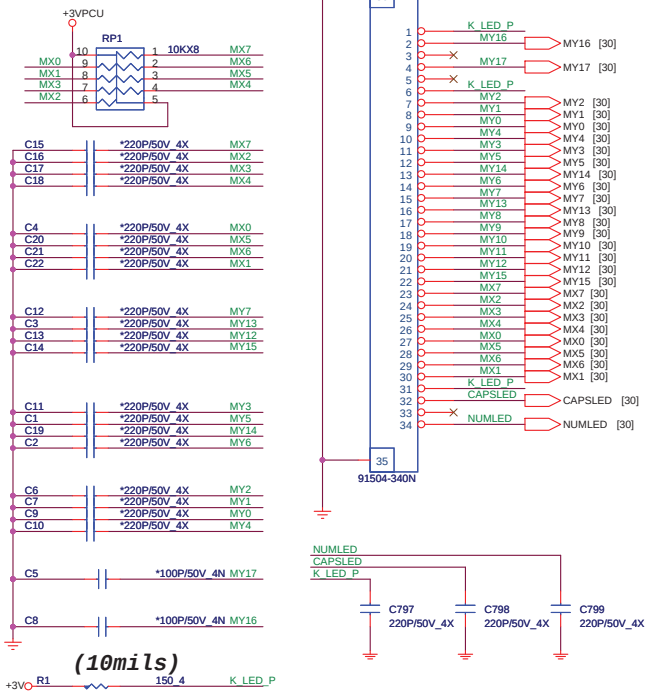


Quanta Computer Inc.
PROJECT : TE2

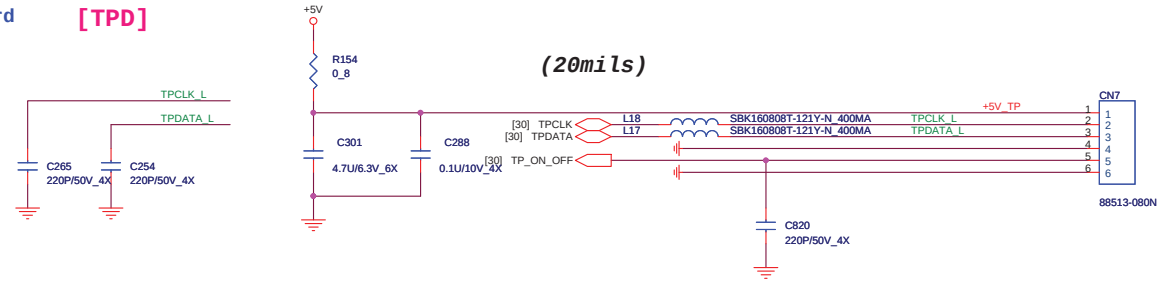
Size	Document Number	Rev
	EC-WPC8763LDG/WPC8769L(O)	2A

Date: Wednesday, March 10, 2010 Sheet 30 of 45

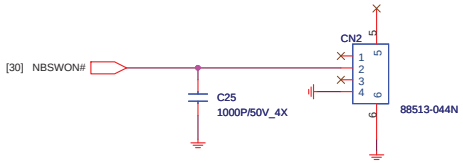
INT KeyBoard [KBC]



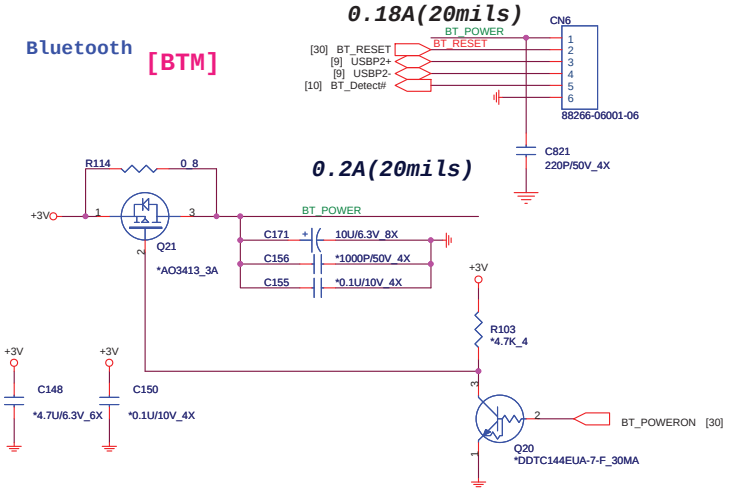
TP board [TPD]



Power board [PSW]

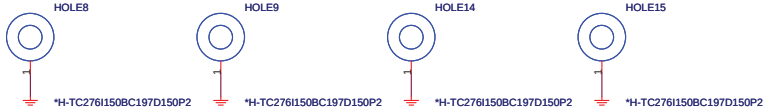


Bluetooth [BTM]

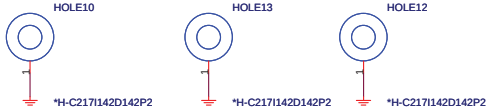


HOLE

CPU

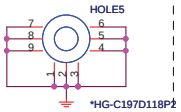


VGA

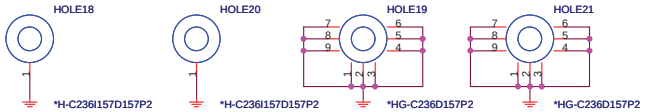


HDD&ODD

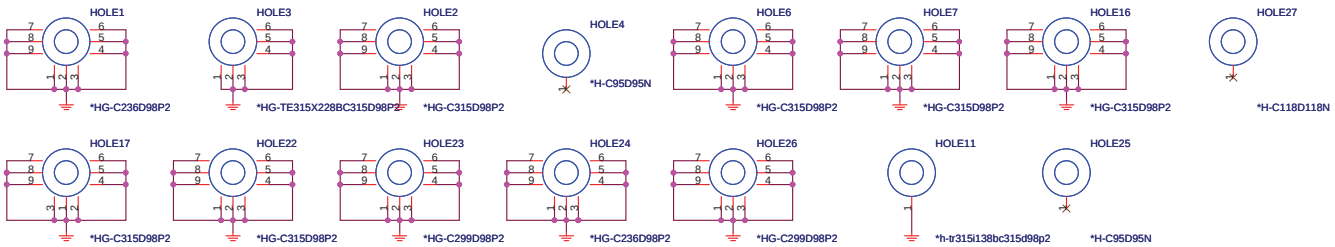
MDC



MINI CARD



EMI PAD



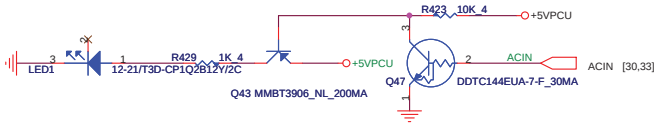
Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	KB/TP&TP/PB/FL/LEB/MMB/B-CAS	2A

Date: Wednesday, March 10, 2010 Sheet 31 of 45

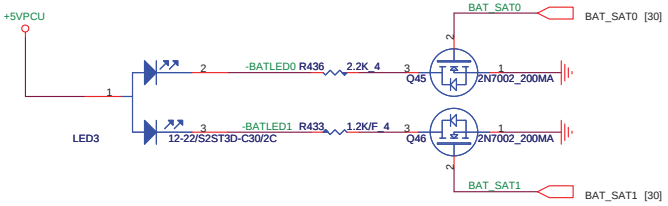
LED [LED]

AC-IN



BATERRY

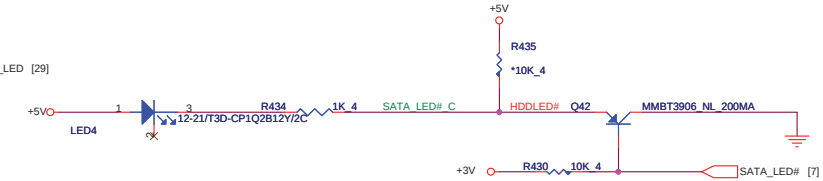
D3A : LED luminance to light,1K-ohm change 2.2K-ohm.



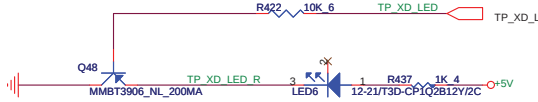
RF LED

D3A : LED luminance to light,560-ohm change 220-ohm.

HDD/ODD

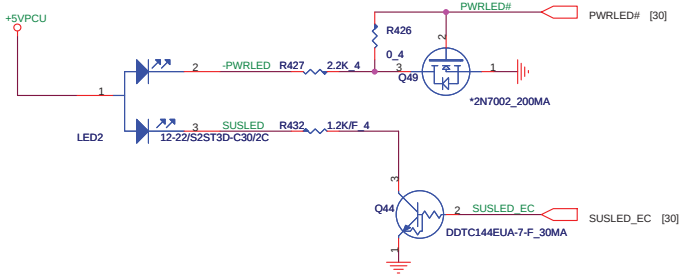


CARDREADER

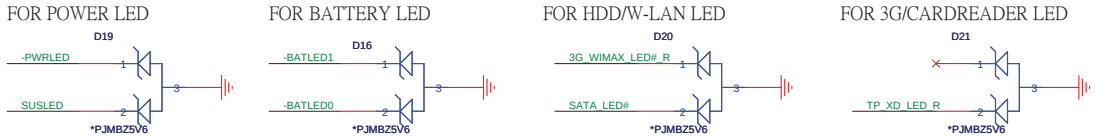


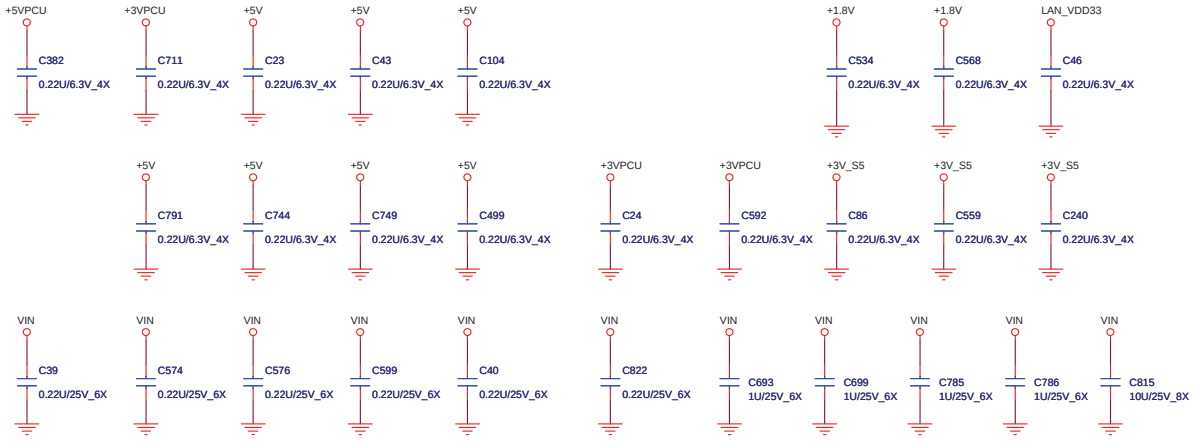
POWER

D3A : LED luminance to light,1K-ohm change 2.2K-ohm.

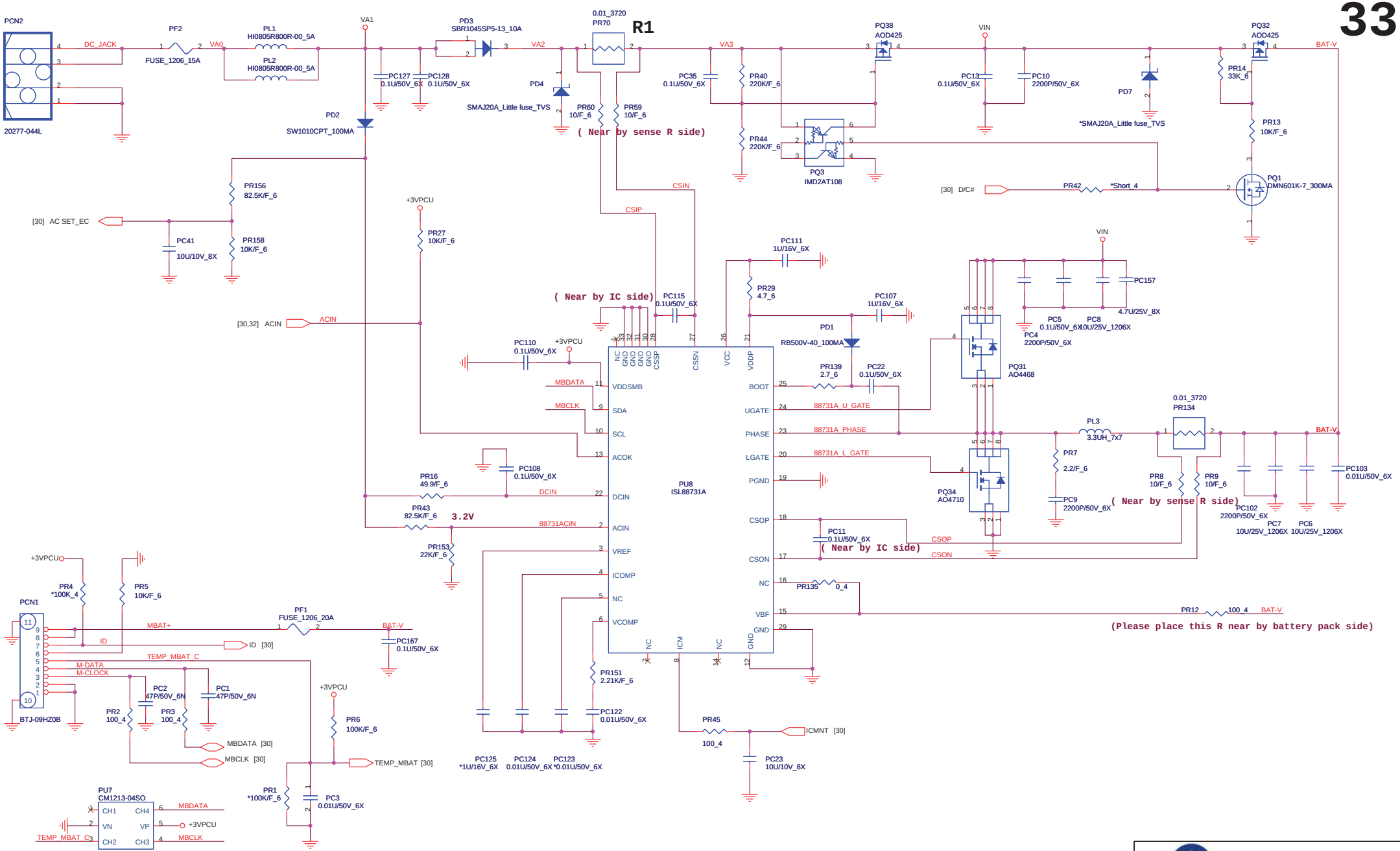


ESD Protect





Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number LED/HOLE	Rev 2A
Date: Tuesday, March 09, 2010	Sheet 32 of 45	



Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: Charger (ISL88731)	Rev: 1A
Date: Wednesday, March 10, 2010	Sheet 33 of 43	

For RT8210B or UP6184 0_4 & 10K_4

For ISL6237 ZD5.6V , 100K/F_4 & 200K/F_4

09/10/15

f : 400k Hz
ESR : 17mΩ
Total capacitor : 370 uF
(Peak 10.2 ,AVG 8.135A)
OCP:11A

f : 500k Hz
ESR : 17mΩ
Total capacitor : 342uF
(Peak 9A, AVG 7.623A)
OCP:11.055~11.345A

OCP:11.12~11.9525A
AO4710 Rdson=14.2mOhm.max.
△I=[(Vin-Vout)*Vout]/Vin*L*f
Iocp=OCP-(△I/2)
Vth*10=R(Ilim)*5uA
So,R(Ilim) use 2870 ==>
Vin=19V OCP=11.9525A ,
Vin=9V OCP=11.12A

OCP:11.055~11.345A
AO4710 Rdson=14.2mOhm.max.
△I=[(Vin-Vout)*Vout]/Vin*L*f
Iocp=OCP-(△I/2)
Vth*10=R(Ilim)*5uA
So,R(Ilim) use 287K ==>
Vin=19V OCP=11.345A ,
Vin=9V OCP=11.055A

F=500K
Rilim=Ilim*LRdson*10/5uA

11A

2.834A

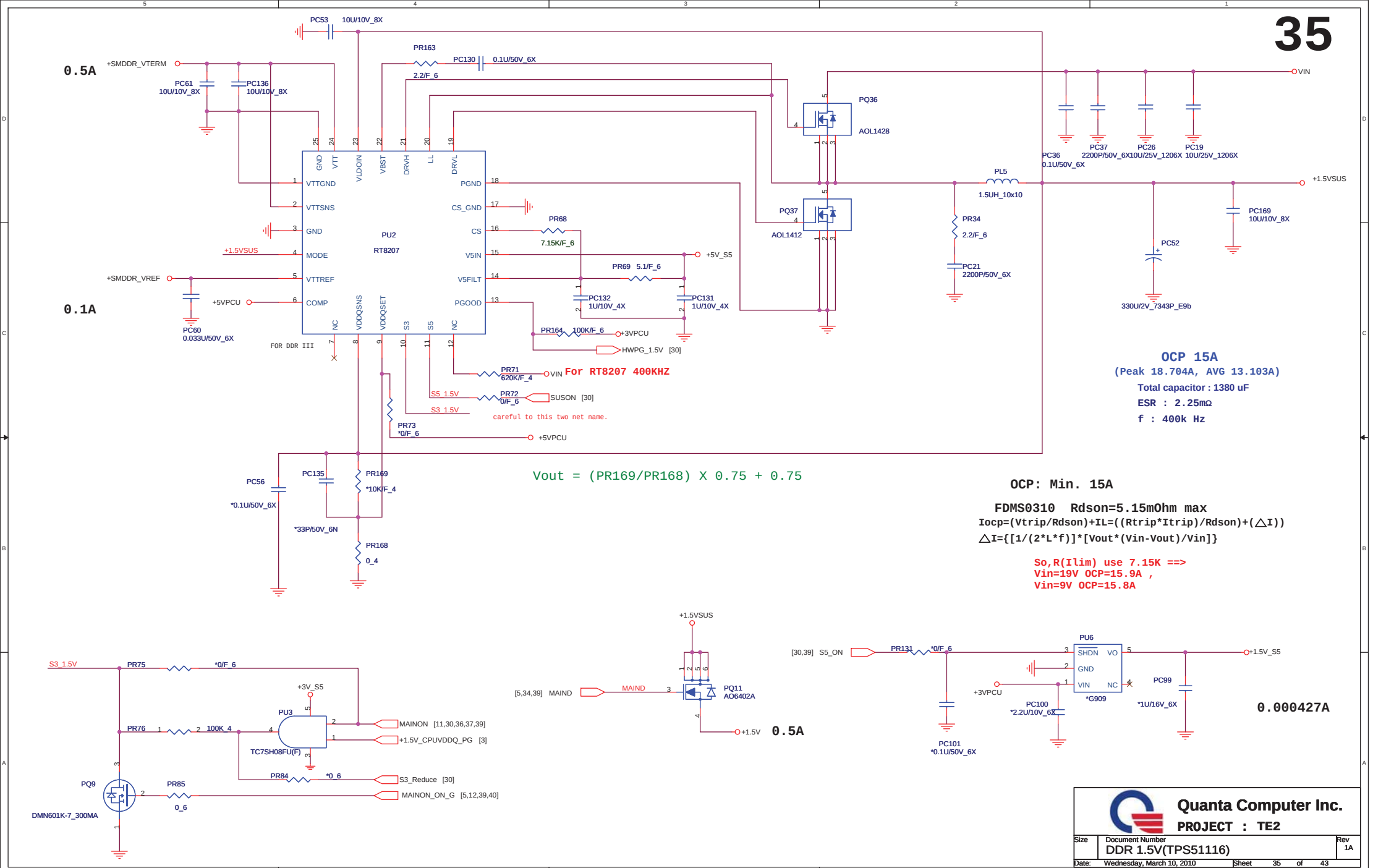
4.523A

4.984A

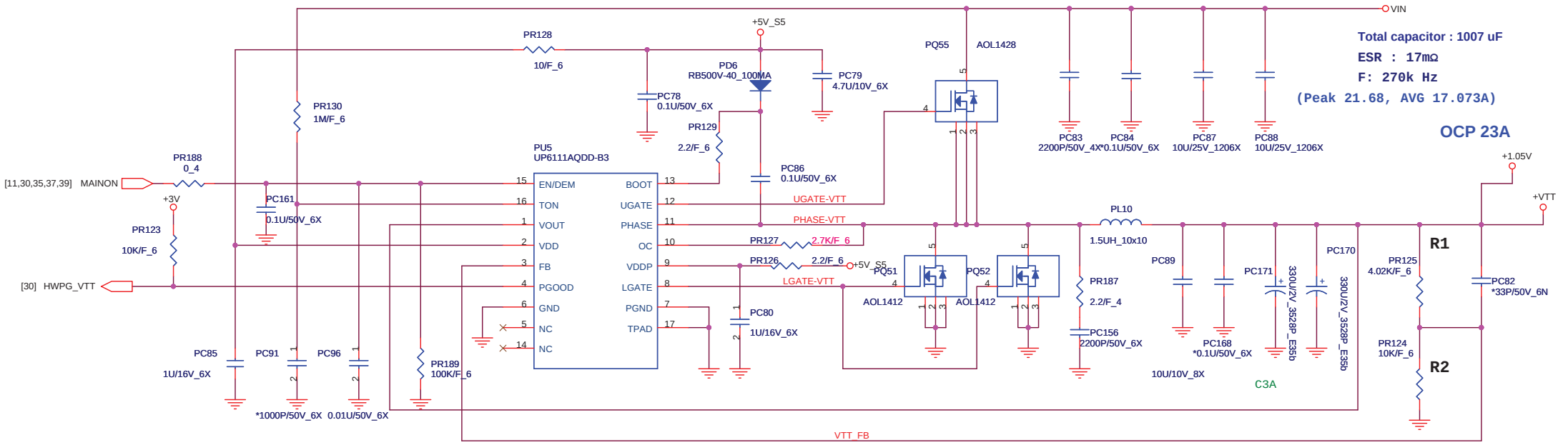
0.001A

Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	System 3V/5V(RT8210B)	1A
Date: Wednesday, March 10, 2010	Sheet 34 of 43	



Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: DDR 1.5V(TPS51116)	Rev: 1A
Date: Wednesday, March 10, 2010	Sheet 35 of 43	



VOUT=(1+R1/R2)*0.75

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

OCP:23.18~23.27A

FDMS0310 Rdson=5.15mOhm max

Iocp=(Vtrip/Rdson)+IL=((Rtrip*Itrip)/Rdson)+(△I))

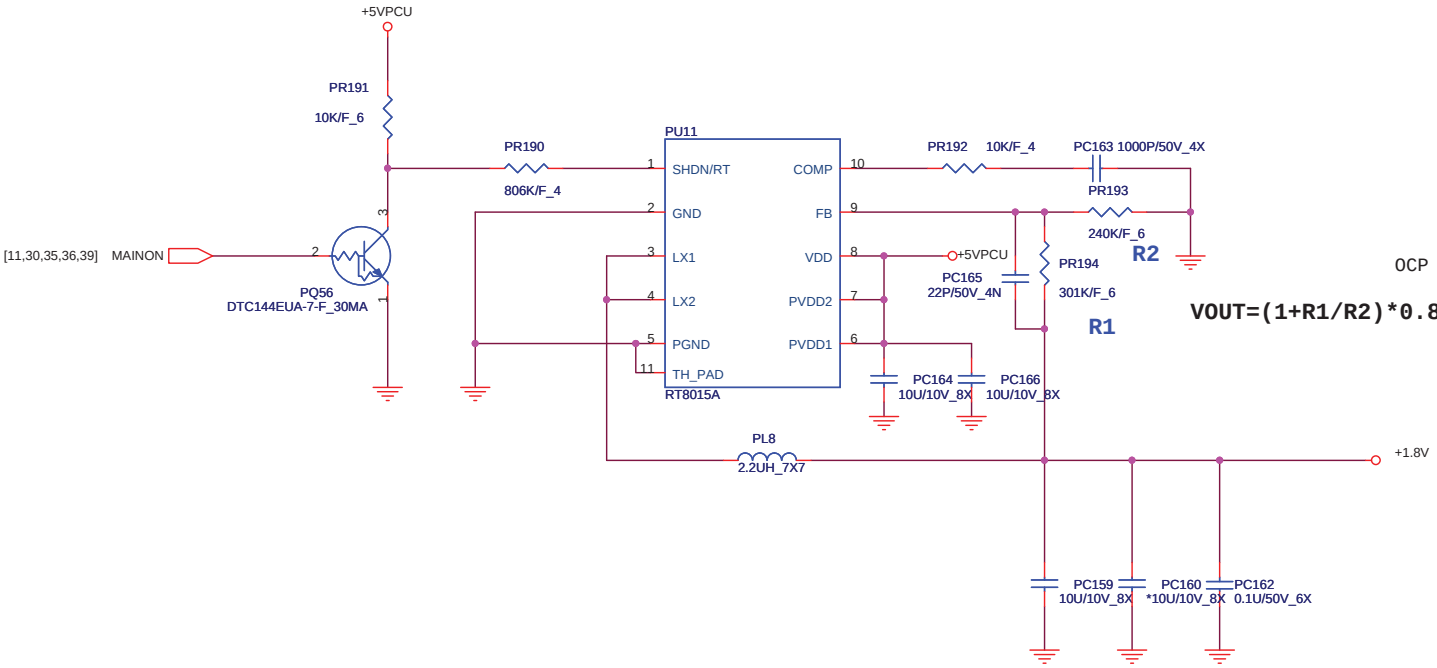
△I={[1/(2*L*f)]*[Vout*(Vin-Vout)/Vin]}

Rdson*OCP=RIlim*20uA

So,R(Ilim) use 2.7K ==>
Vin=19V OCP=23.18A ,
Vin=9V OCP=23.27A

Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	+VTT (UP6111A)	1A
Date: Wednesday, March 10, 2010	Sheet 36 of 43	

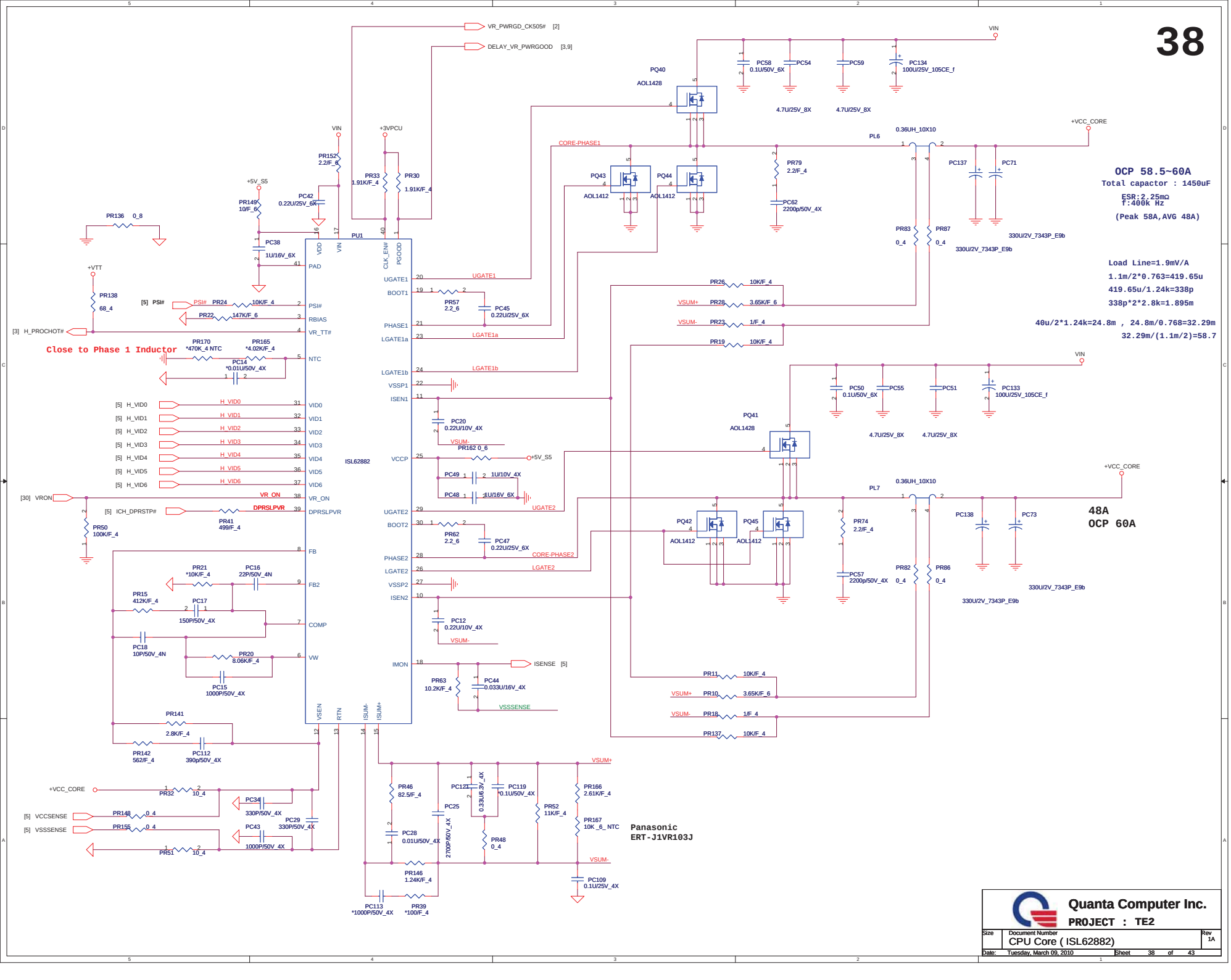


OCP Fellow IC spec~3.7A

VOUT=(1+R1/R2)*0.8

FOR UMA 0.194A
For VGA 1.345A

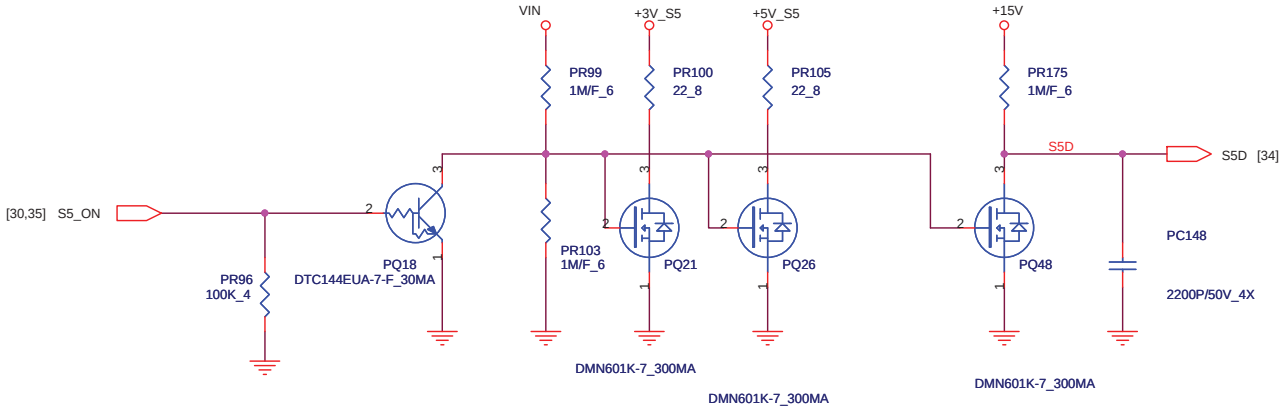
Quanta Computer Inc.		
PROJECT : TE2		
Size	Document Number: +1.8V (RT8015A)	Rev: 1A
Date: Wednesday, March 10, 2010	Sheet 37 of 43	

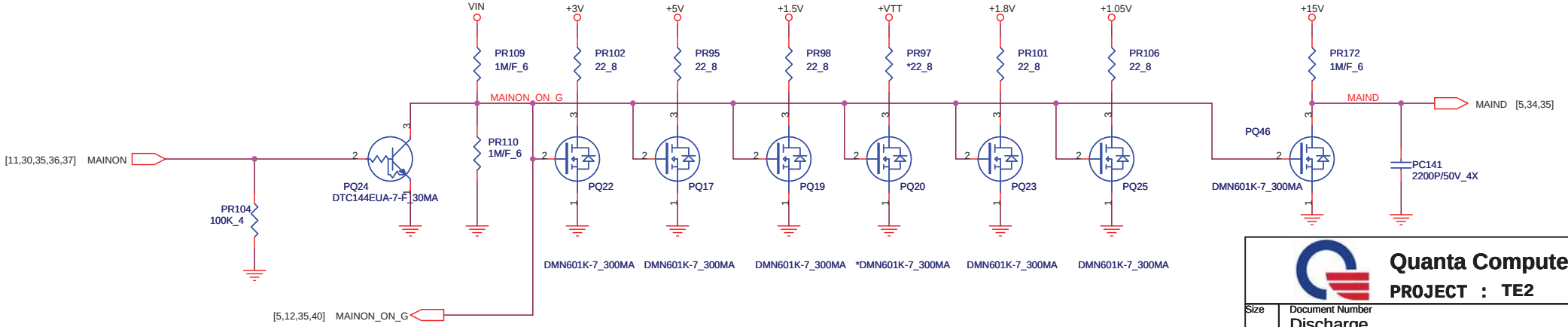


Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	CPU Core (ISL62882)	1A

Date: Tuesday, March 09, 2010 Sheet 38 of 43



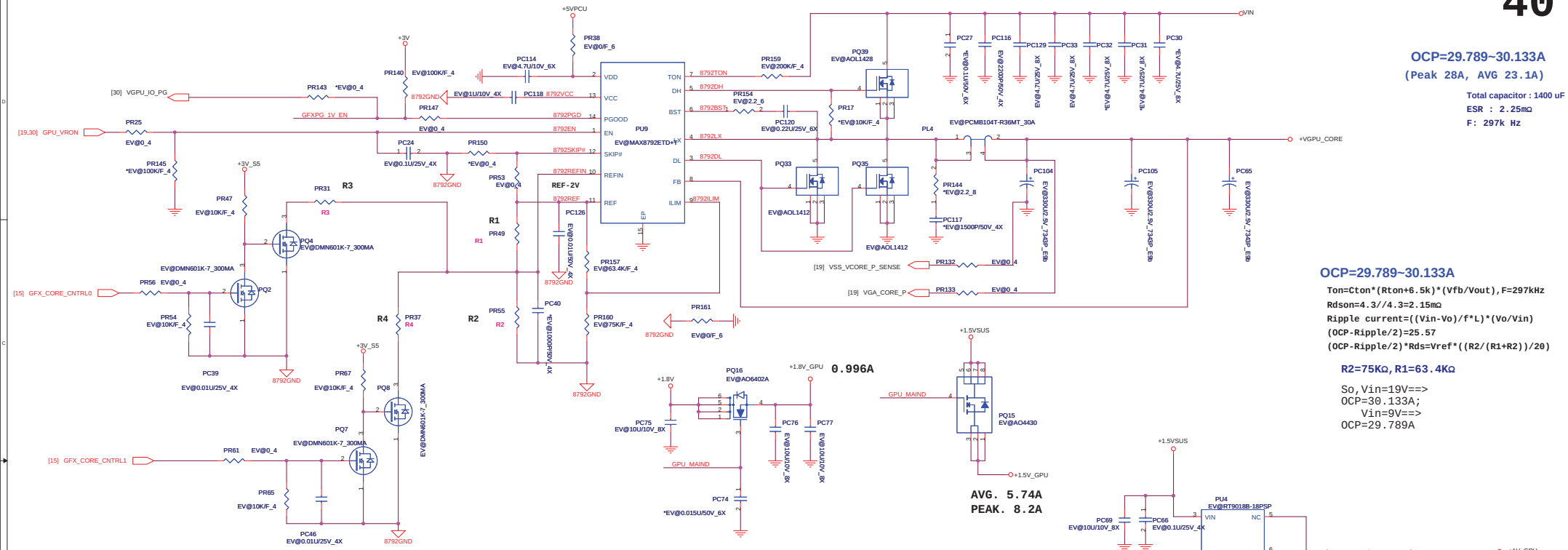


Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	Discharge	1A

Date: Thursday, February 25, 2010 Sheet 39 of 43



OCP=29.789~30.133A
(Peak 28A, AVG 23.1A)

Total capacitor : 1400 uF
ESR : 2.25mΩ
F: 297k Hz

OCP=29.789~30.133A
Ton=Ctop*(Rton+6.5k)*(Vfb/Vout),F=297kHz
Rdson=4.3//4.3=2.15mΩ
Ripple current=((Vin-Vo)/f*L)*(Vo/Vin)
(OCP-Ripple/2)=25.57
(OCP-Ripple/2)*Rds=Vref*((R2/(R1+R2))/20)

R2=75KΩ, R1=63.4KΩ

So,Vin=19V==>
OCP=30.133A;
Vin=9V==>
OCP=29.789A

GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	Madison/Park	M92	M96
LOW	LOW	0.9V	0.9V	0.95V
HIGH	LOW	0.95V	0.95V	0.95V
LOW	HIGH	1.12V	1.1V	1.0V
HIGH	HIGH	N/A	1.2V	1.1V

		Madison/Park	M92	M96
R1	PR49	39.2K CS33922FB15	39.2K CS33922FB15	39.2K CS33922FB15
R2	PR55	60.4K CS36042FB10	60.4K CS36042FB10	49.9K CS34992FB10
R3	PR31	309K CS43092FB16	270K CS42702FB10	249K CS42492FB18
R4	PR37	88.7K CS38872FB18	93.1K CS39312FB15	140K CS41402FB14

PCIE_VDDC
M92,M96-->1.1V
Madison,Park-->1.0V

	Madison,Park	M92,M96
PR91	25.5K/F_4 (CS32552FB11)	39.2K/F_4 (CS33922FB15)
PR89	100K/F_4 (CS41002FB28)	100K/F_4 (CS41002FB28)

Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	+VGPU_CORE(MAX8792)	1A

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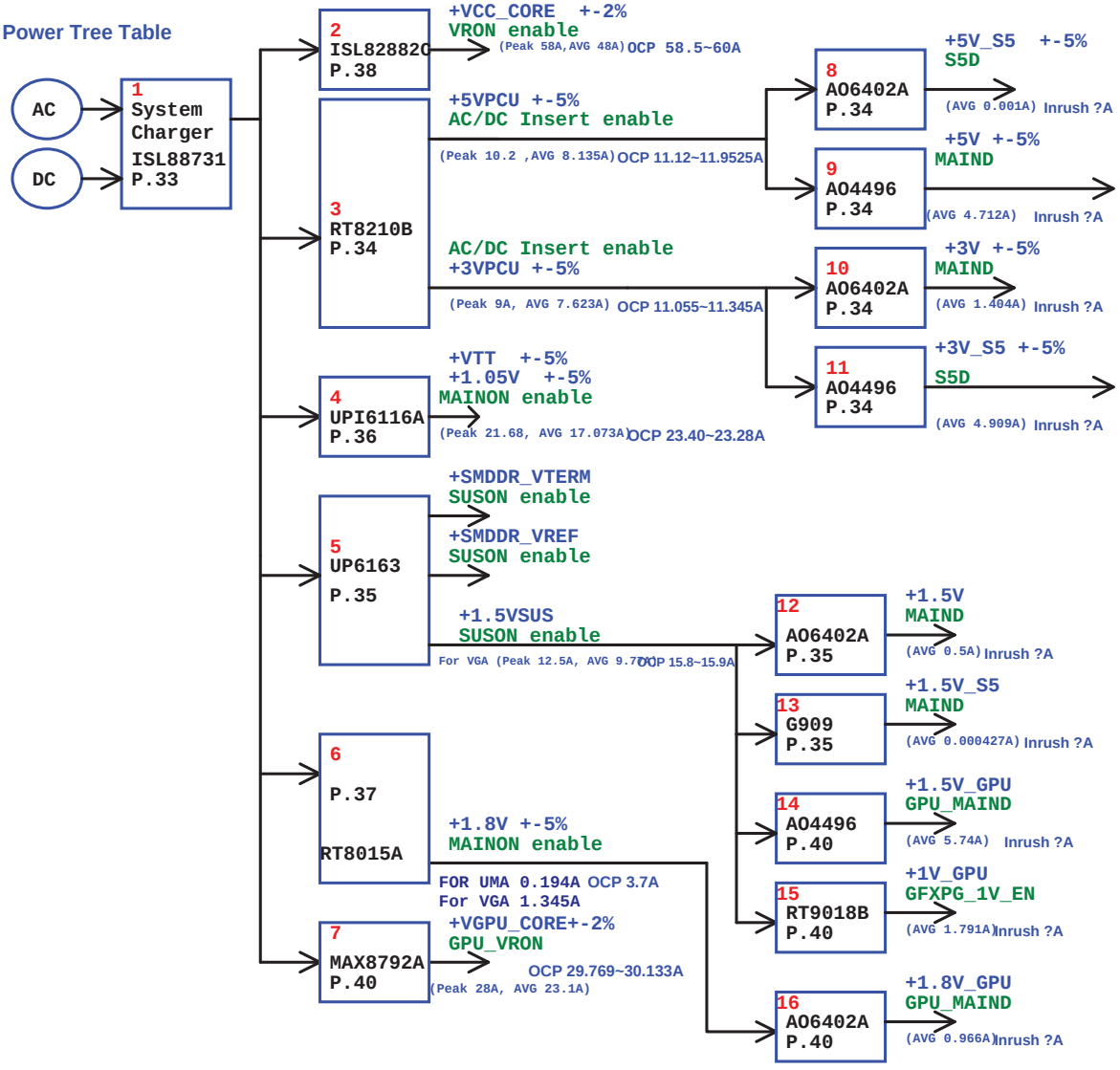
Power Tree Table



Power Distribution List

Power	Distribution

Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	Power Tree Table	2A

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Table of Contents

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
+5V_TMA	+5V	MAIN_ON	S0
WIMAX_P	+3.3V	WMAX_P for EC	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_S5	+1.5V	S5_ON	S0~S5
+1.5V_SUS	+1.5V	SUSON	S0~S3
+VCC_CORE		VRON	S0
+VTT	+1.05V~+1.1V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		GFXVR_EN	S0

GND PLANE	PAGE
GND_SIGNAL	32
CARD_GND	21
AGND_DC/DC	31
GND	ALL

Quanta Computer Inc.

PROJECT : TE2

Size	Document Number	Rev
	POWER STAGE AND BOI-FUNCTION	2A

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Model	REV	CHANGE LIST
TE2D MB	B2A	PAGE (16) : Add BT_EN# for combo RF control for BT PAGE (27) : Change DDR S3_1.5V ON circuit.
	C3A	PAGE (07) : Add ESATA re-driver IC
	D3A	PAGE(32) : LED luminance to light,R436、R427 1K-ohm change 2.2K-ohm. PAGE(32) : LED luminance too low,R428 560-ohm change 220-ohm. PAGE(27) : Add R230,R231,R286,R287 0.1-ohm to avoid speaker burn. PAGE(16):Add Q62 to avoid leakage current.

MODEL: TE2

PAGE	FROM	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	
16	1A	
17	1A	
18	1A	
19	1A	
20	1A	
21	1A	
22	1A	
23	1A	
24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	

DOC NO. 204					
PROJECT MODEL :	TE2	APPROVED BY:	Mosy Li	DATE:	2009/10/27
PART NUMBER:		DRAWING BY:	Mosy Li	REVISON:	1A

Quanta Computer Inc.
PROJECT : TE2
Size | Document Number: Change list | Rev: 2A
Date: Friday, March 19, 2010 | Sheet 31 of 33