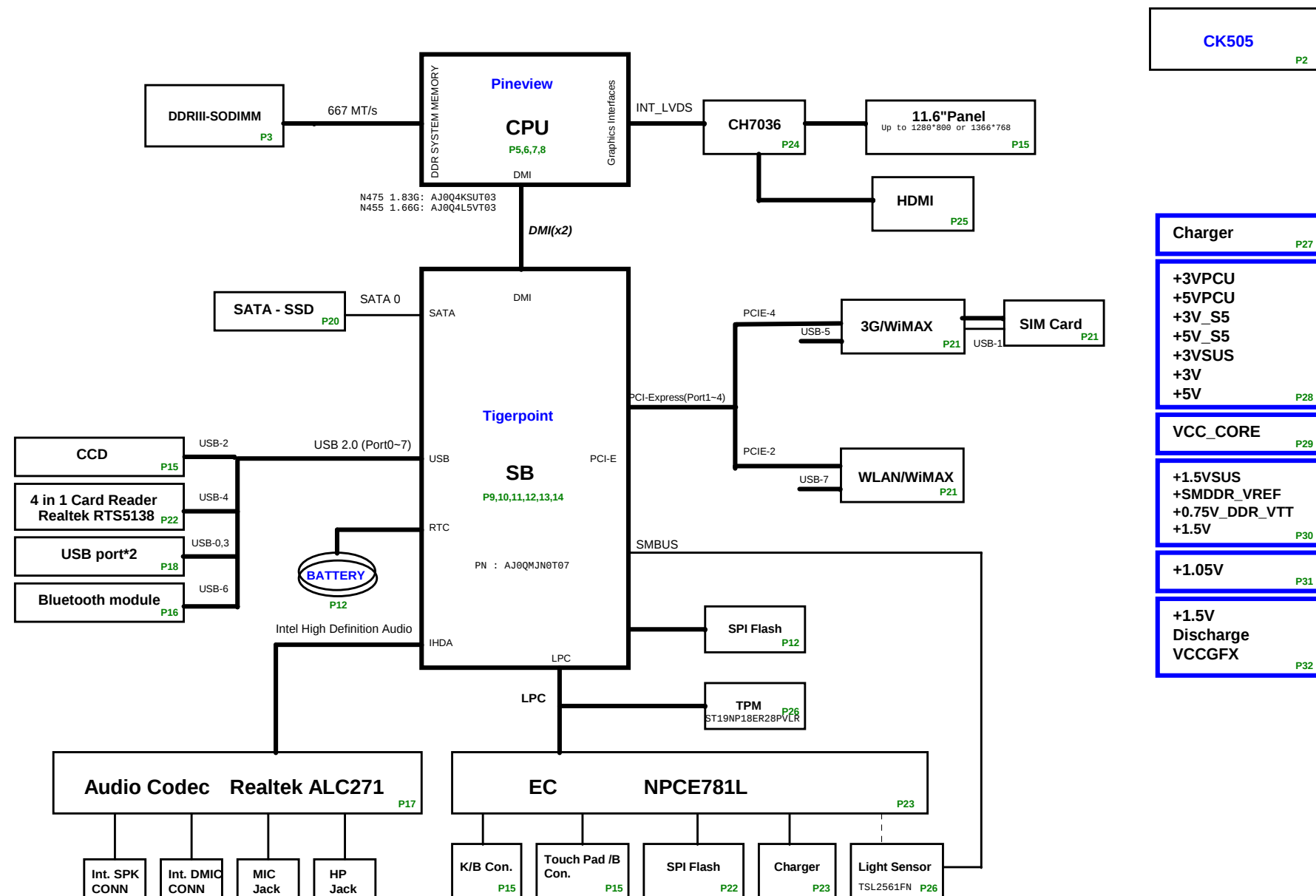


ZGA Block Diagram



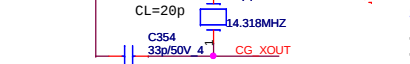
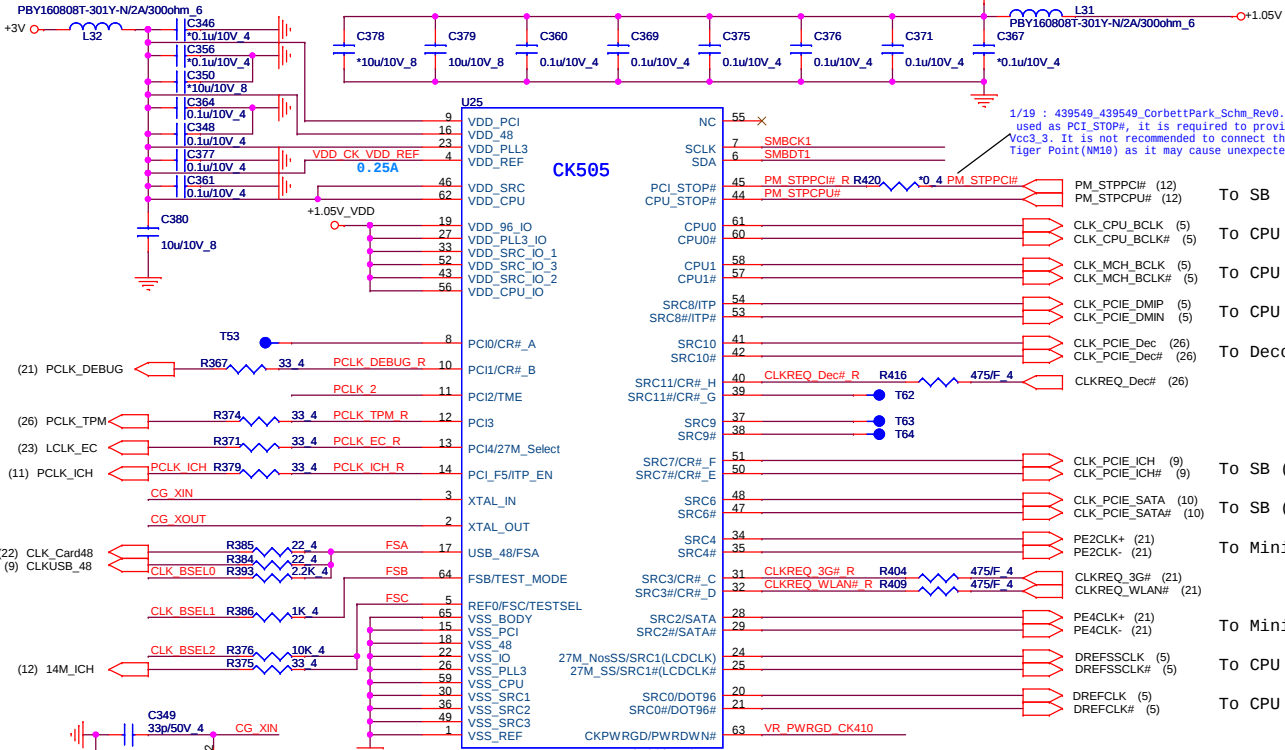
Clock Generator(CLK)

The Beads for power 3.3V/1.05 are for EMI solution.
It is recommended to add it for better power/EMI performance.

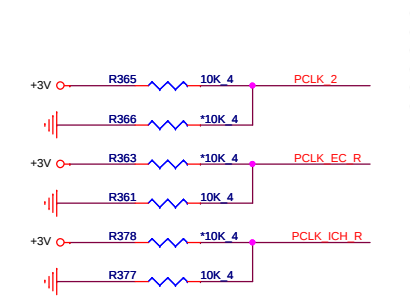
0.08A

+1.05V_VDD

02



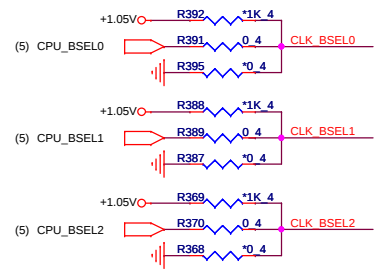
<Layout note>
Crystal place within 500mil of CK505



	SLG8SP513VTR (AL8SP513000)	ICS9LPRS365 (ALPRS365000)	PULL HIGH	PULL DOWN
Pin 11	PCI2	PCI2/TME	NO OVERCLOCKING (default)	NORMAL RUN
Pin 13	PCI4/ SEL_LCDCLK#	PCI4/ 27_Select	PIN 20/21 IS SRC0 PIN 24/25 IS 27MHz	PIN 20/21 IS DOT96 (default) PIN 24/25 IS LCDCLK
Pin 14	PCIF5/ITP_EN	PCIF5/ITP_EN	PIN 53/54 IS CPUITP	PIN 53/54 IS SRC8 (default)

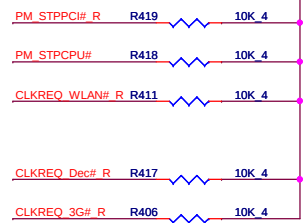
SLG8SP513VTR, ICS9LPRS365BKLFT
<MAIN> : SLG8SP513VTR(AL8SP513000)
<SECOND> : ICS9LPRS3165BKLFT(AL003165000)
<SECOND> : ICS9LPRS365BKLFT(ALPRS365000)

CLKREQA# CONTROL SRC0(default) or SRC2
CLKREQB# CONTROL SRC1(default) or SRC4
CLKREQC# CONTROL SRC2
CLKREQD# CONTROL SRC4
CLKREQE# CONTROL SRC6
CLKREQF# CONTROL SRC8
CLKREQG# CONTROL SRC9
CLKREQH# CONTROL SRC10

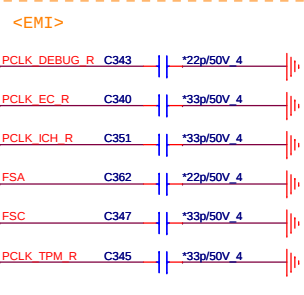


FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF	USB	DOT
0	0	0	266.66	100	33.33	14.318	48	96
0	0	1	133.33	100	33.33	14.318	48	96
0	1	0	200.00	100	33.33	14.318	48	96
0	1	1	166.66	100	33.33	14.318	48	96
1	0	0	333.33	100	33.33	14.318	48	96
1	0	1	100.00	100	33.33	14.318	48	96
1	1	0	400.00	100	33.33	14.318	48	96
1	1	1						
RESERVED								

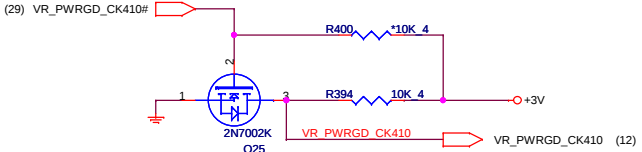
<20090721(B2A)_Intel MW MW28,2009>
Stuff R56,R60 to solve system maybe boot failure issue



<20090527(A1A)_Silago suggestion>
The EMI capacitor should be placed
between pin and series resistor for
good EMI and SI

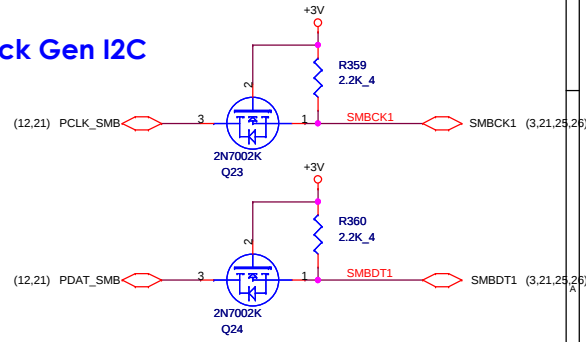


VR PWRGD



<20090721(B2A)>
Change Q3,Q5,Q6 from BAH700200F6 to BAH700200E2 (with ESD protection function)

Clock Gen I2C

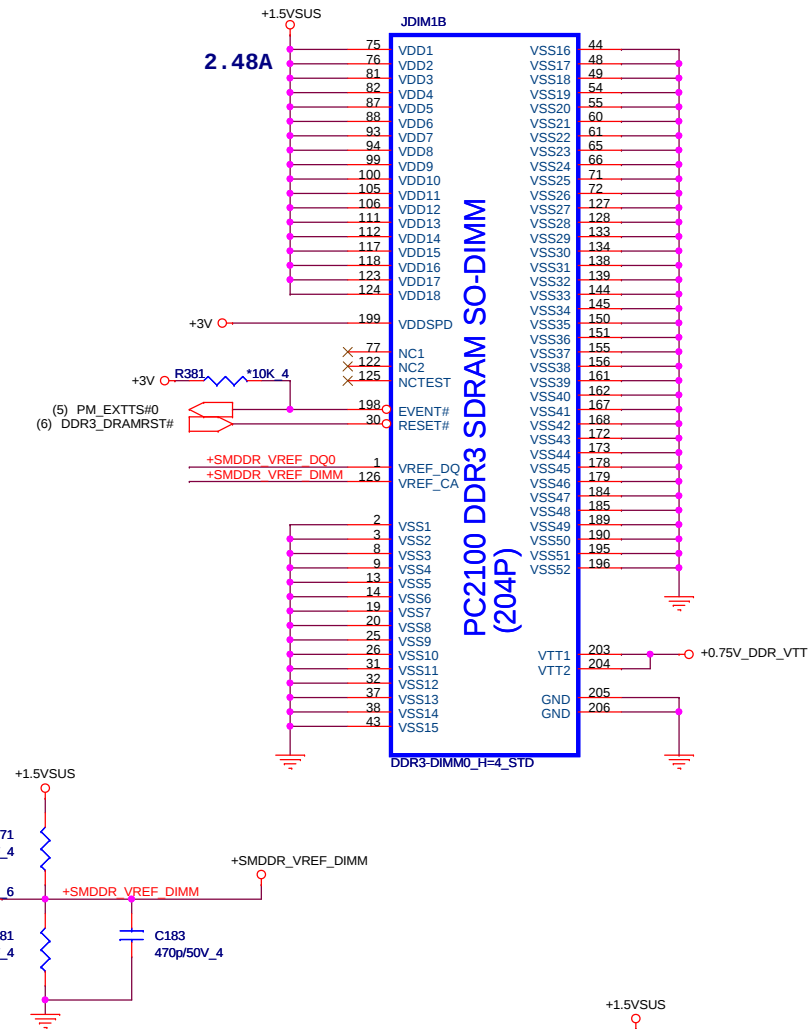
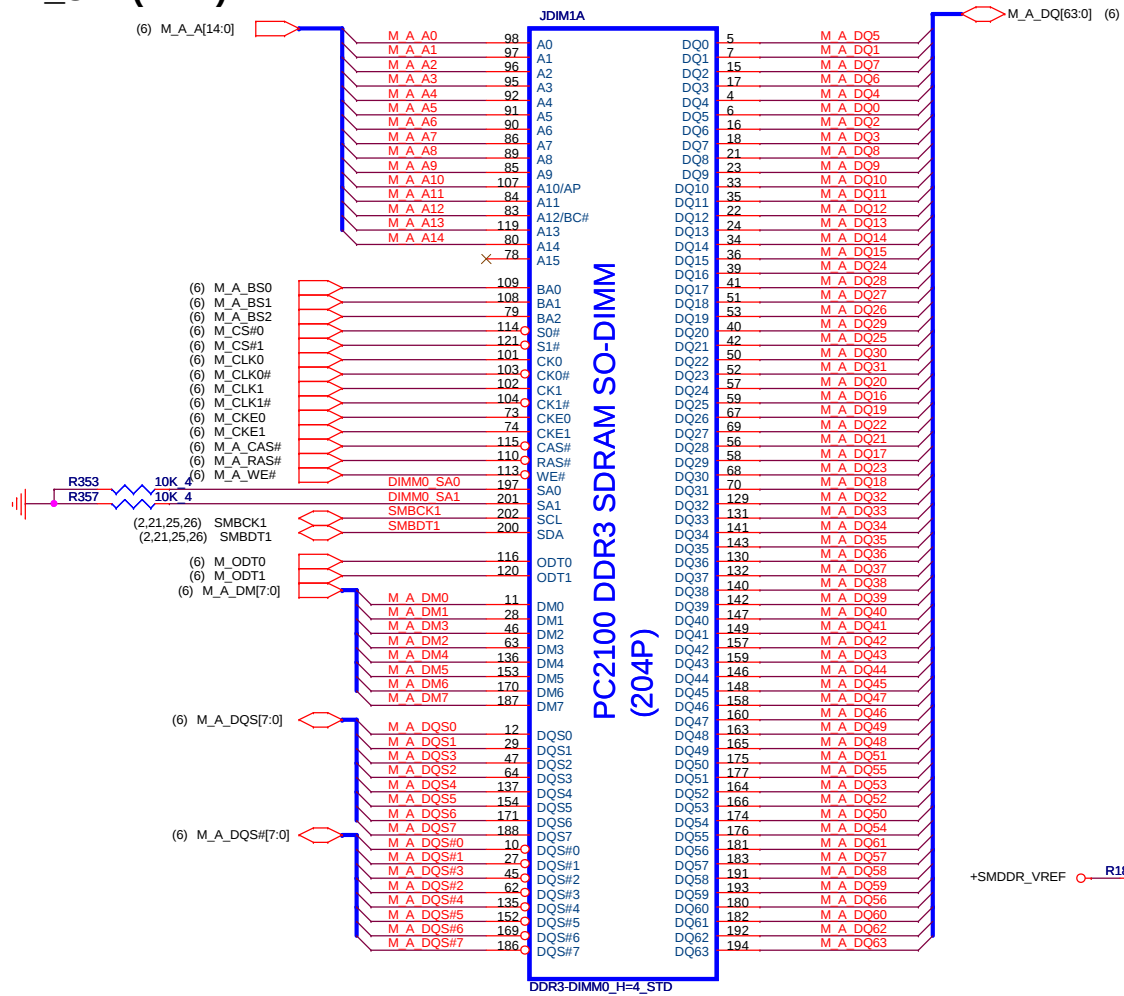


Quanta Computer Inc.
PROJECT : Z6A

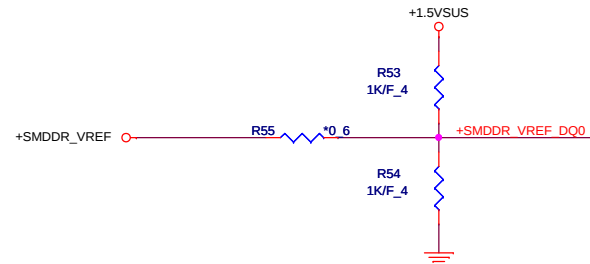
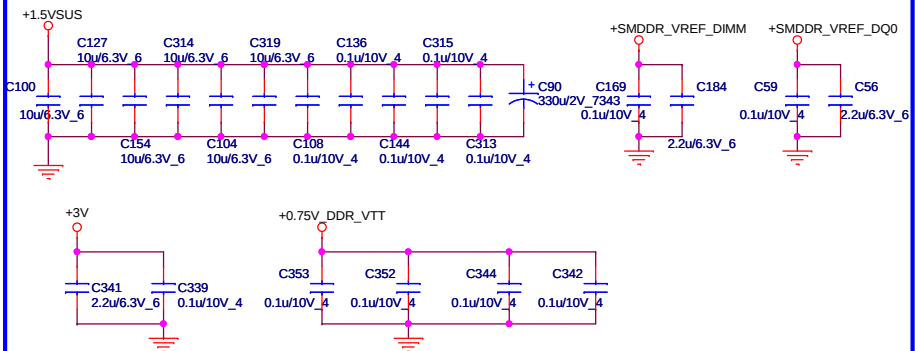
Size Document Number
CLOCK GENERATOR
Date: Wednesday, July 07, 2010 Sheet 2 of 38

Rev
1B

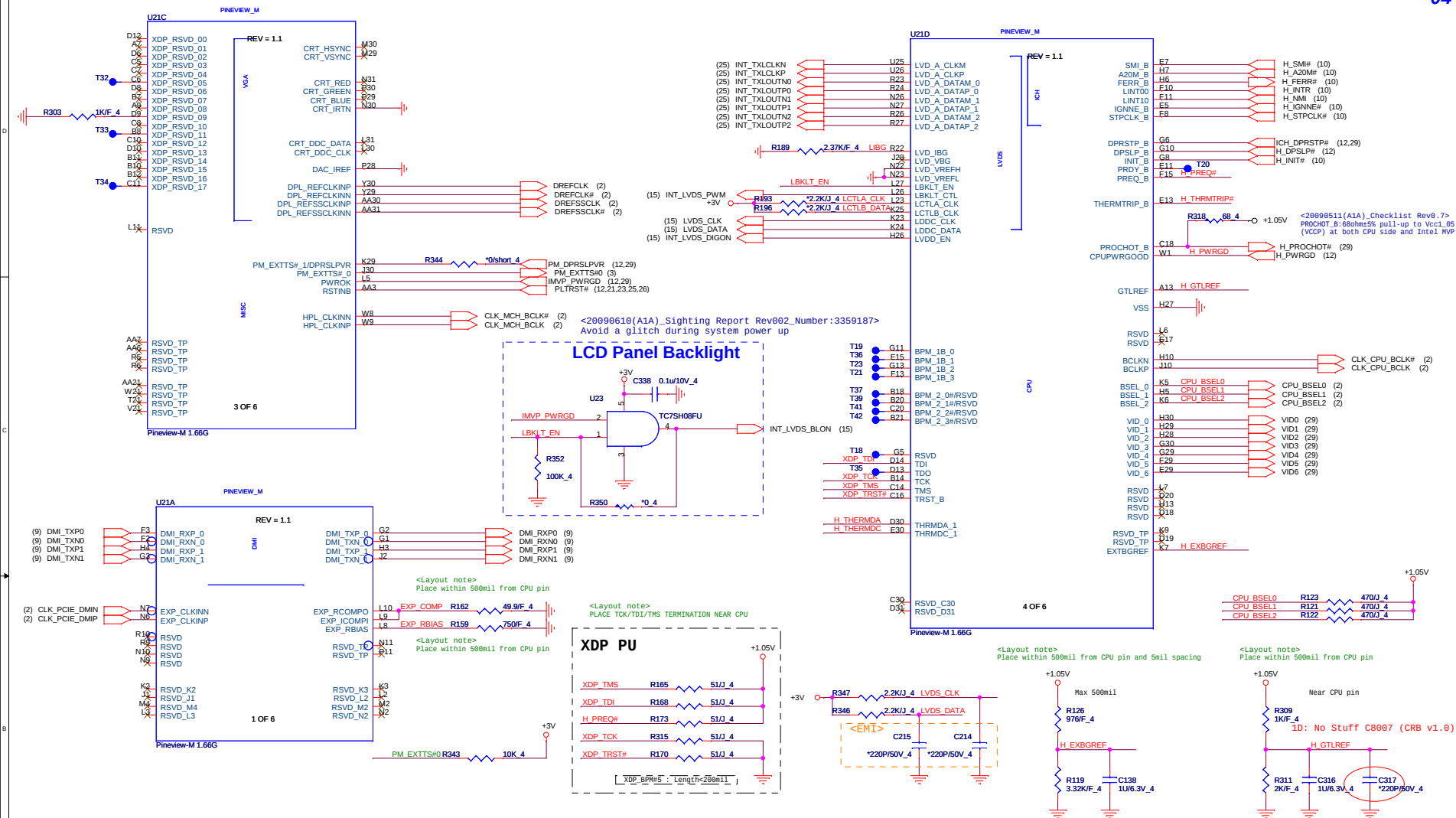
DDR_STD(DDR)



Place these Caps near So-Dimm0.

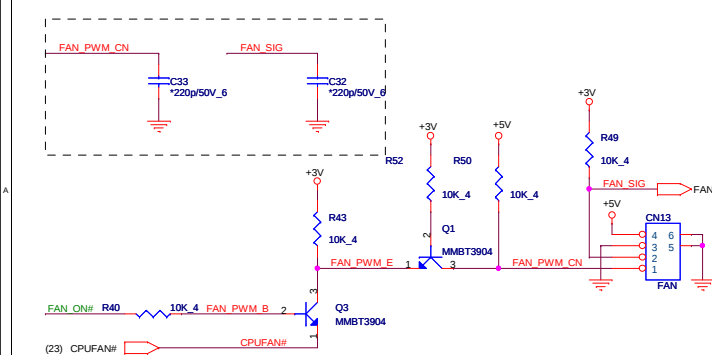


	5	4	3	2	1
D					
C					
B					
A					

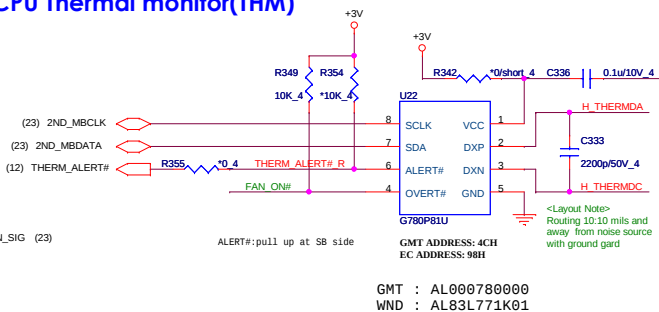


CPU FAN CTRL(THM)

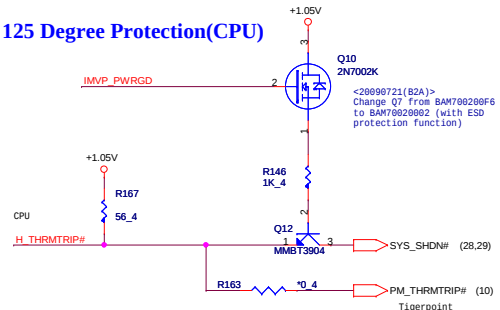
8/11 B-test : for EMI



CPU Thermal monitor(THM)



125 Degree Protection(CPU)





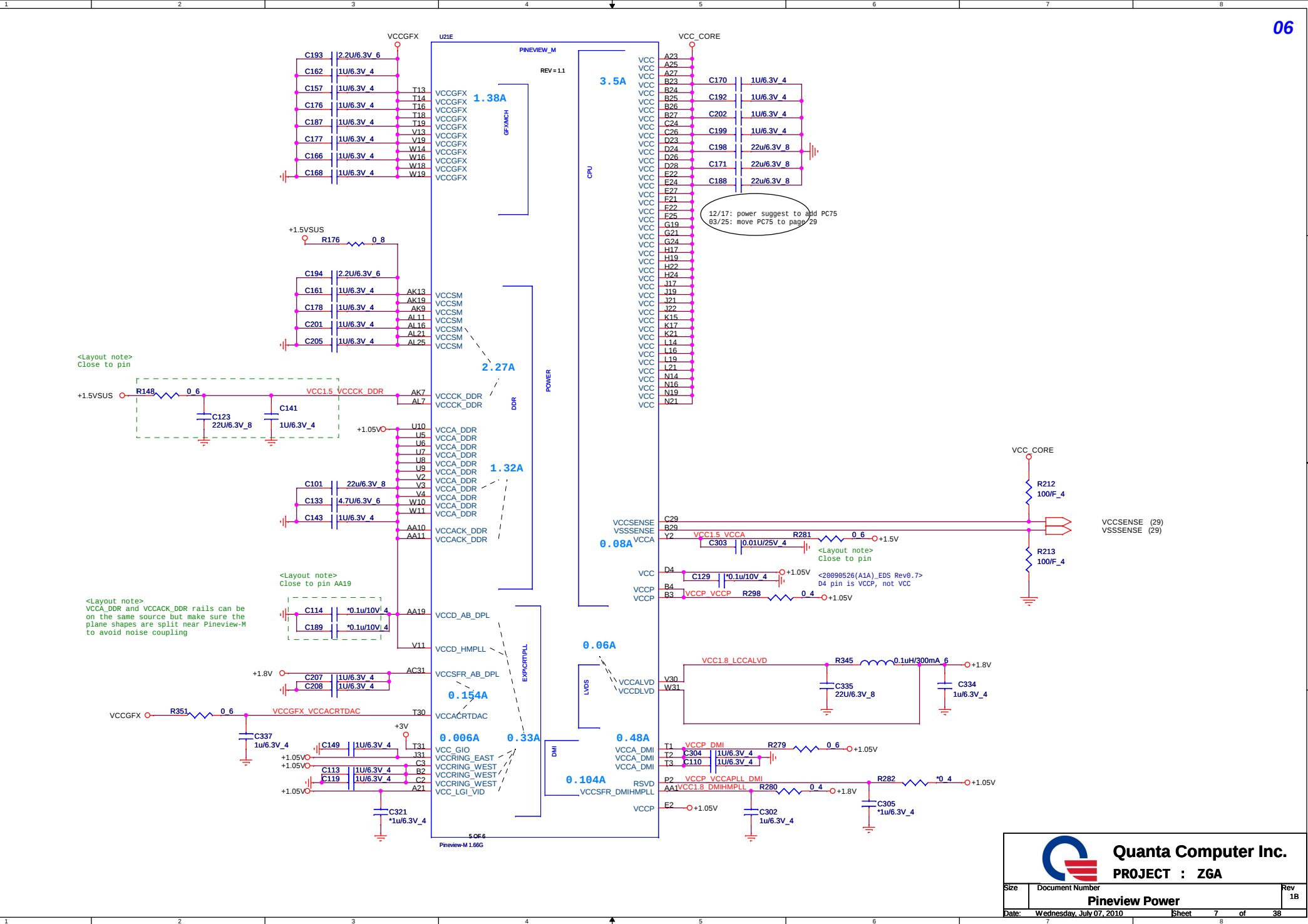
DDR_A_DQ0_6	AD3	M A DQ50
DDR_A_DQS#0_6	AD2	M A DQS#0
DDR_A_DM_0_6	AD4	M A DM0
DDR_A_DQ_0	AC4	M A DQ0
DDR_A_DQ_1	AC1	M A DQ1
DDR_A_DQ_2	AE1	M A DQ2
DDR_A_DQ_3	AG2	M A DQ3
DDR_A_DQ_4	AB2	M A DQ4
DDR_A_DQ_5	AB3	M A DQ5
DDR_A_DQ_6	AE2	M A DQ6
DDR_A_DQ_7	AB3	M A DQ7
DDR_A_DQS_0	AB8	M A DQS1
DDR_A_DQS#0_0	AD7	M A DQS#1
DDR_A_DM_1_0	AA9	M A DM1
DDR_A_DQ_8	AB6	M A DQ8
DDR_A_DQ_9	AB7	M A DQ9
DDR_A_DQ_10	AE5	M A DQ10
DDR_A_DQ_11	AB5	M A DQ11
DDR_A_DQ_12	AA5	M A DQ12
DDR_A_DQ_13	AB9	M A DQ13
DDR_A_DQ_14	AB9	M A DQ14
DDR_A_DQ_15	AD6	M A DQ15
DDR_A_DQS_2	AD8	M A DQS2
DDR_A_DQS#2_2	AD10	M A DQS#2
DDR_A_DM_2_2	AE8	M A DM2
DDR_A_DQ_16	AG8	M A DQ16
DDR_A_DQ_17	AG7	M A DQ17
DDR_A_DQ_18	AF10	M A DQ18
DDR_A_DQ_19	AE11	M A DQ19
DDR_A_DQ_20	AG11	M A DQ20
DDR_A_DQ_21	AE7	M A DQ21
DDR_A_DQ_22	AD11	M A DQ22
DDR_A_DQ_23	AE10	M A DQ23
DDR_A_DQS_3	AK5	M A DQS3
DDR_A_DQS#3_3	AK3	M A DQS#3
DDR_A_DM_3_3	A13	M A DM3
DDR_A_DQ_24	AH1	M A DQ24
DDR_A_DQ_25	A12	M A DQ25
DDR_A_DQ_26	AJ7	M A DQ26
DDR_A_DQ_27	AF3	M A DQ27
DDR_A_DQ_28	AE11	M A DQ28
DDR_A_DQ_29	AH2	M A DQ29
DDR_A_DQ_30	AL5	M A DQ30
DDR_A_DQ_31	AG2	M A DQ31
DDR_A_DQS_4	AG36	M A DQS4
DDR_A_DQS#4_4	AD19	M A DQS#4
DDR_A_DM_4_4	AD21	M A DM4
DDR_A_DQ_32	AE19	M A DQ32
DDR_A_DQ_33	AE19	M A DQ33
DDR_A_DQ_34	AE22	M A DQ34
DDR_A_DQ_35	AD22	M A DQ35
DDR_A_DQ_36	AF17	M A DQ36
DDR_A_DQ_37	AE19	M A DQ37
DDR_A_DQ_38	AD21	M A DQ38
DDR_A_DQ_39	AE21	M A DQ39
DDR_A_DQS_5	AE26	M A DQS5
DDR_A_DQS#5_5	AG27	M A DQS#5
DDR_A_DM_5_5	AJ27	M A DM5
DDR_A_DQ_40	AE24	M A DQ40
DDR_A_DQ_41	AG25	M A DQ41
DDR_A_DQ_42	AD25	M A DQ42
DDR_A_DQ_43	AD24	M A DQ43
DDR_A_DQ_44	AC22	M A DQ44
DDR_A_DQ_45	AD24	M A DQ45
DDR_A_DQ_46	AE27	M A DQ46
DDR_A_DQ_47	AE27	M A DQ47
DDR_A_DQS_6	AE30	M A DQS6
DDR_A_DQS#6_6	AE29	M A DQS#6
DDR_A_DM_6_6	AF30	M A DM6
DDR_A_DQ_48	AG31	M A DQ48
DDR_A_DQ_49	AD29	M A DQ49
DDR_A_DQ_50	AD30	M A DQ50
DDR_A_DQ_51	AD30	M A DQ51
DDR_A_DQ_52	AJ29	M A DQ52
DDR_A_DQ_53	AE29	M A DQ53
DDR_A_DQ_54	AE29	M A DQ54
DDR_A_DQ_55	AD28	M A DQ55
DDR_A_DQS_7	AB27	M A DQS7
DDR_A_DQS#7_7	AA27	M A DQS#7
DDR_A_DM_7_7	AB26	M A DM7
DDR_A_DQ_56	AE24	M A DQ56
DDR_A_DQ_57	W25	M A DQ57
DDR_A_DQ_58	BZ4	M A DQ58
DDR_A_DQ_59	AB28	M A DQ60
DDR_A_DQ_60	AB23	M A DQ61
DDR_A_DQ_61	AC23	M A DQ62
DDR_A_DQ_62	W27	M A DQ63

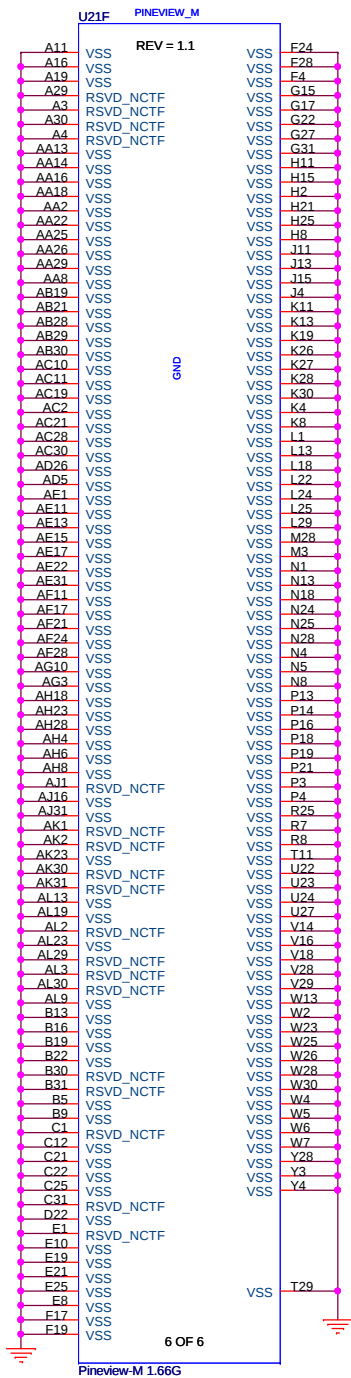
 M_A_DQ[63..0] (3)

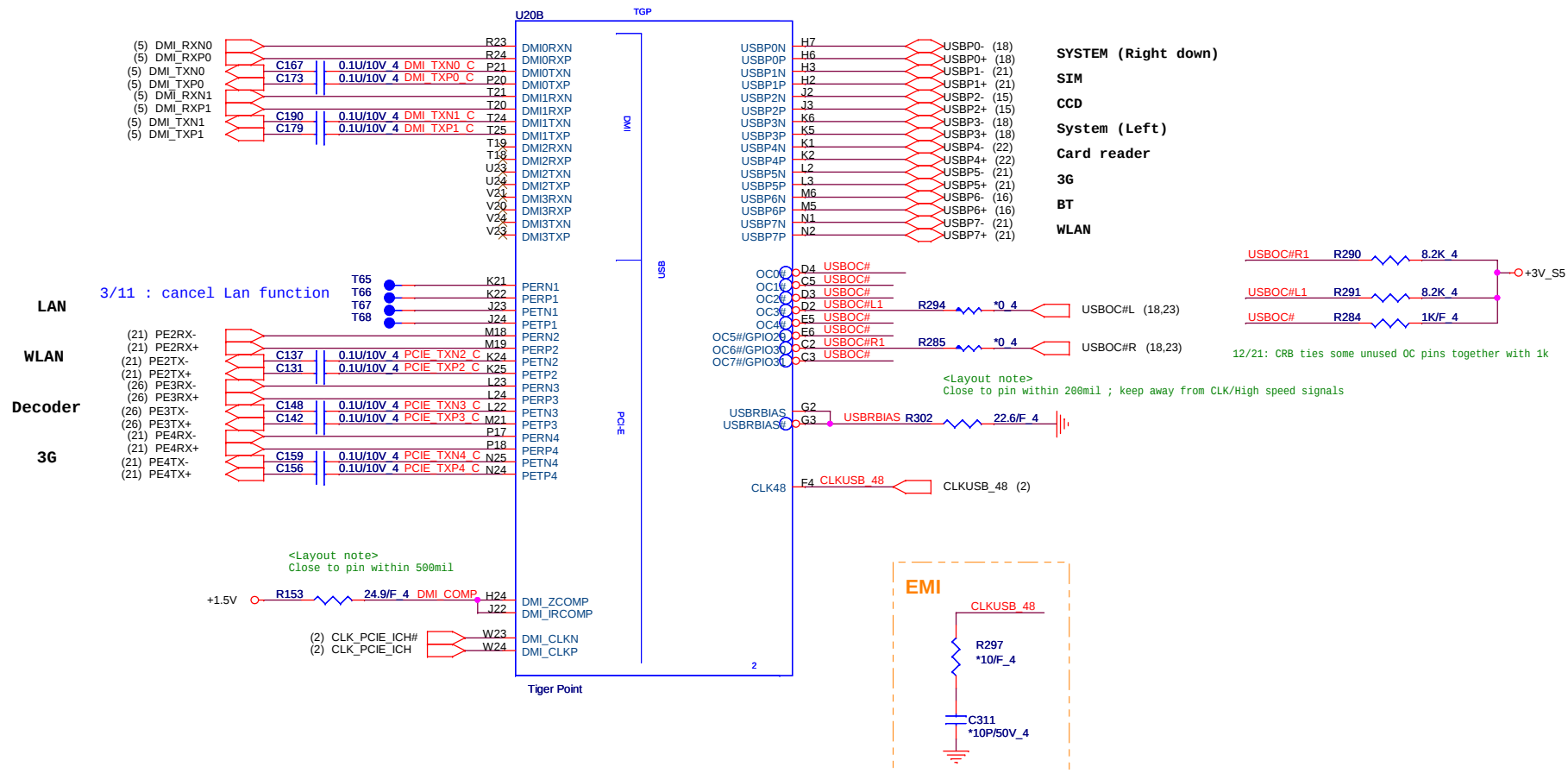
 M_A_DM[7..0] (3)

 M_A_DQS[7..0] (3)

 M_A_DQS#[7..0] (3)



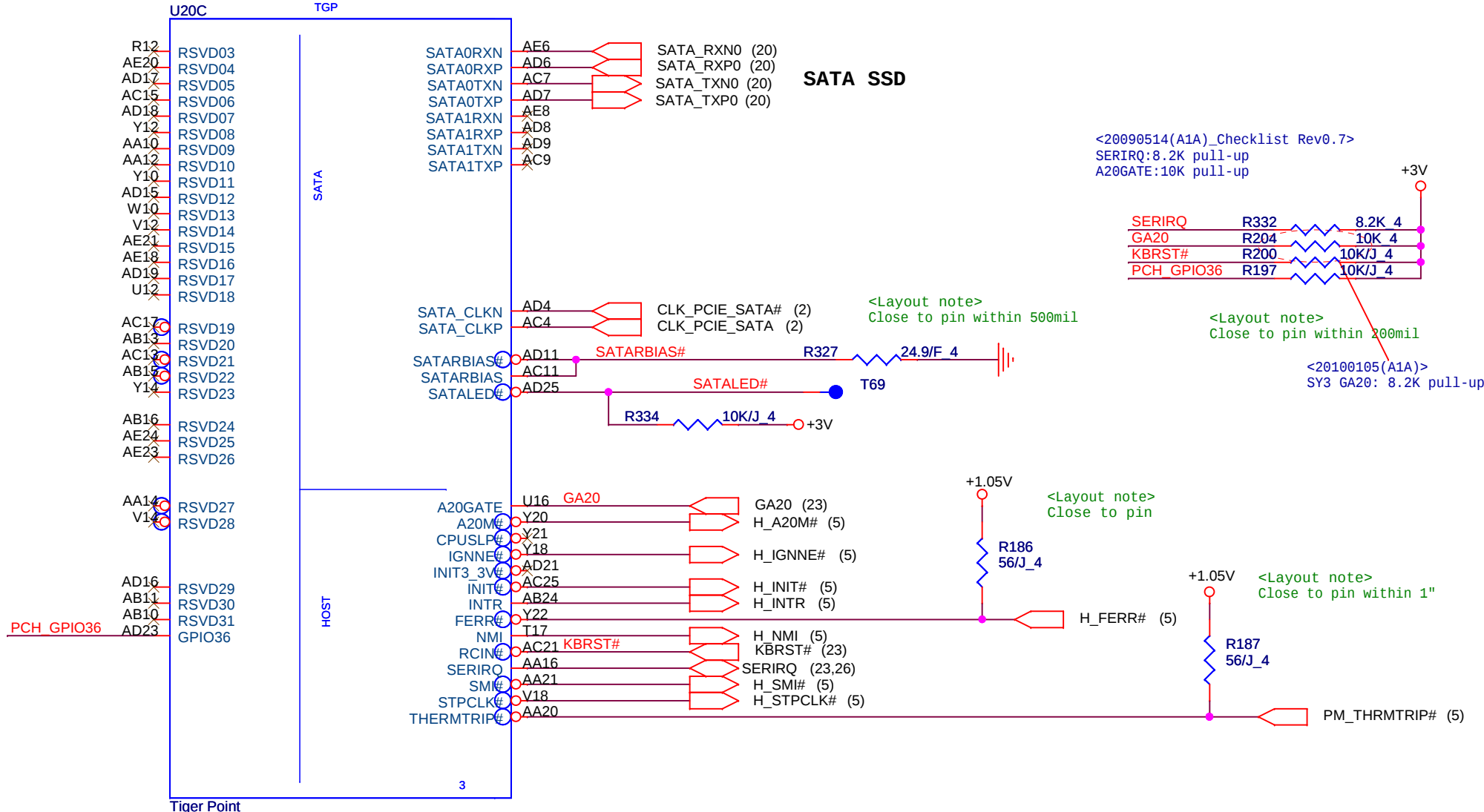




Quanta Computer Inc.
PROJECT : Z6A

Size	Document Number	Rev
	Tiger Point DMI/PCIE/USB	1B

Date: Wednesday, July 07, 2010 Sheet 9 of 38



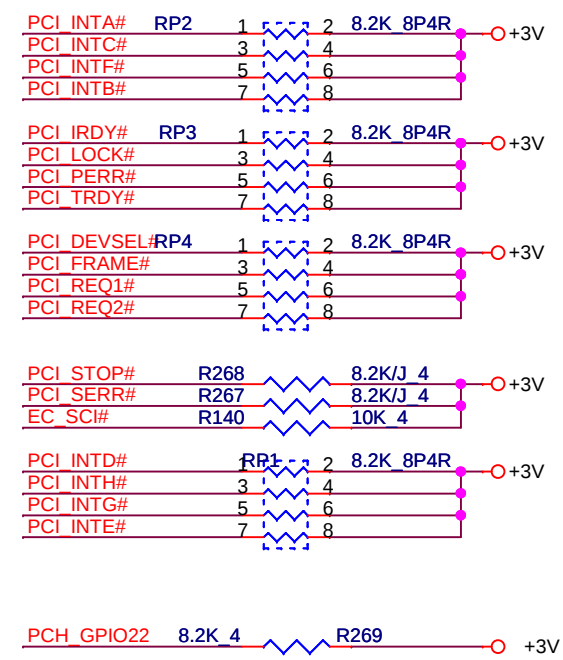
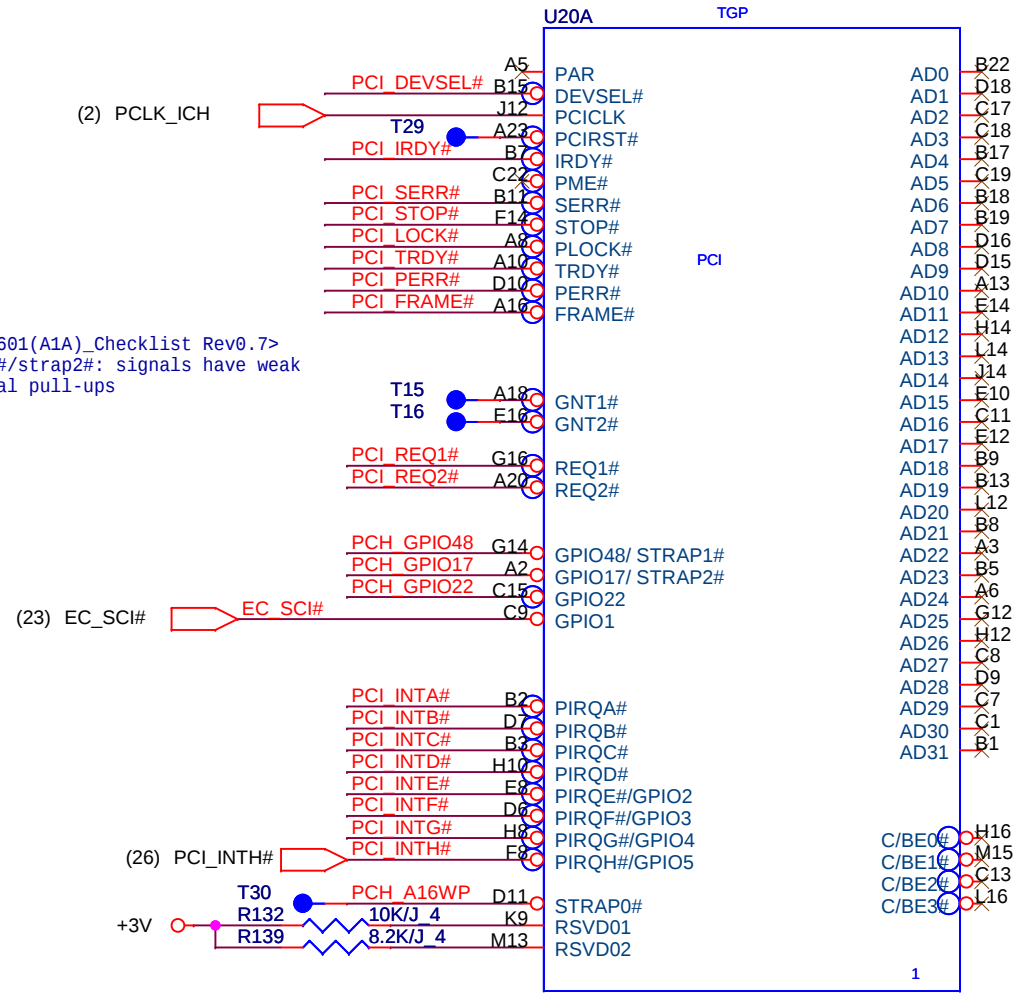
NOTE :
1. CPUSLP# is supported only on nettop platforms.

Quanta Computer Inc.

PROJECT : ZGA

Size	Document Number	Rev
	Tiger Point Sata/Host	1B
Date:	Wednesday, July 07, 2010	Sheet 10 of 38

<20090601(A1A)_Checklist Rev0.7>
Strap1#/strap2#: signals have weak
internal pull-ups



ICH Boot BIOS select

PCH_GPIO17 (INT PU)	PCH_GPIO48 (INT PU)	Boot BIOS Location
0	1	SPI (Default)
1	0	PCI
1	1	LPC



A16 SWAP Override strap

PCH_A16W (INT PU)	Low = A16 swap override enabled High = Default
----------------------	---

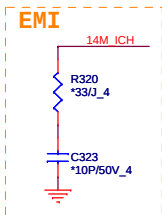
IRQ	Description
PIRQA	USB UHCI Controller #1, #4
PIRQB	AC'97 Codec; option for SMBUS
PIRQC	USB UH Controller #3; SATA/IDE Native Mode
PIRQD	USB UHCI Controller #2
PIRQE	Internal LAN; Option for SCI, TCO, HPET#0,1,2
PIRQF	Option for SCI, TCO, HPET#0,1,2
PIRQG	Option for SCI, TCO, HPET#0,1,2
PIRQH	USB EHCI Controller; Option for SCI, TCO, HPET#0,1,2

PCI_GNT#2	Internal PU Should not be PD
-----------	---------------------------------

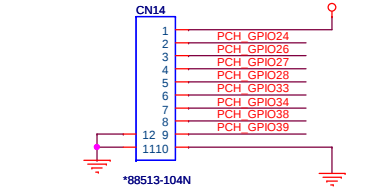
Quanta Computer Inc.

PROJECT : ZGA

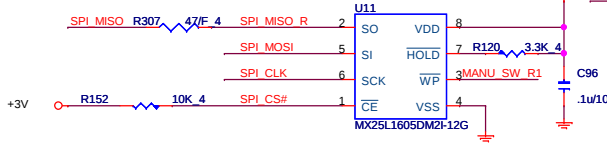
Size	Document Number	Rev 1B
TigerPoint PCI(3/6)		
Date:	Wednesday, July 07, 2010	Sheet 11 of 38



debug port for google require

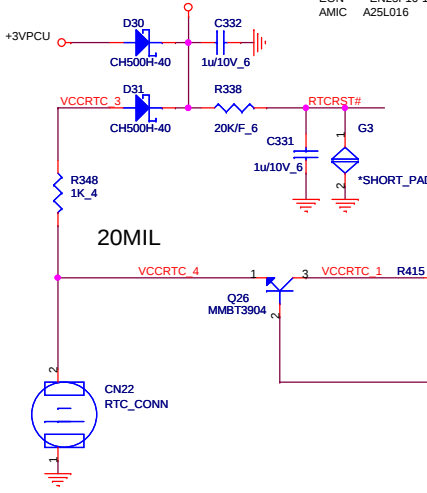


SPI FLASH(CLG)



1/13 Confirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

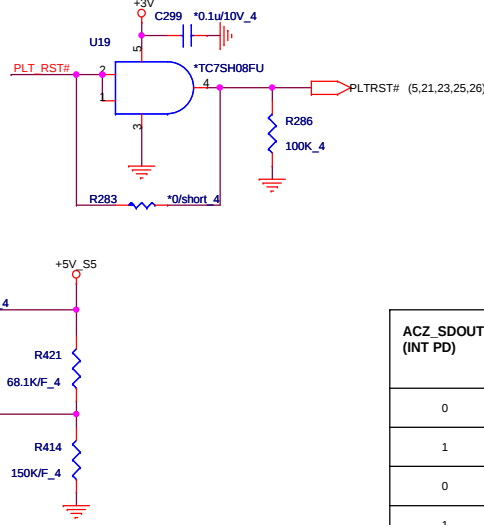
RTC(RTC)



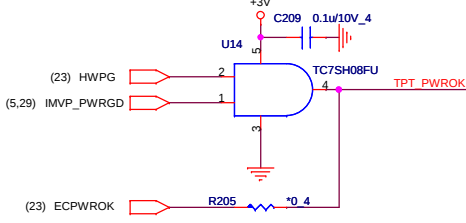
At 11/24 add
Winbond W25X16AVSSIG
MXIC MX25L1605AM2C-15G
EON EN25F16-100HIP
AMIC A25L016

AKE382P0N01
AKE37FP0Z13
AKE38ZADQ00
AKE382N0800

Platform Reset



TPT Power OK



ACZ_SDOUT (INT PD)	ACZ_SYNC (INT PD)	Description
0	0	* 4 x 1s
1	0	Reserved
0	1	Reserved
1	1	1 x 4s (1 port/4 lanes)

INTVRMEN	
1	Enable internal VccSus1_5 VRM (default)
0	Disable

Quanta Computer Inc.
PROJECT : ZGA

Size: Document Number: TigerPoint GPIO

Date: Wednesday, July 07, 2010 Sheet 12 of 38

Rev 1A

1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

D23, D24 are just for preventing EC/SB F/W error to cause to leakage current. If test OK, they can be connected directly.

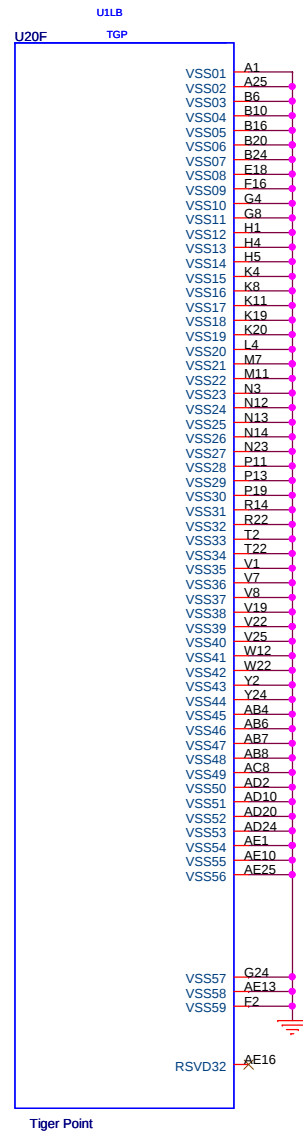
<20090515(A1A).Checklist Rev0.7>
BATLOW#:8.2K pull-up to V3ALWAYS
WAKE#:10K pull-up to VccSus3_3
SYS_RST#:10K pull-up to VccSus3_3



1



Size	Document Number	Rev
	TigerPoint Power	1B
Date:	Wednesday, July 07, 2010	Sheet 13 of 38



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



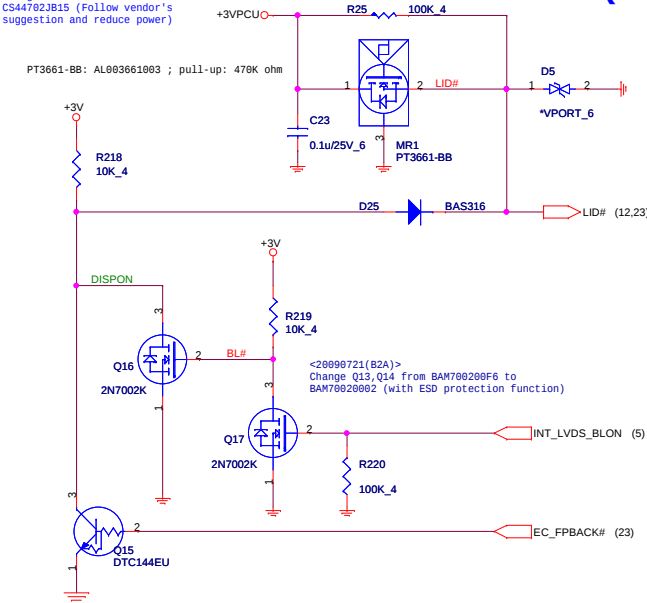
Quanta Computer Inc.
PROJECT : ZGA

Size	Document Number	Rev
	TigerPoint GND	1B
Date:	Wednesday, July 07, 2010	Sheet 14 of 38

HALL SENSOR(HSR)

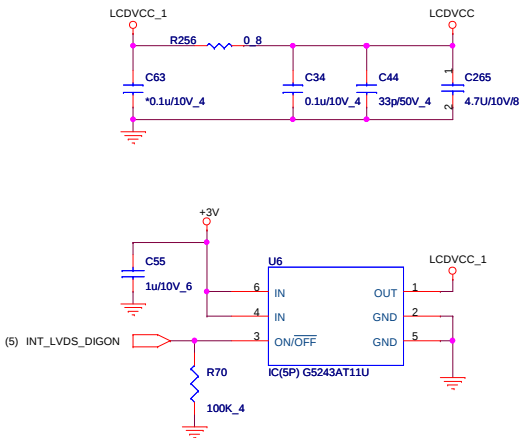
<20090724(B2A)>

Change R5 from CS41002J820 to CS44702J815 (Follow vendor's suggestion and reduce power)



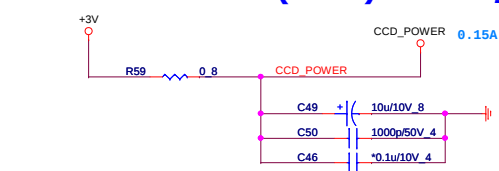
LED Panel POWER SWITCH(LDS)

Irush=1.5A

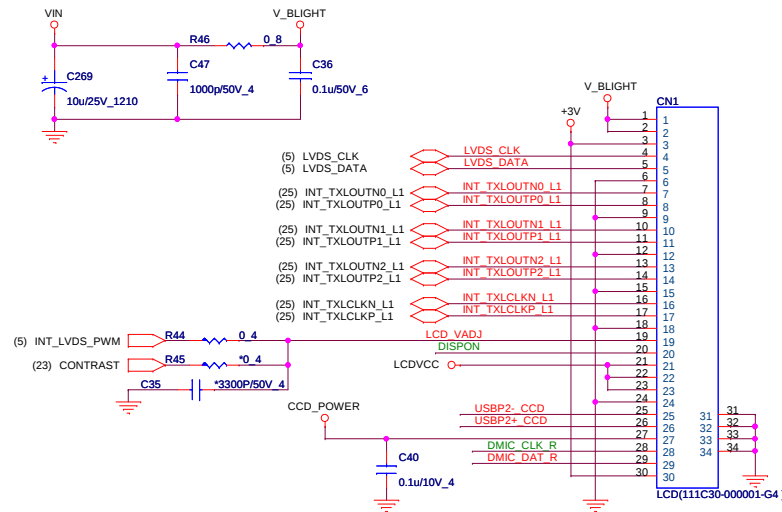


CAMERA POWER(CCD)

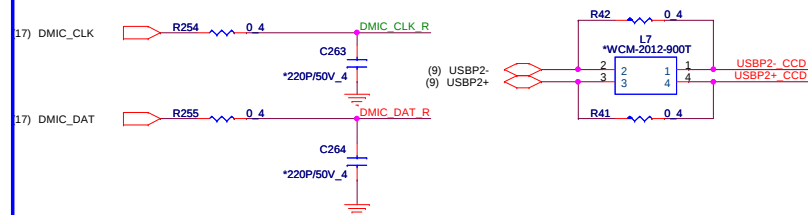
14



LED Panel(LDS)



B-test 8/11: for EMI



CRT(CRT)

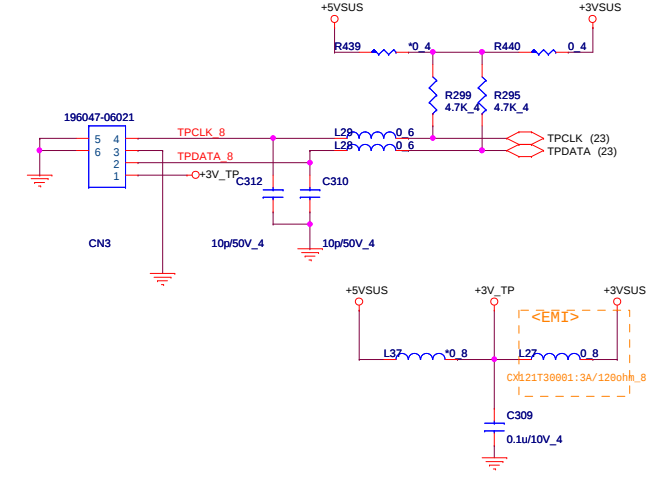
3/11 : cancel CRT function



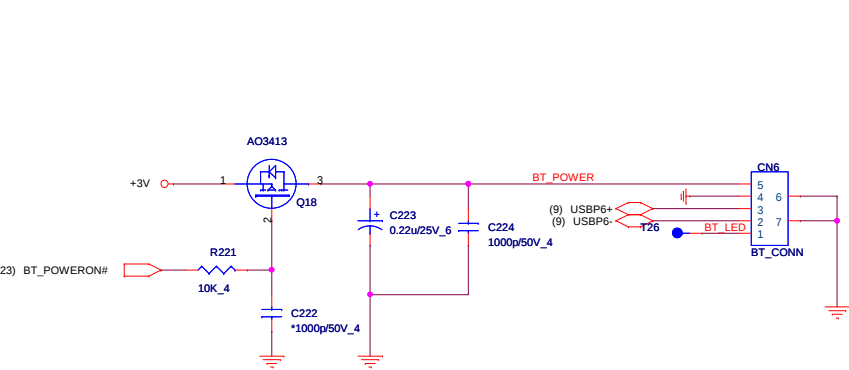
Quanta Computer Inc.
PROJECT : Z6A

Size	Document Number	Rev
	CRT/LVDS	1B
Date:	Wednesday, July 07, 2010	Sheet 15 of 38

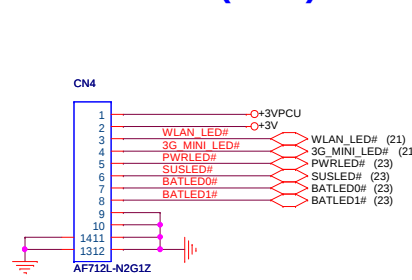
TOUCH PAD(TPD)



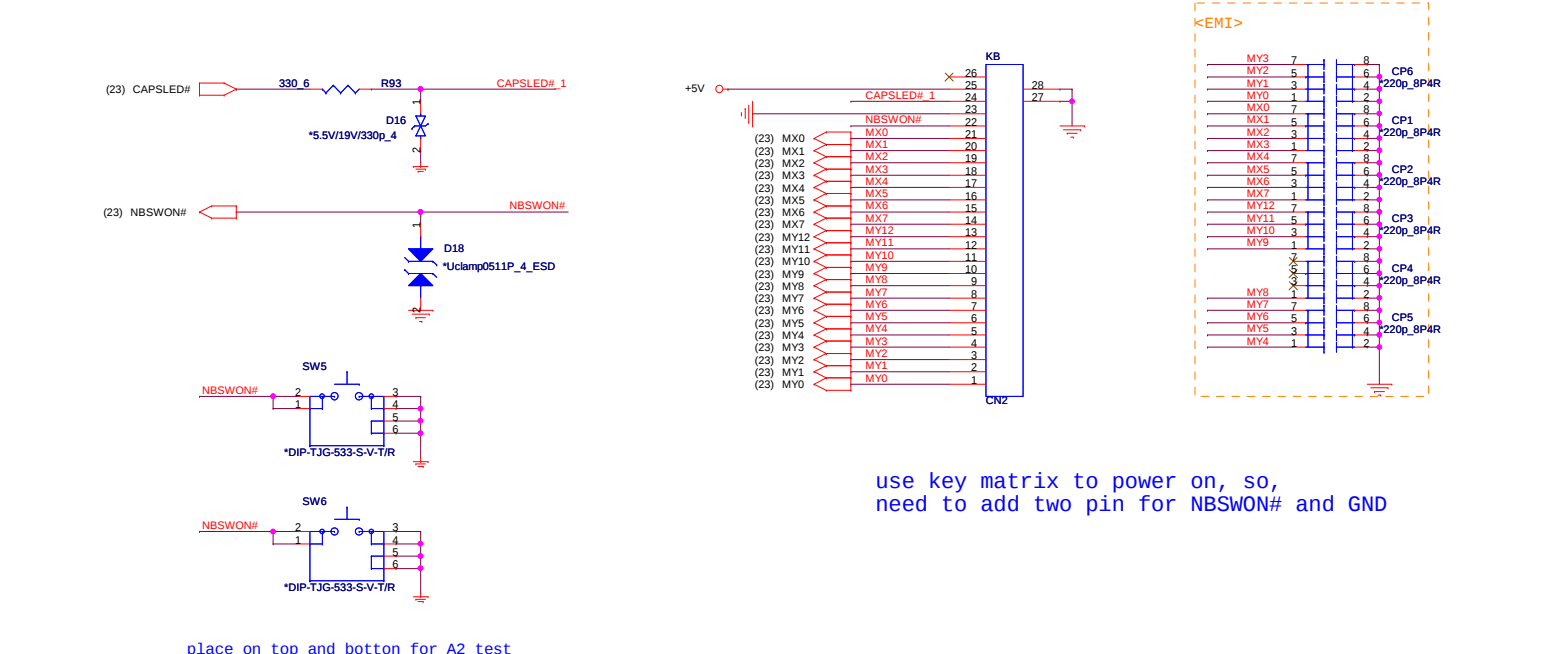
BLUETOOTH(BTM)



Connector (UIF)



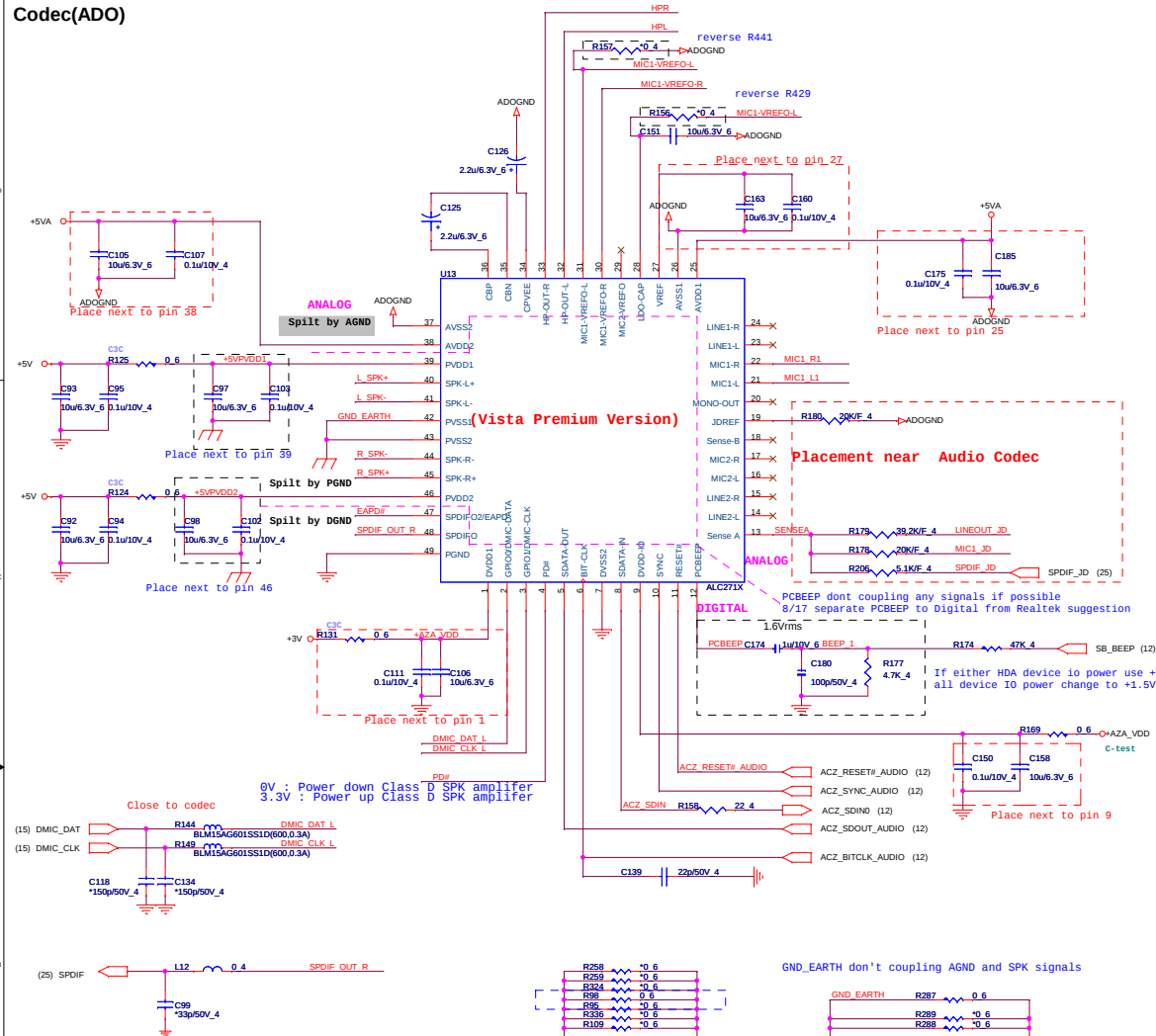
KEYBOARD(KBC)



RGB to HDMI(DB)

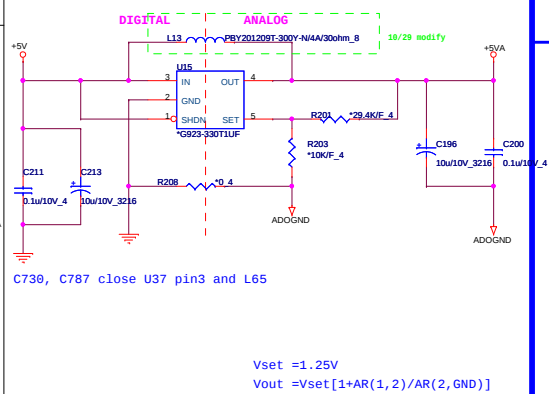
use LVDS to HDMI solution, so delete CN11

Codec(ADO)

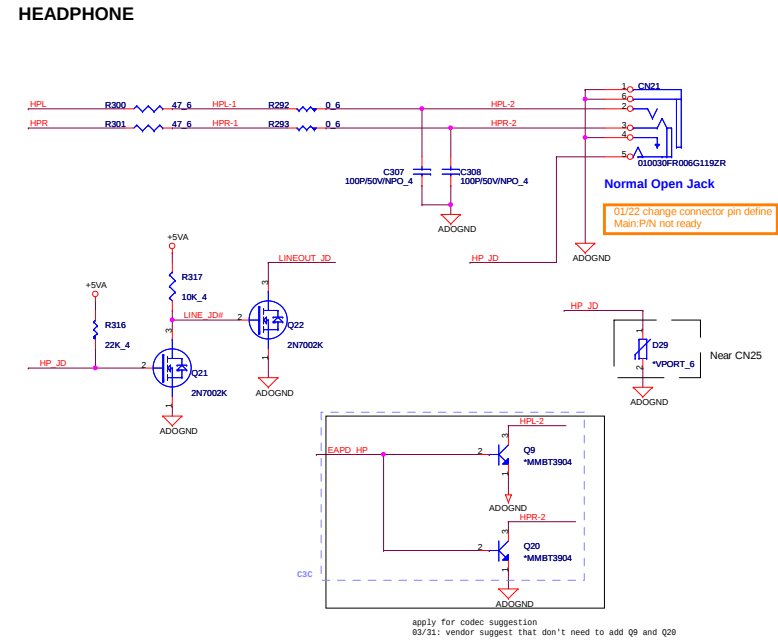


Power (ADO)

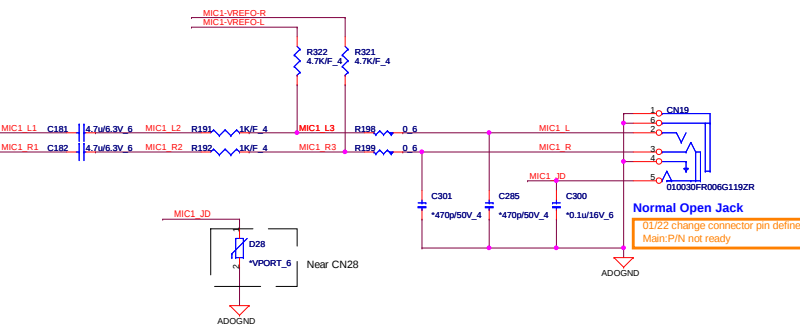
Demodulation Filter L65 Place close to Codec



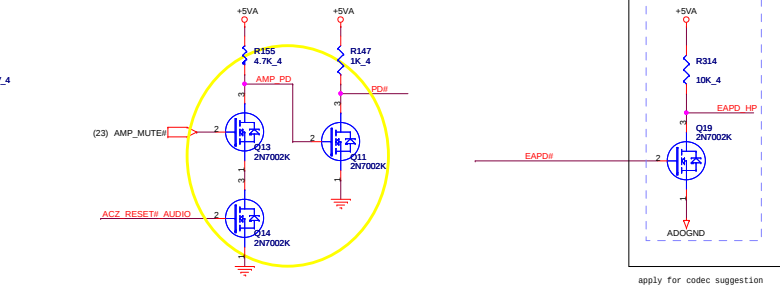
HEADPHONE



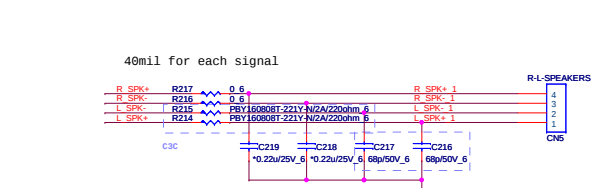
System MIC



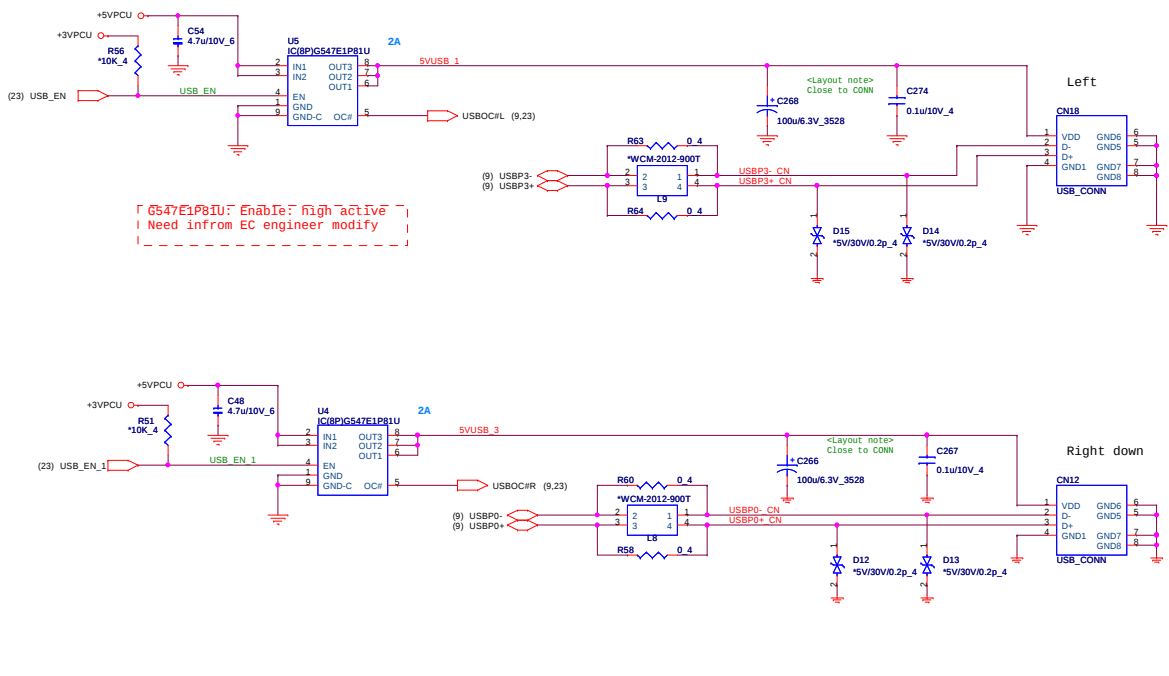
Mute(ADO)



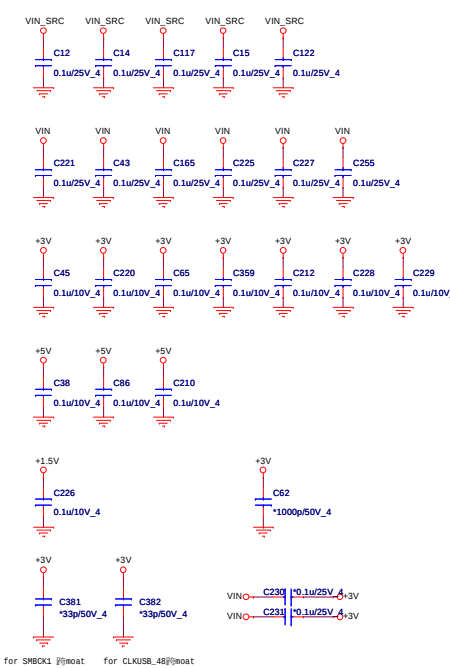
Internal Speaker



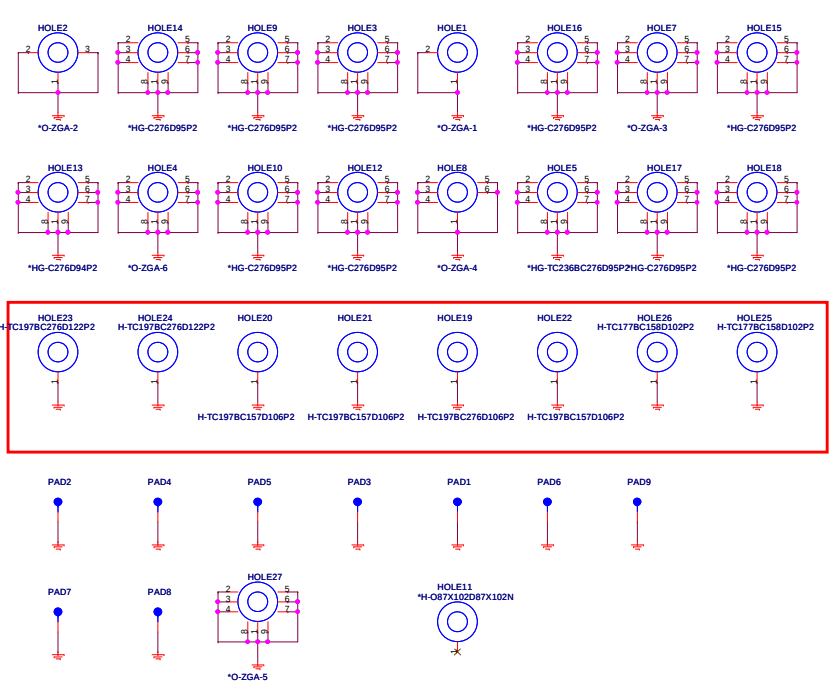
USB(USB)



EMI



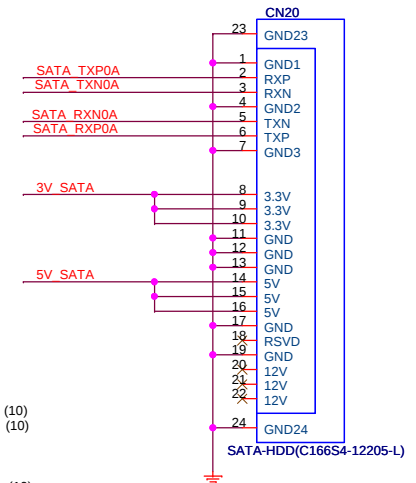
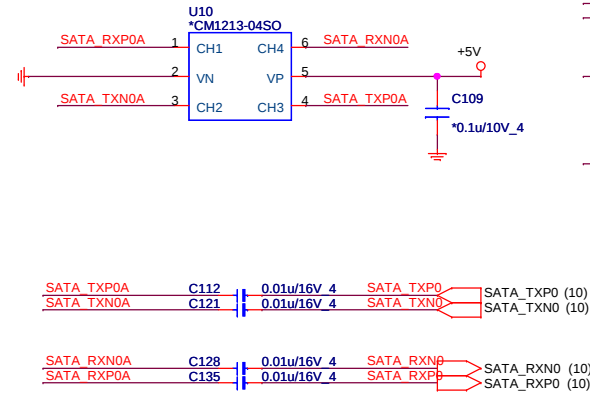
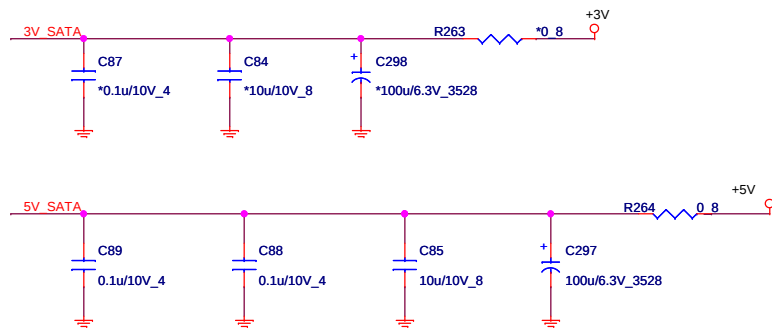
Hole



Giga-LAN AR8151(LAN)

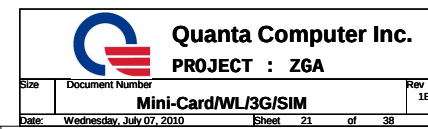
TRANSFORMER(LAN)

RJ45(LAN)

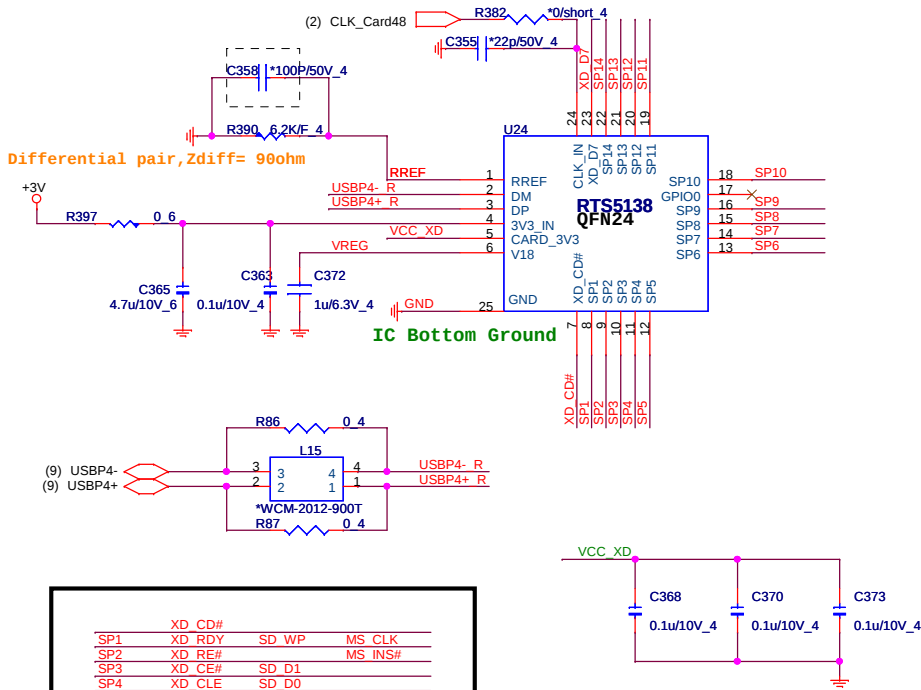


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	SATA-HDD/SSD	1B
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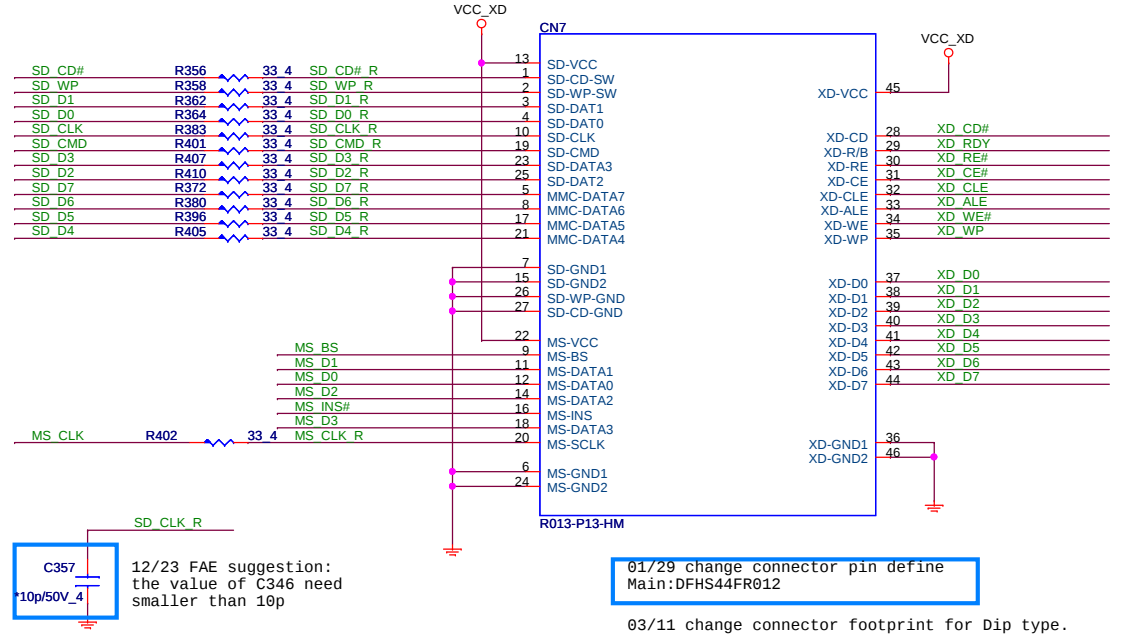


RTS5138



	XD_CD#			
SP1	XD_RDY	SD_WP	MS_CLK	
SP2	XD_RE#	SD_D1	MS_INS#	
SP3	XD_CE#	SD_D0		
SP4	XD_CLE	SD_D7	MS_D3	
SP5	XD_ALE	SD_CD#		
SP6	XD_WE#	SD_CLK	MS_D2	
SP7	XD_WP	SD_D6	MS_D0	
SP8	XD_D0	SD_D5		
SP9	XD_D1	SD_CMD		
SP10	XD_D2	SD_D4		
SP11	XD_D3	SD_D3	MS_D1	
SP12	XD_D4	SD_D2		
SP13	XD_D5			
SP14	XD_D6		MS_BS	
	XD_D7			

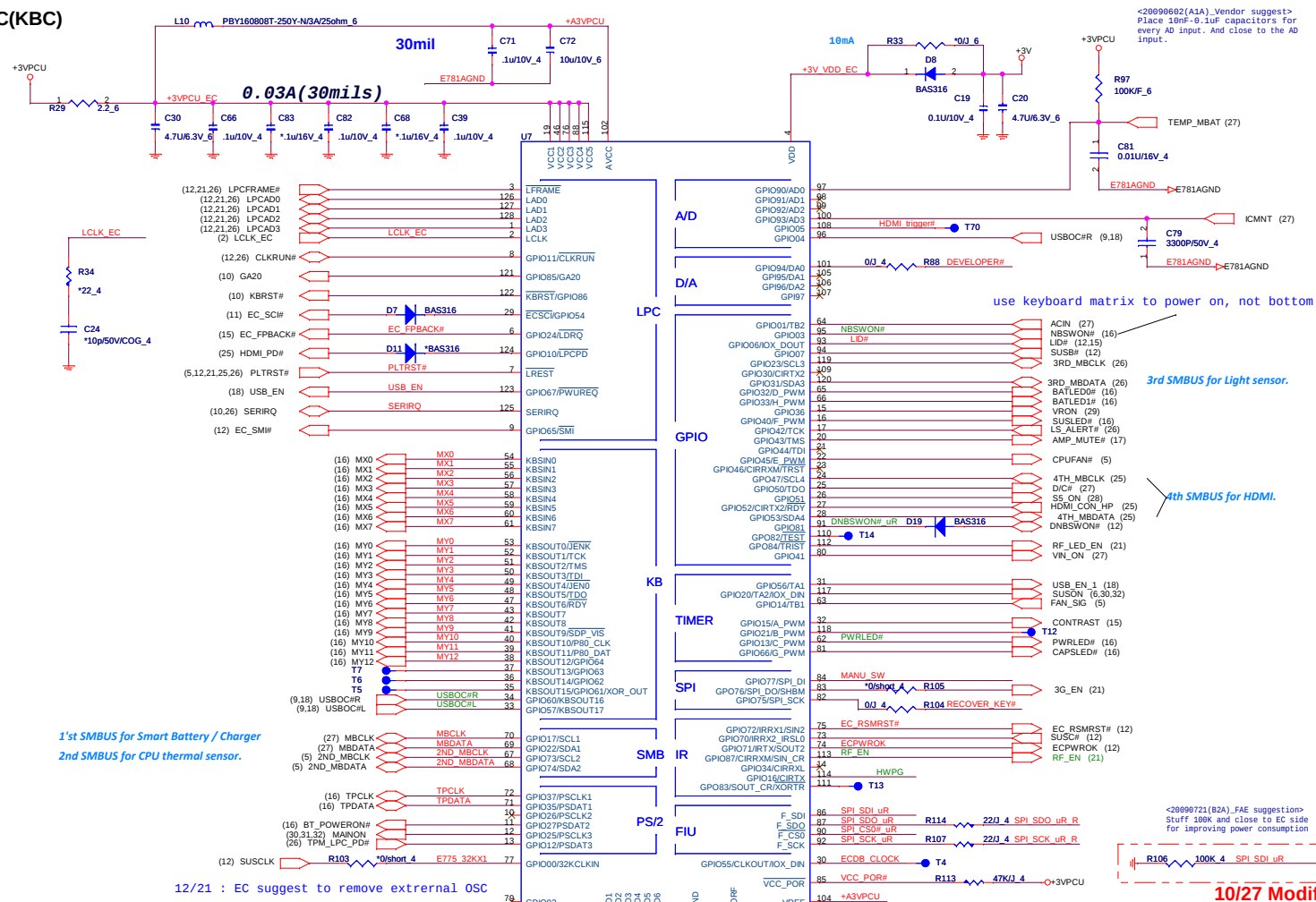
Share Pin



01/29 change connector pin define
Main:DFHS44FR012

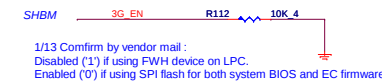
03/11 change connector footprint for Dip type.

EC(KBC)

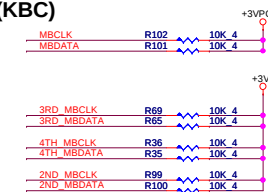


I/O ADDRESS SETTING(KBC)

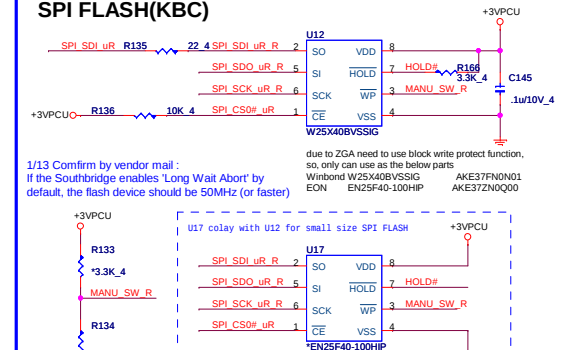
SHBM=0: Enable shared memory with host BIOS



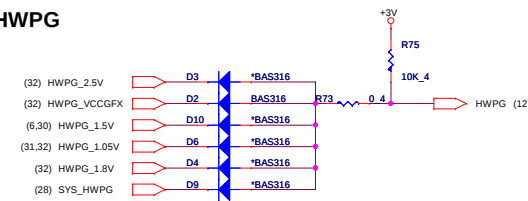
SM BUS PU(KBC)



SPI FLASH(KBC)



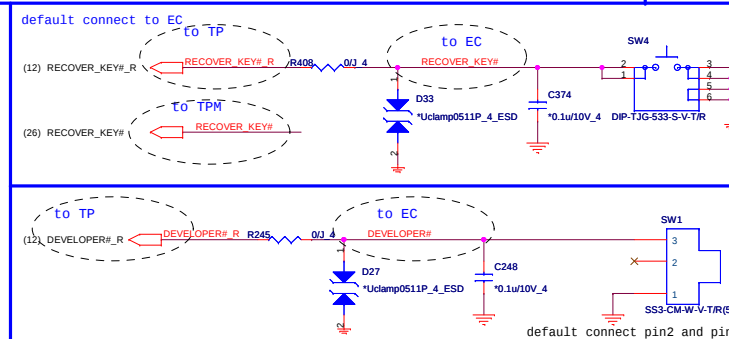
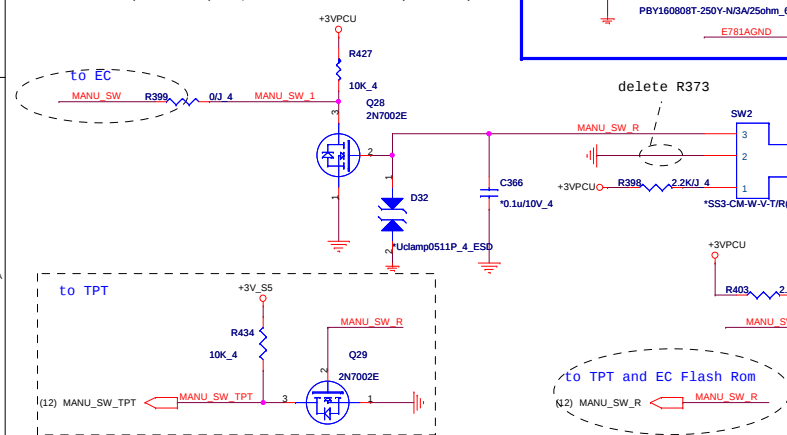
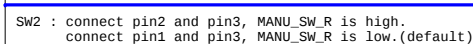
HWPG



SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	CPU thermal sensor
SM Bus 3	Light sensor

INTERNAL KEYBOARD STRIP SET(KBC)





PROJECT : ZGA

Size

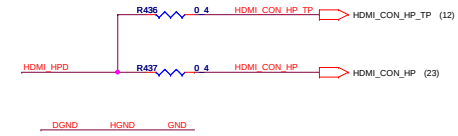
Document Number

HDMI(1/2)

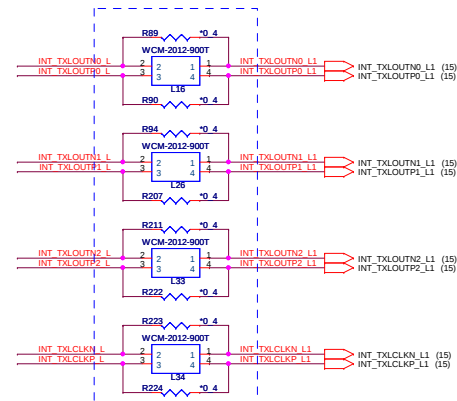
Rev

REV
1A

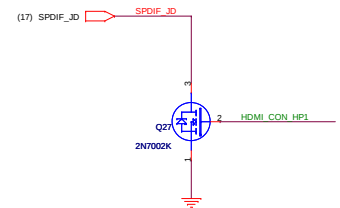
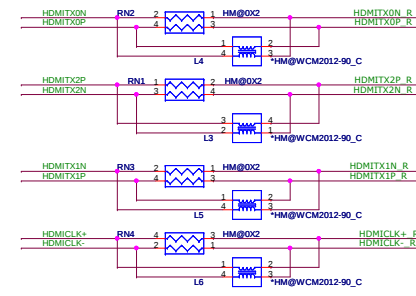
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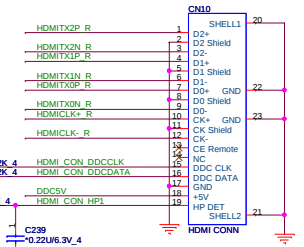
for SPDIF level shift



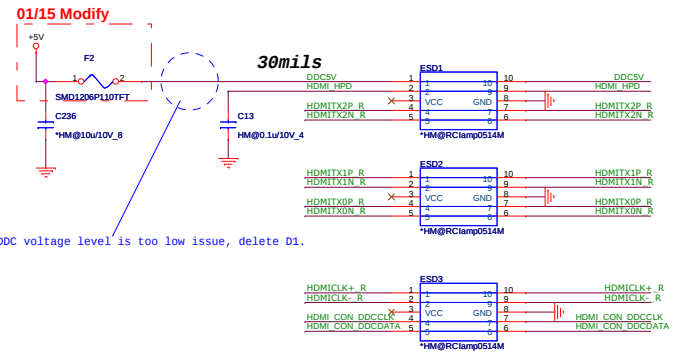
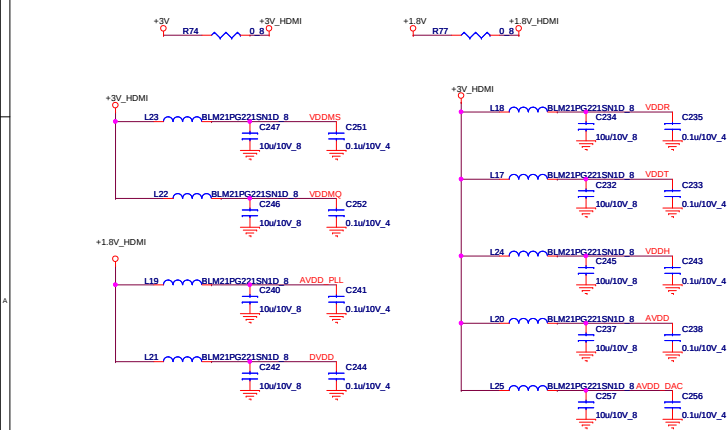
6/29 : RF team suggest to add L16,L26,L33,L34



HDMI CONN

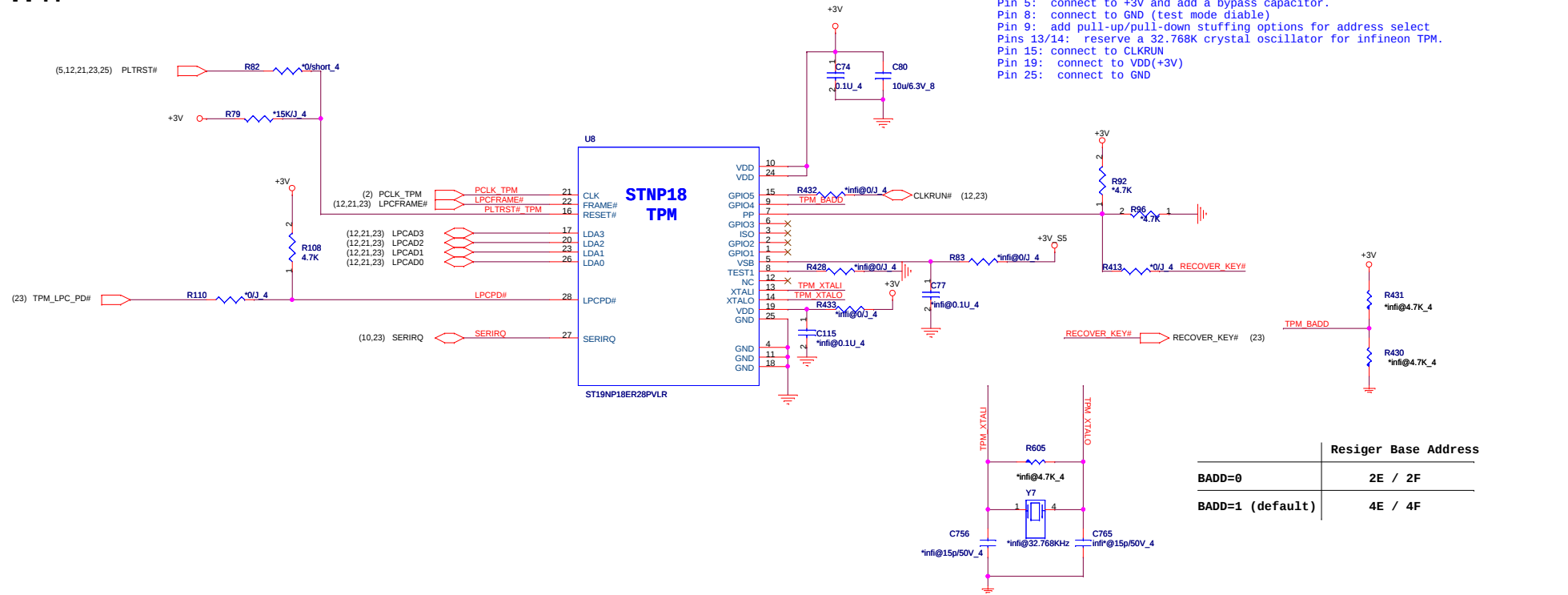


vendor suggest to devide the the voltage.



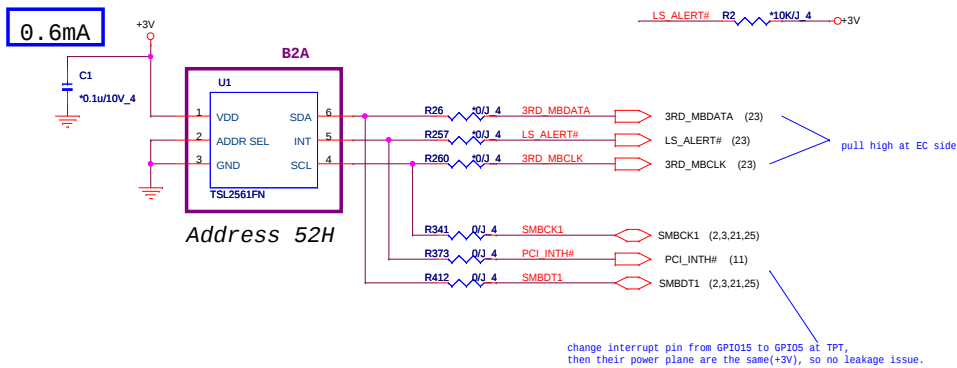
due to DDC voltage level is too low issue, delete D1.

TPM



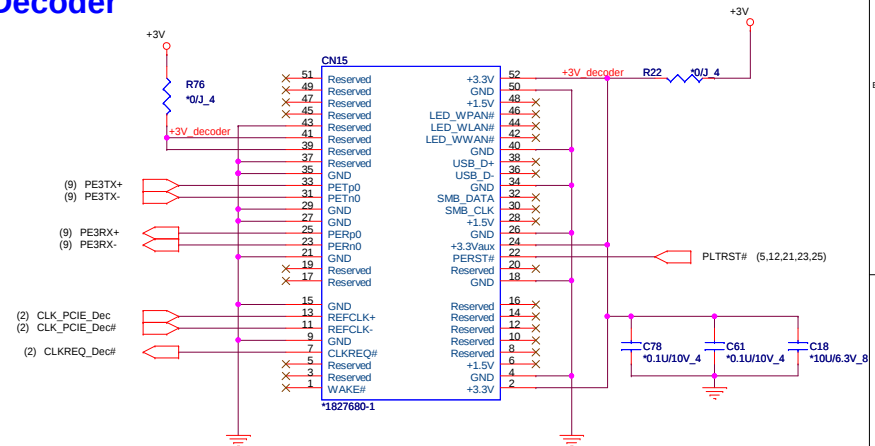
Light Sensor(LSR)

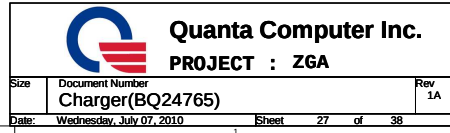
connector to EC, just stuff R2,R26,R257,R260
 connector to TPT, just stuff R341,R373,R412



Video Decoder

dont need to stuff first, use innr document to add it.





OCP:5.5A

3.8A 152mIl

+5VPCU

OCP:5.5A

L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
~2.525A
Iocp=5.5-(2.525/2)=4.24A
Vth=4.24A*14.2mOhm=0.06V
R(Ilim)=(0.06V*10)/5uA
~120K

0.1A

10mIl

OCP:5A

L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
~1.267A
Iocp=5-(1.267/2)=4.37A
Vth=4.37A*19.6mOhm=85.59mV
R(Ilim)=(85.59mV*10)/5uA
~171K

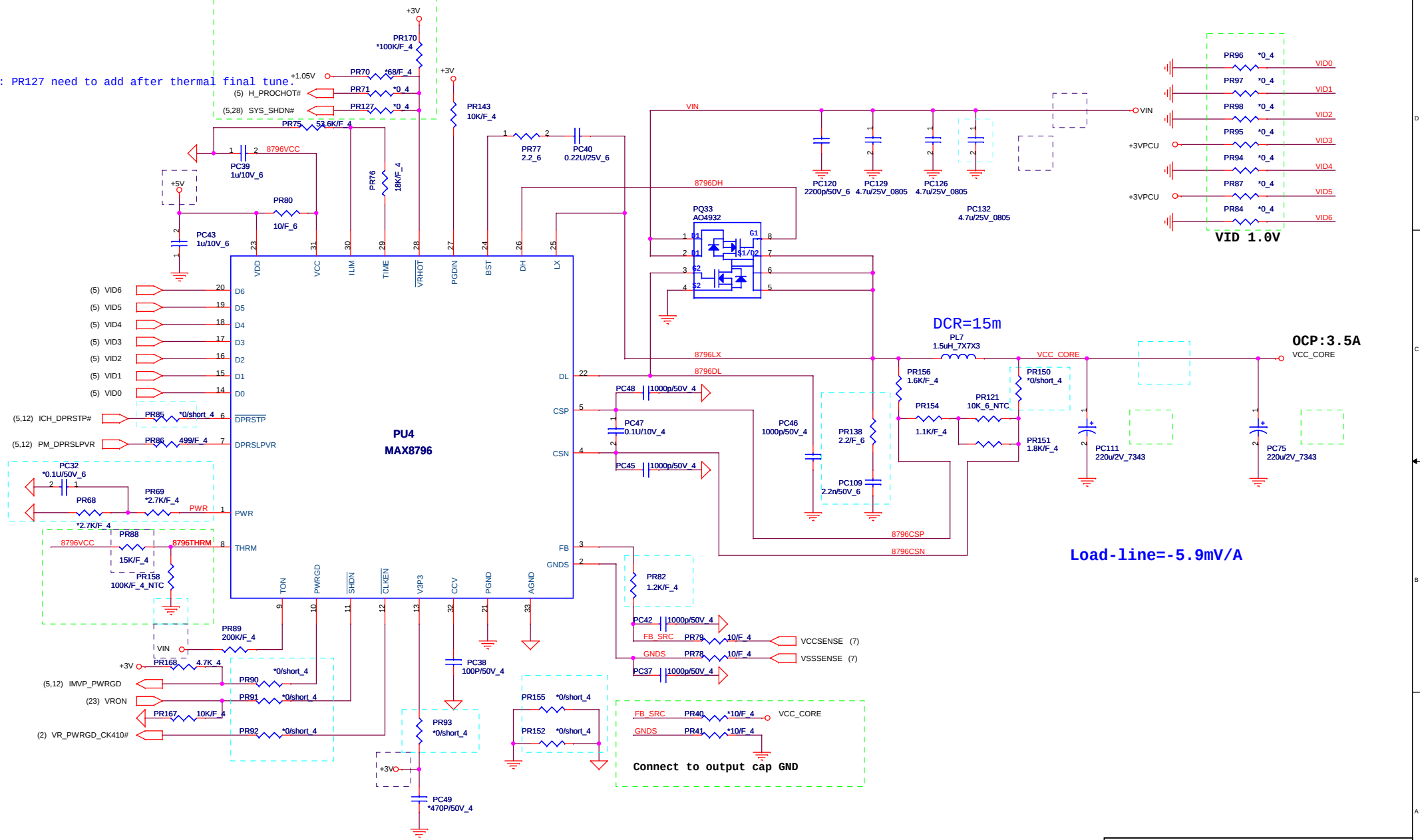
148mIl

OCP:5A

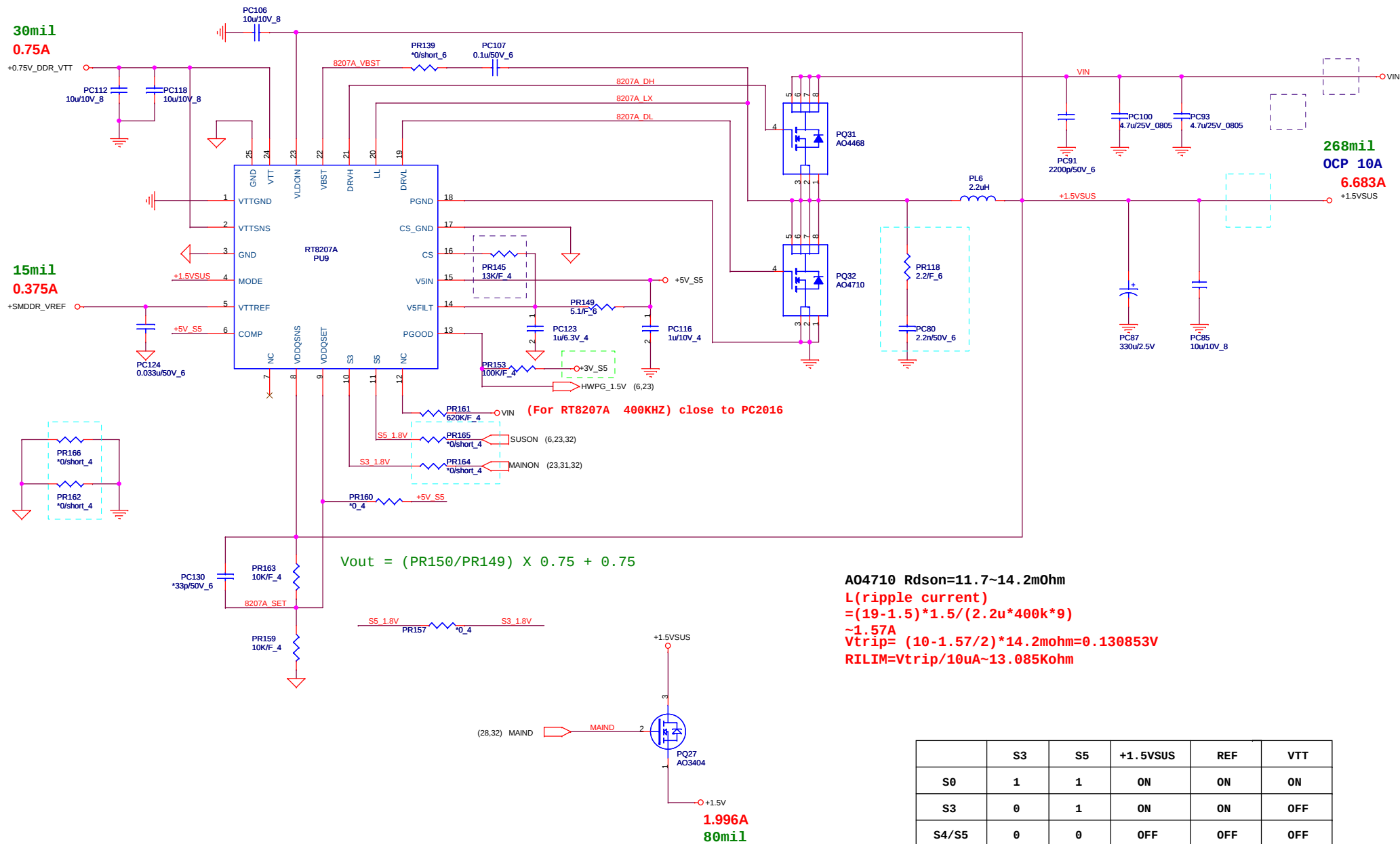
3.7A

+3VPCU

6/24 : PR127 need to add after thermal final tune

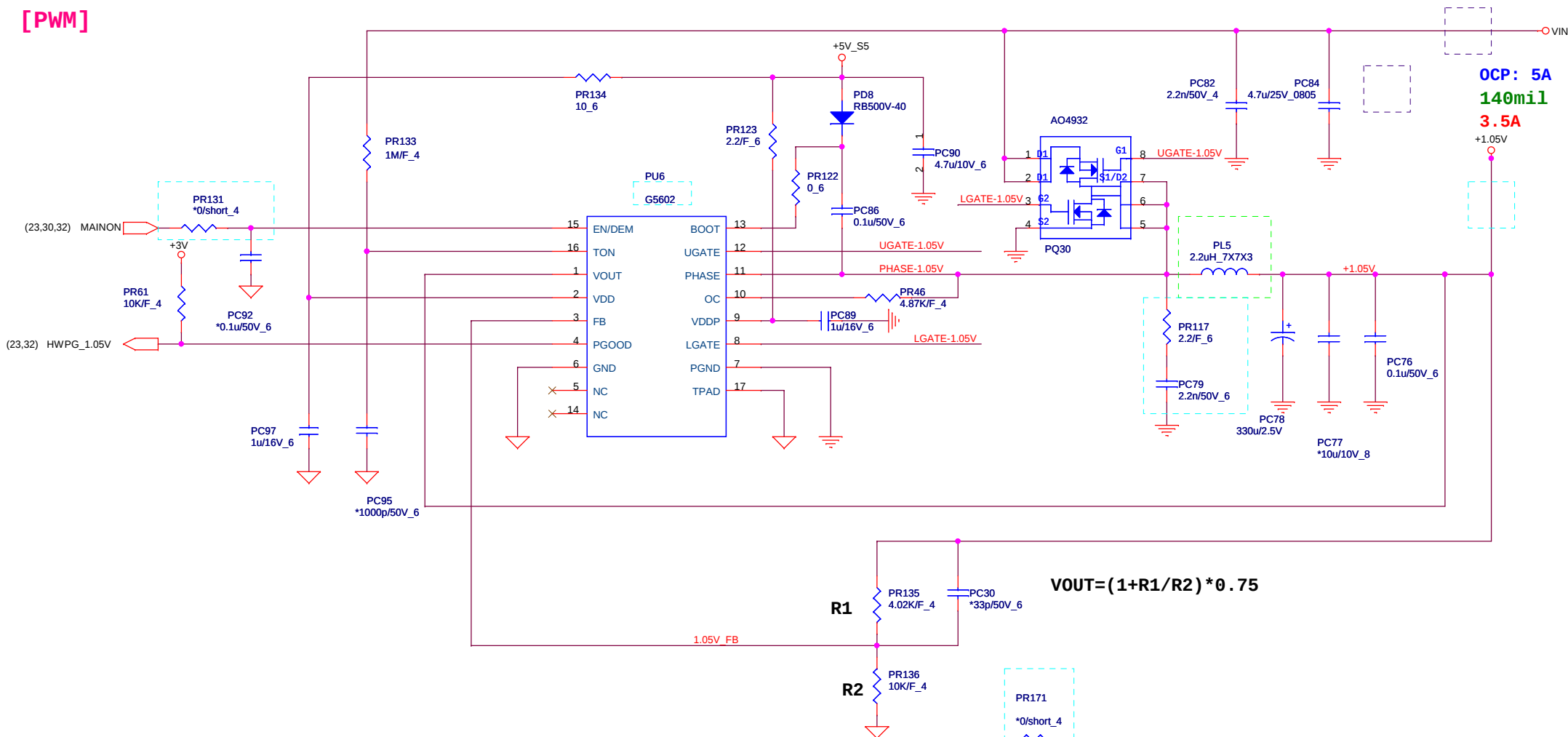


[PWM]



	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

[PWM]



OCP: 5A
140mil
3.5A

+1.05V

$$VOUT = (1 + R1/R2) * 0.75$$

$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

$$TON = 3.85p * 1M * 1 / (Vin - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

A04932 Rdson=15.8~19.6m0hm

$$L(ripple\ current) = (19 - 1.05) * 1.05 / (2.2u * 272k * 19) \sim 1.658A$$

$$Rth = 19.6m * (5 - 0.829) / 20uA$$

$$RILIM = 4.087Kohm$$



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	+1.05V(UP6111AQDD)	1A

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Size

Document Number

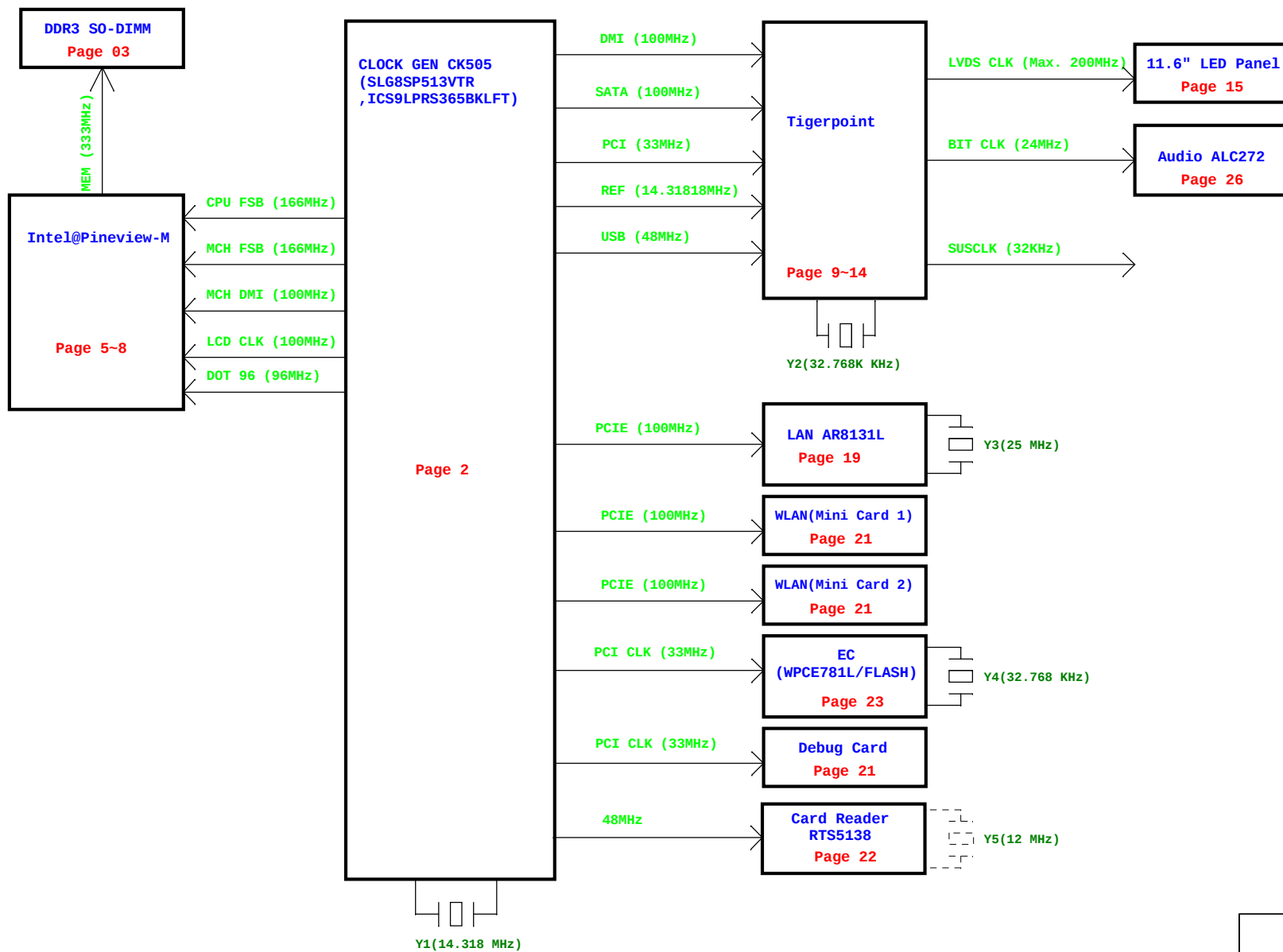
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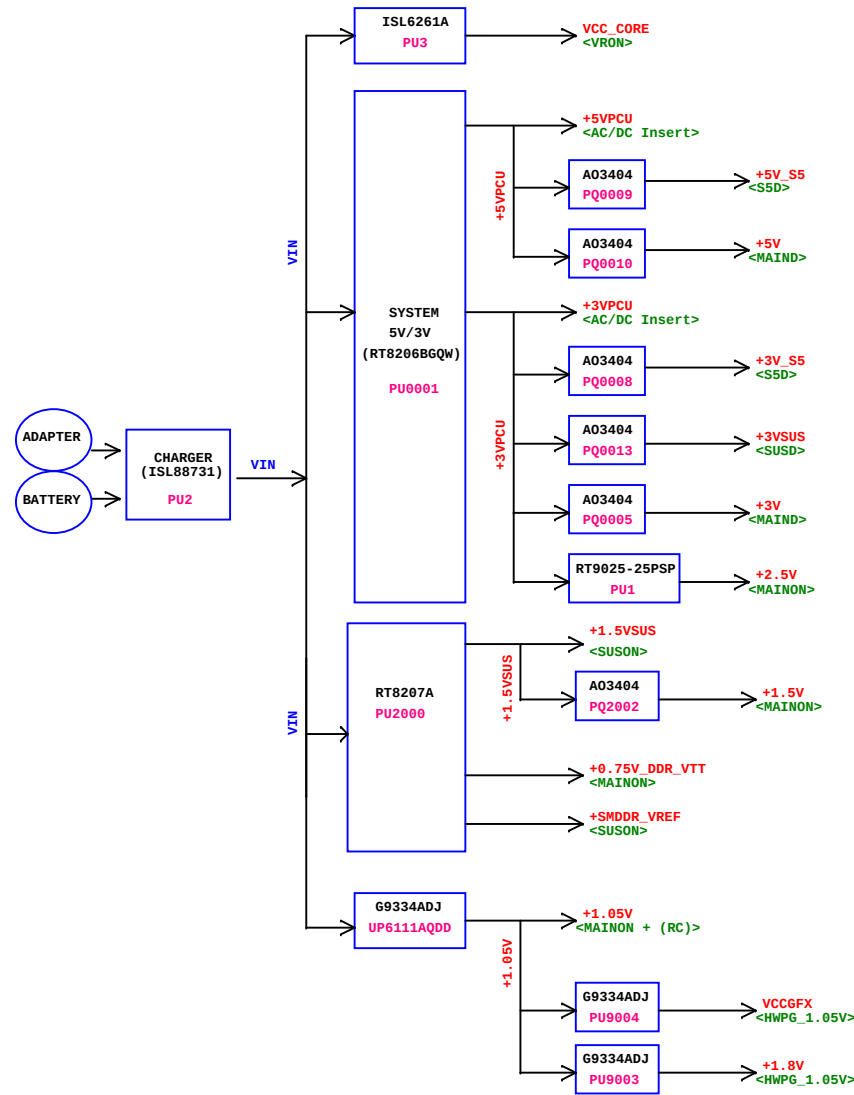
Rev

1A

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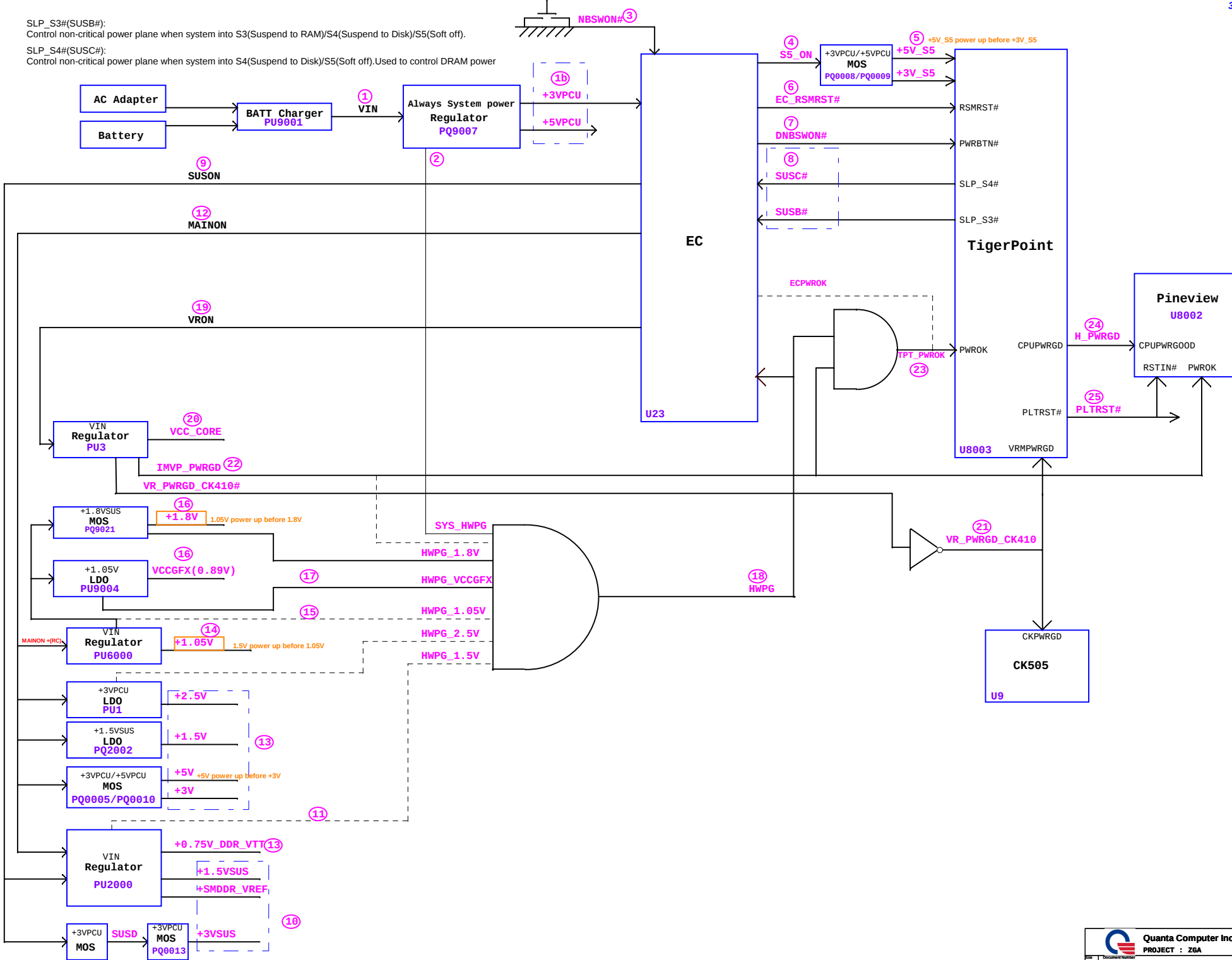




POWER	Distribution
VIN	LCD Backlight
VCC_CORE	CPU
+5VPCU	USB Connector
+5V_S5	RTC, TPT
+5V	TPT , CRT , TouchPad , Codec , SATA , FAN , HDMI
+3VPCU	RTC, Hall Sensor, Light Sensor, EC, BIOS
+3V_S5	TPT , LAN , LAN EEPROM , RJ45 LED
+3VSUS	3G
+3V	CLK_GEN, CPU, TPT , LCD , CCD, DMIC, BT, Codec, WLAN/Wimax, Card reader, EC, DDR, HDMI
+1.5VSUS	DDR
+1.8V	CPU, HDMI
+1.5V	CPU, TPT
+0.75V_DDR_VTT	DDR
+SMDDR_VREF	CPU, DDR
+1.05V	CLK_GEN , CPU, TPT
VCCGFX	CPU
+2.5V	HDMI

SLP_S3#(SUSB#):
Control non-critical power plane when system into S3(Suspend to RAM)/S4(Suspend to Disk)/S5(Soft off).

SLP_S4#(SUSC#):
Control non-critical power plane when system into S4(Suspend to Disk)/S5(Soft off).Used to control DRAM power



[illegible]