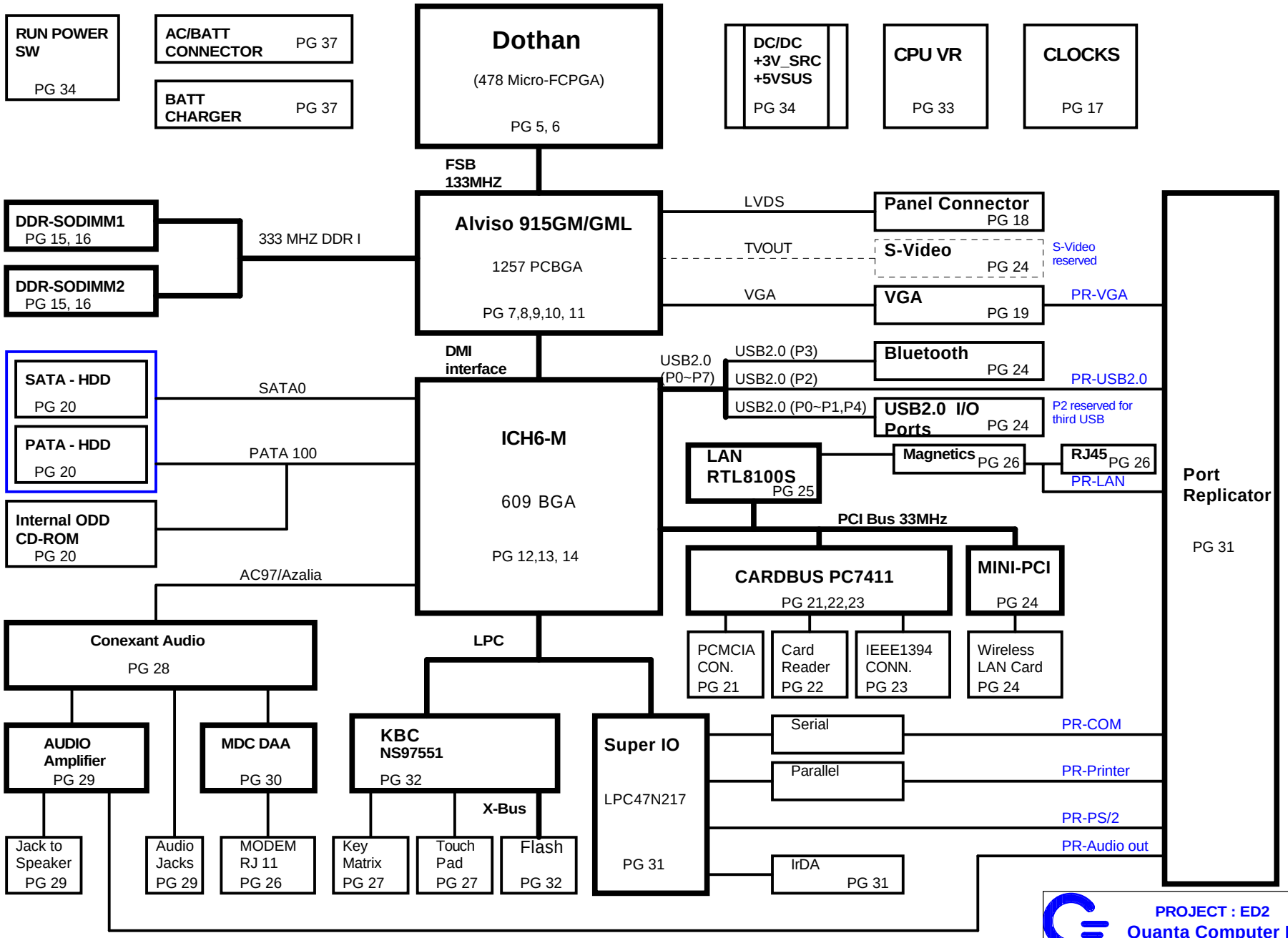
ED2-UMA DESIGN

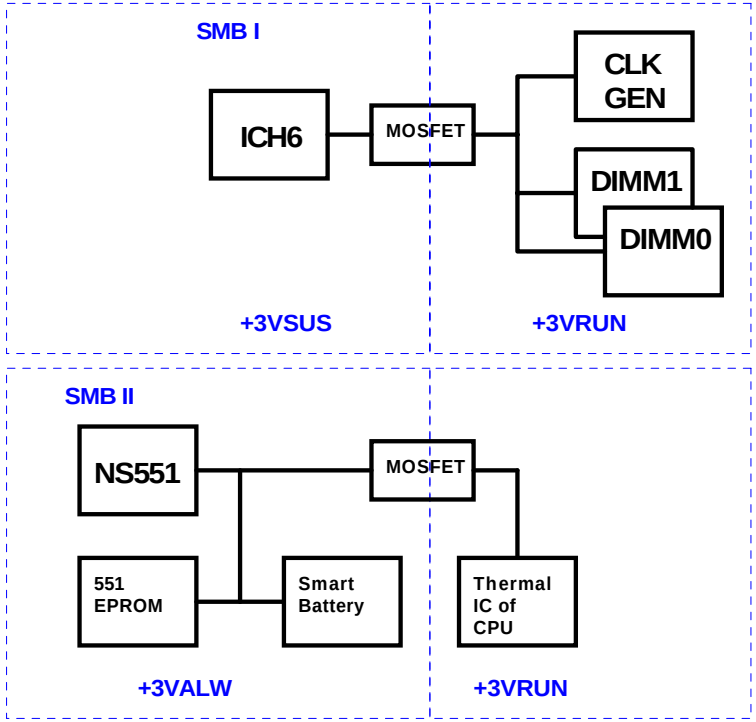
VER : 1C



PROJECT : ED2
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram 1	C2A
Date: Friday, October 22, 2004	Sheet 1 of 38	

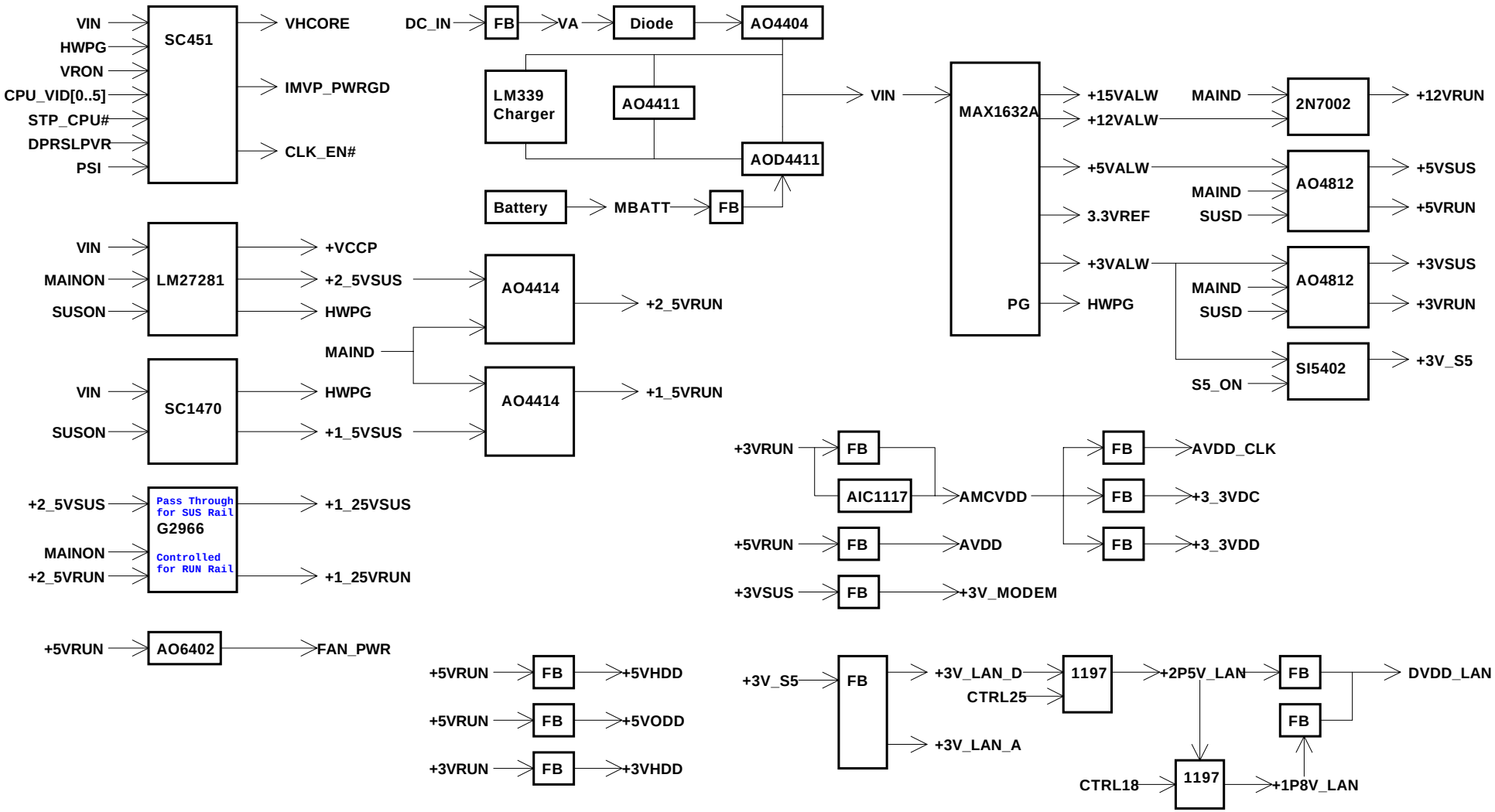
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD24	PIRQA#	RTL8110S
REQ2# / GNT2#	AD19	PIRQB# , PIRQD#	MINI-PCI
REQ1# / GNT1#	AD17	PIRQC#,PIRQD#,PIRQA#	TI 7411



PROJECT : ED2
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram 2	C2A
Date: Friday, October 22, 2004	Sheet 2 of 38	

Power Rail Flow



PROJECT : ED2
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram 3	C2A
Date: Friday, October 22, 2004	Sheet 3 of 38	

INDEX

Power and Ground

New Label	NOTE	Description	Control Signal or Source
VA		AC ADAPTER (20V)	
VIN		MAIN POWER (10~20V)	
MBATT		MAIN BATTERY + (10~17V)	
+15VALW		+15V ALWAYS	
+12VALW		+12V ALWAYS	
+12VRUN		+12V RUN	MAINON
+5VALW		+5V ALWAYS & KBC POWER	
+5V_S5	NO USE	THIS POWER WILL BE TUNEED OFF IN S5 BATTERY MODE	S5_ON
+5VSUS		+5V S5 CONTROLED POWER	SUSD
+5VRUN		+5V S3 CONTROLED POWER	MAIND
+5VHDD	CONNECT TO +5VRUN DIRECTLY	+5V HDD POWER	+5VHDD_EN#
+5VODD	CONNECT TO +5VRUN DIRECTLY	+5V ODD POWER	+5VMOD_EN#
+5VFDD	NO USE	EXTERNAL FDD POWER (5V)	+5VFDD_EN#
FAN_PWR		FAN POWER (5V)	VFAN, MAX6657_OV#
VDDA		Amplifier Power 5V RUN Plane	+5VRUN
AMCVDD		AC97 Code DAC Power 3VRUN	+3VSUS
3V_MODEM		MODEM Power 3VSUS	+5VRUN or +3VRUN
+3VALW		8051 POWER (3V)	
+3V_S5		THIS POWER WILL BE TUNEED OFF IN S5 BATTERY MODE	S5_ON
+3VSUS		SLP_S5# CTRLD POWER	SUSD
+3VRUN		SLP_S3# CTRLD POWER	MAIND
+3VHDD	CONNECT TO +3VRUN DIRECTLY	SATA HDD Power	+3VHDD_EN#
+3V_LAN_D		LAN Digital Power	+3V_S5
+3V_LAN_A		LAN Analog Power	+3V_S5
+2P5V_LAN		LAN Analog Power	+3V_LAN_D (+3V_S5)
DVDD_LAN		LAN Digital Power 1.8 or 2.5V	+2P5V_LAN(+3V_S5)
RTCVCC		RTC & PCL POWER	
REF3V			
+2_5VSUS			SUSON
+2_5VRUN			MAIND
+1_8VSUS	NO USE		
+1_8VRUN	NO USE		+2_5VRUN
+1_8V_M24	NO USE		+1_8VSUS or +1_8VRUN
+1_5V_S5		THIS POWER WILL BE TUNEED OFF IN S5 BATTERY MODE	S5_ON
+1_5VSUS			SUSON
+1_5VRUN		AGP I/O POWER	MAIND
+1_25VSUS		SMDDR_VTERM	+2_5VSUS
+1_25VRUN			MAINON
VGA1_2V	NO USE	ATI VGA 1.2V	+2_5VRUN
VGACORE	NO USE	ATI VGA CORE 1.0/1.2V	MAINON, POW_SW
+VCCP		AGTL+ POWER (1.05V)	MAINON
VHCORE		CPU CORE POWER (1.25/1.15V)	VR_ON, HWPG
GND	ALL PAGES	DIGITAL GROUND	
AGND	Page 28,29	AUDIO GND	
GNDP	NO USE	CPU POWER GND	
CGNDP	NO USE	CHARGER GND	
DC_GND	DC Jcak	DC/DC POWER GND	
LANGND	NO USE	COMBO CONN GND	

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Quanta Computer Inc.

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CT_0505: Change footprint to BGA479M-SOCKET from L100505 from MPGA479M

U31A

Dothan

1 OF 3

HA#[3..31] → HA#[3..31] → A3# A4# A5# A6# A7# A8# A9# A10# A11# A12# A13# A14# A15# A16# A17# A18# A19# A20# A21# A22# A23# A24# A25# A26# A27# A28# A29# A30# A31#

REQUEST PHASE SIGNALS

DATA PHASE SIGNALS

HD#[0..63] → HD#[0..63] 7

D0# HD#0 … D63# HD#63

ADSTB0# ADSTB1#

REQ0# REQ1# REQ2# REQ3# REQ4#

ERROR SIGNALS

ADS# IERR#

ARBITRATION PHASE SIGNALS

BREQ0# BPRI# BNR# LOCK#

SNOOP PHASE SIGNALS

HIT# HITM# DEFER#

RESPONSE PHASE SIGNALS

BPM0# BPM1# BPM2# BPM3# TRDY# RS0# RS1# RS2#

PC COMPATIBILITY SIGNALS

A20M# FERR# IGNNE# PWRGOOD SMI#

DIAGNOSTIC & TEST SIGNALS

TCK TDO TDI TMS TRST# ITP_CLK0 ITP_CLK1 PREQ# PRDY# DBR#

EXECUTION CONTROL SIGNALS

LINT0 LINT1 STPCLK# SLP# DPSLP# DPRSTP#

THERMDA THERMDC

THERMAL DIODE

THERMTRIP# PROCHOT#

DSTBN0# DSTBP0# DSTBN1# DSTBP1# DSTBN2# DSTBP2# DSTBN3# DSTBP3#

DINV0# DINV1# DINV2# DINV3#

DBSY# DRDY#

BCLK1 BCLK0

INIT# RESET# DPWR#

Dothan Processor

G1: NC for Dothan and DPRSTP# for Yonah

+3VRUN

R68 47

C83 .1U/10V_4

15 MIL

3V_THM

THERMDC

THERMDA

C86 2200P

10 mil trace / 10 mil space

U18 MAX6657

VCC DXN DXP -OVT SMDATA SMCLK -ALT GND

KBSMDAT KBSMCLK

R69 10K-0402

R66 10K-0402

Q14 2N7002

Q13 2N7002

MBDATA MBCLK

R71

THRM# 13

MAX6657_AL# 32

R72 10K-0402

R310 10K-0402

MAX6657_OV# 27,34

Item9

ITP disable guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the CPU
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the CPU
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the CPU
TCK	27 ohm +/- 5%	GND	Within 2.0" of the CPU
TDO	Open	VTT	Within 2.0" of the CPU

Note: Populate R58, R62 when ITP connector is populated.

+VCCP

FERR# R60 56_4

IERR# R319 56_4

CPUPWRGD R58 200/F

TCK TRST# R315 27.4/F R62 680

+3VSUS

DBR# R318 150/F_4

+VCCP

R317 54.9/F R316 54.9/F R56 39.2/F R57 150/F_4

TDI TMS TDO CPURST#

PROJECT : ED2

Quanta Computer Inc.

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	Dothan (HOST)	C2A

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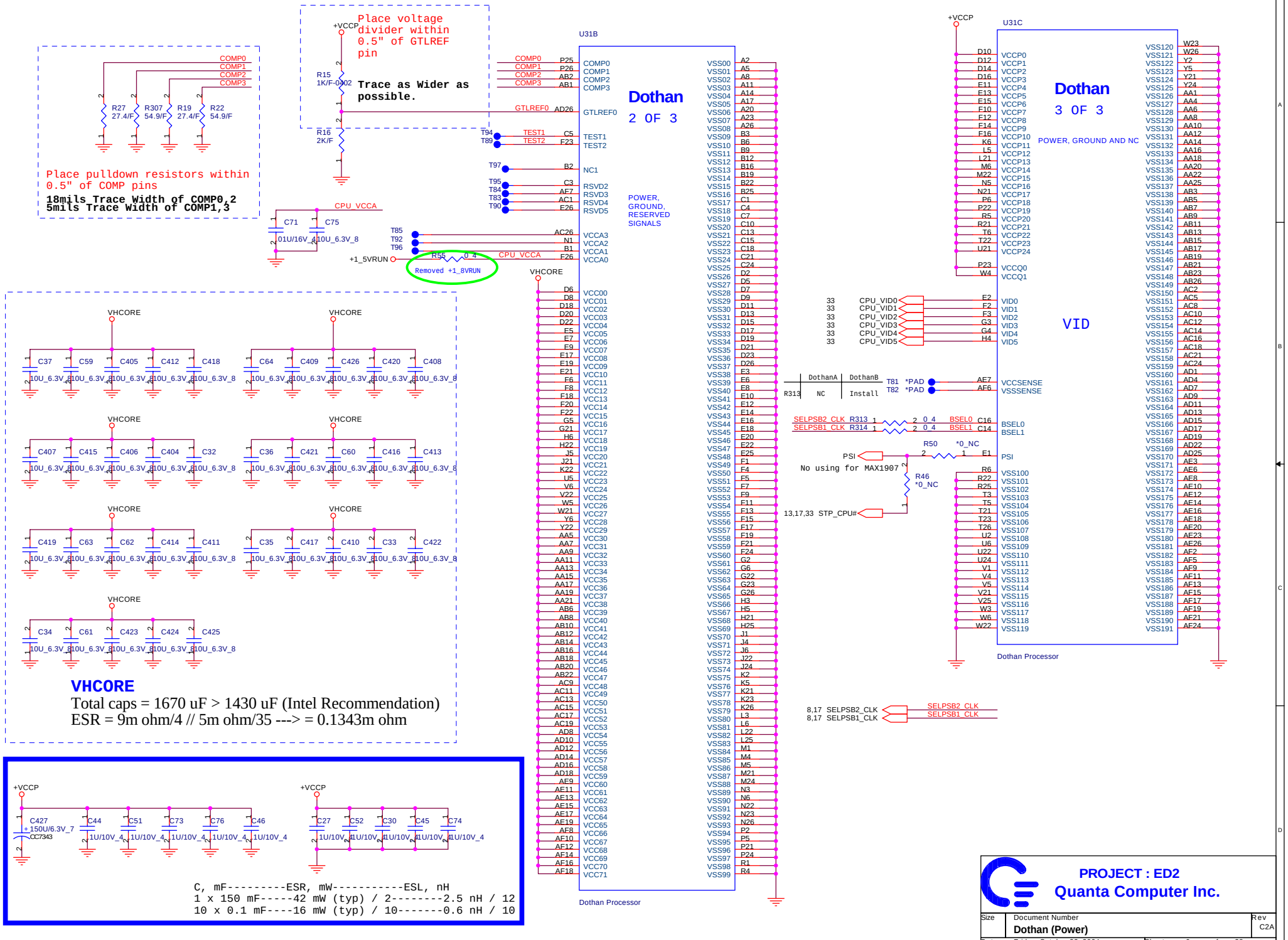
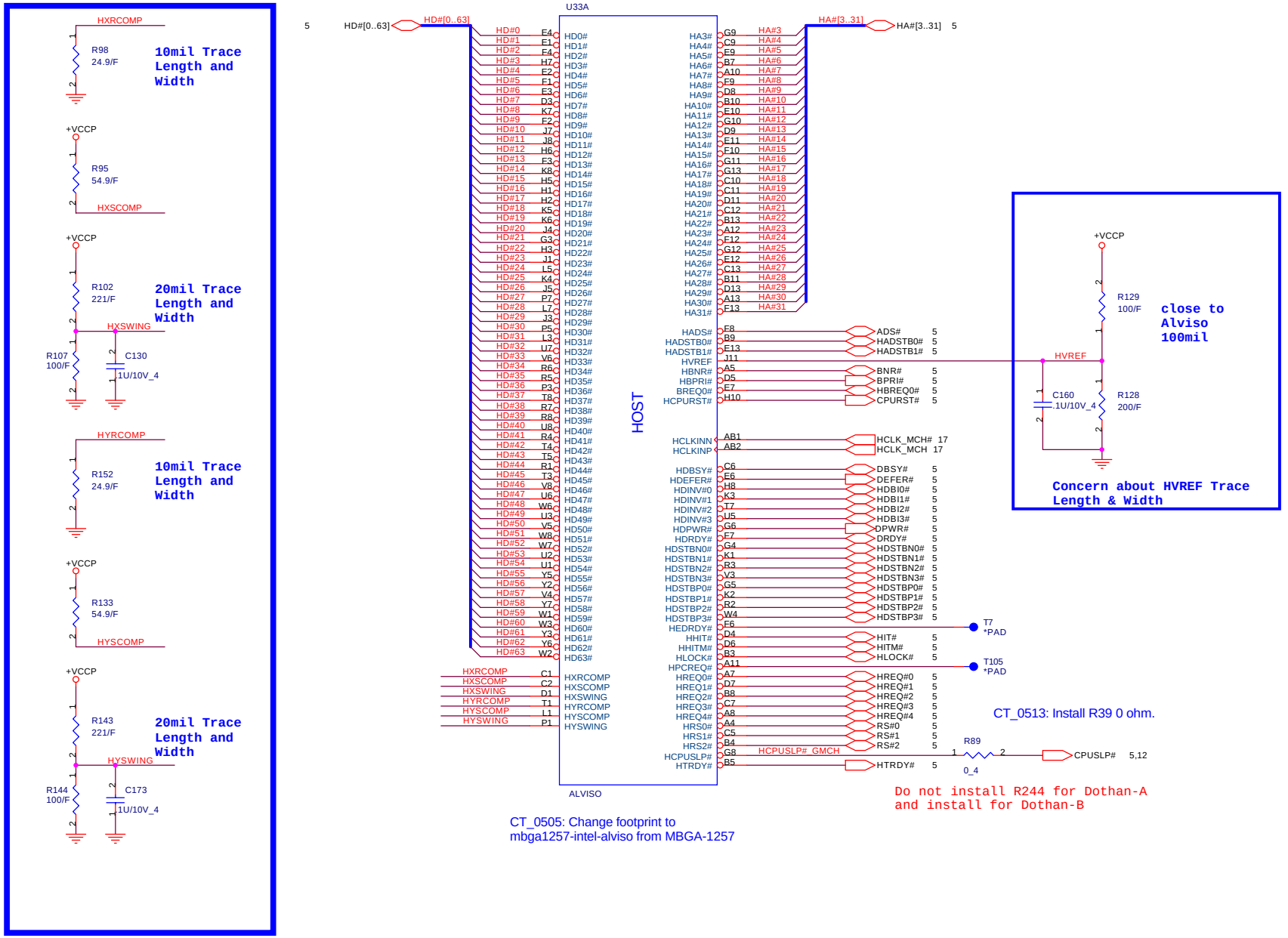

Place pulldown resistors within 0.5" of COMP pins
18mils Trace Width of COMP0,2
5mils Trace Width of COMP1,3
COMP0
COMP1
COMP2
COMP3
R27 27.4/F
R307 54.9/F
R19 27.4/F
R22 54.9/F
Place voltage divider within 0.5" of GTLREF pin
Trace as Wider as possible.
+VCCP
R15 1K/F-0402
R16 2K/F
GTLREF0
CPU_VCCA
C71 01U/16V_4
C75 10U_6.3V_8
+1_5VRUN
R55 0_4
Removed +1_8VRUN
U31B
Dothan
2 OF 3
POWER, GROUND, RESERVED SIGNALS
TEST1
TEST2
NC1
RSVD2
RSVD3
RSVD4
RSVD5
VCCA3
VCCA2
VCCA1
VCCA0
VHCORE
VCC00
VCC01
VCC02
VCC03
VCC04
VCC05
VCC06
VCC07
VCC08
VCC09
VCC10
VCC11
VCC12
VCC13
VCC14
VCC15
VCC16
VCC17
VCC18
VCC19
VCC20
VCC21
VCC22
VCC23
VCC24
VCC25
VCC26
VCC27
VCC28
VCC29
VCC30
VCC31
VCC32
VCC33
VCC34
VCC35
VCC36
VCC37
VCC38
VCC39
VCC40
VCC41
VCC42
VCC43
VCC44
VCC45
VCC46
VCC47
VCC48
VCC49
VCC50
VCC51
VCC52
VCC53
VCC54
VCC55
VCC56
VCC57
VCC58
VCC59
VCC60
VCC61
VCC62
VCC63
VCC64
VCC65
VCC66
VCC67
VCC68
VCC69
VCC70
VCC71
Dothan Processor
U31C
Dothan
3 OF 3
POWER, GROUND AND NC
VCCP0
VCCP1
VCCP2
VCCP3
VCCP4
VCCP5
VCCP6
VCCP7
VCCP8
VCCP9
VCCP10
VCCP11
VCCP12
VCCP13
VCCP14
VCCP15
VCCP16
VCCP17
VCCP18
VCCP19
VCCP20
VCCP21
VCCP22
VCCP23
VCCP24
VCCQ0
VCCQ1
VID
CPU_VID0
CPU_VID1
CPU_VID2
CPU_VID3
CPU_VID4
CPU_VID5
VID0
VID1
VID2
VID3
VID4
VID5
DothanA
DothanB
R313 NC Install
T81 *PAD
T82 *PAD
VCCSENSE
VSSSENSE
SELPSB2_CLK R313
SELPSB1_CLK R314
BSEL0 C16
BSEL1 C14
PSI
No using for MAX1907
R50 *0_NC
R46 *0_NC
13,17,33 STP_CPU#
8,17 SELPSB2_CLK
8,17 SELPSB1_CLK
Dothan Processor
VHCORE
Total caps = 1670 uF > 1430 uF (Intel Recommendation)
ESR = 9m ohm/4 // 5m ohm/35 ---> = 0.1343m ohm
C427 150U/6.3V_7
CC7343
C, mF---------ESR, mW----------ESL, nH
1 x 150 mF-----42 mW (typ) / 2--------2.5 nH / 12
10 x 0.1 mF----16 mW (typ) / 10-------0.6 nH / 10
PROJECT : ED2
Quanta Computer Inc.
Size
Document Number
Dothan (Power)
Rev
C2A
Date: Friday, October 22, 2004
Sheet 6 of 38

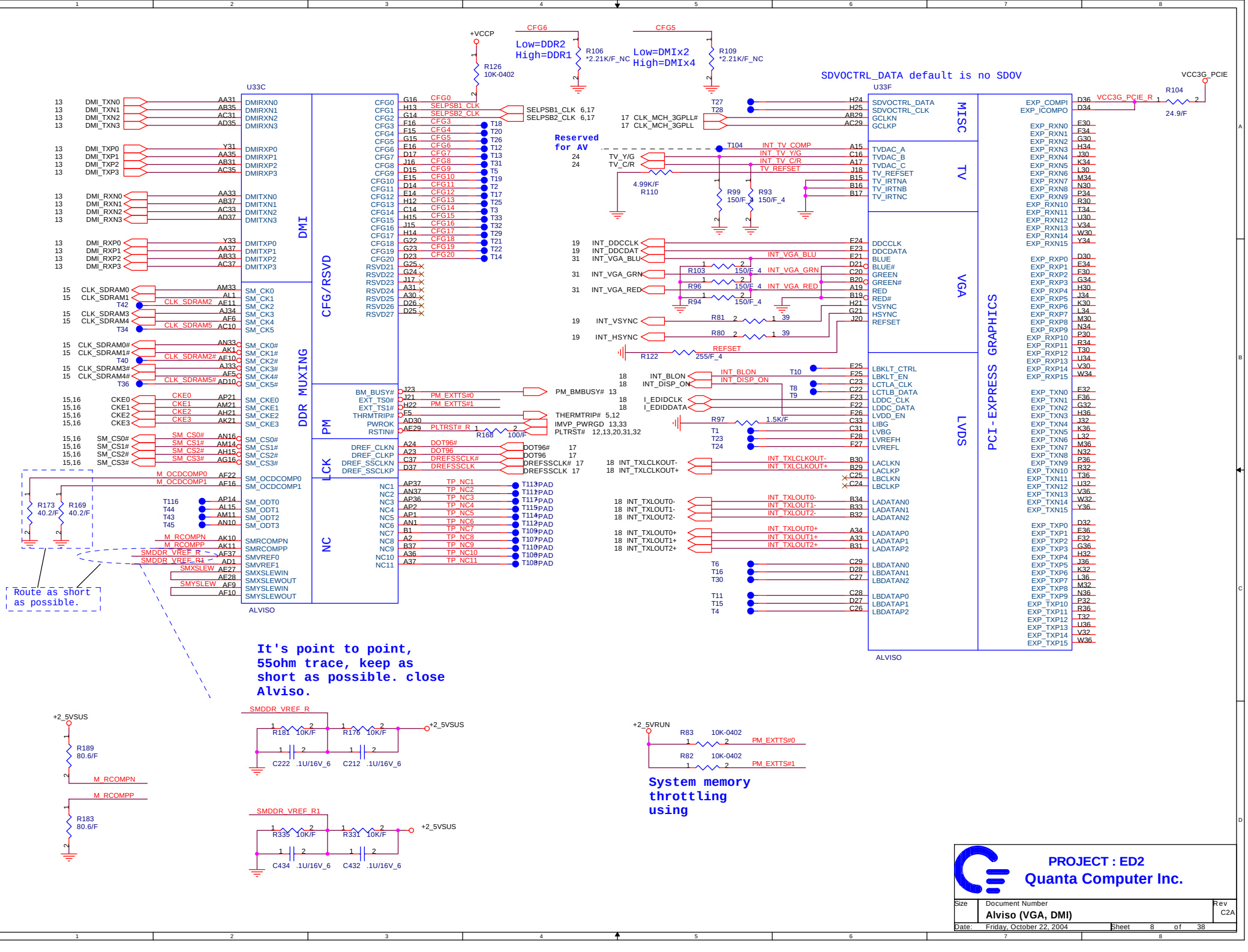


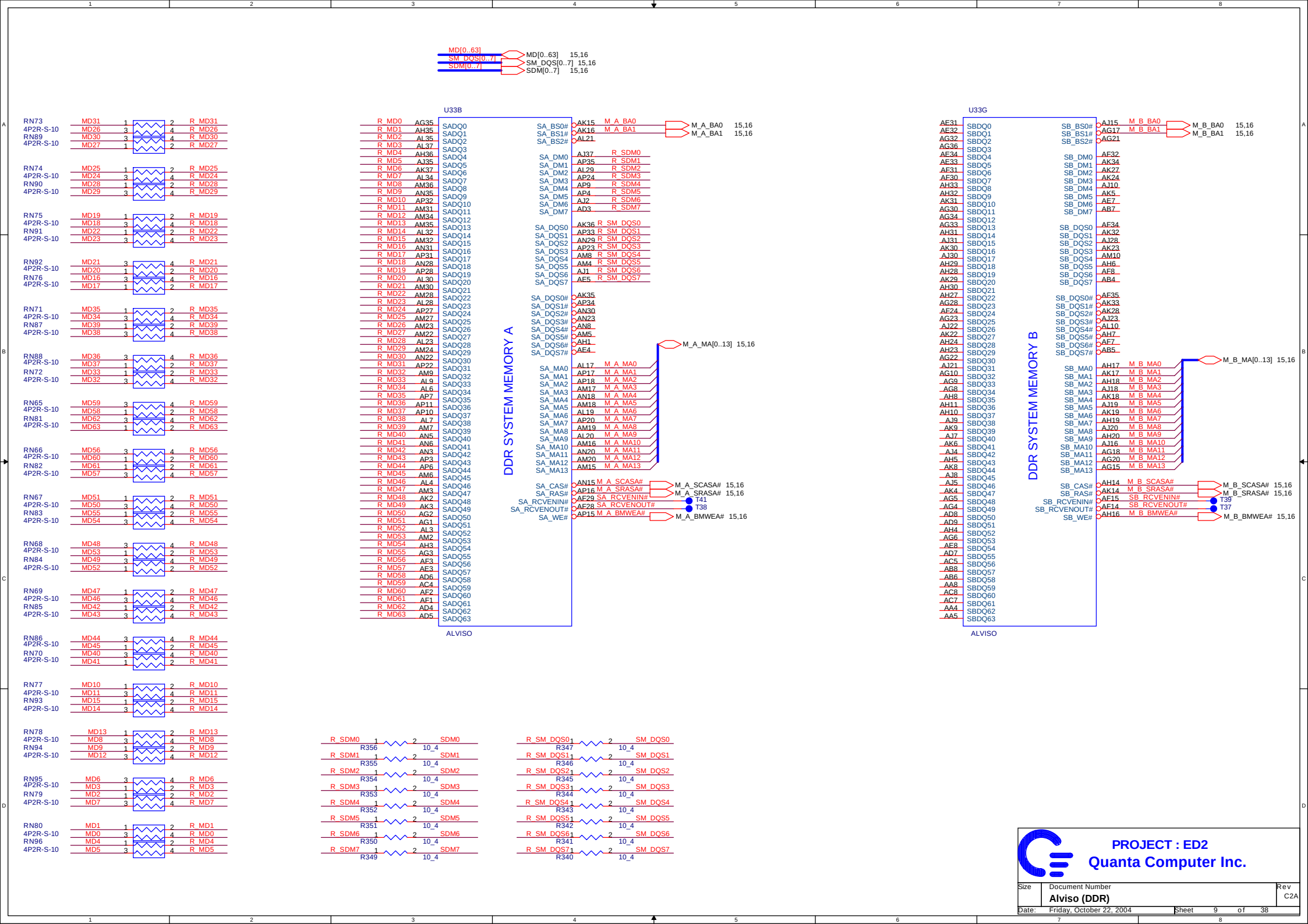
PROJECT : ED2

Quanta Computer Inc.

Size	Document Number	Rev
	Alviso (HOST)	C2A

Date: Friday, October 22, 2004 Sheet 7 of 38


U33C
ALVISO
DMI
DDR MUXING
CFG/RSVD
PM
LCK
NC
U33F
MISC
TV
VGA
LVDS
PCI-EXPRESS GRAPHICS
SDVOCTRL_DATA default is no SDOV
Reserved for AV
Low=DDR2 High=DDR1
Low=DMIx2 High=DMIx4
Route as short as possible.
It's point to point, 55ohm trace, keep as short as possible. close Alviso.
System memory throttling using
PROJECT : ED2
Quanta Computer Inc.
Alviso (VGA, DMI)
Friday, October 22, 2004



PROJECT : ED2

Quanta Computer Inc.

Size	Document Number	Rev
	Alviso (DDR)	C2A
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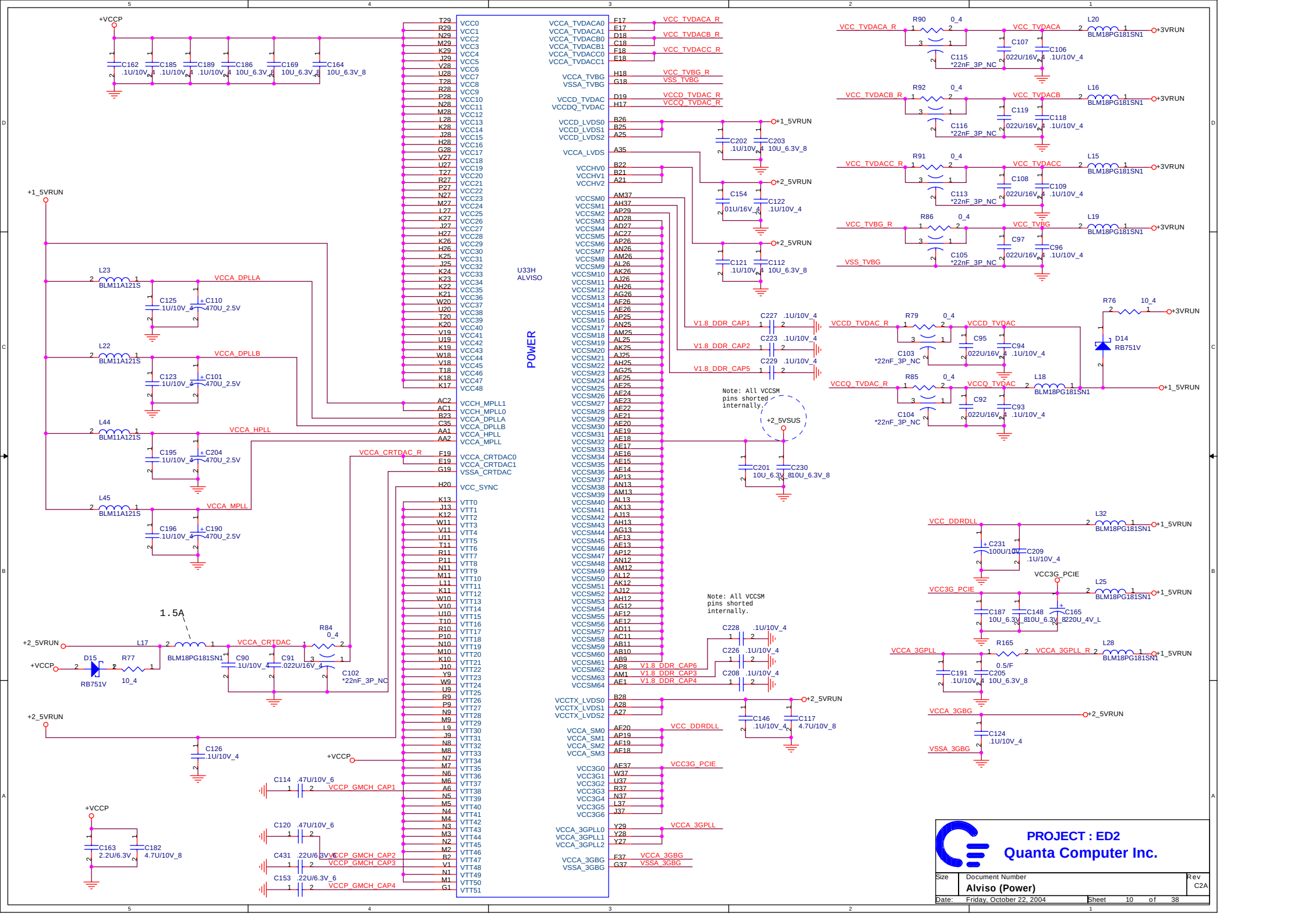
U33H
ALVISO
POWER
Note: All VCCSM pins shorted internally.
Note: All VCCSM pins shorted internally.
1.5A
PROJECT : ED2
Quanta Computer Inc.
Size
Document Number
Alviso (Power)
Rev
C2A
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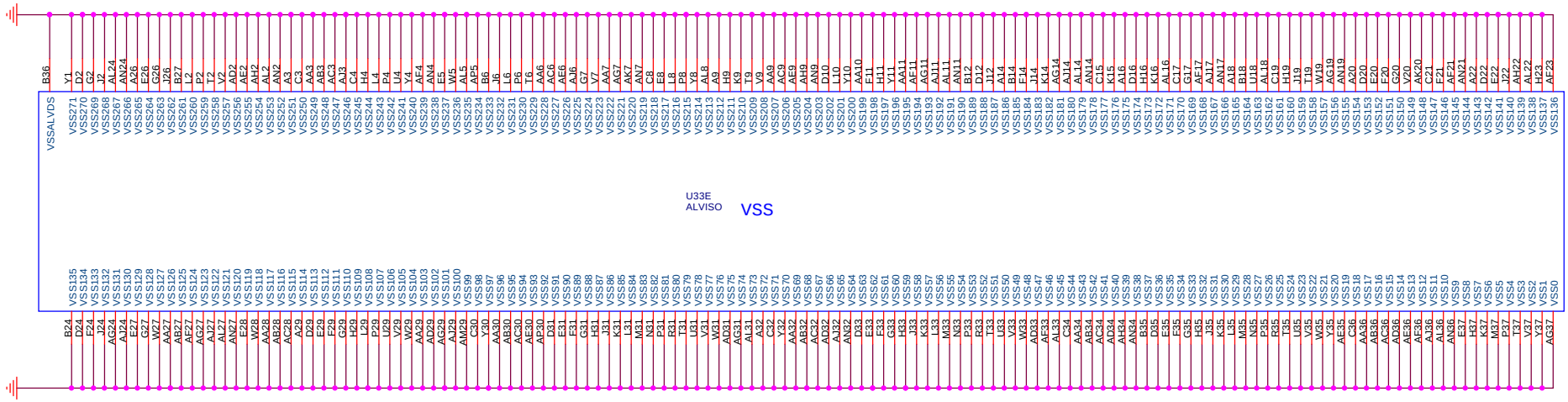

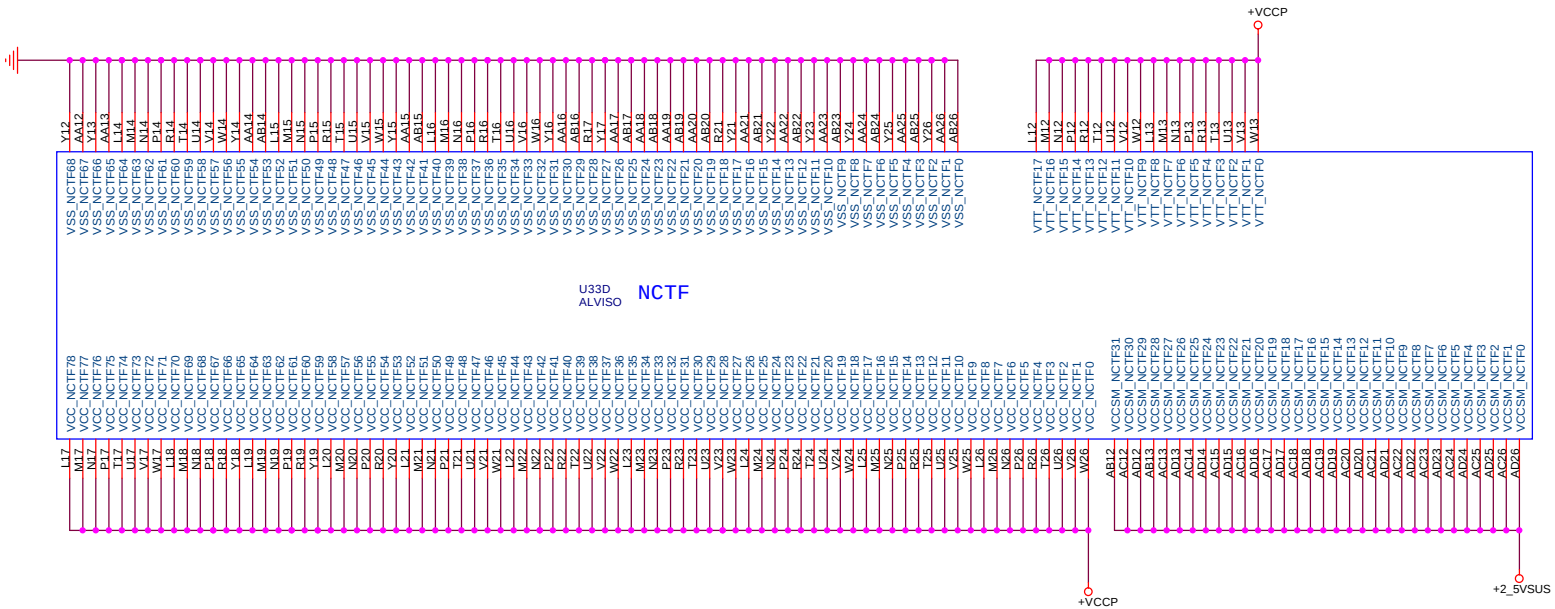

DDRI is 2.5V, DDRII is 1.8V.

PROJECT : ED2

Quanta Computer Inc.

Size	Document Number	Rev
	Alviso (VSS, NCTF0	C2A
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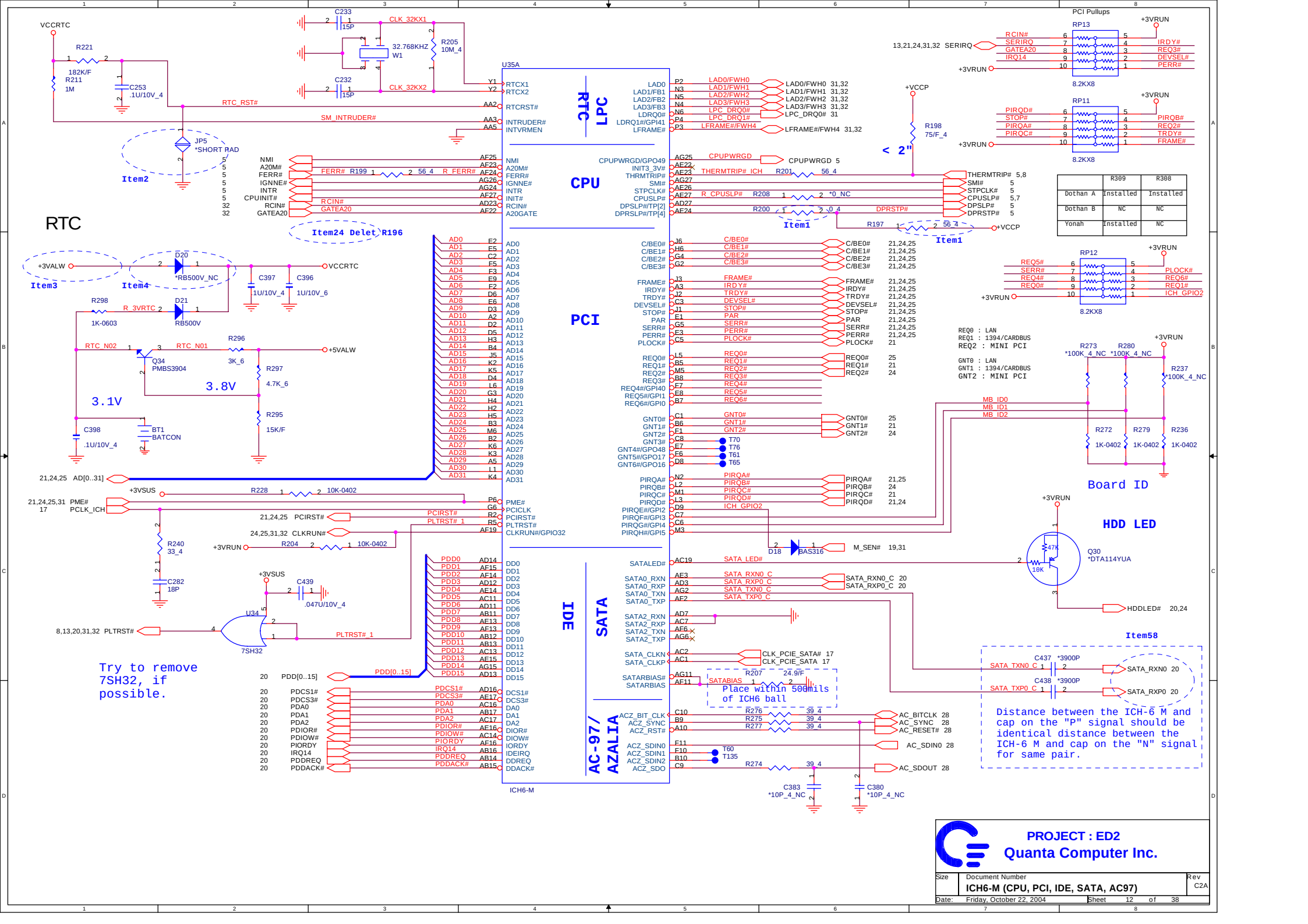
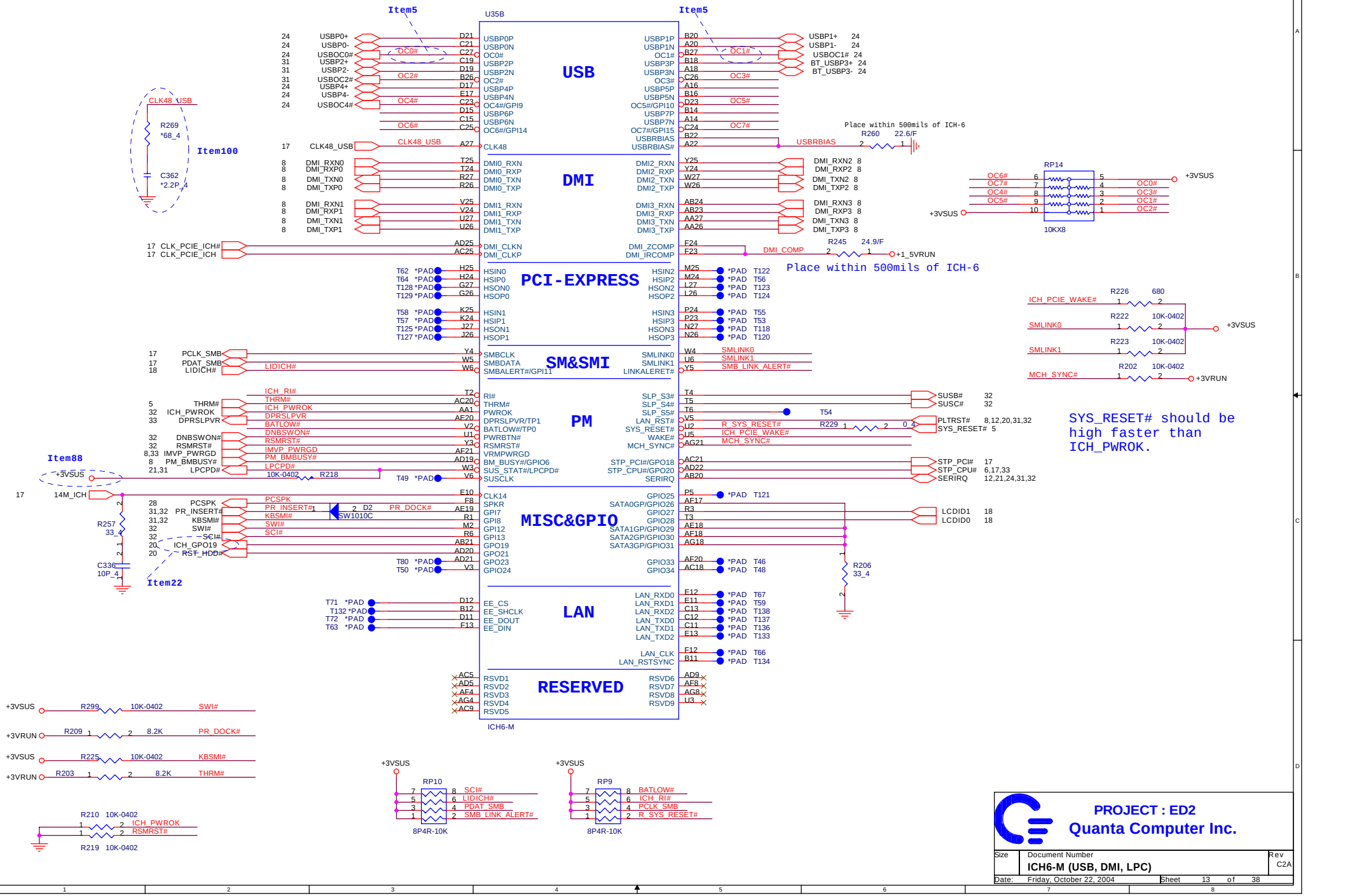

RTC
PCI Pullups
U35A
RTC
LPC
CPU
PCI
IDE
SATA
AC-97/ AZALIA
ICH6-M
Item2
Item24 Delet R196
Item3
Item4
Item1
Item58
3.1V
3.8V
Board ID
HDD LED
Try to remove 7SH32, if possible.
Place within 500mils of ICH6 ball
Distance between the ICH-6 M and cap on the "P" signal should be identical distance between the ICH-6 M and cap on the "N" signal for same pair.
REQ0 : LAN
REQ1 : 1394/CARDBUS
REQ2 : MINI PCI
GNT0 : LAN
GNT1 : 1394/CARDBUS
GNT2 : MINI PCI
PROJECT : ED2
Quanta Computer Inc.
ICH6-M (CPU, PCI, IDE, SATA, AC97)
Friday, October 22, 2004
Sheet 12 of 38


U35B
USB
DMI
PCI-EXPRESS
SM&SMI
PM
MISC&GPIO
LAN
RESERVED
ICH6-M
Item5
Item5
Item100
Item88
Item22
CLK48_USB
R269
*68_4
C362
*2.2P_4
USBP0+
USBP0-
USBOC0#
USBP2+
USBP2-
USBOC2#
USBP4+
USBP4-
USBOC4#
OC0#
OC2#
OC4#
OC6#
USBP0P
USBP0N
OC0#
USBP2P
USBP2N
OC2#
USBP4P
USBP4N
OC4#/GPI9
USBP6P
USBP6N
OC6#/GPI14
CLK48
USBP1P
USBP1N
OC1#
USBP3P
USBP3N
OC3#
USBP5P
USBP5N
OC5#/GPI10
USBP7P
USBP7N
OC7#/GPI15
USBRBIAS
USBRBIAS#
OC1#
OC3#
OC5#
OC7#
USBP1+
USBP1-
USBOC1#
BT_USBP3+
BT_USBP3-
Place within 500mils of ICH-6
R260
22.6/F
DMI_RXN0
DMI_RXP0
DMI_TXN0
DMI_TXP0
DMI_RXN1
DMI_RXP1
DMI_TXN1
DMI_TXP1
DMI0_RXN
DMI0_RXP
DMI0_TXN
DMI0_TXP
DMI1_RXN
DMI1_RXP
DMI1_TXN
DMI1_TXP
DMI2_RXN
DMI2_RXP
DMI2_TXN
DMI2_TXP
DMI3_RXN
DMI3_RXP
DMI3_TXN
DMI3_TXP
DMI_RXN2
DMI_RXP2
DMI_TXN2
DMI_TXP2
DMI_RXN3
DMI_RXP3
DMI_TXN3
DMI_TXP3
RP14
10KX8
+3VSUS
CLK_PCIE_ICH#
CLK_PCIE_ICH
DMI_CLKN
DMI_CLKP
DMI_ZCOMP
DMI_IRCOMP
DMI_COMP
R245
24.9/F
+1_5VRUN
Place within 500mils of ICH-6
HSIN0
HSIP0
HSON0
HSOP0
HSIN1
HSIP1
HSON1
HSOP1
HSIN2
HSIP2
HSON2
HSOP2
HSIN3
HSIP3
HSON3
HSOP3
*PAD
PCLK_SMB
PDAT_SMB
LIDICH#
SMBCLK
SMBDATA
SMBALERT#/GPI11
SMLINK0
SMLINK1
LINKALERT#
SMB_LINK_ALERT#
ICH_PCIE_WAKE#
SMLINK0
SMLINK1
MCH_SYNC#
R226
680
R222
10K-0402
R223
10K-0402
R202
10K-0402
+3VRUN
SYS_RESET# should be high faster than ICH_PWROK.
RI#
THRM#
ICH_PWROK
DPRSLPVR
BATLOW#
DNBSWON#
RSMRST#
IMVP_PWRGD
PM_BMBUSY#
LPCPD#
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
LAN_RST#
SYS_RESET#
WAKE#
MCH_SYNC#
R_SYS_RESET#
R229
ICH_PCIE_WAKE#
SUSB#
SUSC#
PLTRST#
SYS_RESET#
8,12,20,31,32
5
10K-0402
R218
14M_ICH
PCSPK
PR_INSERT#
KBSMI#
SWI#
SCI#
ICH_GPO19
RST_HDD#
SW1010C
PR_DOCK#
R257
33_4
C336
10P_4
CLK14
SPKR
GPI7
GPI8
GPI12
GPI13
GPO19
GPO21
GPO23
GPO24
GPIO25
SATA0GP/GPIO26
GPIO27
GPIO28
SATA1GP/GPIO29
SATA2GP/GPIO30
SATA3GP/GPIO31
GPIO33
GPIO34
STP_PCI#/GPIO18
STP_CPU#/GPO20
SERIRQ
STP_PCI#
STP_CPU#
SERIRQ
6,17,33
12,21,24,31,32
LCDID1
LCDID0
R206
33_4
EE_CS
EE_SHCLK
EE_DOUT
EE_DIN
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
LAN_CLK
LAN_RSTSYNC
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
RSVD7
RSVD8
RSVD9
R299
10K-0402
SWI#
R209
8.2K
PR_DOCK#
R225
10K-0402
KBSMI#
R203
8.2K
THRM#
R210
10K-0402
ICH_PWROK
RSMRST#
R219
10K-0402
RP10
SCI#
LIDICH#
PDAT_SMB
SMB_LINK_ALERT#
8P4R-10K
RP9
BATLOW#
ICH_RI#
PCLK_SMB
R_SYS_RESET#
8P4R-10K
PROJECT : ED2
Quanta Computer Inc.
Size
Document Number
ICH6-M (USB, DMI, LPC)
Rev
C2A
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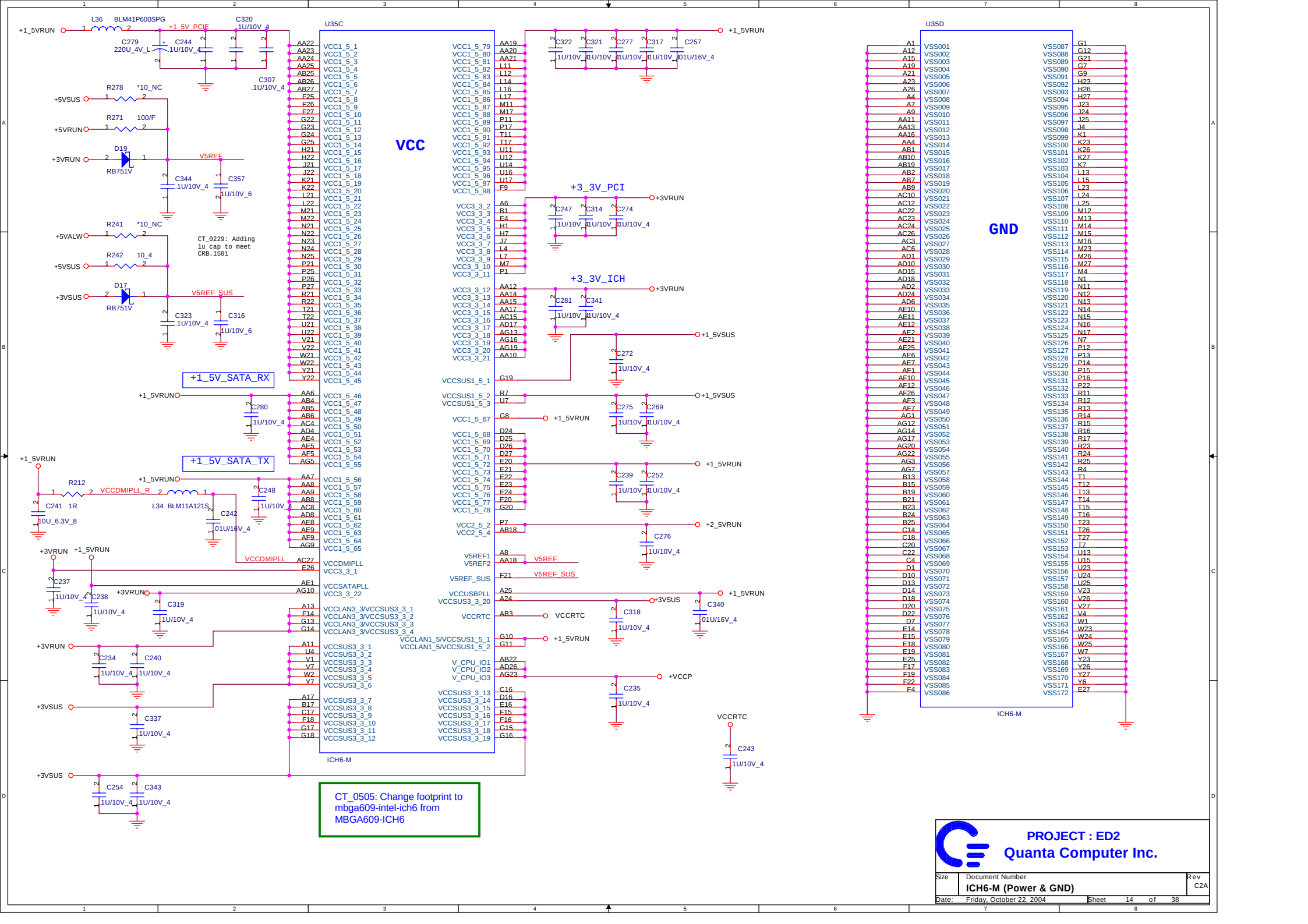
U35C
VCC
ICH6-M
U35D
GND
ICH6-M
+1_5V_SATA_RX
+1_5V_SATA_TX
+3_3V_PCI
+3_3V_ICH
CT_0229: Adding 1u cap to meet CRB.1501
CT_0505: Change footprint to mbga609-intel-ich6 from MBGA609-ICH6
PROJECT : ED2
Quanta Computer Inc.
Size
Document Number
ICH6-M (Power & GND)
Rev
C2A
Date: Friday, October 22, 2004
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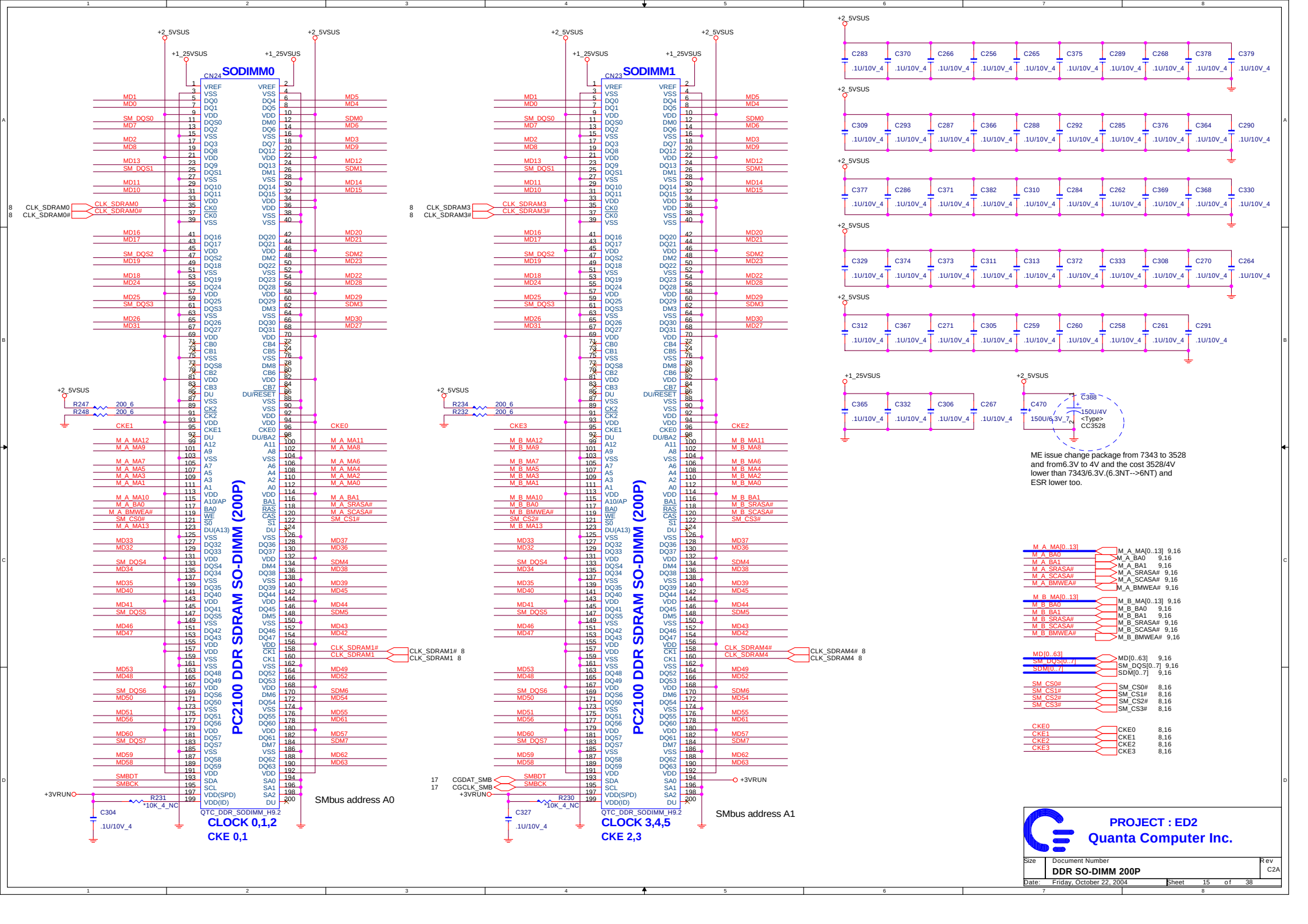
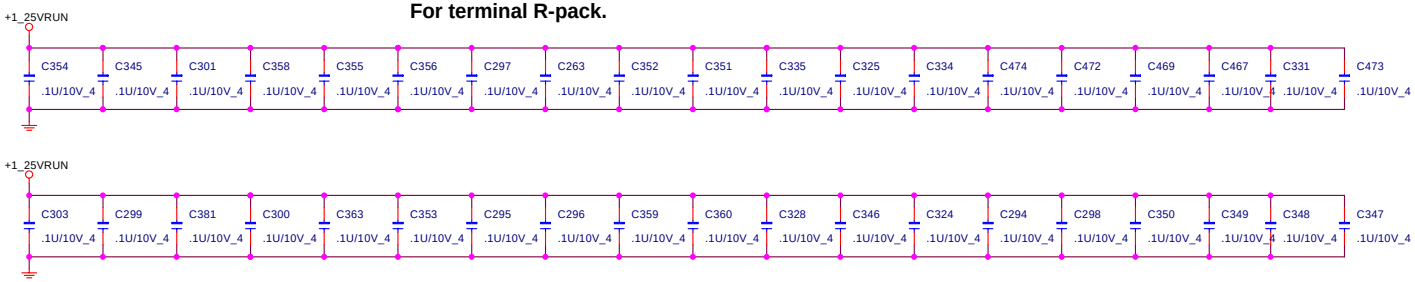
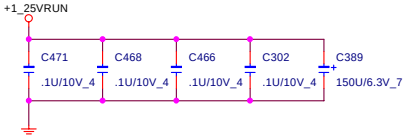
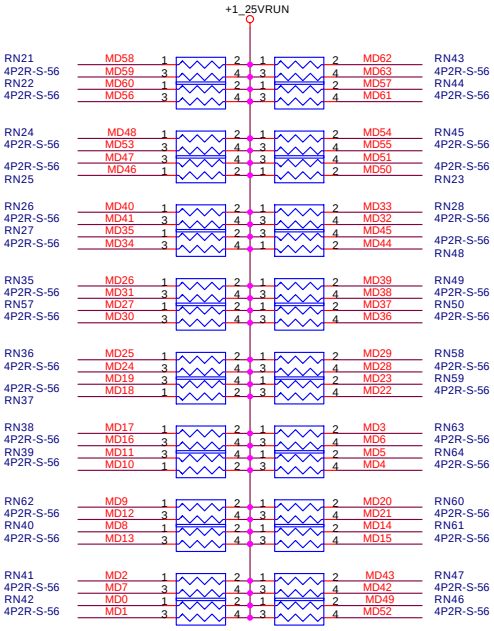
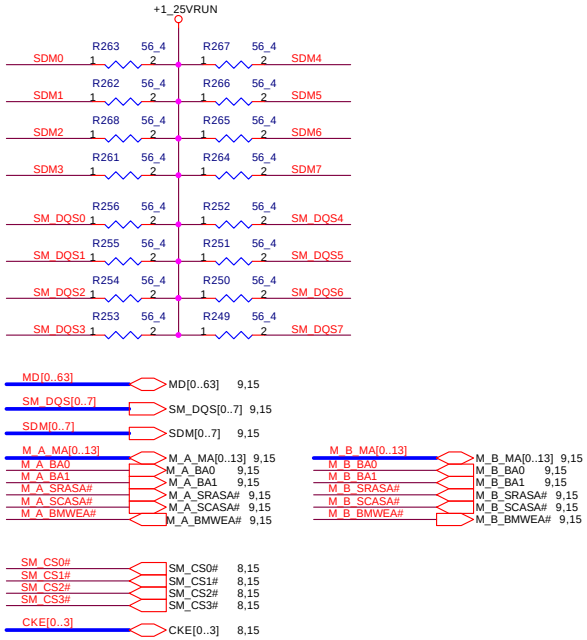

SODIMM0
CN24
PC2100 DDR SDRAM SO-DIMM (200P)
QTC_DDR_SODIMM_H9.2
CLOCK 0,1,2
CKE 0,1
SMbus address A0
SODIMM1
CN23
PC2100 DDR SDRAM SO-DIMM (200P)
QTC_DDR_SODIMM_H9.2
CLOCK 3,4,5
CKE 2,3
SMbus address A1
+2_5VSUS
+1_25VSUS
+3VRUN
CLK_SDRAM0
CLK_SDRAM0#
CLK_SDRAM3
CLK_SDRAM3#
CLK_SDRAM1#
CLK_SDRAM1
CLK_SDRAM4#
CLK_SDRAM4
SMBDT
SMBCK
CGDAT_SMB
CGCLK_SMB
R231 *10K_4_NC
R230 *10K_4_NC
C304 .1U/10V_4
C327 .1U/10V_4
R247 200_6
R248 200_6
R234 200_6
R232 200_6
C283 C370 C266 C256 C265 C375 C289 C268 C378 C379
C309 C293 C287 C366 C288 C292 C285 C376 C364 C290
C377 C286 C371 C382 C310 C284 C262 C369 C368 C330
C329 C374 C373 C311 C313 C372 C333 C308 C270 C264
C312 C367 C271 C305 C259 C260 C258 C261 C291
C365 C332 C306 C267
C470 150U/6.3V_7
C388 150U/4V <Type> CC3528
ME issue change package from 7343 to 3528 and from6.3V to 4V and the cost 3528/4V lower than 7343/6.3V.(6.3NT-->6NT) and ESR lower too.
M_A_MA[0..13]
M_A_BA0
M_A_BA1
M_A_SRASA#
M_A_SCASA#
M_A_BMWEA#
M_B_MA[0..13]
M_B_BA0
M_B_BA1
M_B_SRASA#
M_B_SCASA#
M_B_BMWEA#
MD[0..63]
SM_DQS[0..7]
SDM[0..7]
SM_CS0#
SM_CS1#
SM_CS2#
SM_CS3#
CKE0
CKE1
CKE2
CKE3
PROJECT : ED2
Quanta Computer Inc.
Size
Document Number
DDR SO-DIMM 200P
Rev
C2A
Date: Friday, October 22, 2004
Sheet 15 of 38

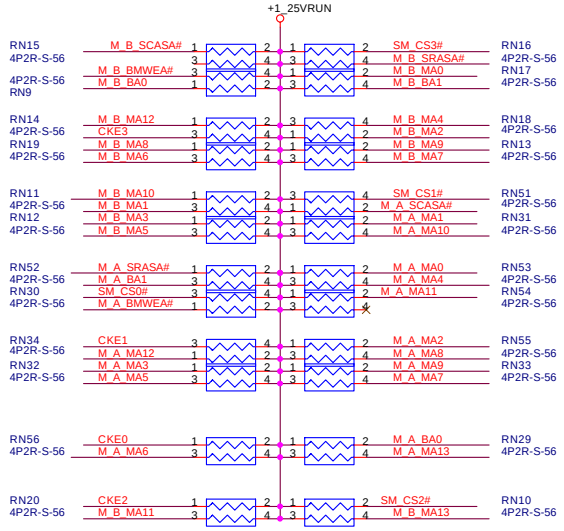
For terminal R-pack.











PROJECT : ED2

Quanta Computer Inc.

Size	Document Number	Rev
	DDR TERMINATION	C2A
Date: Friday, October 22, 2004	Sheet 16 of 38	

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

	DothanA	DothanB
R137	Install	NC
R330	NC	NC

Place these termination to close CK410M. Cause those Pin-out is for Current-Mode.

SMbus address D2

FSB and FSC are directly controlled by Dothan-B

Iref=5mA, Ioh=4*Iref

CK-410M

ICS954206/CY284XX
250mA (MAX.)

CT_0505: Change footprint to TSSOP56-8_1-5 from TSSOP56-240

CK-410M PIN 35,36 Strap Pin. for ITP or PCIE using.

Tie to VCC (Logic 1) is for ITP using.
Tie to GND (Logic 0) is for PCIE using.

Connect ICH6 SMB

Connect DDR Module's SMB

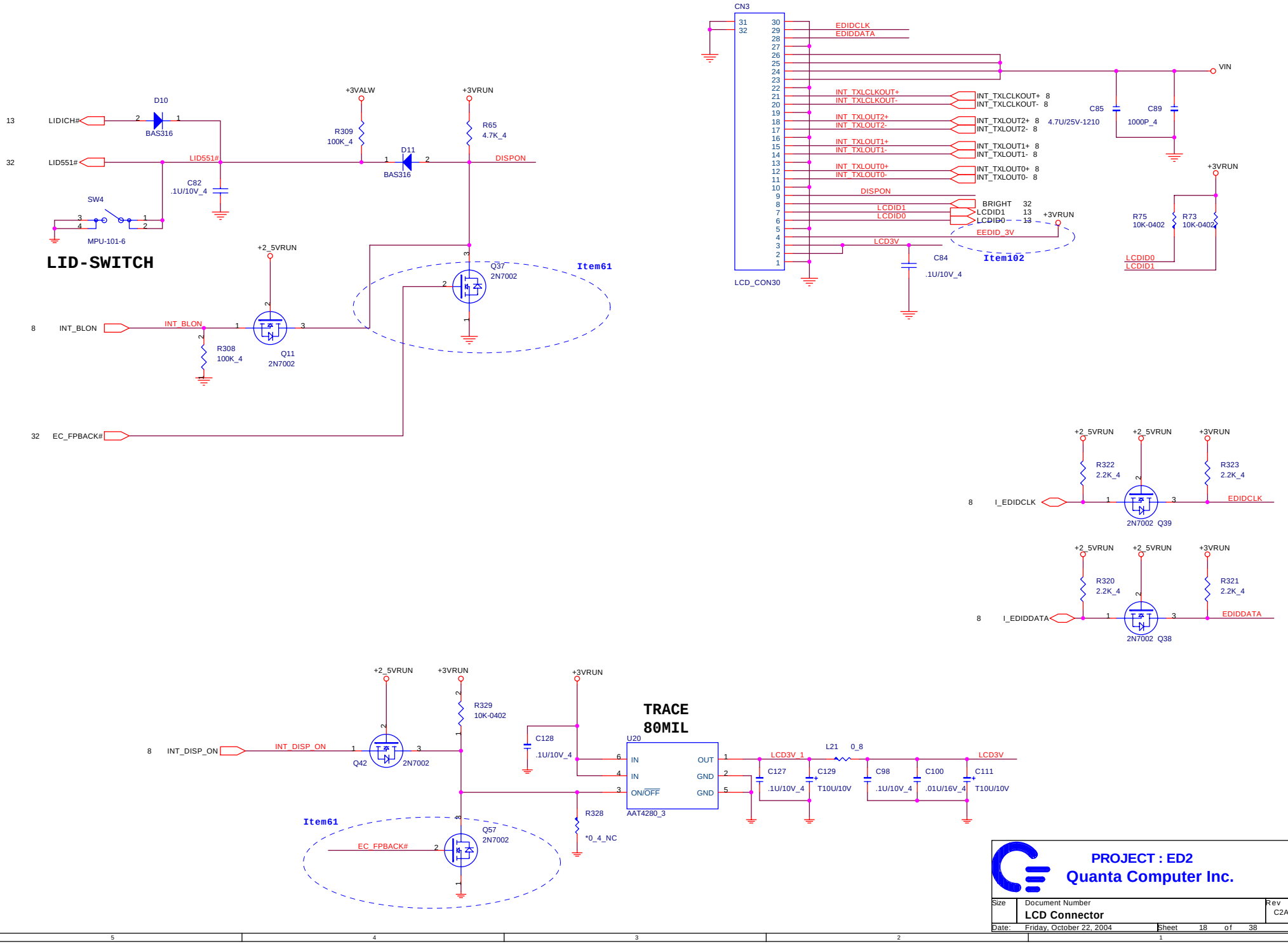
These are for backdrive issue

CT_0229: Change MOS to RHU002N06 due to layout concern.

Bypass CAPs need to follow Bypass CAP. Routing Rule, no vias between CAP to CHIPSET VCC Pin or GND.

Place these termination to close CK410M. Cause those Pin-out is for Current-Mode.

PROJECT : ED2			
Quanta Computer Inc.			
Size	Document Number		Rev
	CLOCK Generator		C2A
Date:	Friday, October 22, 2004	Sheet 17 of 38	


LID-SWITCH
D10
BAS316
LIDICH#
LID551#
SW4
MPU-101-6
C82
.1U/10V_4
+3VALW
R309
100K_4
D11
BAS316
+3VRUN
R65
4.7K_4
DISPON
+2_5VRUN
Q37
2N7002
Item61
INT_BLON
R308
100K_4
Q11
2N7002
EC_FPBACK#
CN3
EDIDCLK
EDIDDATA
INT_TXLCLKOUT+
INT_TXLCLKOUT-
INT_TXLOUT2+
INT_TXLOUT2-
INT_TXLOUT1+
INT_TXLOUT1-
INT_TXLOUT0+
INT_TXLOUT0-
DISPON
LCDID1
LCDID0
LCD3V
LCD_CON30
C84
.1U/10V_4
BRIGHT
EEDID_3V
Item102
VIN
C85
1000P_4
C89
4.7U/25V-1210
R75
10K-0402
R73
10K-0402
I_EDIDCLK
R322
2.2K_4
R323
2.2K_4
2N7002 Q39
I_EDIDDATA
R320
2.2K_4
R321
2.2K_4
2N7002 Q38
INT_DISP_ON
Q42
2N7002
R329
10K-0402
TRACE
80MIL
U20
IN
IN
ON/OFF
OUT
GND
GND
AAT4280_3
C128
.1U/10V_4
LCD3V_1
L21
0_8
C127
.1U/10V_4
C129
T10U/10V
C98
.1U/10V_4
C100
.01U/16V_4
C111
T10U/10V
R328
*0_4_NC
Q57
2N7002
PROJECT : ED2
Quanta Computer Inc.
Size
Document Number
LCD Connector
Rev
C2A
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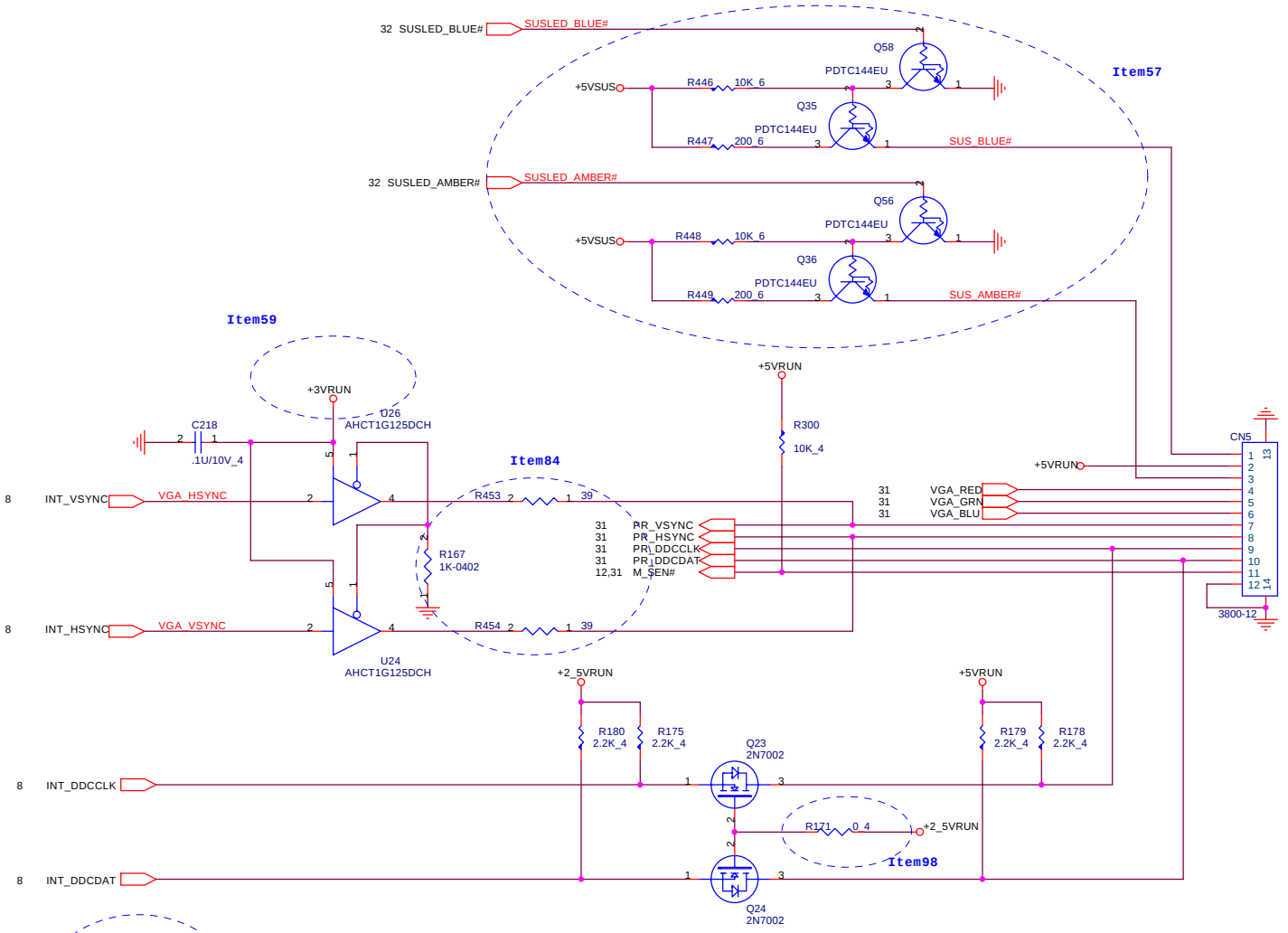
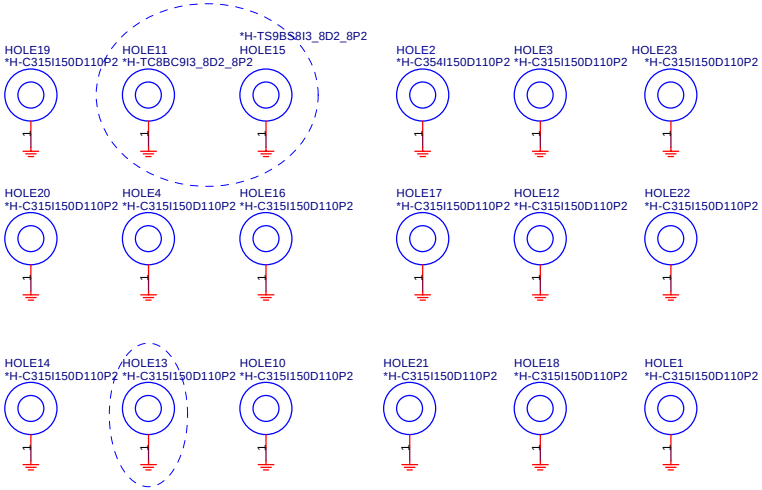
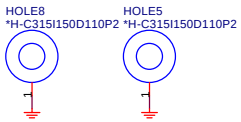
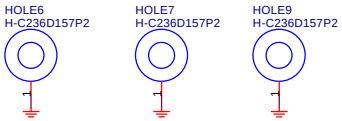


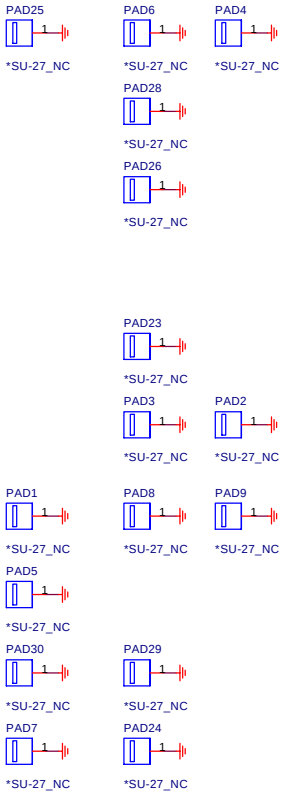


TV-Board fixing Nut



CPU SOCKET

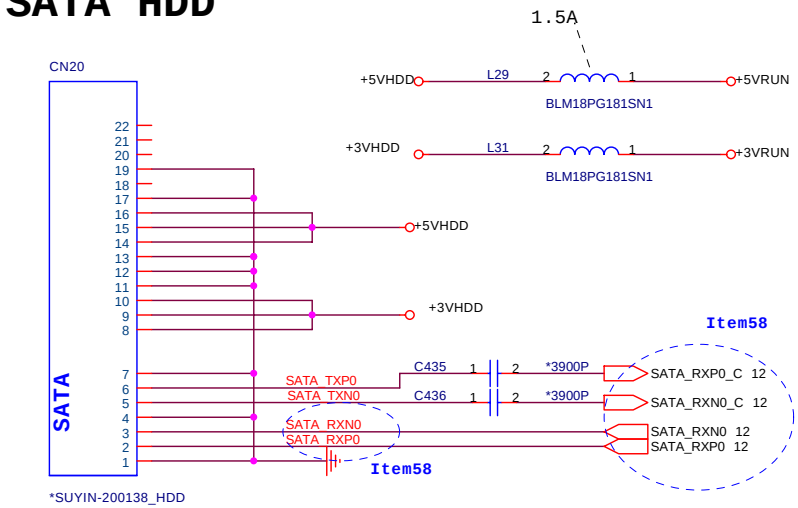


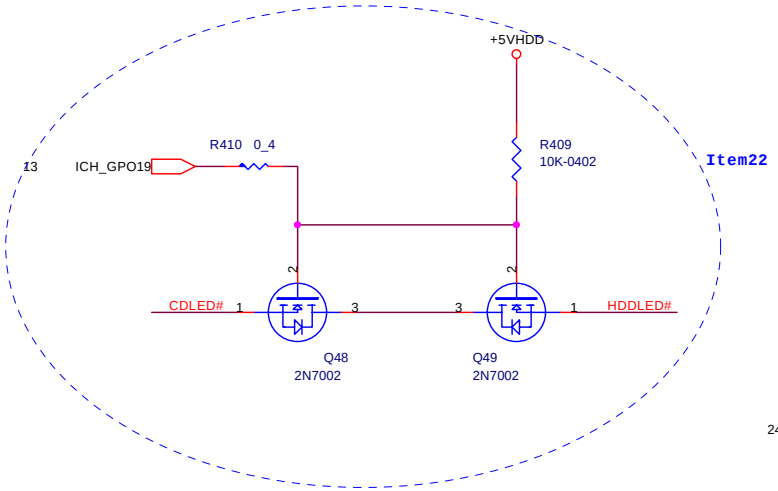


PROJECT : ED2
Quanta Computer Inc.

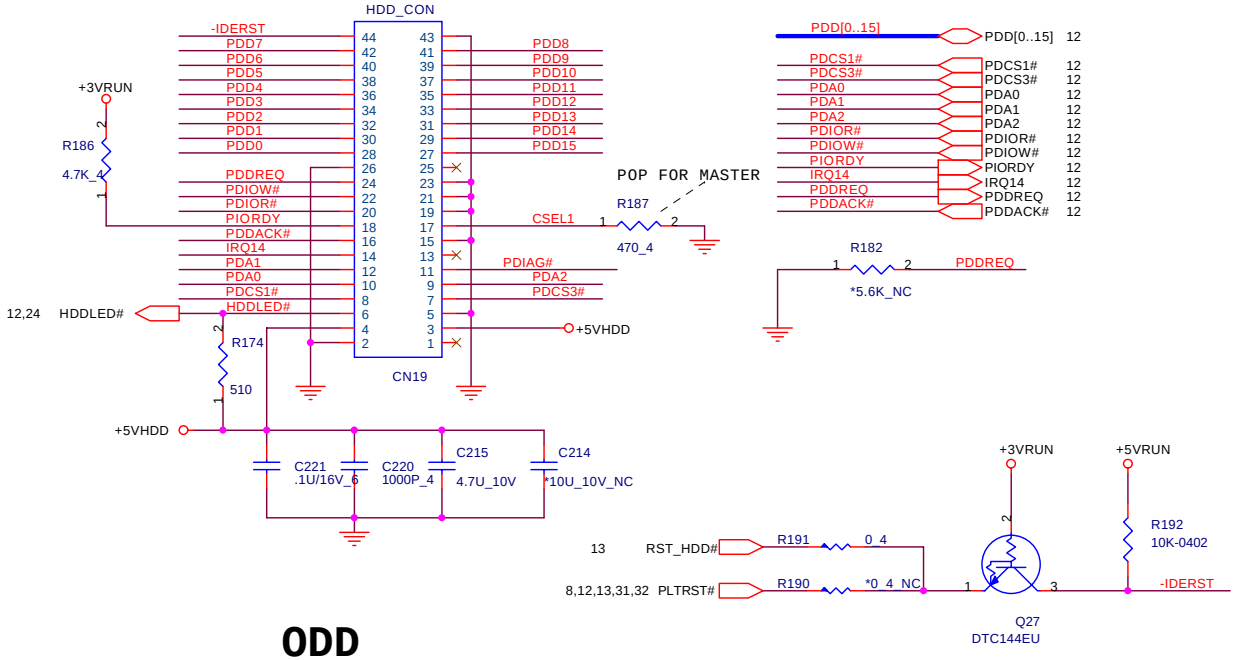
Size	Document Number	Rev
	CRT & TV Connector	C2A
Date: Friday, October 22, 2004	Sheet 19 of 38	

SATA HDD

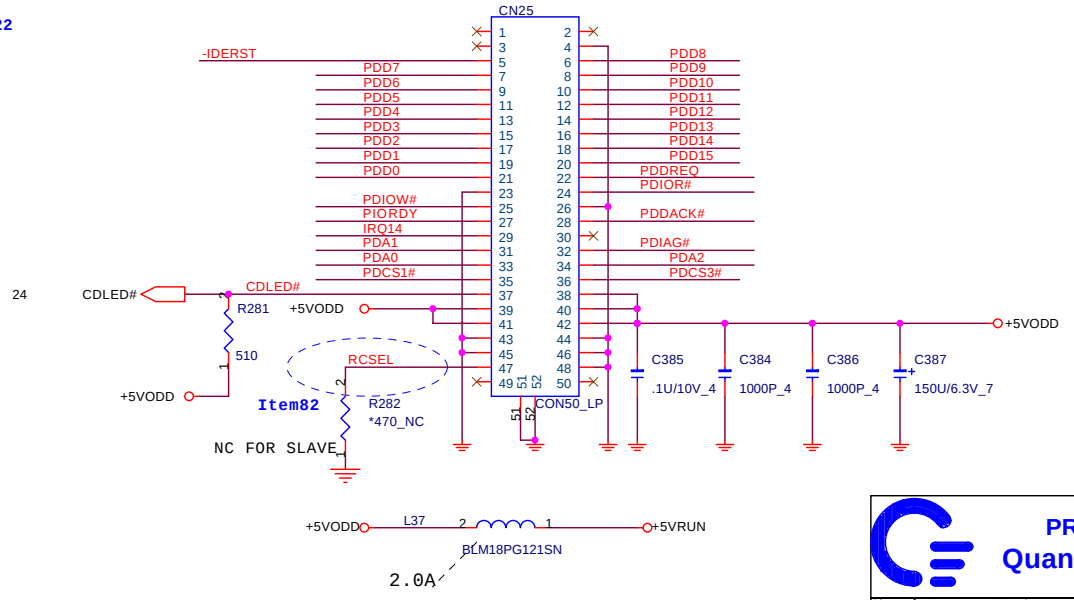




PATA HDD



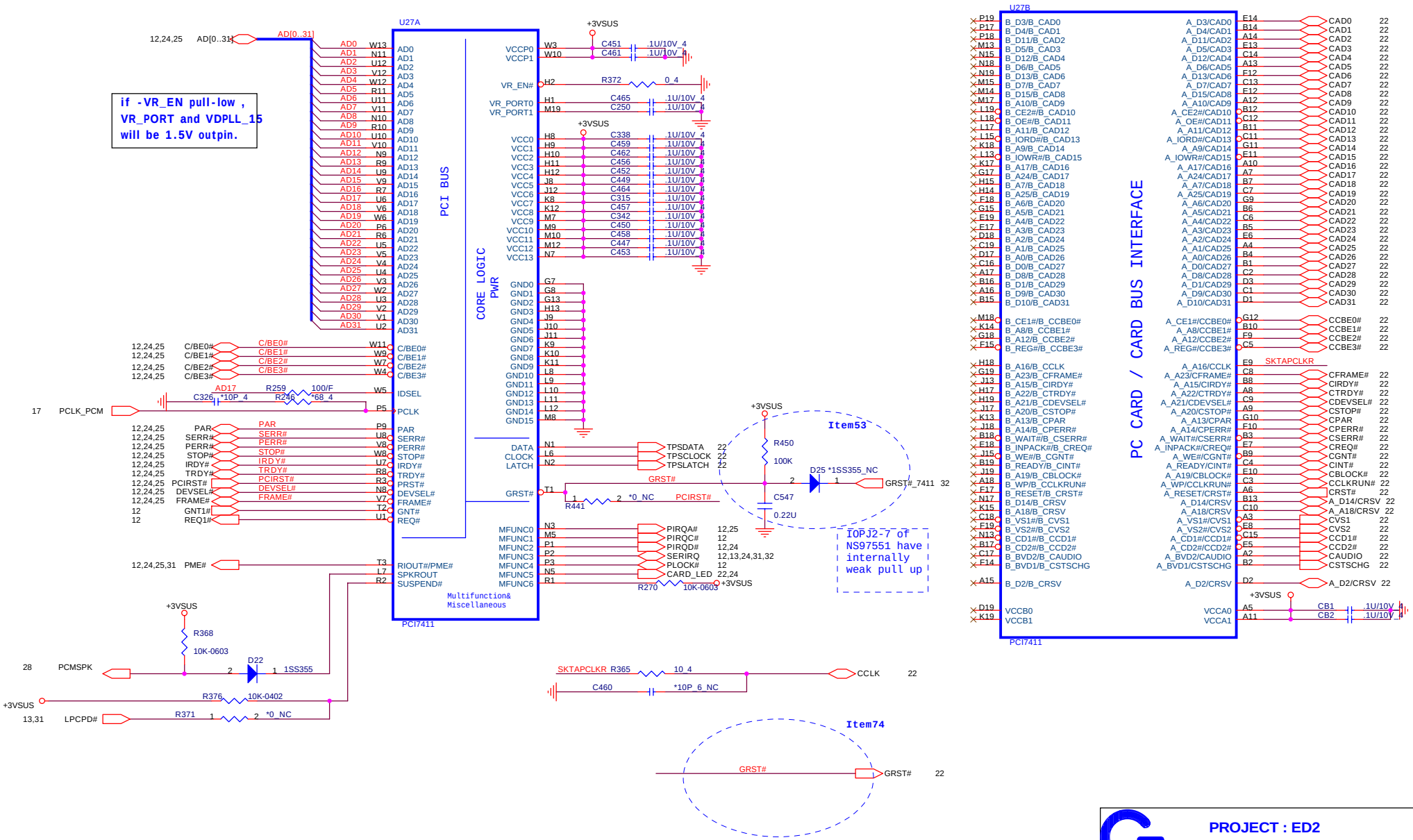
ODD



PROJECT : ED2

Quanta Computer Inc.

Size	Document Number	Rev
	HDD & CDROM Connector	C2A
Date: Friday, October 22, 2004	Sheet 20 of 38	


if -VR_EN pull-low , VR_PORT and VDPLL_15 will be 1.5V outpin.
U27A
PCI BUS
CORE LOGIC
PWR
Multifunction& Miscellaneous
PCI7411
U27B
PC CARD / CARD BUS INTERFACE
PCI7411
Item53
IOPJ2-7 of NS97551 have internally weak pull up
Item74
PROJECT : ED2
Quanta Computer Inc.
PCMCIA TI7411
Rev C2A
Friday, October 22, 2004
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PCMCIA SOCKET

CN4

		1	GND
21	CAD0	2	D3 - CAD0
21	CAD1	3	D4 - CAD1
21	CAD3	4	D5 - CAD3
21	CAD5	5	D6 - CAD5
21	CAD7	6	D7 - CAD7
21	CCBE0#	7	CE1- CCBE0
21	CAD9	8	A10- CAD9
21	CAD11	9	OE - CAD11
21	CAD12	10	A11- CAD12
21	CAD14	11	A9 - CAD14
21	CCBE1#	12	A8 - CCBE1
21	CPAR	13	A13- CPAR
21	CPERR#	14	A14- CPERR
21	CGNT#	15	WE/PGM - CGNT
21	CINT#	16	RDY/BSY,IRQ*INT
	VCCCB	17	VCC
	VPPCB	18	VPP1
21	CCLK	19	A16- CCLK
21	CIRDY#	20	A15- CIRDY
21	CCBE2#	21	A12- CCBE2
21	CAD18	22	A7 - CAD18
21	CAD20	23	A6 - CAD20
21	CAD21	24	A5 - CAD21
21	CAD22	25	A4 - CAD22
21	CAD23	26	A3 - CAD23
21	CAD24	27	A2 - CAD24
21	CAD25	28	A1 - CAD25
21	CAD26	29	A0 - CAD26
21	CAD27	30	D0 - CAD27
21	CAD29	31	D1 - CAD29
21	A_D2/CRSV	32	D2 - RFU
21	CCLKRUN#	33	WP,IOIS16-CKRUN
		34	GND
		35	GND
21	CCD1#	36	CD1- CCD1
21	CAD2	37	D11- CAD2
21	CAD4	38	D12- CAD4
21	CAD6	39	D13- CAD6
21	A_D14/CRSV	40	D14- RFU
21	CAD8	41	D15- CAD8
21	CAD10	42	CE2- CAD10
21	CVS1	43	RFSH,VS*1-CVS1
21	CAD13	44	IORD-CAD13
21	CAD15	45	IOWR-CAD15
21	CAD16	46	A17- CAD16
21	A_A18/CRSV	47	A18- RFU
21	CBLOCK#	48	A19- CBLOCK
21	CSTOP#	49	A20- CSTOP
21	CDEVSEL#	50	A21- CDEVSEL
	VCCCB	51	VCC
	VPPCB	52	VPP2
21	CTRDY#	53	A22- CTRDY
21	CFRAME#	54	A23- CFRAME
21	CAD17	55	A24- CAD17
21	CAD19	56	A25- CAD19
21	CVS2	57	NC - CVS2
21	CRST#	58	RESET-CRST
21	CSERR#	59	WAIT-CSERR
21	CREQ#	60	INPACK-CREQ
21	CCBE3#	61	REG- CCBE3
21	CAUDIO	62	BVD2,SP-CAUDIO
21	CSTSCHG	63	BVD1,STSCHG-C*
21	CAD28	64	D8 - CAD28
21	CAD30	65	D9 - CAD30
21	CAD31	66	D10- CAD31
21	CCD2#	67	CD2- CCD2
		68	GND
		69	GND
		70	GND
		71	GND
		72	GND
		73	GND
		74	GND

SANTA-1306-68P

MC_PWR_CTR low active(default) , or change register to high active

U27C

MC_CTRL0#	F1	MC_PWR_CTRL_0
T68	F2	MC_PWR_CTRL_1
-MSCD	F5	MS_CD#
-SDCD	E3	SD_CD#
-SMCD	F6	SM_CD#
MSCLK/SDCLK/-SMELWP R375 33_4 MSCLK/SDCLK/-SMELWP_PCI7411	G5	MS_CLK//SD_CLK//SM_EL_WP#
MSBS/SDCMD/-SMWE	F3	MS_BS//SD_CMD//SM_WE#
MS/SD/SM D3	H5	MS_DATA3//SD_DAT3//SM_D3
MS/SD/SM D2	G3	MS_DATA2//SD_DAT2//SM_D2
MS/SD/SM D1	G2	MS_DATA1//SD_DAT1//SM_D1
MS/SD/SM D0	G1	MS_SDIO(DATA0)//SD_DAT0//SM_D0
SM_RE#	J5	SM_RE#
SM_ALE	J3	SM_ALE
SM_D4	H3	SM_D4
SM_D5	J6	SM_D5
SM_D6	J1	SM_D6
SM_D7	J2	SM_D7
SD_WP/-SMCE	H7	SD_WP//SM_CE#
SM_CLE/SC_GPIO0	J7	SM_CLE//SC_GPIO0
SM_R/B#/SC_RFU	K1	SM_R/B#//SC_RFU
T79	K2	SM_PHYS_WP#//SC_FCB
T130	L5	SC_PWR_CTRL
T75	L2	SC_CD#
T78	K5	SC_CLK
T69	K3	SC_RST
T77	L1	SC_DATA
T131	L3	SC_OC#
+5VSUS R217 10K-0603 SC_VCC5V	K7	SC_VCC_5V

PCI7411

Six For 1 Card

Flash Media Layout Guidelines:

1. Signal traces should be 60 Ohm +/- 10%.
2. All signal traces should be routed with equal propagation delay, and with trace lengths as short as practical.

3. A 56 Ohm damping resistor for MS_CLK and SD_CLK should be placed near the PCI7411 source.

IRLML5103
Rds(on)=0.6

Item74 +3VSUS → Q46 IRLML5103 → MB_VCC; C511 .1U/10V_4; C503 10U_6.3V_8; R397 *100K_NC

Item74 +3VSUS R387 8.2K → MC_CTRL0#

Item74 +3VSUS → Q47 *IRLML5103

21,24 CARD_LED

D23 *1SS355; D24 *1SS355

-SDCD

-SMCD

TI Erratum

TPSDATA C141 *10P_4_NC
TPSCLOCK C142 *10P_4_NC
TPSLATCH C143 *10P_4_NC

VCCCB C134 .1U/10V_4; C133 .1U/10V_4; C132 10U_6.3V_8

VPPCB C135 .1U/10V_4; C136 10U_6.3V_8

4 IN1 CARD READER (XD,MMC/SD,MS)

MB_VCC

CN10

-SDCD	1	CD_SD	VCC 43
MS/SD/SM D2	2	DAT2_SD	
MS/SD/SM D3	3	CD/DAT3_SD	41
MSBS/SDCMD/-SMWE	4	CMD_SD	VCC_XD 40 SM_D7
	5	VSS_SD	D7_XD 39 SM_D6
MSCLK/SDCLK/-SMELWP	6	VDD_SD	D6_XD 38 SM_D5
	7	CLK_SD	D5_XD 37 SM_D4
	8	VSS_SD	D4_XD 36 MS/SD/SM D3
MS/SD/SM D0	9	DAT0_SD	D3_XD 35 MS/SD/SM D2
MS/SD/SM D1	10	DAT1_SD	D2_XD 34 MS/SD/SM D1
SD_WP/-SMCE	11	WP_SD	D1_XD 33 MS/SD/SM D0
	12	VSS_MS	D0_XD 32
	13	VCC_MS	GND_XD 31 MSCLK/SDCLK/-SMELWP
MSCLK/SDCLK/-SMELWP	14	SCLK_MS	-WP_XD 30 MSBS/SDCMD/-SMWE
MS/SD/SM D3	15	RESERVE_MS	-WE_XD 29 SM_ALE
-MSCD	16	INS_MS	ALE_XD 28 SM_CLE/SC_GPIO0
MS/SD/SM D2	17	RESERVE_MS	CLE_XD 27 SD_WP/-SMCE
MS/SD/SM D0	18	SDIO_MS	-CE_XD 26 SM_RE#
MS/SD/SM D1	19	RESERVE_MS	-RE_XD 25 SM_R/B#/SC_RFU
MSBS/SDCMD/-SMWE	20	BS_MS	R/-B_XD 24 -SMCD
	21	VSS_MS	GND_XD 23
	22	GND	GND 42

MSX039-X0-0X00

Item74 +3VSUS C488 4.7U/10V_8; C491 .1U/10V_4

Item74 +5VSUS

Item74 +5VSUS TPSDATA TPSCLOCK TPSLATCH VPPCB VCCCB GRST#

U21

	1	5V_0	5V_2 24
	2	5V_1	NC_4 23
TPSDATA	3	DATA	NC_3 22
TPSCLOCK	4	CLOCK	SHDN# 21
TPSLATCH	5	LATCH	12V_1 20
	6	NC_1	BVPP/BVCORE 19
	7	12V_0	BVCC1 18
VPPCB	8	AVPP/AVCORE	BVCC0 17
VCCCB	9	AVCC0	NC_2 16
	10	AVCC1	OC# 15
	11	GND	3.3VIN0 14
GRST#	12	RESET#	3.3VIN1 13
	NC_5 25		

TPS2220A (DB)

C145 10U_6.3V_8; C178 .1U/10V_4; C144 4.7U/10V_8

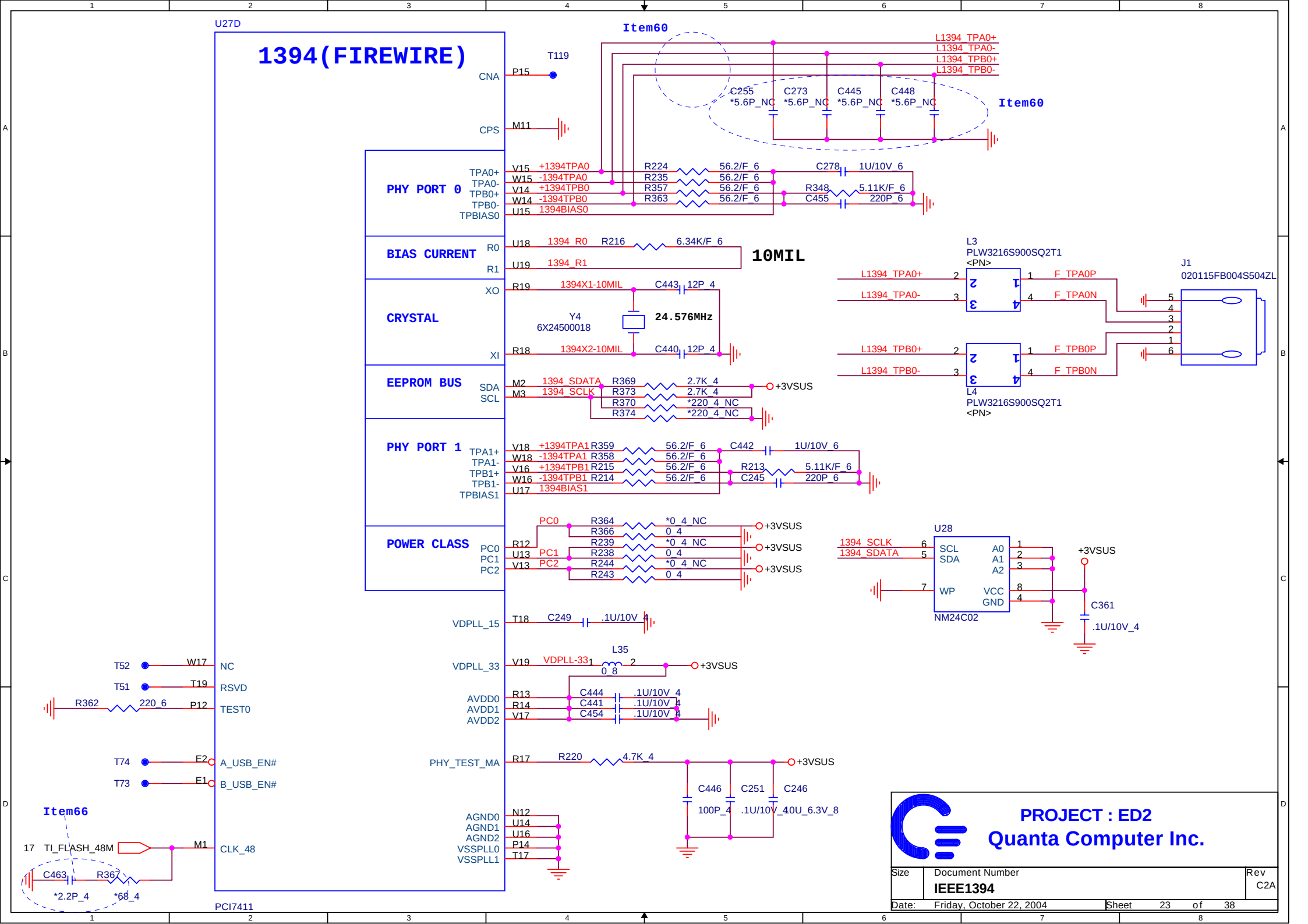
C180 4.7U/10V_8; C181 10U_6.3V_8; C179 .1U/10V_4

Item74 +5VSUS

Item74 +3VSUS

Item74

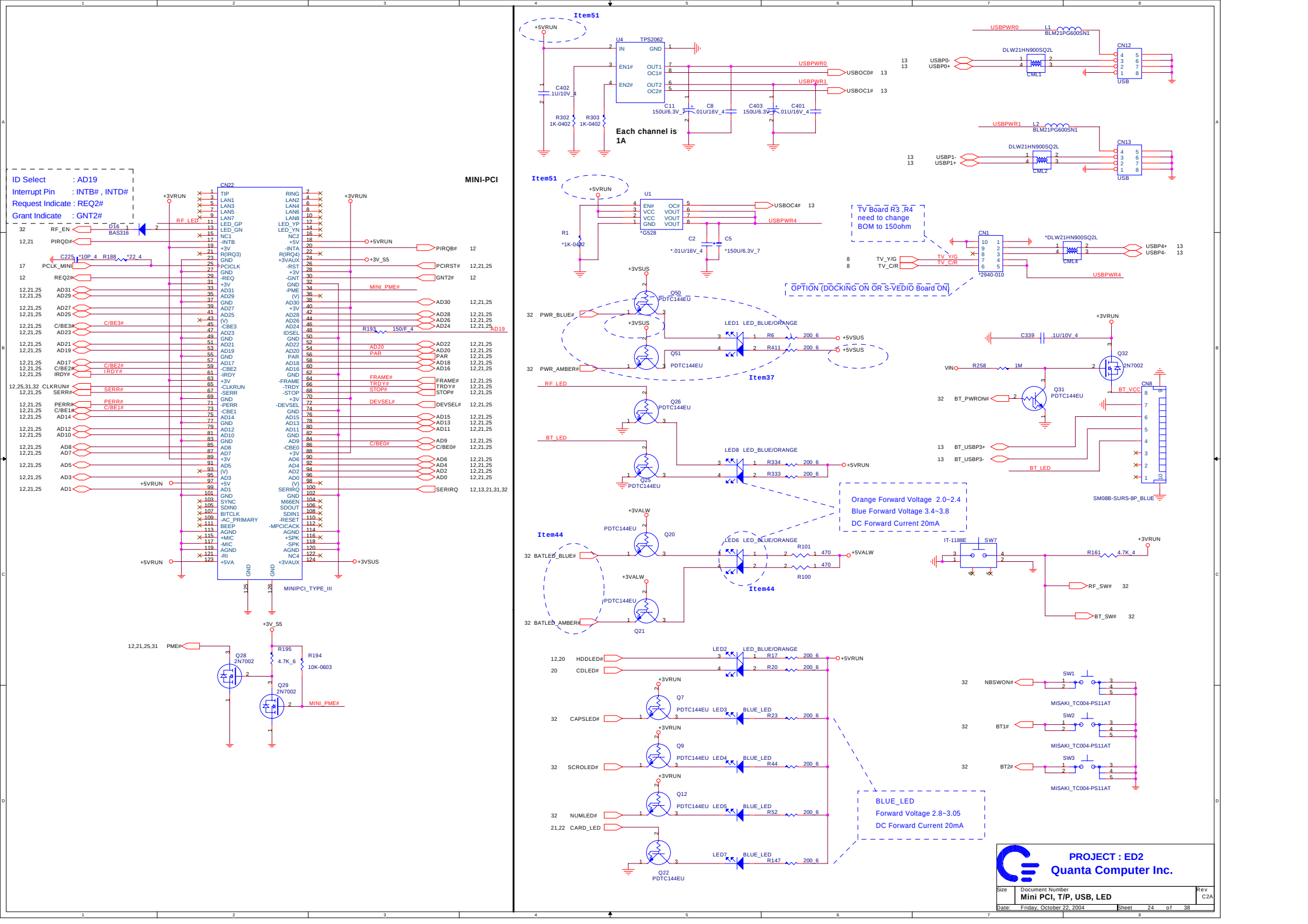
Quanta Computer Inc.	PROJECT : ED2	
Size	Document Number	Rev
	PCMCIA Socket & 4-IN-1	C2A
Date: Friday, October 22, 2004	Sheet 22 of 38	



PROJECT : ED2

Quanta Computer Inc.

Size	Document Number	Rev
	IEEE1394	C2A
Date: Friday, October 22, 2004	Sheet 23 of 38	


ID Select : AD19
Interrupt Pin : INTB# , INTD#
Request Indicate : REQ2#
Grant Indicate : GNT2#
MINI-PCI
CN22
MINIPCI_TYPE_III
Item51
Each channel is 1A
TPS2062
USBPWR0
USBPWR1
USBP0-
USBP0+
USBP1-
USBP1+
CML1
CML2
CML4
USB
TV Board R3 ,R4 need to change BOM to 150ohm
OPTION (DOCKING ON OR S-VEDIO Board ON)
*2940-010
Item37
Item44
LED_BLUE/ORANGE
Orange Forward Voltage 2.0~2.4
Blue Forward Voltage 3.4~3.8
DC Forward Current 20mA
BLUE_LED
Forward Voltage 2.8~3.05
DC Forward Current 20mA
SM08B-SURS-8P-BLUE
MISAKI_TC004-PS11AT
PROJECT : ED2
Quanta Computer Inc.
Mini PCI, T/P, USB, LED
Friday, October 22, 2004

R117
RTL8110SBL(1G)--DEPOP
RTL8100L(10,100)--POP

R116
RTL8110SBL(1G)--POP
RTL8100L(10,100)--DEPOP

RTL81XX's power for Co-lay :

AS	RTL8110SBL(Giga-Lan)	AVDDL CONNECT	+2.5V_A
	RTL8100L(10,100M-Lan)	AVDDL CONNECT	+3V_LAN_A
AS	RTL8110SBL(Giga-Lan)	HSDAC- CONNECT	+3V_LAN_A
	RTL8100L(10,100M-Lan)	HSDAC- CONNECT	+2.5V_A
AS	RTL8110SBL(Giga-Lan)	DVDD CONNECT	+1.8V_D
	RTL8100L(10,100M-Lan)	DVDD CONNECT	+2.5V_A

U23 RTL8110SBL/8100CL

VDD33---+3.3V DIGITAL
AVDDH------+3.3V ANALOG
AVDDL-----+2.5V ANALOG
DVDD-----+1.8V ANALOG
DVDD_A----+1.8VANALOG

RTL8110SBL(1G)--POP 2.49K
RTL8100L(10,100M) POP 5.6K

R113,R114
RTL8110SBL(1G)--POP
RTL8100L(10,100)--DEPOP

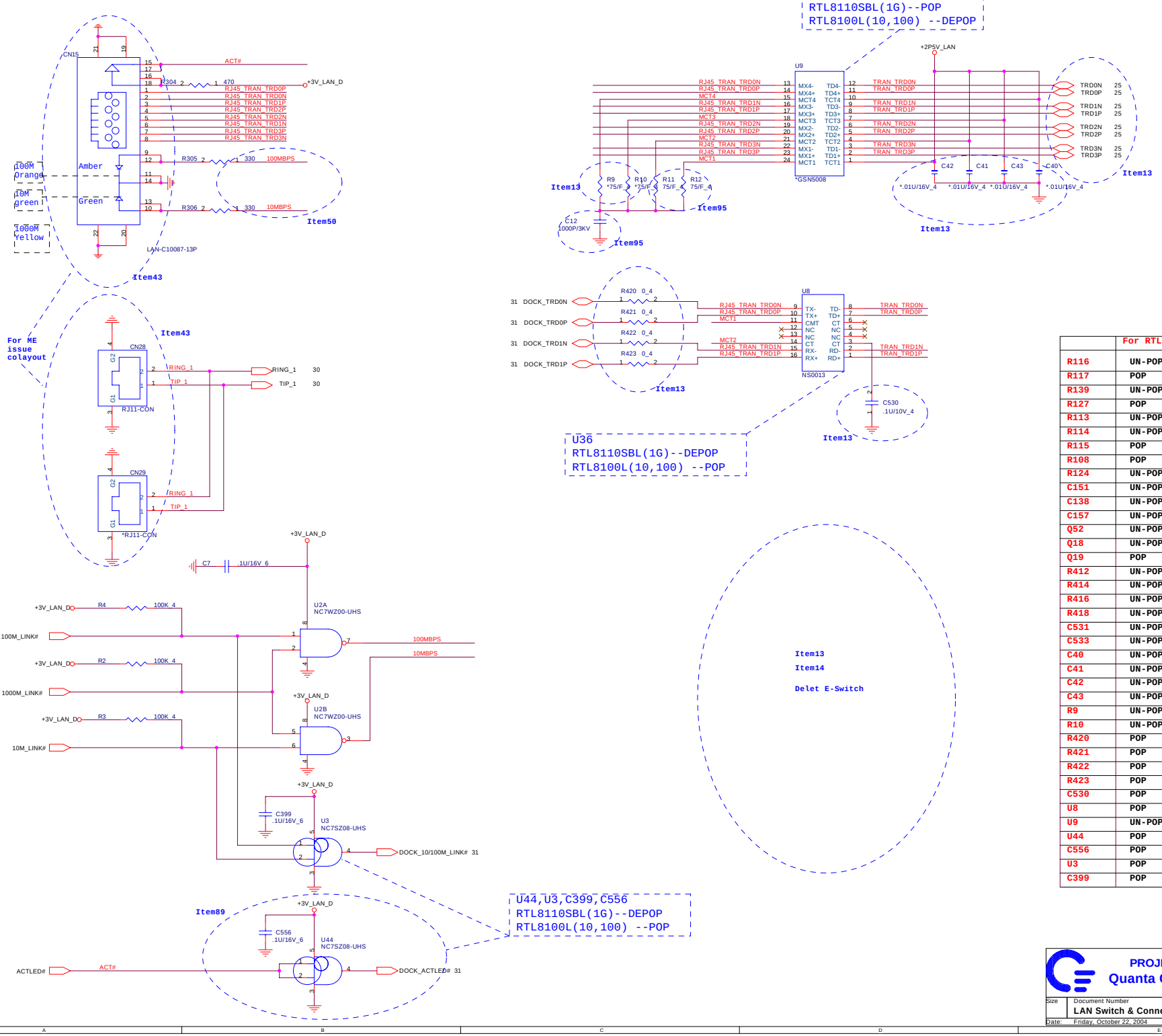
R108,R115,Q19
RTL8110SBL(1G)--DEPOP
RTL8100L(10,100) --POP

R412,R414,R416,R418,C531,C533
RTL8110SBL(1G)--POP
RTL8100L(10,100)--DEPOP

Q52 Colayout with Q19
RTL8110SBL(1G)--POP
RTL8100L(10,100) --DEPOP

Q18,R124,C138,C157,C151
RTL8110SBL(1G)--POP
RTL8100L(10,100) --DEPOP

PROJECT :	ED2
Quanta Computer Inc.	
Size	Document Number: LAN RTL8110S/8100CL — Rev: C2A
Date:	Friday, October 22, 2004 — Sheet 25 of 38

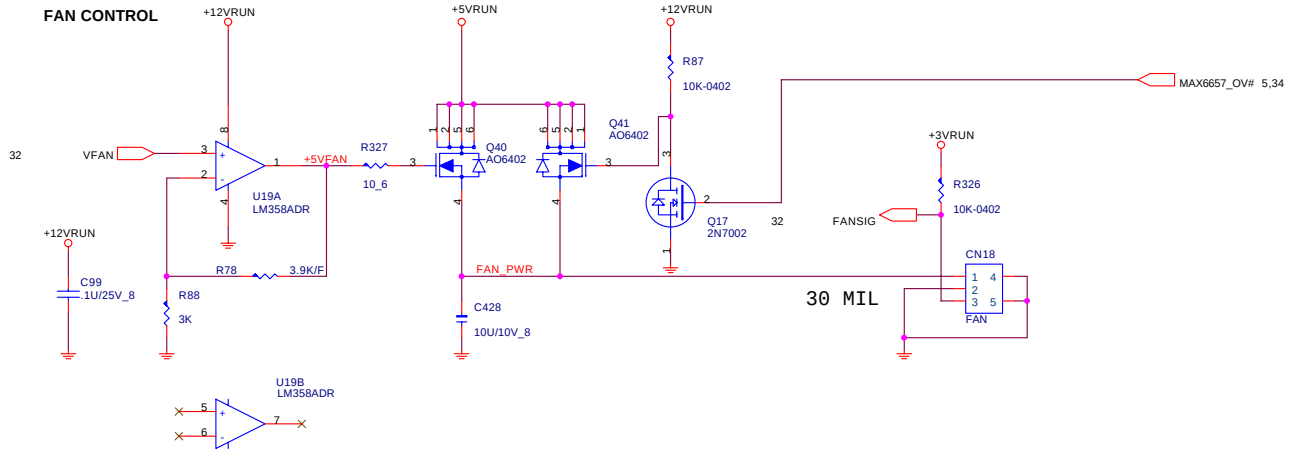


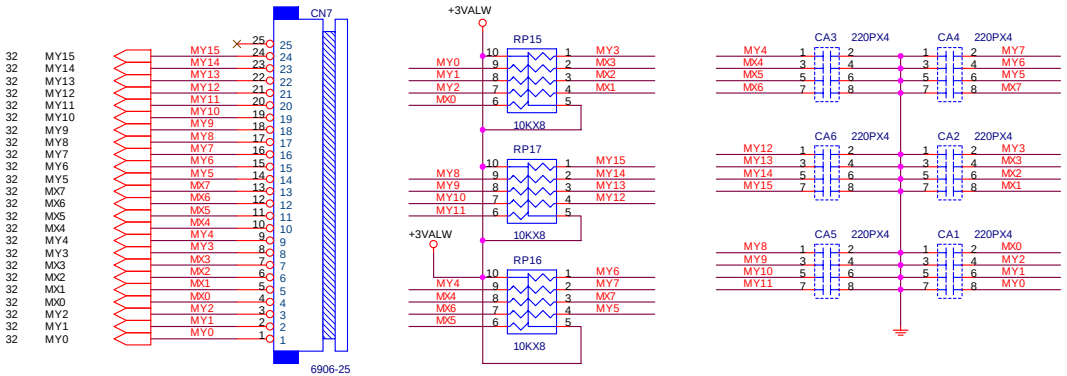
	For RTL8100C	For RTL8110SB
R116	UN-POP	POP
R117	POP	UN-POP
R139	UN-POP	POP
R127	POP	UN-POP
R113	UN-POP	POP
R114	UN-POP	POP
R115	POP	UN-POP
R108	POP	UN-POP
R124	UN-POP	POP
C151	UN-POP	POP
C138	UN-POP	POP
C157	UN-POP	POP
Q52	UN-POP	POP
Q18	UN-POP	POP
Q19	POP	UN-POP
R412	UN-POP	POP
R414	UN-POP	POP
R416	UN-POP	POP
R418	UN-POP	POP
C531	UN-POP	POP
C533	UN-POP	POP
C40	UN-POP	POP
C41	UN-POP	POP
C42	UN-POP	POP
C43	UN-POP	POP
R9	UN-POP	POP
R10	UN-POP	POP
R420	POP	UN-POP
R421	POP	UN-POP
R422	POP	UN-POP
R423	POP	UN-POP
C530	POP	UN-POP
U8	POP	UN-POP
U9	UN-POP	POP
U44	POP	UN-POP
C556	POP	UN-POP
U3	POP	UN-POP
C399	POP	UN-POP

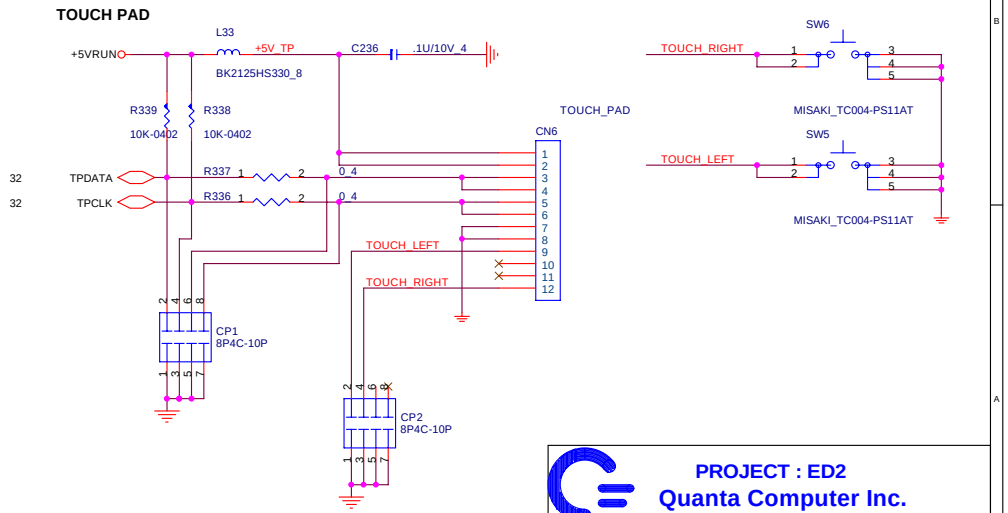
PROJECT : ED2
Quanta Computer Inc.

Size	Document Number	Rev
	LAN Switch & Connector	C2A

Date: Friday, October 22, 2004 Sheet 26 of 38







PROJECT : ED2		
Quanta Computer Inc.		
Size	Document Number	Rev
	T/P, FAN, Switch, K/B	C2A
Date: Friday, October 22, 2004	Sheet 27 of 38	

AC97 codec

For Layout:
Place decoupling caps near the power pins of Malibu device.

For Layout:
Place these resistors close to SmartAMCZ device.

For Layout:
Place crystal and associated circuitry very near SmartAMCZ Device.

For Layout:
Place near SmartAMCZ device

Item10
U40
20551-27P2
SAMART_AMC_HD

Item54

Item52
Docking side have poped 100U series CAP

Item91

LINE IN/MIC IN

Item52
Docking side Phone jack-sense high active

Item92

For AC-Link Mode: An external 14.318MHz clock source can be used to replace the crystal circuitry shown here. It should be connected to XTALIN (pin 15). The XTALOUT (pin 16) should be left floating.

For HD Audio Mode: Do not populate crystal circuitry and leave XTALIN (pin 15) and XTALOUT (pin 16) floating.

Ground Tie

BEEP

Item83

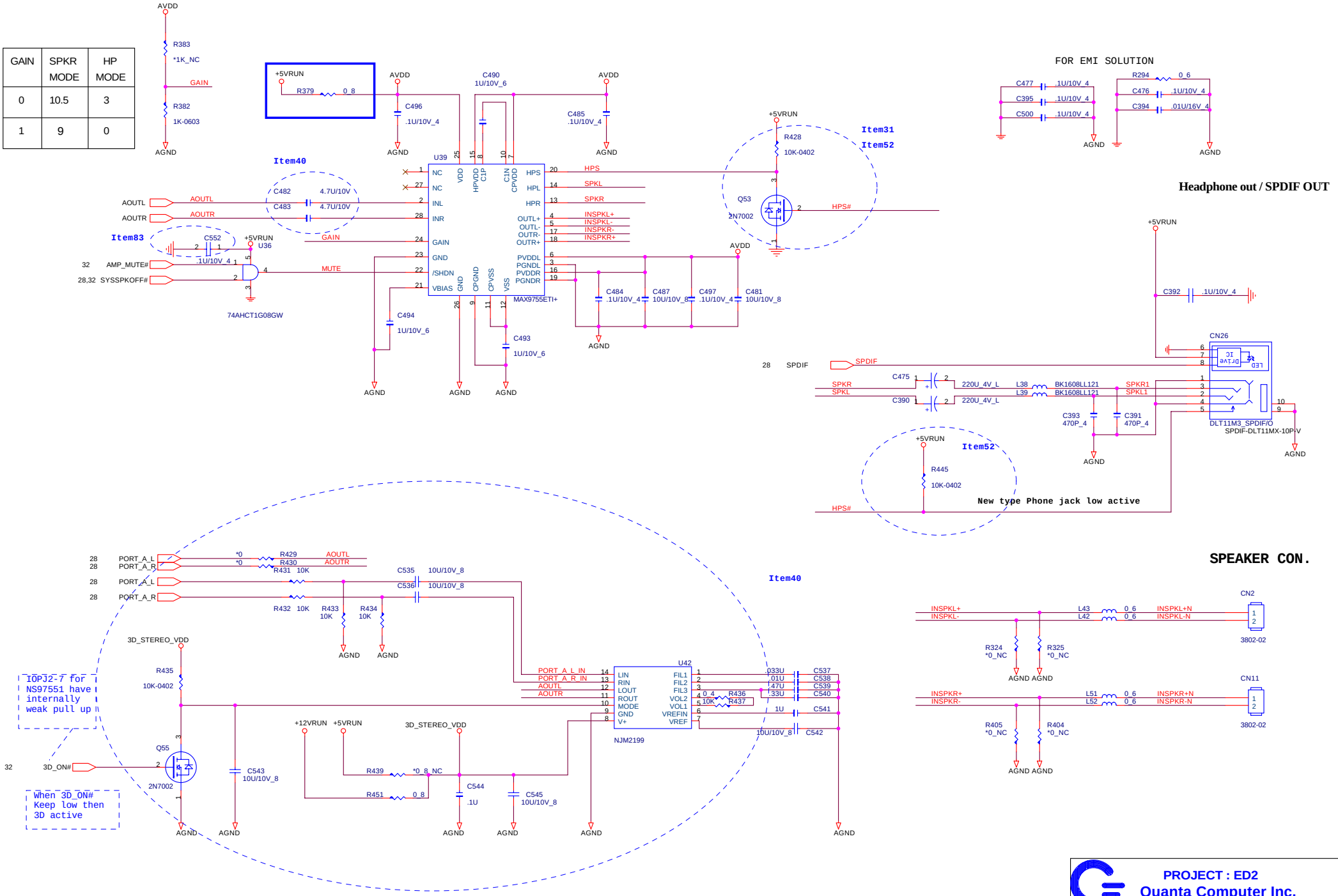
Item93

AC97 codec Power

U38 800mA (30MIL)
AIC1117

PROJECT : ED2		
Quanta Computer Inc.		
Size	Document Number: AC97 CODEC + MODEM	Rev: C2A
Date: Friday, October 22, 2004	Sheet 28 of 38	

GAIN	SPKR MODE	HP MODE
0	10.5	3
1	9	0



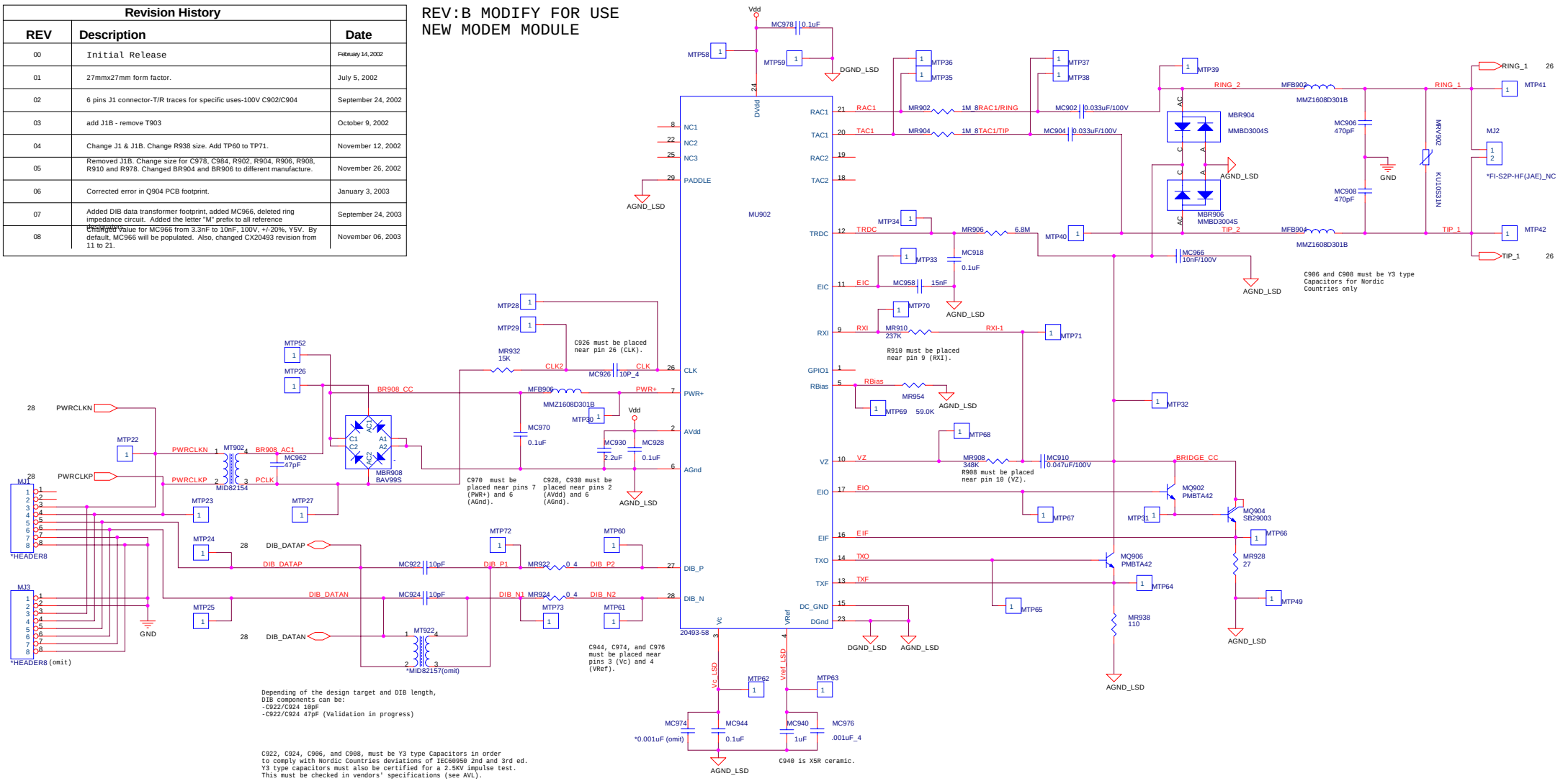
PROJECT : ED2
Quanta Computer Inc.

Size	Document Number	Rev
	Audio Amplifier & Jack	C2A
Date: Friday, October 22, 2004	Sheet 29 of 38	

Revision History

REV	Description	Date
00	Initial Release	February 14, 2002
01	27mmx27mm form factor.	July 5, 2002
02	6 pins J1 connector-T/R traces for specific uses-100V C902/C904	September 24, 2002
03	add J1B - remove T903	October 9, 2002
04	Change J1 & J1B. Change R938 size. Add TP60 to TP71.	November 12, 2002
05	Removed J1B. Change size for C978, C984, R902, R904, R906, R908, R910 and R978. Changed BR904 and BR906 to different manufacture.	November 26, 2002
06	Corrected error in Q904 PCB footprint.	January 3, 2003
07	Added DIB data transformer footprint, added MC966, deleted ring impedance circuit. Added the letter "M" prefix to all reference designators.	September 24, 2003
08	Changed value for MC966 from 3.3nF to 10nF, 100V, +/-20%, Y5V. By default, MC966 will be populated. Also, changed CX20493 revision from 11 to 21.	November 06, 2003

REV:B MODIFY FOR USE
NEW MODEM MODULE



PROJECT : ED2
Quanta Computer Inc.

Size	Document Number	Rev
	MODEM DAA	C2A

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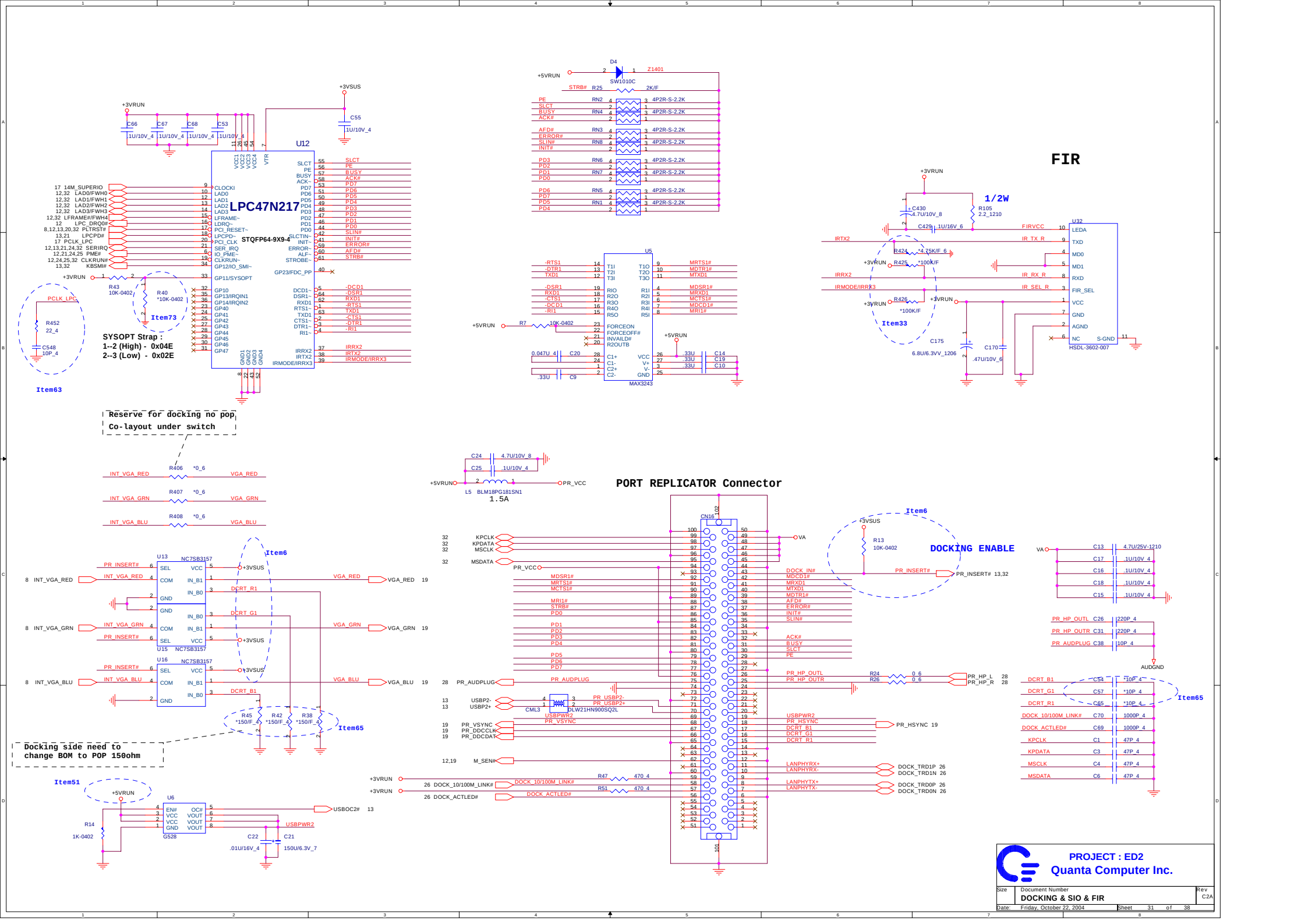
U12
LPC47N217
STQFP64-9X9-4
SYSOPT Strap :
1--2 (High) - 0x04E
2--3 (Low) - 0x02E
Item73
Item63
Reserve for docking no pop
Co-layout under switch
U5
MAX3243
FIR
1/2W
U32
HSDL-3602-007
Item33
PORT REPLICATOR Connector
CN16
DOCKING ENABLE
Item6
Item65
Item51
U13
U15
U16
NC7SB3157
U6
G528
Docking side need to
change BOM to POP 150ohm
PROJECT : ED2
Quanta Computer Inc.
DOCKING & SIO & FIR
Friday, October 22, 2004
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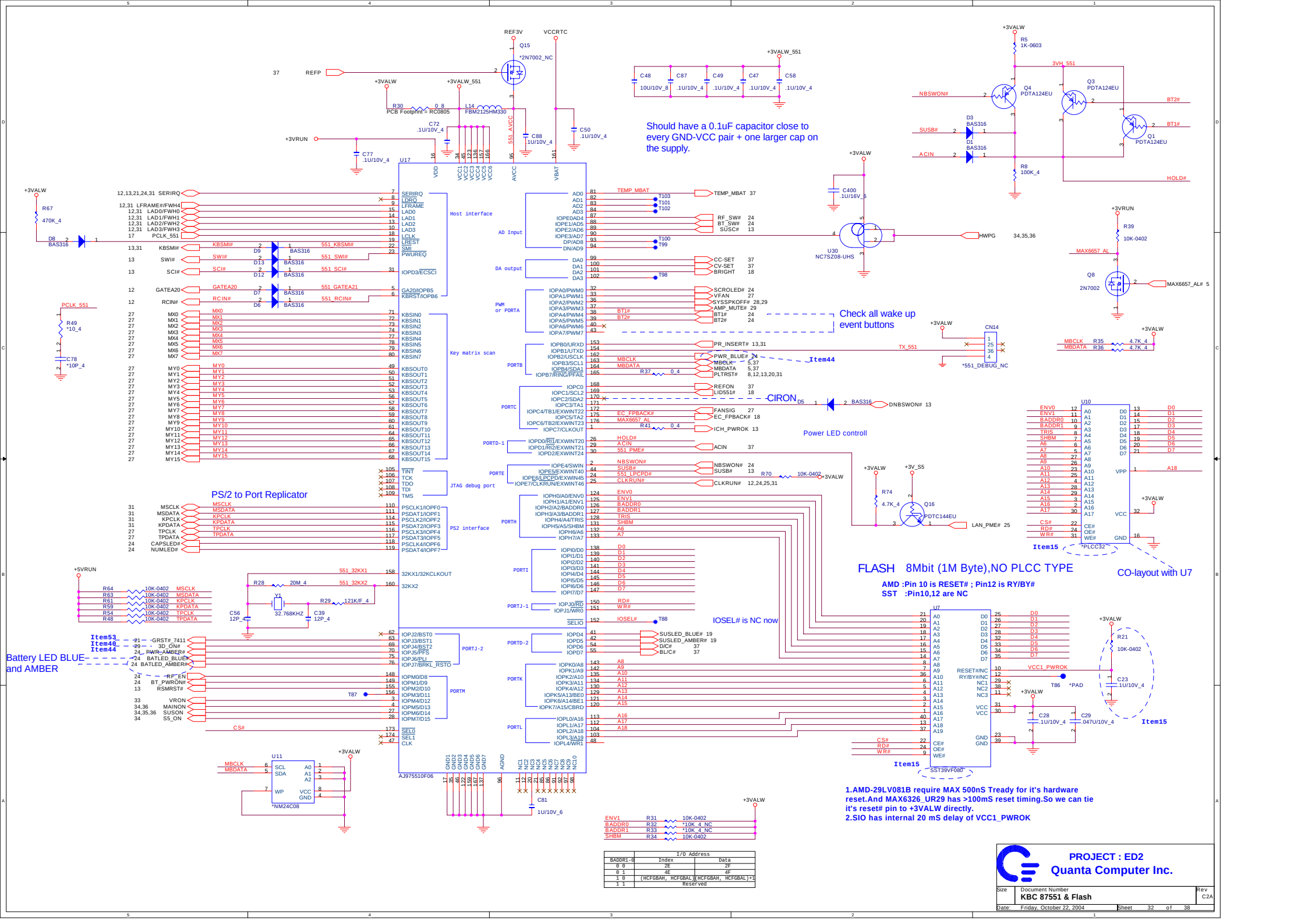
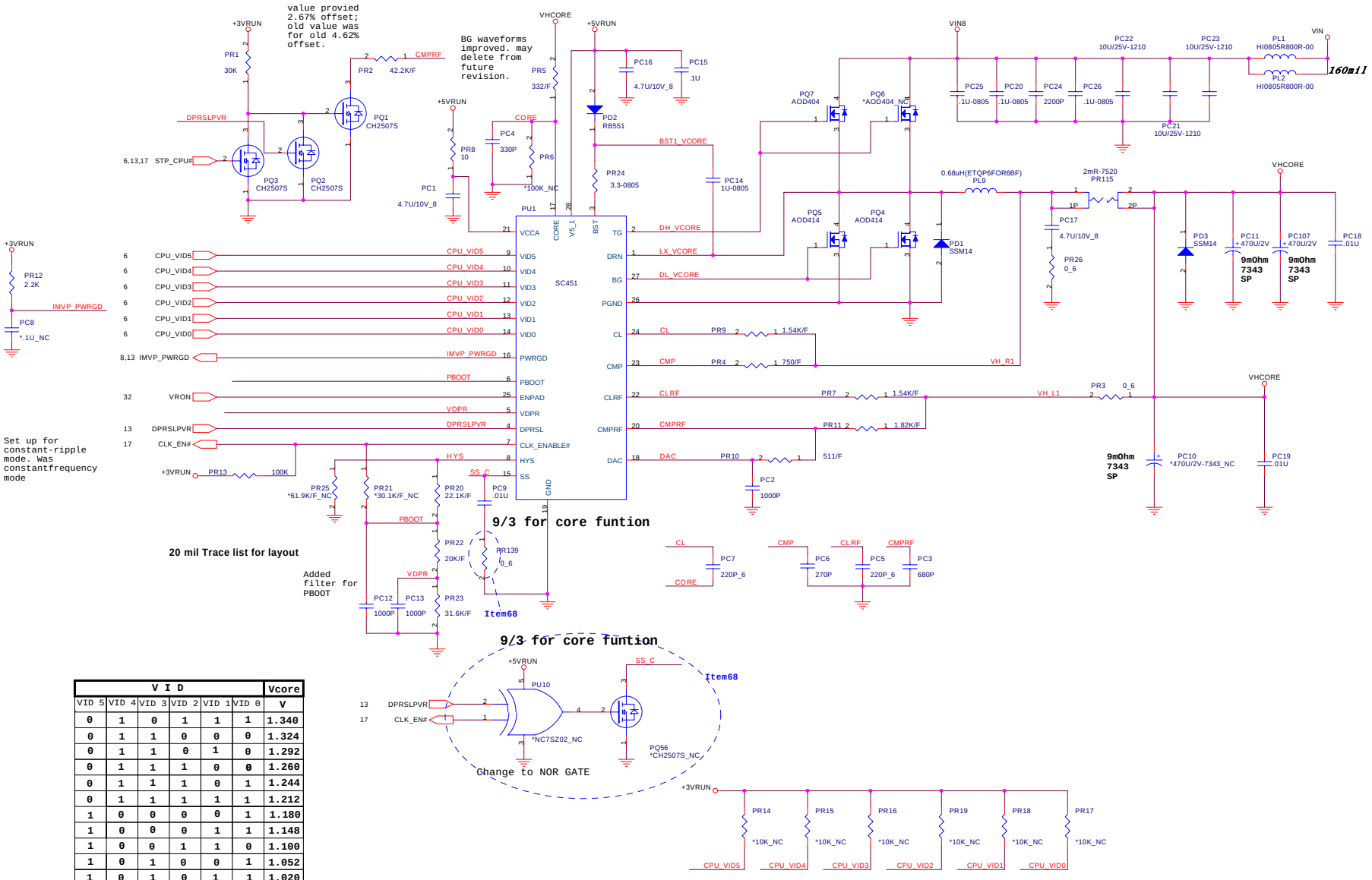

Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.
Check all wake up event buttons
Power LED controll
PS/2 to Port Replicator
Battery LED BLUE and AMBER
FLASH 8Mbit (1M Byte),NO PLCC TYPE
AMD :Pin 10 is RESET# ; Pin12 is RY/BY#
SST :Pin10,12 are NC
CO-layout with U7
IOSEL# is NC now
1.AMD-29LV081B require MAX 500nS Tready for it's hardware reset.And MAX6326_UR29 has >100mS reset timing.So we can tie it's reset# pin to +3VALW directly.
2.SIO has internal 20 mS delay of VCC1_PWROK
PROJECT : ED2
Quanta Computer Inc.
KBC 87551 & Flash
Friday, October 22, 2004



V I D						Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940

PROJECT : ED2
Quanta Computer Inc.

Size	Document Number	Rev
	CPU CORE (SC451)	C2A
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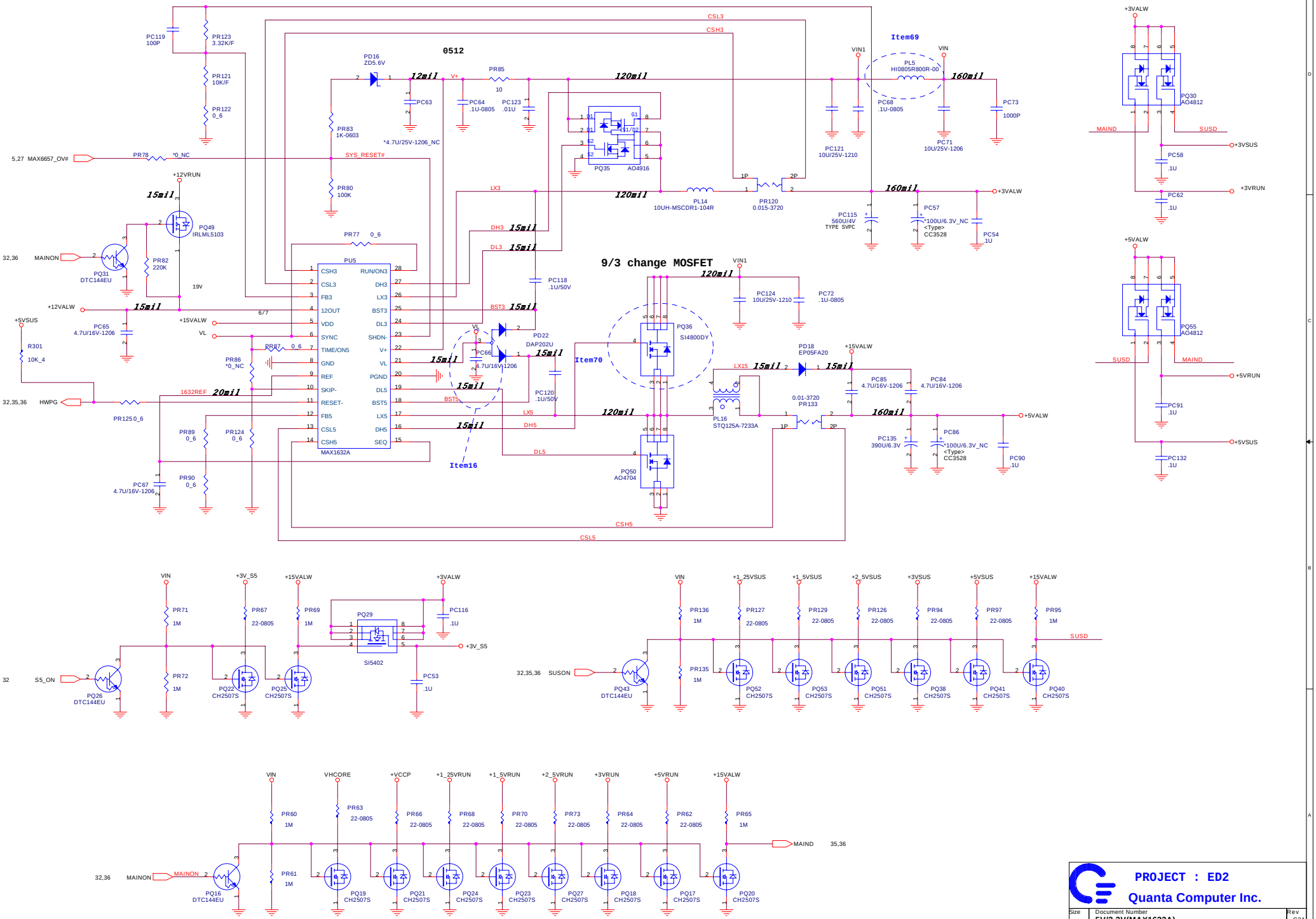
0512
9/3 change MOSFET
MAX1632A
PU5
Item69
Item70
Item16
PQ35 AO4916
PQ36 SI4800DY
PQ50 AO4704
PQ49 IRLML5103
PQ31 DTC144EU
PQ30 AO4812
PQ55 AO4812
PL5 HI0805R800R-00
PL14 10UH-MSCDR1-104R
PL16 STQ125A-7233A
PR120 0.015-3720
PR133 0.01-3720
PD16 ZD5.6V
PD22 DAP202U
PD18 EP05FA20
PQ29 SI5402
PQ26 DTC144EU
PQ22 CH2507S
PQ20 CH2507S
PQ43 DTC144EU
PQ52 CH2507S
PQ53 CH2507S
PQ51 CH2507S
PQ38 CH2507S
PQ41 CH2507S
PQ40 CH2507S
PQ16 DTC144EU
PQ19 CH2507S
PQ21 CH2507S
PQ24 CH2507S
PQ23 CH2507S
PQ27 CH2507S
PQ18 CH2507S
PQ17 CH2507S
PQ20 CH2507S
CSL3
CSH3
CSL5
CSH5
LX3
LX5
LX15
DH3
DL3
BST3
BST5
SYS_RESET#
1632REF
SUSD
MAIND
MAINON
SUSON
S5_ON
HWPG
MAX6657_OV#
+12VRUN
+12VALW
+15VALW
+5VSUS
+3VALW
+5VALW
+3V_S5
+5VSUS
+5VRUN
+3VRUN
VIN
VIN1
VL
VHCORE
+VCCP
+1_25VRUN
+1_5VRUN
+2_5VRUN
+3VRUN
+5VRUN
+15VALW
+1_25VSUS
+1_5VSUS
+2_5VSUS
+3VSUS
+3V_S5
PROJECT : ED2
Quanta Computer Inc.
Document Number
5V/3.3V(MAX1632A)
Rev C2A
Date: Friday, October 22, 2004
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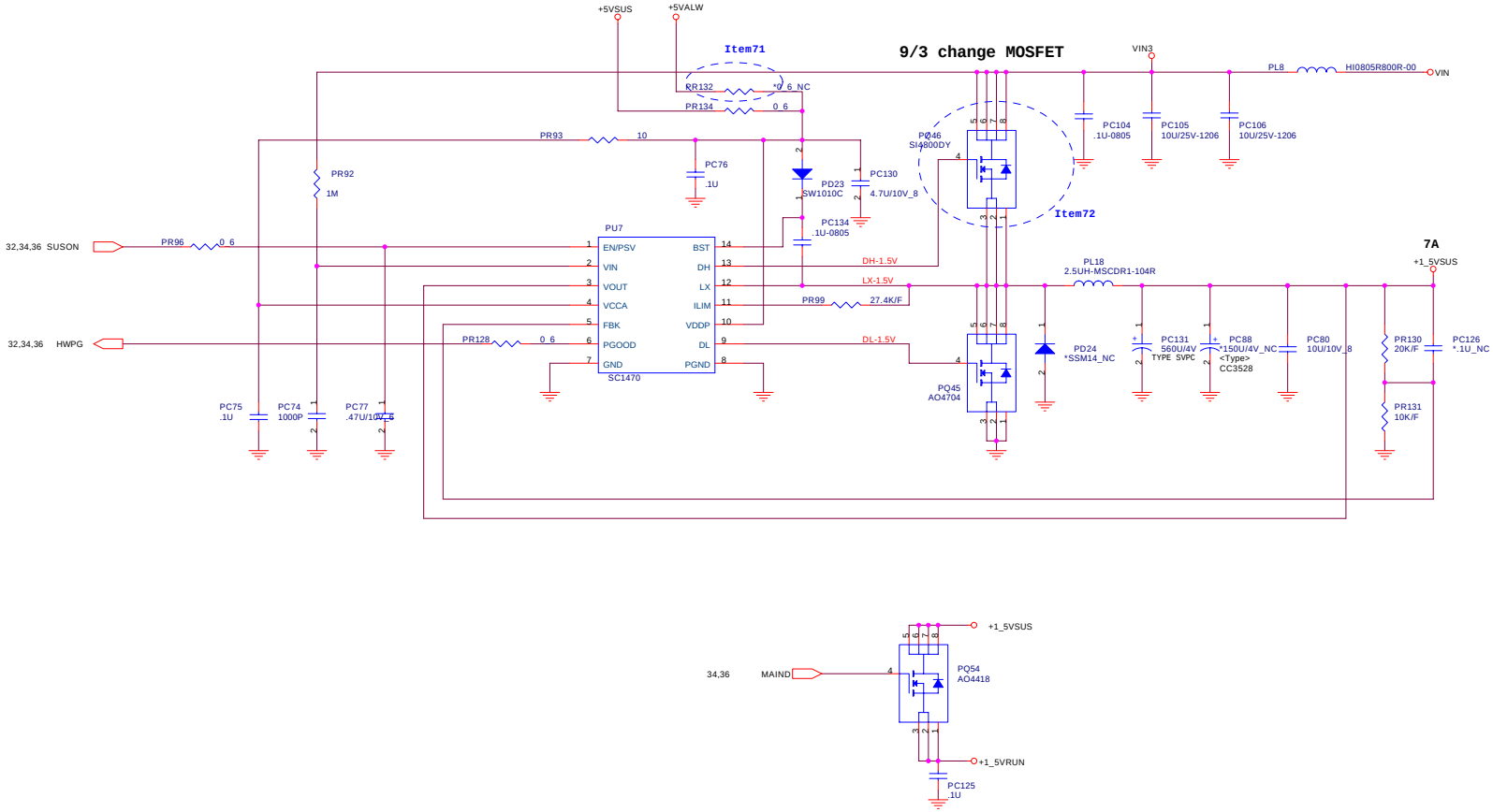

PROJECT : ED2

Quanta Computer Inc.

Size	Document Number	Rev
	2.5VSUS / +1.25TERM	C2A

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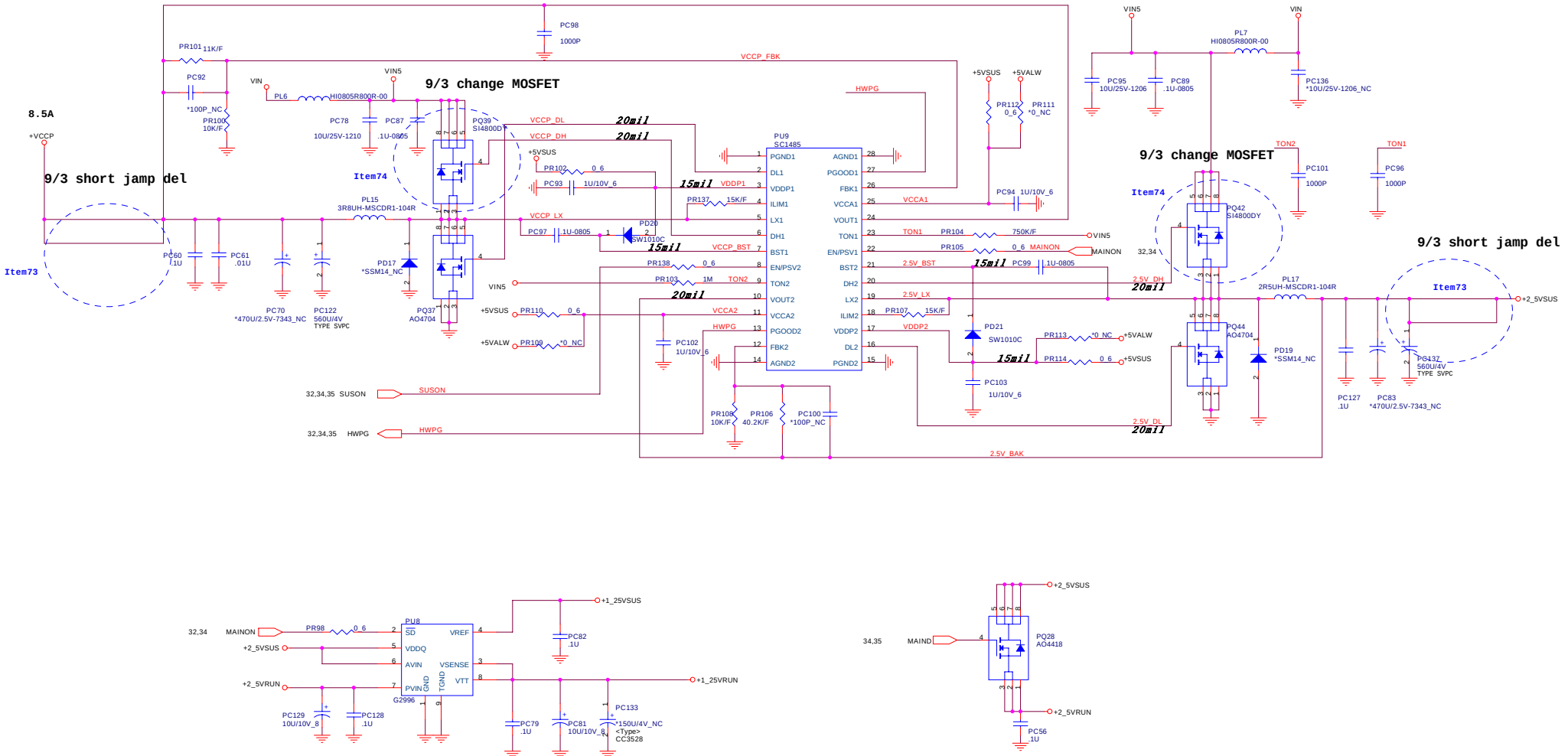
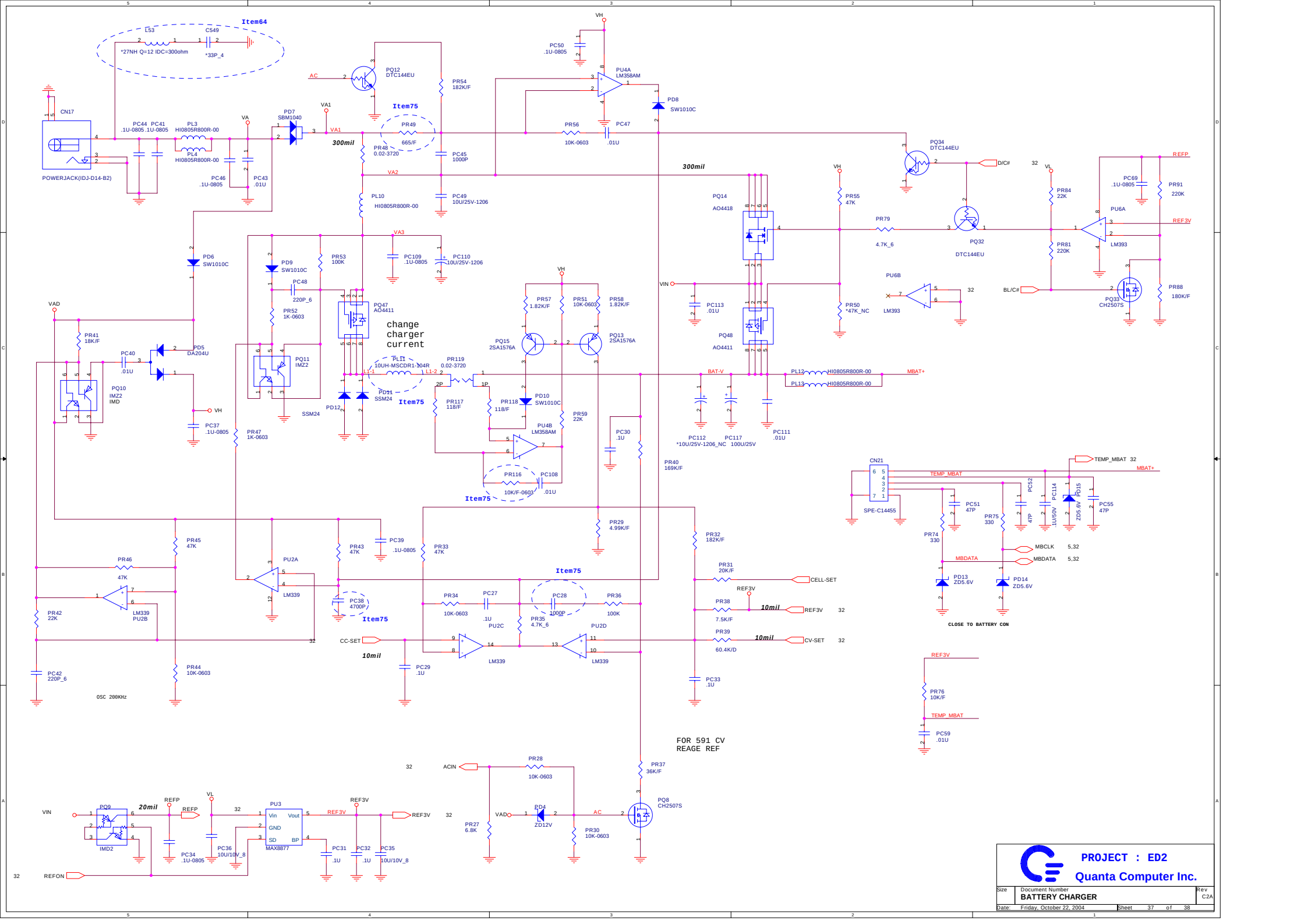


PROJECT : ED2		
Quanta Computer Inc.		
Size	Document Number +VCCP/+1.25V/+2.5V	Rev C2A
Date: Friday, October 22, 2004	Sheet 36 of 38	



PROJECT : ED2		
Quanta Computer Inc.		
Size	Document Number: BATTERY CHARGER	Rev: C2A
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