Tonga-e (ZN5)

01

BOM Option Note

IV@	INSTALL FOR UMA SKU
EV@	INSTALL FOR DISCRETE GRAPHIC SKU
PROTO	INSTALL FOR PROTO ONLY
NI	UNINSTALL
I	INSTALL FOR ALL SKU

Quanta Computer Inc.
PROJECT : ZN5
Size | Document Number: Schematics Index | Rev X4
Date: Friday, March 05, 2010 | Sheet 1 of 40

Tonga-E _ZN5 System Block Diagram

02

VCCP

V_1P1_CORE
V_1P1_PCIEXPRESS
V_1P1_ICH
V_FSB_VTT

V_1P1_CL_MCH
V_3P3_CL

VCC3
3VSB

VCC
5VSB
+12V

V_SM
V_1P5_ICH

System Power

Intel
Yorkfield LP
Wolfdale/Conroe
E7XX0/E8XX0
LGA775
Page 3,4

FSB(800/1067/1333HZ)

CLOCK GENERATOR
CK505
CV193
Page 2

800/1067 MHZ DDR III

CH A/B: DDRIII-SO-DIMM
Page 14

LCD PANEL
21.5" Full HD

NB
Eaglelake
Q43
1254 pin
Page 5,6,7,8,9

PCI-E 2.0 16X

MUX
PI3PCIE2612-A

SDVO

LVDS Transmitter
CH7308B
Page 16

LVDS

LVDS_CONNECT 1

PCI-E(0-3)
PCI-E(7-15)
PCI-E(4-6)

MXM CONNECTOR
VER:3.0
Page 15

LVDS

LVDS_CONNECT 2

DP

DP connect

MUX
PI3PCIE2612-A

SATA - HDD(3.5)
Page 17

SATA 1

SATA - ODD
Page 17

SATA 2

DMI

USB 2.0

Camera
Page 24

USB-1

USB/wirless KB
Dongle

USB-4

USB*4(Rear)
USB-0 for DEBUG
Page 23

USB-0,7,8,9

USB*2(Side)
Page 23

USB-3,5

Azalia

SB
ICH10D
676 pin
Page 10,11,12,13

PCI-Express 1X

PCIE-2

MINI CARD-1
WLAN Page 18
Bluetooth

USB-10

WLAN antenna

PCIE-3

MINI CARD-2
TV card
Page 18

TV antenna or
(F connect)

PCIE-1

LAN
82567QM
Page 20

RJ45

PCIE-4

Card Reader
/JMB380 /JMB385
Page 20

Media Slot

1394a

USB-11

SPI

LPC_BUS

32.768KHz

SUPER IO
SMSC SCH5327
Page 25

TPM
Page 22

EC ITE8512
Page 30

FLASH
ROM

IR
Blaster
Page 30

CIR
Page 30

PS2
Keyboard
Page 25

FAN
Page 24

PS2
Mouse
Page 25

AUDIO CODEC
ALC272
Page 26

H.P
Page 26

A_MIC IN
Page 26

INT SPK
Page 26

DMIC IN
Page 26

2WX2

LINE OUT
Page 27

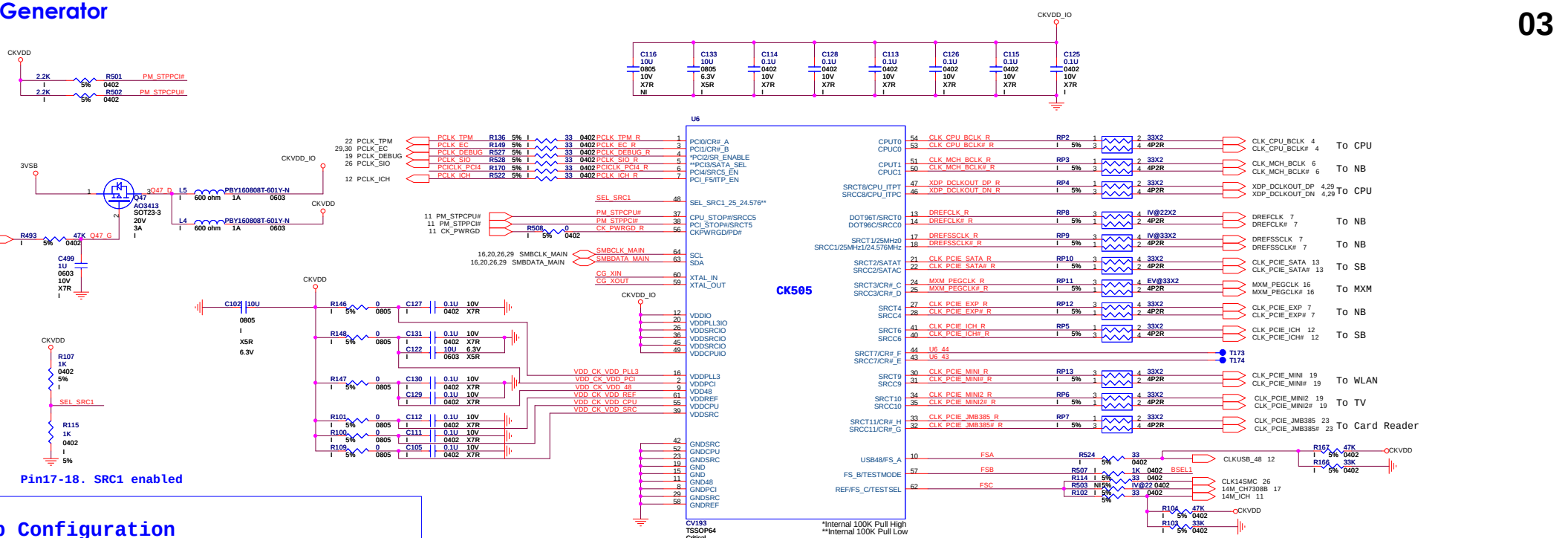
Quanta Computer Inc.
PROJECT : ZN5

Size	Document Number	Rev
	System Block Diagram	X4

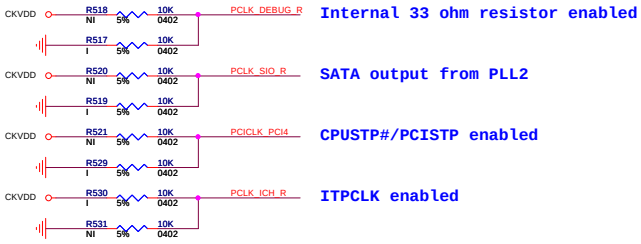
Date: Friday, March 05, 2010 Sheet 2 of 40

Clock Generator

03



Strap Configuration

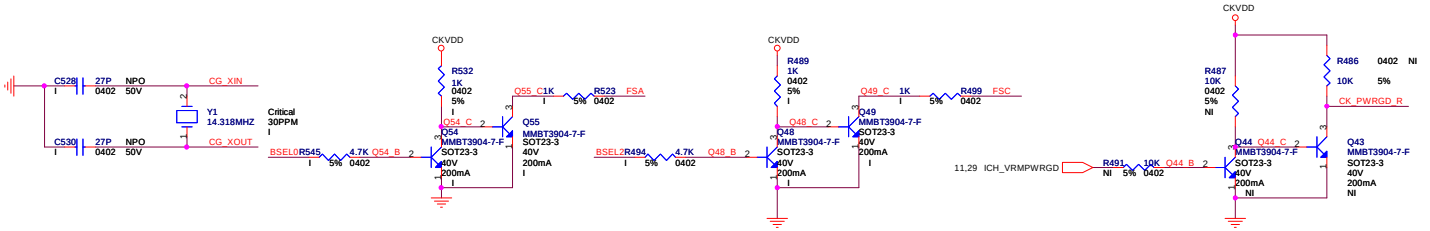


Internal 33 ohm resistor enabled

SATA output from PLL2

CPUSTP#/PCISTP enabled

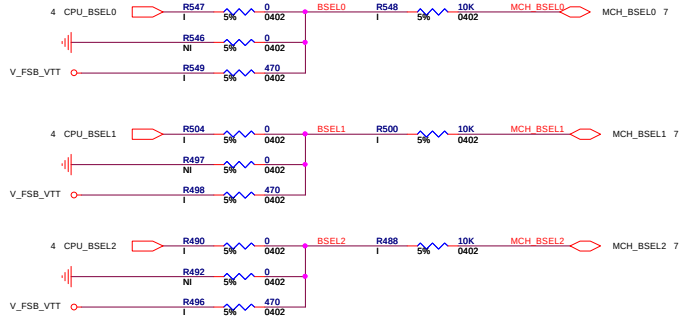
ITPCLK enabled

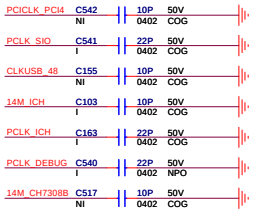


FREQ. SEL TABLE

BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	0	0	333Mhz
1	0	1	100Mhz
1	1	0	400Mhz
1	1	1	Reserved





Quanta Computer Inc.

PROJECT : ZN5

Size	Document Number	Rev
	CLK. GEN./ CK505	X4

Date: Friday, March 05, 2010 Sheet 3 of 40

Termination

XDP

IC design

Thermal Sensor

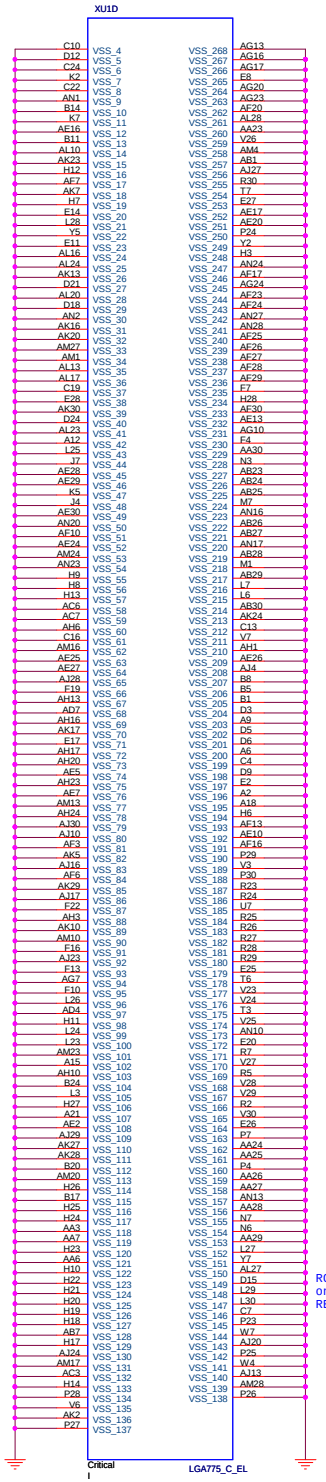
S1	S0	RATIO SET
0	0	0.615xVTT
0	1	0.63xVTT
1	0	0.65xVTT
1	1	0.67xVTT

Address: 9AH

Quanta Computer Inc.
PROJECT : ZN5

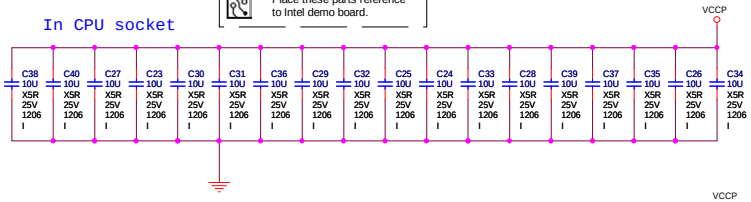
Size	Document Number	Rev
	CPU(1/2)- Host Bus	X4

Date: Friday, March 05, 2010 Sheet 4 of 40

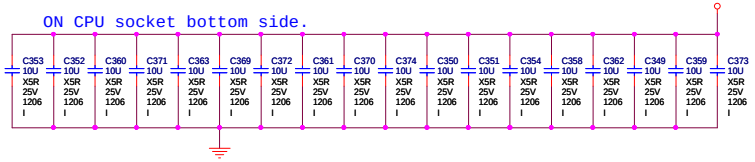


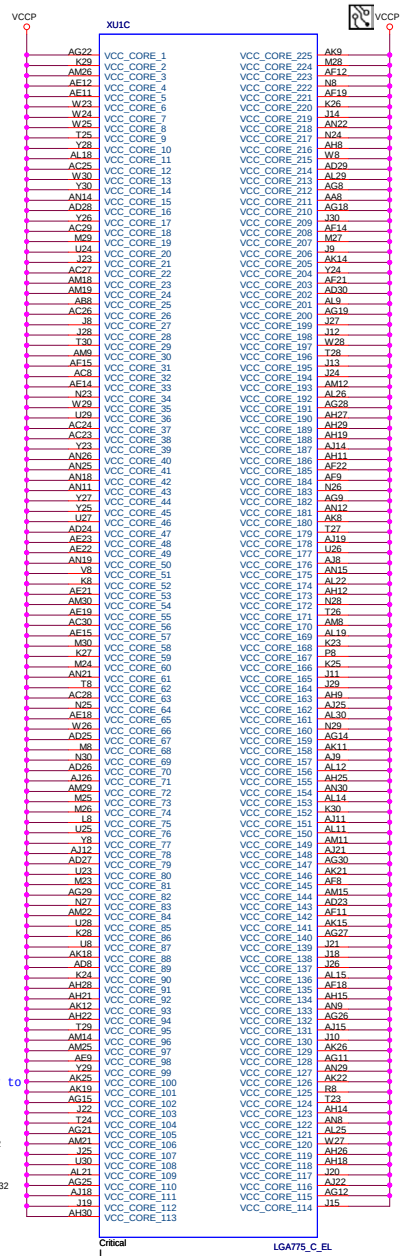
Place these parts reference to Intel demo board.

In CPU socket



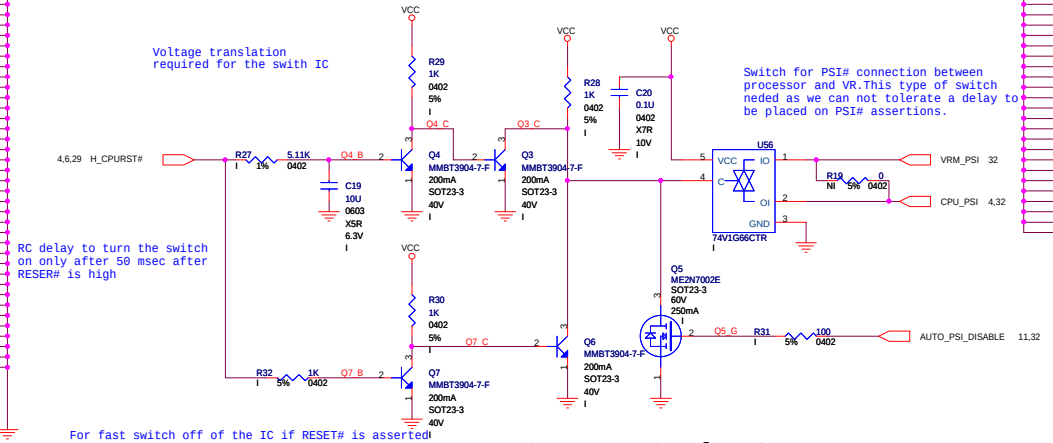
ON CPU socket bottom side.





Yorkfield/Wolfdale CPU Power Status and max current table

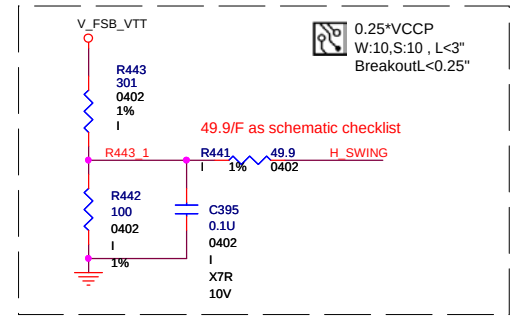
POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC_CORE	O	X	X	VID	100A	Yorkfield@65W
VCC_CORE	O	X	X	VID	75A	Wolfdale
VTT	O	X	X	VCC1.2	4.6A	After VCC stable
VTT	O	X	X	VCC1.2	4.5A	Before VCC stable
VCC_PLL	O	X	X	VCC1.5	260mA	

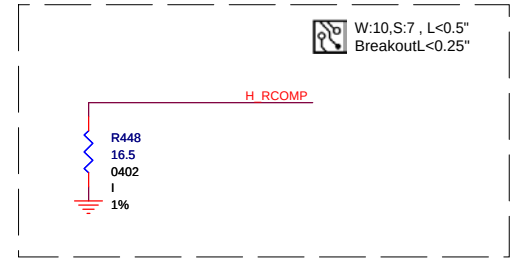


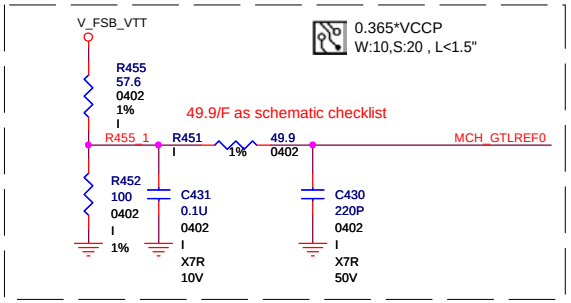
C-step Erratum for PSI

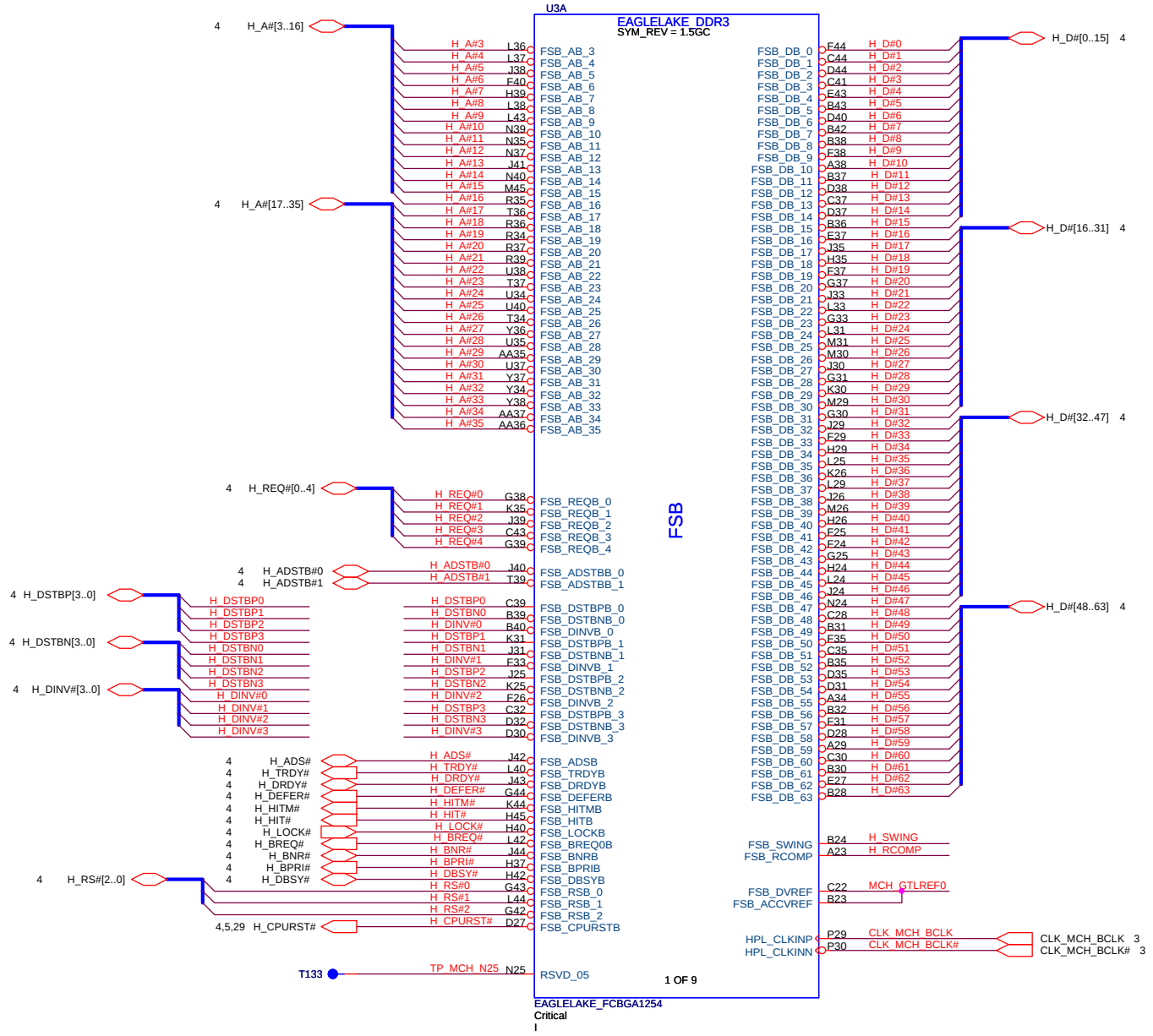
Quanta Computer Inc.
PROJECT : ZN5

Size	Document Number	Rev
	CPU(2/2)- Power	X4
Date: Friday, March 05, 2010	Sheet 5 of 40	









Quanta Computer Inc.	
PROJECT : ZN5	
Size	Document Number: NB (1/5) HOST — Rev: X4
Date: Friday, March 05, 2010	Sheet 6 of 40

SDVO -> LVDS

H:SDVO TO LVDS
L:for MXM lane

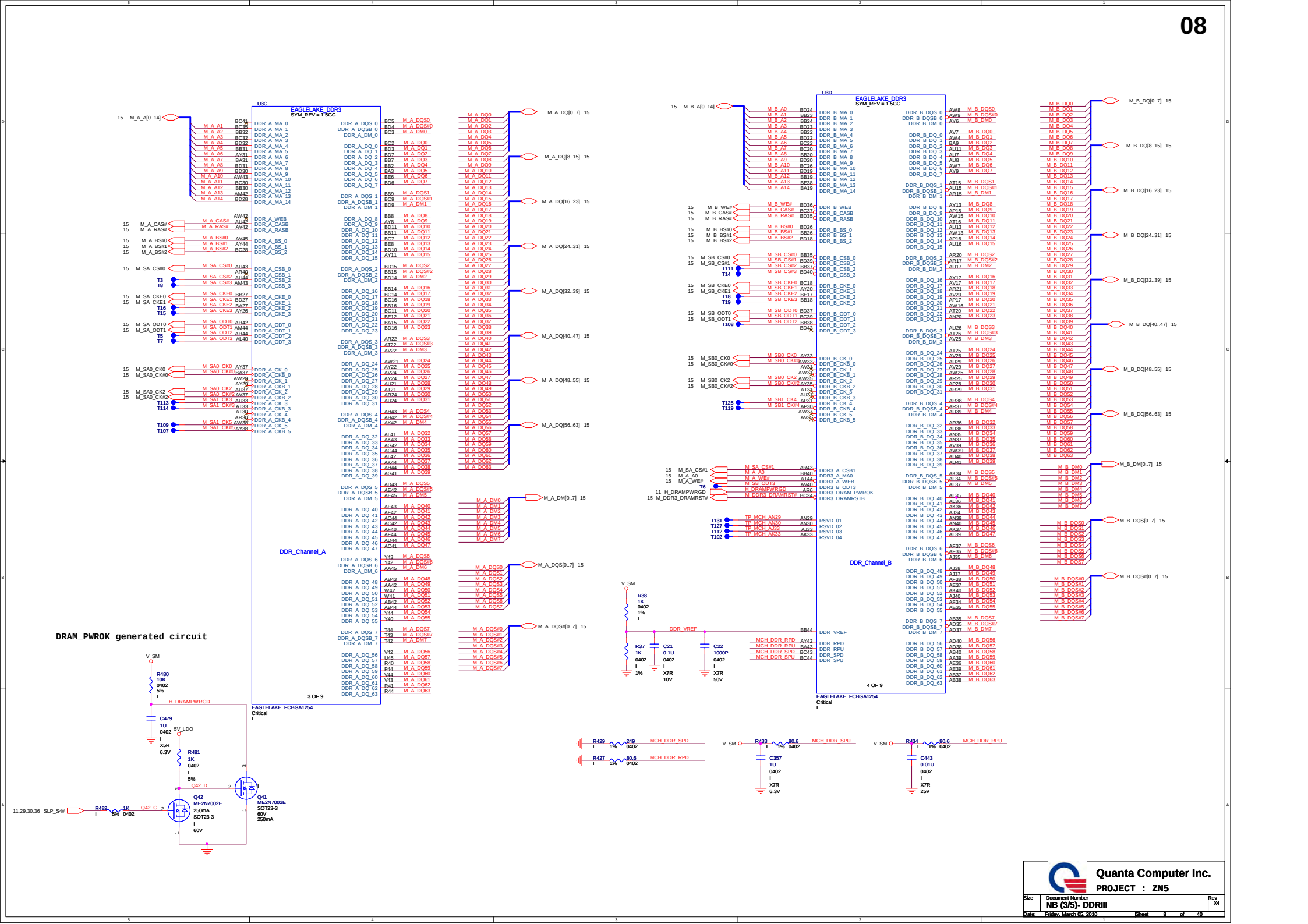
H:PCIE to DP
L:For MXM lane to DP

CLPWROK sequence request
1. asserted after VCC_CL ramp to 1.0V
2. asserted before PWROK

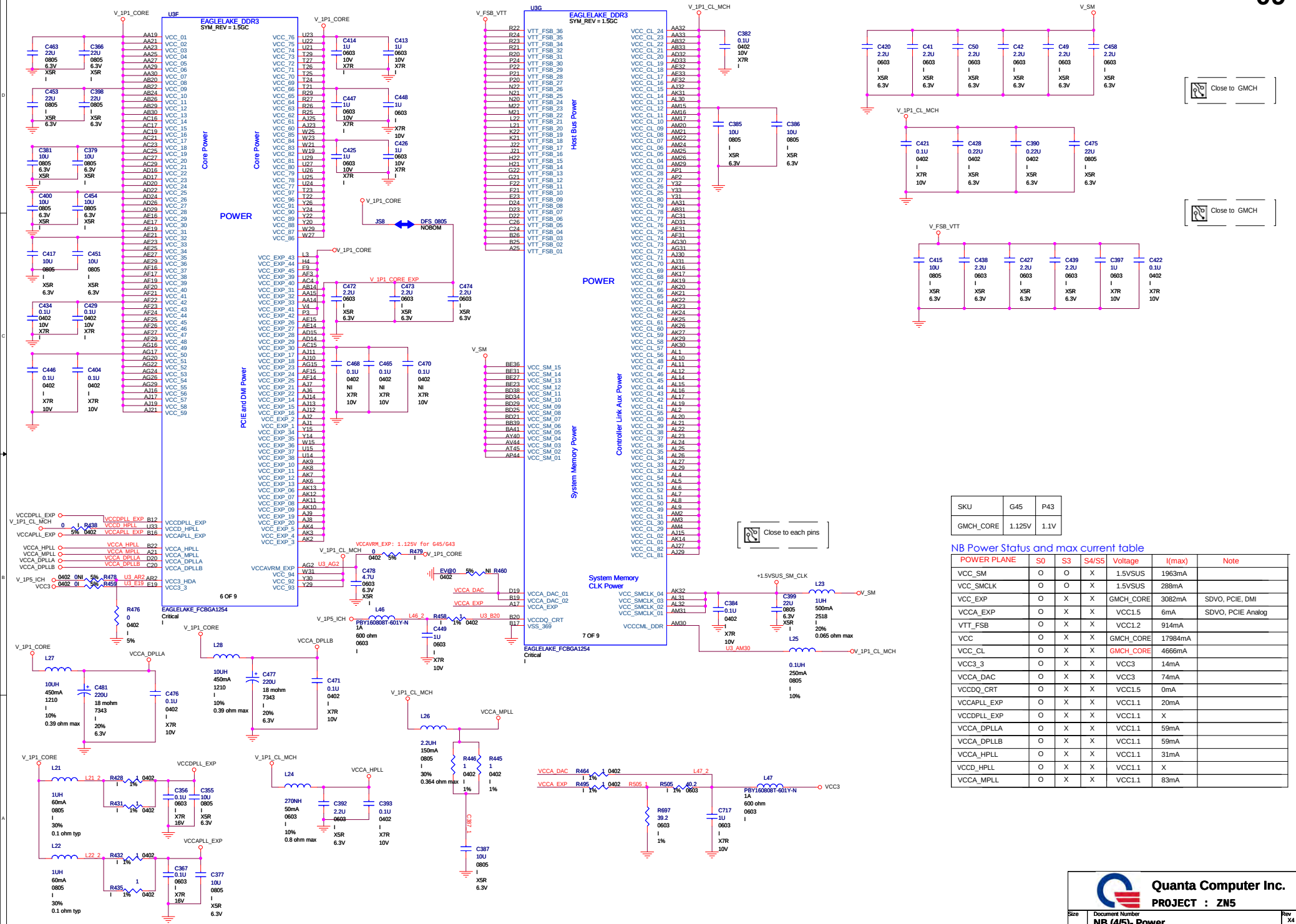
Enable Digital Port B
had PU 5.6K to VCC2.5 on CH7308 side
need to check with intel

ICH_DPRSTP#
The Daisy chain topology should be routed from ICH10 to IMVP , then to (G)MCH and CPU, in that order.

Quanta Computer Inc.	
PROJECT : ZN5	
Size	Document Number: NB (2/5)- VGA, DMI, PCIE — Rev: X4
Date: Friday, March 05, 2010	Sheet 7 of 40



Quanta Computer Inc.			
PROJECT : ZN5			
Size	Document Number		Rev
	NB (3/5)- DDRIII		X4
Date: Friday, March 05, 2010		Sheet 8 of 40	



SKU	G45	P43
GMCH_CORE	1.125V	1.1V

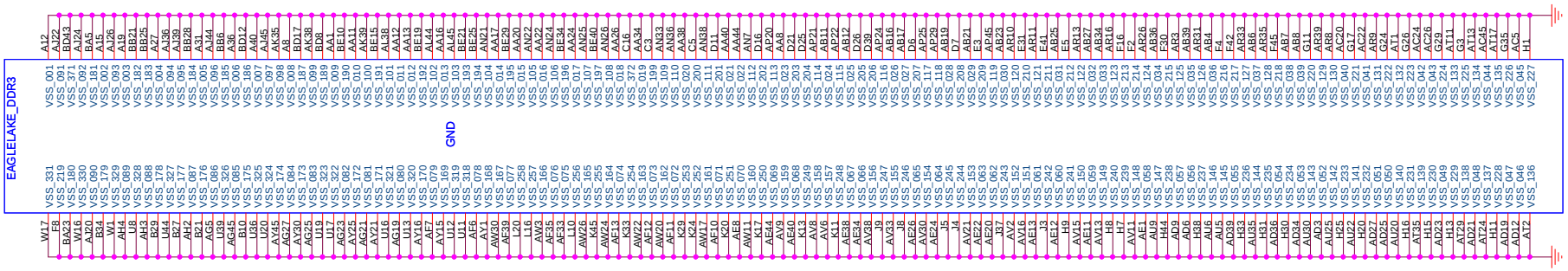
NB Power Status and max current table

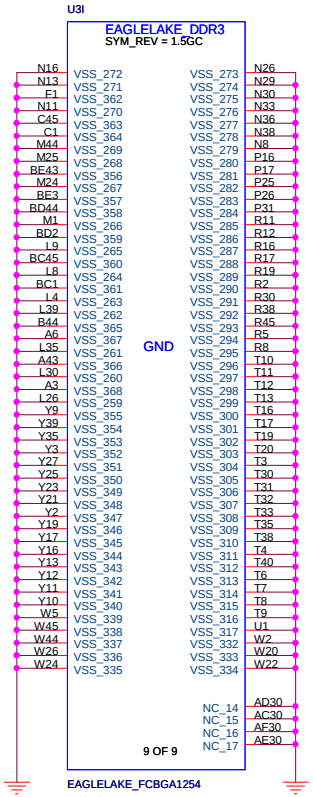
POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC_SM	O	O	X	1.5VSUS	1963mA	
VCC_SMCLK	O	O	X	1.5VSUS	288mA	
VCC_EXP	O	X	X	GMCH_CORE	3082mA	SDVO, PCIE, DMI
VCCA_EXP	O	X	X	VCC1.5	6mA	SDVO, PCIE Analog
VTT_FSB	O	X	X	VCC1.2	914mA	
VCC	O	X	X	GMCH_CORE	17984mA	
VCC_CL	O	X	X	GMCH_CORE	4666mA	
VCC3_3	O	X	X	VCC3	14mA	
VCCA_DAC	O	X	X	VCC3	74mA	
VCCDQ_CRT	O	X	X	VCC1.5	0mA	
VCCAPLL_EXP	O	X	X	VCC1.1	20mA	
VCCDPLL_EXP	O	X	X	VCC1.1	X	
VCCA_DPLLA	O	X	X	VCC1.1	59mA	
VCCA_DPLLB	O	X	X	VCC1.1	59mA	
VCCA_HPLL	O	X	X	VCC1.1	31mA	
VCCD_HPLL	O	X	X	VCC1.1	X	
VCCA_MPLL	O	X	X	VCC1.1	83mA	

Quanta Computer Inc.
PROJECT : ZN5

Size	Document Number	Rev
	NB (4/5)- Power	X4

Date: Friday, March 05, 2010 Sheet 9 of 40





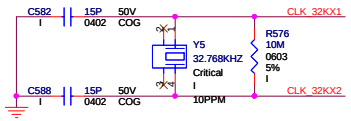
Quanta Computer Inc.

PROJECT : ZN5

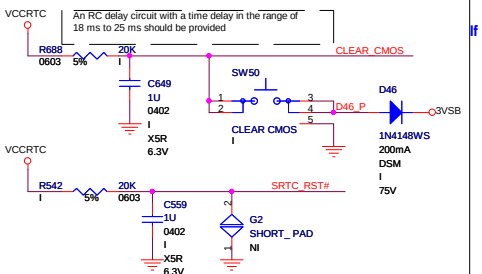
Size	Document Number	Rev
	NB (5/5)- VSS	X4
Date: Friday, March 05, 2010	Sheet 10 of 40	

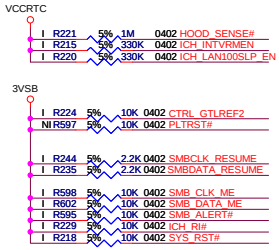
ROM recovery

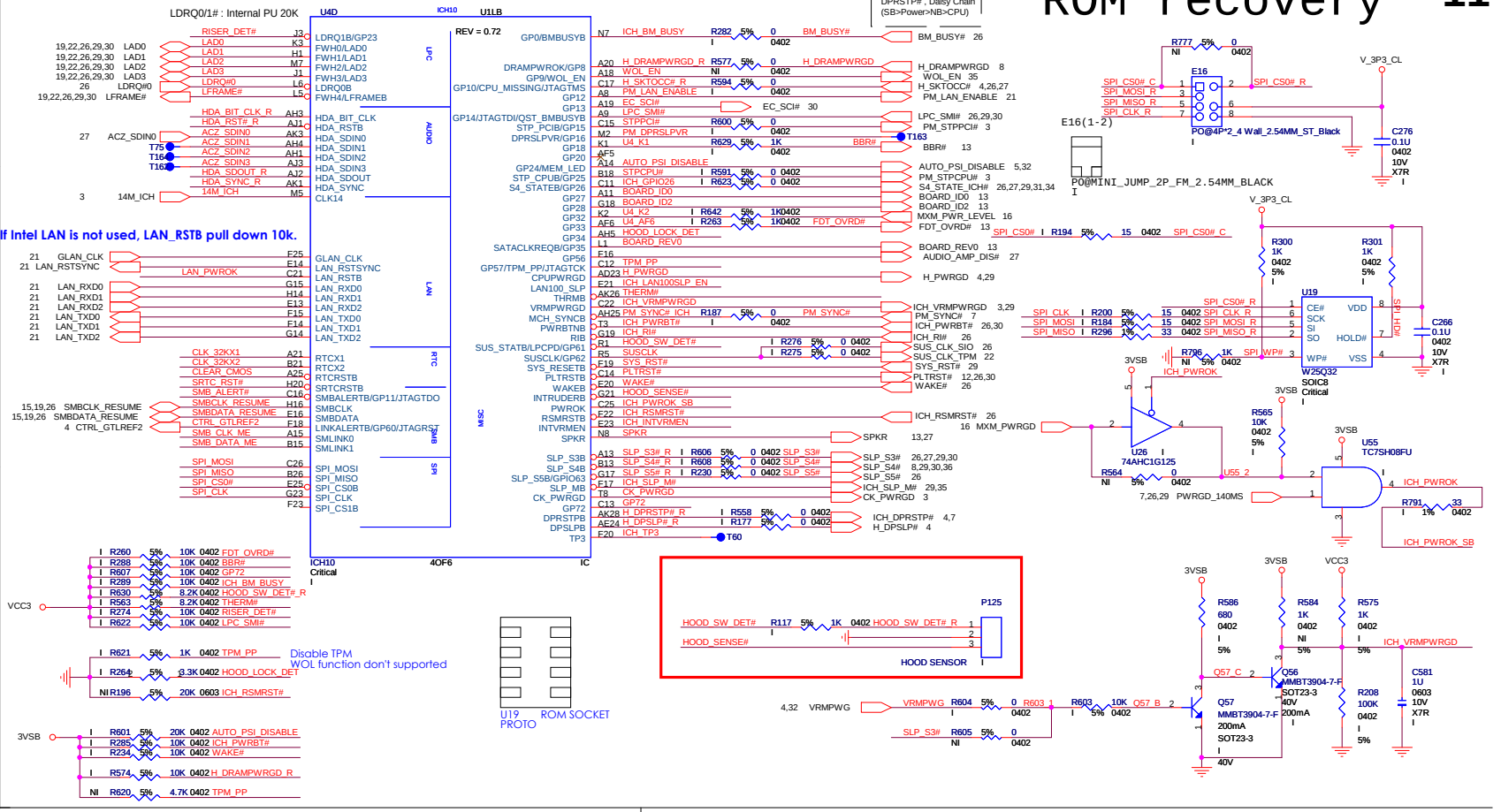
RTC CRYSTAL



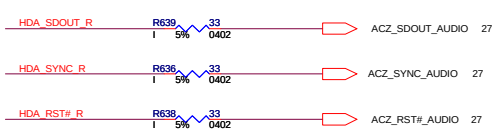
RESET JUMP

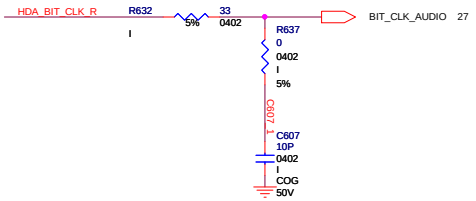






HD Audio I/F(CODEC& iHDMI)



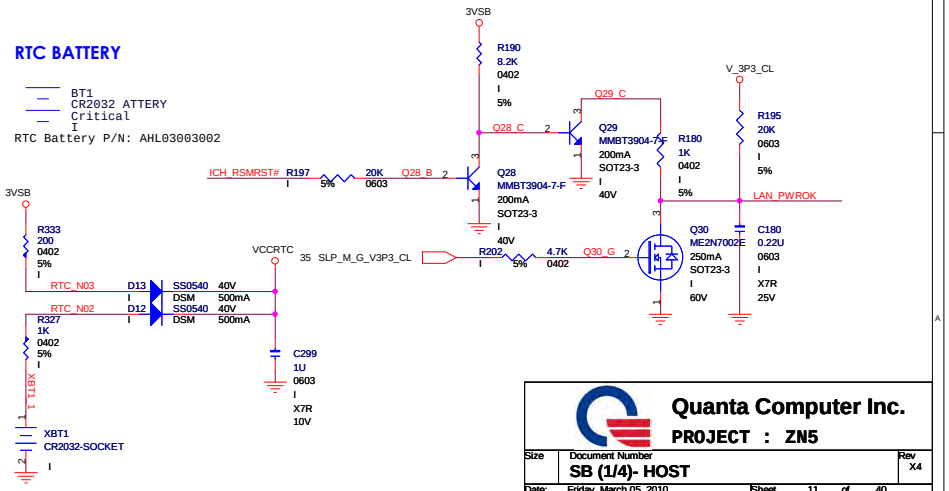


South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	ICH_TP3 R228 NI 1K 0402	
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK	HDA_SDOUT_R R633 NI 3.3K 0402 +3V_HDA_IO_ICH	

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

RTC BATTERY

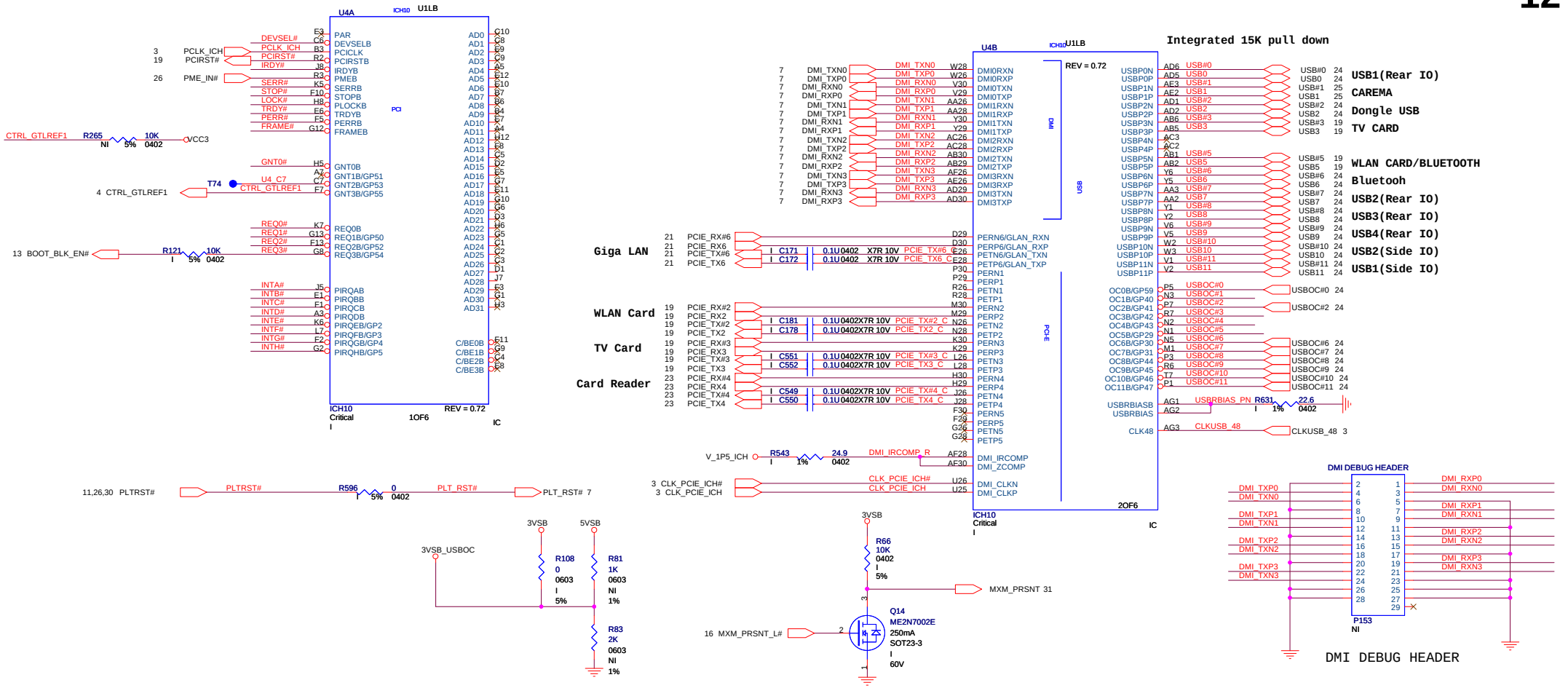


Quanta Computer Inc.
PROJECT : ZN5

Size	Document Number	Rev
	SB (1/4)- HOST	X4

Date: Friday, March 05, 2010 Sheet 11 of 40

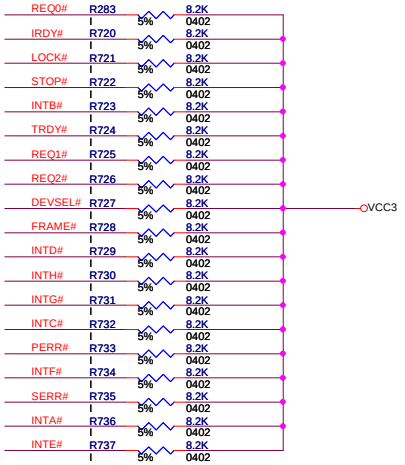
PCI/PCI-E/USB/DMI/SPI



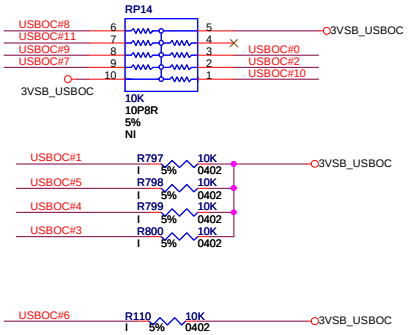
South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	CTRL_GTLREF1 R266 1K NI 5% 0402
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI(Default)	GNT0# R270 1K NI 5% 0402 VCC3 R271 1K I 5% 0402
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1 / 0 / PCI 1 / 1 / LPC	

PCI PULL-UP



USBOC# PULL-UP

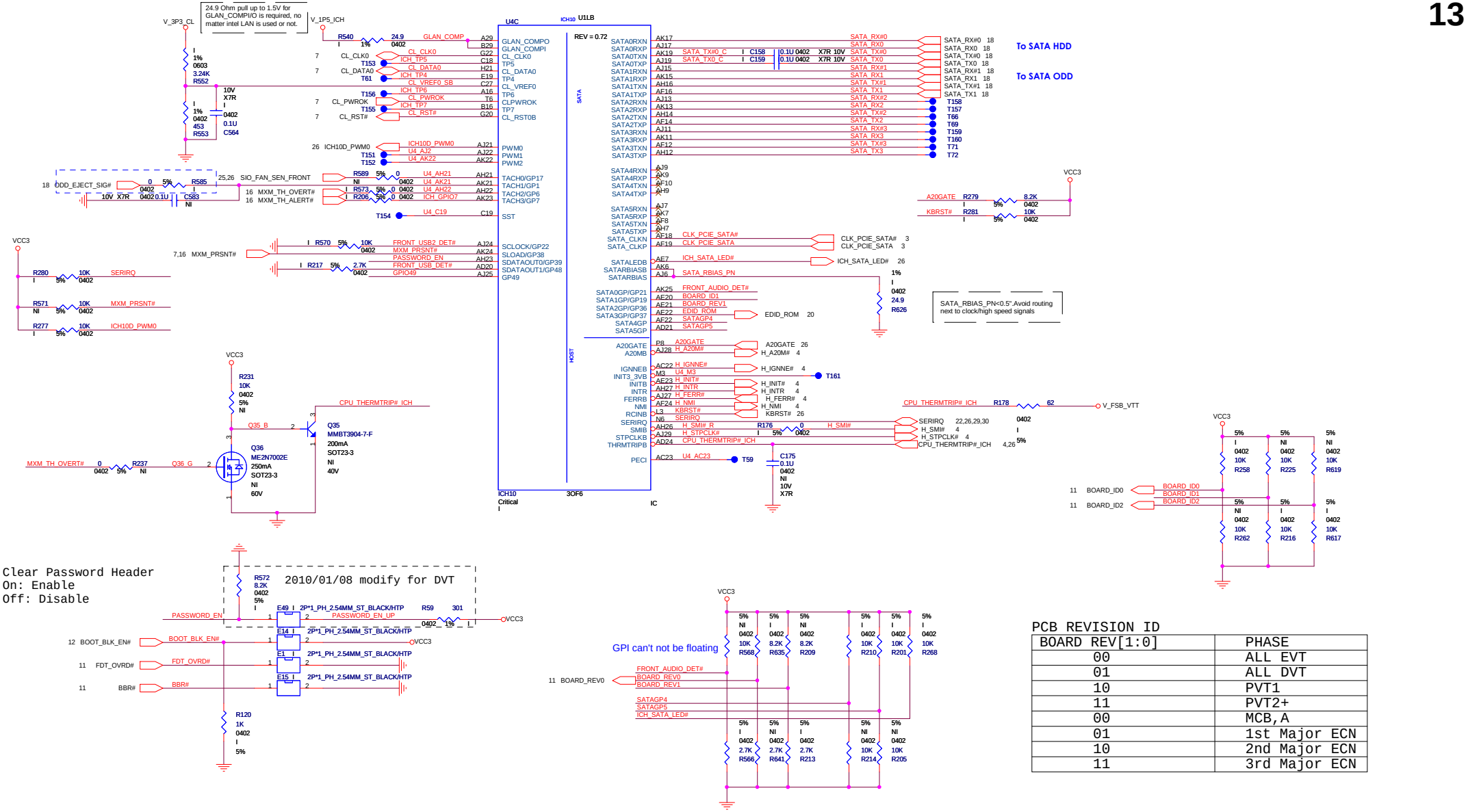


Quanta Computer Inc.

PROJECT : ZN5

Size	Document Number	Rev
	SB (2/4) PCIE/PCI/USB/DMI	X4

Date: Friday, March 05, 2010 Sheet 12 of 40



Clear Password Header
On: Enable
Off: Disable

PCB REVISION ID

BOARD REV[1:0]	PHASE
00	ALL EVT
01	ALL DVT
10	PVT1
11	PVT2+
00	MCB,A
01	1st Major ECN
10	2nd Major ECN
11	3rd Major ECN

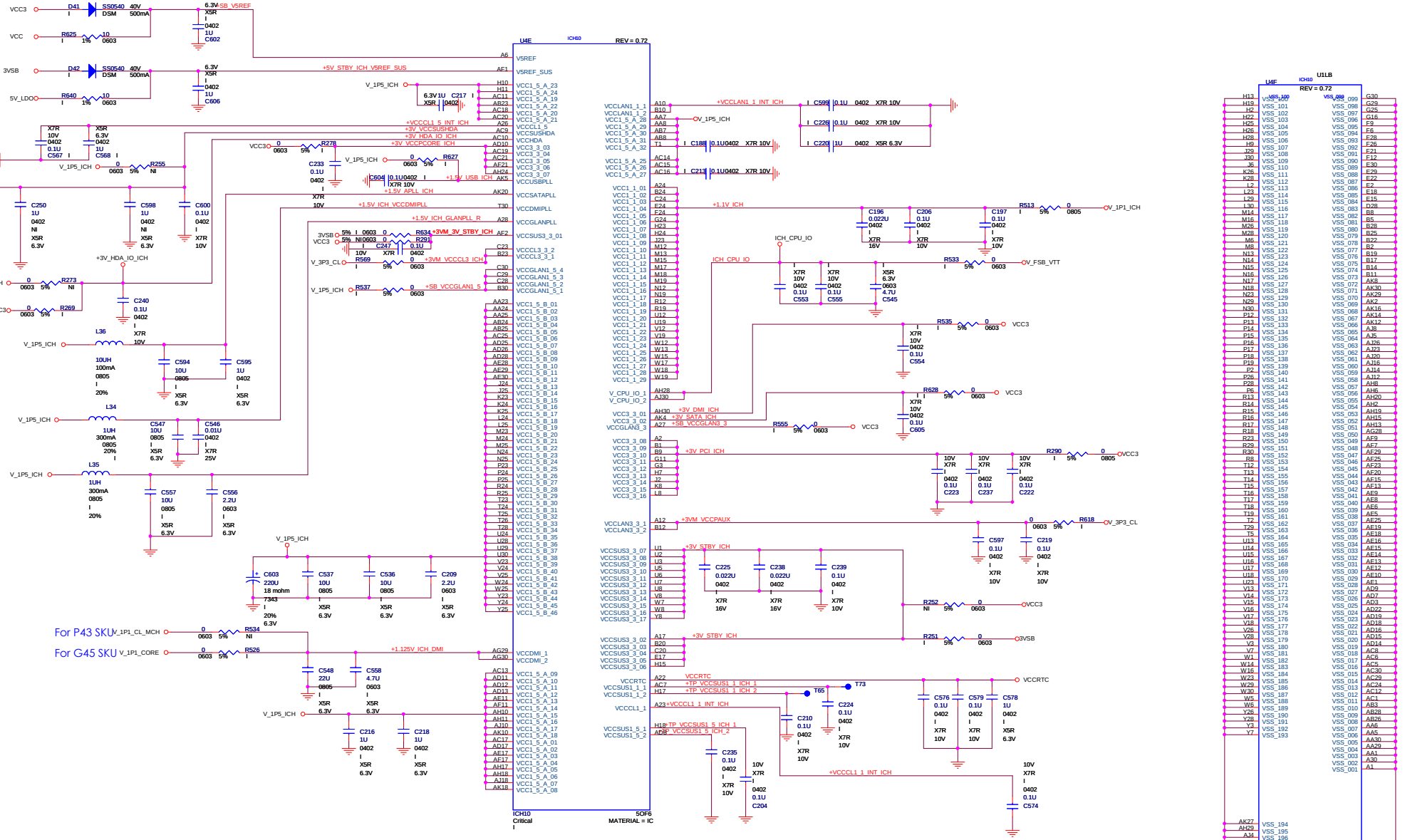
South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	SPKR R284 1K 0402 VCC3
GPIO49	DMI Termination Voltage	PWROK	0 = AC coupled 1 = DC coupled Internal PU	GPIO49 R562 1K 0402

Quanta Computer Inc.
PROJECT : ZN5

Size	Document Number	Rev
	SB(3/4) SATA/GPIO	X4

Date: Friday, March 05, 2010 Sheet 13 of 40



SB Power Status and max current table(1/2)

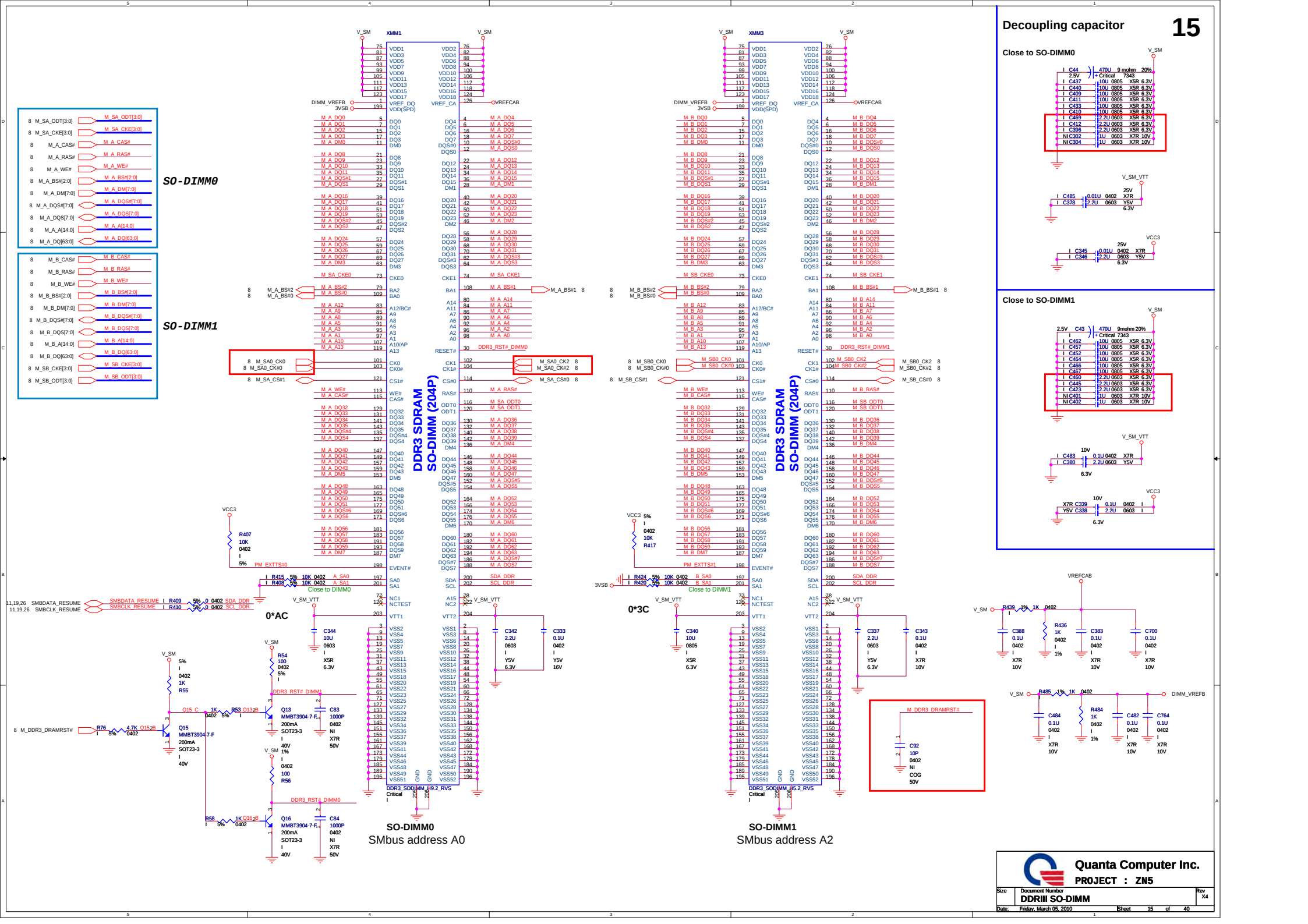
POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCCRTC	X	X	X	VCCRTC	6uA	6uA@G3
V5REF	O	X	X	VCC5	2mA	
V5REF_SUS	O	O	O	5V_STBY	2mA	2mA@S0,1mA@S3/S5
VCC1_5_B	O	X	X	VCC1.5	646mA	
VCCSATAPLL	O	X	X	VCC1.5	47mA	
VCC1_5_A	O	X	X	VCC1.5	1644mA	
VCCUSBPLL	O	X	X	VCC1.5	11mA	
VCCLAN1_1	X	X	X	1.1V	X	Internal VR powered, S3/S5 powered when AMT actived
VCCLAN3_3	O	X	X	VCC3	78mA	78mA@S3/S5 powered when AMT actived
VCCGLANPLL	O	X	X	VCC1.5	23mA	
VCCGLAN1_5	O	X	X	VCC1.5	80mA	
VCCGLAN3_3	O	X	X	VCC3	1mA	

SB Power Status and max current table(2/2)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC1_1	O	X	X	VCC1.1	1.634A	ICH CORE
VCCDMIPLL	O	X	X	VCC1.5	23mA	
VCC_DMI	O	X	X	GMCH_CORE	50mA	1.125V@G45, 1.1V@P43
V_CPU_IO	O	X	X	VCC1.2	2mA	
VCC3_3	O	X	X	VCC3	308mA	
VCCHDA	O	X	X	VCC1.5	70mA	
VCCSUSHDA	O	O	O	RVCC1.5	70mA	
VCCSUS1_1	X	X	X	1.1V	X	Internal VR powered
VCCSUS1_5	X	X	X	1.5V	X	Internal VR powered
VCCSUS3_3	O	O	O	3V_STBY	212mA	53mA@S3/S5
VCCCL1_1	X	X	X	1.1V	X	Internal VR powered
VCCCL1_5	X	X	X	1.5V	X	Internal VR powered
VCCCL3_3	O	X	X	VCC3	73mA	S3/S5 powered when AMT actived

Quanta Computer Inc.
PROJECT : ZN5

Size	Document Number	Rev
	SB(4/4) POWER/VSS	X4
Date: Friday, March 05, 2010	Sheet 14 of 40	


Decoupling capacitor
15
Close to SO-DIMM0
Close to SO-DIMM1
SO-DIMM0
SO-DIMM1
DDR3 SDRAM SO-DIMM (204P)
XMM1
XMM3
SO-DIMM0
SMbus address A0
SO-DIMM1
SMbus address A2
0*AC
0*3C
Close to DIMM0
Close to DIMM1
Quanta Computer Inc.
PROJECT : ZN5
DDRIII SO-DIMM
Friday, March 05, 2010
Sheet 15 of 40

MXM Module

MXM_PRSNT#	Sku
Low	MXM
High	W/O MXM

DP_CAD	Behavior
Low	DP signal (AC couple)
High	TMDS signal (DC couple)

DisplayPort

DP connector

PS8325

MXM_LVDS_CONNECT

LVDS PIN Swap

MXM_ENABLE

MXM Reset

Swap pin

Change Footprint

To low power status mode

update MXM footprint to Mem-mm70-314-310b1-1-310p

max low power consumption for S5: 2uA

max low power consumption for S5: 2uA

Activate: H

MAINON

MXMPWR_EN

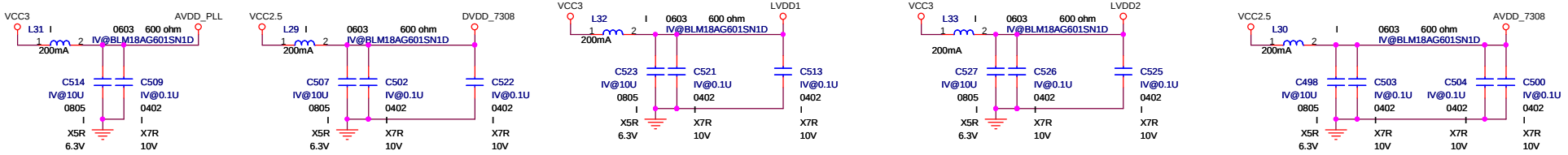
PLTRST#

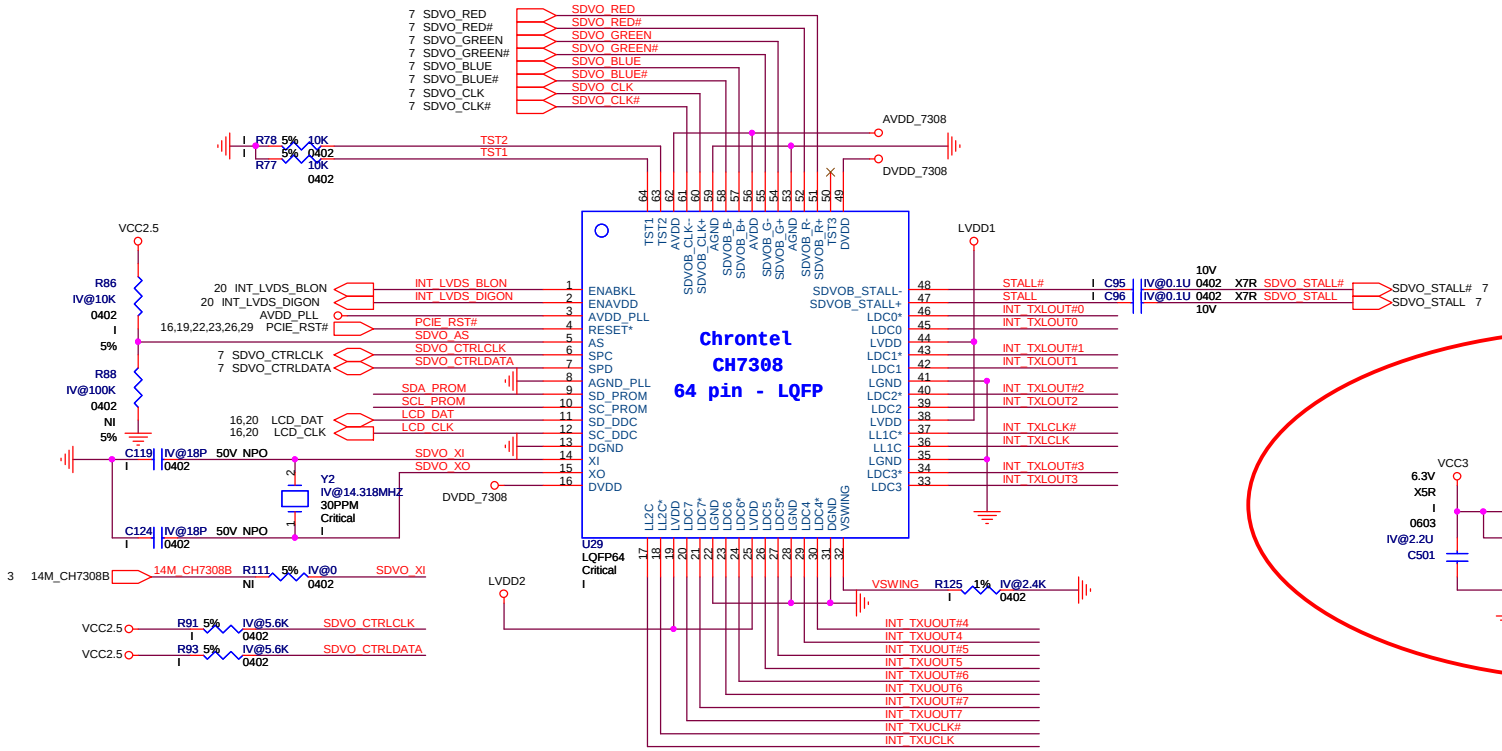
10Amp

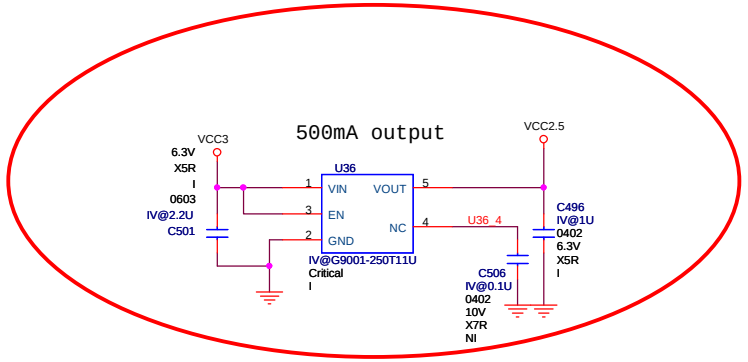
2.5Amp

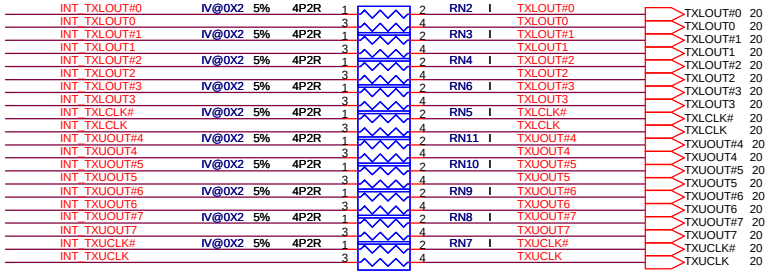
1Amp

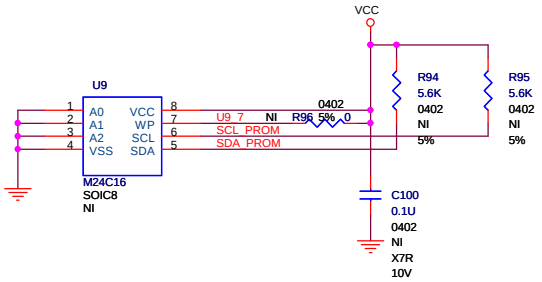
Quanta Computer Inc.
PROJECT : ZN5
Size: Document Number: MXM3.0
Rev: X4
Date: Friday, March 05, 2010 Sheet 16 of 40









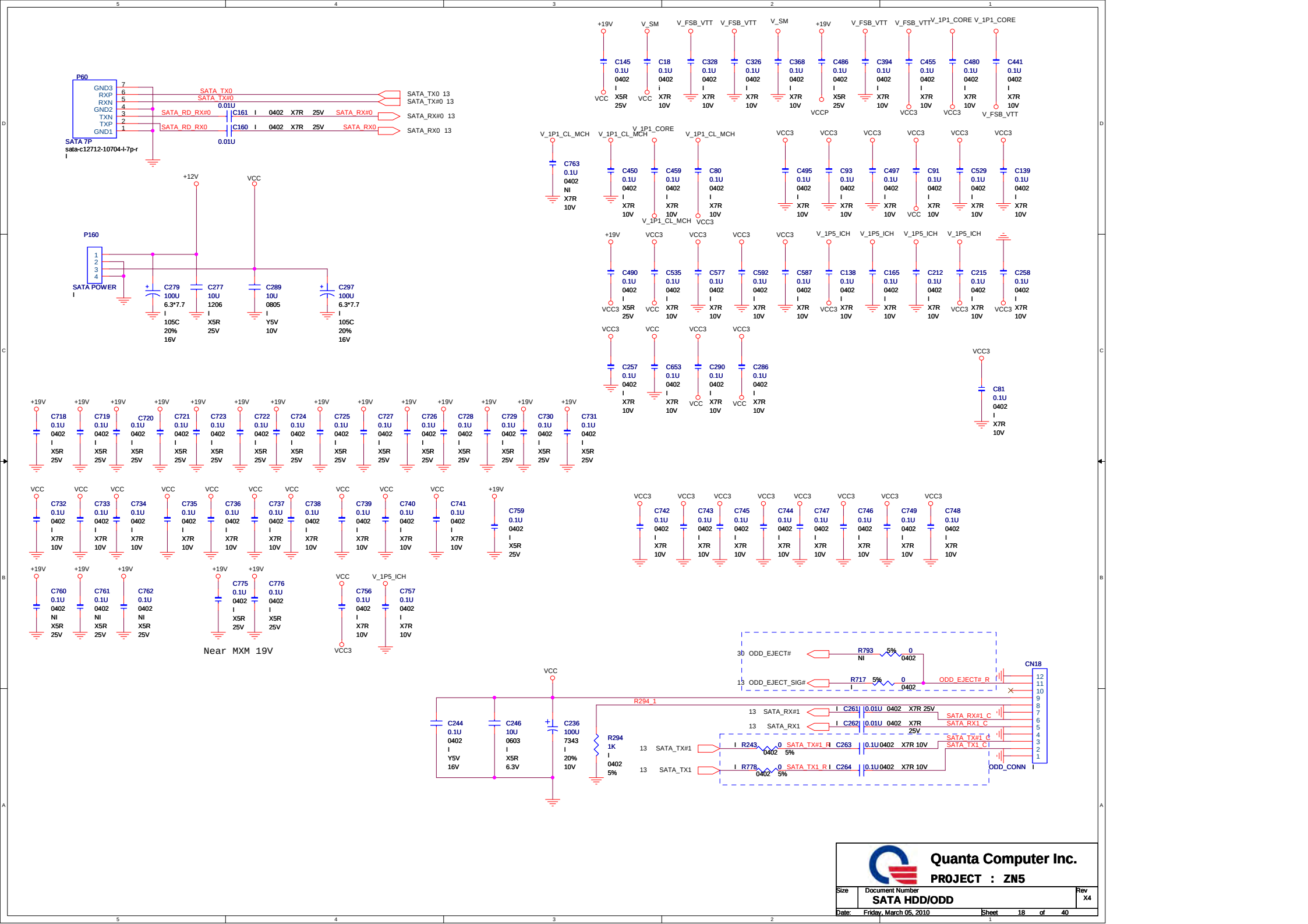


Quanta Computer Inc.

PROJECT : ZN5

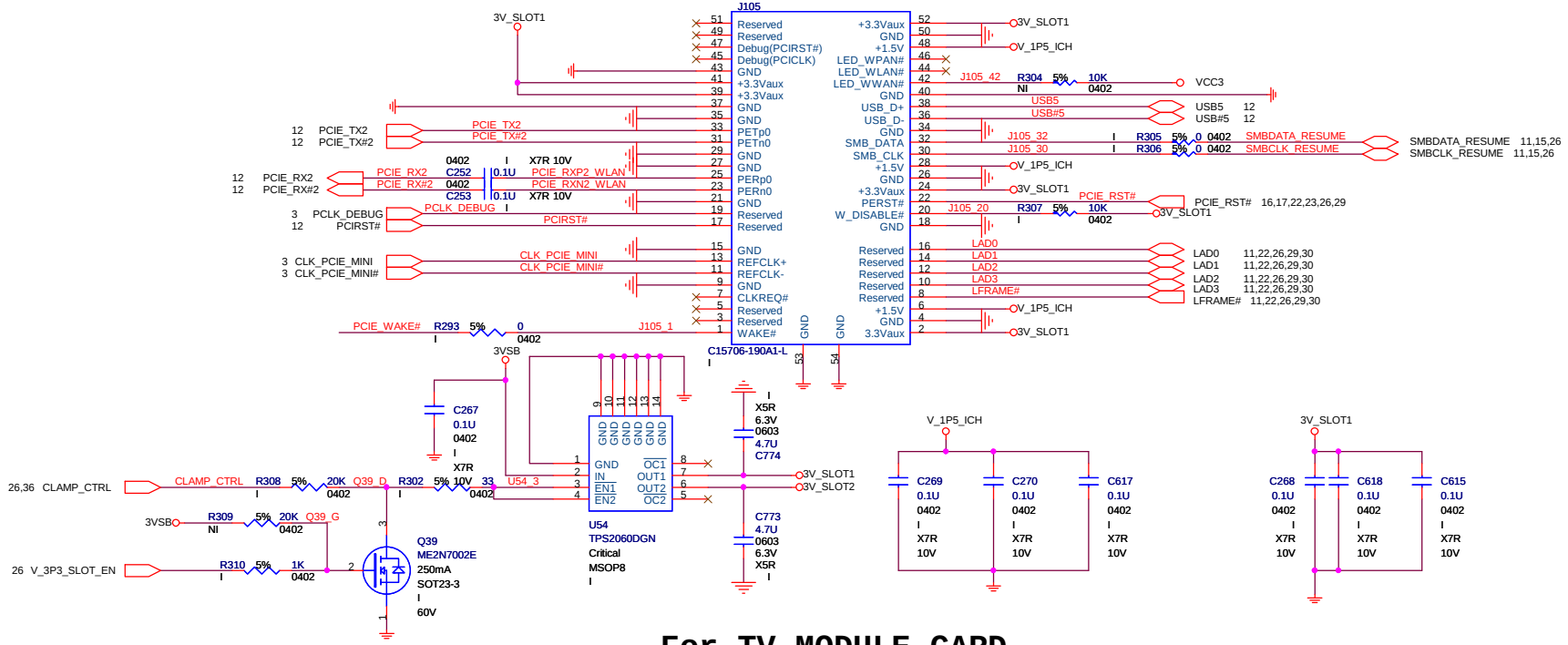
Size	Document Number	Rev
	LVDS TRANSMITTER	X4

Date: Friday, March 05, 2010 Sheet 17 of 40

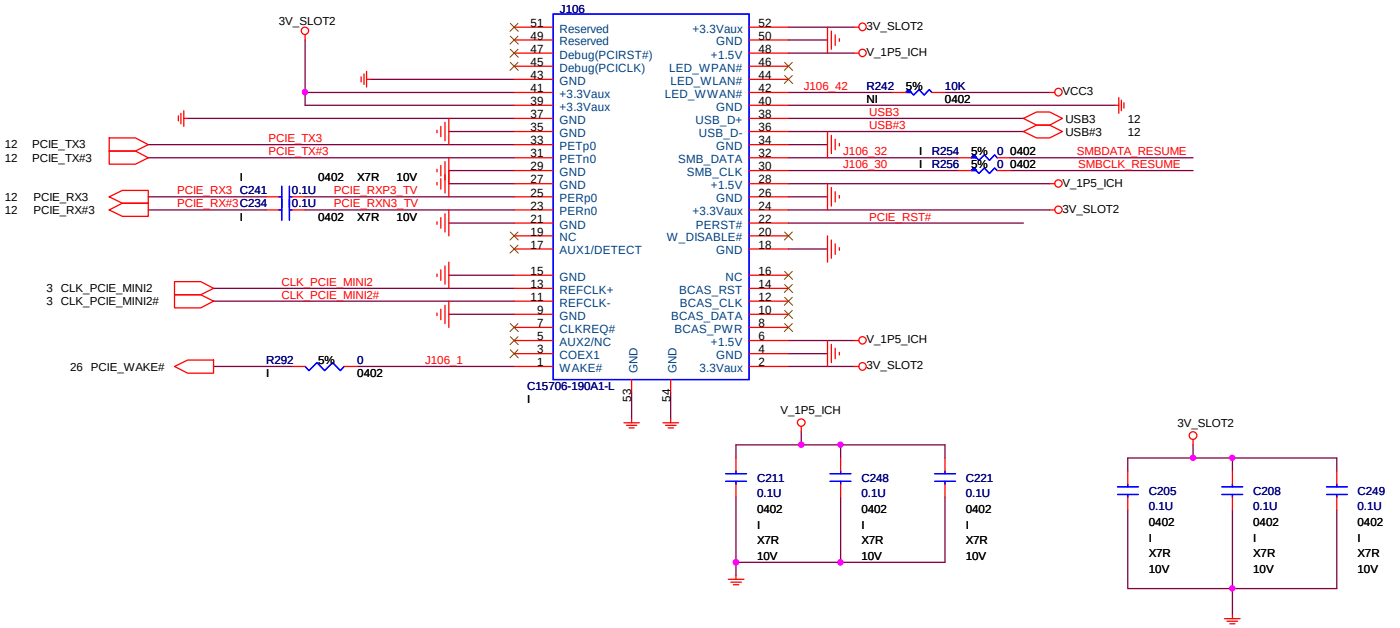


Quanta Computer Inc.		
PROJECT : ZN5		
Size	Document Number: SATA HDD/ODD	Rev: X4
Date: Friday, March 05, 2010	Sheet 18 of 40	

For wirlesss Lan card/Bluetooth



For TV MODULE CARD



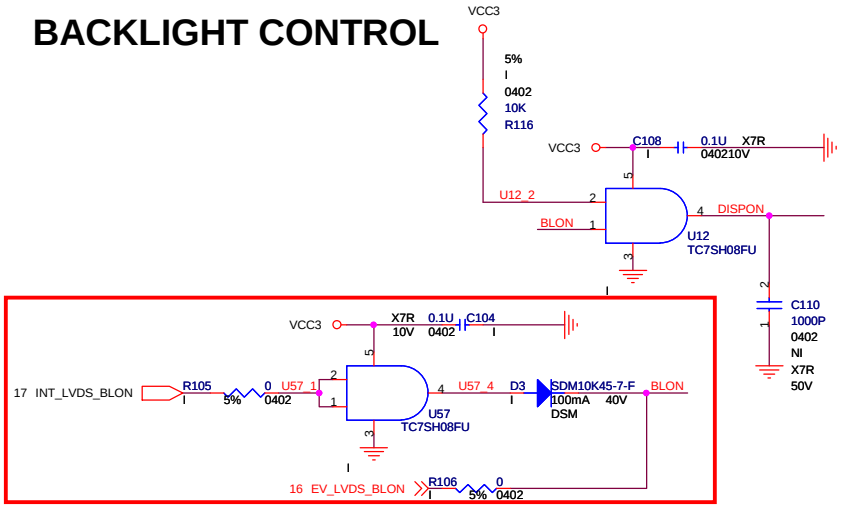
Quanta Computer Inc.

PROJECT : ZN5

Size	Document Number	Rev
	MINI PCIE(WLAN/TV)	X4

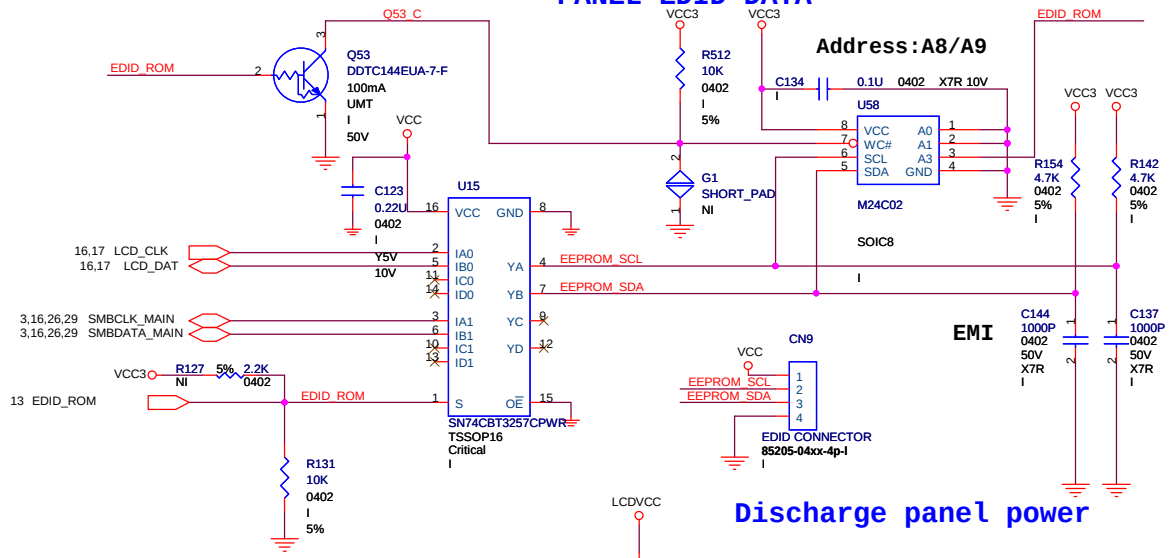
Date: Friday, March 05, 2010 Sheet 19 of 40

BACKLIGHT CONTROL

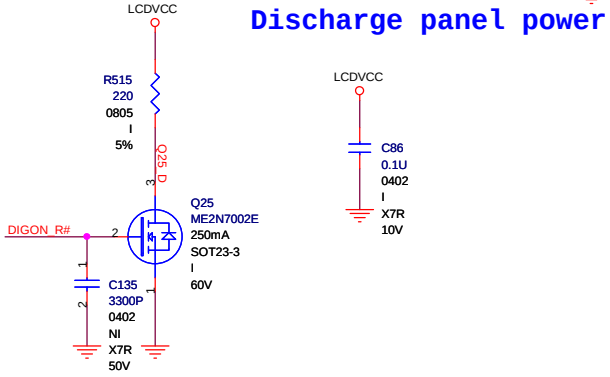


EEPROM IIC Selection

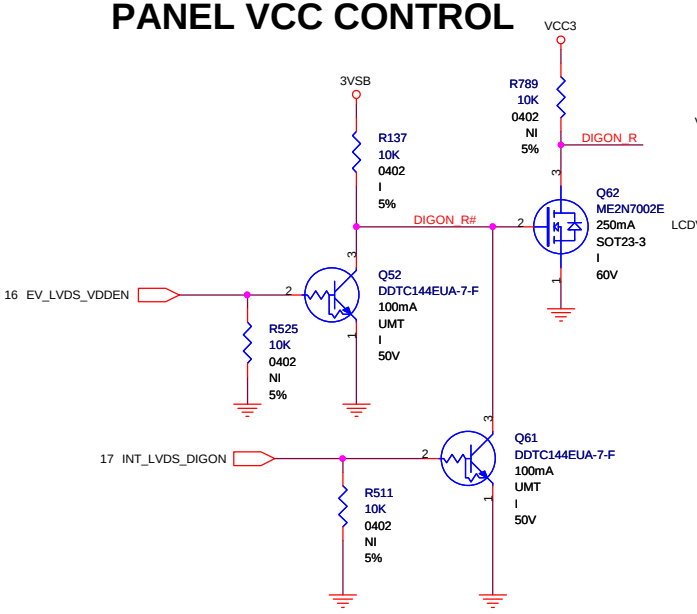
PANEL EDID DATA



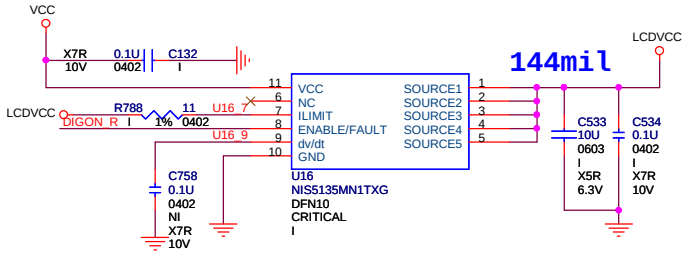
Discharge panel power



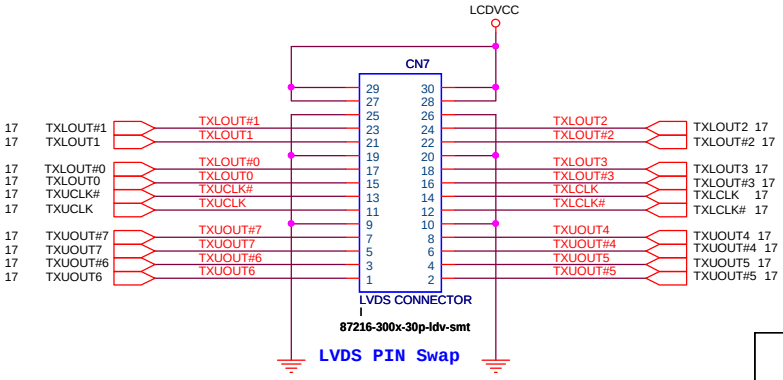
PANEL VCC CONTROL



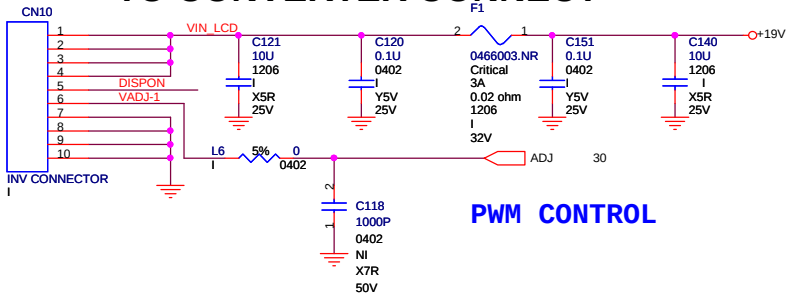
144mil



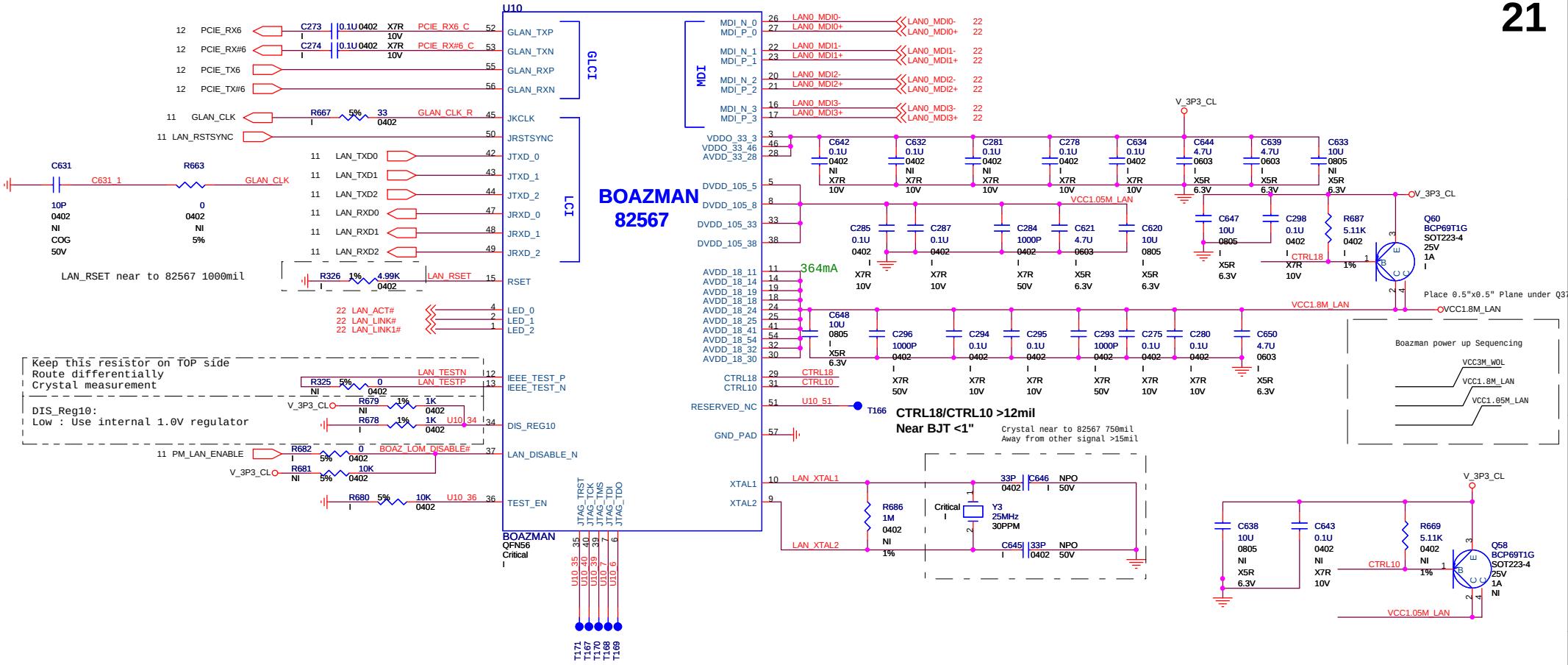
LCD PANEL CONNECTOR



TO CONVERTER CONNECT

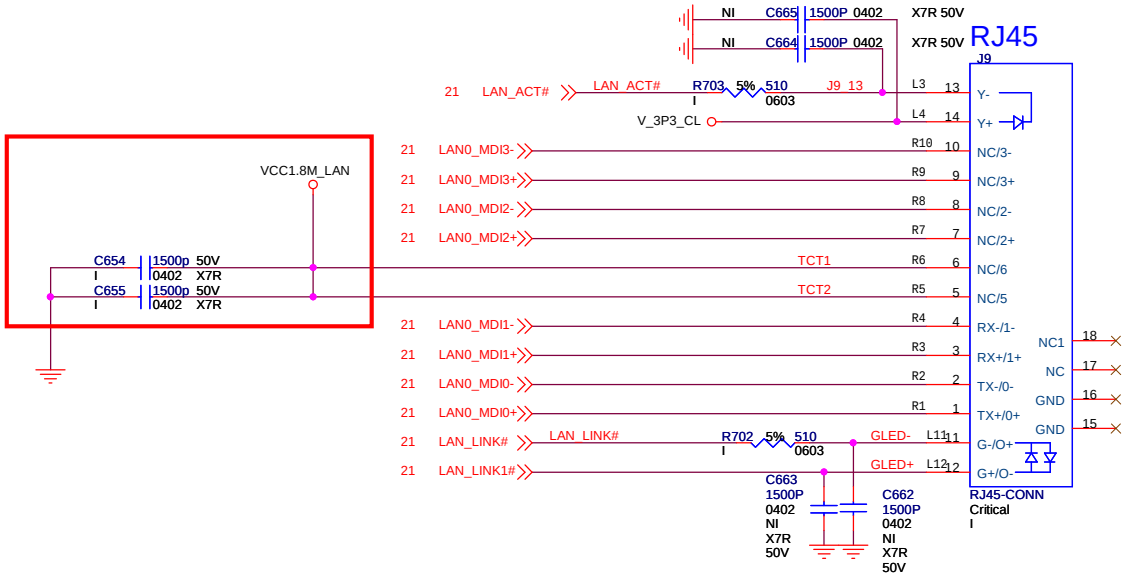


PWM CONTROL

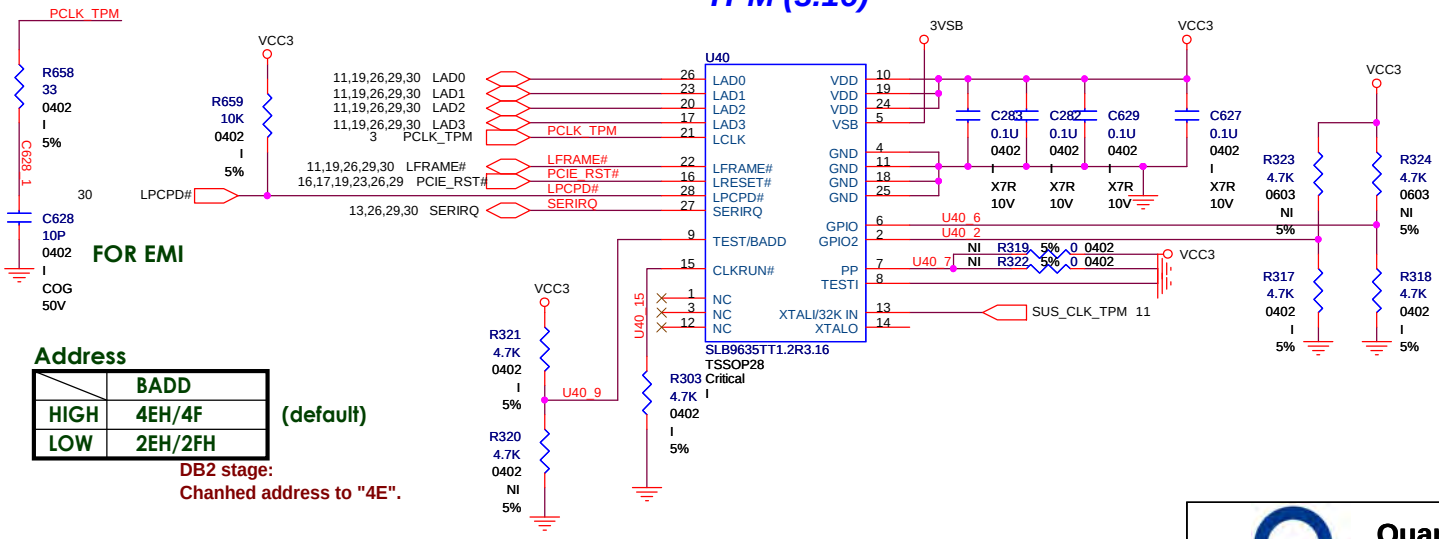


Quanta Computer Inc.			
PROJECT : ZN5			
Size	Document Number		Rev
	LAN BOAZMAN 82567		X4
Date: Friday, March 05, 2010	Sheet 21 of 40		

LAN Transformer & EOS CONN to RJ45



TPM (3.16)



Address

	BADD	
HIGH	4EH/4F	(default)
LOW	2EH/2FH	

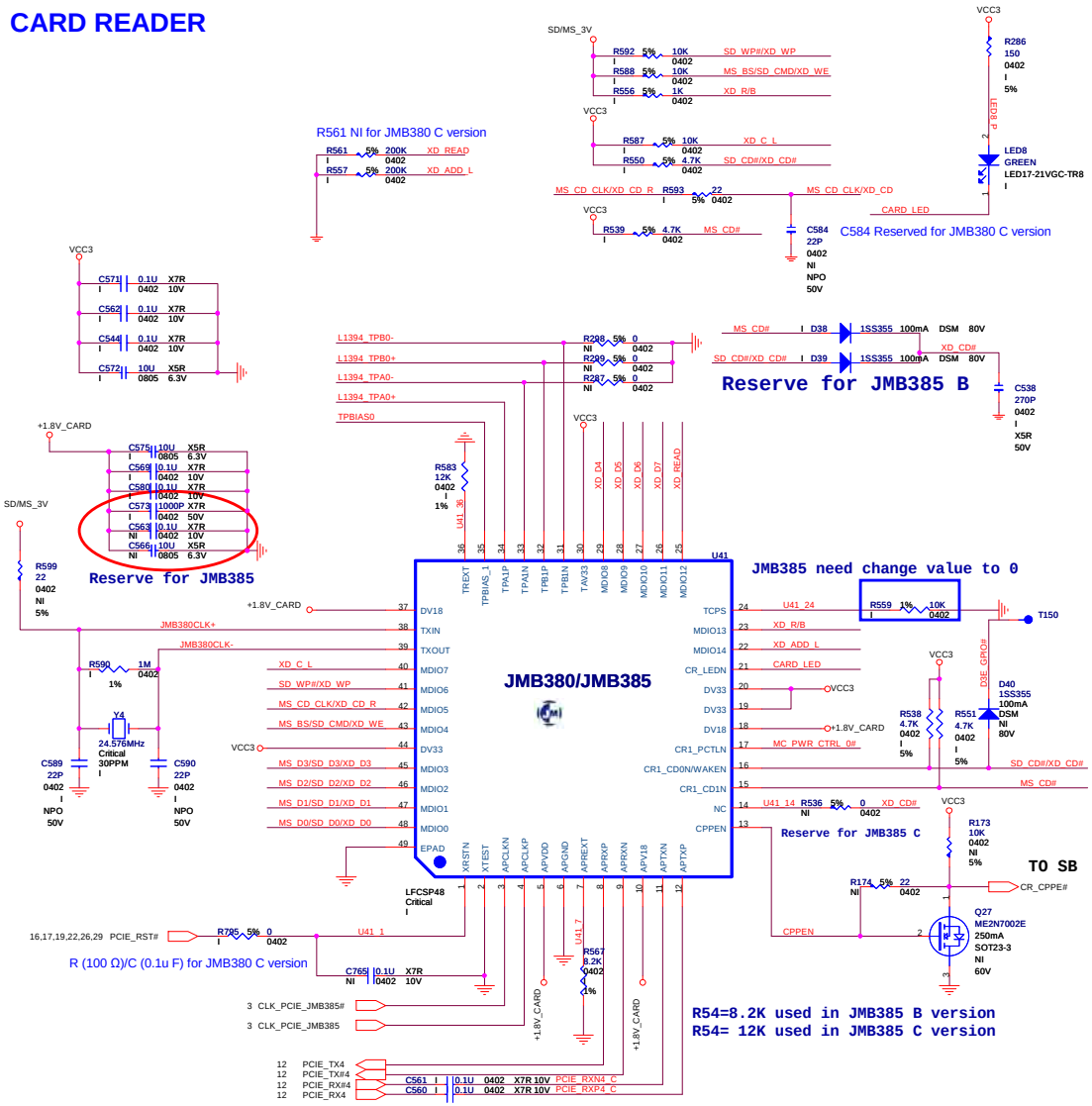
DB2 stage:
Chanhed address to "4E".

Quanta Computer Inc.
PROJECT : ZN5

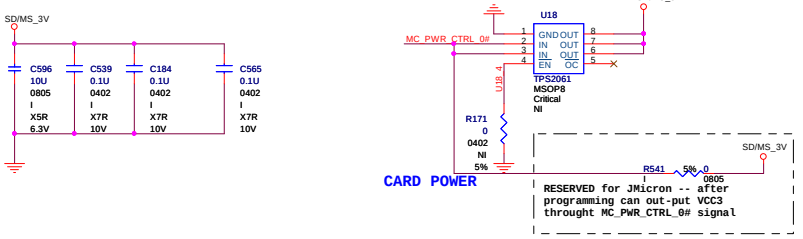
Size	Document Number	Rev
	TPM & RJ45 with LAN Transformer	X4

Date: Friday, March 05, 2010 Sheet 22 of 40

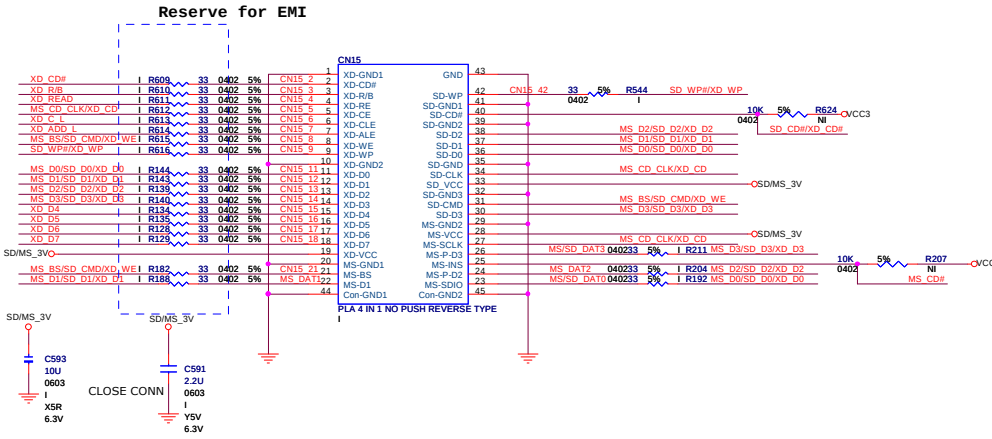
CARD READER



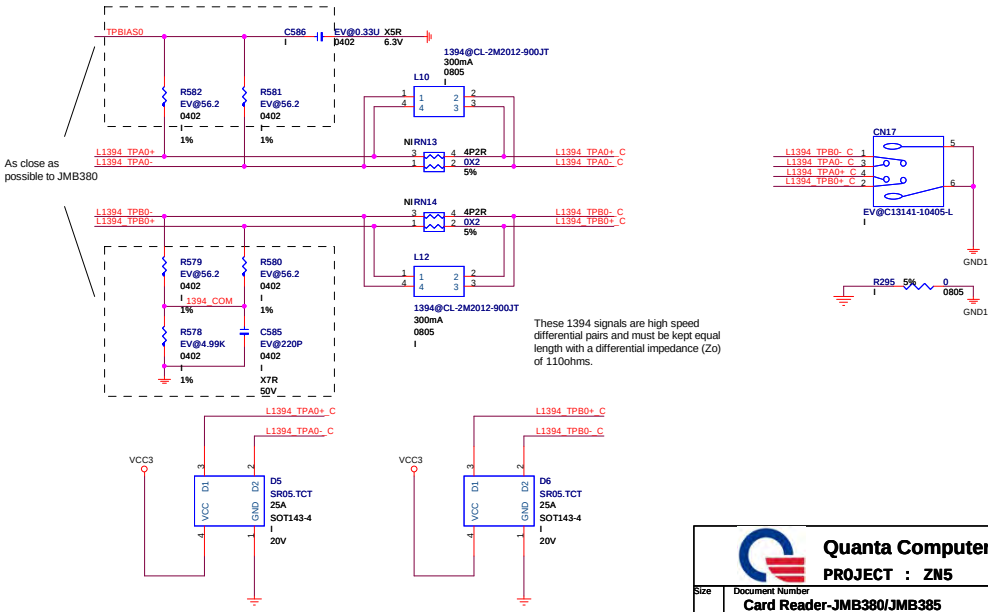
CARDREADER POWER



4 IN 1 CONN



1394



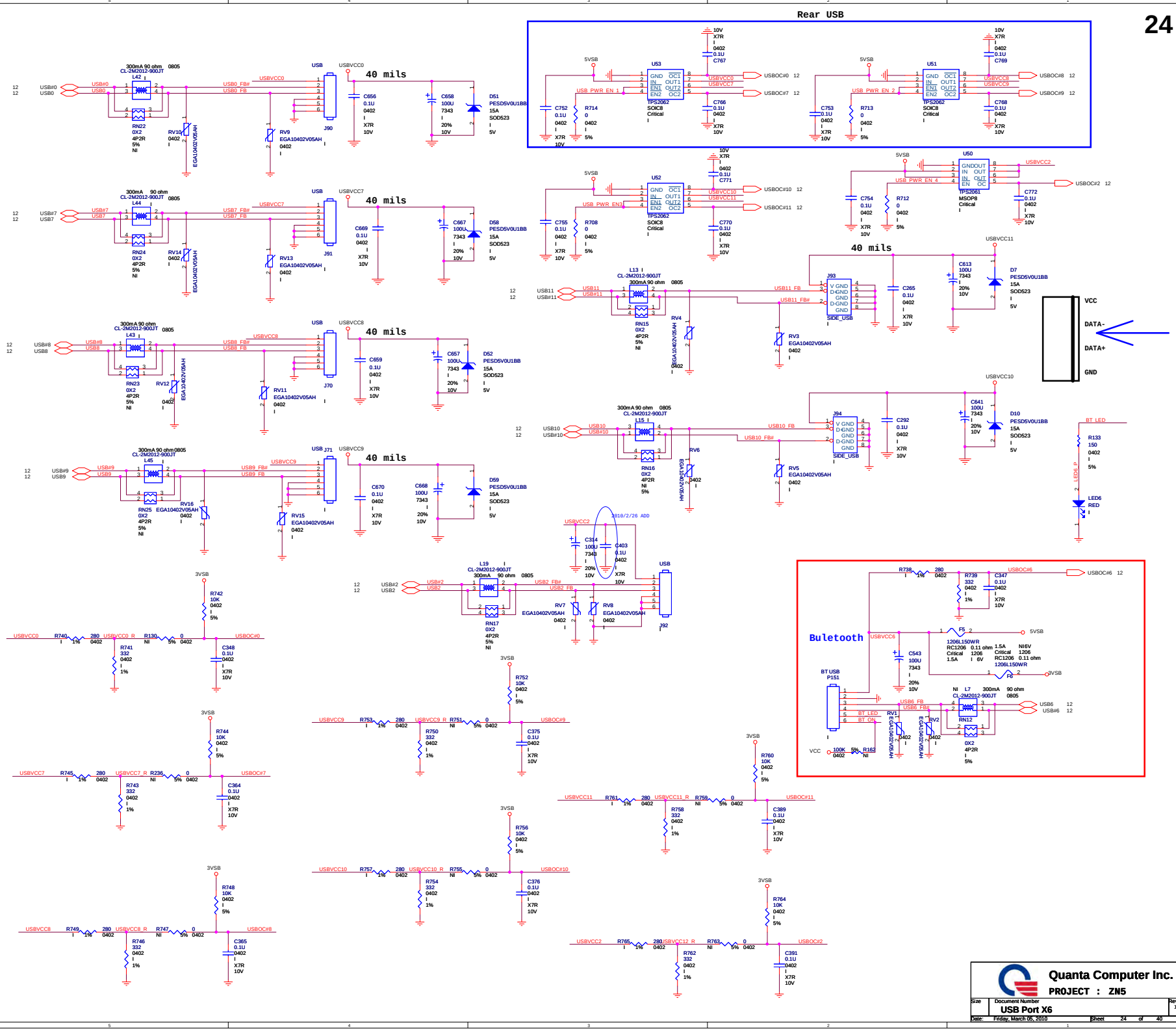
Quanta Computer Inc.

PROJECT : ZN5

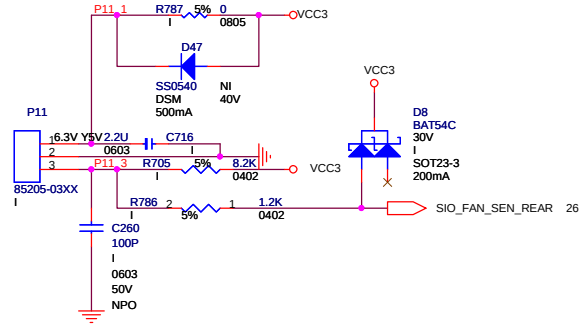
Size	Document Number	Rev
	Card Reader-JMB380/JMB385	X4

Date: Friday, March 05, 2010 Sheet 23 of 40

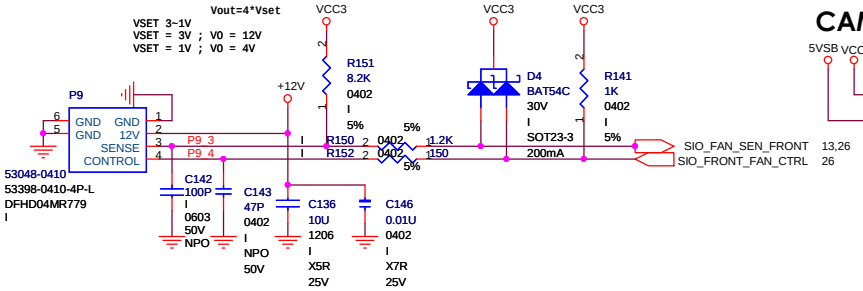
Rear USB


300mA 90 ohm 0805
CL-2M2012-900JT
USB
USBVCC0
40 mils
USB#0
USB0
USB0_FB#
USB0_FB
RN22 0X2 4P2R 5% NI
RV10 0402
EGA10402V05AH
RV9 EGA10402V05AH 0402
J90
C656 0.1U 0402 X7R 10V
C658 100U 7343 20% 10V
D51 PESD5V0U1BB 15A SOD523 5V
USBVCC7
USB#7
USB7
USB7_FB#
USB7_FB
RN24 0X2 4P2R 5% NI
RV14 0402
RV13 EGA10402V05AH 0402
J91
C669 0.1U 0402 X7R 10V
C667 100U 7343 20% 10V
D58 PESD5V0U1BB 15A SOD523 5V
USBVCC8
USB#8
USB8
USB8_FB#
USB8_FB
RN23 0X2 4P2R 5% NI
RV12 0402
RV11 EGA10402V05AH 0402
J70
C659 0.1U 0402 X7R 10V
C657 100U 7343 20% 10V
D52 PESD5V0U1BB 15A SOD523 5V
USBVCC9
USB#9
USB9
USB9_FB#
USB9_FB
RN25 0X2 4P2R 5% NI
RV16 0402
RV15 EGA10402V05AH 0402
J71
C670 0.1U 0402 X7R 10V
C668 100U 7343 20% 10V
D59 PESD5V0U1BB 15A SOD523 5V
3VSB
R742 10K 0402 5%
USBVCC0 R740 280 1% 0402 USBOC#0
R741 332 0402 1%
R130 0 NI 5% 0402
C348 0.1U 0402 X7R 10V
R744 10K 0402 5%
USBVCC7 R745 280 1% 0402 USBOC#7
R743 332 0402 1%
R236 0 NI 5% 0402
C364 0.1U 0402 X7R 10V
R748 10K 0402 5%
USBVCC8 R749 280 1% 0402 USBOC#8
R746 332 0402 1%
R747 0 NI 5% 0402
C365 0.1U 0402 X7R 10V
R752 10K 0402 5%
USBVCC9 R753 280 1% 0402 USBOC#9
R750 332 0402 1%
R751 0 NI 5% 0402
C375 0.1U 0402 X7R 10V
R756 10K 0402 5%
USBVCC10 R757 280 1% 0402 USBOC#10
R754 332 0402 1%
R755 0 NI 5% 0402
C376 0.1U 0402 X7R 10V
R760 10K 0402 5%
USBVCC11 R761 280 1% 0402 USBOC#11
R758 332 0402 1%
R759 0 NI 5% 0402
C389 0.1U 0402 X7R 10V
R764 10K 0402 5%
USBVCC2 R765 280 1% 0402 USBOC#2
R762 332 0402 1%
R763 0 NI 5% 0402
C391 0.1U 0402 X7R 10V
5VSB
U53 TPS2062 SOIC8 Critical
USB_PWR_EN_1
R714 0 0402 5%
C752 0.1U 0402 X7R 10V
C767 10V X7R 0402 0.1U
C766 0.1U 0402 X7R 10V
USBOC#0 12
USBOC#7 12
U51 TPS2062 SOIC8 Critical
USB_PWR_EN_2
R713 0 0402 5%
C753 0.1U 0402 X7R 10V
C769 10V X7R 0402 0.1U
C768 0.1U 0402 X7R 10V
USBOC#8 12
USBOC#9 12
U52 TPS2062 SOIC8 Critical
USB_PWR_EN3
R708 0 0402 5%
C755 0.1U 0402 X7R 10V
C771 10V X7R 0402 0.1U
C770 0.1U 0402 X7R 10V
USBOC#10 12
USBOC#11 12
U50 TPS2061 MSOP8 Critical
USB_PWR_EN_4
R712 0 0402 5%
C754 0.1U 0402 X7R 10V
C772 0.1U 0402 X7R 10V
USBOC#2 12
L13 CL-2M2012-900JT 300mA 90 ohm 0805
USB11
USB#11
USB11_FB
USB11_FB#
RN15 0X2 4P2R 5% NI
RV4 EGA10402V05AH 0402
RV3 EGA10402V05AH 0402
J93 SIDE_USB
C265 0.1U 0402 X7R 10V
C613 100U 7343 20% 10V
D7 PESD5V0U1BB 15A SOD523 5V
L15 CL-2M2012-900JT 300mA 90 ohm 0805
USB10
USB#10
USB10_FB
USB10_FB#
RN16 0X2 4P2R NI 5%
RV6 EGA10402V05AH 0402
RV5 EGA10402V05AH 0402
J94 SIDE_USB
C292 0.1U 0402 X7R 10V
C641 100U 7343 20% 10V
D10 PESD5V0U1BB 15A SOD523 5V
BT_LED
R133 150 0402 5%
LED6 RED
L19 CL-2M2012-900JT 300mA 90 ohm 0805
USB2
USB#2
USB2_FB#
USB2_FB
RN17 0X2 4P2R 5% NI
RV7 EGA10402V05AH 0402
RV8 EGA10402V05AH 0402
J92
C314 100U 7343 20% 10V
C403 0.1U 0402 X7R 10V
2010/2/26 ADD
VCC
DATA-
DATA+
GND
Buletooth
BT USB P151
R738 1% 280 0402
R739 332 0402 1%
C347 0.1U 0402 X7R 10V
USBOC#6 12
F5 1206L150WR RC1206 0.11 ohm Critical 1206 1.5A 1.5A NI 6V RC1206 0.11 ohm 1206L150WR F6
C543 100U 7343 20% 10V
BT_LED
BT_ON
RV1 EGA10402V05AH 0402
RV2 EGA10402V05AH 0402
RN12 0X2 4P2R 5%
L7 CL-2M2012-900JT 300mA 90 ohm 0805
USB6
USB#6
R162 100K 5% 0402 NI
Quanta Computer Inc.
PROJECT : ZN5
Size
Document Number
USB Port X6
Rev X4
Date: Friday, March 05, 2010
Sheet 24 of 40

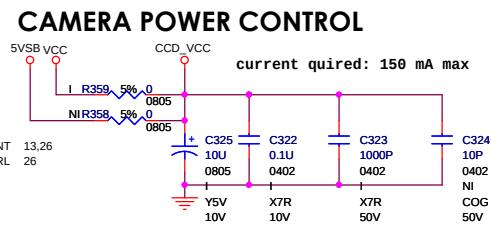
2nd FAN



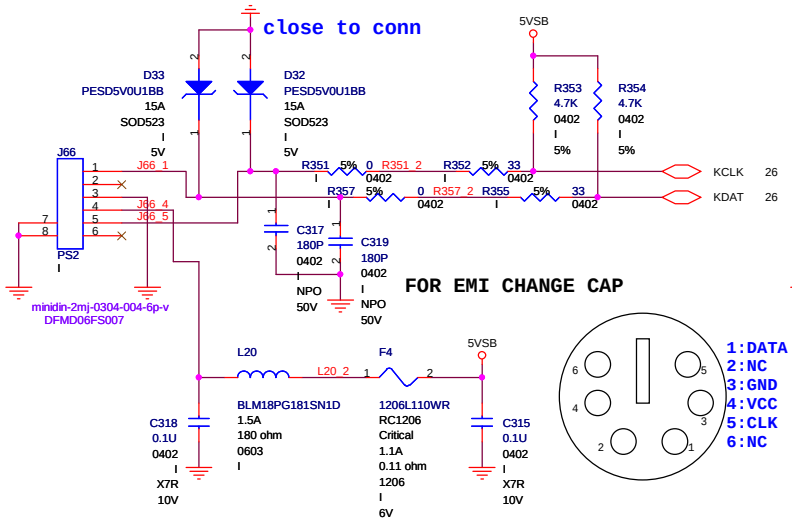
SYSTEM FAN CONN

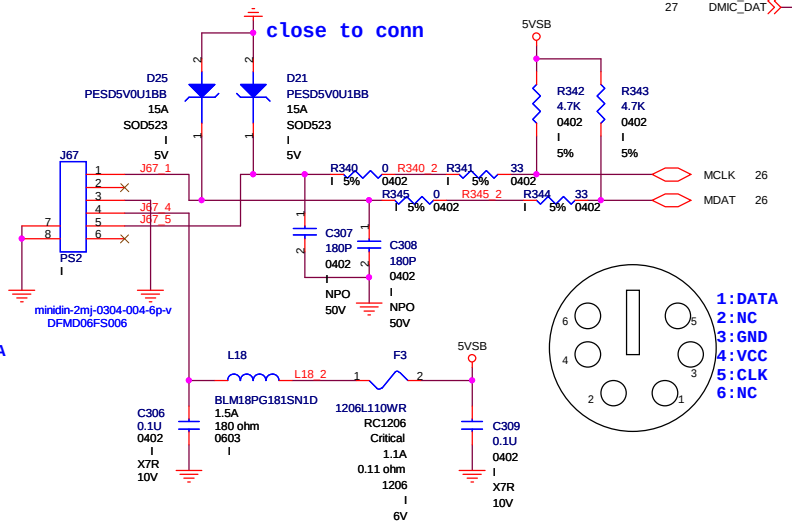


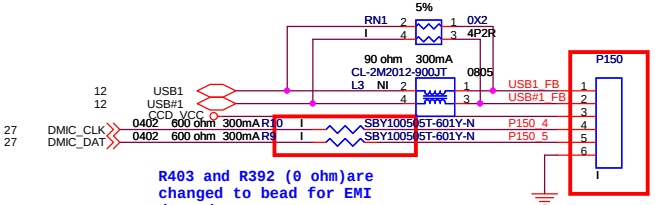
CAMERA POWER CONTROL



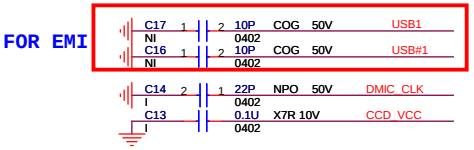
PS2 KEYBOARD& PS2 MOUSE







TO WEB CAM MODULE

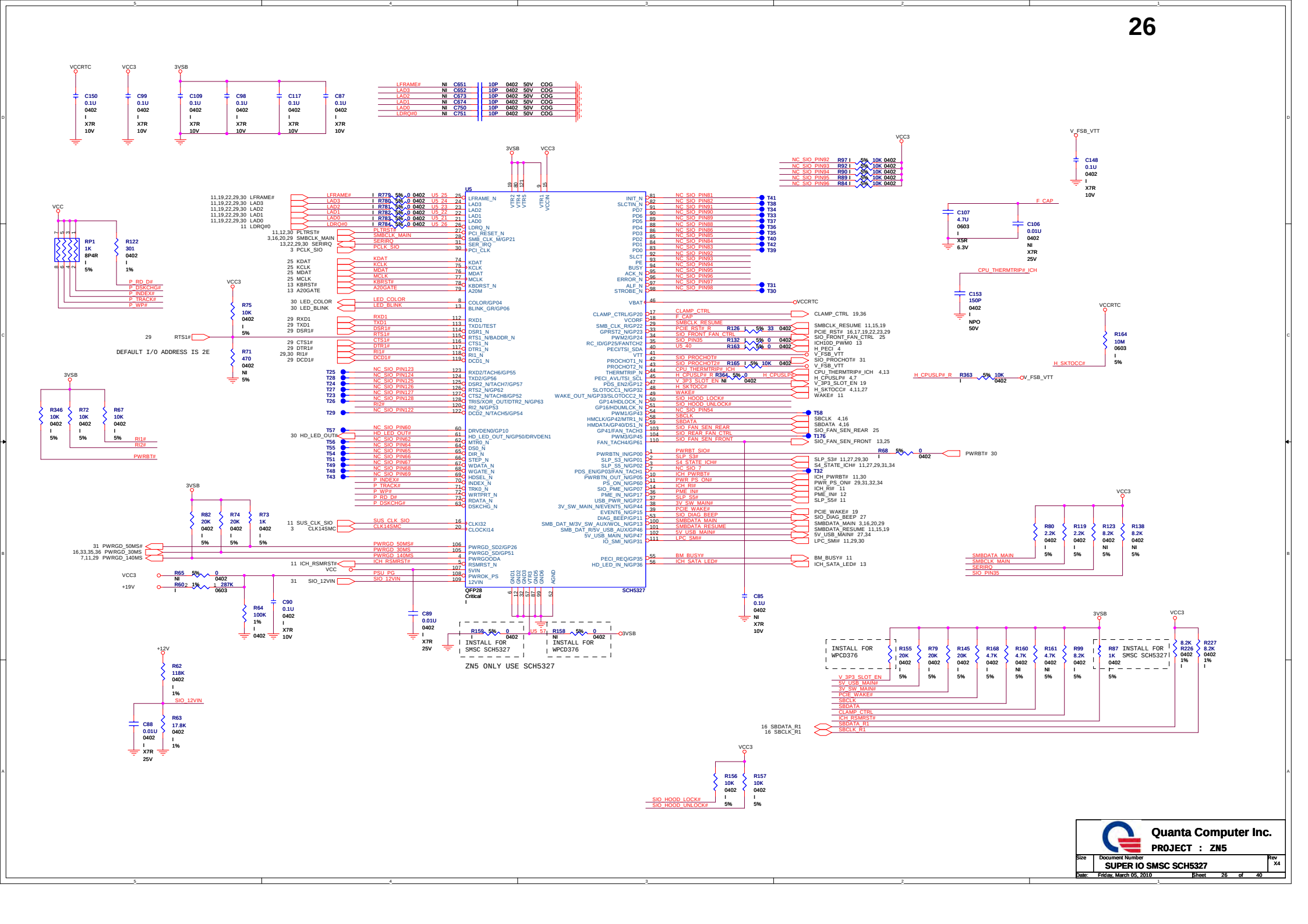


Quanta Computer Inc.

PROJECT : ZN5

Size	Document Number	Rev
	FAN/CAM/PS2	X4

Date: Friday, March 05, 2010 Sheet 25 of 40


U5
SCH5327
QFP28
Critical
DEFAULT I/O ADDRESS IS 2E
ZN5 ONLY USE SCH5327
INSTALL FOR SMSC SCH5327
INSTALL FOR WPCD376
Quanta Computer Inc.
PROJECT : ZN5
SUPER IO SMSC SCH5327
Rev X4
Friday, March 05, 2010
Sheet 26 of 40

1/20 Wei modify;
AR34 I change to NI

AR34 0R 0603 1%
AC18 NI
0.1U X5R 10V 0402

Please next to U14

AR15 0R 0603 1%
AC14 NI
0.1U 0402 X5R 10V

Analog_ground digital_ground

Please next to CODEC

2/12 Wei modify:
from Vendor suggesion reduce POP noise
AC25 from 0.1uF/10V X5R --> 0,1uF/ 16v X7R
AC27 from 10uF / 6.3v --> 2.2uF/ 6,3v

Spilt by DGND

ALC272AF-GR

ANALOG

DIGITAL

LQFP48 Critical

Place next to pin 25

Place next to pin 9

2/10 Wei modify:
from HP request import sonic focus in DVT 1.5

D28 D26 D19 D18
D29 D30 D24 D23
BAV99 SOT23-3 100V 200mA

ADOUTR ADOUTL HPOUT_R HPOUT_L
LINEOUT_R LINEOUT_L MICIN_R MICIN_L

1/20 Wei modify;
AGND --> DGND

2/10 Wei modify;
impot correct HF connector for ZN5

30mil

100 mil

PIN1:Internal SPK_L+
PIN2:Internal SPK_L-
PIN3:Internal SPK_R-
PIN4:Internal SPK_R+

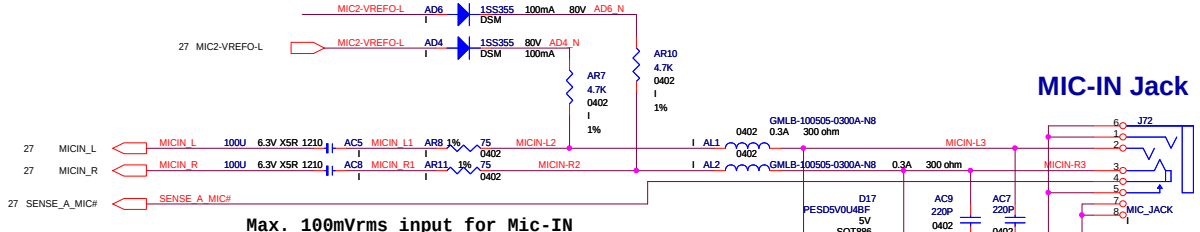
1/25 Wei modify;
AGND --> DGND

2/12 Wei modify:
from Vendor suggesion
LDO grounding from AGND to DGND

Vout = Vref(1+AR20/AR21)
1.24(1+309K/100K)=5.07

Quanta Computer Inc.
PROJECT : ZN5
Realtek ALC272AF-GR
Size: Document Number: Rev: X4
Date: Friday, March 05, 2010 Sheet 27 of 40

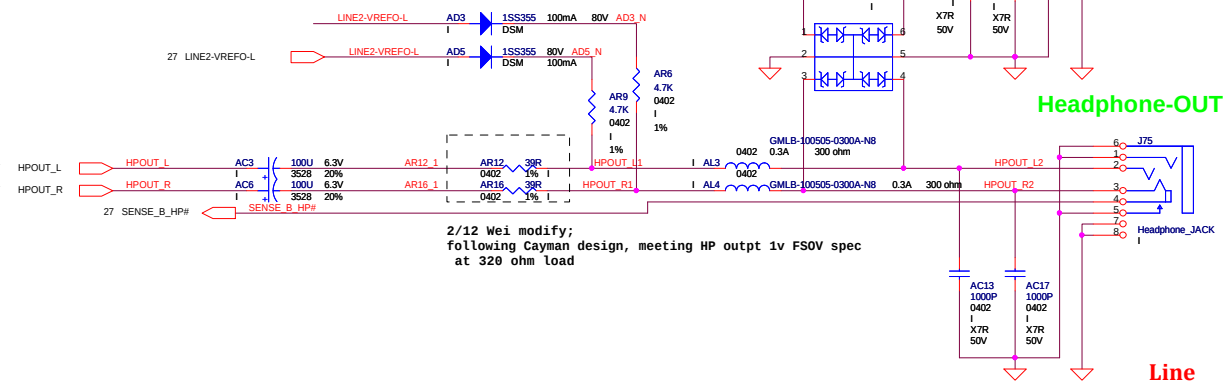
MIC-IN Jack



Max. 100mVrms input for Mic-IN

Please next to MIC IN Jack

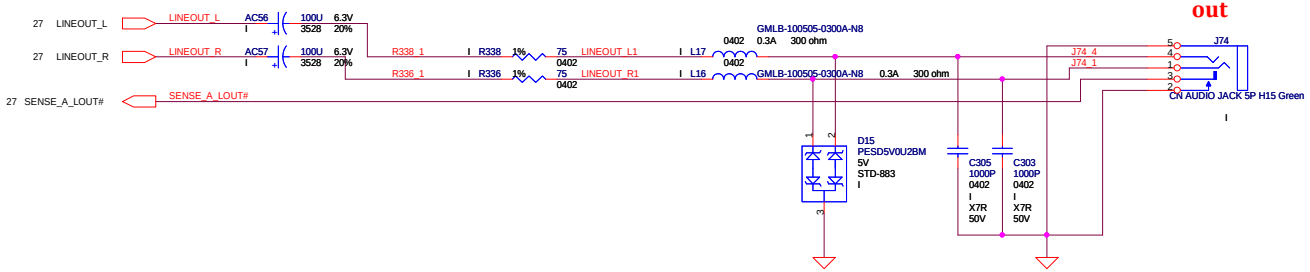
Headphone-OUT



2/12 Wei modify;
following Cayman design, meeting HP outpt 1v FSOV spec
at 320 ohm load

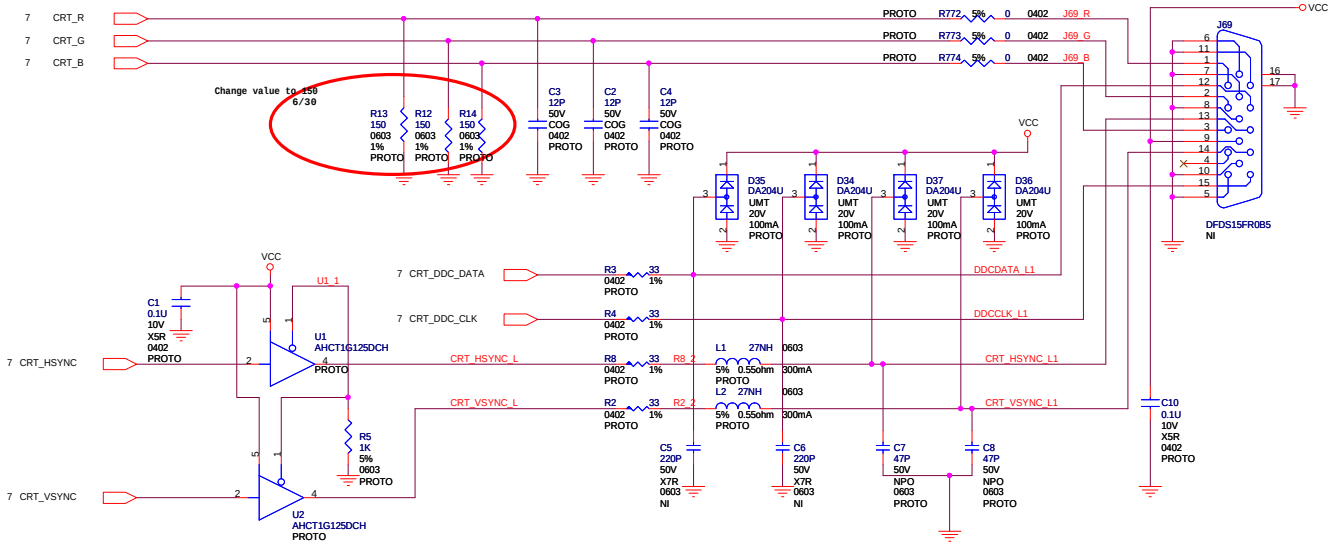
Please next to Headphone Out Jack

Line out



Please next to Line Out Jack

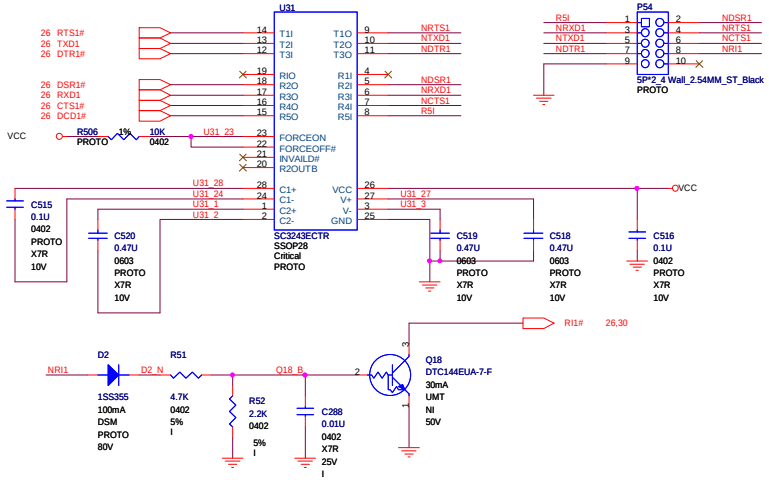
Reserve to CRT



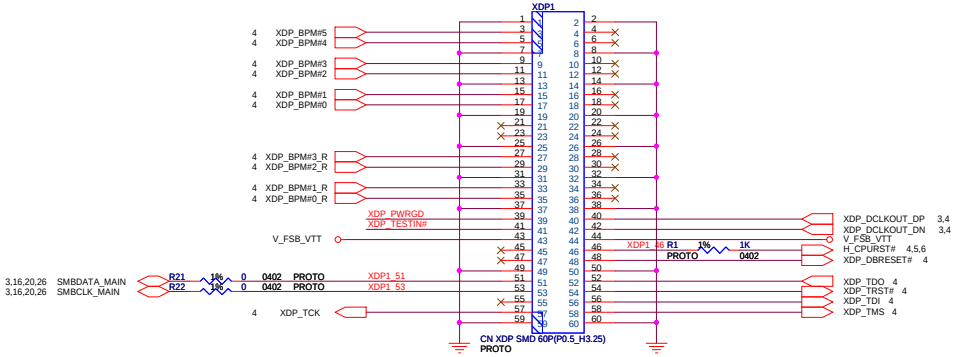
Quanta Computer Inc.
PROJECT : ZN5

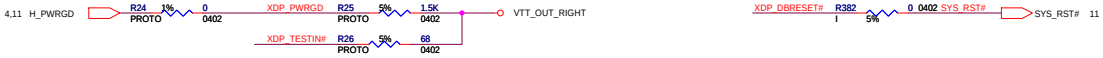
Size	Document Number	Rev
	AUDIO JACK/CRT	X4
Date: Friday, March 05, 2010	Sheet 28 of 40	

SERIAL PORT



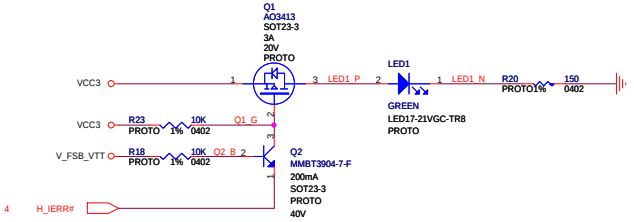
CPU XDP Debug Port

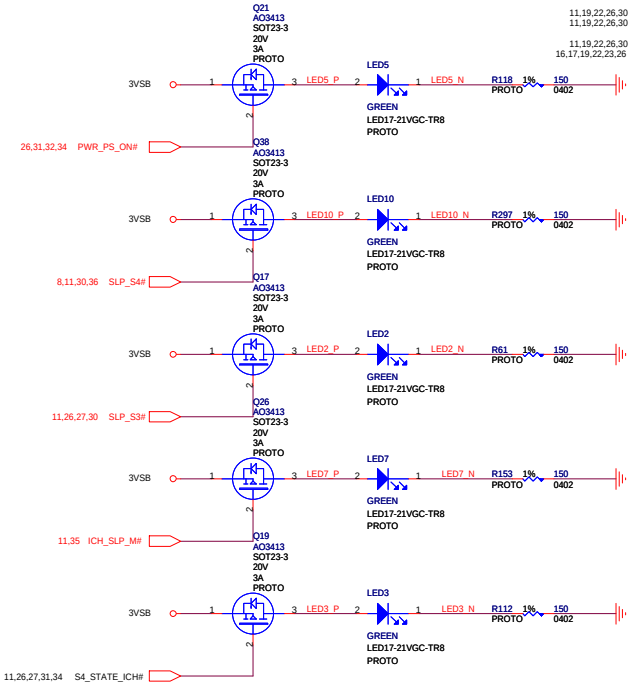


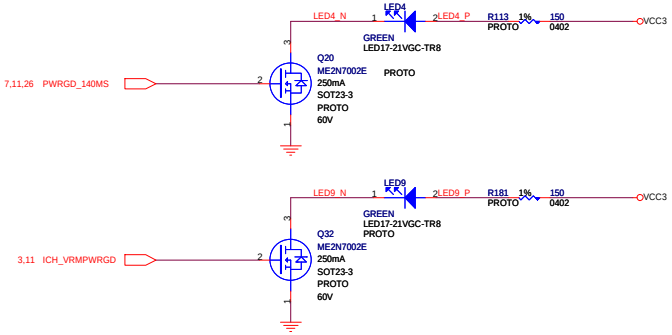


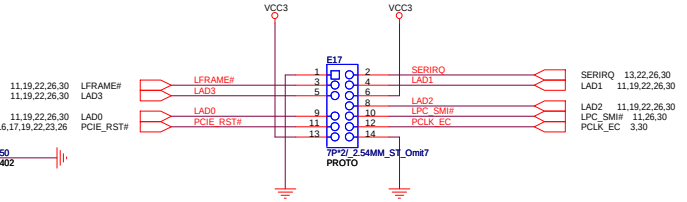
LPC HEADER

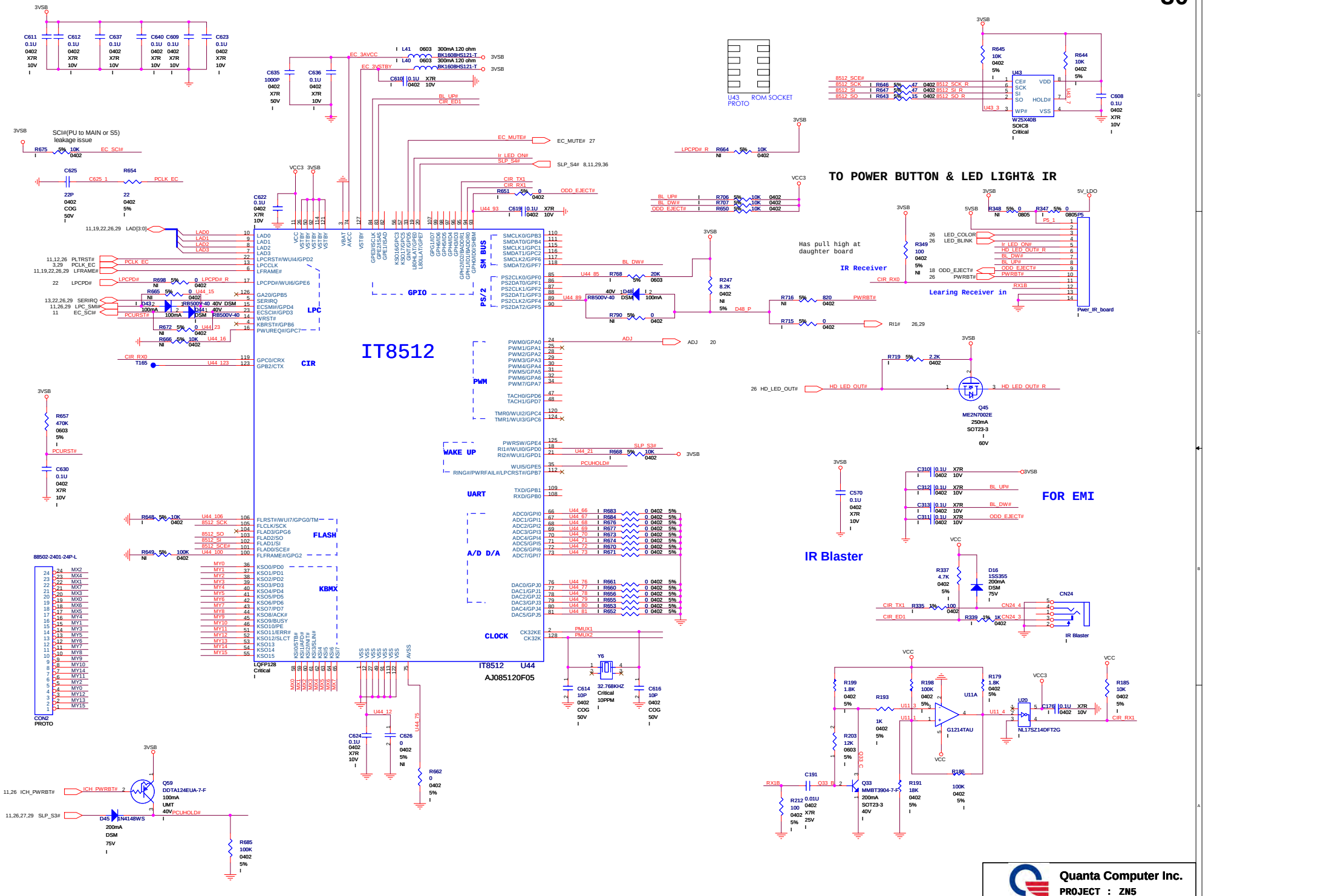
LED

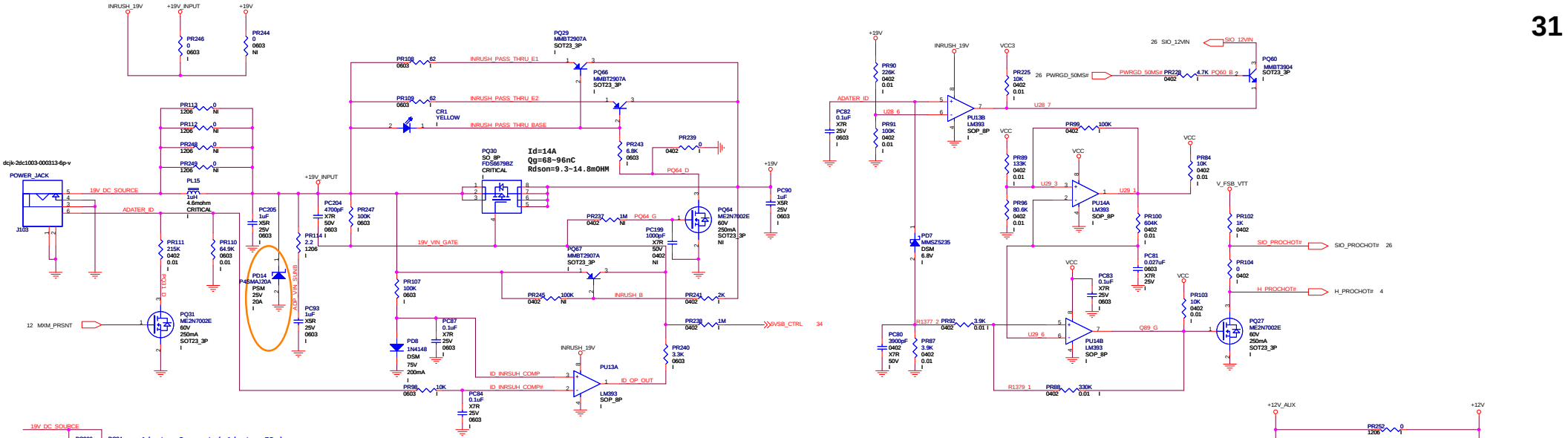


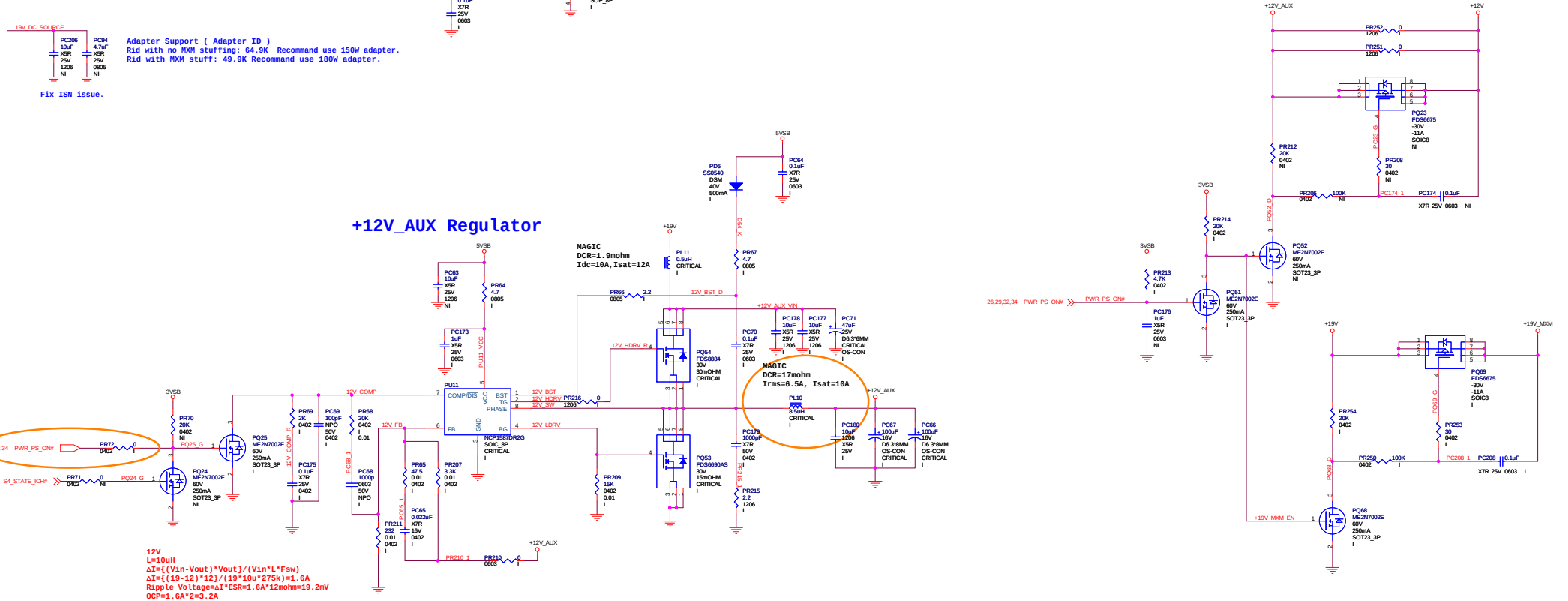




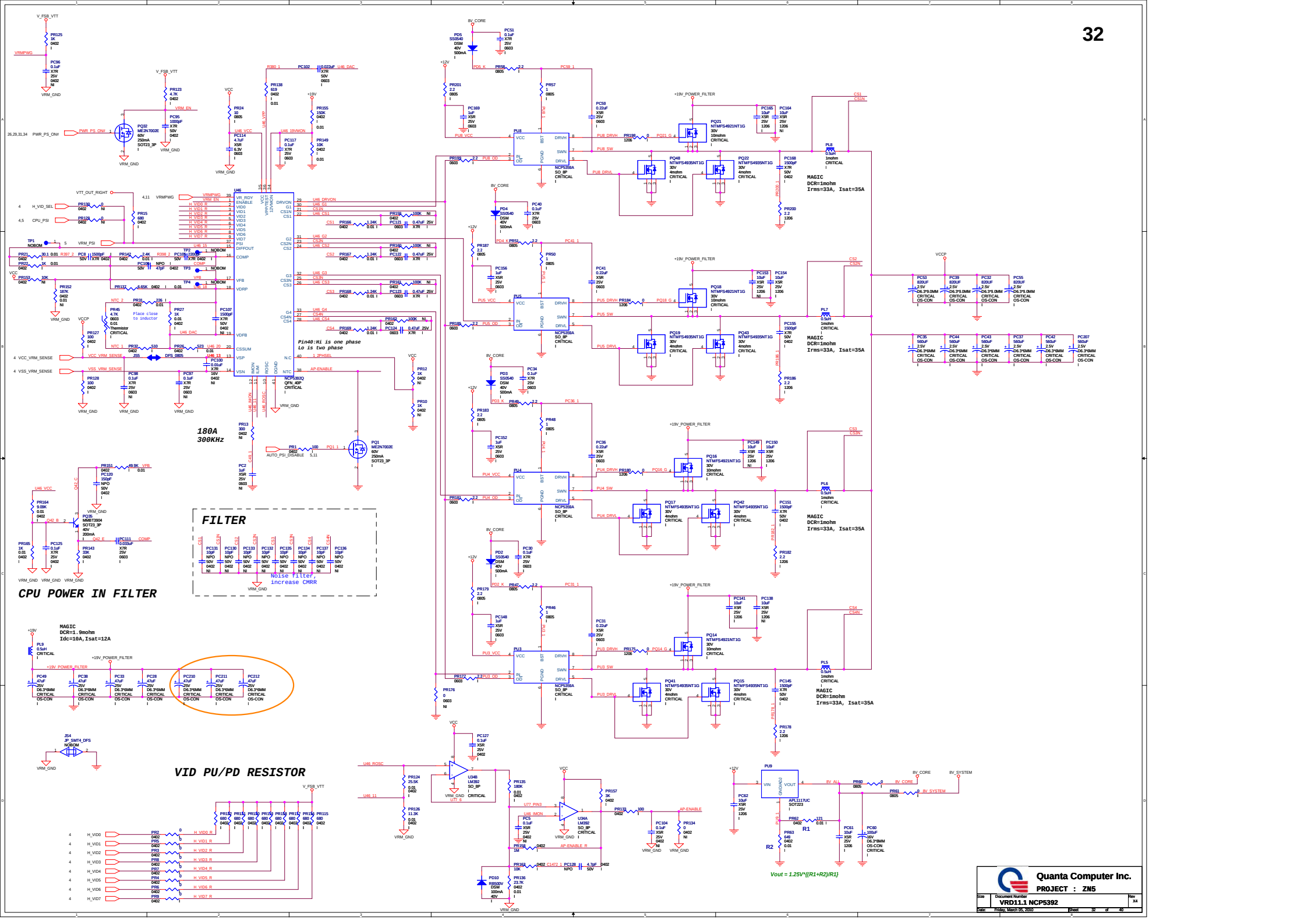



IT8512
AJ085120F05
IT8512 U44
LPC
CIR
GPIO
PS/2
SM BUS
PWM
WAKE UP
UART
A/D D/A
CLOCK
FLASH
KBMX
TO POWER BUTTON & LED LIGHT& IR
FOR EMI
IR Blaster
IR Receiver
Has pull high at daughter board
Learing Receiver in
Pwer_IR_board
W25X40B SOIC8 Critical
ROM SOCKET
U43 PROTO
CON2 PROTO
88502-2401-24P-L
LQFP128 Critical
32.768KHZ Critical 10PPM
G1214TAU
NL17SZ14DFT2G
SCI#(PU to MAIN or S5) leakage issue
Quanta Computer Inc.
PROJECT : ZN5
ITE8512
Rev X4
Size
Document Number
Date: Friday, March 05, 2010
Sheet 30 of 40

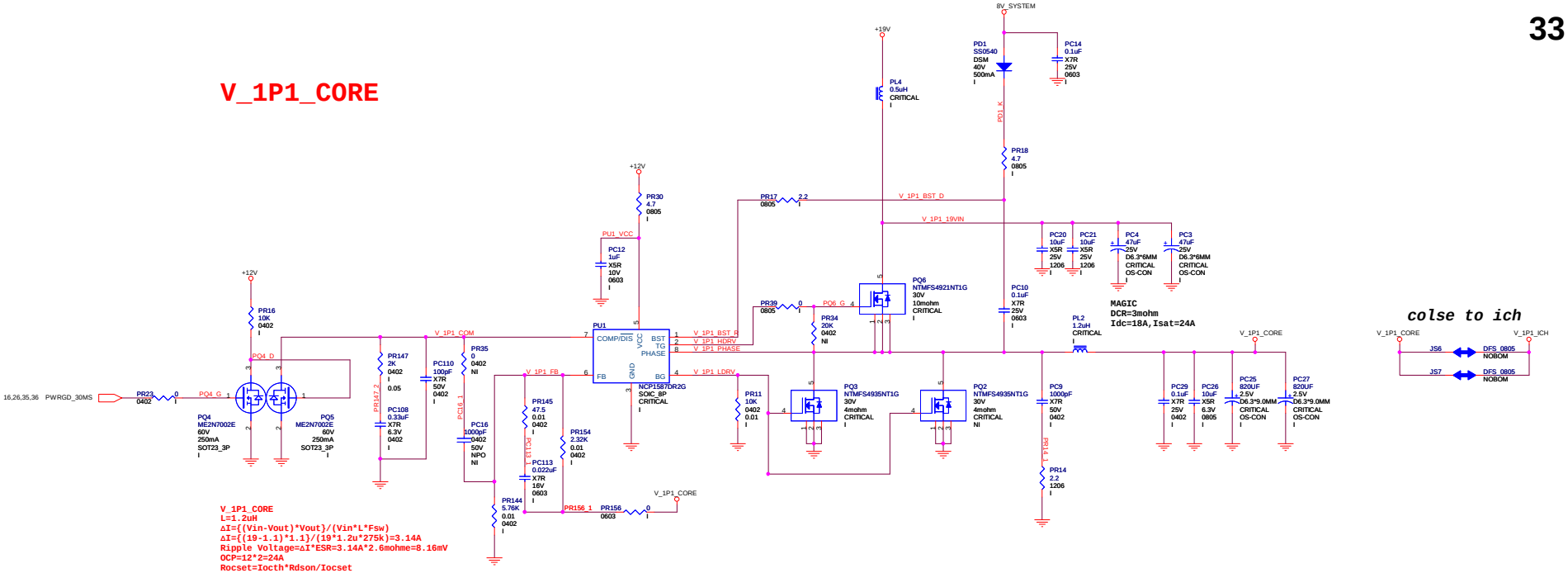




Quanta Computer Inc.			
PROJECT : ZN5			
Size	Document Number		Rev
	DC-IN,+12V		X4
Date: Friday, March 05, 2010		Sheet 31 of 40	

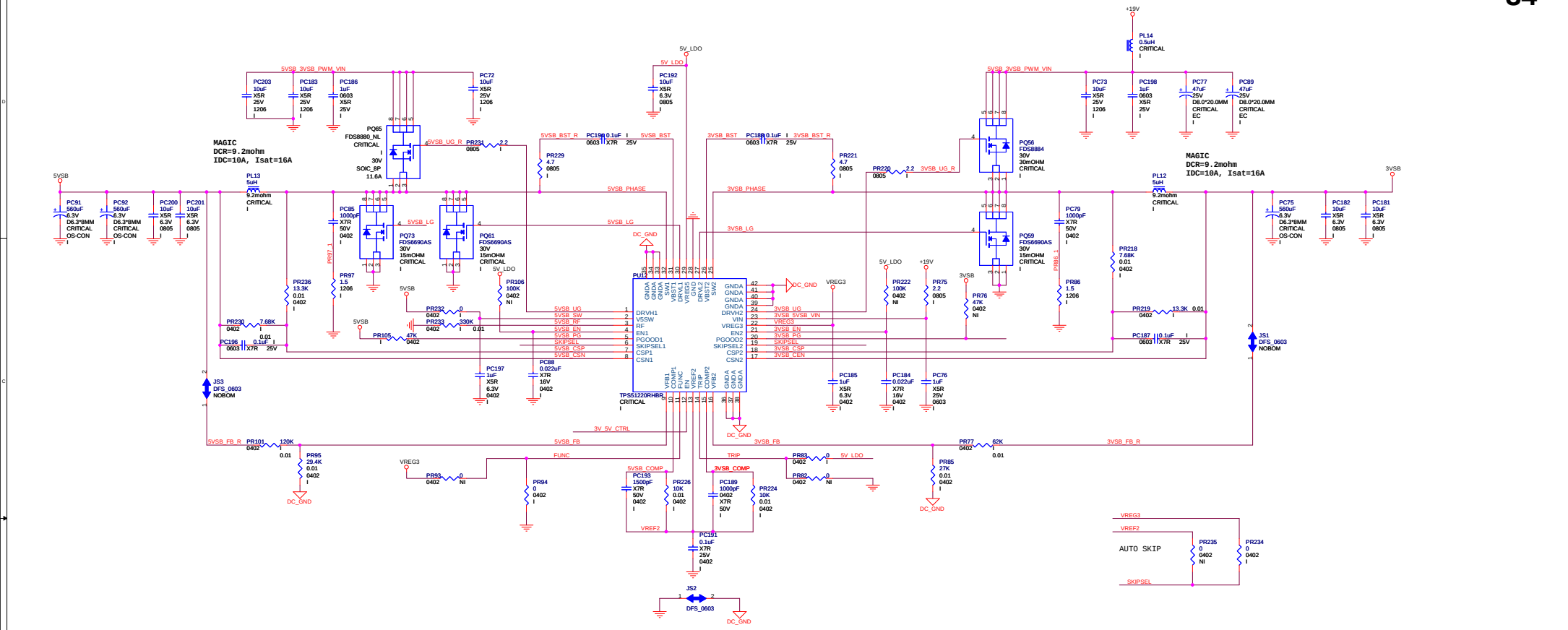

180A
300KHz
Pin40:Hi is one phase
Lo is two phase
CPU POWER IN FILTER
FILTER
Noise filter, increase CMRR
VID PU/PD RESISTOR
MAGIC
DCR=1mohm
Irms=33A, Isat=35A
MAGIC
DCR=1.9mohm
Idc=10A,Isat=12A
Vout = 1.25V*(R1+R2)/R1
Quanta Computer Inc.
PROJECT : ZN5
VRD11.1 NCP5392
Friday, March 05, 2010

V_1P1_CORE

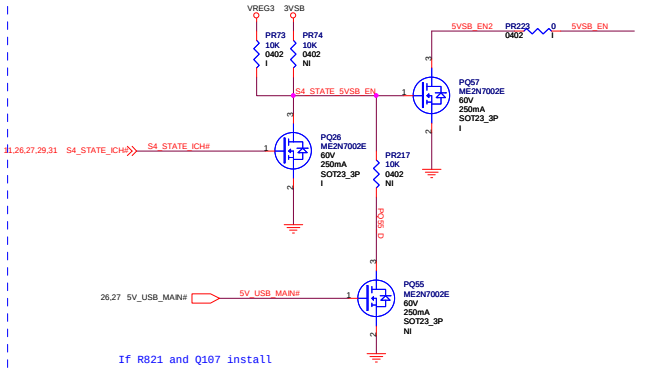


V_1P1_CORE
L=1.2uH
ΔI={(Vin-Vout)*Vout}/(Vin*L*Fsw)
ΔI={(19-1.1)*1.1}/(19*1.2u*275k)=3.14A
Ripple Voltage=ΔI*ESR=3.14A*2.6mohme=8.16mV
OCP=12*2=24A
Rocset=Iocth*Rdson/Iocset
Rocset=24A*4mohm/10uA=10Kohm

Quanta Computer Inc.			
PROJECT : ZN5			
Size	Document Number		Rev
	V_1P1_CORE		X4
Date: Friday, March 05, 2010	Sheet 33 of 40		

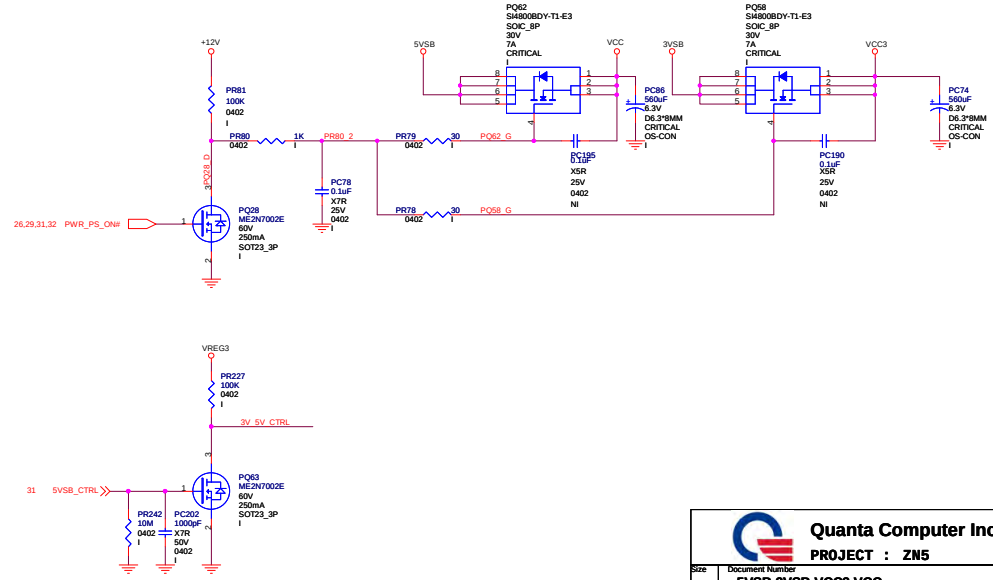


5VSB_EN control



If R821 and Q107 install

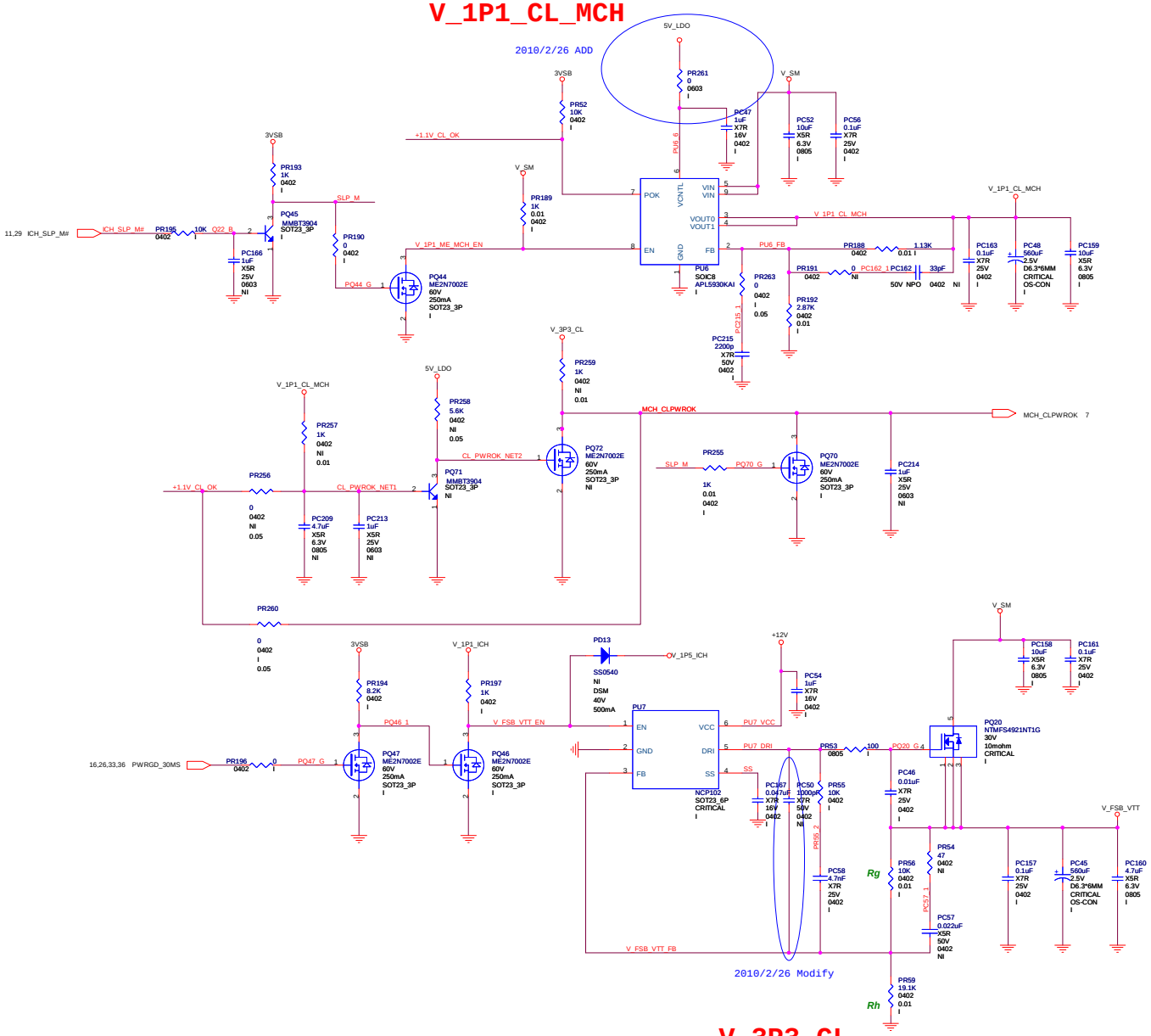
S4_STATE_ICH-	5V_USB_MAIN-	VR_5VSB_EN
0	1	1
0	0	0
1	X	1
1	X	1



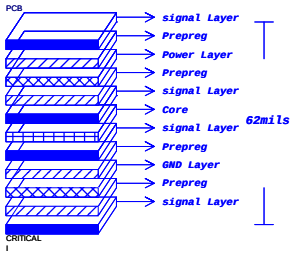
Quanta Computer Inc.	
PROJECT : ZN5	
Size	Document Number: 5VSB,3VSB,VCC3,VCC — Rev: X4
Date: Friday, March 05, 2010	Sheet 34 of 40

V_1P1_CL_MCH

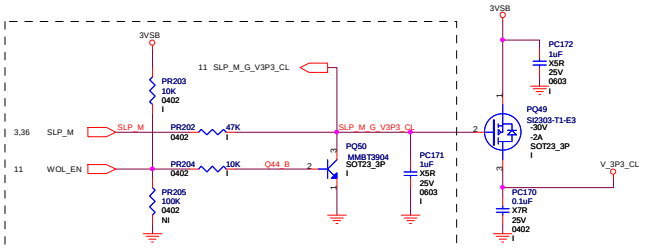
2010/2/26 ADD



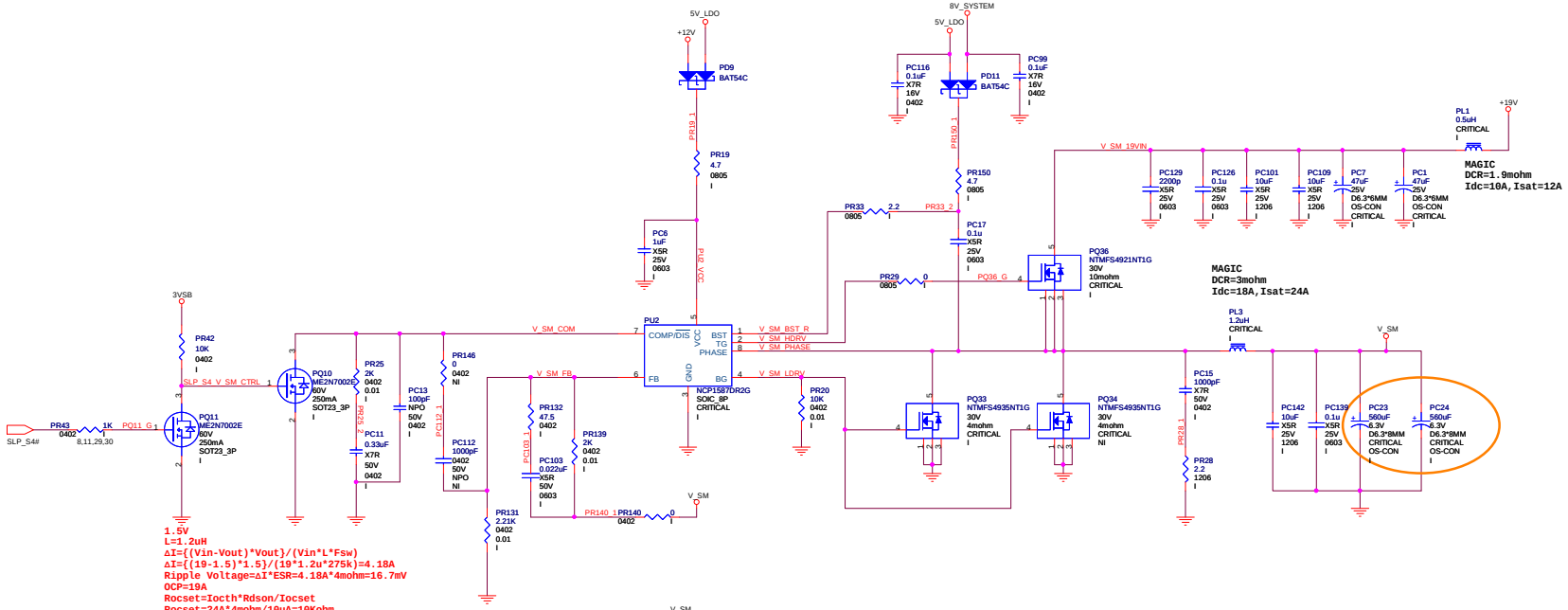
2010/2/26 Modify

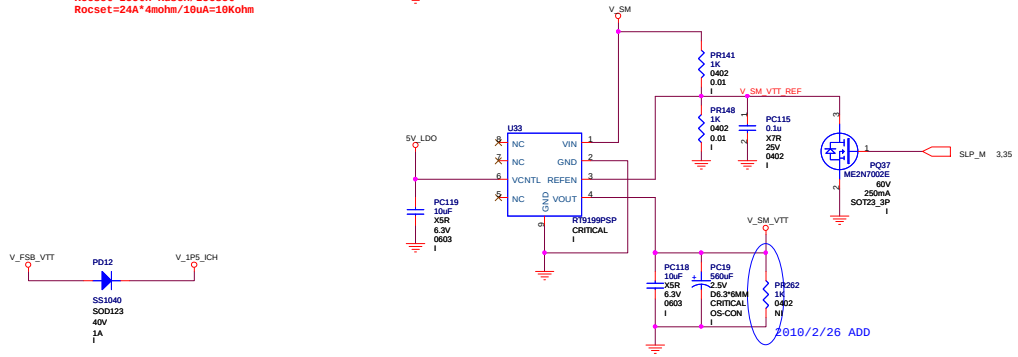


V_3P3_CL

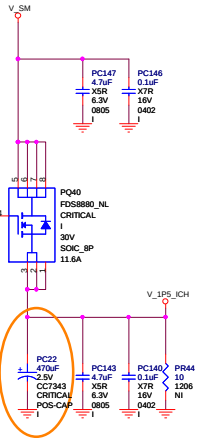


Quanta Computer Inc.		
PROJECT : ZN5		
Size	Document Number	Rev
	V_3P3_CL/V_1V_1P1_ME+T/U PAR	X4
Date: Friday, March 05, 2010	Sheet 35 of 40	

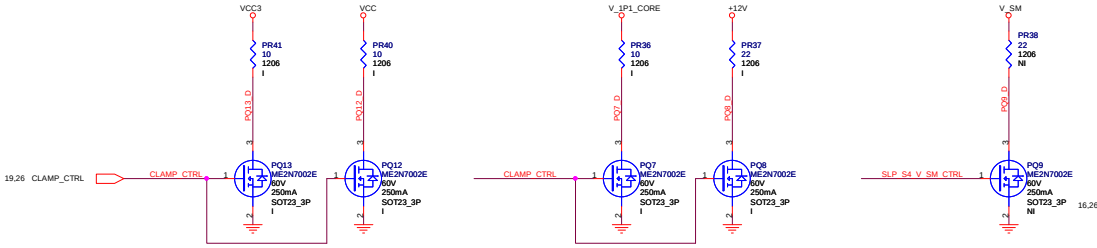


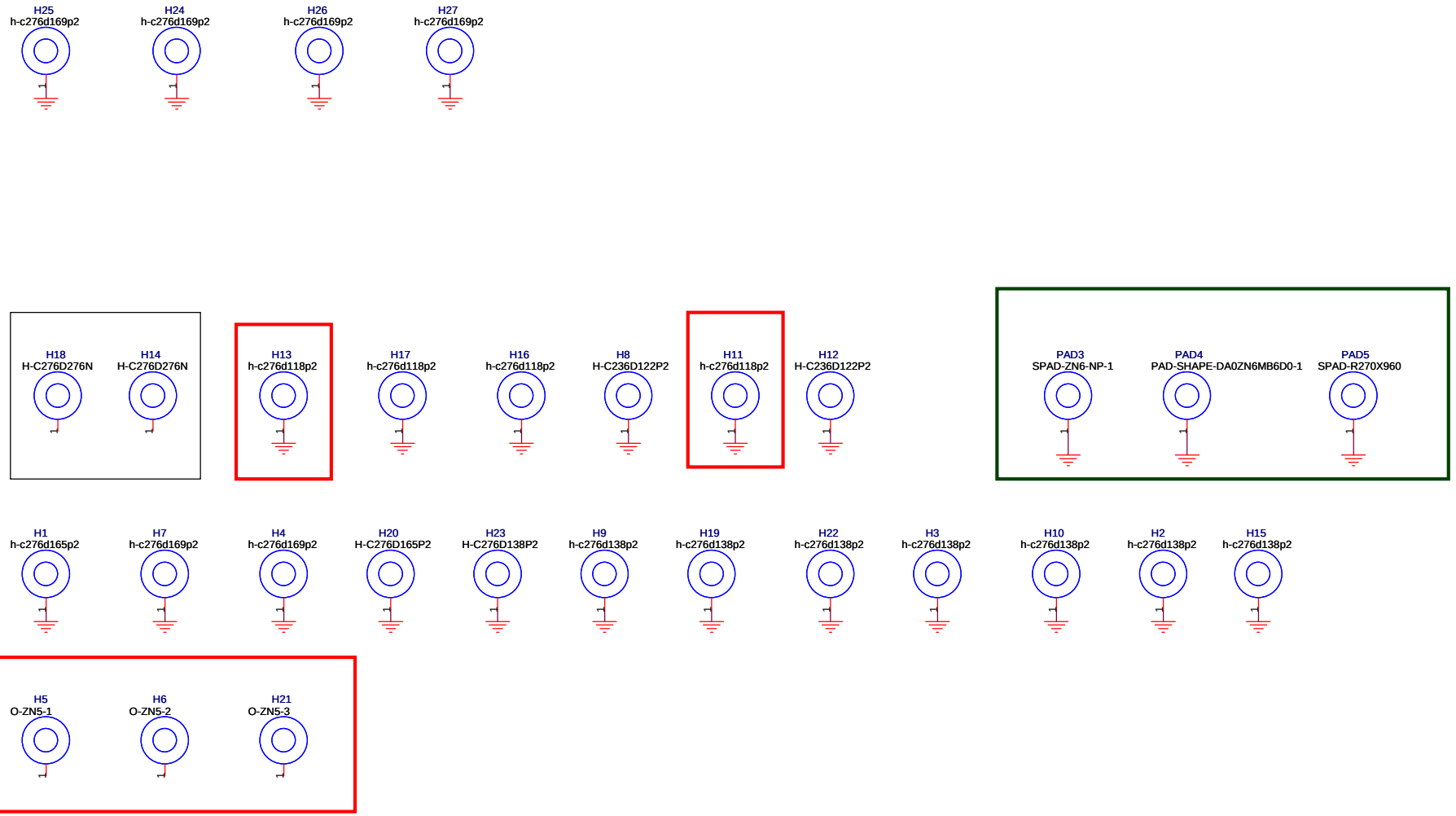


V_1P5_ICH



CLAMP_CTRL





Quanta Computer Inc.

PROJECT : ZN5

Size	Document Number	Rev
	SCREW HOLE & EMI	X4

Date: Friday, March 05, 2010 Sheet 37 of 40

DATE	ZN5 Schematic file for EVT2	Revision
18th Dec. 2009	ZN5-1218-1.DSN	X2
PS	ZN5 Schematic Change from EVT1 to EVT2	

Schematic Change Description
1. Change AVDD/DVDD name to AVDD_7308/DVDD_7308 on CH7308 chip side
2. Add R81(I),R83(I),R715(I), R716(NI), R717(NI), change 3VSB name to 3VSB_USBOC of RP14 and RP18
3. Add 32 pcs 0.1uF capacitor C718-C749 (NI), change SATA HDD connector footprint and reverse pin define
4. Change dedicated component location to follow HP PCA specification
ACN1 to J74, ACN2 to J72, ACN3 to J75, ACN4 to P6, AU2 to U13, AU3 to U14, BT1 to XBT1, CN1 to J69, CN11 to P60, CN12 to P151
CN13 to P9, CN14 to J41, CN16 to J106, CN19 to J105, CN2 to P11, CN20 to J93, CN22 to J94, CN21 to P160, CN23 to J64, CN25 to J67
CN33 to J66, CN26 to J9, CN27 to J70, CN28 to J60, CN29 to P5, CN3 to P150, CN30 to J92, CN31 to J71, CN32 to J91, CN4 to XDP1
CN5 to XMM2, CN6 to XMM1, CN8 to P125, P1 to P54, P2 to P153, SW1 to SW50, U10 to U29, U11 to U5, U29 to U53, U19 to U11
U13 to U51, U14 to U52, U23 to U19, U25 to U40, U48 to U55, U3 to U50, U37 to U31, U31 to U54, U39 to U6, U6 to U10, PJ1 to J103
U5 to U3, U42 to U4, U4 to XU1, Y1 to Y2, Y2 to Y1, Y3 to Y6, Y6 to Y3
5. Change Audio Amplifier from TPA6020A2 to SSM2306CP2, Del de-pop circuit
Del AC1(NI), AC2(NI), AC20(NI), AC21(NI) AC38(I), AC40-AC44(I) AD1(NI), AD2(NI), AQ1(NI), AQ2(NI), AR1-AR3(NI)
Change AC10 and AC19 from 1000pF(NI) to 0.1uF(NI), change footprint
Change AC45 from 1uF(I) to 0.047uF(I), change footprint Del D57, BAT54A(I)
Add AC56 and AC57, 22uF(I) Add AC58, 1000pF(I) Add AC60,AC77, 0.047uF(I) Add AC71,AC72,AC73,AC65, 470pF(I)
Add AC74, 10uF(I) Add AC75, 0.1uF(I) Add AC66, AC76,AC78,AC79, 10pF(I) Add AC64, 10uF(I)
Add AD43, AD8, SS1040(I) Add AD44,AD7, SSM24PT(I) Add AD46, BAT54A(I) Add AL15-19, MPZ1608S221AT(I)
Change AR17 POP from I to NI
Change AR33, AR41 value from 14K ohm to 76.8K ohm (I)
Change AR34, AR38 value from 14K ohm to 0 ohm(NI)
Add AR72 and AR74 76.8K ohm(I) Add AR76 and AR80 0 ohm (I)
6. Change Speaker connector tyrpe from vertical to right angle
7. Del DP AUX SW unnecessary circuit Del C181, 0.1uF (I) Del C276, 0.22uF (I), Del Q22 and Q23, ME2N7002E(I)
8. Change 2nd FAN connector from 4 pin to 3pin Del C11, 0.01uF (I) C12, 100pF (I) C15, 10uF (I), C9, 47pF(I), Del D1, BAT54A(I)
9. Change C122 voltage rating from 10V to 6.3V
10. Change C175 POP from I to NI
11. Change C236(I), C260(NI),C288(NI),C314(I),C543(I),C668(I)C289(I) footprint and QPN
12. Change C256(NI),C613(I),C641(I), C302(NI), C304(NI) footprint and QPN
13. Change C356(I) and C367(I), C440(I) footprint and QPN to follow Intel Spec
14. Del C651(I), C652(I), C673(I), C674(NI)
15. Add C675-C715, 0.1uF(I), Add C716, 2.2uF(I), Add C717, 1uF(I), Add C718-C749, 0.1uF(NI)
16. Change CCD connector type from right angle to vertical
17. Change CN9 EDID connector POP from NI to I
18. Del CT1, CT label(I)
19. Change D11 and D14 value(I)
20. Change D4 from BAT54A to BAT54C(I)
21. Change L34 and L35 footprint and QPN(I), Add L46(I) and L47(I)to follow Intel Spec
22. Del Q24, DDTC144EUA(I). Del Q31(I), Q34(I), Q40(I), Q45(I), Q46(I), Q50(I), Q51(I), ME2N7002E
23. Change Q52(I) footprint and QPN, Chnage L23(I) and L22(I) QPN
24. Add Q61(I), BA0B1440013 Del Q62(NI), Q63(NI), Q64(NI)
25. Del R188(I), R110(I), R11(I), R15(I), R16(I), R17(NI), R236(I), R283(I), R312(I), R316(I), R6(I), R7(I),RN18-21(I)
26. Change R117(I) value from 0 ohm to 1K ohm
27. Change R123,R172,R196,R226,R227,R282,R347,R348, R564 POP friom I to NI
28. Change R282, R347, R565, R650, R693 POP from NI to I
29. Change R308(I) value from 100 ohm to 20K ohm
30. Change R313(NI) value from 0 ohm to 4.7K ohm
31. Change R464(I) value from 0 ohm to 1 ohm
32. Change R495(I) value from 1M ohm to 1 ohm
33. Change R505(I) value from 1M ohm to 40.2 ohm
34. Change R510(NI) value 0 ohm to 4.7K ohm
35. Change R514(I). R516(I) value from 2K ohm to 4.7K ohm
36. Change R515(I) value from 169 ohm to 220 ohm
37. Change R62(I) value from 11.8K ohm to 118K ohm, Change R63(I) value from 1.78K ohm to 17.8K ohm
38. Change R630(I) value from 10K ohm to 8.2K ohm
39. Change R689(I), R698(I) value from 1K to 4.7K ohm
40. Change R691(NI) and R692(NI) value from 30K ohm to 4.7K ohm
41.Change R694(NI) value from 1K ohm to 4.7K ohm
42.Change R695(I) value from 1K ohm to 4.99K ohm
43.Change R697(I) value from 30K ohm to 39.2K ohm
44. Change R698(NI) value from 30K ohm to 0 ohm
45. Add R710-714(I) and R716(I), R715(NI), R717(NI)
46. Change R81(I)value from 100K ohm to 1K ohm
47. Change R83(I)value from 100K ohm to 1K ohm
48. Del RN18-21(I)
49. Change RP1(I) QPN
50. Change U26 value from SN74CBT3257GPWR to 74AHC1G125
51. Add PS8325 DisplayPort Dual Mode 2x2 Crosspoint Switch
52. Change C646(I) and C645(I) value from 180pF to 18pF
53. Change PC102(I), PC113(I), PC115(I), PC175(I), PC186(I), PC198(I), PC47(I), PR100(I), PR102(I), PR103(I) QPN
54. Change PC18(I), PC19(I), PC22(I), PC23(I), PC24(I). PC25(I), PC27(I), PC45(I), PC48(I), PC60(I) footprint and QPN
55. Add PC207(I), PC208(NI). PC209(NI), PC210(I), PC211(I), PC212(I), PQ68(NI), PQ69(NI), PQ70(NI), PR250-PR254(NI)
56. Change PC35(I) and PC37(I), PC42(I), PC43(I), PC44(I) value, footprint and QPN
57. Change PC66(I), PC67(I), PR99(I) footprint and QPN
58. Change PD1-PD7(I), PR111(I), PR241(I), PR62(I), PR63(I)footprint
59. Change PC11(I), PC1107(I) , PR125(I), PR132(I), PR141(I), PR148(I), PR149(I), PR156(I). PR16(I), PR163 QPN
60. Change PC137(I), PR142(I), PR166-PR169(I) value and QPN
61. Change PR170(I), PR171(I), PR193(I), PR195(I), PR197(I), PR203(I), PR204(I). PR213(I), PR221(I) QPN
62. Change PR224-PR229(I), PR23(I), PR232(I), PR234(I), PR42(I), PR43(I), PR52(I), PR55(I), PR56(I), PR73(I) QPN
63. Change PR45 POP from NI to I
64. Change PR80(I), PR81(I), PR83-84(I), PR87-89(I), PR91-92(I), PR94(I), PR96(I) QPN
65. Change Thermal sensor from EMC1412-2 to EMC1402-2
66. Change R127 POP from NI to I, R131, R389 POP from I to NI
67. Del 20 pcs 10uF 0805 package capacitor in page 5
68. Add R718(NI). R312(NI), R316(NI), Q40(NI). Q45(I), R719(I)
69. Change EMI Cap POP from NI to I in page 18, Change USB/1394 Resistor array to common choke in page 23 and page 24
70. Change P5 pin2 power source from VCC3 to 5VSB
71. RP14 pin 10 change to 3VSB_USBOC, PCLK_ICH change to U39 pin 7
72. Change J41, CON1, P11, P125. CN7 footprint
73. DEL D48(NI),D47(NI),D54(NI),D53(NI),D50(NI),D49(NI),D56(NI),D55(NI),D9(NI),D8(NI),D14(NI),D11(NI)
74. Change AC14 and AC18 POP from I to NI
75. Change AR34/AR15 POP from NI to I, footprint and QPN
76. Change AC37/AC77/AC60/AC45/AR31/AR32/AR42/AR43 QPN
77. Change AC47/AC46/AC36/AC35 footprint and QPN
78. Change L8, L9 and L11 POP form NI to I, Change L37, L38 and L39 from I to NI.
79. Move R226 and R227 tp page 26 and change them POP from NI to I, Change R160 and R161 and C85 from I to NI
80. Add over current design for each USB port, BT power add over current design and reverse power connect to 3VSB
81. Del R130(1) in page 20, change CS5 POP form I to NI
82. Del RP15-RP17(I) footprint, and Add R720-737(I) footprint
83. Move 1394 ESD protect device to near connector side
84. Change PQ40 value from FDC653N to SI4800BDY and footprint change
85. Change P5 pin 1 power source from 5VSB to 5V_LDO
86. Change R249 value from 10K ohm to 20K ohm, Add R766(I), R767(I), Q46(I)
87. Add R768(I) for EC code ID selection
88. Change All component that use BS870-7-F originally to ME2N7002E
89. Connecto PQS2 pin 1 to PQ68 pin1, Change PR254, PR250, PR253, PC208, PQ69 from NI to I
90. Add R769-R776(I)
91. Change PL2(I). PL3(I), PL5(I), PL6(I), PL7(I), PL8(I) QPN
92. Change PC210, PC211, PC212 from NI to I
93. Change PQ40(1), PR209(I), PR20(I), PC58(I) value to QPN
94. Change PQ2, PC164, PC149. PC153, PC138 from I to NI
95. Change CRT connector from I to NI
96. Change R241 POP from I to NI, R223 POP form NI to I
97. Add E16(I) and R777(NI), E16(1-2)Jumper(I)
98. Change R296(I) value and QPN
99. Change AC3(I) and AC6(I) value, description and QPN
100. Add R243(I), R778-R784(I), C651(NI), C652(NI), C673(NI), C674(NI), C750(NI), C751(NI)
101. Change CN15, CN17, J66, J67, J105, J106, J74, CN24, J72, J75 QPN
102. Change Location: JP1 to JP49, JP2 to E1, JP3 to E15, JP4 to E14
103. Change schematic reversion from 1B to X2
104. Change R81, R83, RP14 from I to NI
105. Add R110(I), R108(I), C752-C755(I)

DATE	ZN5 Schematic file for EVT2	Revision
6th Feb. 2010	ZN5-0206.DSN	X3
PS	ZN5 Schematic Change from EVT2 to DVT1.0	

Schematic Change Description
1. Update schematic reversion and sheet number
2. Change C43 POP from NI to I, F6 POP from I to NI
3. Change U7, U10 value, footprint and QPN
4. Add CN25(I),R785(I),C756(I),C757(I) for B-CAS feature
5. Change dedicated location: XMM1 to XMM3, XMM3 to XMM1
6. Change R59 to 301 ohm, R572 to 8.2K ohm, Change JP49 dedicated location to E49.
7. Add PAD3, PAD4 and PAD5 for gasket mount.
8. Del PC18(I), Change value, footprint and QPN for PC22,PC25,PC27, Change PC23 and PC24 footprint and QPN
9. Change R704 from 0 ohm to 22 ohm, Del R705(I) in page 27
10. Chnage R693 ,R696, R336 and R338 footprint, QPN
11. Del D20(I), D22(I), D27(I), D31(I), C302(NI), C304(NI)
12. Change D15 ,D17 value, footprint and QPN, Change AR18 and AC15 vlue and QPN
13. Change C303 and C305 footprint and QPN, Change AL1, AL2, AL3, AL4, L16, L17, AR17, AC16, AC56,,AC57 value, footprint and QPN
14. Change Speaker conn to DFHD04MR103 for halogen free request
15. Add AQ8(I), AQ9(I), AR44(I), AR45(I), AC20(I), AD45(I), AR46(I), AR47(I)
16. Add R786(NI), R787(I), D47(NI), R705(I),C260(I),D8(I) for 2nd FAN
17. Change SATA HDD CONN footprint and QPN
18. Change dedicated location: U50 to U56, U51 to U57, U52 to U58, U53 to U59, U54 to U53, U48 to U50, U47 to U51, U45 to U52
19. Change dedicated location: U10 to U47, U46 to U10, PU10 to U46, U24 to U54
20. Change E16 vaule, footprint and QPN, B-CAS connector footprint and QPN
21. Change R9 and R10 value and QPN
22. Change PL10 value, footprint and QPN
23. Change R127 POP from I to NI, R131 POP from NI to I, AR46 POP from I to NI, R468 and R469 POP from I to NI
24. Change AQ9 value to QPN, Change PR132 value
25. modify netname MICIN-L1 error
26. Change AR12 and AR16 value and QPN
27. Change SW50 material to Halogen free
28. Add PR251(NI), PR252(NI)
29. SWAP Memory CHA CK0/CK0# and CK2/CK2#
30. Connect RJ45 CONN Pin 5 to power plane VCC1.8M_LAN
31. Change LED1 vaule and QPN
32. Change AR45 from 49.9K to 100K, AR44 from 100K to 49.9K
33. Change AC3, AC6, H14, H18, H20, H23 footprint
33. Change C163, C540, R654, C625, C103 POP from NI to I
34. Change C119, C124, C656, C646, C582 and C588 value and QPN
35. Change R769, R770, R771, R775 and R776 POP from I to NI
36. Change AR34 POP from I to NI
37. Change AQ7 pin 1, U14 Pin.16 and Pin.17 connect from AGND to DGND
38. Change AC58, AC64, AC65, AC66, AC71, AC72, AC73, AC76, AC78, AC79, AQ3.1, AQ6.1 connect from AGND to DGND
39. Add VCC1.8M_LAN power source node
40. Add U19 and U43 ROM SOCKET
41. Change U16 to NIS5135, Add R788(I), C758(NI), PD14(I)
42. Change AR34 and AR15 change footprint to 0603
43. Don't connect RJ-45 pin15 & pin16 to GND, and connect H18 and H14 to GND
44. Change PR71,PR70,PR212,PR206,PR208,PC174,PQ24,PQ52,PQ23 POP from I to NI. Change PR72,PR252,PR251 POP from NI to I
45. Move PR72 to PQ24.3
46. Change AL1-AL4, L16 and L17 value and QPN, Change R709, R700, R350, R701 QPN(from 5% to 1%)
47. Change P5, P150, P151, CN7, CON1, CN18 QPN for plating request
48. Change R104 and R112 value and QPN for 14M CLK fine tune
49. Change C163,C625 vaule and QPN, Stuff C541 22pF. Change R658 and C628 POP from NI to I
50. Change Q52 and Q61 from bipolar to MOS(footprint change). Add Q62(I) and R789(I)
50. Change C654 and C655 value, footprint and QPN
51. Change L24 and L26 power source to V_1P1_CL_MCH, Change L26 and L23 value/footprint, QPN and current rating
52. Change C41,C42,C49,C50,C420,C458 value, footprint and QPN
53. Change C469,C412,C396,C460,C445 and C423 QPN and temperature characteristic
54. Change C43 and C44 value and QPN
55. Change E1, E14, E15, E49, E16, E17, P54 QPN for plating 15u request
56. Del R247(I) and R257(I),T123,T124
57. Change C357 and C443 value and QPN
58. Add C302(NI), C304(NI), C401(NI), C402(NI)
59. Change XMM1 and XMM3 QPN for silkscreen modificaton
60. Change R213,PR36,PR40,PR41,D43,D44,R716 value and QPN
61. Change C135 POP from I to NI
62. Change Q61 from MOS to bipolar
63. Change R525, R517,R476 POP from NI to I
64. Change R789,R518,R641,R478 POP from I to NI, Change R641 value
65. Change R635 from NI to I, Change R635, R209 vaule and QPN
66. Change PC121,PC122,PC123,PC124,PR166,PR167,PR168,PR169,PC167 value and QPN
66. Change PR152 POP from I to NI, Change PR225,L23 QPN
67. Change XDP1,R1,R21,R22,R24,R51,R52,R25,R26,LED1,R20,R113,R181,R118,R297,R61,R153,R112,Q1,Q21,Q38,Q17 POP to PROTO
68. Change Q26,Q19,R18,R23,R506,Q2,Q20,Q32,LED4,LED9,LED5,LED10,LED2,LED7,LED3,U31,C515,C516,C518,C519,C520,D2,P54 POP to PROTO
69. Change E17,U19,U43,R12,R13.R14,R39,R40,R42,C2,C3,C4,R772,R773,R774,U1,U2,C1,C10,R5,R2,R3,R4,R8,L1,L2,C7,C8,D34 POP to PROTO
70. Change D35,D36,D37,CON2 POP to PROTO

Quanta Computer Inc.
PROJECT : ZN5
Size | Document Number: CHANGE LIST(EVT2 to DVT1.0) | Rev: X4
Date: Friday, March 05, 2010 | Sheet 39 of 40

DATE	ZN5 Schematic file for EVT2	Revision
5th Mar. 2010	ZN5-0305.DSN	X4
PS	ZN5 Schematic Change from DVT1.0 to DVT1.5	

Schematic Change Description
1. Update schematic reversion and sheet number
2. Add JS8 short pin to separate V_1P1_CORE_EXP to V_1P1_CORE
3. Connect RJ45 connector pin 6 to VCC1.8M_LAN
4. Change Q25 pin 2 netname to DIGON_R#
5. Change R716 POP from I to NI, R715 and R259 POP form NI to I
6. Add D48(I), R790(NI),R247(NI)
7. Add R791(I) as ICH_PWROK damping resistor
8. Change L23 footprint
9. Change R718 pull up source to V_1P1_CORE
10. Add D60(NI),R257(NI),R792(NI)
11. Add C759(I) for stitching cap, Change R51,R52 value to 4.7K & 2.2K. Add C288(I)
12. Change R39,R40 and R42 the footprint to 0402 from 0603 and change the location near to GMCH
13. BOM change apply correct HF speaker connector
14. BOM change from HP request, apply sonic focus function ALC272AF-GR chip
15. Change Pin L3, H4, F9, AF3, AC4, V4, P3 power source to V_1P1_CORE
16. Change R131 POP from NI to I and R127 POP from I to NI
17. Schematic change from vendor suggestion. LDO Vin GND from AGND to DGND
18. Reduce POP noise, AC27 from 0.1uF/10v X5R to 0.1uF/25v/X7R ; AC25 from 10uF / 6.3v to 2.2uF /6.3v
19. Follow Cayman design HP output FSOV >= 1Vrms spec AR12/AR16 from 56 ohm to 39 ohm
20. Change R85 value and QPN
21. Change R585 and R717 POP from NI to I. Add R793(NI), Move C263 and C264 near to ODD connector side
22. update dedicated netname on schematic page 31-36
23. Change C486, C490,C718-C731,C756-C759 QPN, Add C760(NI),C761(NI),C762(NI),C763(NI)
24. Change R481 pull high source to 5V_LDO, Change PU6 pin 6 connect to 5V_LDO, Add PR255(I), PQ70(I)
25. Add C766-C772(I) ,PR256-PR259(NI), PR260(I),PC209(NI), PC213(NI), PC214(NI), PQ71(NI), PQ72(NI)
26. Change R420 pull up power source to 3VSB, Add C403(I), Change PC159 value
27. Add PC215(I), PR261(I), Change PR191 and PC162 from I to NI, Add PR262(NI), PC50(NI)
28. Change R437 and R483 POP from I to NI, Change R439, R436, R485, R484 POP from NI to I
29. Add C764(I), R794(I), C405(NI), Change R525 POP from I to NI, Change Q52 to Bipolar, R137 pull up voltage change to 3VSB
30. Add R795(I), C765(NI), Change D40 POP from I to NI, Add R796(NI), Change R300 and R301 value and QPN
31. Change C7, C8, C321, C260,C142, PC68, C481, C477, C603, R264, PR95 QPN, Change C153 footprint and QPN
32. Del RP18, Add R797-R800(I), Change J93,J94,J70,J71,J90,J91,J92 QPN
33. Change PD13 to SS0540 and POP from I to NI
34. Update dedicated netname on schematic page 3-36
35. Change AL1-AL4, L16, L17 value and QPN
36. Change U8 to PI3PCIE2612-BZFE
37. Move PC215 to PU6.2 and Change PC215 footprint and QPN, Add PR263(I), C773(I), C774(I)
38. Change U54 to TPS2060, Correct 2 pcs Mini Card CONN Symbol, Connect the pin 41,39,24 to 3V_SLOT1 for 2 pcs Mini Card CONN.
39. Add PQ73(I)
40. Del R785(I), CN25(I)
41. Change D12, D13, D41, D42 to SS0540, Swap U8 some net for la yout smoothly
42. Change XMM1 and XMM3 to right color, Change L21, L22, L23, L24, L26 component, Add AC38(NI)
43. Del C81(I), R437(NI), R483(NI), Change L23 value footprint and QPN, Change L27, L28 footprint and QPN
44. Move R791 near U55 output side, Change R21, R22, R24 and R26 value and QPN, Chnage XDP conn pin 48 connection
45. Add C81(I), Change L23 value footprint and QPN for HP reqeust
46. Change to AU1 pin7 and pin9 to AGND

Quanta Computer Inc.
PROJECT : ZN5

Size	Document Number	Rev
	CHANGE LIST(DVT1.0 to DVT1.5)	X4

Date: Friday, March 05, 2010 Sheet 40 of 40