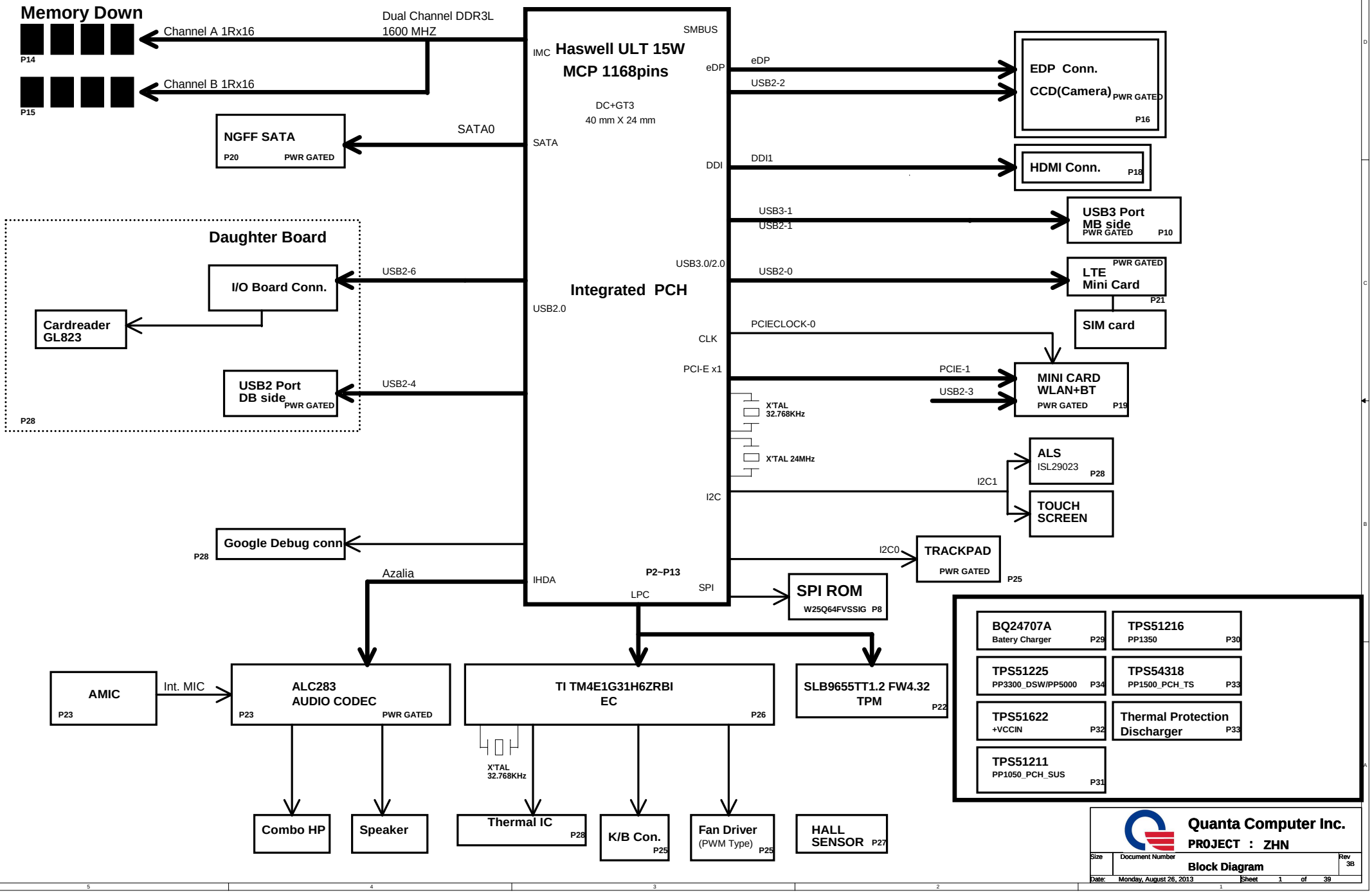
ZHN SHB ULT SYSTEM BLOCK DIAGRAM

01



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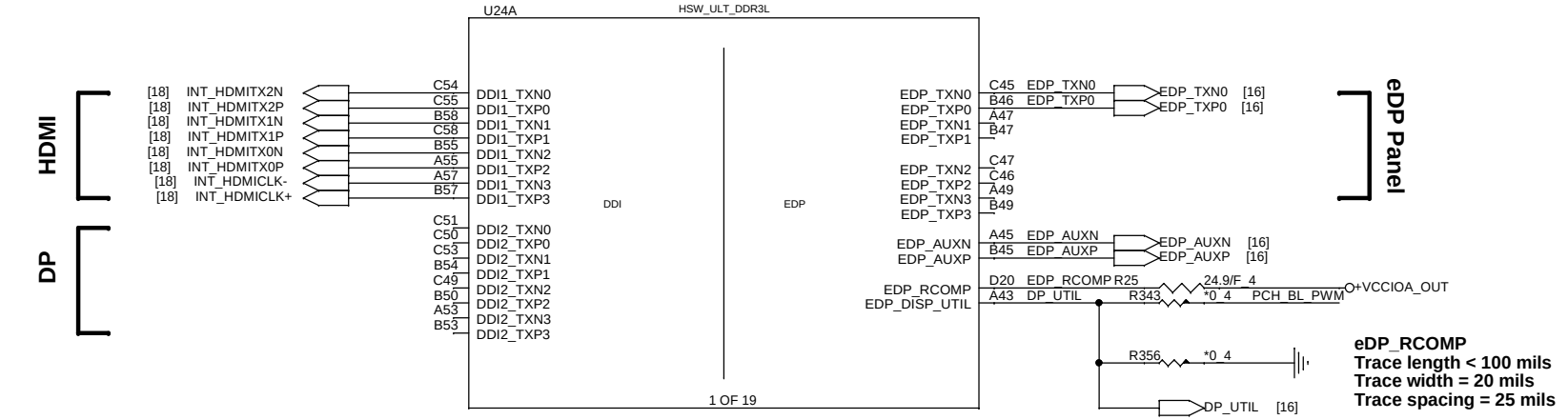
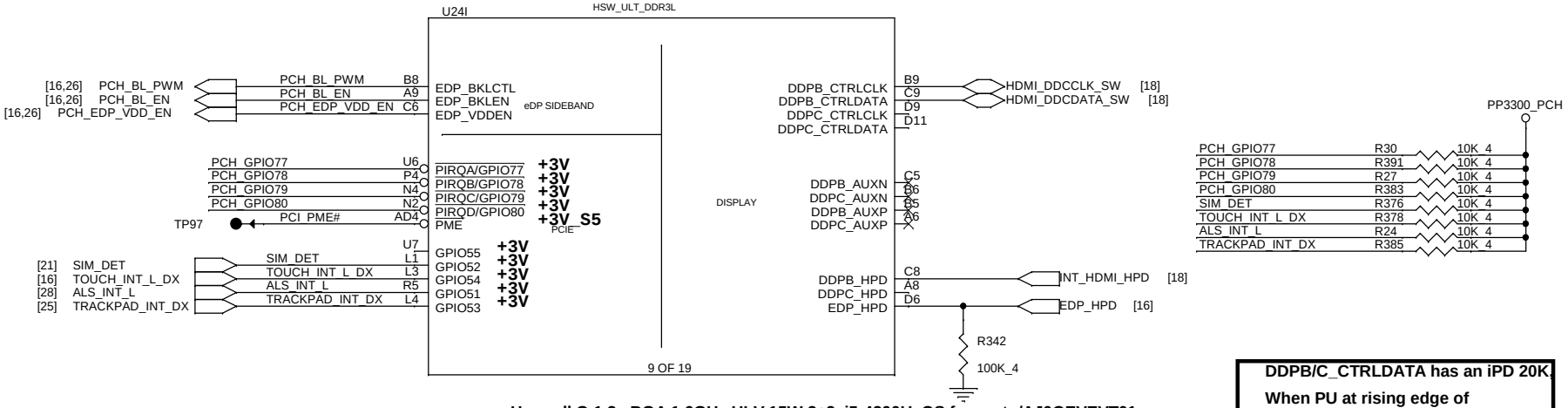
Haswell ULT (DISPLAY,eDP)

02



eDP_RCOMP
Trace length < 100 mils
Trace width = 20 mils
Trace spacing = 25 mils



DDPB/C_CTRLDATA has an iPD 20K.

When PU at rising edge of PCH_PWROK, the DDI port will be detected

Haswell C-1 2c BGA 1.6GHz ULV 15W 2+2 i5-4200U QS for proto/AJ0QEVEVT01

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Haswell ULT (DDR3L)

Haswell Processor (DDR3L)

03

U24C — HSW_ULT_DDR3L — DDR CHANNEL A — 3 OF 19

[14] M_A_DQ<0>	AH63	SA_DQ0	
[14] M_A_DQ<1>	AH62	SA_DQ1	
[14] M_A_DQ<2>	AK63	SA_DQ2	
[14] M_A_DQ<3>	AK62	SA_DQ3	
[14] M_A_DQ<4>	AH61	SA_DQ4	
[14] M_A_DQ<5>	AH60	SA_DQ5	
[14] M_A_DQ<6>	AK61	SA_DQ6	
[14] M_A_DQ<7>	AK60	SA_DQ7	
[14] M_A_DQ<8>	AM63	SA_DQ8	
[14] M_A_DQ<9>	AM62	SA_DQ9	
[14] M_A_DQ<10>	AP63	SA_DQ10	
[14] M_A_DQ<11>	AP62	SA_DQ11	
[14] M_A_DQ<12>	AM61	SA_DQ12	
[14] M_A_DQ<13>	AM60	SA_DQ13	
[14] M_A_DQ<14>	AP61	SA_DQ14	
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[14] M_A_DQ<16>	AP58	SA_DQ16	
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[14] M_A_DQ<21>	AK58	SA_DQ21	
[14] M_A_DQ<22>	AR57	SA_DQ22	
[14] M_A_DQ<23>	AN57	SA_DQ23	
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[14] M_A_DQ<25>	AR55	SA_DQ25	
[14] M_A_DQ<26>	AM54	SA_DQ26	
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[14] M_A_DQ<29>	AK55	SA_DQ29	
[14] M_A_DQ<30>	AR54	SA_DQ30	
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[14] M_A_DQ<33>	AW58	SA_DQ33	
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[14] M_A_DQ<36>	AV58	SA_DQ36	
[14] M_A_DQ<37>	AU58	SA_DQ37	
[14] M_A_DQ<38>	AV56	SA_DQ38	
[14] M_A_DQ<39>	AU56	SA_DQ39	
[14] M_A_DQ<40>	AY54	SA_DQ40	
[14] M_A_DQ<41>	AW54	SA_DQ41	
[14] M_A_DQ<42>	AY52	SA_DQ42	
[14] M_A_DQ<43>	AW52	SA_DQ43	
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[14] M_A_DQ<49>	AK42	SA_DQ49	
[14] M_A_DQ<50>	AM43	SA_DQ50	
[14] M_A_DQ<51>	AM45	SA_DQ51	
[14] M_A_DQ<52>	AK45	SA_DQ52	
[14] M_A_DQ<53>	AK43	SA_DQ53	
[14] M_A_DQ<54>	AM40	SA_DQ54	
[14] M_A_DQ<55>	AM42	SA_DQ55	
[14] M_A_DQ<56>	AM46	SA_DQ56	
[14] M_A_DQ<57>	AK46	SA_DQ57	
[14] M_A_DQ<58>	AM49	SA_DQ58	
[14] M_A_DQ<59>	AK49	SA_DQ59	
[14] M_A_DQ<60>	AM48	SA_DQ60	
[14] M_A_DQ<61>	AK48	SA_DQ61	
[14] M_A_DQ<62>	AM51	SA_DQ62	
[14] M_A_DQ<63>	AK51	SA_DQ63	

SA_CLK#0	AU37	M_A_DIM0_CK_DDR0_DN	[14]
SA_CLK0	AV37	M_A_DIM0_CK_DDR0_DP	[14]
SA_CLK#1	AW36		
SA_CLK1	AY36		
SA_CKE0	AU43	M_A_DIM0_CKE0	[14]
SA_CKE1	AW43	TP127	
SA_CKE2	AY42	TP128	
SA_CKE3	AY43	TP129	
SA_CS#0	AP33	M_A_DIM0_CS0_N	[14]
SA_CS#1	AR32	TP41	
SA_ODT0	AP32	TP40	
SA_RAS	AY34	M_A_RAS_N	[14]
SA_WE	AW34	M_A_WE_N	[14]
SA_CAS	AU34	M_A_CAS_N	[14]
SA_BA0	AU35	M_A_BS0	[14]
SA_BA1	AV35	M_A_BS1	[14]
SA_BA2	AY41	M_A_BS2	[14]
SA_MA0	AU36	M_A_A<0>	[14]
SA_MA1	AY37	M_A_A<1>	[14]
SA_MA2	AR38	M_A_A<2>	[14]
SA_MA3	AP36	M_A_A<3>	[14]
SA_MA4	AU39	M_A_A<4>	[14]
SA_MA5	AR36	M_A_A<5>	[14]
SA_MA6	AV40	M_A_A<6>	[14]
SA_MA7	AW39	M_A_A<7>	[14]
SA_MA8	AY39	M_A_A<8>	[14]
SA_MA9	AU40	M_A_A<9>	[14]
SA_MA10	AP35	M_A_A<10>	[14]
SA_MA11	AW41	M_A_A<11>	[14]
SA_MA12	AU41	M_A_A<12>	[14]
SA_MA13	AR35	M_A_A<13>	[14]
SA_MA14	AV42	M_A_A<14>	[14]
SA_MA15	AU42	M_A_A<15>	[14]
SA_DQSN0	AJ61	M_A_DQS_DN<0>	[14]
SA_DQSN1	AN62	M_A_DQS_DN<1>	[14]
SA_DQSN2	AM58	M_A_DQS_DN<2>	[14]
SA_DQSN3	AM55	M_A_DQS_DN<3>	[14]
SA_DQSN4	AV57	M_A_DQS_DN<4>	[14]
SA_DQSN5	AV53	M_A_DQS_DN<5>	[14]
SA_DQSN6	AL43	M_A_DQS_DN<6>	[14]
SA_DQSN7	AL48	M_A_DQS_DN<7>	[14]
SA_DQSP0	AJ62	M_A_DQS_DP<0>	[14]
SA_DQSP1	AN61	M_A_DQS_DP<1>	[14]
SA_DQSP2	AN58	M_A_DQS_DP<2>	[14]
SA_DQSP3	AN55	M_A_DQS_DP<3>	[14]
SA_DQSP4	AW57	M_A_DQS_DP<4>	[14]
SA_DQSP5	AW53	M_A_DQS_DP<5>	[14]
SA_DQSP6	AL42	M_A_DQS_DP<6>	[14]
SA_DQSP7	AL49	M_A_DQS_DP<7>	[14]
SM_VREF_CA	AP49	+VREF_CA_CPU	
SM_VREF_DQ0	AR51	+VREFDQ_SA_M3	
SM_VREF_DQ1	AP51	+VREFDQ_SB_M3	

6/25 Add TP127~TP132 for XDP by Intel.

U24D — HSW_ULT_DDR3L — DDR CHANNEL B — 4 OF 19

[15] M_B_DQ<0>	AY31	SB_DQ0	
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[15] M_B_DQ<4>	AV31	SB_DQ4	
[15] M_B_DQ<5>	AU31	SB_DQ5	
[15] M_B_DQ<6>	AV29	SB_DQ6	
[15] M_B_DQ<7>	AU29	SB_DQ7	
[15] M_B_DQ<8>	AY27	SB_DQ8	
[15] M_B_DQ<9>	AW27	SB_DQ9	
[15] M_B_DQ<10>	AY25	SB_DQ10	
[15] M_B_DQ<11>	AW25	SB_DQ11	
[15] M_B_DQ<12>	AV27	SB_DQ12	
[15] M_B_DQ<13>	AU27	SB_DQ13	
[15] M_B_DQ<14>	AV25	SB_DQ14	
[15] M_B_DQ<15>	AU25	SB_DQ15	
[15] M_B_DQ<16>	AM29	SB_DQ16	
[15] M_B_DQ<17>	AK29	SB_DQ17	
[15] M_B_DQ<18>	AL28	SB_DQ18	
[15] M_B_DQ<19>	AK28	SB_DQ19	
[15] M_B_DQ<20>	AR29	SB_DQ20	
[15] M_B_DQ<21>	AN29	SB_DQ21	
[15] M_B_DQ<22>	AR28	SB_DQ22	
[15] M_B_DQ<23>	AP28	SB_DQ23	
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[15] M_B_DQ<27>	AP25	SB_DQ27	
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[15] M_B_DQ<29>	AM26	SB_DQ29	
[15] M_B_DQ<30>	AK25	SB_DQ30	
[15] M_B_DQ<31>	AL25	SB_DQ31	
[15] M_B_DQ<32>	AY23	SB_DQ32	
[15] M_B_DQ<33>	AW23	SB_DQ33	
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[15] M_B_DQ<35>	AW21	SB_DQ35	
[15] M_B_DQ<36>	AV23	SB_DQ36	
[15] M_B_DQ<37>	AU23	SB_DQ37	
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[15] M_B_DQ<49>	AR22	SB_DQ49	
[15] M_B_DQ<50>	AL21	SB_DQ50	
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[15] M_B_DQ<61>	AM20	SB_DQ61	
[15] M_B_DQ<62>	AR18	SB_DQ62	
[15] M_B_DQ<63>	AP18	SB_DQ63	

SB_CK#0	AM38	M_B_DIM0_CK_DDR0_DN	[15]
SB_CK0	AN38	M_B_DIM0_CK_DDR0_DP	[15]
SB_CK#1	AK38		
SB_CK1	AL38		
SB_CKE0	AY49	M_B_DIM0_CKE0	[15]
SB_CKE1	AU50	TP130	
SB_CKE2	AW49	TP131	
SB_CKE3	AV50	TP132	
SB_CS#0	AM32	M_B_DIM0_CS0_N	[15]
SB_CS#1	AK32	TP35	
SB_ODT0	AL32	TP31	
SB_RAS	AM35	M_B_RAS_N	[15]
SB_WE	AK35	M_B_WE_N	[15]
SB_CAS	AM33	M_B_CAS_N	[15]
SB_BA0	AL35	M_B_BS0	[15]
SB_BA1	AM36	M_B_BS1	[15]
SB_BA2	AU49	M_B_BS2	[15]
SB_MA0	AP40	M_B_A<0>	[15]
SB_MA1	AR40	M_B_A<1>	[15]
SB_MA2	AP42	M_B_A<2>	[15]
SB_MA3	AR42	M_B_A<3>	[15]
SB_MA4	AR45	M_B_A<4>	[15]
SB_MA5	AP45	M_B_A<5>	[15]
SB_MA6	AW46	M_B_A<6>	[15]
SB_MA7	AY46	M_B_A<7>	[15]
SB_MA8	AY47	M_B_A<8>	[15]
SB_MA9	AU46	M_B_A<9>	[15]
SB_MA10	AK36	M_B_A<10>	[15]
SB_MA11	AV47	M_B_A<11>	[15]
SB_MA12	AU47	M_B_A<12>	[15]
SB_MA13	AK33	M_B_A<13>	[15]
SB_MA14	AR46	M_B_A<14>	[15]
SB_MA15	AP46	M_B_A<15>	[15]
SB_DQSN0	AW30	M_B_DQS_DN<0>	[15]
SB_DQSN1	AV26	M_B_DQS_DN<1>	[15]
SB_DQSN2	AN28	M_B_DQS_DN<2>	[15]
SB_DQSN3	AN25	M_B_DQS_DN<3>	[15]
SB_DQSN4	AW22	M_B_DQS_DN<4>	[15]
SB_DQSN5	AV18	M_B_DQS_DN<5>	[15]
SB_DQSN6	AN21	M_B_DQS_DN<6>	[15]
SB_DQSN7	AN18	M_B_DQS_DN<7>	[15]
SB_DQSP0	AV30	M_B_DQS_DP<0>	[15]
SB_DQSP1	AW26	M_B_DQS_DP<1>	[15]
SB_DQSP2	AN28	M_B_DQS_DP<2>	[15]
SB_DQSP3	AM25	M_B_DQS_DP<3>	[15]
SB_DQSP4	AV22	M_B_DQS_DP<4>	[15]
SB_DQSP5	AW18	M_B_DQS_DP<5>	[15]
SB_DQSP6	AM21	M_B_DQS_DP<6>	[15]
SB_DQSP7	AM18	M_B_DQS_DP<7>	[15]

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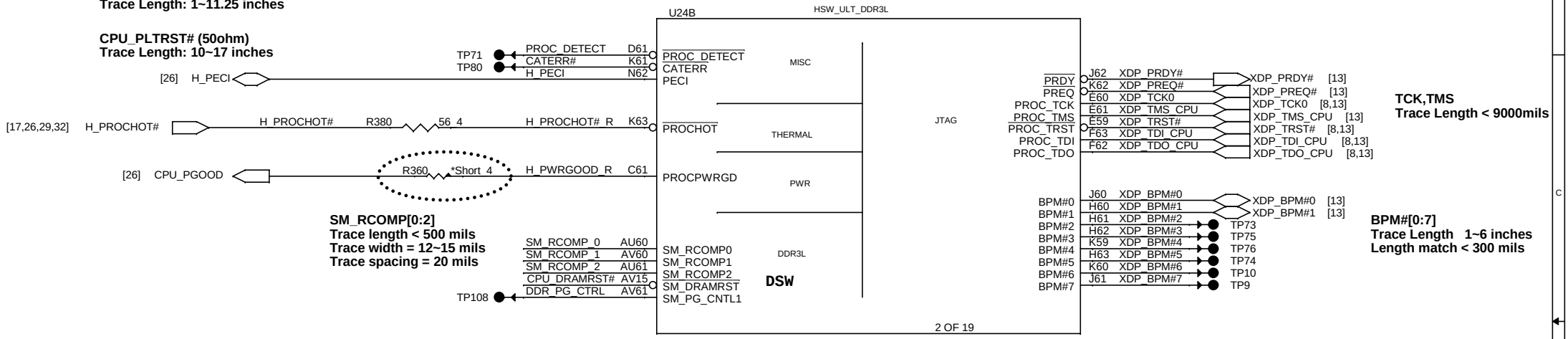
Haswell ULT (SIDEBAND)

H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

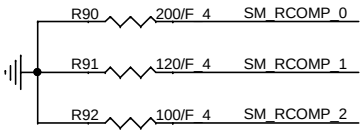


SM_RCOMP[0:2]
Trace length < 500 mils
Trace width = 12~15 mils
Trace spacing = 20 mils

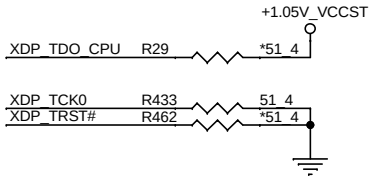
TCK,TMS
Trace Length < 9000mils

BPM#[0:7]
Trace Length 1~6 inches
Length match < 300 mils

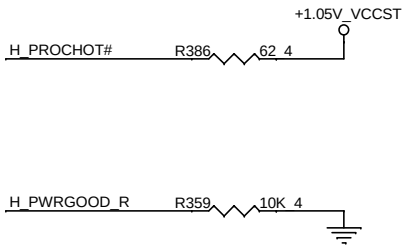
DRAM COMP



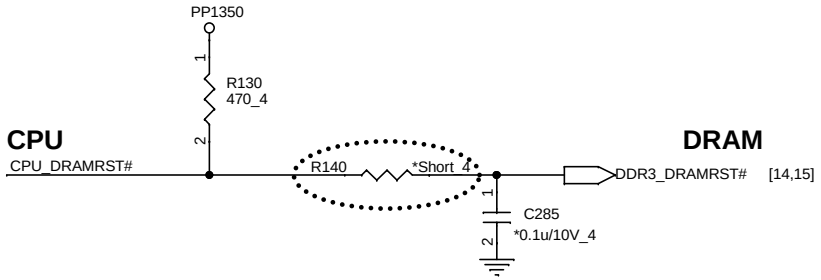
XDP PU/PD



PU/PD of CPU



DRAMRST



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	Haswell 3/5 (SideBand)	3B
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Haswell ULT (POWER)

05

VDDQ Output Decoupling Recommendations		
330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

6/21 Add C384~C388 by Intel DDR.

+1.35V_CPU 1.4A

C388 2.2u/6.3V_6, C91 10u/6.3V_6, C281 10u/6.3V_6, C92 10u/6.3V_6, C90 10u/6.3V_6

C385 22u/6.3V_8, C384 10u/6.3V_6, C386 10u/6.3V_6, C387 2.2u/6.3V_6, C283 10u/6.3V_6, C282 10u/6.3V_6

5/16 modify C282,C283 value by Intel suggest.

300mA
300mA

0415 VCCST_PWRGD need PP1050_RUN power good

0729 Add PWR_DEBUG to CN15.

U24L HSW_ULT_DDR3L

HSW ULT POWER

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VCC Output Decoupling Recommendations		
470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

Remove C390~C396

+VCCIN 32A

SVID

Layout note: need routing together and ALERT need between CLK and DATA.

Place PU resistor close to CPU

Place PU resistor close to CPU

VCCST PWRGD

U20 74AUP1G07GW

G Path

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	Haswell 4/5 (POWER)	3B
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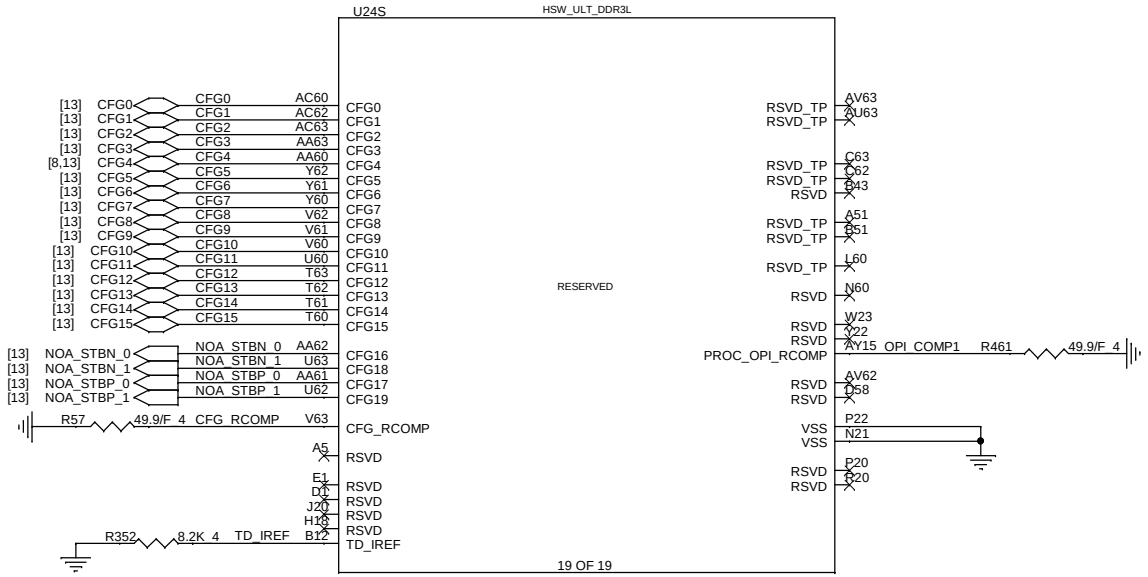
Haswell ULT (CFG,RSVD)

06



Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	**(DEFAULT) NORMAL OPERATION; NO STALL**	STALL	CFG0 R417 *1K 4
CFG1 PCH/ PCH LESS MODE SELECTION	**(DEFAULT) NORMAL OPERATION**	PCH-LESS MODE	CFG1 R423 *1K 4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	**DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT**	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R409 *1K 4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	**DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS**	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R403 *1K 4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	**VRS SUPPORTING SVID PROTOCOL ARE PRESENT**	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R394 *1K 4
CFG10 SAFE MODE BOOT	**POWER FEATURES ACTIVATED DURING RESET**	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R56 *1K 4

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Haswell ULT PCH (PM)

07

U24H HSW_ULT_DDR3L

SYSTEM POWER MANAGEMENT

[26] PCH_SUSACK_L — R428 *0_4 SUSACK#_R — SUSACK AK2
[13,17] SYS_RESET# — SYS_RESET# — SYS_RESET AC3
[5,13,26] SYS_PWROK — SYS_PWROK R421 — C265 *1u/6.3V_4 *Short_4 — SYS_PWROK_R AG2 — SYS_PWROK
PCH_PWROK R482 *Short_4 — PCH_PWROK_R AY7 — PCH_PWROK
APWROK_R AB5 — APWROK
PCI_PLTRST# AG7 — PLTRST

+3V_S5

[26] PCH_RSMRST_L — R478 *Short_4 — PCH_RSMRST# AW6 — RSMRST
[26] PCH_SUSWARN_L — R453 *0_4 — PCH_SUSPWRACK AV4 — SUSWARN/SUSPWRDNACK/GPIO30
[26] PCH_PWRBTN_L — R147 *Short_4 — PCH_PWRBTN# AL7 — PWRBTN
[29] ACPRESENT — R61 *Short_4 — PCH_ACPRESENT AJ8 — ACPRESENT/GPIO31
PCH_BATLOW# AN4 — BATLOW/GPIO72
[13,26] PCH_SLP_S0_L — R415 *Short_4 — PCH_SLP_S0#_R AF3 — SLP_S0
AM5 — SLP_WLAN/GPIO29
TP37

+3V_S5

DSW

DSWVRMEN — AW7 DSWVREN — R477 *Short_4 — DSWVREN [8]
DPWROK — AV5 DPWROK_R — PCH_DPWROK [26]
WAKE — AJ5 PCIE_PCH_WAKE# — R74 *Short_4 — PCH_WAKE_L [26]

Deep Sx

CLKRUN/GPIO32 — V5 CLKRUN# — R38 *Short_4 — LPC_CLKRUN_L — LPC_CLKRUN_L [26]
SUS_STAT/GPIO61 — AG4 PCH_SUS_STAT — TP27
SUSCLK/GPIO62 — AE6 PCH_SUSCLK — TP23
SLP_S5/GPIO63 — AP5 PCH_SLP_S5_L — PCH_SLP_S5_L [13,26,30,35]

SLP_S4 — AJ6 PCH_SLP_S4_L — PCH_SLP_S4_L [13]
SLP_S3 — AT4 PCH_SLP_S3_L — PCH_SLP_S3_L [13,26,30,31,33,35]
SLP_A — AL5 PCH_SLP_A_L — PCH_SLP_A_L [13]
SLP_SUS — AP4 PCH_SLP_SUS_L — PCH_SLP_SUS_L [26,35]
SLP_LAN — AJ7 PCH_SLP_LAN# — TP38

PCH_SUSPWRACK R427 0_4 SUSACK#_R

8 OF 19

6/25 R74 stuff by Google.

4/22 modify, default skip EC control

PCH PM PU/PD

PP3300_PCH
CLKRUN# R37 8.2K_4
SYS_RESET# R406 10K_4

PCH_RSMRST# R479 10K_4
SYS_PWROK R80 *10K_4
DPWROK_R R473 100K/F_4

PP3300_PCH_SUS
PCH_SUSPWRACK R454 10K_4
SYS_PWROK R426 *1K_4

PP3300_DSW
PCH_ACPRESENT R62 10K_4
PCH_BATLOW# R444 8.2K_4
PCIE_PCH_WAKE# R75 10K_4
PCH_PWRBTN# R151 *10K_4

PCH PWROK

[5,26] PCH_PWROK — PCH_PWROK — R483 *Short_4 — PCH_PWROK_R
R487 100K_4
PCH_RSMRST_L — R474 *0_4 — DPWROK_R
Non Deep Sx

PLTRST# Buffer

PCI_PLTRST# R152 *Short_4 PLTRST#
PP3300_PCH
C94 *0.1u/10V_4
U6 *TC7SH08FU
PCI_PLTRST# — PLTRST# [13,19,21,22,26]
R155 100K_4

4/22 modify, default is bypass PLTRST#

Quanta Computer Inc.
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Size	Document Number	Rev
	PCH 1/6 (PM)	3B
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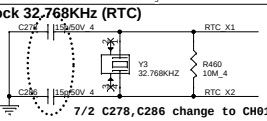
Haswell ULT PCH (RTC/HDA/SATA/SPI)

Haswell ULT PCH(LPC,SPI,SMBUS,C-LINK,THERMAL)

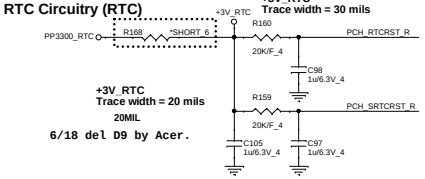
08

RTC Clock 32.768KHz (RTC)



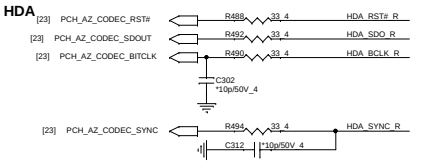
7/2 C278,C286 change to CH01506JB06.

RTC Circuitry (RTC)



6/18 del D9 by Acer.

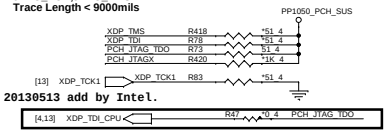
HDA



PCH JTAG

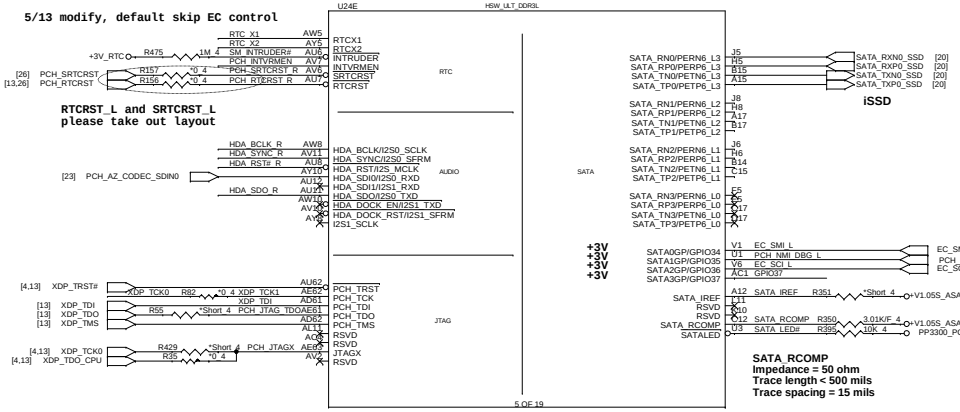
JTAG_TCK,JTAG_TMS
Trace Length < 9000mils

MP remove(Intel)



20130513 add by Intel.

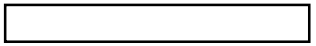
5/13 modify, default skip EC control



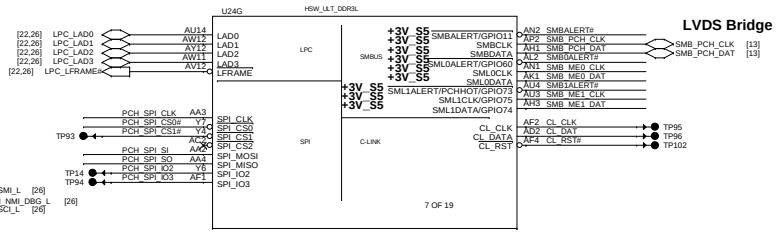
SATA_RCOMP
Impedance = 50 ohm
Trace length < 500 mils
Trace spacing = 15 mils

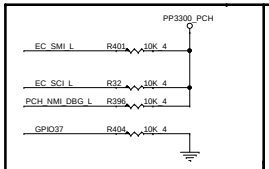
6/18 del RTC battery circuit by Acer.

4/23 modify for WP circuit

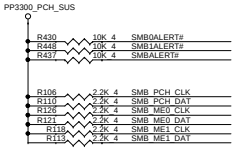


LVDS Bridge



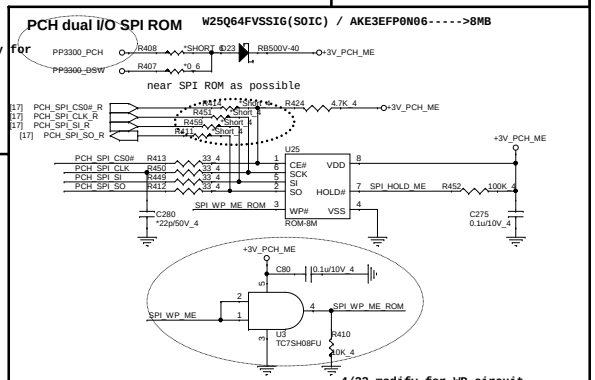


SMBus

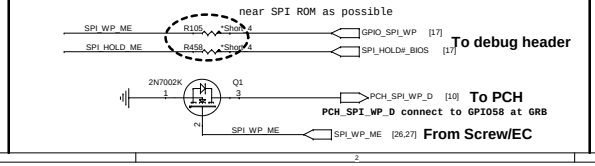


PCH dual i/O SPI ROM

W25Q64FVSSIG(SOIC) / AKE3EFP0N06----->8MB



4/23 modify for WP circuit



ULT Strapping Table

Note: R493 need stuff on MP.

Pin Name	Strap description	Sampled	Configuration	note
GPIO81(SPKR)	No reboot on TCO Timer expiration	PWROK	**0 = Default enable (iPD 20K)** 1 =Disable No-Reboot mode	PP3300_PCH R400 *1K_4 SPKR SPKR [10,23]
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	**0 = Default can program ME (iPD 20K)** 1 =can't program ME	HDA_SDO_R R493 *0_4 PCH_HDA_SDO [26]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	**1=Should be always pull-up**	+3V_RTC R484 330K_4 PCH_INTVRMEN R485 *330K_4
GPIO66	Top-Block Swap override		**0 = Default disable (iPD 20K)** 1 = Enable TBS function	[10] GPIO66 PP3300_PCH R330 *1K_4 GPIO66 R340 *1K_4
GPIO86	Boot BIOS Strap Bit		**0 = Default SPI (iPD 20K)** 1 =LPC	[10] GPIO86 PP3300_PCH R1 *1K_4 GPIO86 R7 *1K_4
GPIO15	TLS(Transport layer security)		**0 = Default enable w/o confidentiality(iPD 20K)** 1 =Default enable with confidentiality	[10] GPIO15 PP3300_PCH_SUS R50 *8.2K_4 GPIO15 R58 *1K_4 x86 stuff
CFG4	DP presence strap		**0 = Enable an external display port is connected to the eDP** 1 =disable	[6,13] CFG4 CFG4 R64 1K_4
DSWVREN	Deep Sx well on die VR enable		**1=Should be always pull-up**	[7] DSWVREN +3V_RTC R476 330K_4 DSWVREN R472 *330K_4

Quanta Computer Inc.
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	PCH 2/6 (RTC/HDA/SATA/SPI)	3B

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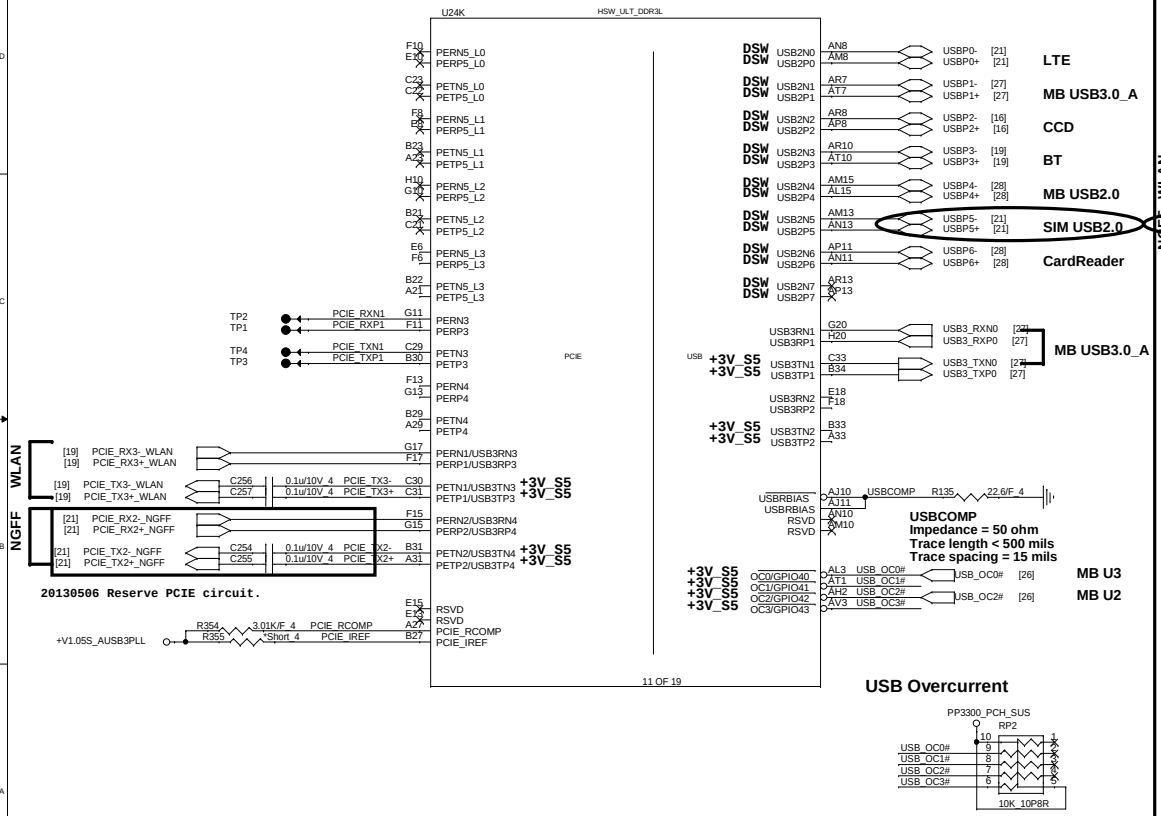
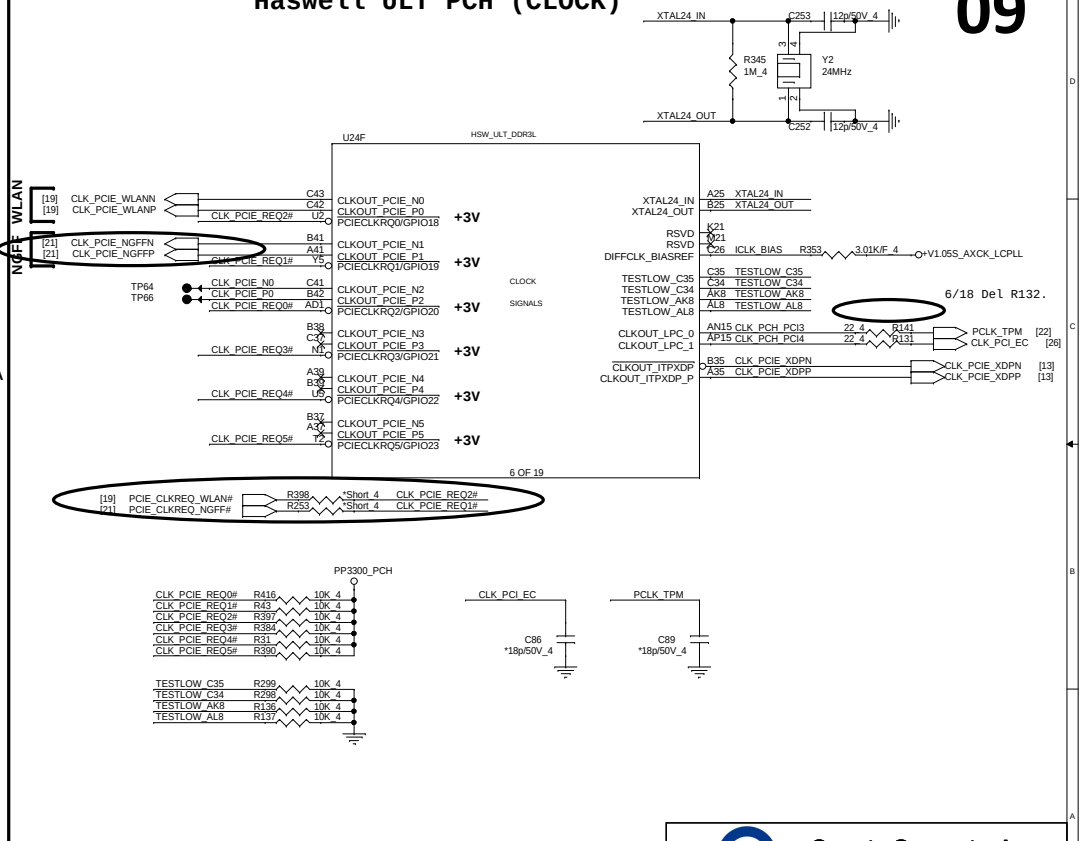
Haswell ULT PCH (PCIE,USB3.0,USB2.0)



Haswell ULT PCH (CLOCK)

09



Haswell ULT PCH (GPIO,CPU/MISC,NCTF)

U24J — HSW_ULT_DDR3L — 10 OF 19

4/22 modify

LTE_DISABLE_L need PU to +3V_LTE

4/23 modify

6/24 Connect DEVSLP0 to SSD.

4/23 modify, those 3 power enable pin are PD 100K already

4/23 modify, follow Intel suggestion to un-stuff for unused GPIO

strapping

strapping

TRACKPAD

TOUCHSCREEN / ALS

PCH GPIO PU/PD

20130507 Add R1014 for PU DEVSLP0.

20130613 change R331,R332 to 4.7K.

RAM ID

4/22 modify

Vender	RAM_ID ID2	ID1	ID0	Q PN	Mfr. PN	Freq.
Micron(4G)	0	0	0	AKD5JGSTL10	MT41K256M16HA-125:E	1600MHz
Hynix(4G)	0	0	1	AKD5JGETW04	H5TC4G63AFR-PBA	1600MHz
Elpida(4G)	0	1	0	AKD5JGST407	EDJ4216EFBG-GNL-F	1600MHz
Micron(2G)	1	0	0	AKD5JGSTL10	MT41K256M16HA-125:E	1600MHz
Hynix(2G)	1	0	1	AKD5JGETW04	H5TC4G63AFR-PBA	1600MHz
Elpida(2G)	1	1	0	AKD5JGST407	EDJ4216EFBG-GNL-F	1600MHz

CPU thermal trip

GPIO27 : If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

5/31 Reserve R16 and R575 to PU.

Quanta Computer Inc.	
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Size	Document Number: PCH 4/6 (GPIO/MISC) — Rev: 3B
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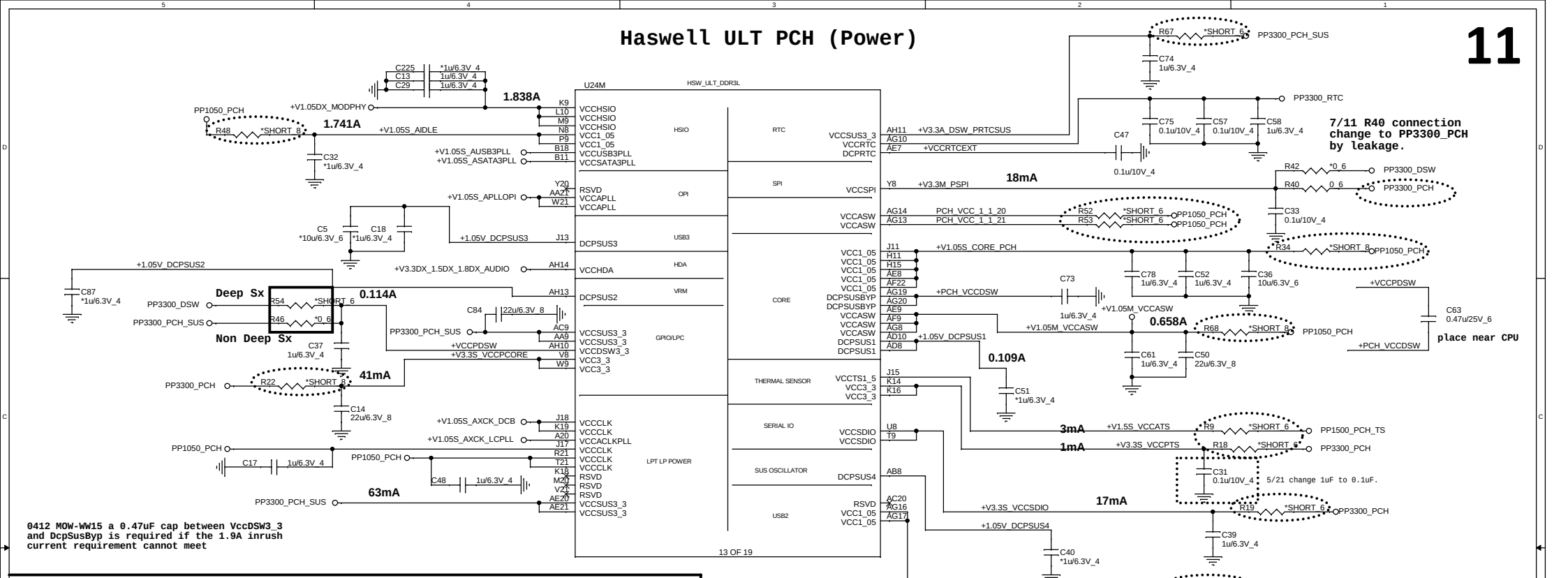
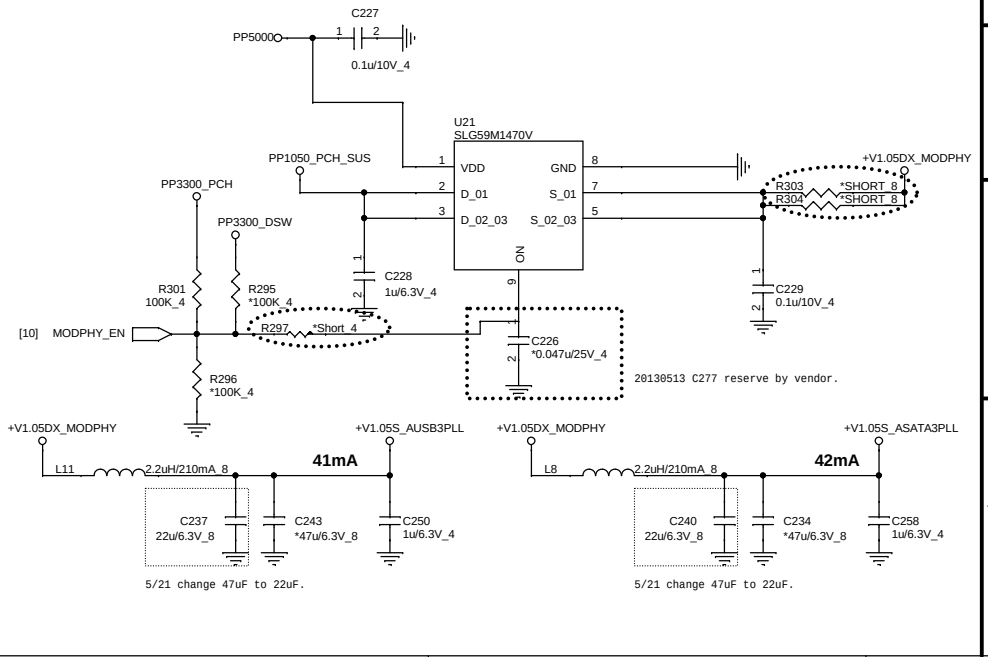
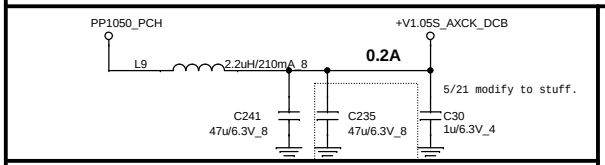
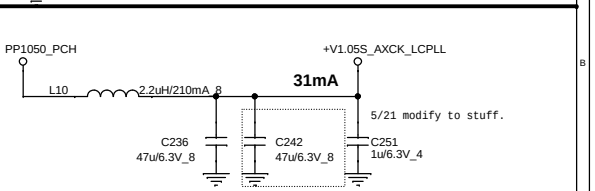
Haswell ULT PCH (Power)



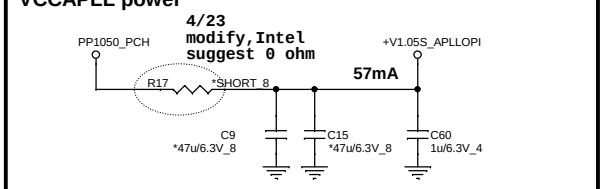
PCH VCCHSIO Power



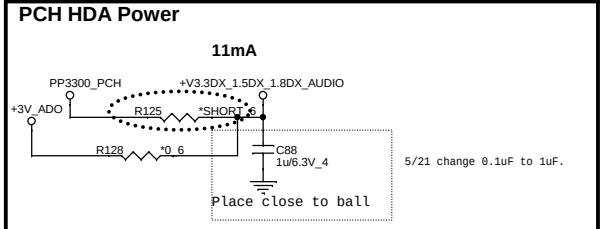




VCCAPLL power



PCH HDA Power



Quanta Computer Inc.		
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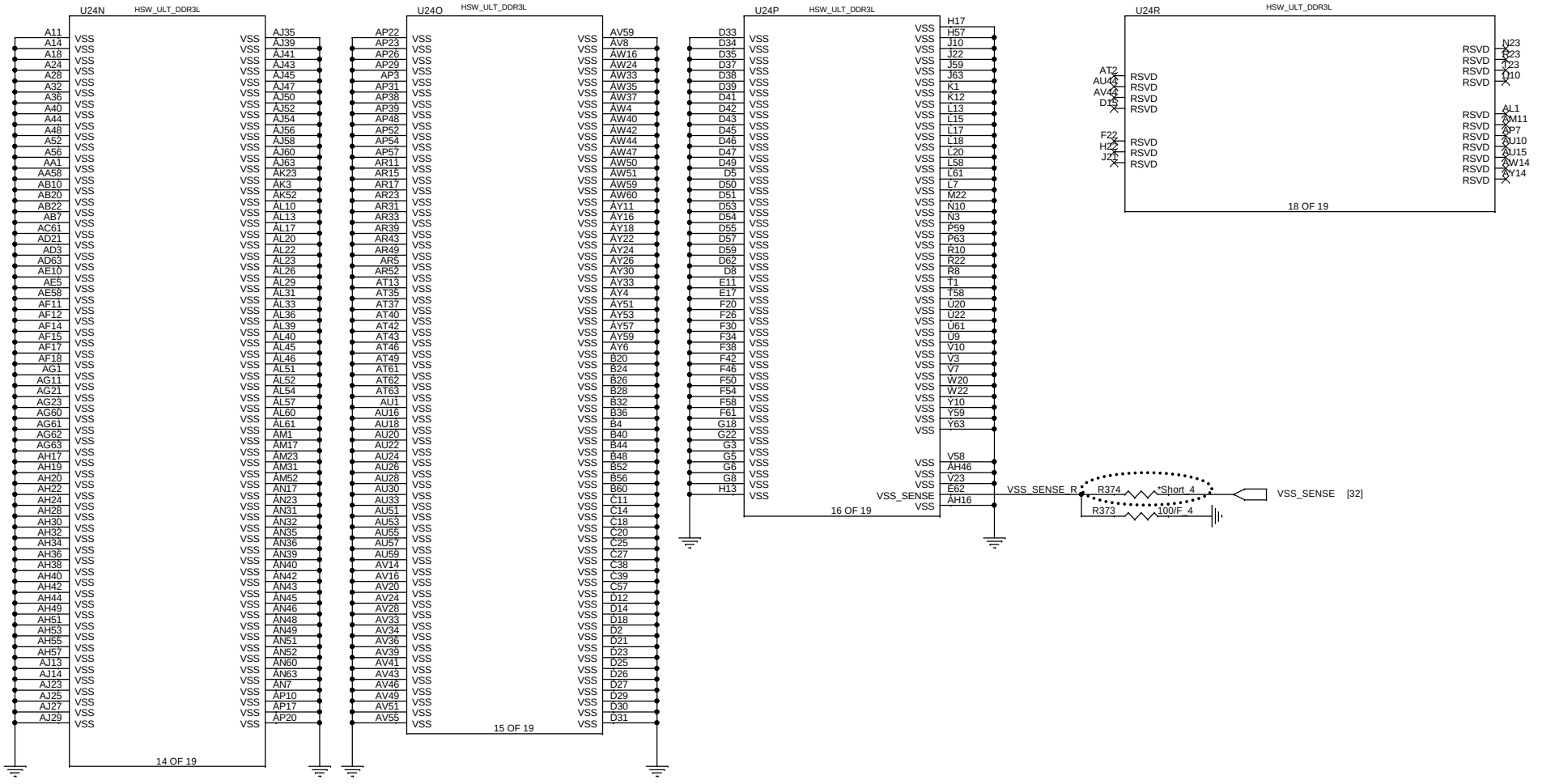
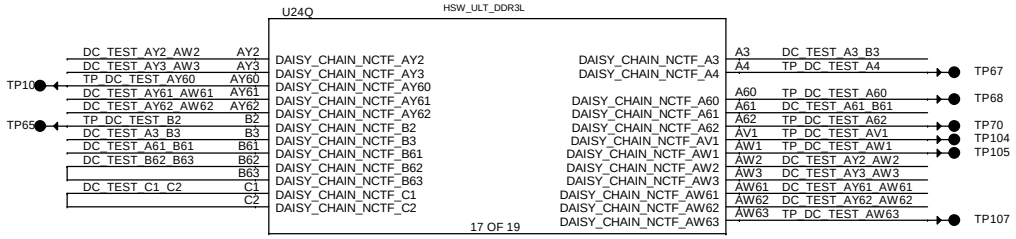
Haswell ULT (GND)





Quanta Computer Inc.		
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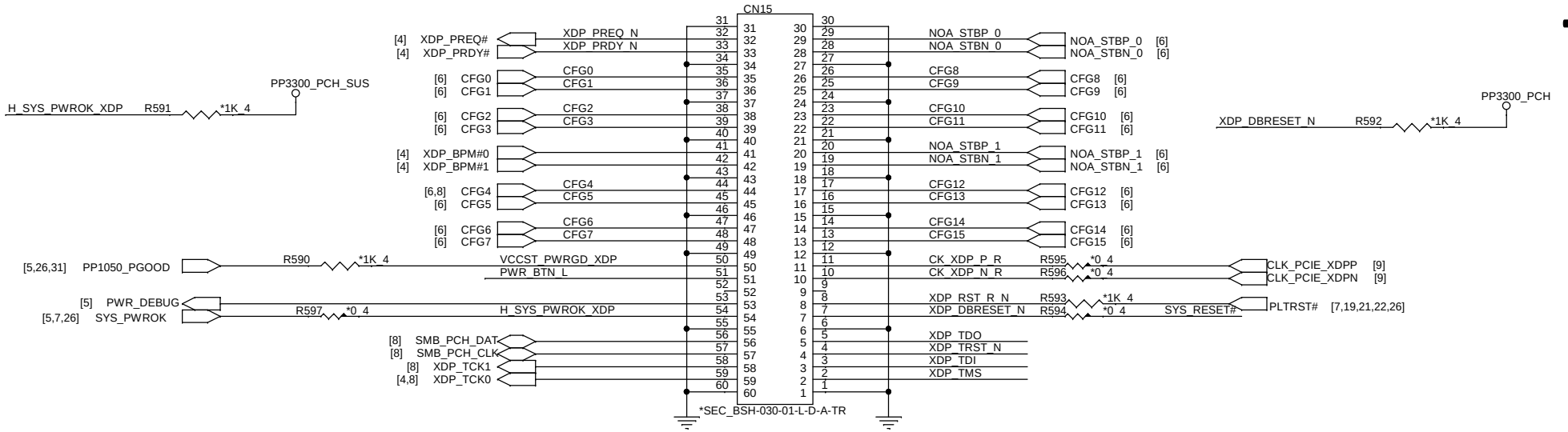
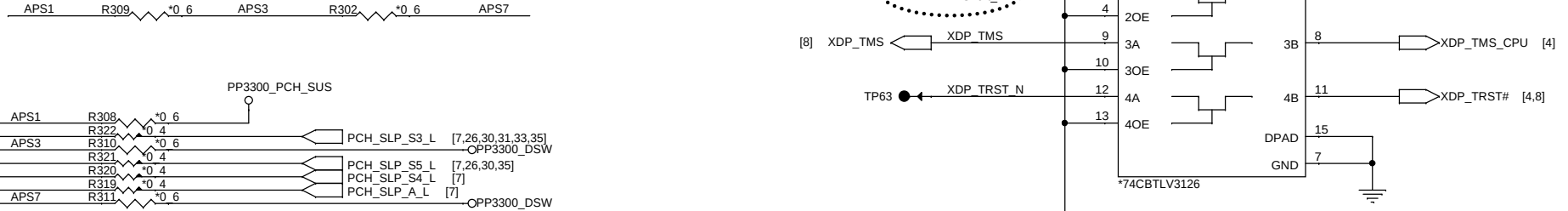
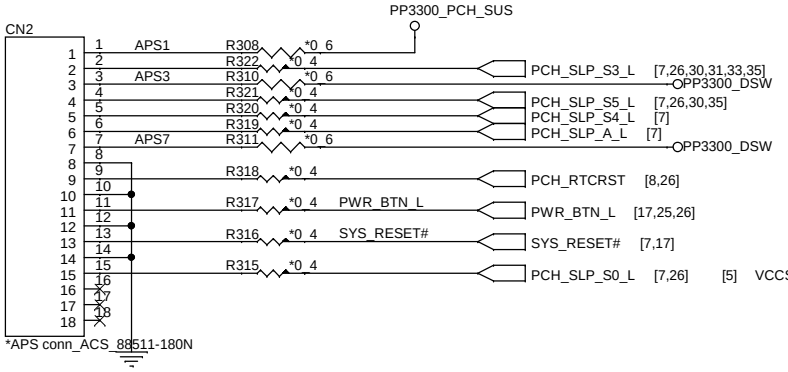
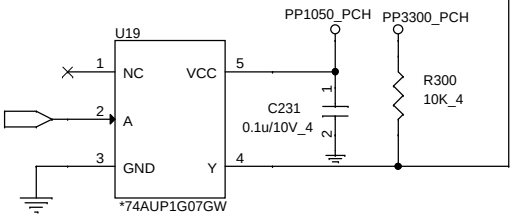




APS





Quanta Computer Inc.

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Size	Document Number	Rev
	CPU/PCH XDP	3B
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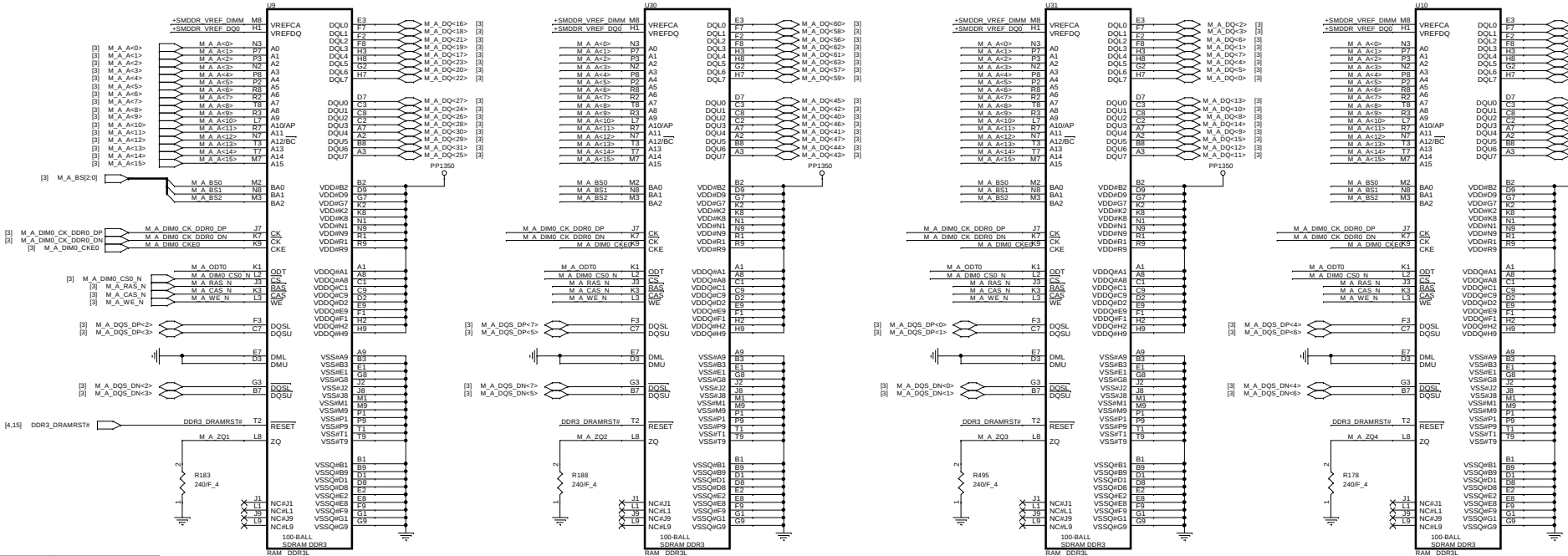
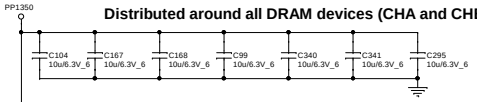
<DDR>

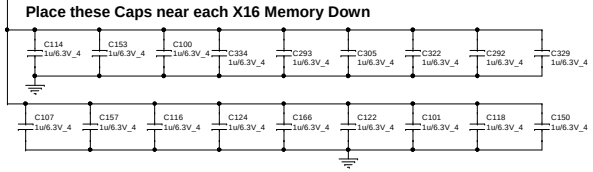
BYTE2_16-23
BYTE3_24-31
BYTE7_56-63
BYTE5_40-47
BYTE0_0-7
BYTE1_8-15
BYTE4_32-39
BYTE6_48-55

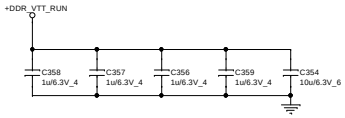


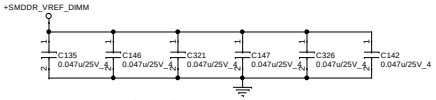
Micron/MT41K256M16HA-125:E/AKD5JGSTL02 for proto board

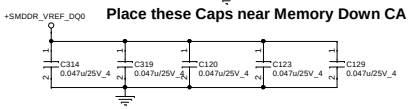
Vendor	P/N	
Hynix		
Elpida	AKD5JGST400	DDR3L 1333Mhz 4Gb
	AKD5JGST404	DDR3L 1600Mhz 4Gb

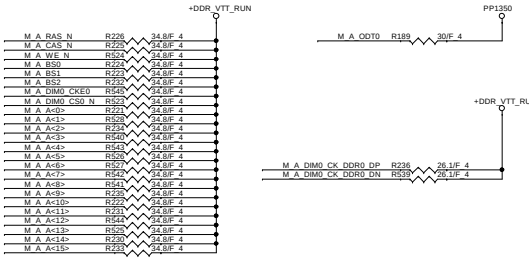


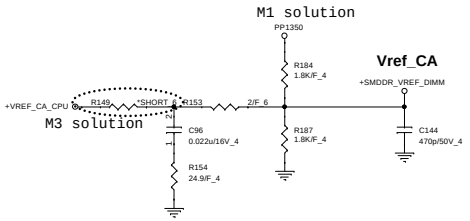


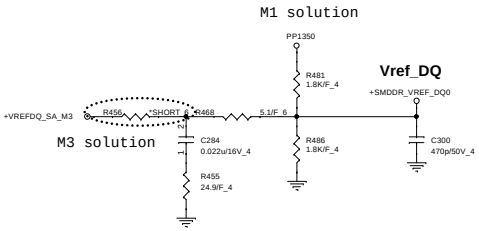












S_CLIP1 *SUL-12A2M
S_CLIP3 *SUL-12A2M
S_CLIP2 *SUL-12A2M
S_CLIP4 *SUL-12A2M

Quanta Computer Inc.
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	DDR3L MEMORY DOWNx16 A	3B
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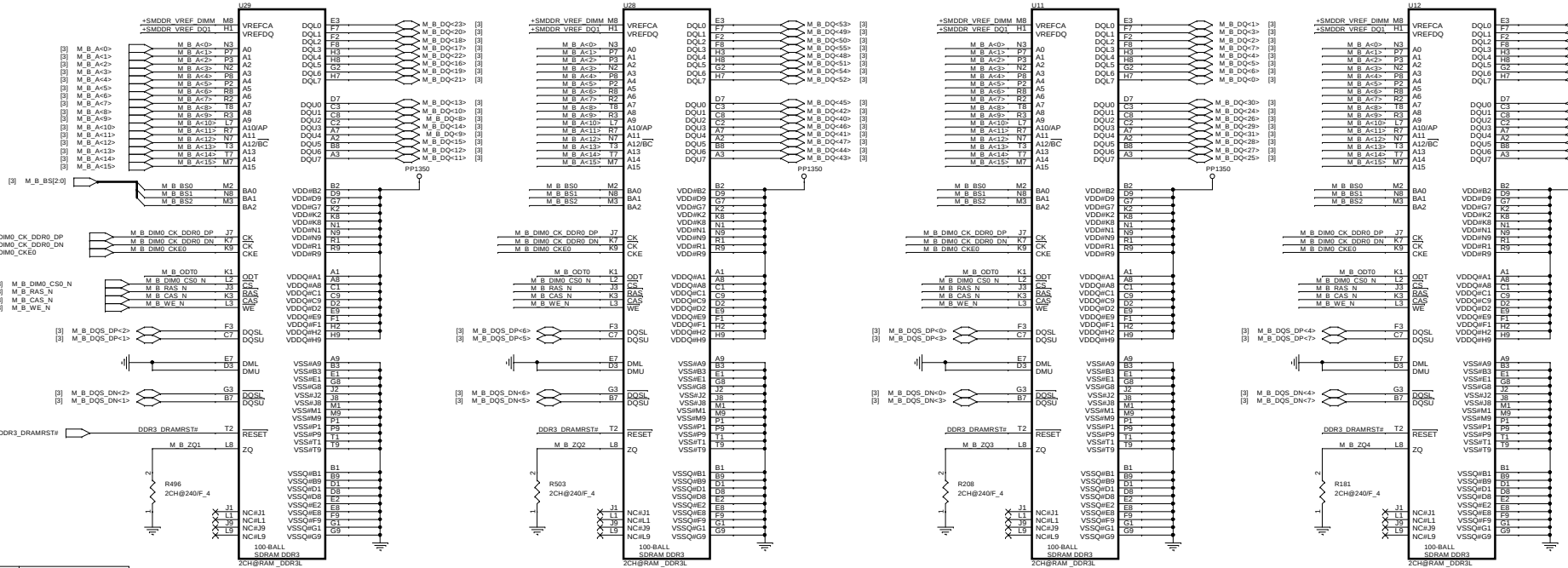
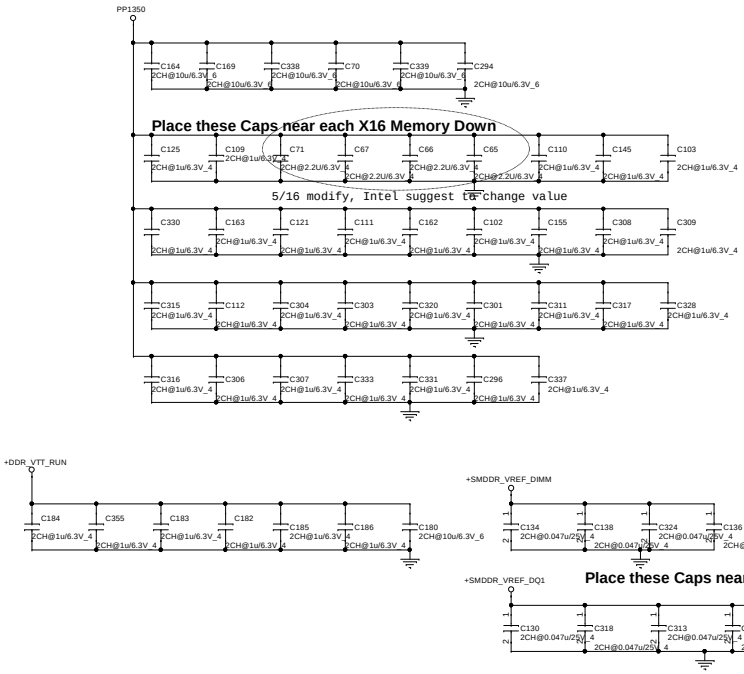
<DDR>

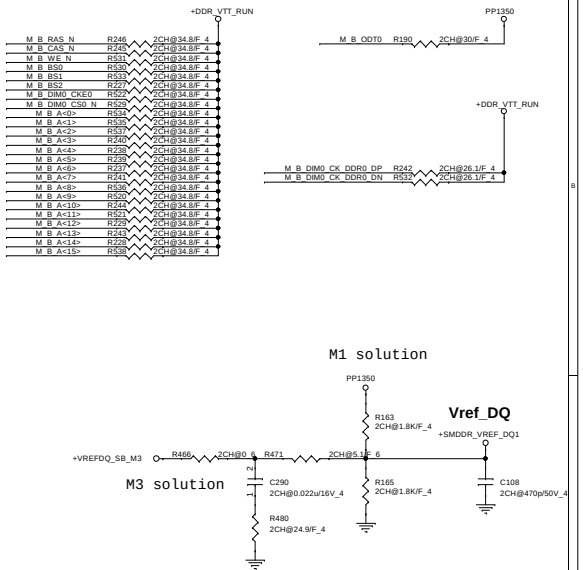
BYTE1_8-15
BYTE2_16-23
BYTE5_40-47
BYTE6_48-55
BYTE0_0-7
BYTE3_24-31
BYTE4_32-39
BYTE7_56-63



Vendor	P/N	
Hynix	AKD5JGETW04	DDR3L 1600Mhz 4Gb
Elpida	AKD5JGST407	DDR3L 1600Mhz 4Gb
Micron	AKD5JGSTL10	DDR3L 1600Mhz 4Gb

Micron/MT41K256M16HA-125:E/AKD5JGSTL02 for proto board





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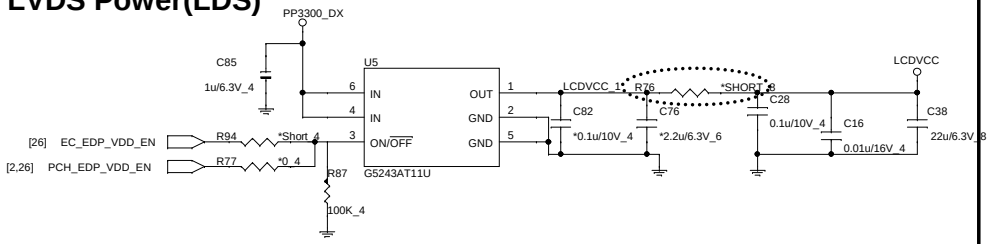
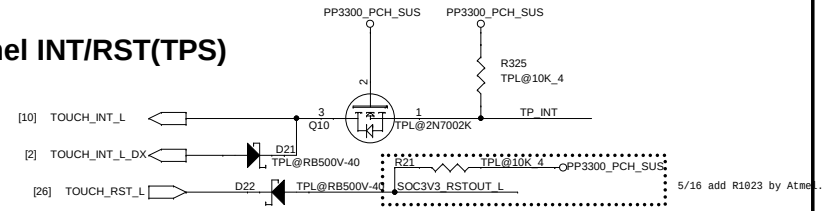
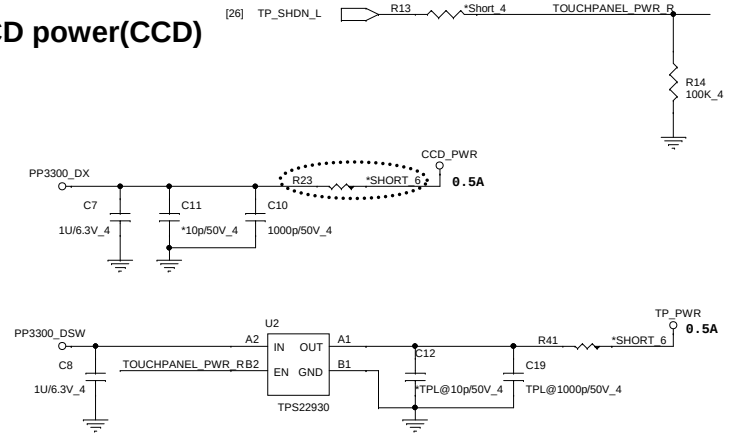
LVDS Power(LDS)



Touch Panel INT/RST(TPS)

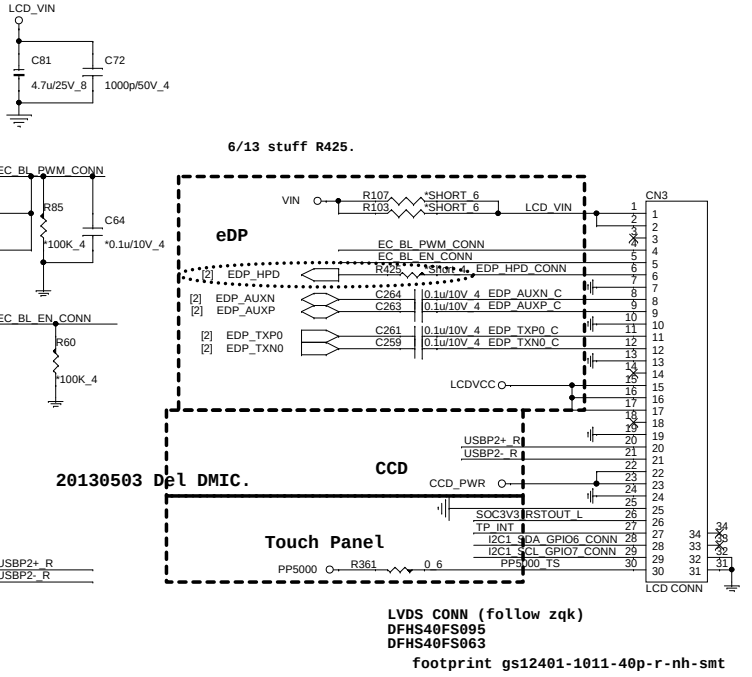


CCD power(CCD)



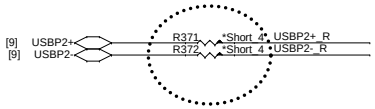
5/17 change U4 solution by ACER

LVDS(LDS)



20130503 Del DMIC.

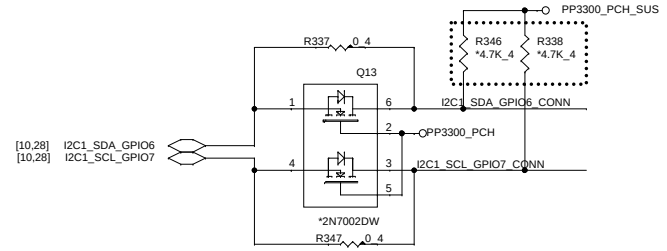
CCD(CCD)



7/26 Del L12 by SMT.

LVDS CONN (follow zqk)
DFHS40FS095
DFHS40FS063
footprint gs12401-1011-40p-r-nh-smt

Touch Panel level shift(TPS)



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Quanta Computer Inc.
PROJECT : ZHN

Size	Document Number	Rev
	LVDS/CCD/DMIC/TS	3B
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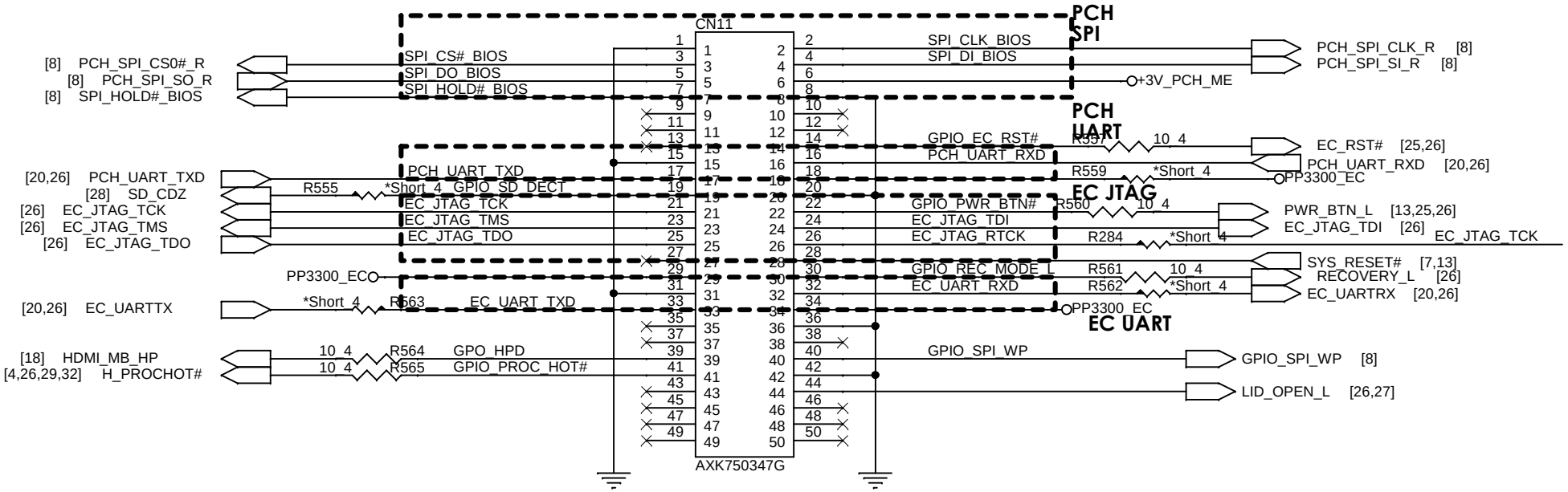
Debug Port(DBG)

PIN7 OD
PIN14 OD
PIN19 OD
PIN22 OD
PIN28 OD
PIN30 OD
PIN37 OD
PIN38 OD
PIN39 OD
PIN41 OD
PIN43 OD
PIN44 OD
PIN45 OD
PIN46 OD
PIN47 OD
PIN48 OD
PIN49 OD
PIN50 OD



Quanta Computer Inc.		
PROJECT : ZHN		
Size	Document Number: Google Debug	Rev: 3B
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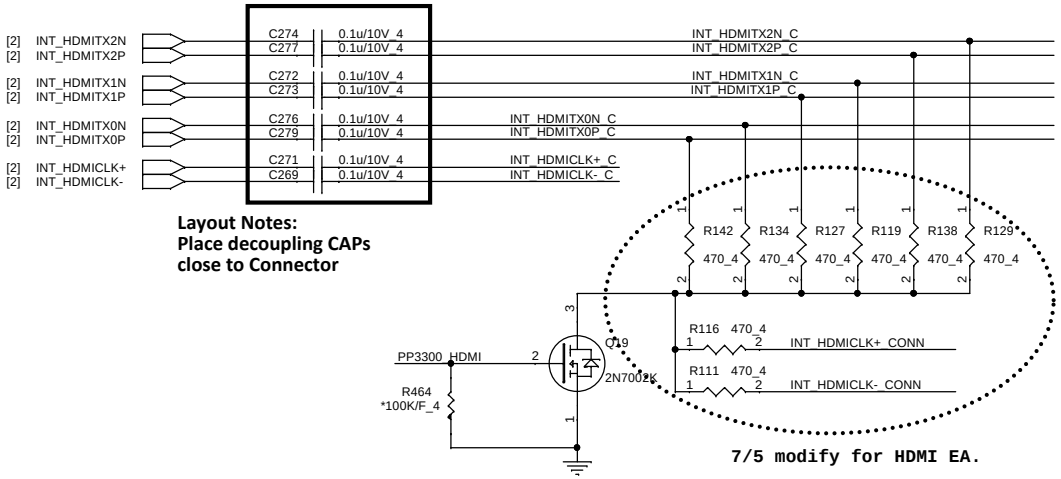
HDMI Cost Reduced level shift (HDM)



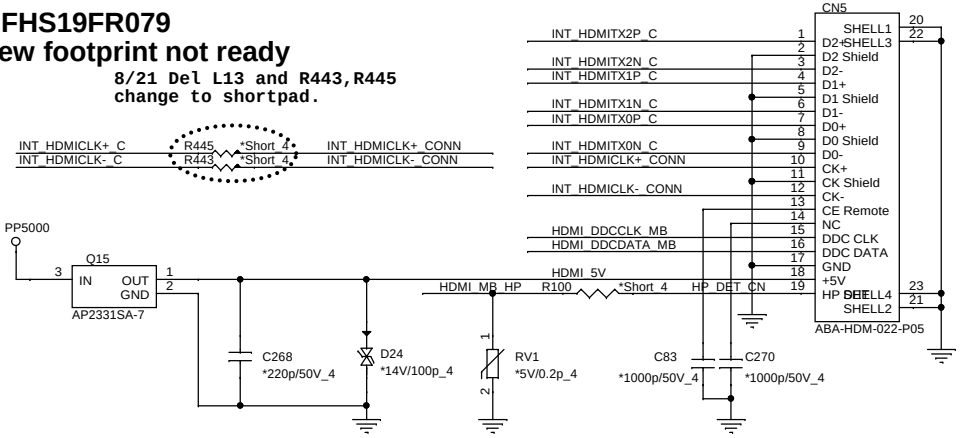
Layout Notes:
Place decoupling CAPs close to Connector

7/5 modify for HDMI EA.

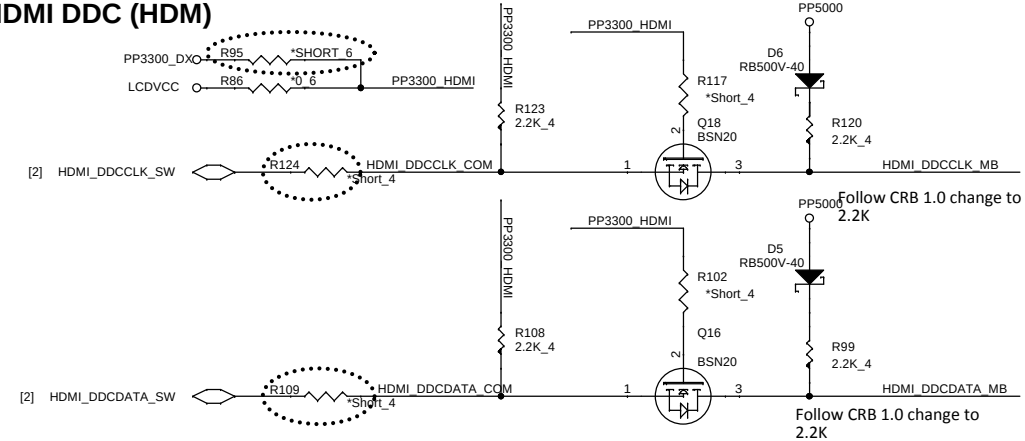
HDMI connector (HDM)

DFHS19FR079
new footprint not ready

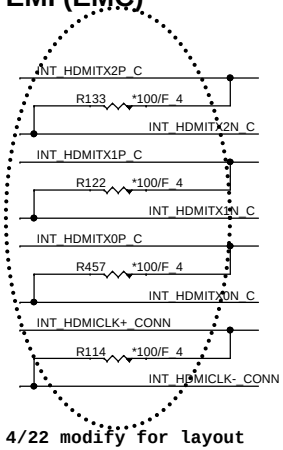
8/21 Del L13 and R443,R445 change to shortpad.



HDMI DDC (HDM)

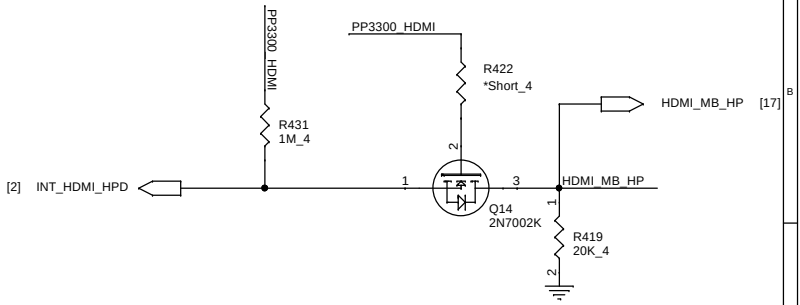


EMI (EMC)



4/22 modify for layout
7/5 unstuff by HDMI EA.

HDMI-detect (HDM)



Quanta Computer Inc.
PROJECT : ZHN

Size	Document Number	Rev
	HDMI	3B
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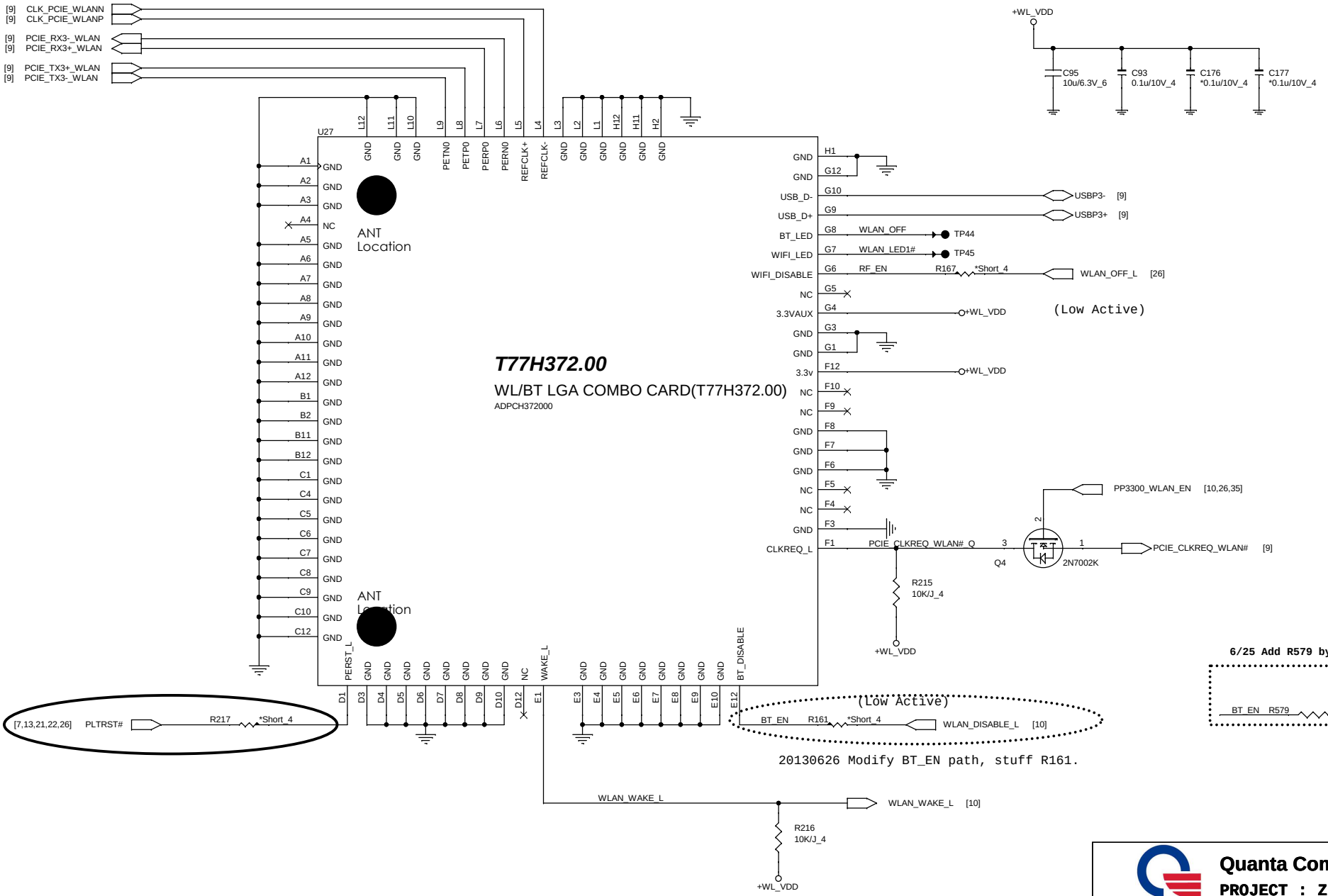

Quanta Computer Inc.		
PROJECT : ZHN		
Size	Document Number: WIFI / BT	Rev: 3B
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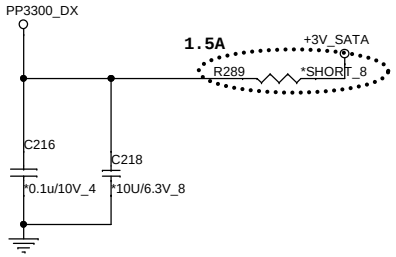
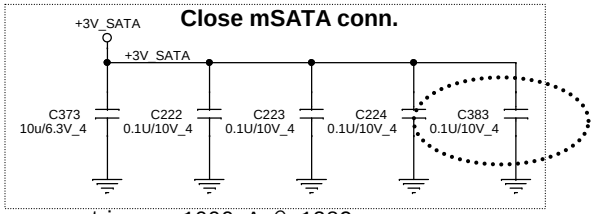
NGFF SSD connector.
San Disk SSD Card.

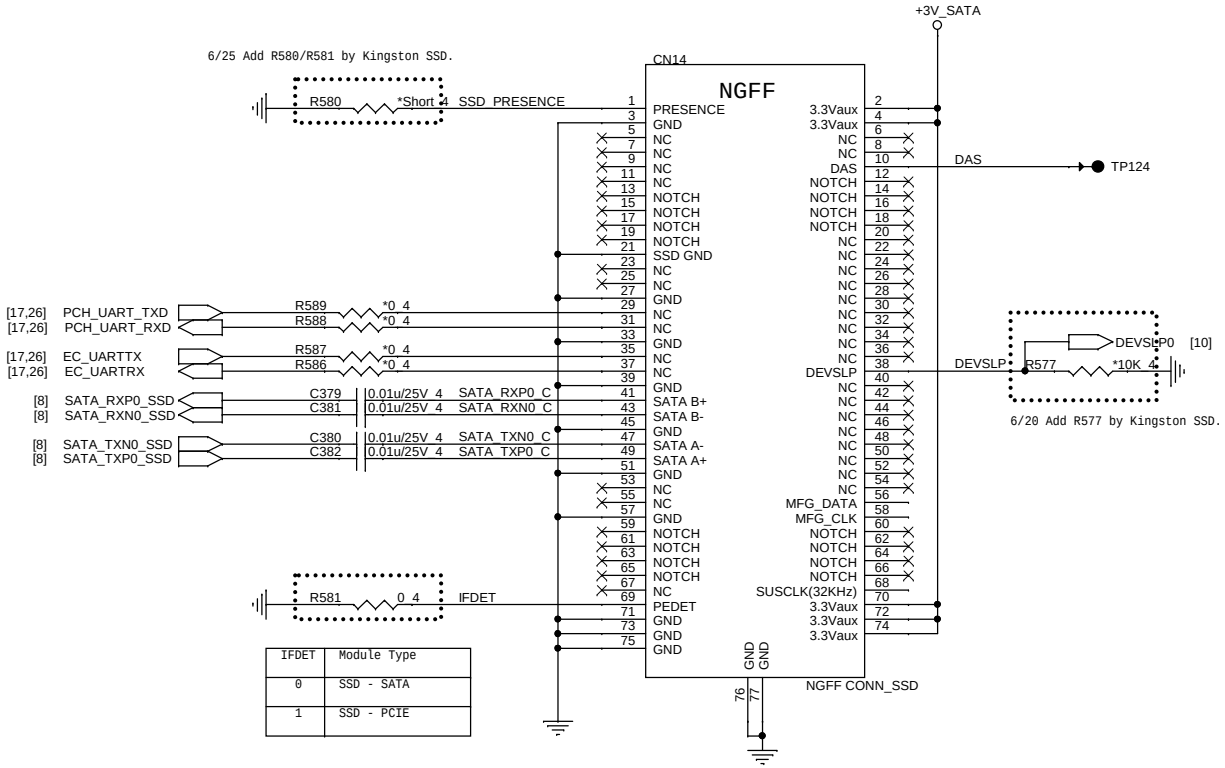




20130616 Add decouple Cap C383.

rating = 1000mA @ 128G

20130521 Page20 Change CN14 to NGFF type.



IFDET	Module Type
0	SSD - SATA
1	SSD - PCIE

Quanta Computer Inc.
PROJECT : ZHN

Size	Document Number	Rev
	NGFF SSD	3B
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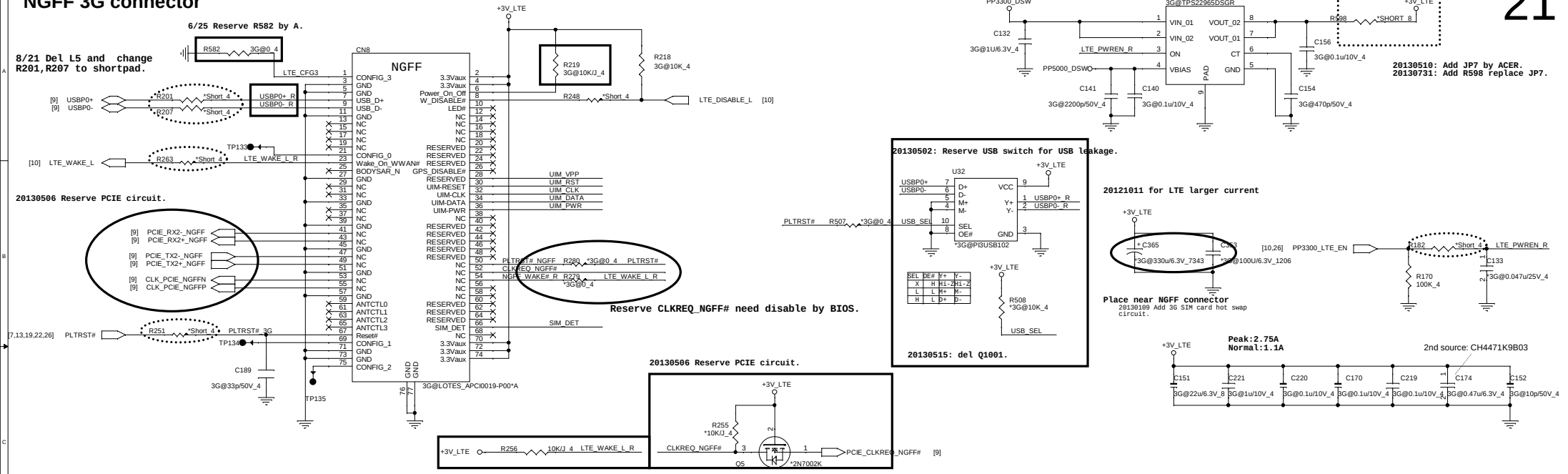
NGFF 3G connector



8/21 Del L5 and change R201,R207 to shortpad.

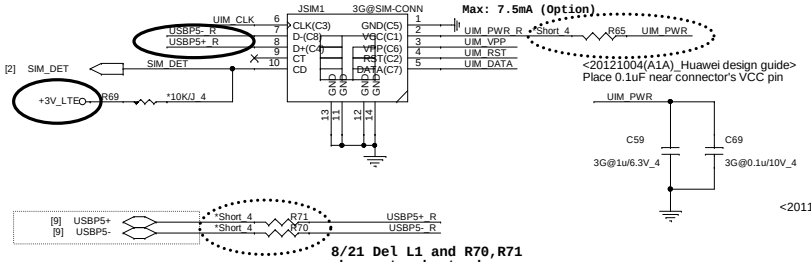
20130506 Reserve PCIE circuit.

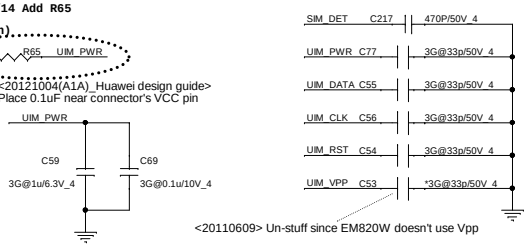
Reserve CLKREQ_NGFF# need disable by BIOS.

MultiMedia SIM (MNC)

<Layout Notes> Keep USIM signals max length within 8000mils.

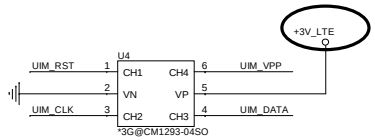
5/14 Add R65

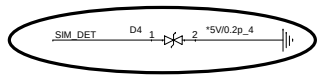




<20110609> Un-stuff since EM820W doesn't use Vpp

20130515 change.





20130513: Reserve D30 for SIM_DET.

Quanta Computer Inc.			
PROJECT : ZHN			
Size	Document Number		Rev
	NGFF/ SIM conn		3B
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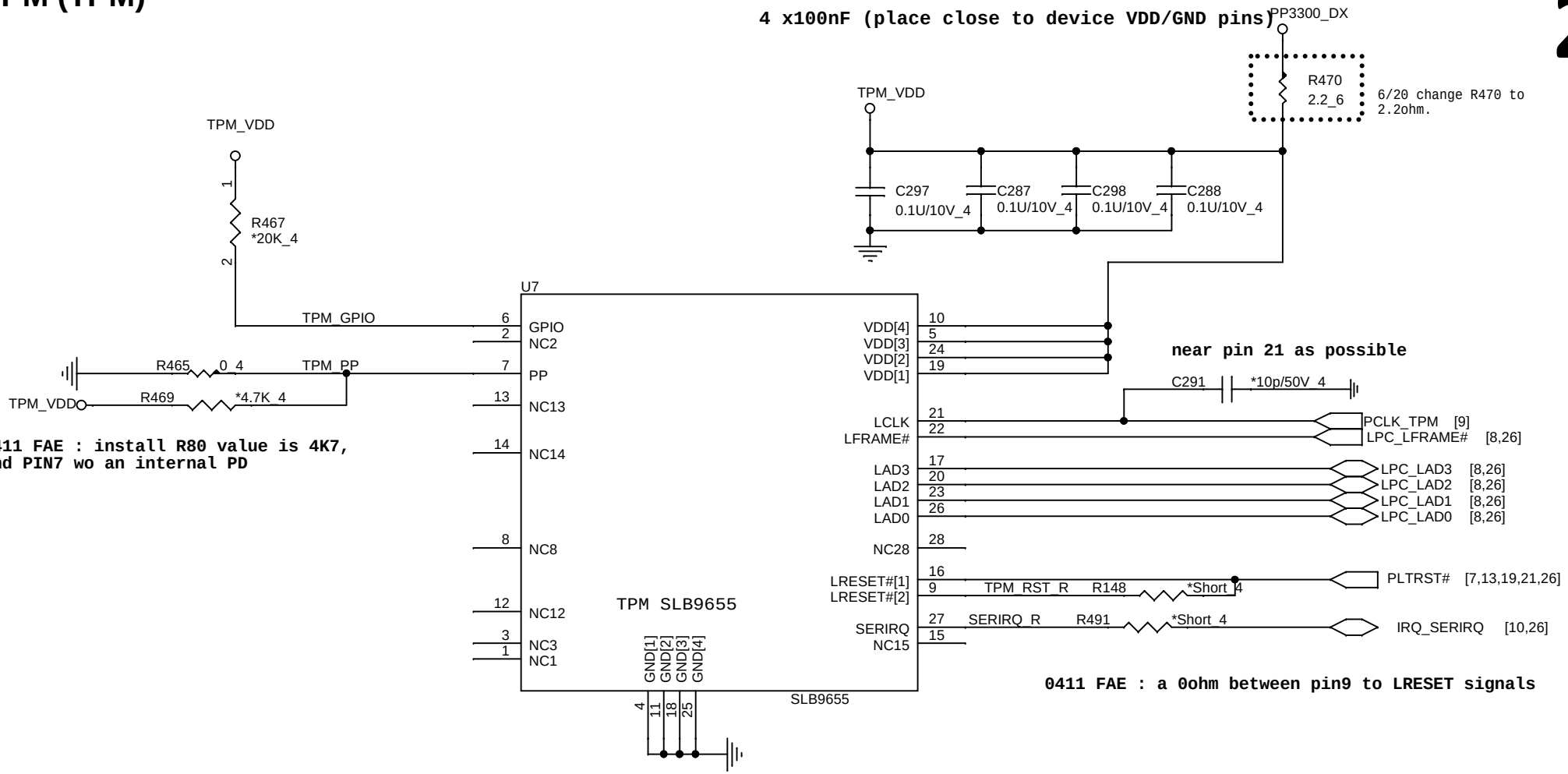
TPM (TPM)



Quanta Computer Inc.		
PROJECT : ZHN		
Size	Document Number: TPM SLB9655 / LED	Rev: 3B
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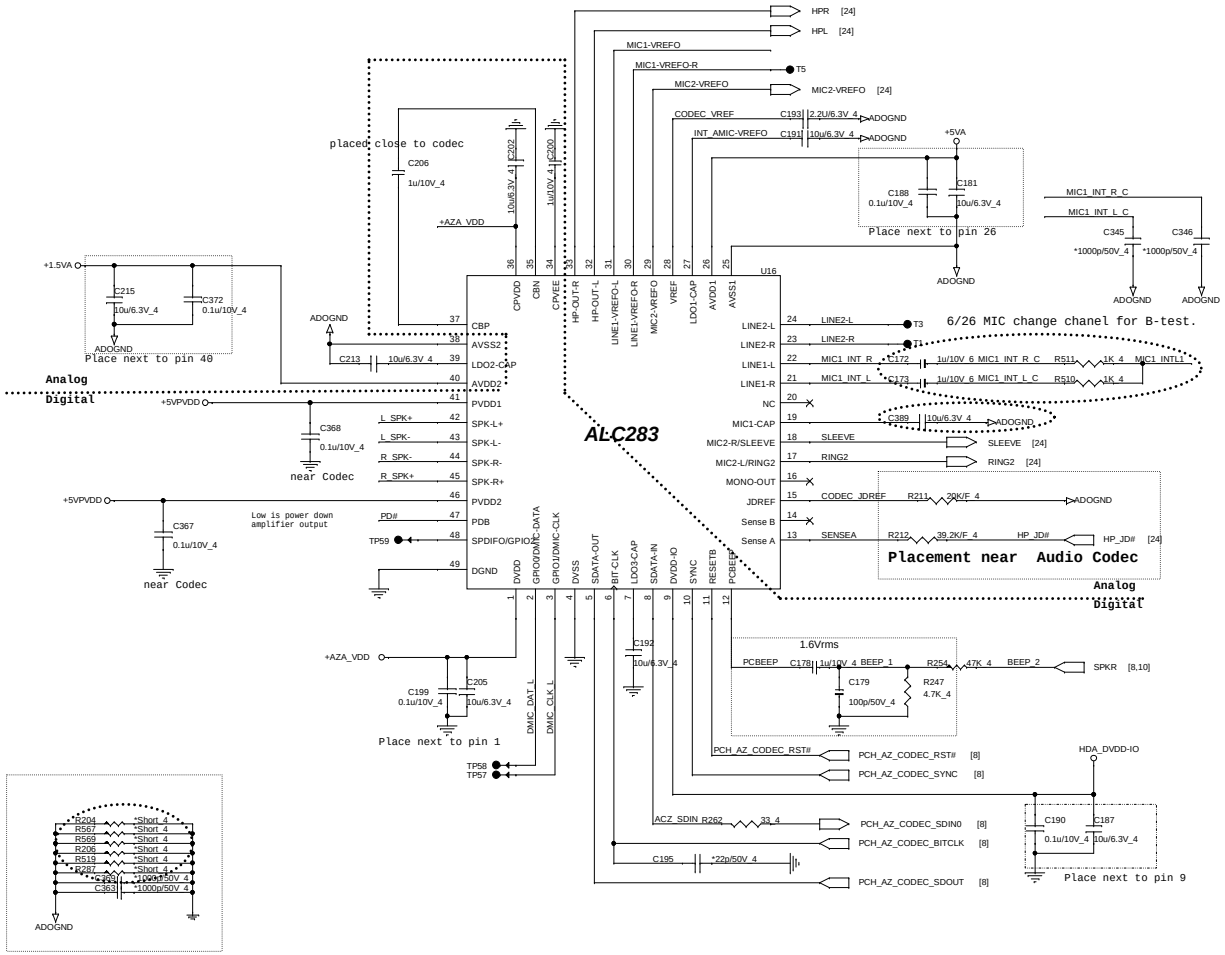
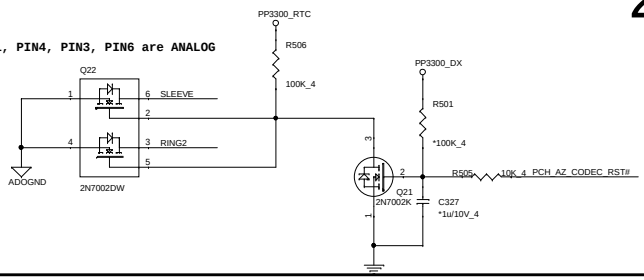
Codec(ADO)

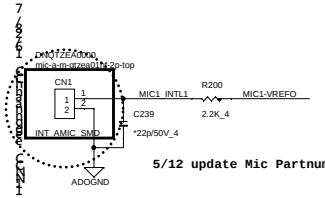


Grounding circuit(ADO)

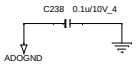
PIN1, PIN4, PIN3, PIN6 are ANALOG



INT MIC array



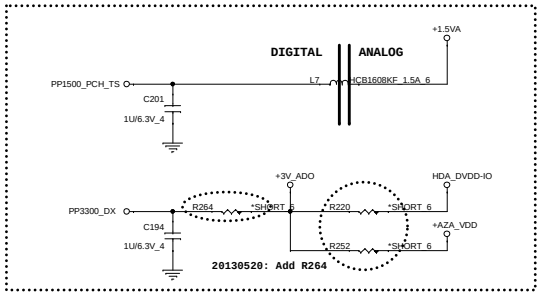
5/12 update Mic Partnumber & Footprint



cap place close to MIC-connector

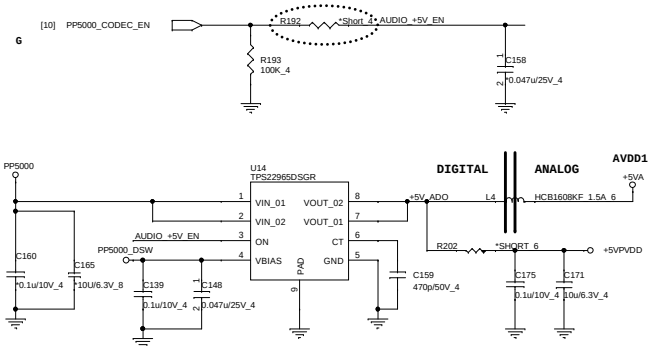
20130517 U13 remove, power source pass through to output.

Codec PWR 3V/1.5V(ADO)

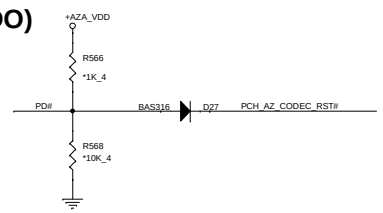


Codec PWR 5V(ADO)

5/31 RevB Del R195, C161.



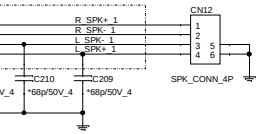
Mute(ADO)



Internal Speaker

footprint 88266-040xx-xxx-4p-l

40mil for each signal



20130515 swap pin by ME.

Quanta Computer Inc.		
PROJECT : ZHN		
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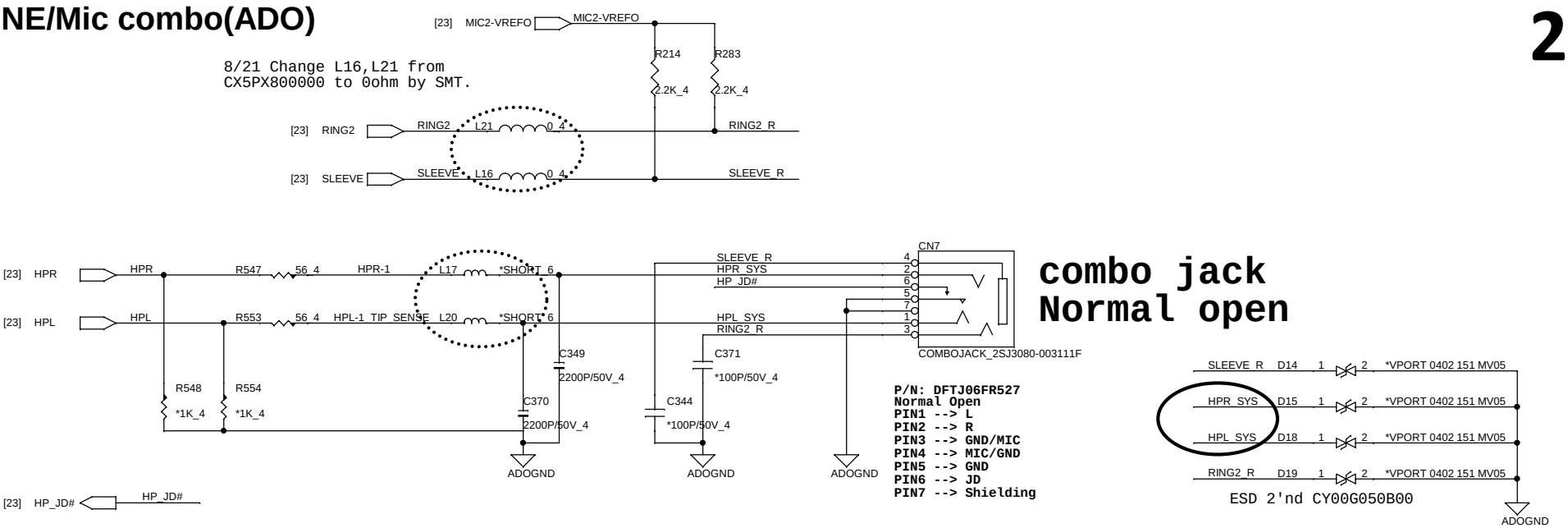
HEADPHONE/Mic combo(ADO)

8/21 Change L16,L21 from
CX5PX800000 to 0ohm by SMT.



combo jack
Normal open

P/N: DFTJ06FR527
Normal Open
PIN1 --> L
PIN2 --> R
PIN3 --> GND/MIC
PIN4 --> MIC/GND
PIN5 --> GND
PIN6 --> JD
PIN7 --> Shielding

ESD 2'nd CY00G050B00

Quanta Computer Inc.
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	Audio Headset SW	3B
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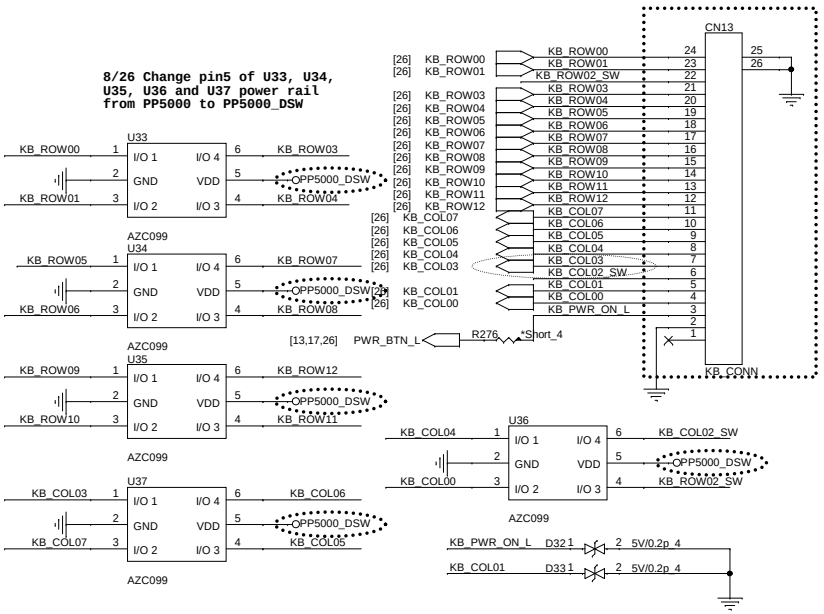
K/B (KBC)

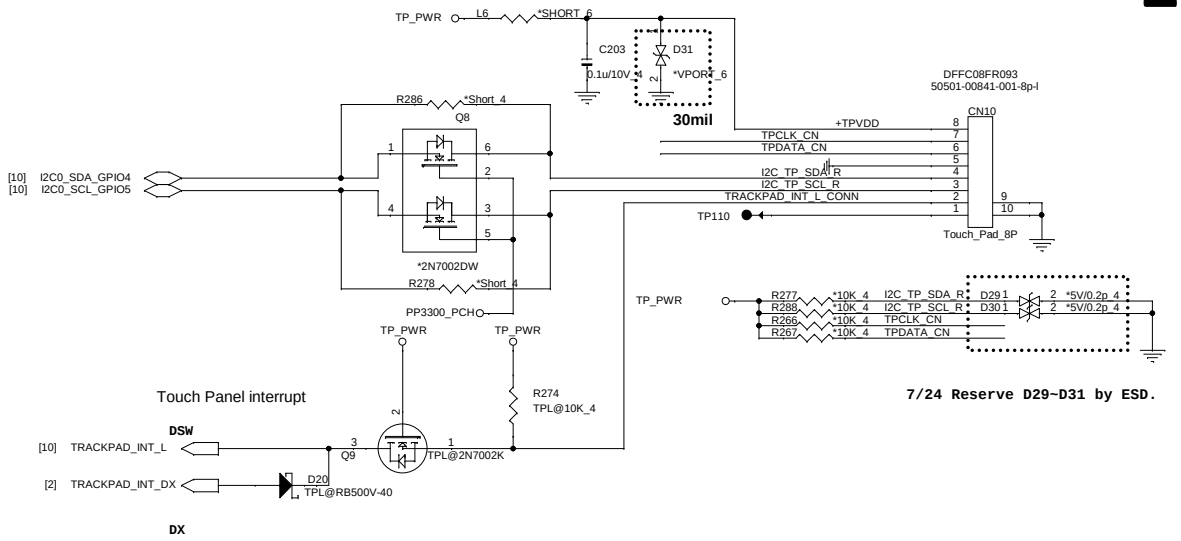
8/22 DFFC24FR098
footprint 88502-2401-24P-L-SMT

8/26 Change pin5 of U33, U34, U35, U36 and U37 power rail from PP5000 to PP5000_DSW



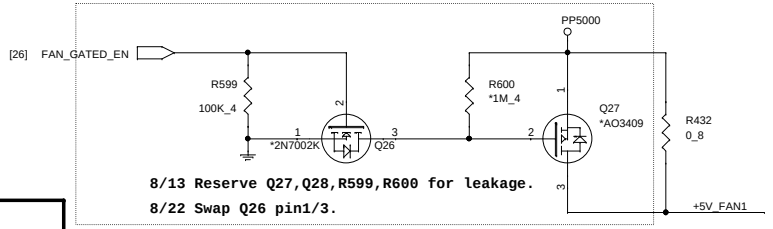
8/22 Swap Q26 pin1/3.

TOUCHPAD BOARD CONN (TPD)



7/24 Reserve D29~D31 by ESD.

8/13 Reserve Q27,Q28,R599,R600 for leakage.
8/22 Swap Q26 pin1/3.

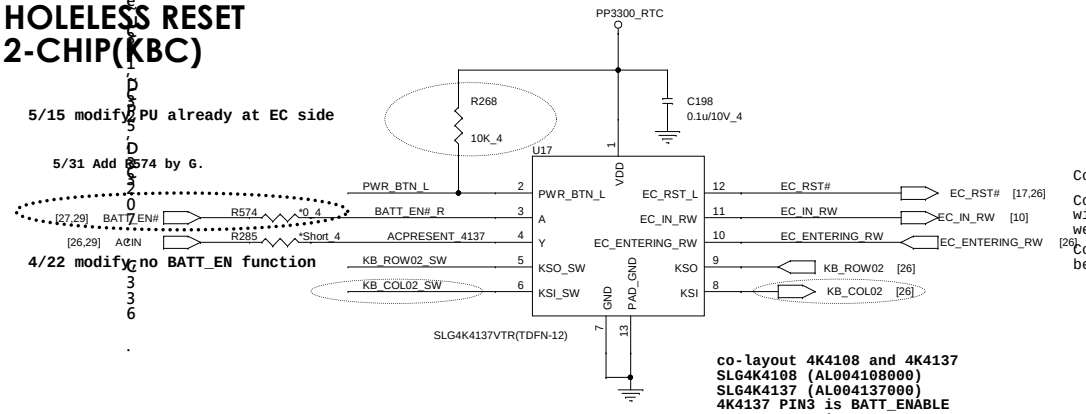


HOLELESS RESET 2-CHIP(KBC)

5/15 modify PU already at EC side

5/31 Add R574 by G.

4/22 modify no BATT_EN function



Connect to EC reset pin

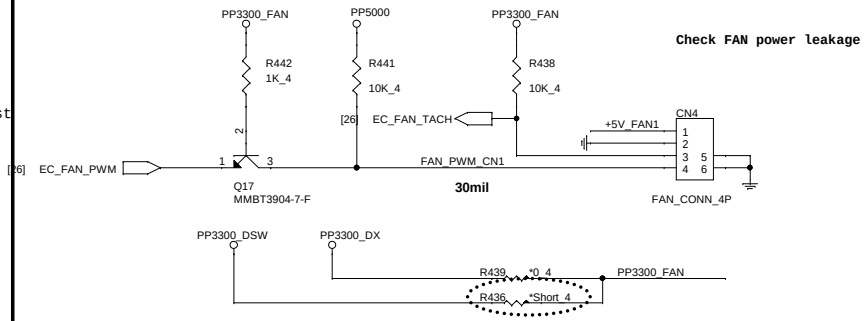
Connect to GPIO on CPU with PU to GPIO power well

Connect to EC pin C5 (must be low when EC IN RESET)

co-layout 4K4108 and 4K4137
SLG4K4108 (AL004108000)
SLG4K4137 (AL004137000)
4K4137 PIN3 is BATT_ENABLE
4K4137 PIN4 is AC_PRESENT

CPU FAN1 (THM)

Check pin define 0321
footprint 88266-040xx-xxx-4p-l



Check FAN power leakage

Quanta Computer Inc.		
PROJECT : ZHN		
Size	Document Number: KB/TP/FAN/HW Reset	Rev: 3B
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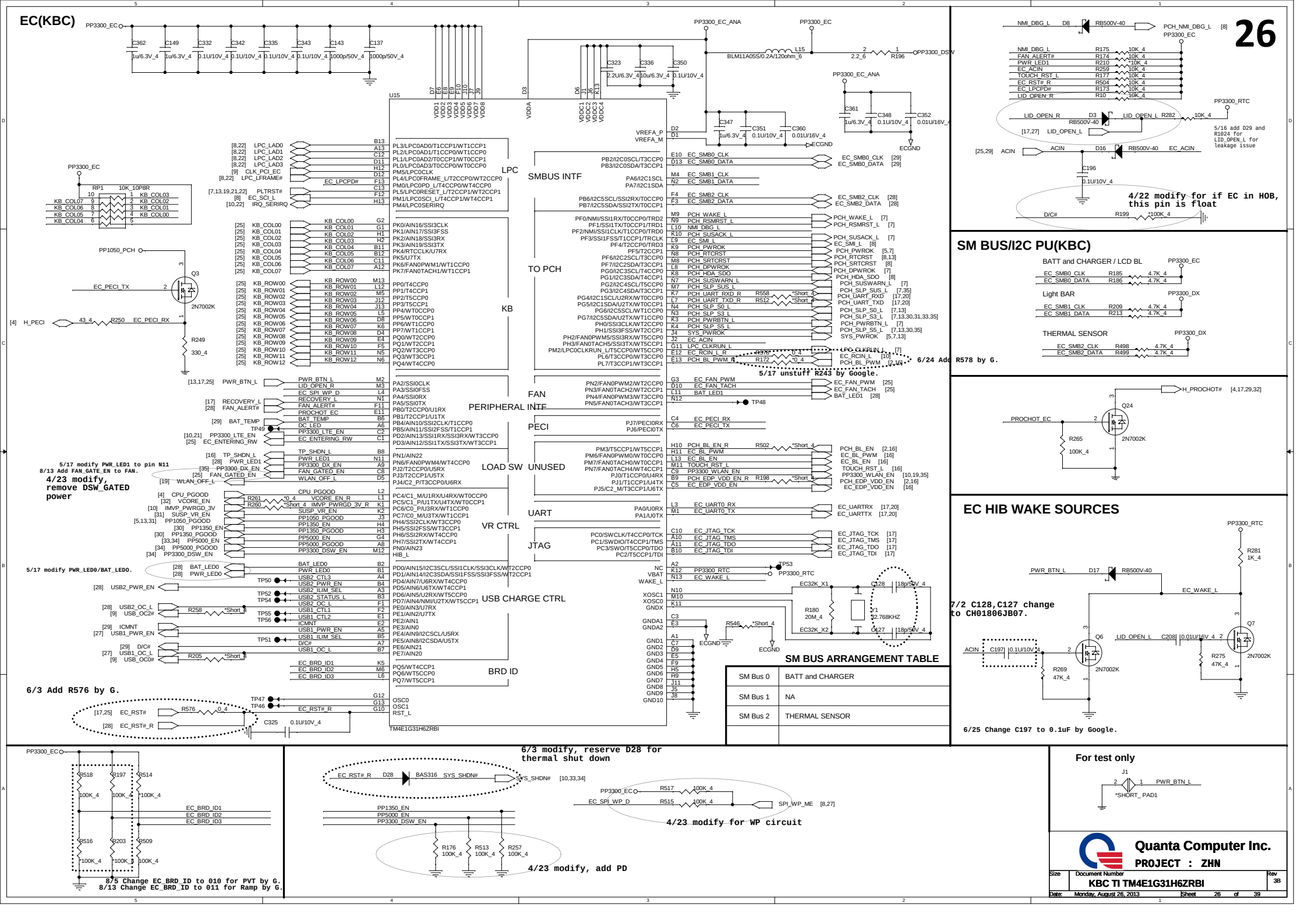
EC(KBC)



SM Bus 0	BATT and CHARGER
SM Bus 1	NA
SM Bus 2	THERMAL SENSOR

SM BUS ARRANGEMENT TABLE

SM BUS/I2C PU(KBC)

EC HIB WAKE SOURCES

Quanta Computer Inc.

PROJECT : ZHN

Size	Document Number	Rev
	KBC TI TM4E1G31H6ZRBI	3B
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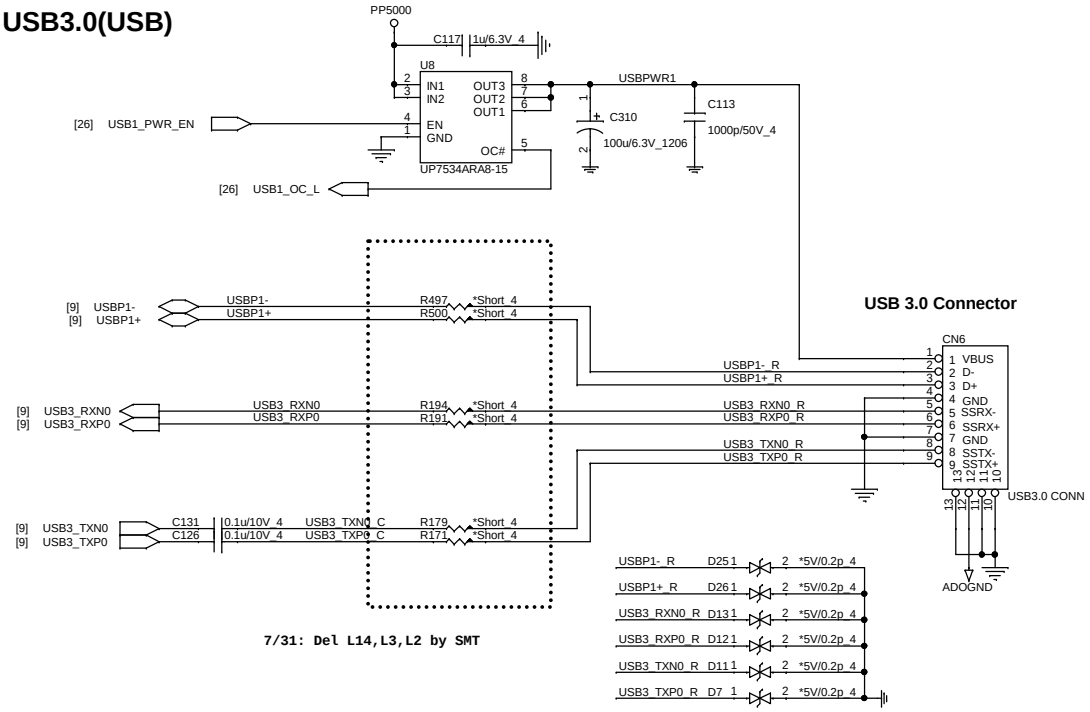
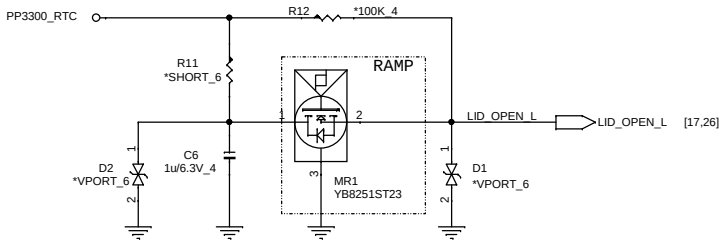
USB3.0(USB)



7/31: Del L14,L3,L2 by SMT

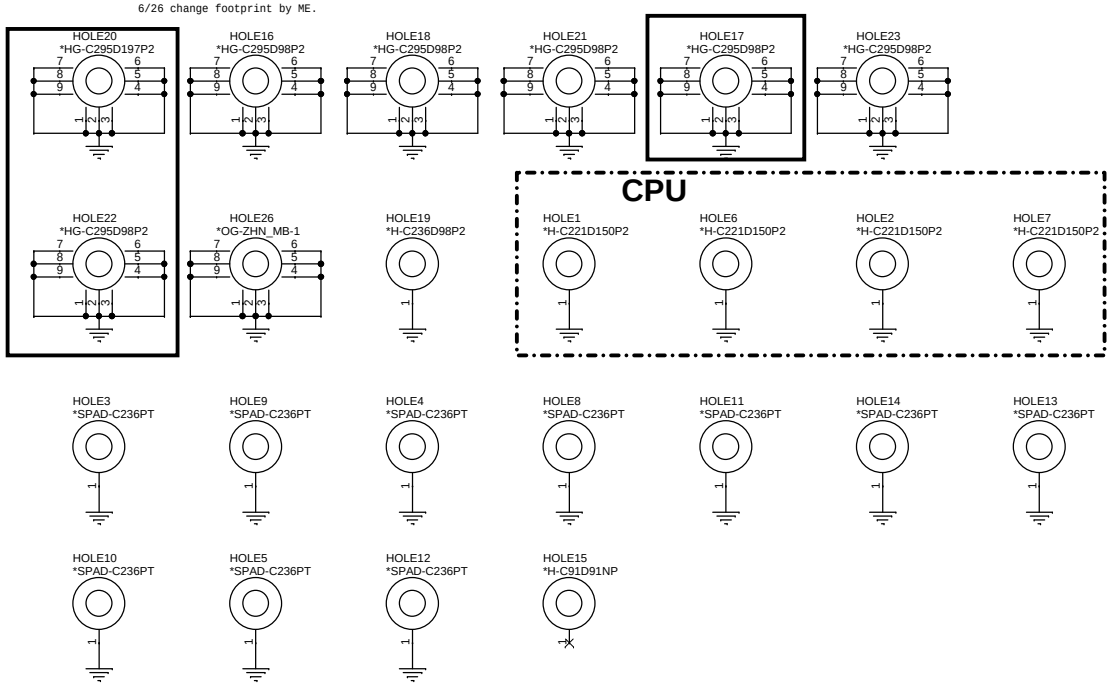
Lid Switch (HSR)



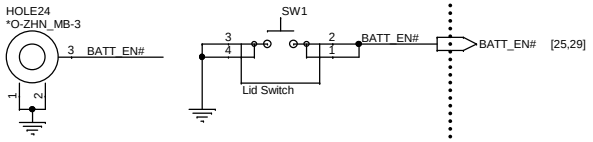
20130515 Add Hall IC by ME.

HOLE(OTH)

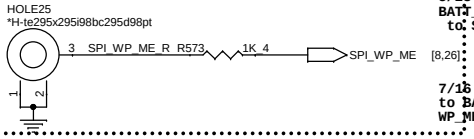
6/26 change footprint by ME.



BATT Enable short pad



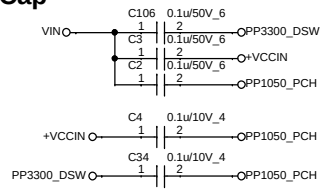
ROM WP#



5/23: Change hole24 from BATT_EN# to SPI_WP_ME, Add R573

7/16: modify Hole17; Hole24 to BATT_EN#; Hole25 to SPI WP_ME

EMI Cap



20130520: Add C6417, C6418,C6419,C6420,C6421

Quanta Computer Inc.

PROJECT : ZHN

Size	Document Number	Rev
	USB3/Hole	3B
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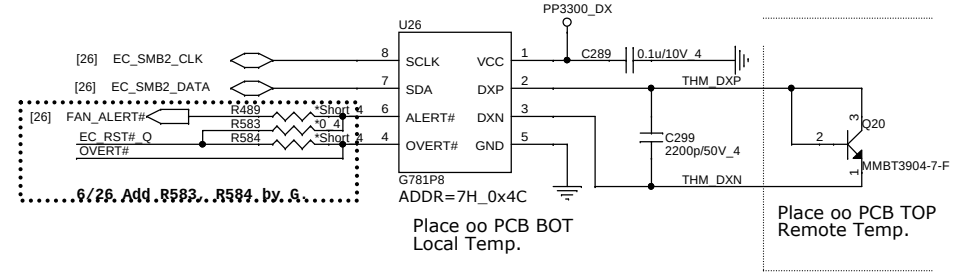
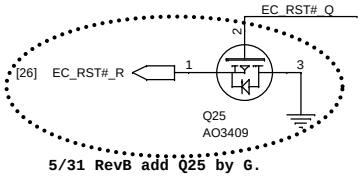
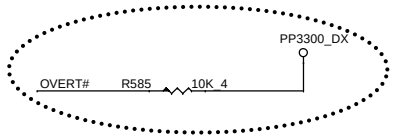
Thermal Sensor(THM)





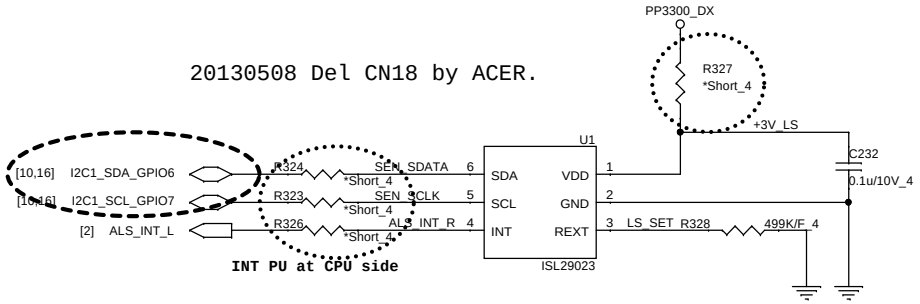
5/31 RevB add Q25 by G.



5/31 Add R585 to pull up.

Light sensor & TP (SER)

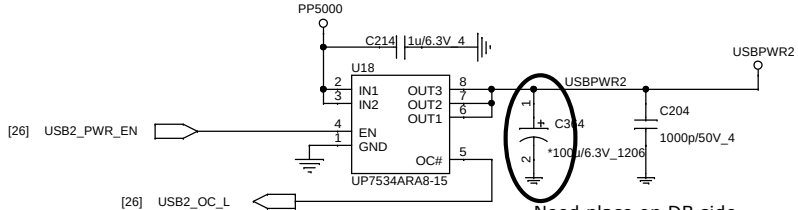
20130508 Del CN18 by ACER.

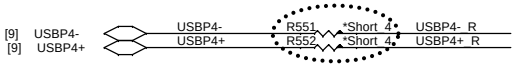


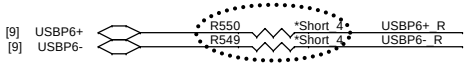
INT PU at CPU side

ADDR: 1000100

FUNCTION DB



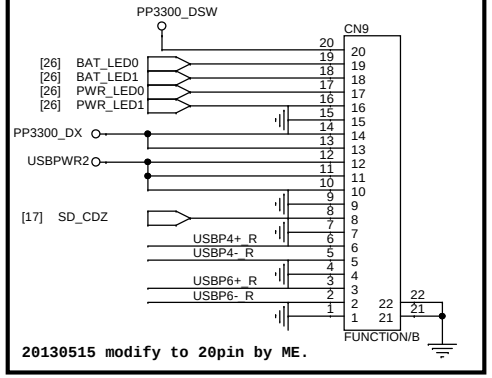




7/31 Del L18,L19 by SMT.

HSR	+3VPCU
	LID_OPEN_L
	GND
LED	+3VPCU
	LED x 4
	GND
USB	+3V x 2
	GND x 2
	USBP0+
	USBP0-
CR	CR_DET
	+3V x 2
	USBP6+
	USBP6-
	GND x 2

footprint 88511-2001-20p-l
DFFC20FR043

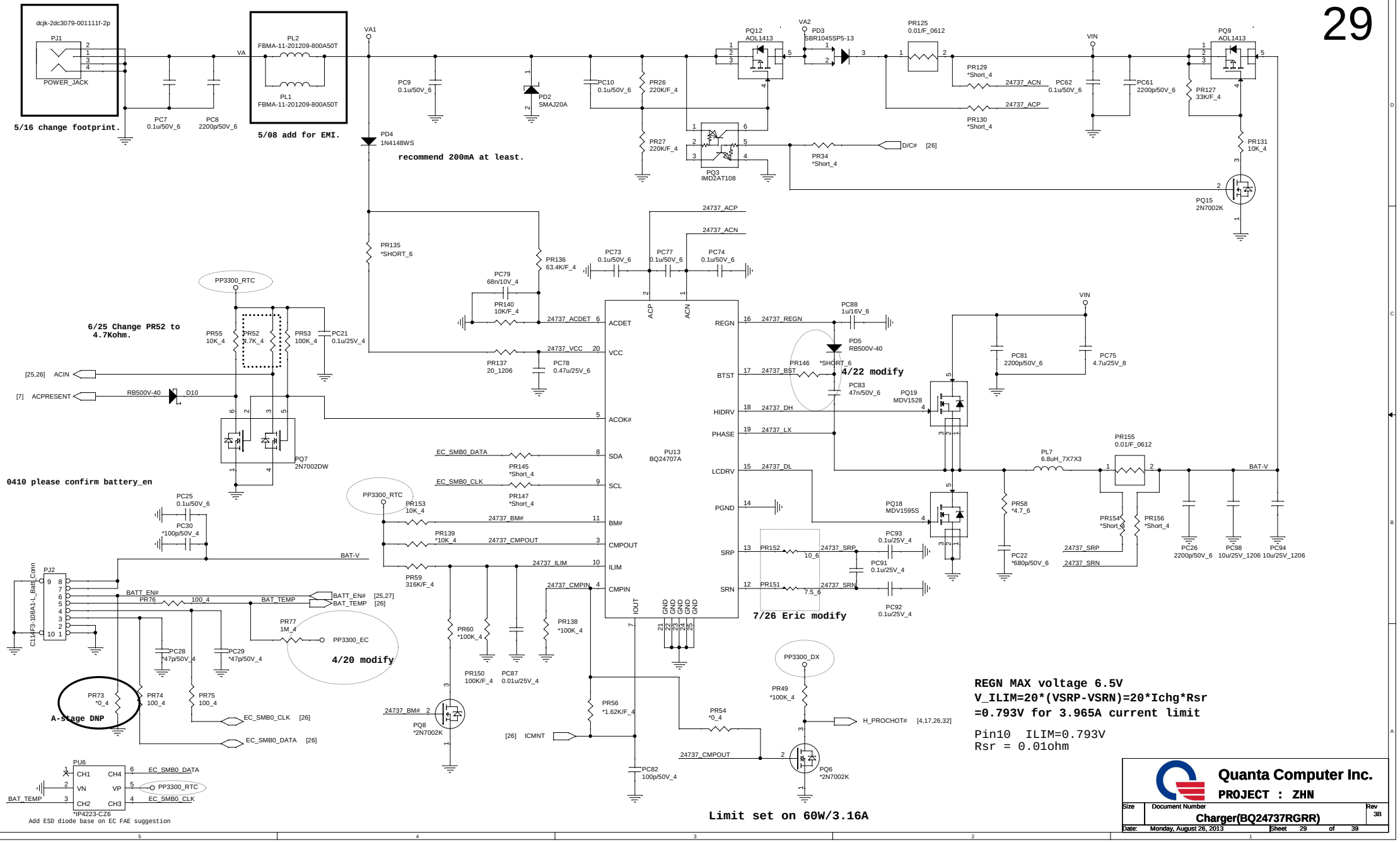


20130515 modify to 20pin by ME.

Quanta Computer Inc.

PROJECT : ZHN

Size	Document Number	Rev
	DB/ALS/Thermal sensor	3B
Date: Monday, August 26, 2013	Sheet 28 of 39	


dcjk-2dc3079-001111f-2p
PJ1
POWER_JACK
5/16 change footprint.
PC7 0.1u/50V_6
PC8 2200p/50V_6
PL2 FBMA-11-201209-800A50T
PL1 FBMA-11-201209-800A50T
5/08 add for EMI.
VA1
PD4 1N4148WS
recommend 200mA at least.
PC9 0.1u/50V_6
PD2 SMAJ20A
PC10 0.1u/50V_6
PR26 220K/F_4
PR27 220K/F_4
PQ12 AOL1413
PQ3 IMD2AT108
VA2
PD3 SBR1045SP5-13
PR125 0.01/F_0612
PR129 *Short_4
PR130 *Short_4
24737_ACN
24737_ACP
PC62 0.1u/50V_6
PC61 2200p/50V_6
VIN
PQ9 AOL1413
PR127 33K/F_4
PR131 10K_4
PQ15 2N7002K
D/C# [26]
PR34 *Short_4
PR135 *SHORT_6
PR136 63.4K/F_4
PC79 68n/10V_4
PR140 10K/F_4
PC73 0.1u/50V_6
PC77 0.1u/50V_6
PC74 0.1u/50V_6
PP3300_RTC
6/25 Change PR52 to 4.7Kohm.
PR55 10K_4
PR52 4.7K_4
PR53 100K_4
PC21 0.1u/25V_4
[25,26] ACIN
[7] ACPRESENT
RB500V-40
D10
PQ7 2N7002DW
0410 please confirm battery_en
PC25 0.1u/50V_6
PC30 *100p/50V_4
PR137 20_1206
PC78 0.47u/25V_6
24737_ACDET
24737_VCC
ACDET
VCC
ACOK#
SDA
SCL
BM#
CMPOUT
ILIM
CMPIN
ACP
ACN
IOUT
REGN
BTST
HIDRV
PHASE
LCDRV
PGND
SRP
SRN
PU13 BQ24707A
24737_REGN
24737_BST
24737_DH
24737_LX
24737_DL
PC88 1u/16V_6
PD5 RB500V-40
PR146 *SHORT_6
4/22 modify
PC83 47n/50V_6
PQ19 MDV1528
PC81 2200p/50V_6
PC75 4.7u/25V_8
PR155 0.01/F_0612
PL7 6.8uH_7X7X3
BAT-V
PR58 *4.7_6
PC22 *680p/50V_6
PR154 *Short_4
PR156 *Short_4
PC26 2200p/50V_6
PC98 10u/25V_1206
PC94 10u/25V_1206
PQ18 MDV1595S
PC93 0.1u/25V_4
PC91 0.1u/25V_4
PC92 0.1u/25V_4
PR152 10_6
PR151 7.5_6
24737_SRP
24737_SRN
7/26 Eric modify
EC_SMB0_DATA
EC_SMB0_CLK
PR145 *Short_4
PR147 *Short_4
PR153 10K_4
PR139 *10K_4
PR59 316K/F_4
24737_BM#
24737_CMPOUT
24737_ILIM
24737_CMPIN
PR138 *100K_4
PR60 *100K_4
PR150 100K/F_4
PC87 0.01u/25V_4
PR56 *1.62K/F_4
PQ8 *2N7002K
[26] ICMNT
PR54 *0_4
PQ6 *2N7002K
PC82 100p/50V_4
PP3300_DX
PR49 *100K_4
H_PROCHOT# [4,17,26,32]
PJ2
C114F53-108A1-L_Batt Conn
BATT_EN#
BAT_TEMP
PR76 100_4
BATT_EN# [25,27]
BAT_TEMP [26]
PR77 1M_4
PP3300_EC
4/20 modify
PC28 *47p/50V_4
PC29 *47p/50V_4
PR73 *0_4
PR74 100_4
PR75 100_4
A-stage DNP
EC_SMB0_CLK [26]
EC_SMB0_DATA [26]
PU6
*IP4223-CZ6
PP3300_RTC
Add ESD diode base on EC FAE suggestion
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit
Pin10 ILIM=0.793V
Rsr = 0.01ohm
Limit set on 60W/3.16A
Quanta Computer Inc.
PROJECT : ZHN
Charger(BQ24737RGRR)
Rev 3B
Date: Monday, August 26, 2013
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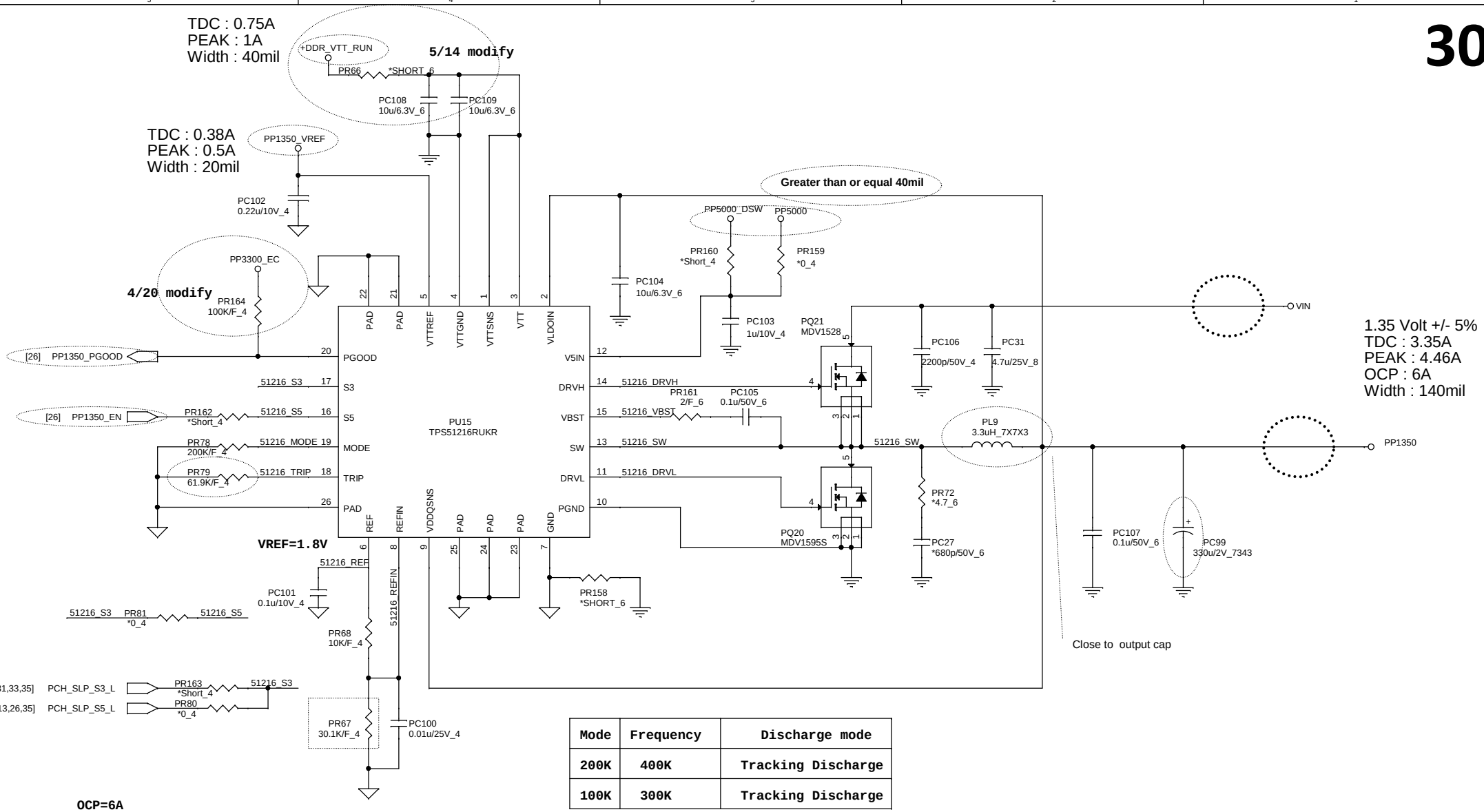

Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

OCP=6A
L ripple current
=(19-1.35)*1.35/(3.3u*400k*19)
=0.95A
Vtrip=[6-(0.95/2)]*14mohm
=0.07735V
Rlimit=0.07335/10uA*8=61.88Kohm

Quanta Computer Inc.
PROJECT : ZHN

Size	Document Number	Rev
	DDR 1.35V(TPS51216)	3B
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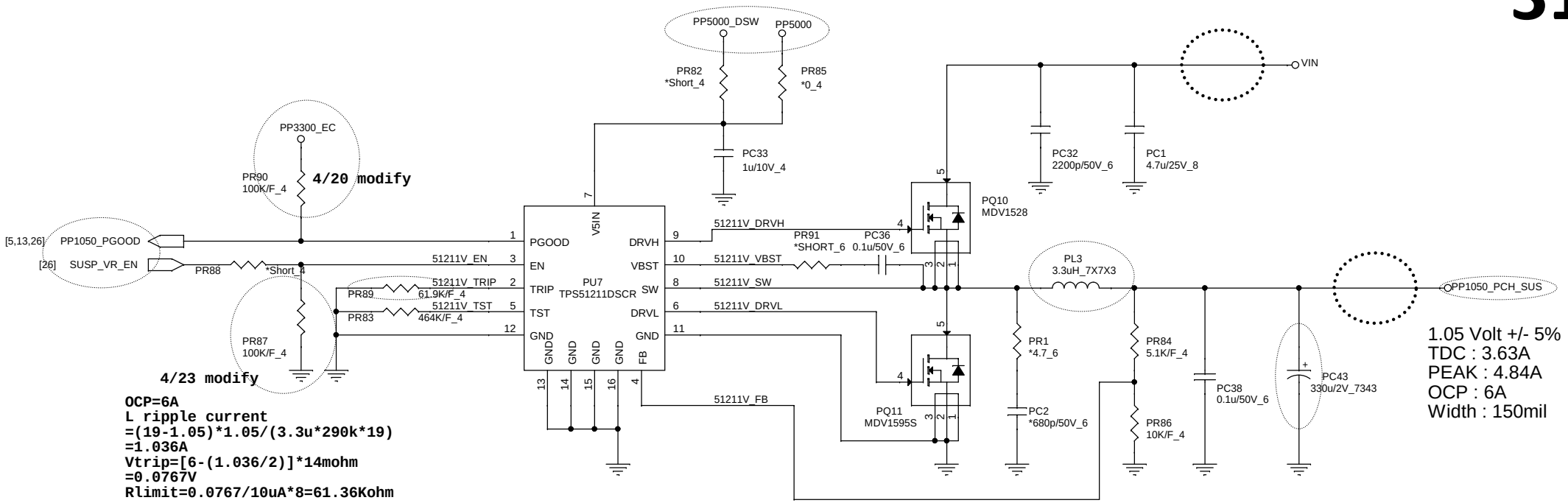
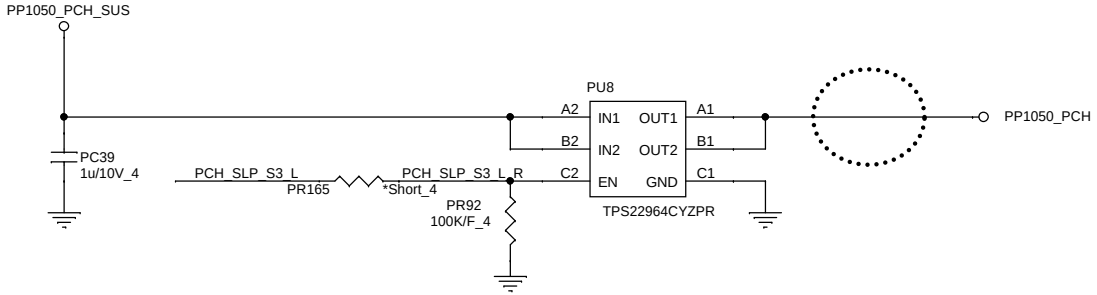
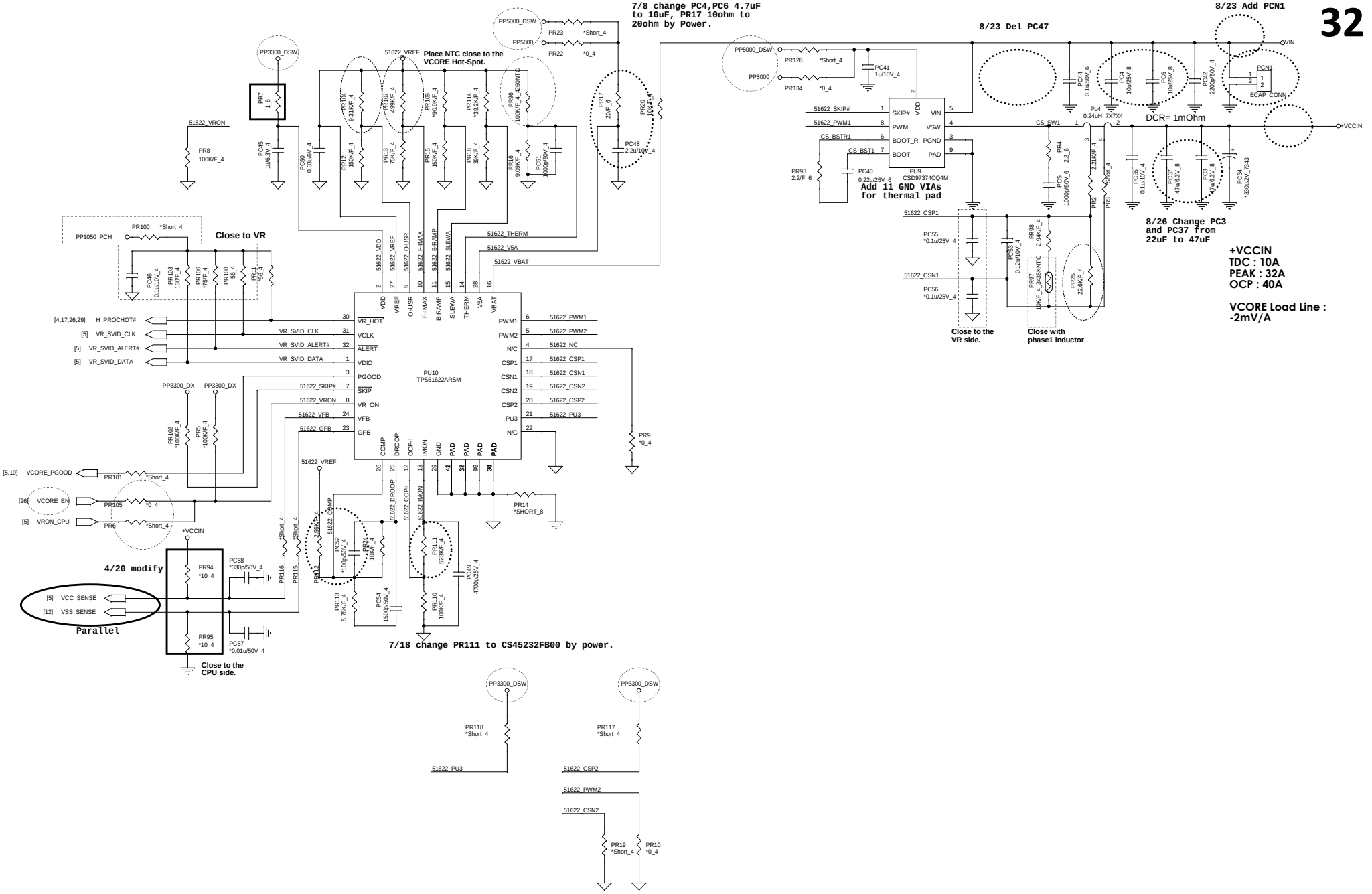


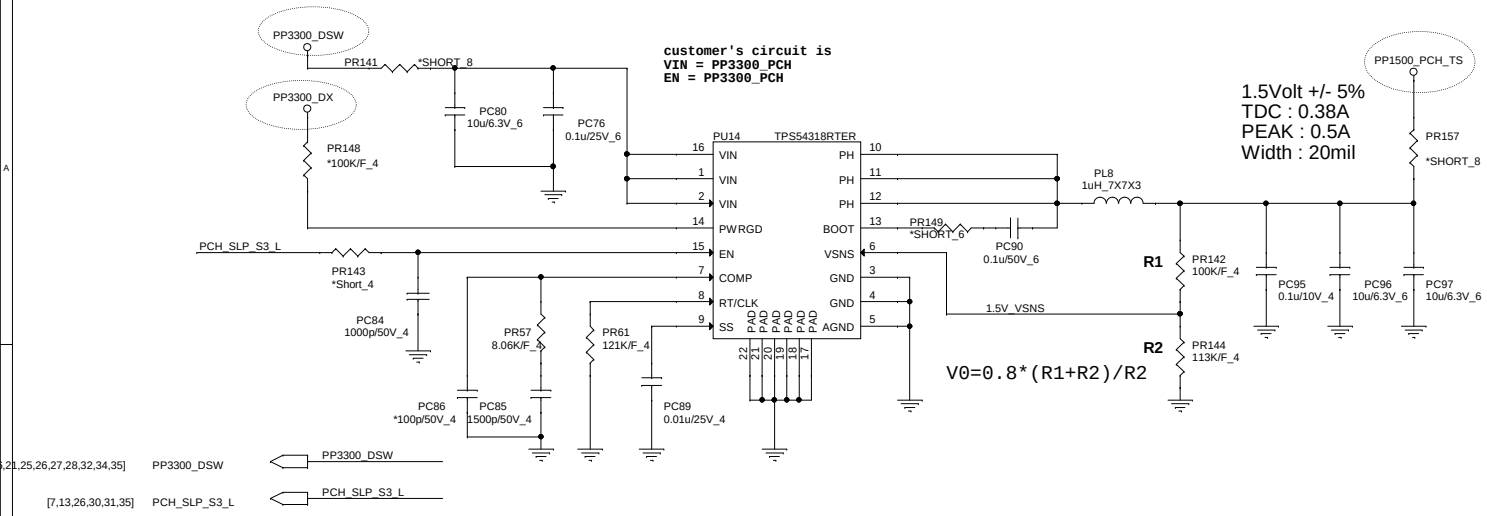
place at PQ37 area

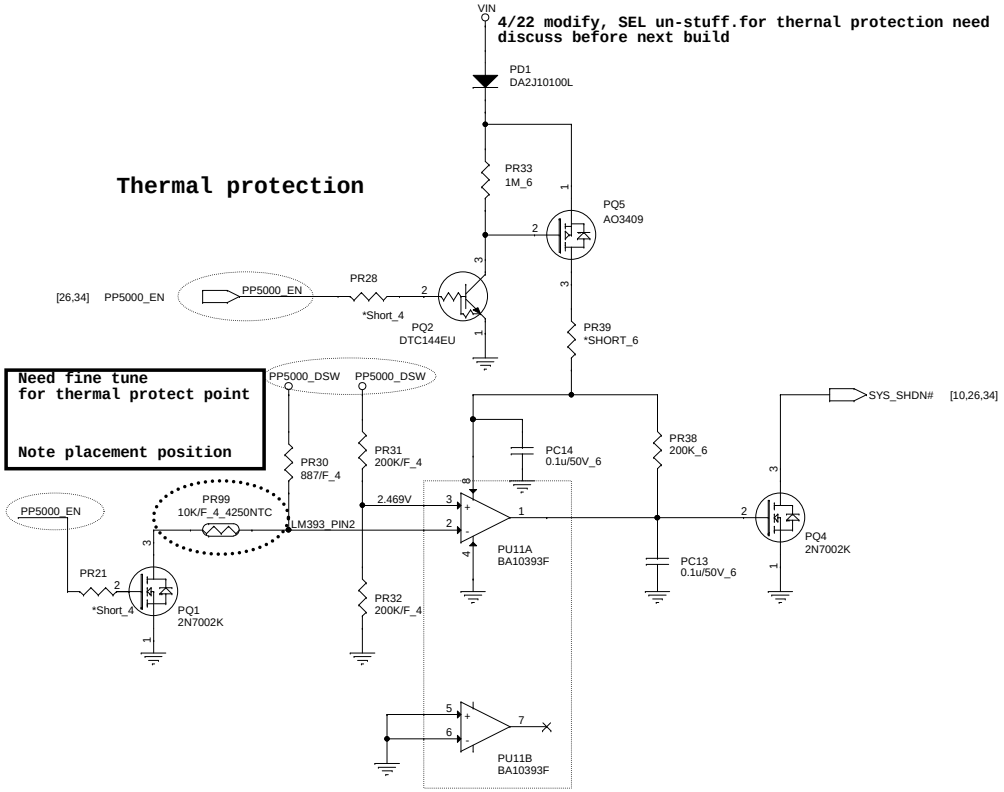


Quanta Computer Inc.		
PROJECT : ZHN		
Size	Document Number: +1.05V(TPS51211)	Rev: 3B
Date: Monday, August 26, 2013	Sheet 31 of 39	



Quanta Computer Inc.			
PROJECT : ZHN			
Size	Document Number		Rev
	+VCCIN(TPS51622)		3B
Date: Monday, August 26, 2013		Sheet 32 of 39	





For EC control thermal protection (output 3.3V)

Quanta Computer Inc.
PROJECT : ZHN

Size	Document Number	Rev
	+1.2V/+1.5V/+1.8V/Thermal protect	3B
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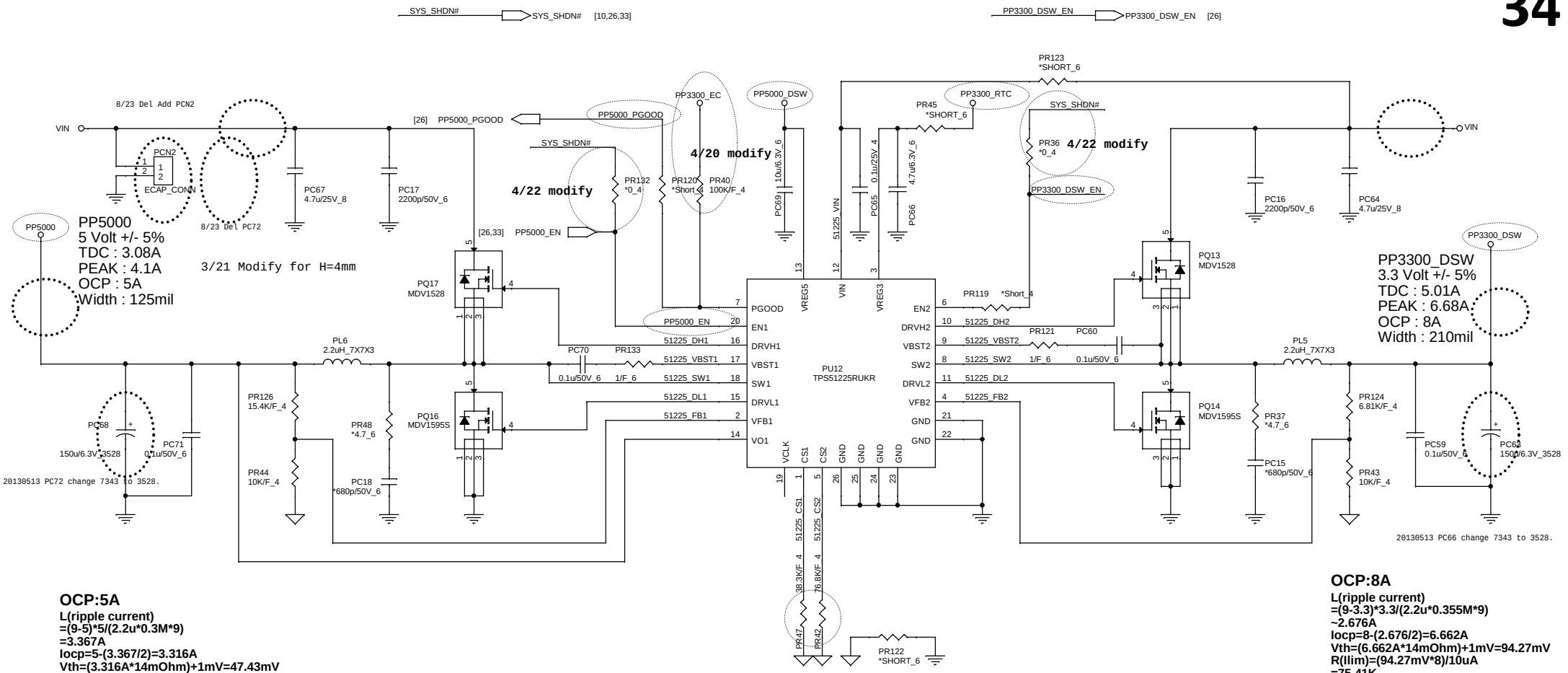
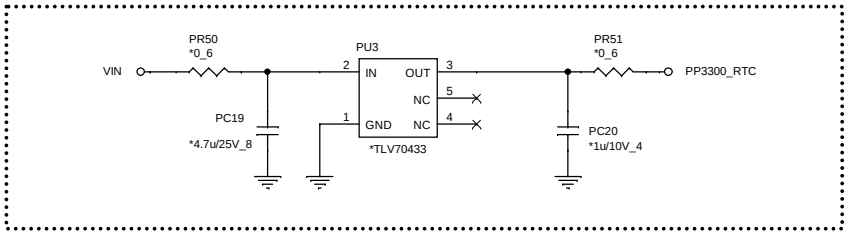


OCP:5A
L(ripple current)
=(9-5)*5/(2.2u*0.3M*9)
=3.367A
Iocp=5-(3.367/2)=3.316A
Vth=(3.316A*14mOhm)+1mV=47.43mV
R(Ilim)=(47.43mV*8)/10uA
=37.94K

OCP:8A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.355M*9)
~2.676A
Iocp=8-(2.676/2)=6.662A
Vth=(6.662A*14mOhm)+1mV=94.27mV
R(Ilim)=(94.27mV*8)/10uA
=75.41K

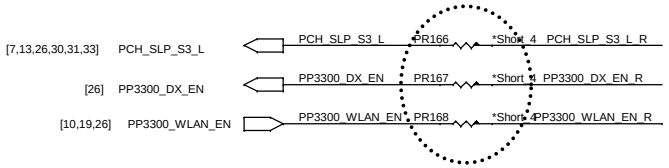
0716 unstuff PU3,PC19,PC20 by power.

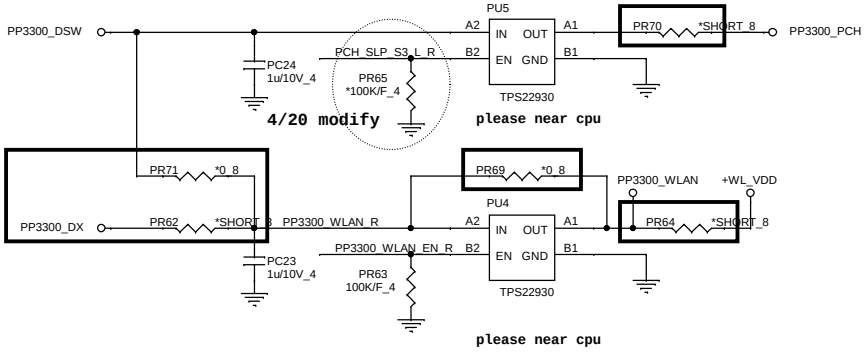


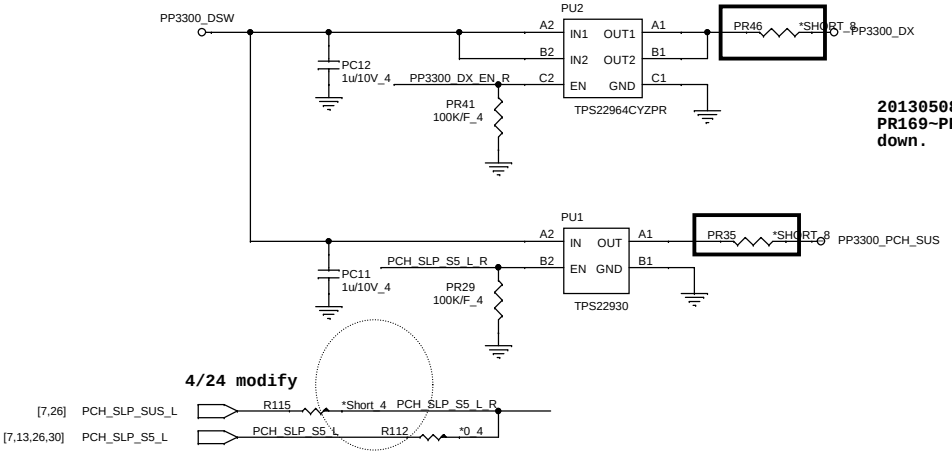
Quanta Computer Inc.
PROJECT : ZHN

Size	Document Number	Rev
	SYSTEM 5V/3V (TPS51225)	3B
Date: Monday, August 26, 2013	Sheet 34 of 39	

6/23 Add PR166~168 for debug.







20130508 Add PR169~PR172 for break down.

20130517 Page35 Add PR174 & reserve PR175,PR176 to input pwr PU4 by ACER.

Quanta Computer Inc.
PROJECT : ZHN

Size	Document Number	Rev
	Load Switch	3B
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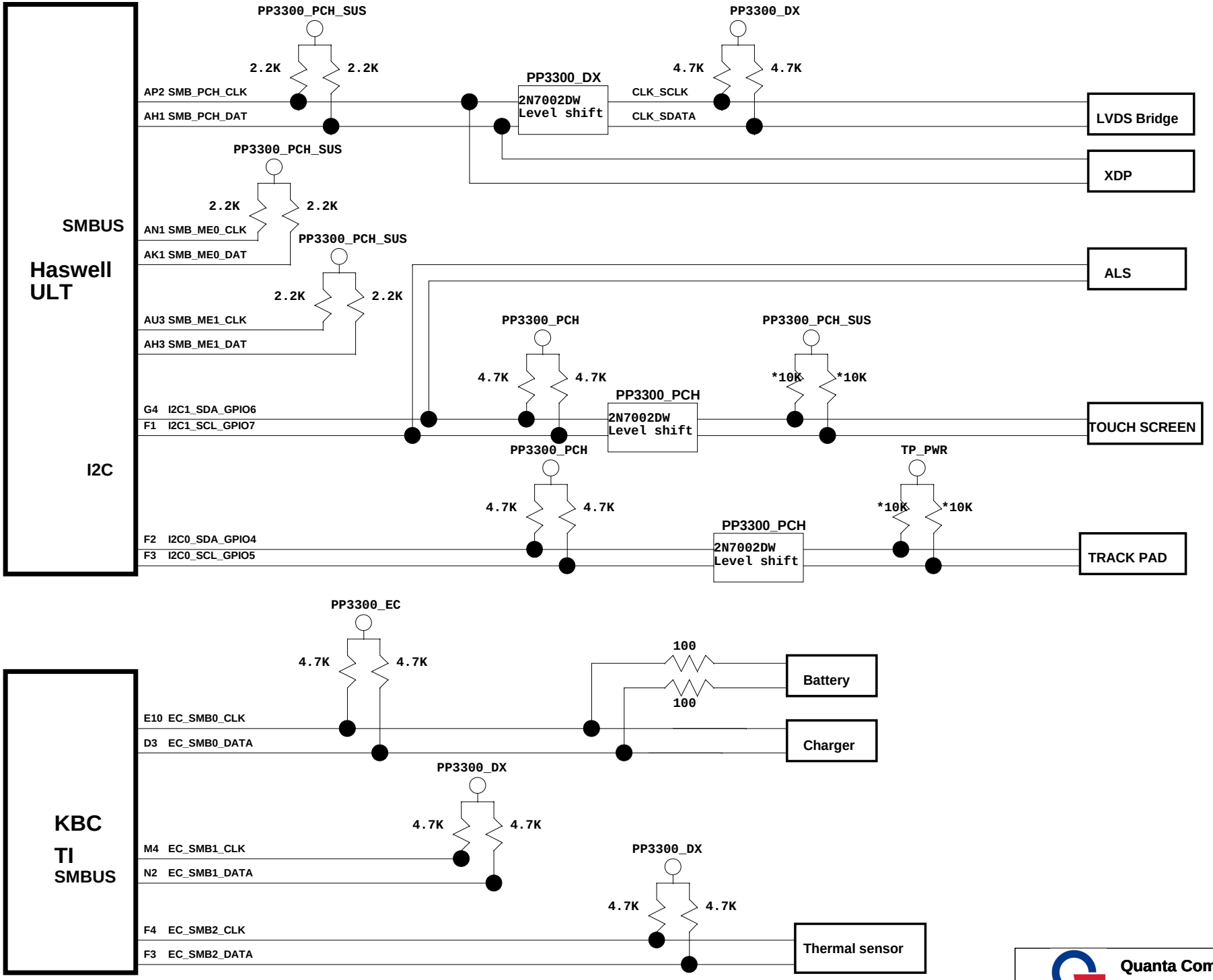
Battery Mode

Quanta Computer Inc.
PROJECT : ZHN
Size | Document Number: Power Sequence | Rev: 3B
Date: Monday, August 26, 2013 | Sheet 36 of 39



Quanta Computer Inc.
PROJECT : ZHN

Size	Document Number	Rev
	SMBUS_I2C	3B

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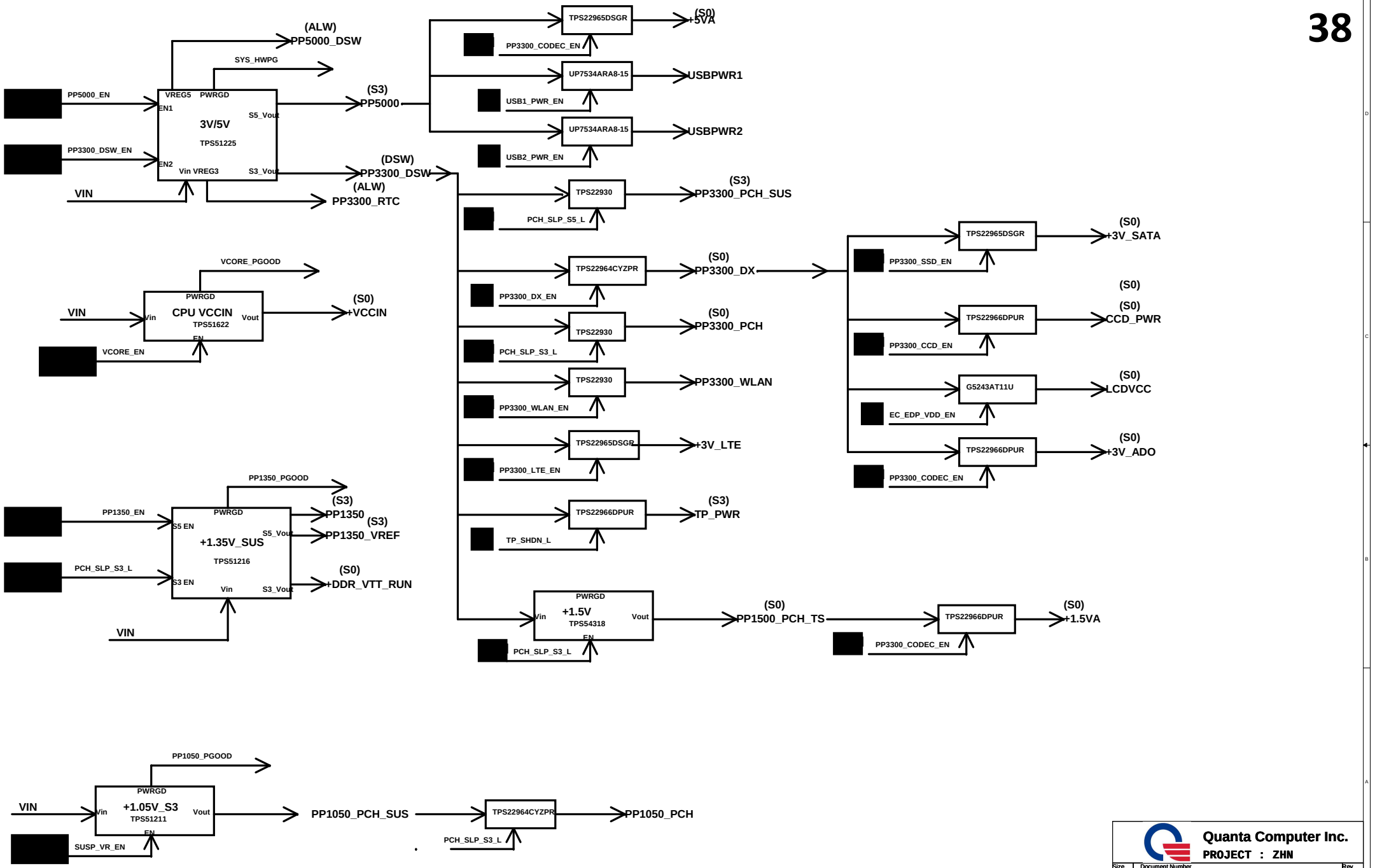

Quanta Computer Inc.
PROJECT : ZHN

Size	Document Number	Rev
	ULT PWR CONTROL	3B

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Model	Version	CHANGE LIST
Benetton	**1A**	**20130426 Page 21: Change net name USBP8+_R to USBP0+_R,USBP8-_R to USBP0-_R** **20130502 Page21: Reserve USB switch US010, Q1001,R1001 for USB leakage.** **20130502 Page33 Del +1.8V_SSD, +1.2V_SSD power circuit.** **20130502 Page13 Del CN1 for XDP debug.** **20130502 Page17 Del RSVD DP EEPROM Mode strapping R163,R162,R176,R177.** **20130503 Page16 Del DMIC circuit R421,R422,C315,C316.** **20130503 Page23/24 Del DMIC & Auto switch by Google.** **20130503 Page20 Add Cap C6410~C6413.** **20130503 Page29 Change PJ1 and PJ2 footprint.** **20130503 Page9 Add USBP5 and CLK_PCI_LPC with R1004.** **20130506 Page23 Change AMIC(CN17) footprint to mic-kecg2242sbl-2p.** **20130506 Page21 Reserve PCIE circuit & U5010 pin4,5 connect to GND & change JSIM1footprint to sim-ce01x-3-14p-smt by ME.** **20130506 Page9 Reserve PCIE circuit** **20130507 Page10 Add R1014 for PU DEVSLP0.** **20130507 Change connector footprint by ME.** **20130508 Page 29 Change connector PJ1 footprint by ME, add PL8,PL9 for EMI.** **20130508 Page28 Del CN18 by ACER.** **20130508 Page35 Add PR169~PR172 for power breakdown.** **20130509 Page19 Del R1005,R602,R604, R605 by ACER.** **20130509 Page25 change KB conn CN13 to 26pin first by ACER.** **20130510 Page27 Add Hole and SW6 for BATT_EN#.** **20130510 Page21: Add JP11 by ACER.** **20130510 Page26: Add R1015.** **20130510 Page25 change KB conn CN13 to 24pin first by ACER.** **20130510 Page31: Add JP12.** **20130511 Page34: change PC66,PC72 from 7343 to 3528.** **20130513 Page21: Reserve D30 for SIM_DET.** **20130513 Page28: Change CN2 from 20 to 24 pins for LED/B.** **20130513 Page22: Del R6,R7,LED1, move to LED/B.** **20130513 Page8,13: Reserve XDP resistor R1016~R1019.** **20130514 Page21 Add R1020.** **20130514 Page30 Add PR173.** **20130514 Page25 swap CN13 pin define.** **20130515 Page23 swap CN8 pin define by ME.** **20130515 Page27 Add Hall IC by ME.** **20130515 Page28 change CN2 from 24 to 20pin.** **20130516 Page26 add diode D29 and R1024 for LID_OPEN_L for leakage issue** **20130516 Page16 add R1023 by Atmel.** **20130517 Page25 swap CN12 pin define by ME.** **20130517 Page16 change U4 solution by ACER.** **20130517 Page20 U36 remove , mSATA power connect to PP3300_DX.** **20130517 Page23 U13 remove, power source pass through to output.** **20130517 Page35 Add PR174 & reserve PR175,PR176 to input pwr of PU4 by ACER.** **20130517 Page26 net Bat_LED1-->(pin name) L.11& PWRLED1-->N11; Battery LED0-->B2, PWRLED0-->B1** **20130517 Page25 U15 pin 5 -->ROW2, pin 6 -->COL3 (113 key)** **20130517 Page16 stuff R62,unstuff R60 & R243.** **20130520 Page23 Add R1025** **20130520 Page8 Remove +3V_RTC intersheet** **20130520 Page14 RemoveRemove +SMDDR_VREF_DQ0 intersheet** **20130520 Page15 RemoveRemove +SMDDR_VREF_DQ1 intersheet** **20130520 Page11 Remove +V3.3DX_1.5DX_1.8DX_AUDIO intersheet** **20130520 Page11 Remove +V1.05S_APLLOPI intersheet** **20130520 Page27 Add C6417,C6419,C6419,C6420,C6421** **20130520 Page27 Add Add USBPWR2 at CN2.10** **20130521 Page10 Add R1026 for PU GPIO28.** **20130521 Page11 Change C143 from 0.1uF to 1uF; C78 1uF to 0.1uF; R103 shortpad to 0ohm; C280&C284 stuff; C274&C286 47uF to 22uF .** **20130521 Page20 Change CN15 footprint to minipci-80060-1021-52p.** **20130522 Page2~12 Change U25 P/N to AJSR16YTT01.** **20130522 Page20 Change CN15 P/N to DFHS52FR161.** **20130522 Page15 modify all compenent to 2CH@value & Hynix RAM P/N for BOM.** **20130522 Rename from IS22-2000.** **20130523 Page25 stuff R268,R285 by Google.** **20130523 Page10 change R331,R332 from 4.7K to 2.2K by TS suggestion & stuff Q23.** **20130523 Page27 change Change hole24 from BATT_EN# to SPI_WP_ME, and add R573** **20130523 Page7 R74 un-stuff by I.** **20130523 Page13 R72, R300, C230, C231, U19, U22 stuff by I.** **20130523 Page4 R29 un-stuff.**
	2A	**20130531 Page28 Add Q25 to EC_RST# by G.** **20130531 Page23 Del R195, C161.** **20130531 Page10 Reserve R16 and R575 to PU PP3300_PCH_SUS.** **20130603 Page26 Add R576, reserve D28 for thermal shut down** **20130603 Page13 Add TP111~TP122 by ICT** **20130613 Page10 change R331,R332 to 4.7K for ALS abnormal.** **20130613 Page16 stuff R425 for EDP.** **20130616 Page20 change CN14 from mSATA to NGFF type and add C383.** **20130617 Page18 change CN5 footprint from hdmi-80103-1121-19p-ldv to hdmi-80103-1121-19p-ldv-smt.** **20130617 Page27 change CN6 footprint from usb-53065-00902-001-9p to usb-53065-00902-001-9p-smt.** **20130618 Page08 Del RTC circuit (D9, R169,BT1,Q2,R158,R162,R164,R166) by A .** **20130618 Page09 Del R132.** **20130620 Page22 Change R470 to 2.2ohm.** **20130620 Page28 6/20 Add R577 by Kingston SSD; change CN14 to DFHS75FR003 by ME.** **20130620 Del all Offpage of power signals in all page.** **20130621 Add C384~C388 by Intel DDR layout.** **20130621 Change CN1 to DN00024000 by ME.** **20130624 Page 26 Add R578 for B-test by G.** **20130624 Page 10 Modify RAM ID table & connect DEVSLP0 to NGFF SSD for B-test by G.** **20130624 Page 35 Add PR166~168 for B-test debug.** **20130624 Rename PP5000_AL W to PP5000_DSW by G.** **20130625 Page07 R74 stuff by G.** **20130625 Page19 Add BT_EN PU resistor R579 to PP3300_PCH R579 by G.** **20130625 Page26 Change C197 to 0.1uF; Change EC_BRD_ID to 001 by G.** **20130625 Page29 Change PR52 to 4.7Kohm by G.** **20130625 Page03 Add TP127~TP132 for XDP by Intel.** **20130625 Page20 Add R580/R581 by Kingston SSD.** **20130625 Page21 Reserve R582 by A.** **20130626 Page23 Change MIC chanel from pin19/20 to pin21/22, and add cap C389 by vendor.** **20130626 Page19 Modify BT_EN path, stuff R161.** **20130626 Page21 Add TP133~135 by A.** **20130626 Page28 Add R583,R584 by G.** **20130626 Page27 Change Hole20,22 footprint by ME.** **20130626 Page8 Change C278,C286 to 15pF by crystal.** **20130626 Page26 Change C127,C128 to 18pF by crystal.** **20130626 Page33 Change PR99 to CU310015Z02 on C-test by Power.** **20130705 Page18 Change R142,R134,R127,R119,R138,R129,R116,R111 from 680 to 470ohm; unstuff R114,R122,R133,R457 by HDMI EA test.** **20130709 Page32 change PC4,PC6 from 4.7uF to 10uF, PR17 from 10ohm to 20ohm by Power.**
	3A	**20130711 Page11 R40 connection change to PP3300_PCH by leakage.** **20130711 Page25 unstuff R574 by G.** **20130716 Page34 unstuff PU3,PC19,PC20 by power.** **20130716 Page27 modify Hole17 to GND; Hole24 to BATT_EN#; Hole25 to SPI WP_ME by G.** **20130718 Page32 change PR111 to CS45232FB00 by power.** **20130718 Page13 unstuff U19,U22 by ICT.** **20130722 Page32 modify PU30,PC3,PC37,PC4,PC6,PC48,PR110,PR111,PR112, unstuff PC52 by power.** **20130723 Page23 Change SW2 to J1 by ME space.** **20130723 Page26 Change EC_BRD_ID fromn 001 to 010(stuff R197,R516; unstuff R203,R518).** **20130724 Page25 Reserve D29~D31 by ESD.** **20130726 Page29~35 Del JP and change 0ohm to shortpad.** **20130726 Page16 Del colayout L12 by SMT.** **20130729 Page28 Add R585 for OVERT# pull high by G.** **20130729 Page20 Reserve R586~R589 for UART debug/B.** **20130729 Page13 Reserve CN15, R590~R597 for XDP debug by Intel.** **20130731 Page21 Add R598 replace JP7.** **20130731 Page28 Del L18,L19 by SMT.** **20130731 Page27 Del L14,L3,L2 by SMT.** **20130731 Page23 Change CN1 to DNQTZEA0000 (SMD type: mic-obs-f1342-22hf-2p) by SMT.** **20130801 Page23 Change CN1 to footprint to mic-a-au-qtza01hf-2p-tnp** **20130801 Page25 Remove CP1~CP5,C207,C336** **20130801 Page25 Add U33~U37,D32,D33 for ESD** **20130801 Page10 Stuff R382 by G** **20130801 Page20 Un-Stuff R577 by G** **20130802 Page5 Add C390~C396** **20130802 Page5 Remove C390~C396** **20130802 Change C35, C266, C244, C62, C248, C49, C262, C260, C41, C46, C42, C246, C21, C267, C23, C20, C25, C44, C27, C26, C24, C43, C45, C22, C247, C245,C14, C38, C50, C84, C151, C237, C240, C385, PC3, PC37 from CH6221M9900 to CH1221M9A02** **20130805 Page26 Change EC_BRD_ID to 010 for PVT by G.** **20130806 Page32 Change PR112 value to 2.55K by power.** **20130806 Change C35, C266, C244, C62, C248, C49, C262, C260, C41, C46, C42, C246, C21, C267, C23, C20, C25, C44, C27, C26, C24, C43, C45, C22, C247, C245,C14, C38, C50, C84, C151, C237, C240, C385, PC3, PC37 from CH1221M9A02 to CH1221M9A03** **20130806 Unstuff C22,C25,C26,C41,C49 for acoustic noise by Pwr.** **20130813 Page25 Reserve Q27,Q28,R599,R600 for FAN leakage.** **20130813 Change R95,R125,R54,R408,R152,R307,R152,R51,R93,R94 from 0 to shortpad.** **20130821 Page21 Change R76,RC1,R207,R201 from 0 to shortpad & del L1,5 co-lay by SMT.** **20130821 Page18 Change R443,R445 from 0 to shortpad & del L13 co-lay by SMT.** **20130821 Page24 Change L16,L21 from CXSPX800000 to 0ohm by SMT.** **20130822 Page25 Change CN13 footprint from 88502-2401-24P-R-SMT to 88502-2401-24P-L-SMT and swap CN13, Q26 pin define.** **20130823 Page32 Del PC47 and Add PCN1** **20130823 Page34 Del PC72 and Add PCN2** **20130823 Page4 Change TP73, TP74, TP75 and TP76 footprint from TP2650 to TP2050** **20130823 Page5 Change TP81 footprint from TP2650 to TP2050** **20130823 Page8 Change TP93 footprint from TP2650 to TP2050** **20130826 Page25 Change pin5 of U33, U34, U35, U36 and U37 power rail from PP5000 to PP5000_DSW** **20130826 Page32 Change PC3 and PC37 from 22uF to 47uF. Unstuff others Vccin capacitors.** **20130826 Page5 Change C247, C244, C27, C23, C25, C21, C20 and C48 from 22uF to 47uF. Unstuff others Vccin capacitors.**