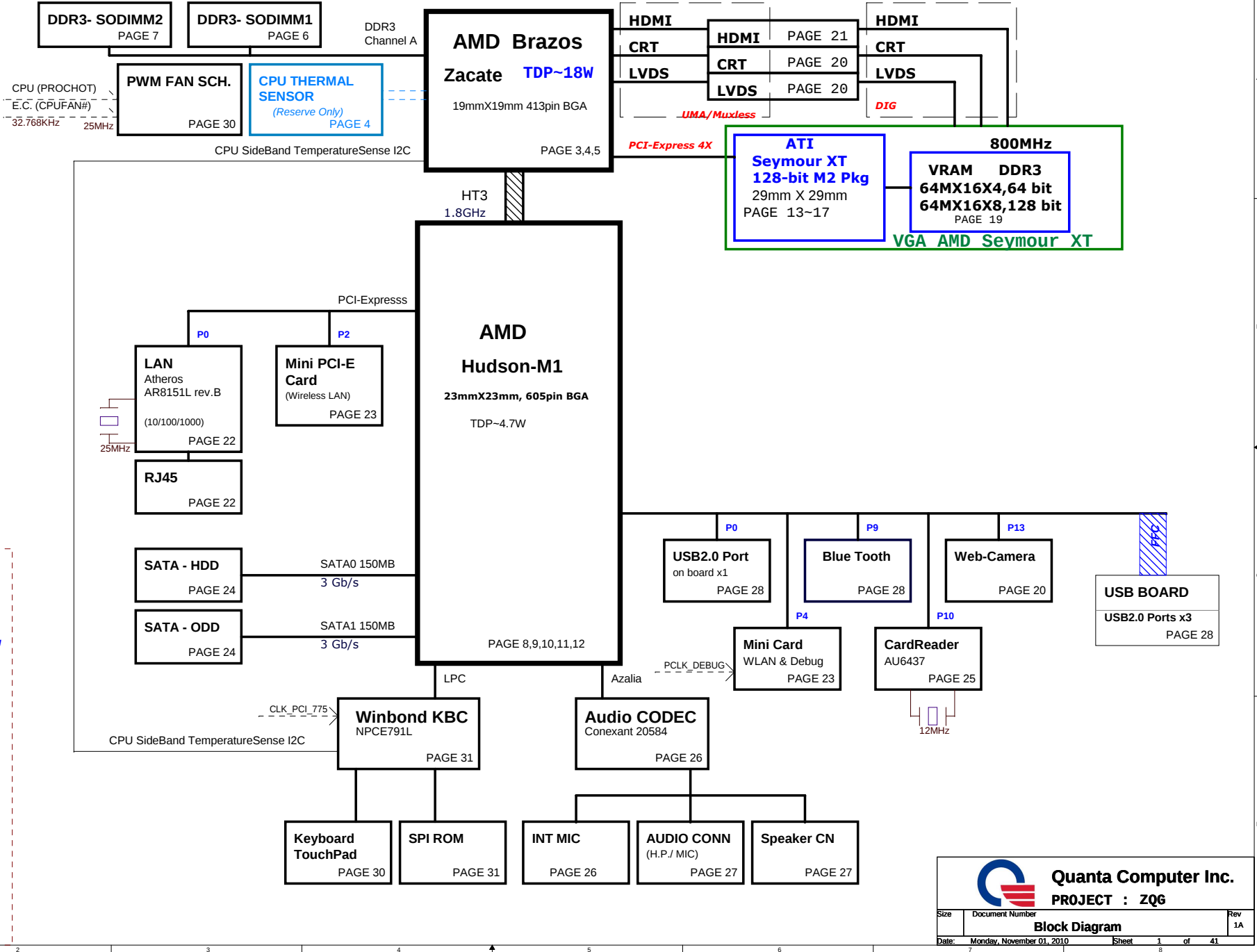


ZQG SYSTEM DIAGRAM

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

IV@ -----> iGPU / PWW control
SW@ -----> Switchable iGPU & dGPU
SWS@ -----> VRAM / Strap / BACO option
SP@ -----> Board ID / VBIOS option / CPU

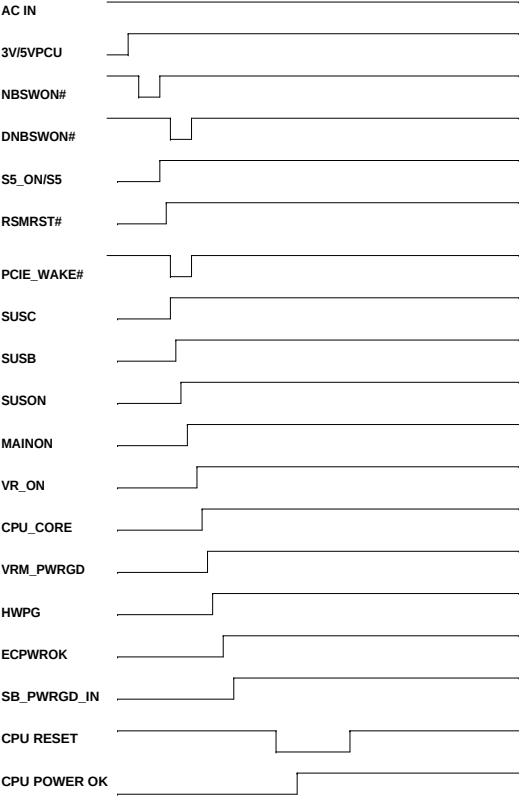


Quanta Computer Inc.
PROJECT : ZQG

Size	Document Number	Rev
	Block Diagram	1A
Date:	Monday, November 01, 2010	Sheet 1 of 41

PAGE#	DESCRIPTION	NOTE
1	BLOCK DIAGRAM	
2	SYSTEM INFORMATION	
3	ONTARIO MEM & PCIE I/F(1/3)	
4	ONTATIO DISPLAY/CLK/MI(2/3)	
5	ONTARIO POWER & DECOUP(3/3)	
6	DDR3 SO-DIMM (RVS)	
7	DDR3 SO-DIMM (STD)	
8	HUDSON PCIE/LPC/CPU I/F(1/5)	
9	HUDSON ACPI/GPIO/USB(2/5)	
10	HUDSON SATA/BIDs(3/5)	
11	HUDSON PWR/GND(4/5)	
12	HUDSON STRAPS/PWRGD(5/5)	
13	Seymour - PCIE	
14	Seymour - HOST	
15	Seymour - MEM	
16	Seymour - PWR/GND	
17	Seymour - DP_PWR/GND (BACO)	
18	VRAM strap	
19	VRAM channel B	
20	CRT/LVDS/LID	
21	HDMI	
22	LAN AR8151	
23	MINI PCI-E	
24	HDD /ODD	
25	CARD READER	
26	AUDIO - CONEXANT 20584	
27	AUDIO JACK CONN	
28	USB / BT /TP	
29	LED / NUT	
30	KB/FAN/TP	
31	WPCE791 /FLASH	
32	CHARGER (ISL88731)	
33	SYSTEM 5V/3V (RT8206)	
34	CPU CORE (OZ8380)	
35	VCCP 1.1V (UP6111A)	
36	+1V(G5602)	
37	DDR 1.5V (TPS51116)	
38	GPU CORE (MAX8792)	
39	+1.8V/+1.5_GPU/+1.8V_GPU	
40	Discharge/Thermal Protection	

Power Sequence



Hudson M1 SM BUS

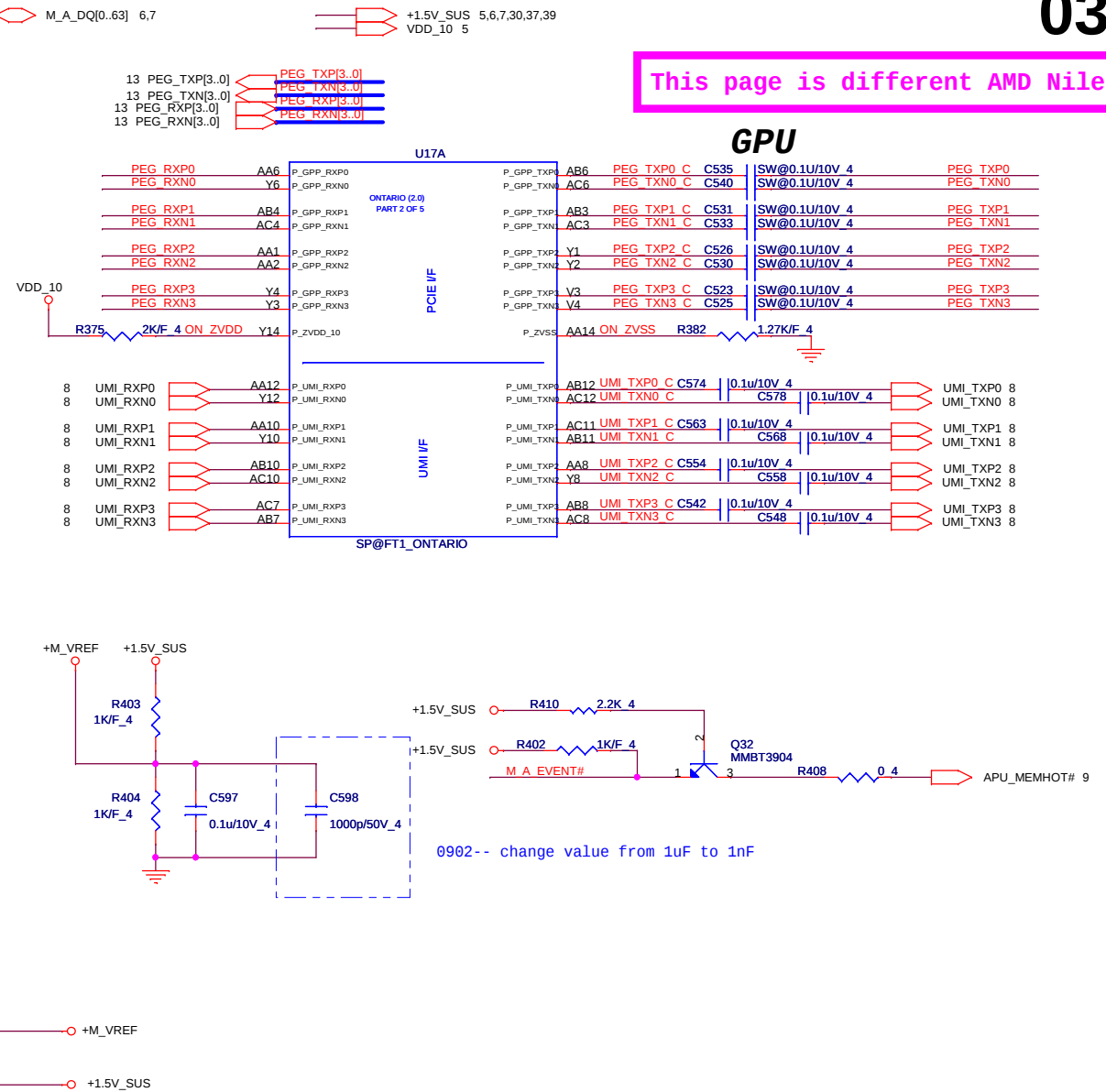
SB820 SMBUS	Pin NO.	SMBUS Function Define
PCLK_SMB PDAT_SMB (+3V)	AD22 AE22	DDR / RFID
SB_SMBCLK1 SB_SMBDATA1 (+3V_S5)	F5 F4	not used
SB_SCLK2 SB_SDATA2 (+3V_S5)	D25 F23	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used

KBC(EC) SM BUS

KBC SMBUS	Pin NO.	SMBUS Function Define
MBCLK MBDATA (+3VPCU)	110 111	Battery
MBCLK_THRM MBDATA_THRM (+3VPCU)	115 116	Thermal

This page is different AMD Nile

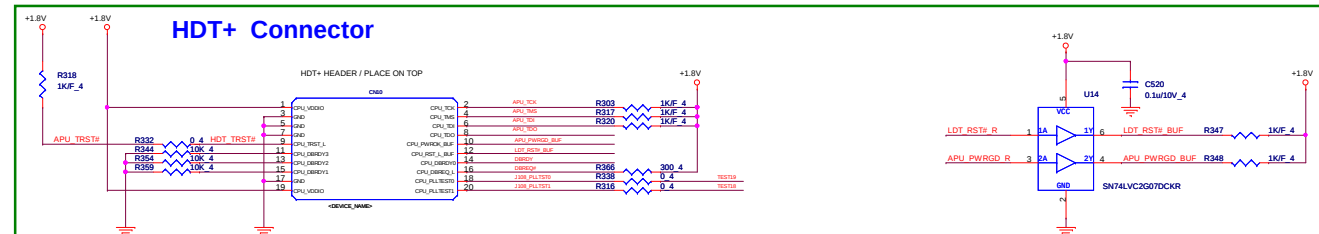
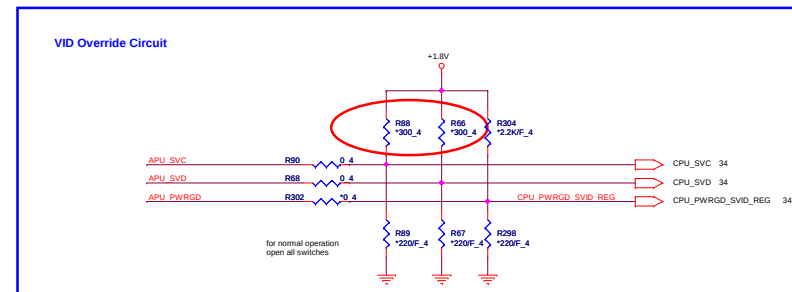
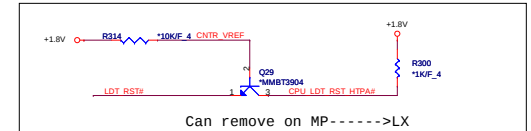
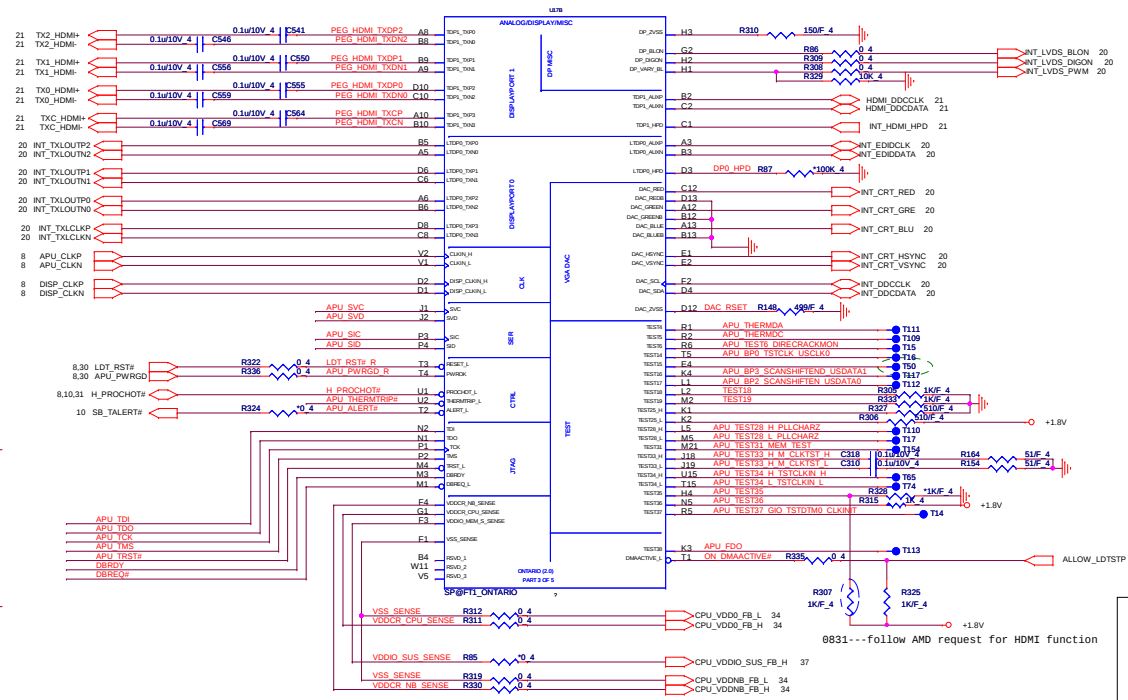
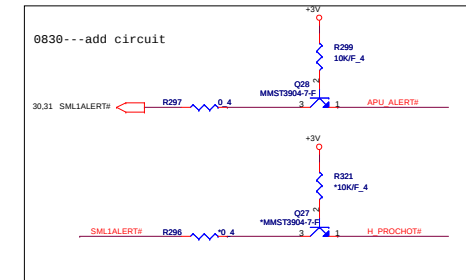
GPU



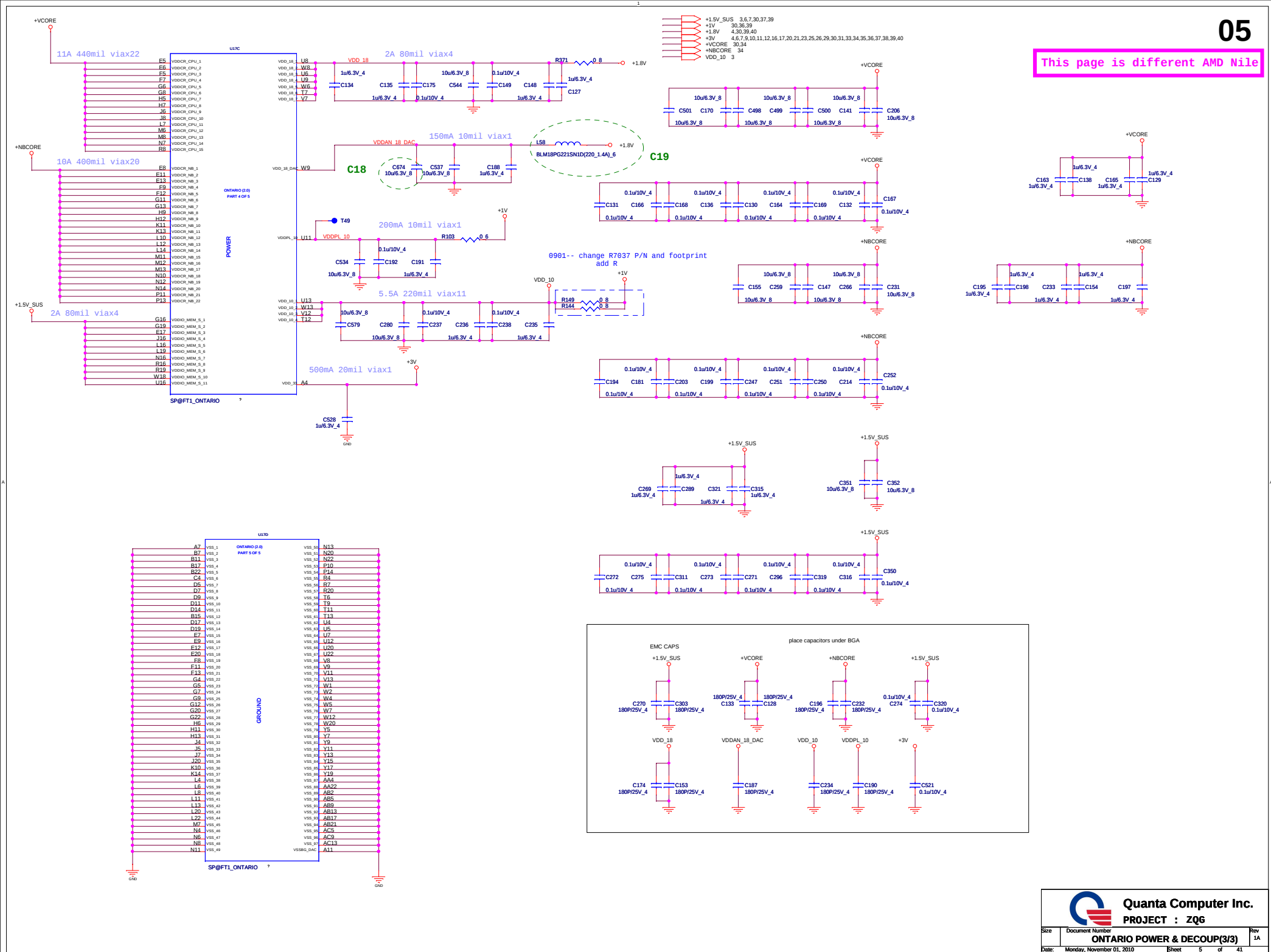
Quanta Computer Inc.
PROJECT : ZQG

Size	Document Number	Rev
	ONTARIO MEM & PCIE I/F(1/3)	1A

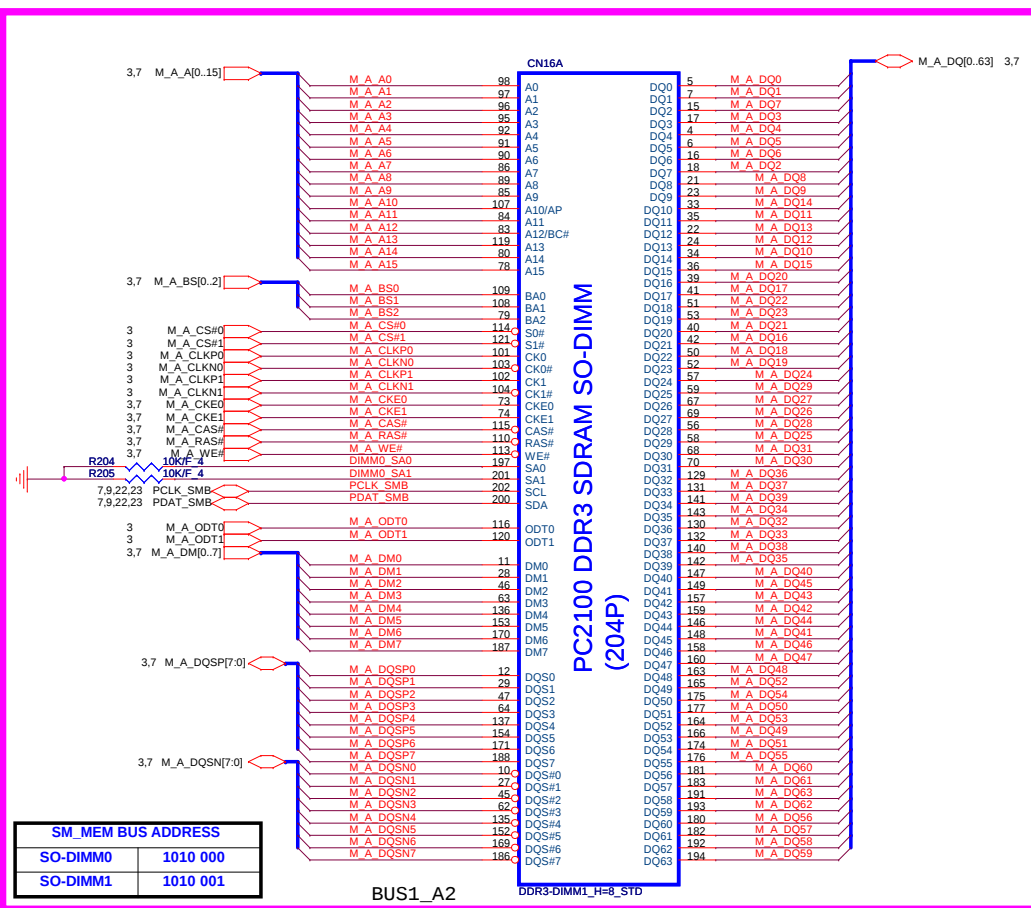
Date: Monday, November 01, 2010 Sheet 3 of 41



This page is different AMD Nile



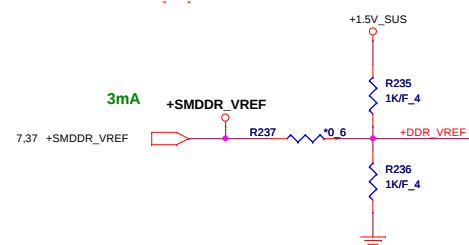
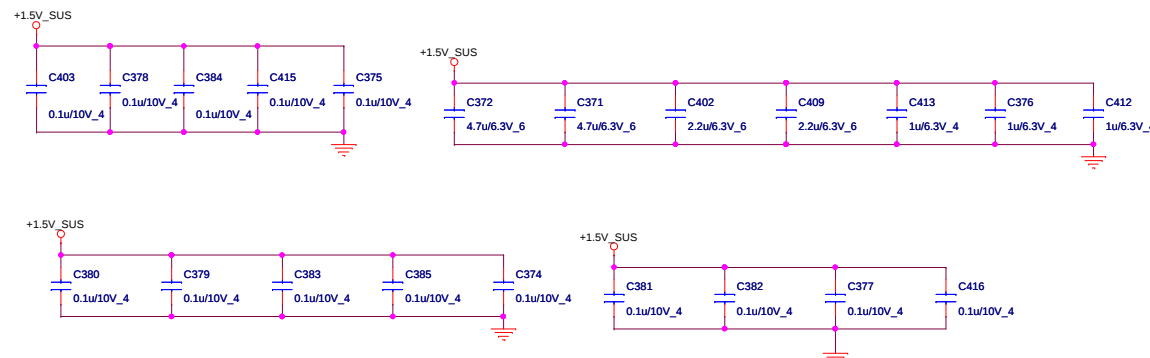
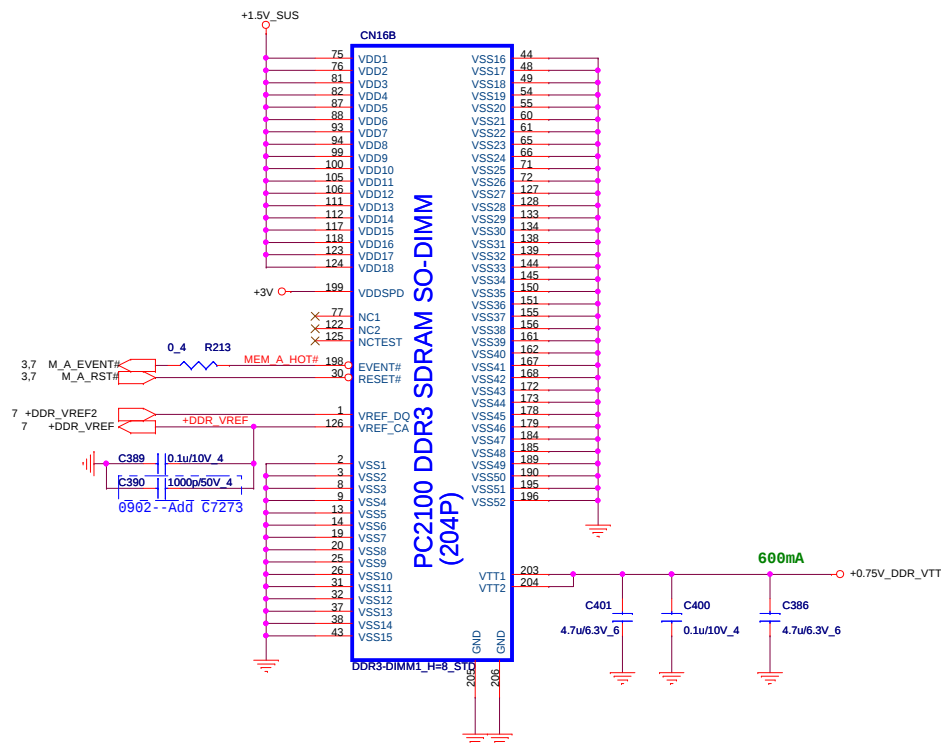
0830--P/N and footprint are follow ZR7B

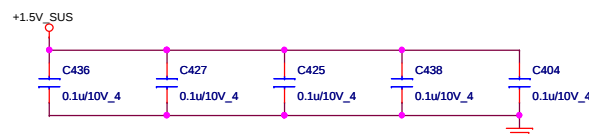
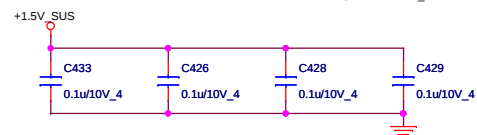
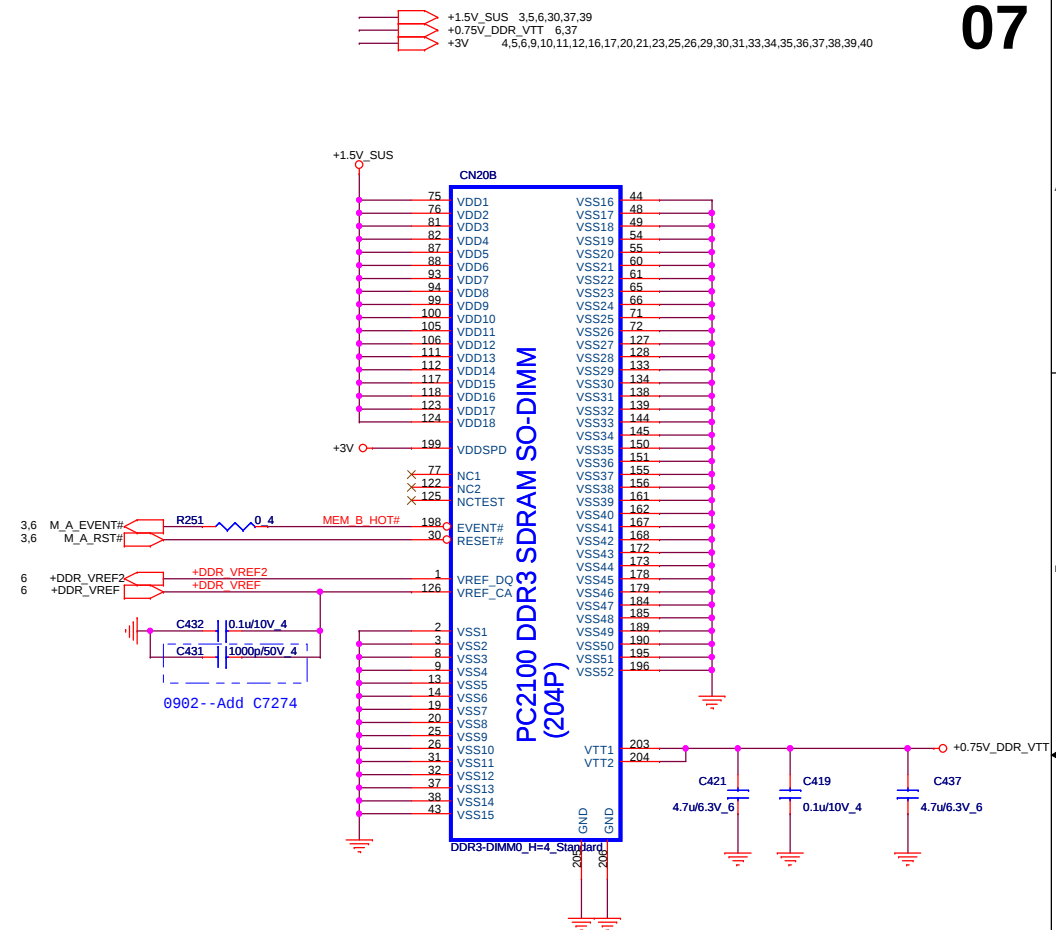


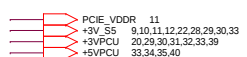
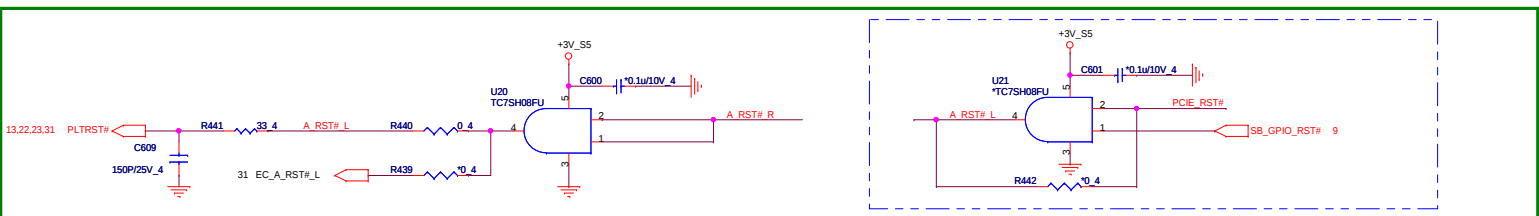
+1.5V_SUS 3.5,7,30,37,39

+0.75V_DDR_VTT 7,37

+3V 4,5,7,9,10,11,12,16,17,20,21,23,25,26,29,30,31,33,34,35,36,37,38,39,40

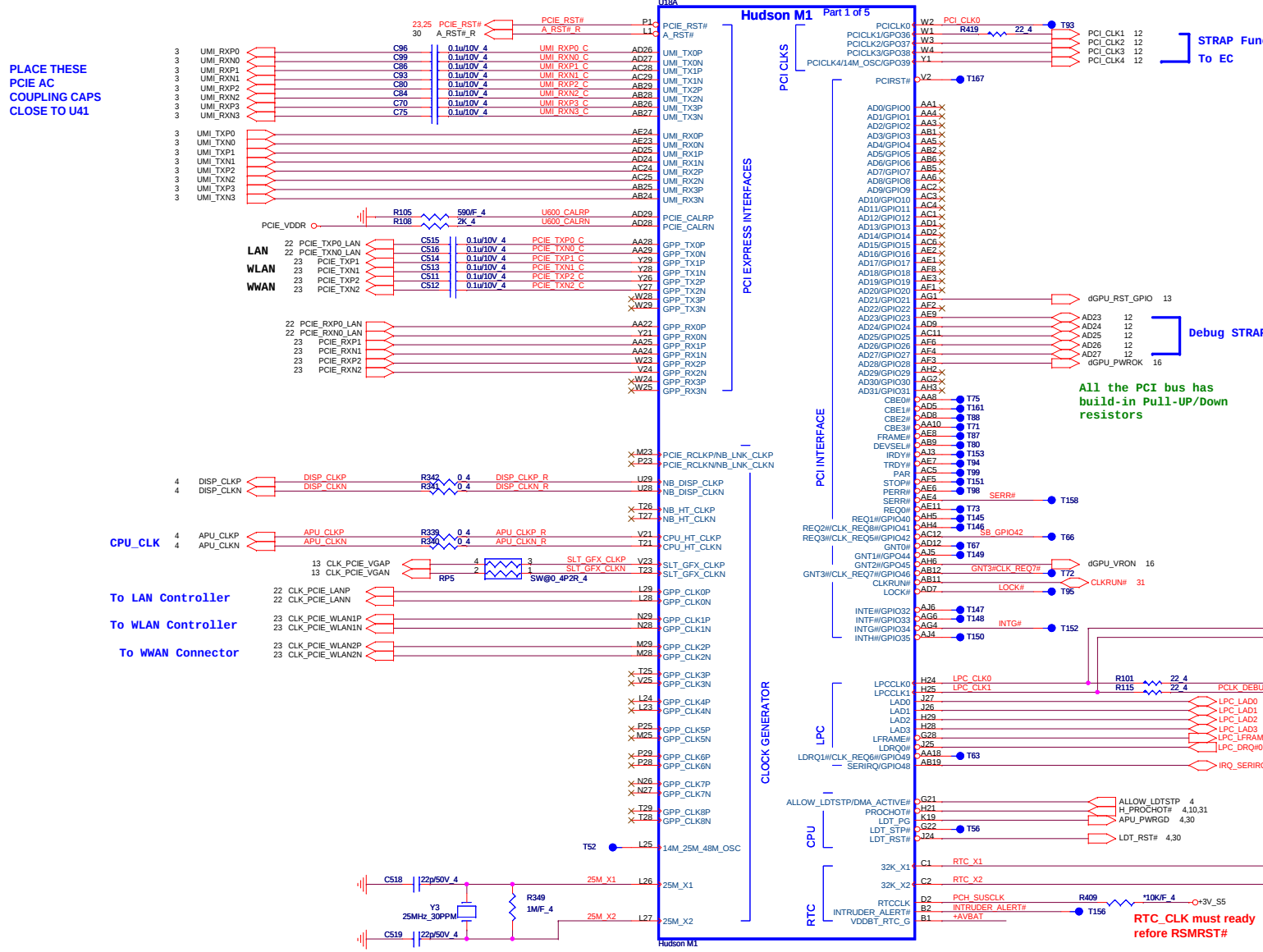




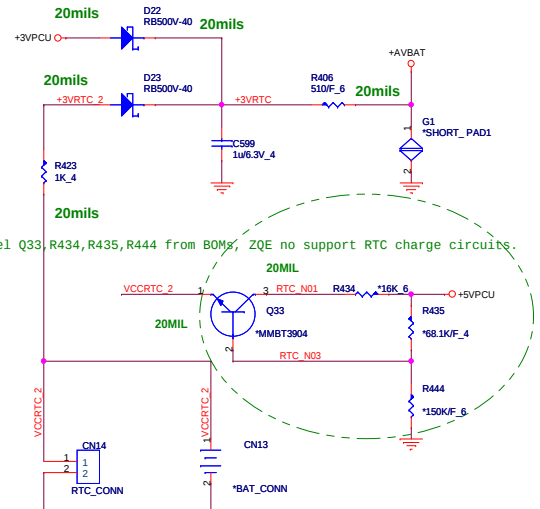


This page is different AMD Nile expect RTC circuit

PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO U41



RTC

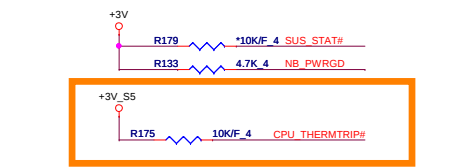
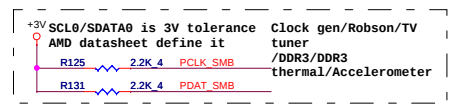


CR2032 with cable
AHL03003004
AHL03003032
AHL03003037 , AHL03001044

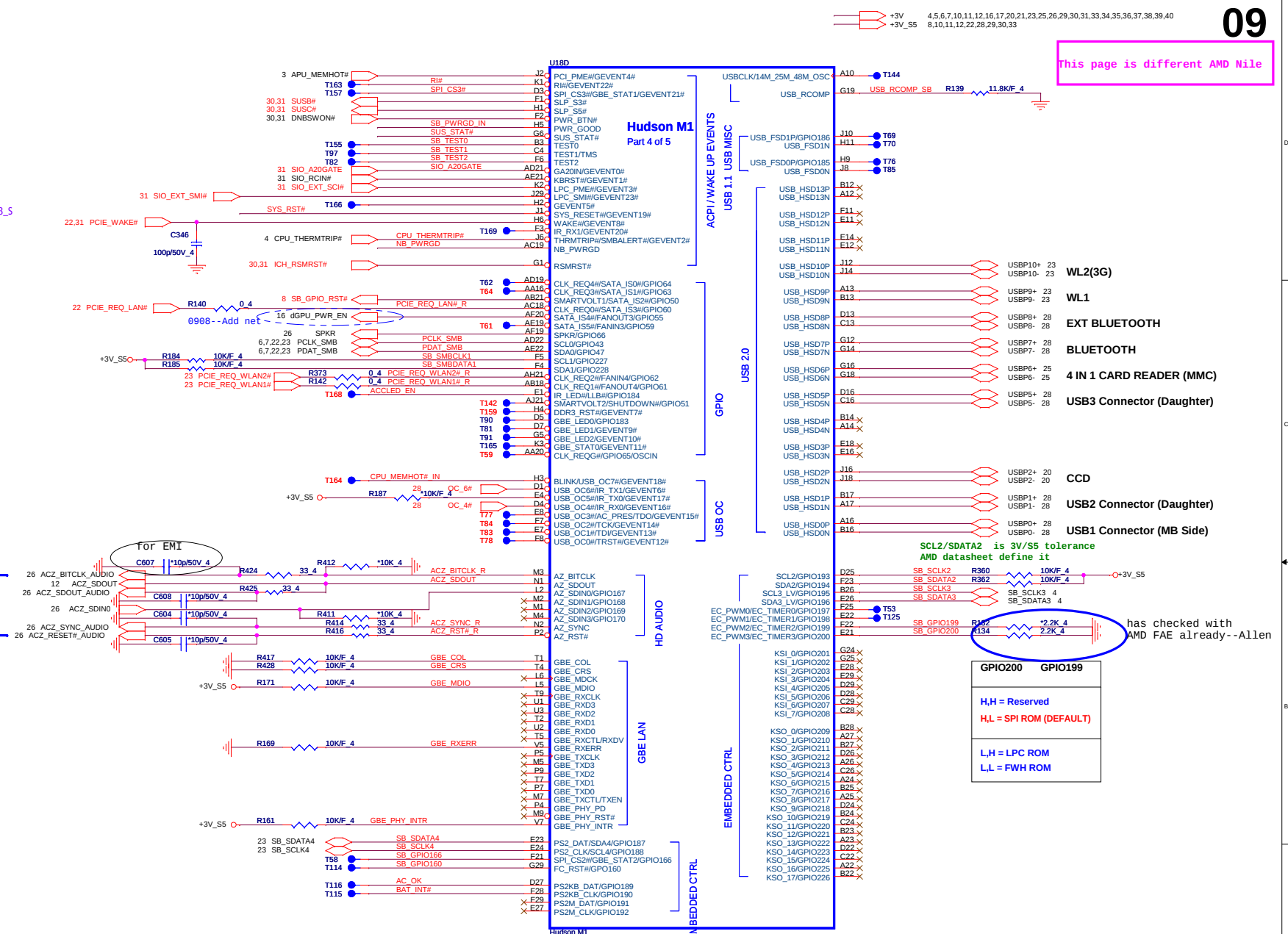
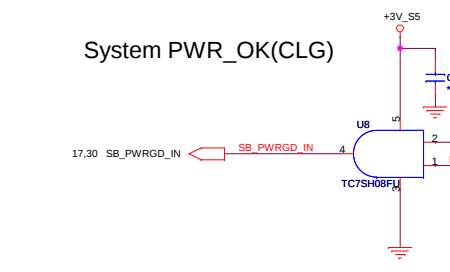
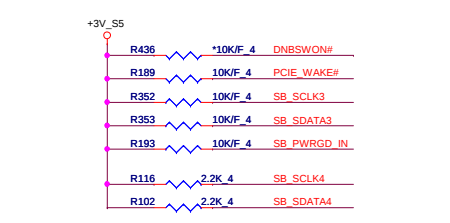
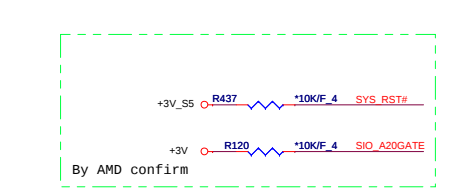
CR2032 (Non-Chargeable)
AHL03003014
AHL0300M009

To STRAPS Page

INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).



SB/ PWR_GOOD / VDDIO_33_5





SATA PORT 0,1,2,3
can support AHCI
mode

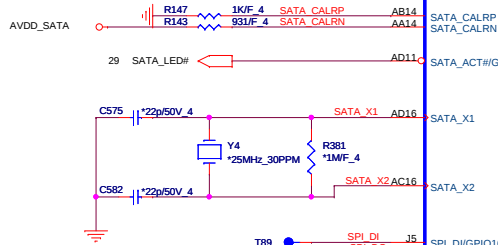
PLACE SATA AC COUPLING
CAPS CLOSE TO HUDSON M1

SATA HDD

SATA ODD

XTLVDD_SATA-- SATA
crystal power
PLVDD_SATA--
SATA PLL
POWER

PLACE SATA_CAL RES
VERY CLOSE TO BALL
OF HUDSON M1



T89
T96
T100
T79
T162

SPI DI J5
SPI DO E2
SPI CLK K4
SPI CS1# K9
ROM_RST# G2

SERIAL ATA

HW MONITOR

SPI ROM

Hudson M1 Part 2 of 5

FLASH

BOARD ID0
BOARD ID1
SB_PROCHOT#

BOARD ID2
BOARD ID3
BOARD ID4

TEMPIN0
TEMPIN1
TEMPIN2
SB_TALERT#

CPU TYPE
SB_HOLE_TIME
CPU_SENSOR

VIN2
VIN3
VIN4
VIN5
BOARD ID5

VIN0/GPIO175
VIN1/GPIO176
VIN2/GPIO177
VIN3/GPIO178
VIN4/GPIO179
VIN5/GPIO180
VIN6/GBE_STAT3/GPIO181
VIN7/GBE_LED3/GPIO182

NC1
NC2

G27
Y2

H_PROCHOT#

SB_PROCHOT#

4.8.31 H_PROCHOT#

R8500V40

0831--add circuit

0831--modify location

0831--add circuit

0831--add circuit

0831--add circuit

0831--add circuit

0831--add circuit

0831--add circuit

0831--add circuit

0831--add circuit

0831--add circuit

0831--add circuit

0831--add circuit

0831--add circuit

0831--add circuit

0831--add circuit

0831--add circuit

0831--add circuit

0831--add circuit

0831--add circuit

0831--add circuit

0831--add circuit

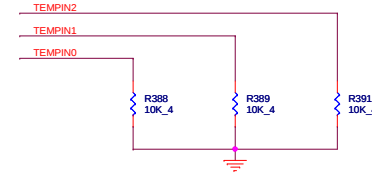
0831--add circuit

AVDD_SATA 11
+3V 4,5,6,7,9,11,12,16,17,20,21,23,25,26,29,30,31,33,34,35,36,37,38,39,40
+3V_S5 8,9,11,12,22,28,29,30,33

10

This page is different AMD Nile

AMD recommend : TEMPIN0 / TEMPIN1 / TEMPIN2
can not maintain on floating stages when without usage.
Do not care pull high or pull down.



MB ID

CPU THERMAL	GPIO52
External	1
SB-TSI	0

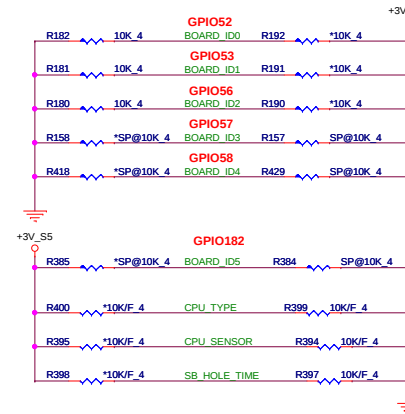
SB8XX Hold Time	GPIO53
1.2V	1
1.1V	0

DU1/MK2	GPIO56
MK2.0 AMD	1
DU1.0 AMD	0

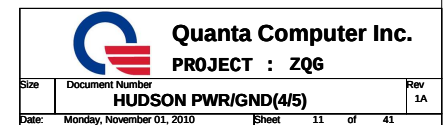
(Dis) SW	GPIO57
UMA	0

VRAM - 800	GPIO58
VRAM-900	0

PX4.0	GPIO182
PX3.0	0



PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

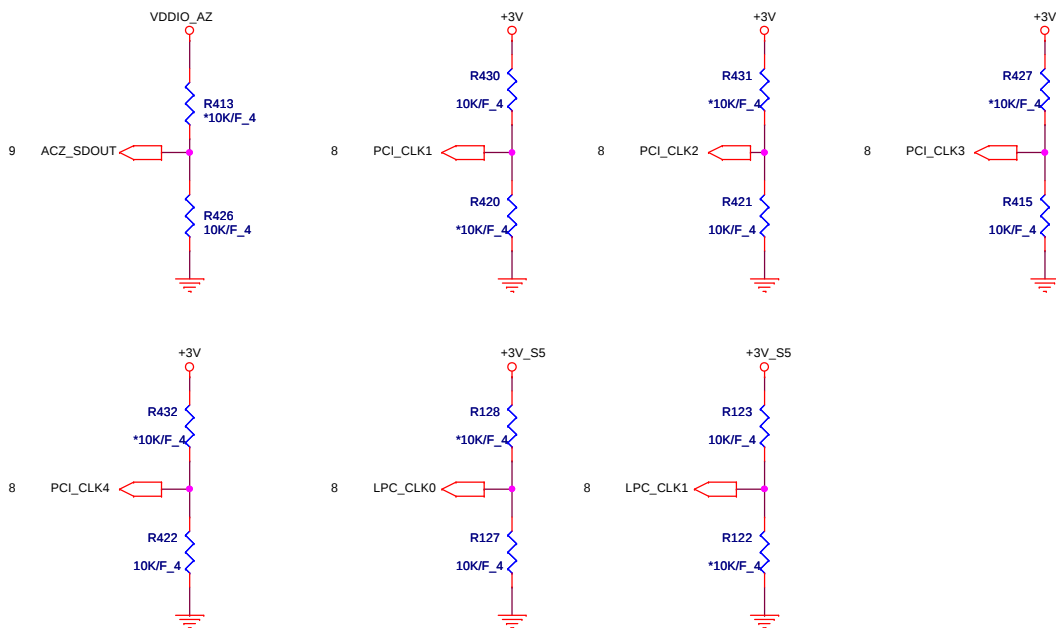




OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS

internal have pull
Hi 10K, confirm AMD
ward this pull Hi
not need



PCI_CLK4 CPU/NB HT Clock Selection
0 V - Reserved.
3.3 V - Required setting for integrated clock mode.
This strap is not used if the strap CLKGEN is
configured for external clock generator mode.

REQUIRED STRAPS

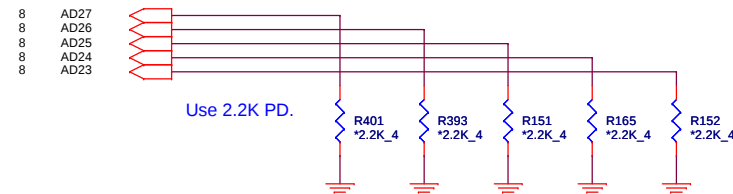
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM (Default)	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM L,L = FWH ROM	

VDDIO_AZ 11
+3V 4,5,6,7,9,10,11,16,17,20,21,23,25,26,29,30,31,33,34,35,36,37,38,39,40
+3V_S5 8,9,10,11,22,28,29,30,33

12

DEBUG STRAPS

HUDSON-M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

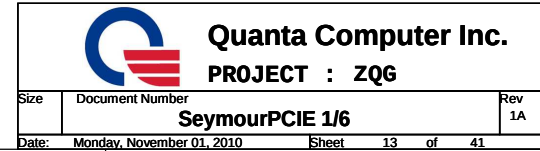


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



Quanta Computer Inc.
PROJECT : ZQG

Size Document Number
Date: Monday, November 01, 2010 Sheet 12 of 41
HUDSON STRAPS/PWRGD(5/5)
Rev 1A



GPU Power-on sequence

```
1 => +3V_D
2 => +VGPU_CORE
3 => +1V
4 => +1.5V_GPU
5 => +1.8V_GPU
6 => dGPU_PWROK
```

1.8V GPIO

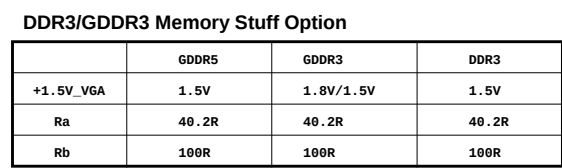
For Park-M2 NC
pin

For Park-M2 NC
pin
DVPDATA_17 -
DVPDATA_23
+3V_D

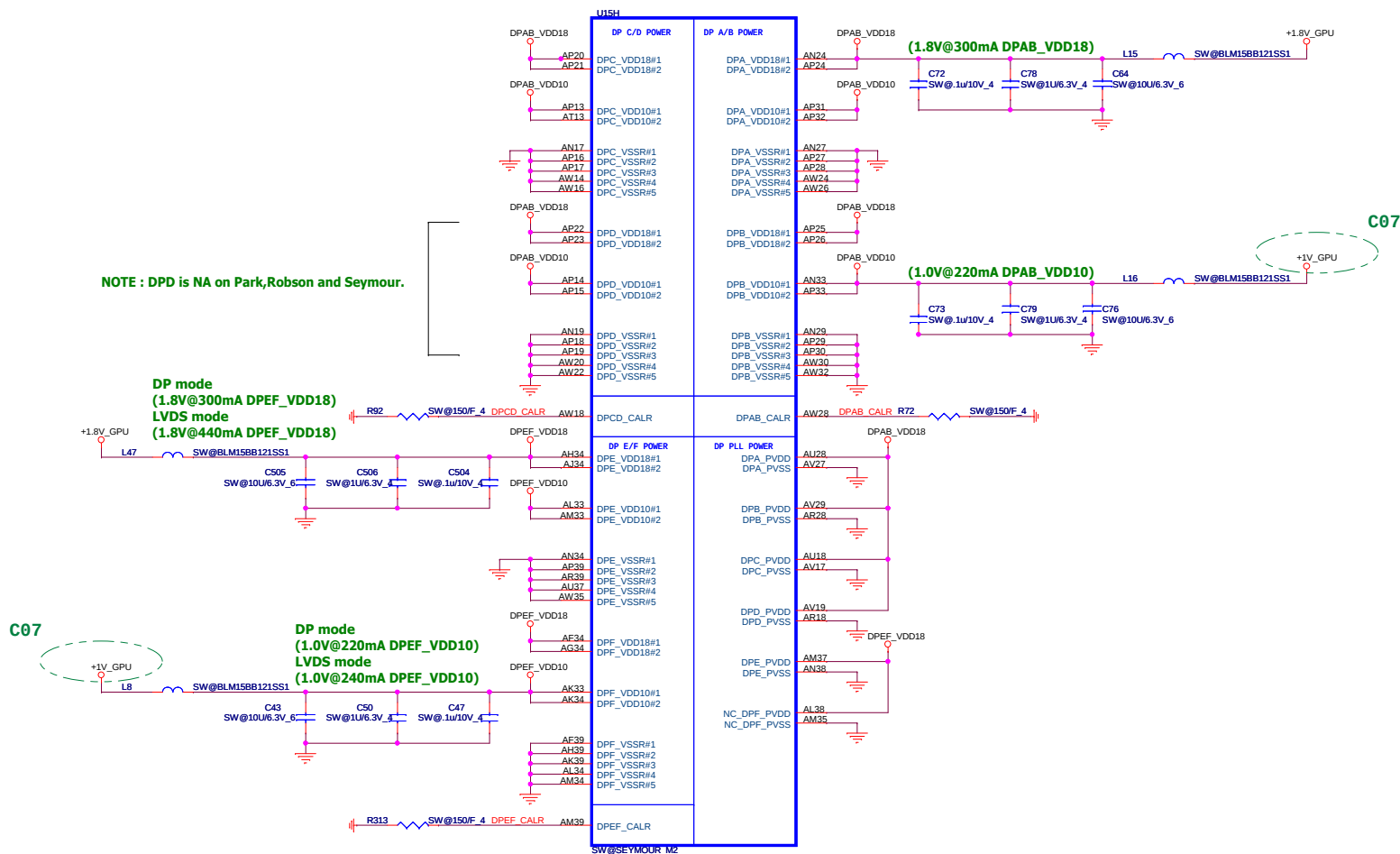
3.3V GPIO

SW@SEYMOUR_M2

SW@SEYMOUR_M2

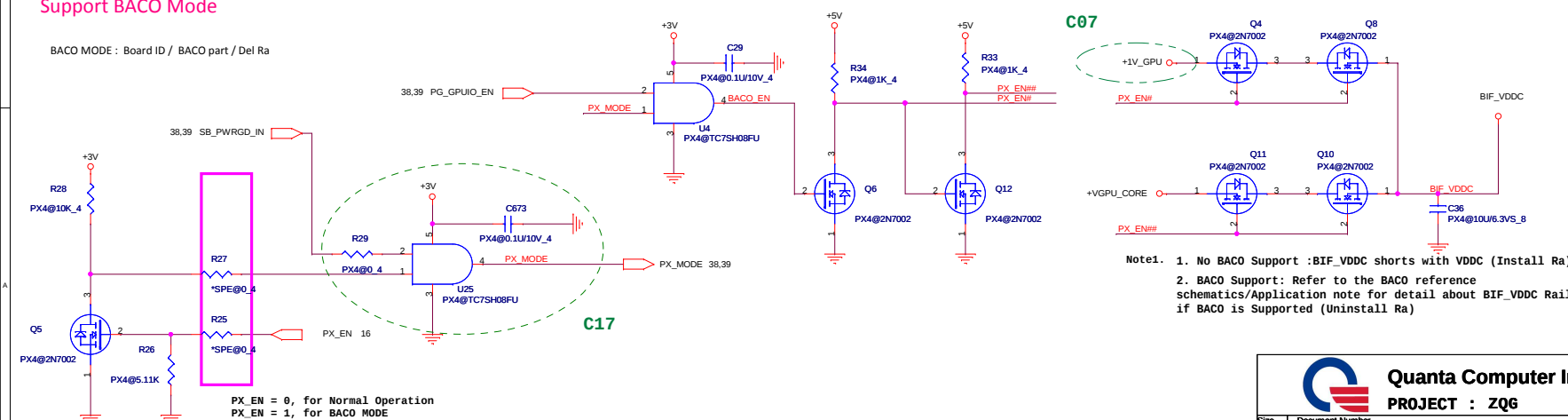




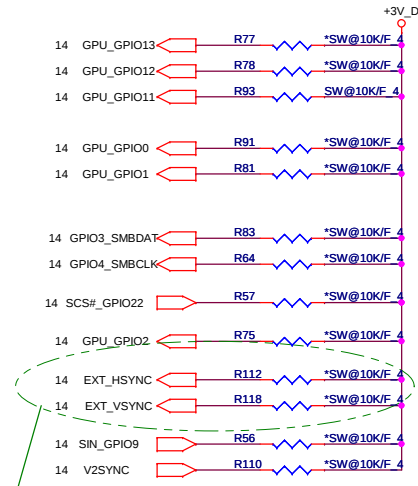


Support BACO Mode

BACO MODE : Board ID / BACO part / Del Ra



PIN STRAPS



C08 : to slove the HDMI issue , remove R112,R118 from BOMs

Memory Aperture size

GPIO[13:11] Size

000	128MB
001	256MB
010	64MB
011	32MB

C02 : to slove the Power DVD issue , setting size to 256MB

ROM Table

EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

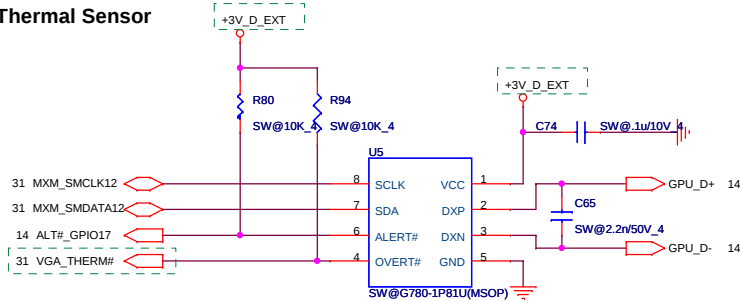
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1:0] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	00	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

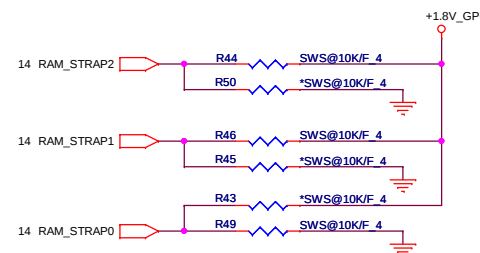
DDR3 Memory Aperture size

Vendor	Vendor P/N	STN B/S P/N	Total Memory Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0	ZQE/G
Hynix	H5TQ1G63DFR-11C	AKD5LZWTW05 (64M*16)	1GB (900 Mhz)	1	1	0	V
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1GB (800 Mhz)	1	0	0	V
	H5TQ2G63BFR-12C	AKD5MGGTW03 (128M*16)	2GB	1	1	1	V
Samsung	K4W1G1646G-BC11	AKD5EGGT503 (64M*16)	1GB	0	1	0	
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1GB (800 Mhz)	0	0	0	V
	K4W2G1646B-HC12	AKD5MGGT500	2GB	0	0	1	

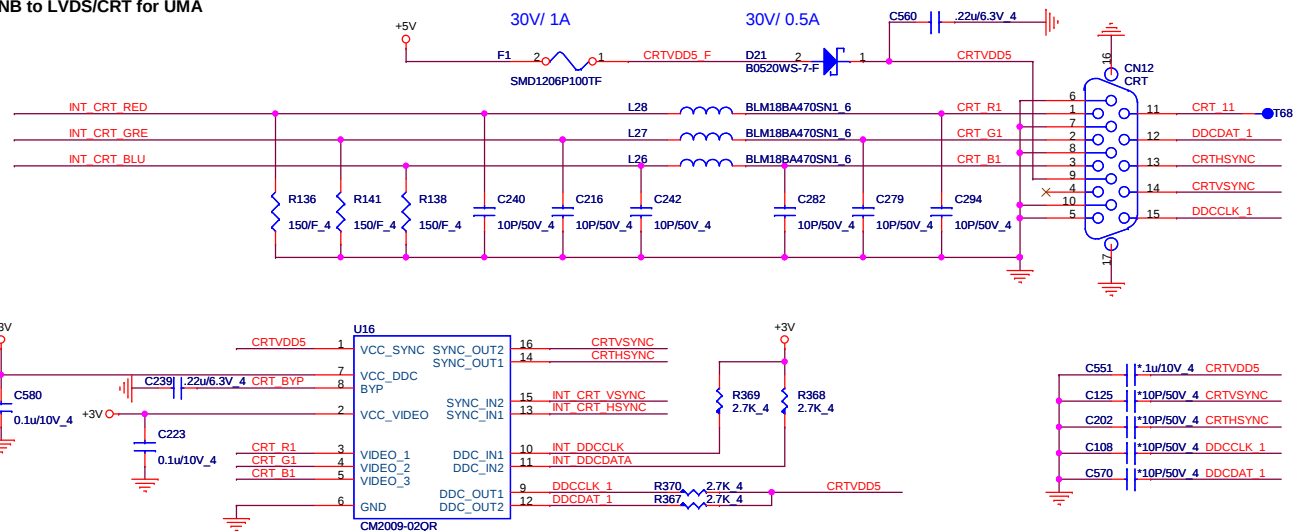
Thermal Sensor



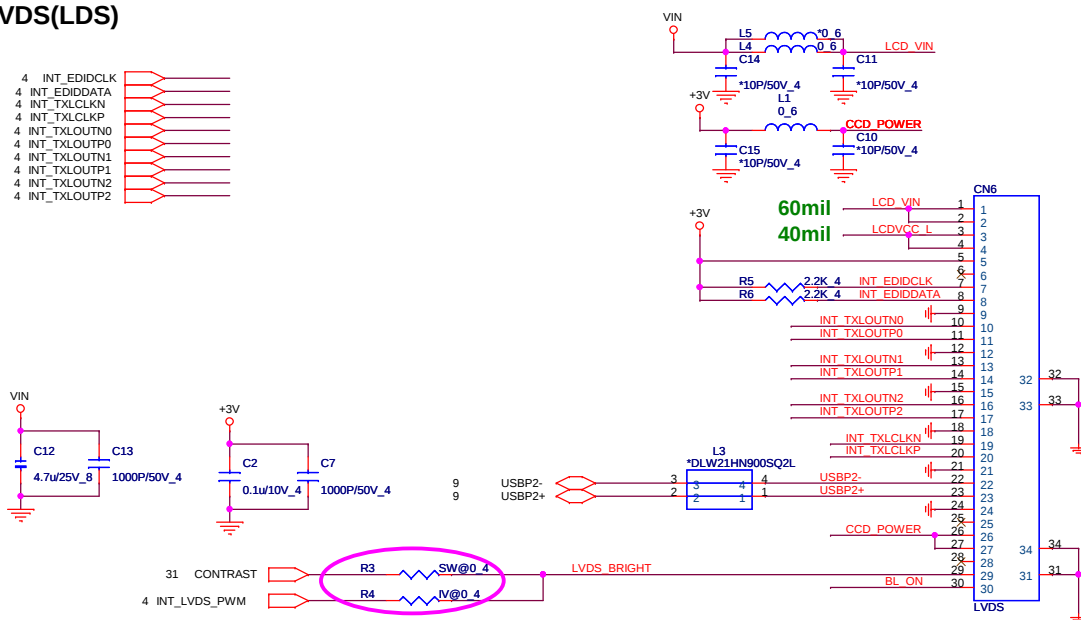
Address ID: 98H

RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

OPTION SIGNAL FROM NB to LVDS/CRT for UMA



4 INT_EDIDCLK
4 INT_EDIDDATA
4 INT_TXLCLKN
4 INT_TXLCLKP
4 INT_TXLOUTN0
4 INT_TXLOUTP0
4 INT_TXLOUTN1
4 INT_TXLOUTP1
4 INT_TXLOUTN2
4 INT_TXLOUTP2



PT3661-BB (PLC) : AL003661003
ME268-002 (FCE) : AL00268000

[illegible]

The schematic diagram illustrates the BLON driver circuit. It features a 3V power supply connected to a network of resistors and MOSFETs. The input signal, INT_LVDS_BLON, is connected to the gate of MOSFET Q3 (2N7002K). The drain of Q3 is connected to the gate of MOSFET Q1 (2N7002K). The drain of Q1 is connected to the BLON output. MOSFET Q2 (DTC144EUA) is connected to the EC_FPBACK output. A diode D2 (BAS316) is connected between the BLON output and the EC_FPBACK output. Resistors R7 (10K_4) and R8 (10K_4) are connected to the 3V supply, and resistor R9 (100K_4) is connected to ground.

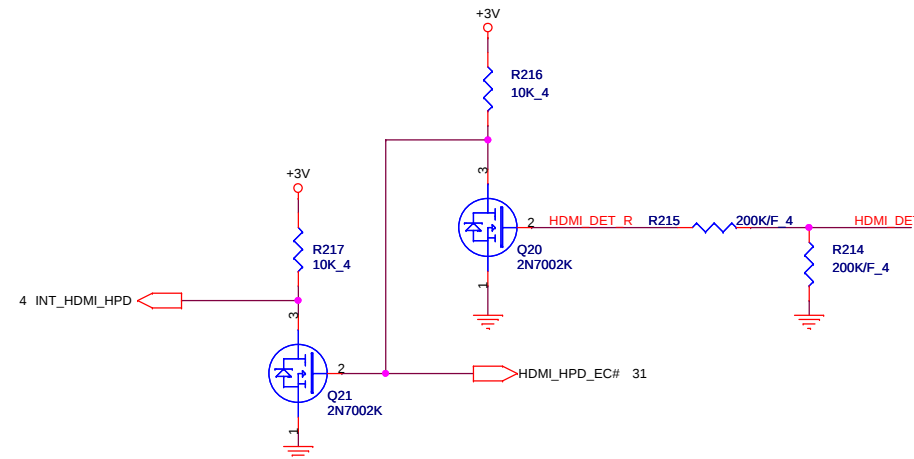
HDMI SDVO I2C Control



HDMI HPD SENSE (HDM)

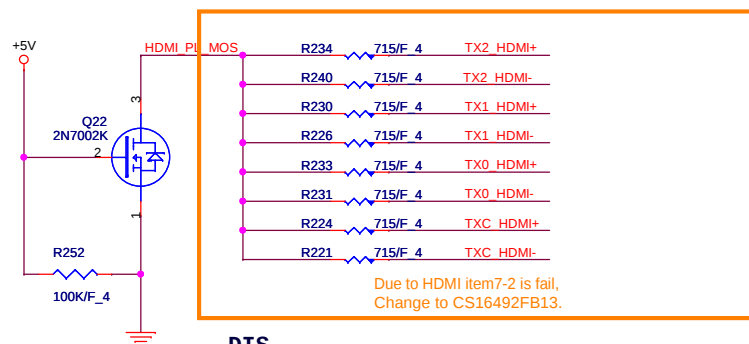
23

UMA use +3V for the detect pin
Dis use +3V_DELAY for the detect pin



HDMI (HDM)

Close to HDMI Connector

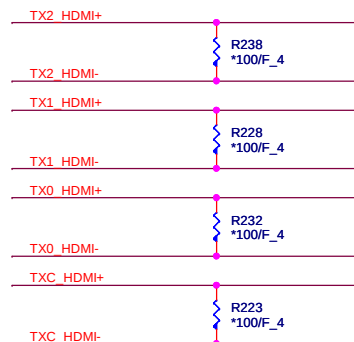


DIS
Stuff 499 ohm CS14992FB24

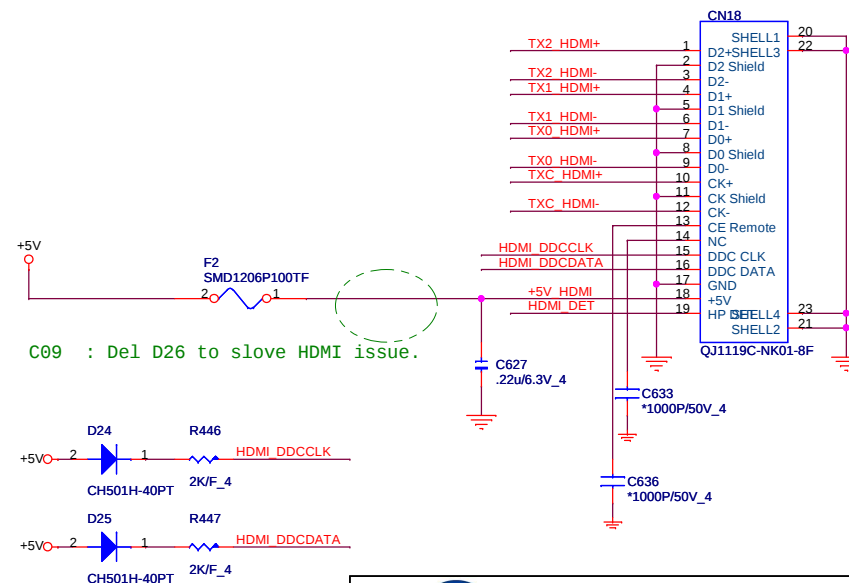


EMI reserve for HDMI(EMC)

Close connector



HDMI PORT (HDM)

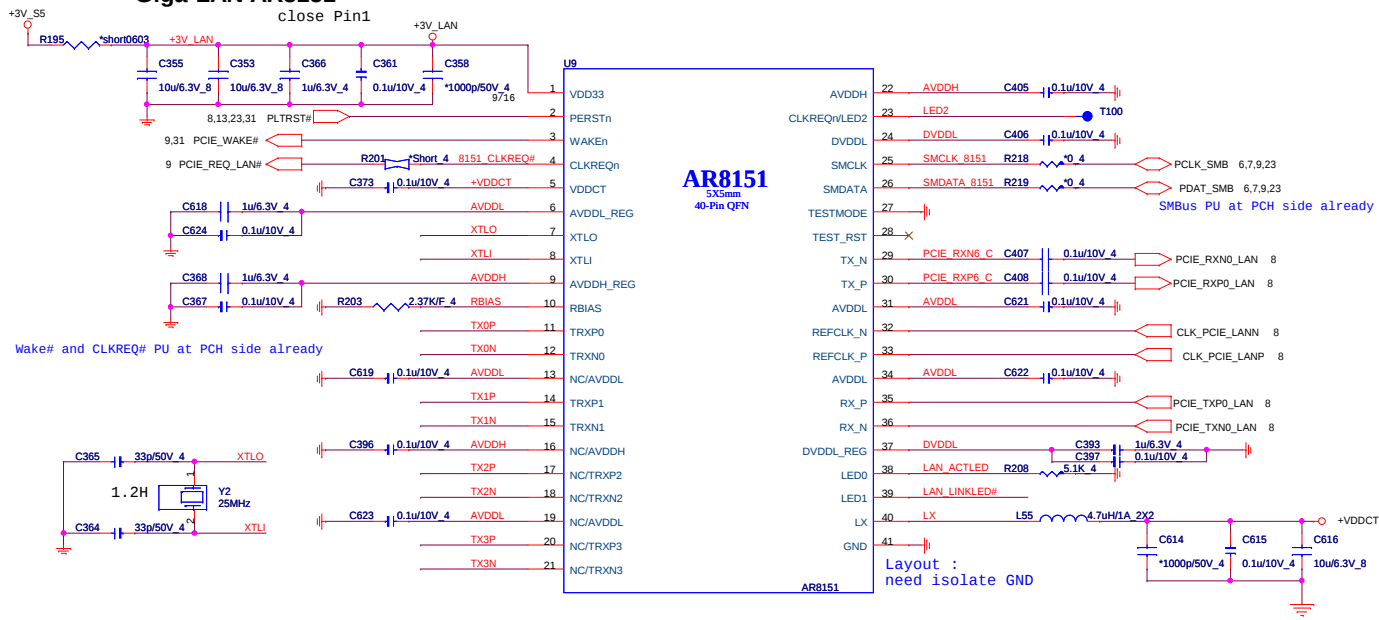


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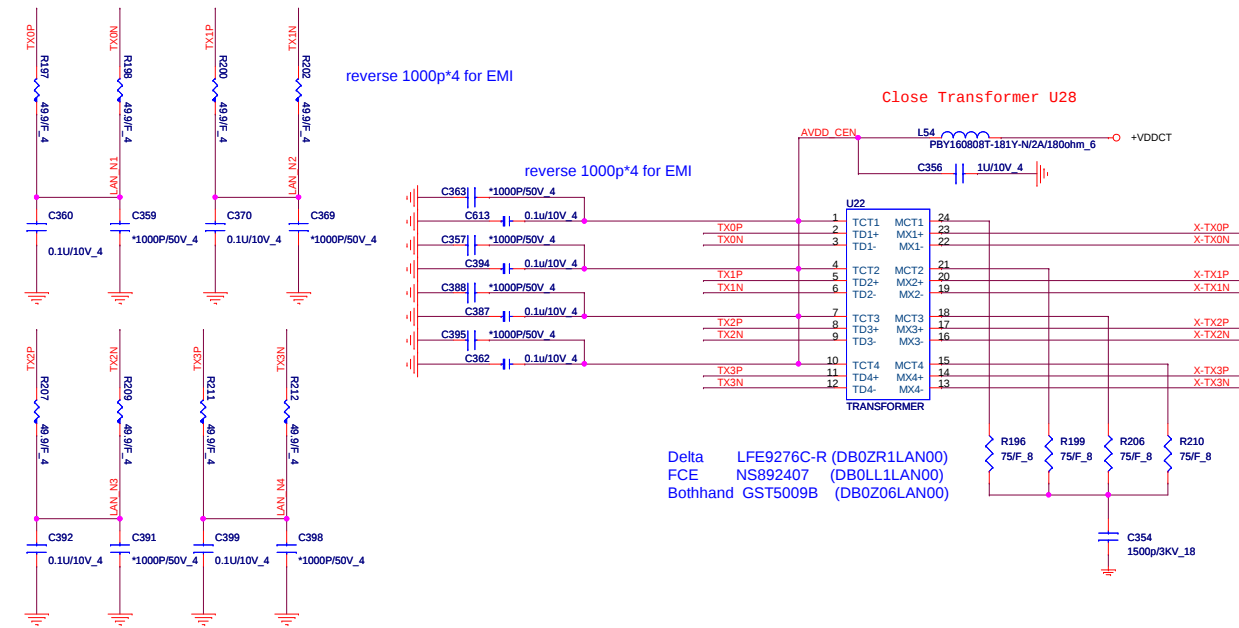
Size	Document Number	Rev
	HDMI	1A

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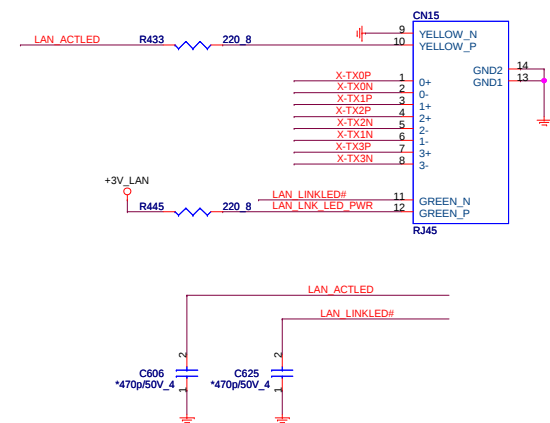
Giga-LAN AR8151



TRANSFORMER(LAN)



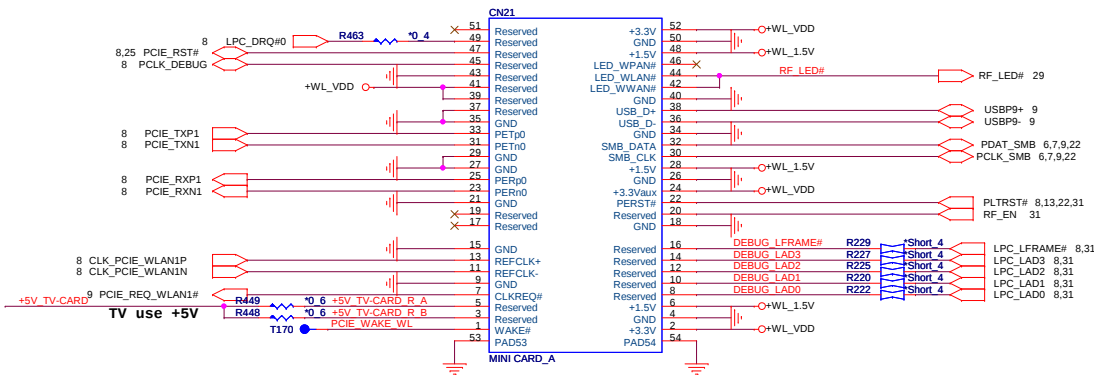
RJ45(LAN)



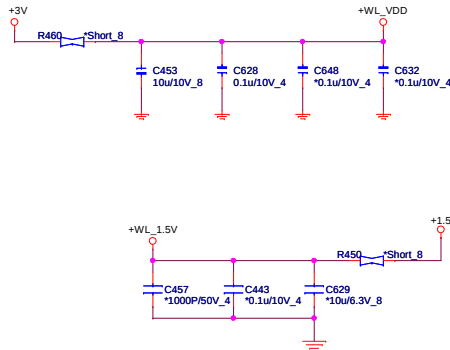
MINI-CARD WLAN(MPC)

Check LED signal. (active high or low)

+3.3V: 1000mA
+3.3Vaux: 330mA
+1.5V: 500mA



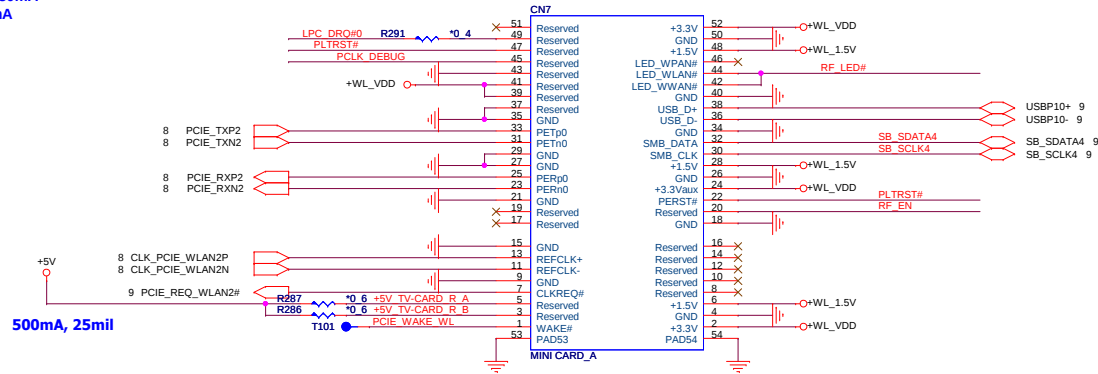
Debug



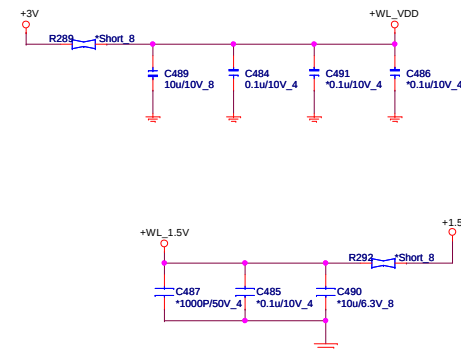
MINI-CARD WLAN(MPC)

Check LED signal. (active high or low)

+3.3V: 1000mA
+3.3Vaux: 330mA
+1.5V: 500mA

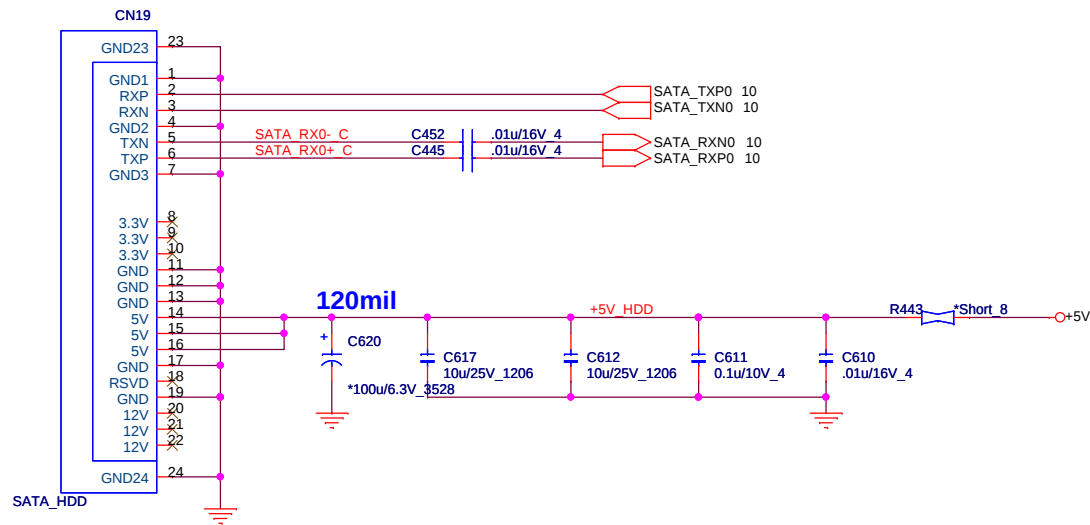


500mA, 25mil

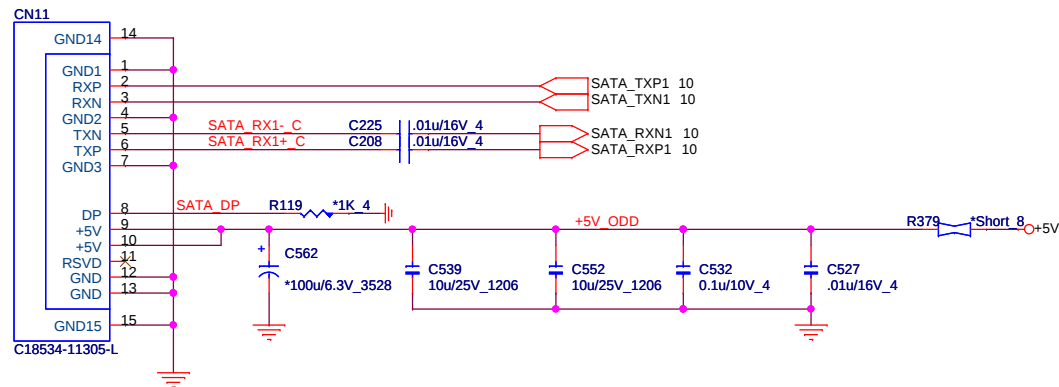


SATA HDD

27



SATA ODD



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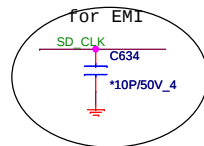
Size	Document Number	Rev
	SATA-HDD/ODD/HOLE	1A

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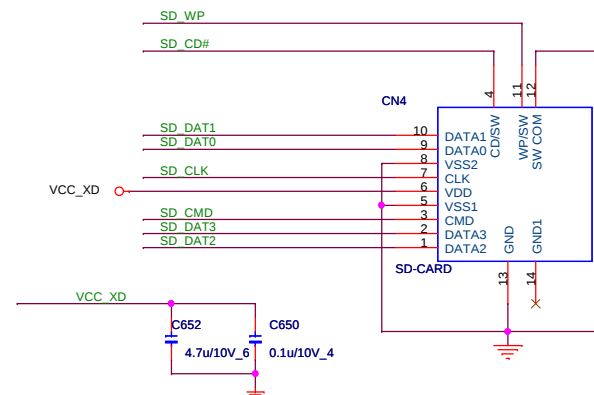
CARD READER Controller

2 IN 1 CARD READER (MMC)

30

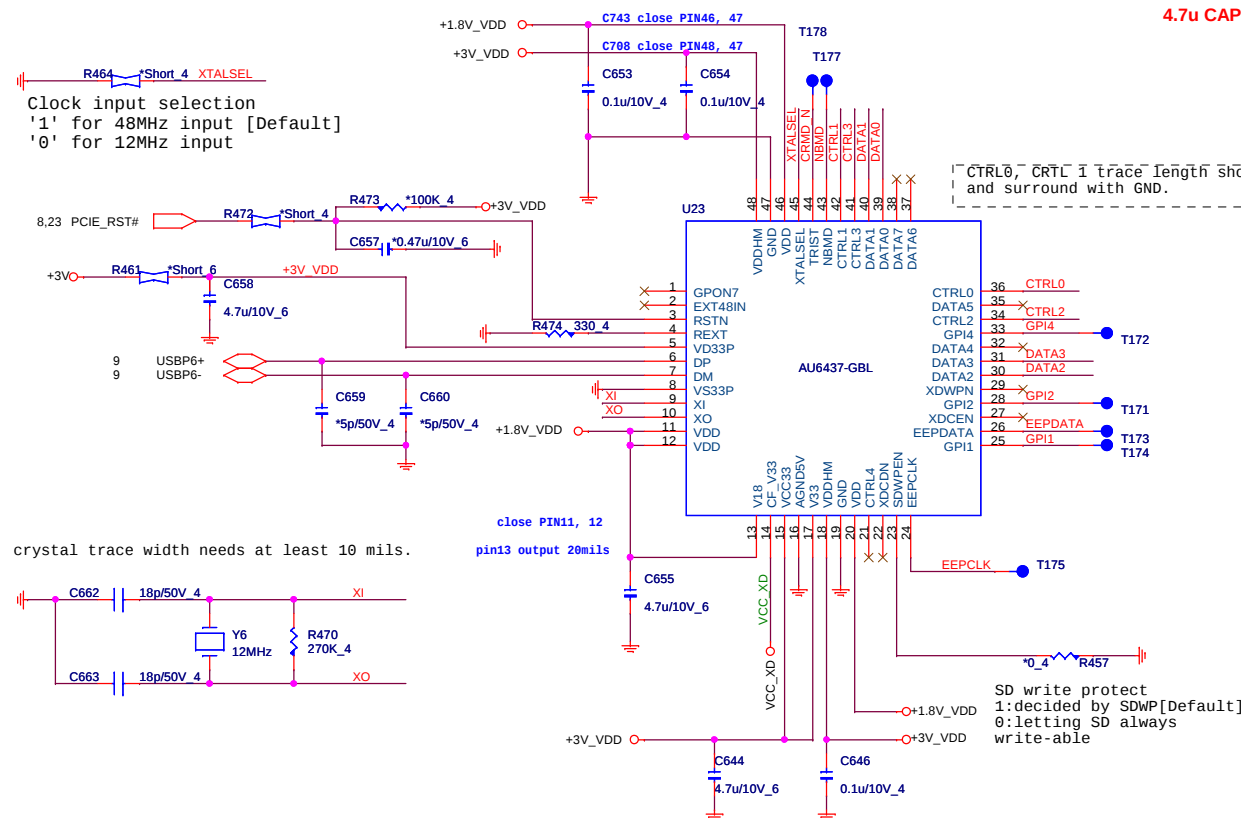


Main	DFHS11FR011
Second	DFHS11FR033

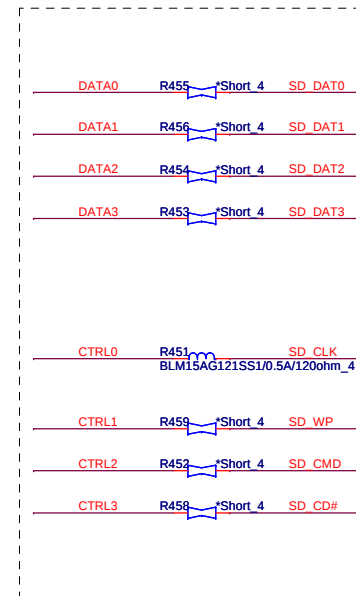


Close to CNxx pin 14 & pin23
4.7u CAP close to pin23

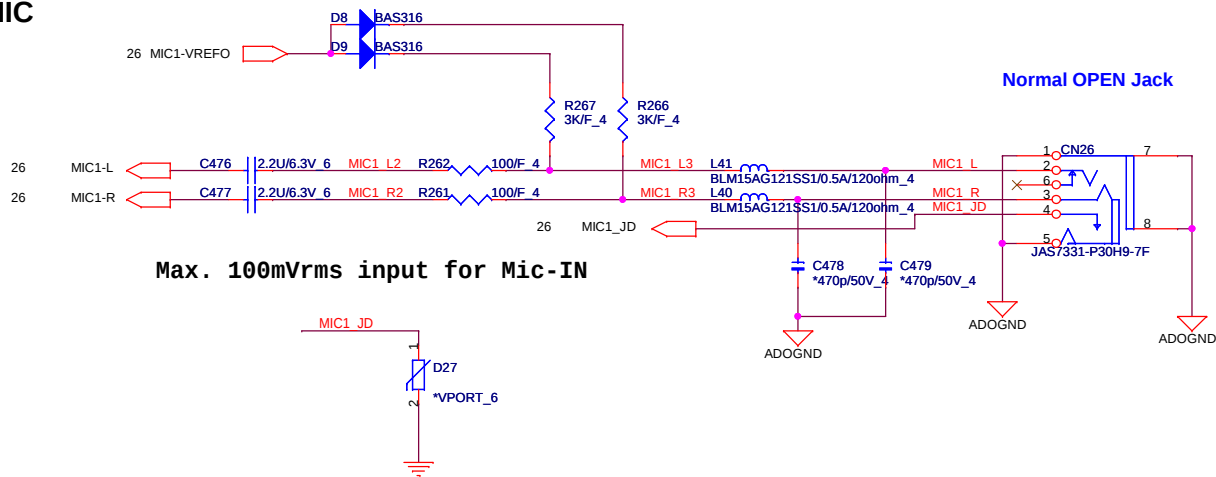
5/10 change Card Redaer conn
footpirnt sdcard-sdsn09-08-xa-11p-smt



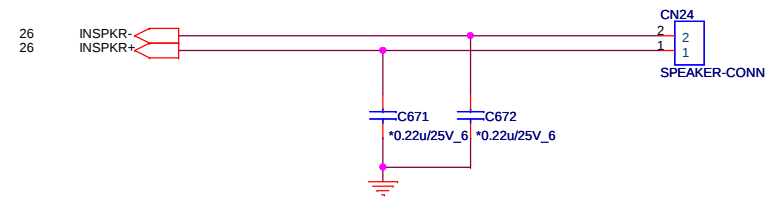
CTRL0, CTRL1 trace length shorter,
and surround with GND.



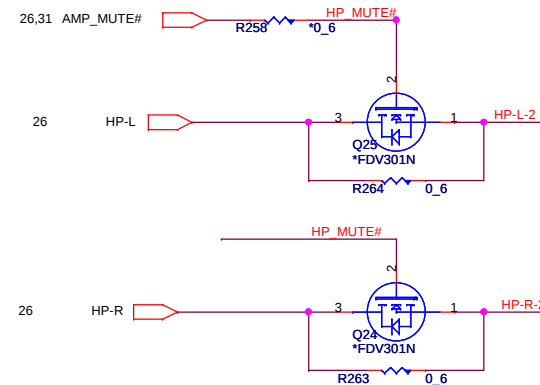
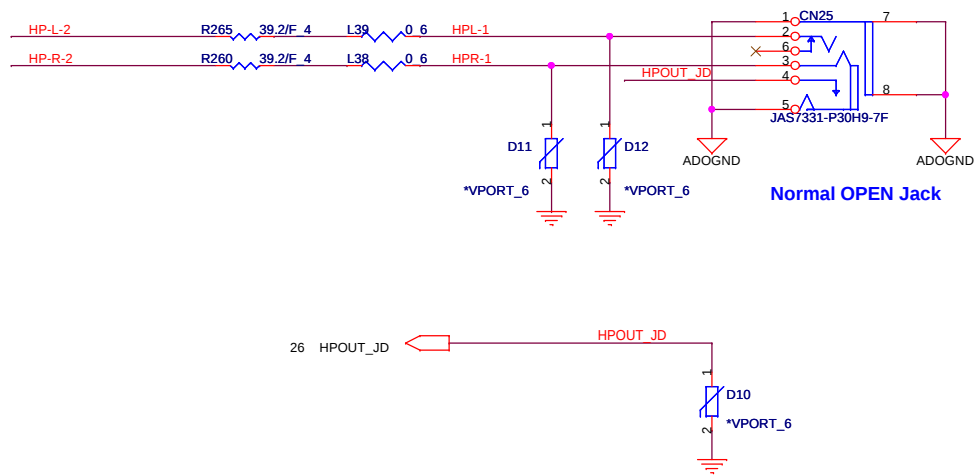
MIC



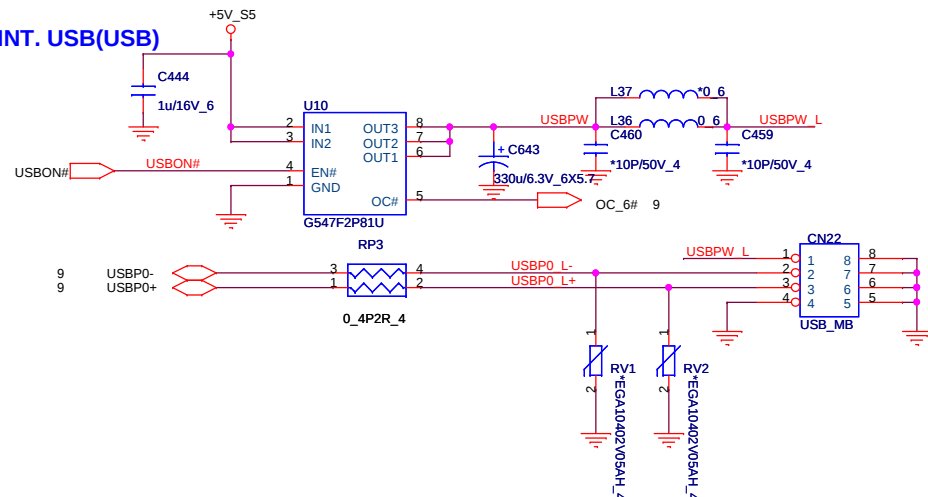
Internal Speaker



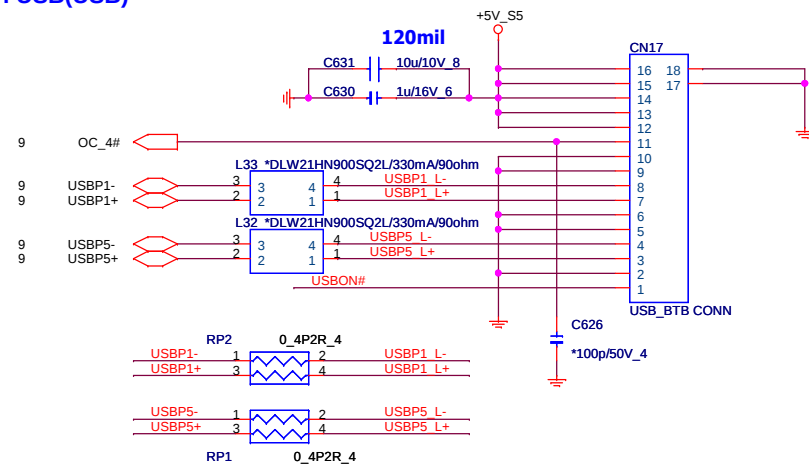
HP



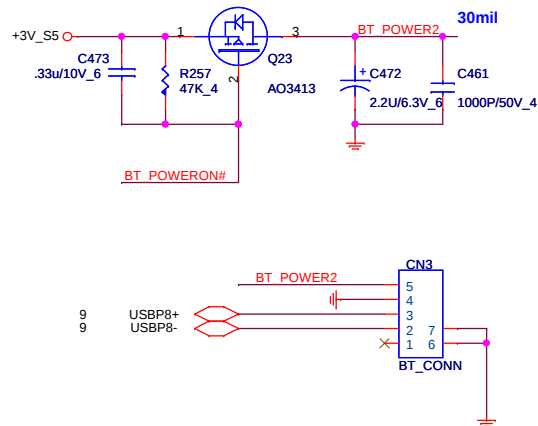
INT. USB(USB)



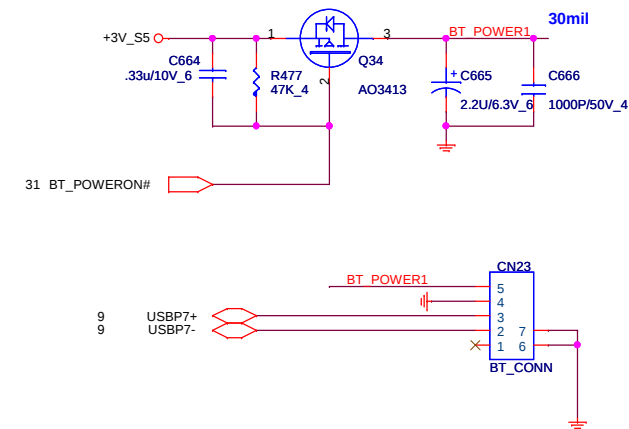
EXT. USB(USB)



BLUETOOTH V2.1 CONN(BTM)



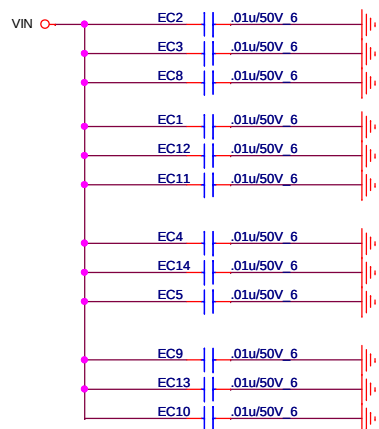
BLUETOOTH V3.0 CONN(BTM)



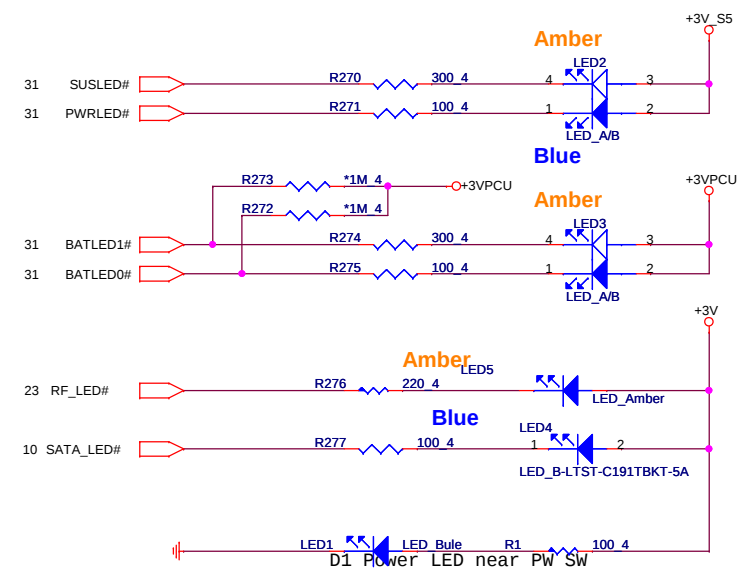
Quanta Computer Inc.
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	USB/BT	1A
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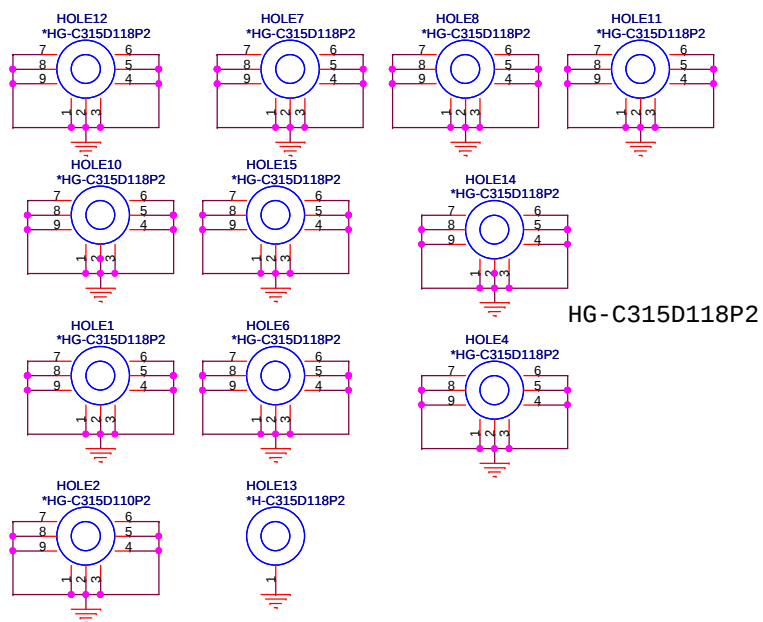
EE RETURN-PATH CAPACITORS(EMC)



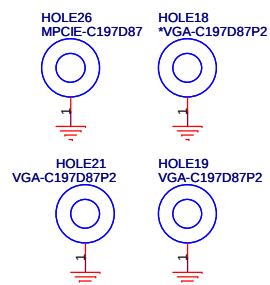
LED(UIF)



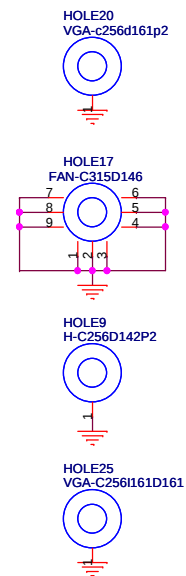
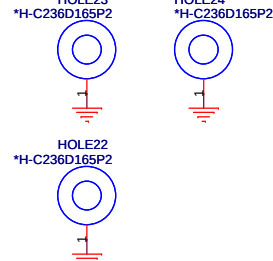
HOLE(OTH)



mini PCI



cpu

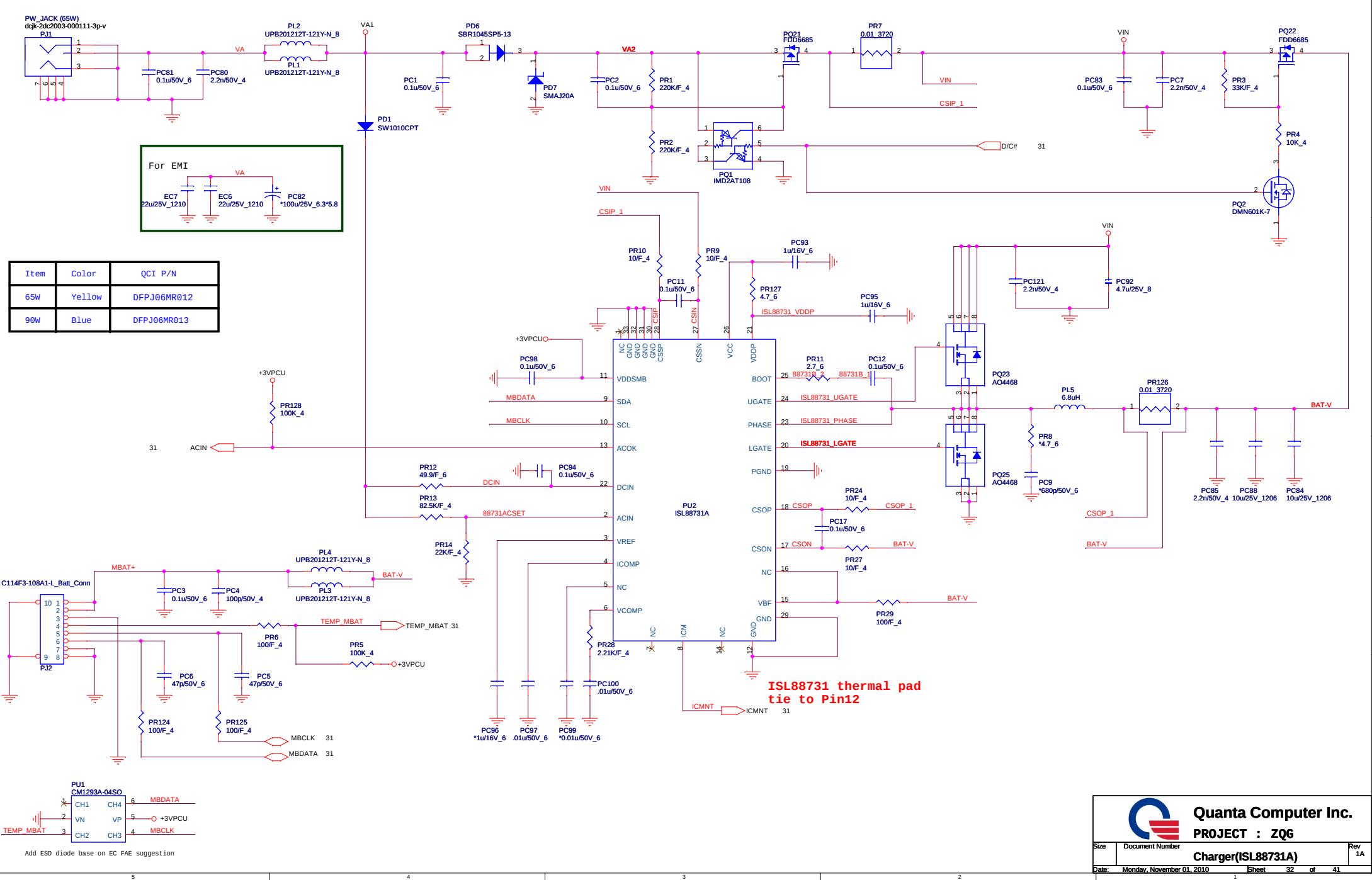


CPU nut PN : FBBU1001010 x 3 @ SHOLE1~3



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	29 -- LED/ EMI/ Screw Hole& Nut	1A
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Item	Color	QCI P/N
65W	Yellow	DFPJ06MR012
90W	Blue	DFPJ06MR013

PU1 CM1293A-04SO	
CH1	CH4
CH2	CH3
VP	VP
VP	VP

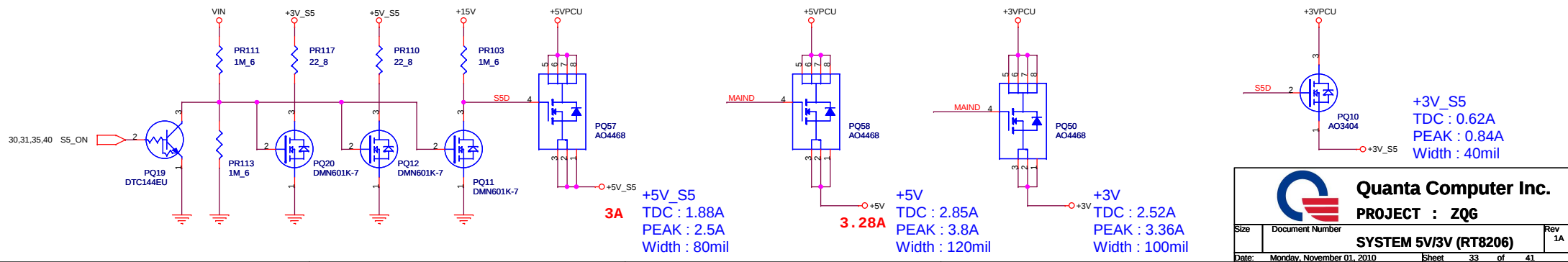
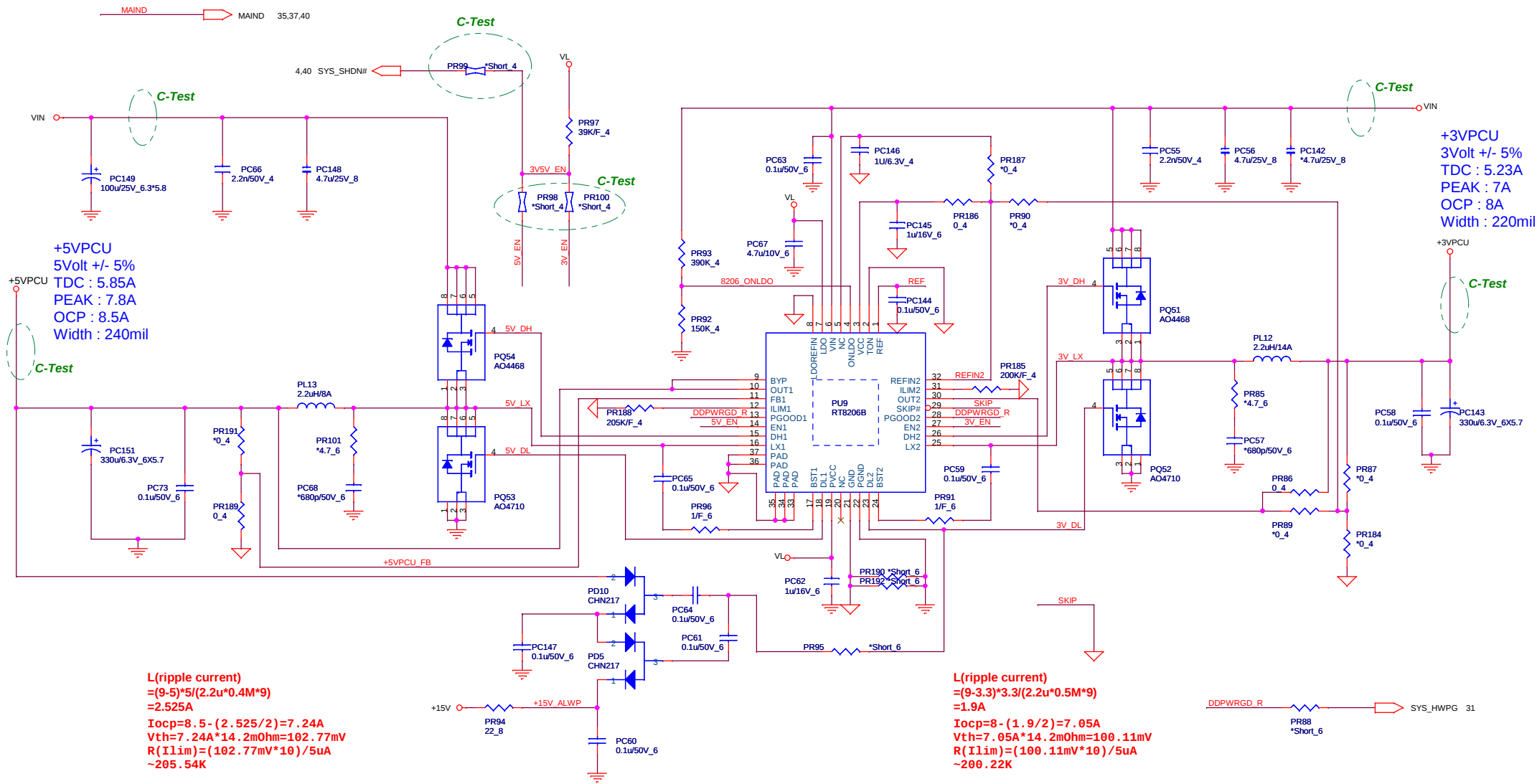


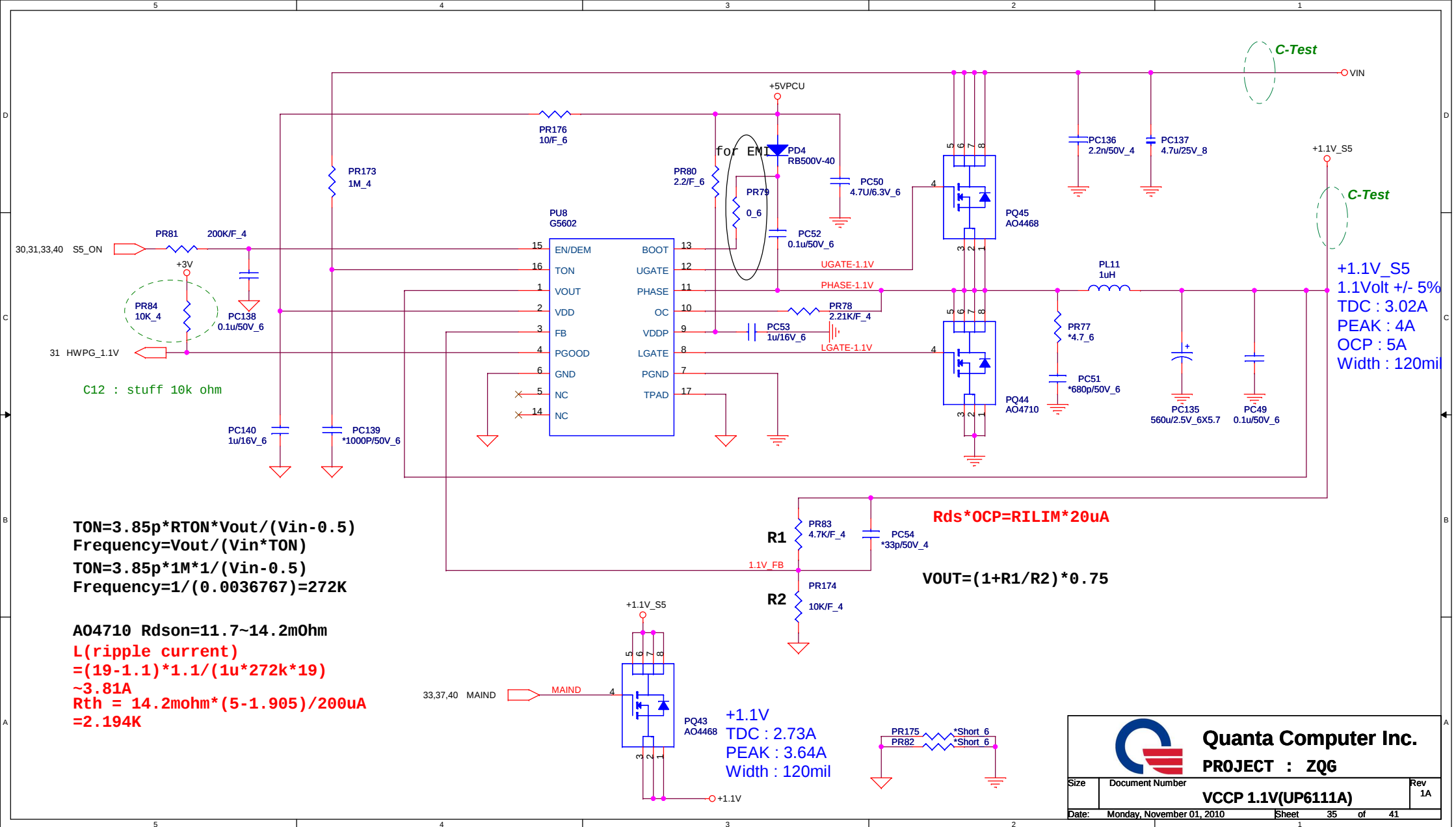
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Charger(ISL88731A)

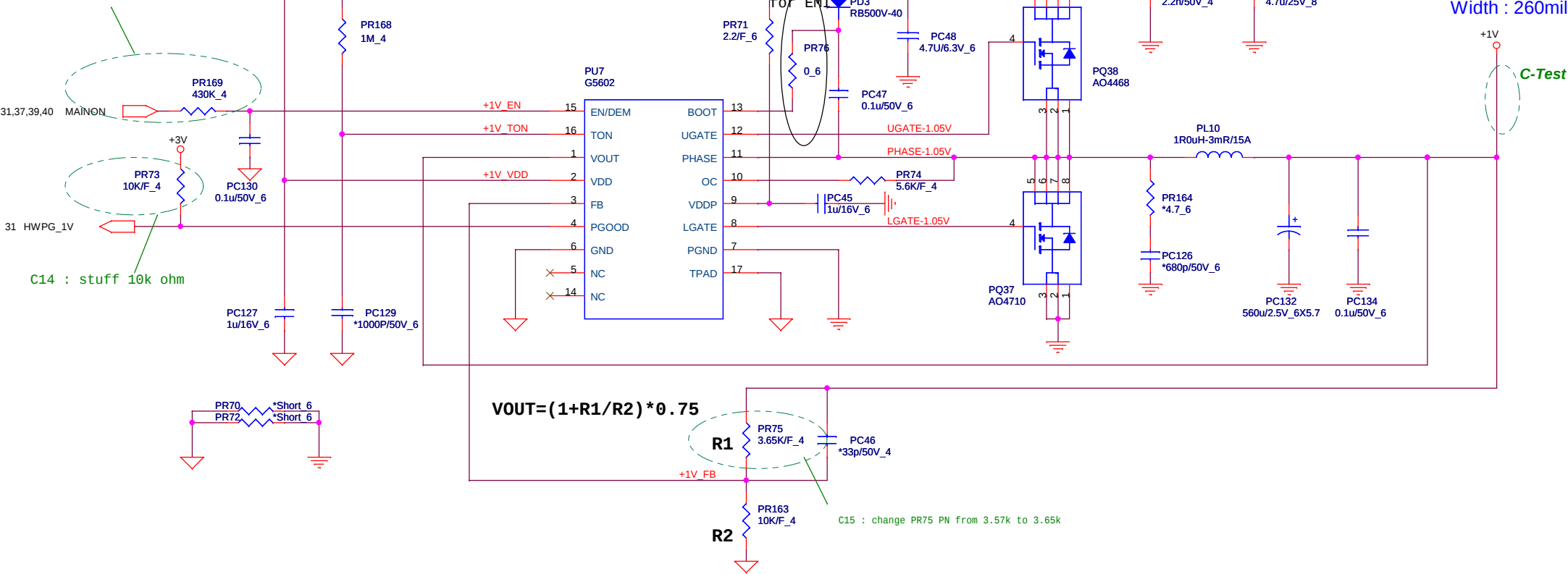
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C13

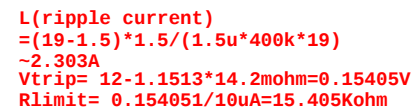
change PR169 PN from 0ohm to 430kohm for timing issue



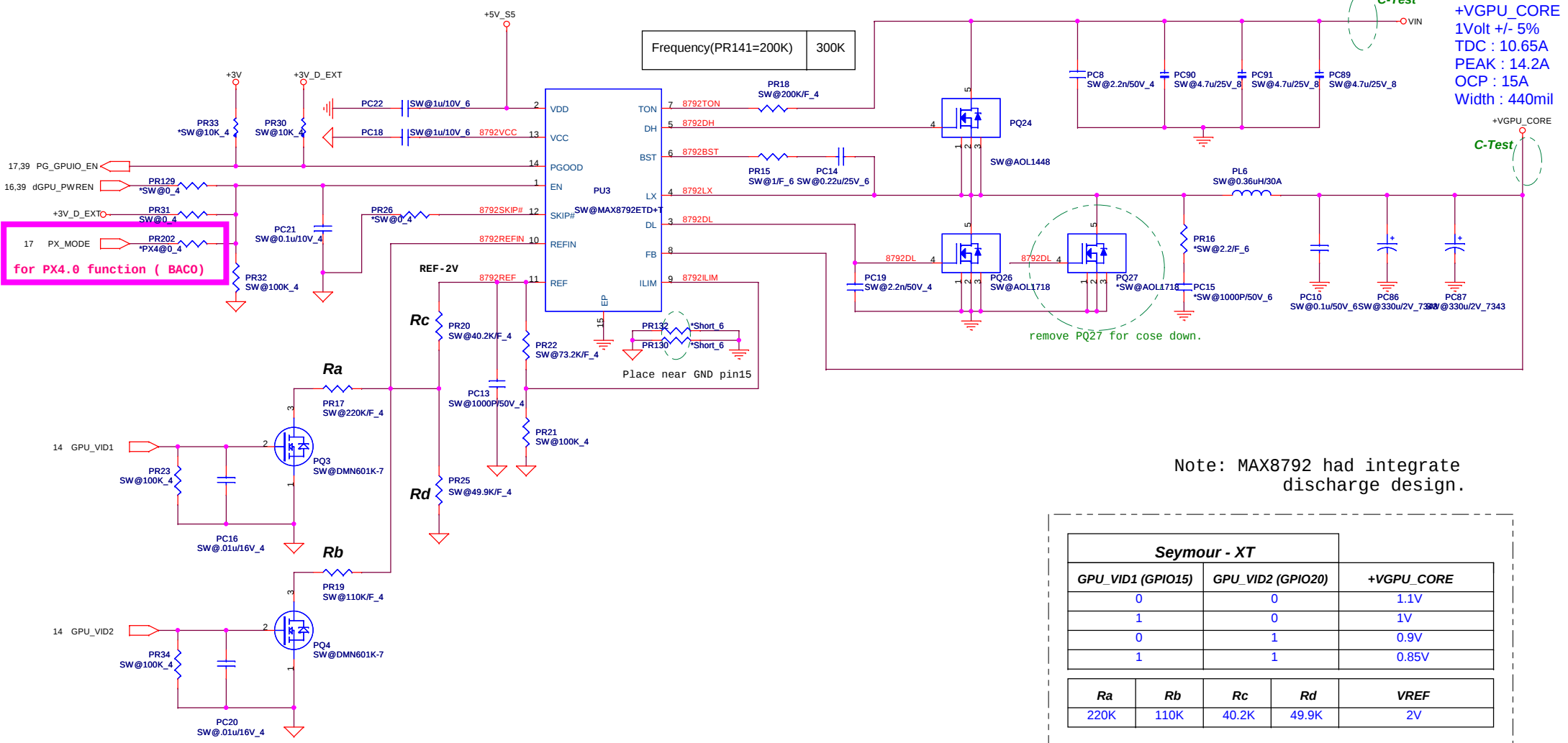
$$\begin{aligned} \text{TON} &= 3.85\text{p} \cdot \text{RTON} \cdot \text{Vout} / (\text{Vin} - 0.5) \\ \text{Frequency} &= \text{Vout} / (\text{Vin} \cdot \text{TON}) \\ \text{TON} &= 3.85\text{p} \cdot 1\text{M} \cdot 1 / (\text{Vin} - 0.5) \\ \text{Frequency} &= 1 / (0.0036767) = 272\text{K} \end{aligned}$$

$$\begin{aligned} \text{A04710 } \text{Rdson} &= 11.7 \sim 14.2\text{m}\Omega \\ \text{L(ripple current)} &= (19-1) \cdot 1 / (1\mu \cdot 272\text{k} \cdot 19) \\ &\sim 3.483\text{A} \\ \text{Rth} &= 14.2\text{m}\Omega \cdot (10-1.741) / 20\mu\text{A} \\ &= 5.863\text{K}\Omega \end{aligned}$$

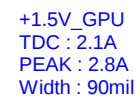
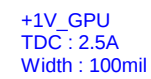
+SMDDR_VREF
TDC : 0.08A
PEAK : 0.1A
Width : 10mil



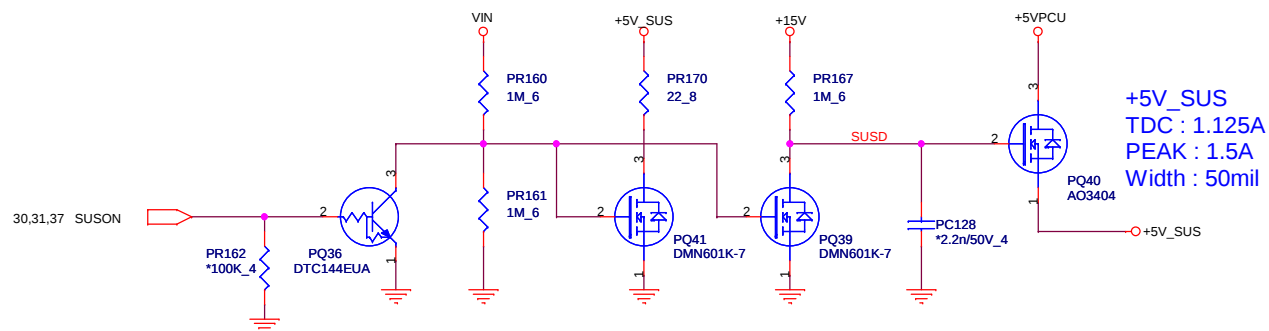
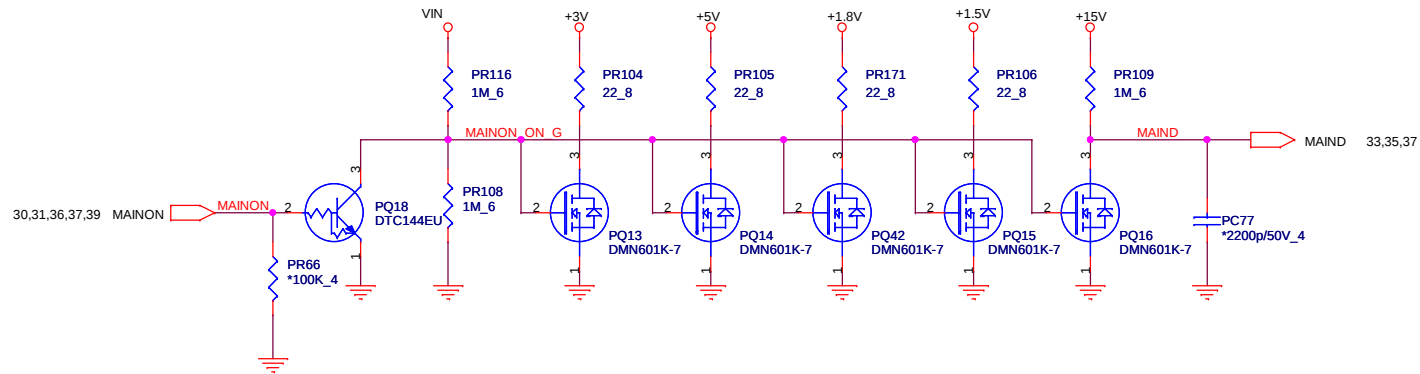
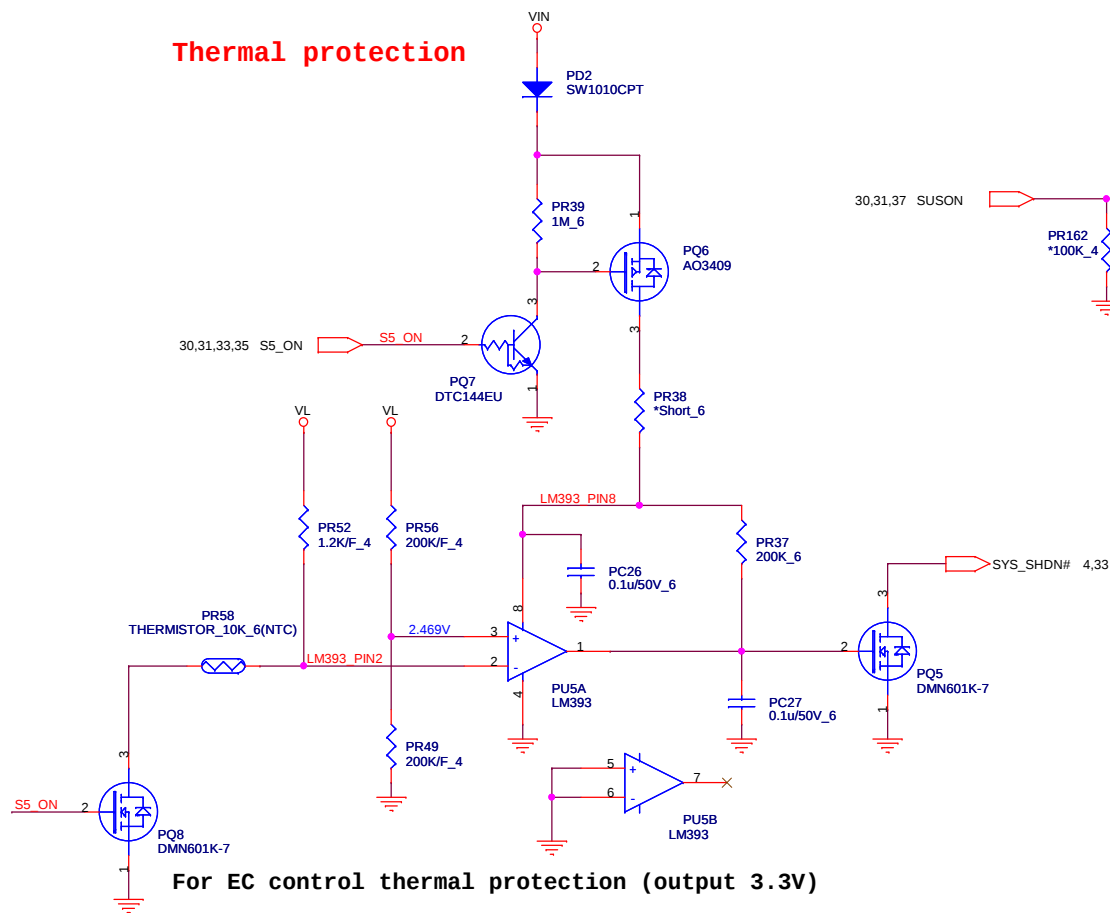
	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF



Ra --> 220K/F_4 (CS42202FB01) Rb --> 110K/F_4 (CS41102FB13)
 Rc --> 40.2K/F_4 (CS34022FB15) Rd --> 49.9K/F_4 (CS34992FB10)



Thermal protection



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Discharge /Thermal protection

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MODEL	REV	CHANGE LIST	Model ZQE/G M/B BOARD		
			Page	From	To
ZQE/G M/B	3A	C01	1	1A	3A
		C02 PAGE18 : to slove the Power DVD issue , setting size to 256MB	2	1A	3A
		C03 PAGE39 : add PR210,PC157,PQ61,PR198,PR200,PR199,PQ60,PC156,PQ69 for GPU +1V power source .	3	1A	3A
		changed control net from HWPG_1V to PG_GPUIO_EN	4	1A	3A
		C04 PAGE13 : change the power source from +1V to +1V_GPU	5	1A	3A
		C05 PAGE14 : change the power source from +1V to +1V_GPU	6	1A	3A
		C06 PAGE16 : change the power source from +1V to +1V_GPU	7	1A	3A
		C07 PAGE17 : change the power source from +1V to +1V_GPU	8	1A	3A
		C08 PAGE18 : to solve the HDMI issue , remove R112,R118 from BOMs	9	1A	3A
		C09 PAGE21 : Del D26 to slove HDMI issue.	10	1A	3A
		C10 PAGE26 : net PCBEEP connects with U11 by 10k ohm for AC pulg in /out function.	11	1A	3A
		C11 PAGE31 : Both MXM_SMCLK12 / MXM_SMDATA12 should be pull up to +3V by 10k ohm.	12	1A	3A
		C12 PAGE35 : stuff 10k ohm	13	1A	3A
		C13 PAGE36 : change PR169 PN from 0 ohm to 430K ohm for timing issue.	14	1A	3A
		C14 PAGE36 : stuff 10k ohm	15	1A	3A
		C15 PAGE36 : change PR75 PN from 3.57k to 3.65k	16	1A	3A
		C16 PAGE38 : remove PQ27 for cose down.	17	1A	3A
		C17 PAGE38 : remove PQ27 for cose down.	18	1A	3A
		C18 PAGE5 : Add C674 to reduce CRT noise.	19	1A	3A
		C19 PAGE5 : del R100 , add L58 to reduce CRT noise.	20	1A	3A
			21	1A	3A
			22	1A	3A
			23	1A	3A
			24	1A	3A
			25	1A	3A
			26	1A	3A
			27	1A	3A
			28	1A	3A
			29	1A	3A
			30	1A	3A
			31	1A	3A
			32	1A	3A
			33	1A	3A
			34	1A	3A
			35	1A	3A
			36	1A	3A
			37	1A	3A
			38	1A	3A
			39	1A	3A
			40	1A	3A
			41	1A	3A
		Note :			
		1. Remove Jumper : JP7,JP11,JP1,JP2,JP3,JP4,JP5,JP6,JP8,JP9,JP10,JP12,JP13,JP14,JP15,JP16,JP17,JP18			
		 Quanta Computer Inc. PROJECT : ZQG Size Document Number Rev 1A CHANGE LIST - 3A Date: Monday, November 01, 2010 Sheet 41 of 41			
Quanta Computer Inc. ZQE/G		PROJECT: ZQE/G	PCBA NO.	REV: 3A	DOC. NO :
		APPROVED BY : Johnny O	CHECK BY : Darren Liao	DRAWING BY : Kenneth Huang	DATE :10/18/2010 SHEET 1