ZQ5 SYSTEM BLOCK DIAGRAM

BOM MARK
IV@: INT VGA
EV@: STUFF FOR EXT VGA
SP@: STUFF FOR UMA or VGA

REV:B

X'TAL 14.318MHz
CLOCK GENERATOR
ICS:
SELGO: SLG8SP513VTR
P2

Penryn 478
uFCPGA
P3, P4

Thermal Sensor
(G780P81U) P3

Fan Driver
(G991) P25

FSB
667/800/1067 Mhz

DDR3 PWR TPS51116 P40
CHARGER ISL88731A P36
THERMAL PROTECTION P44
3/5V SYS PWR RT8206 P37
DISCHARGER P42
CPU CORE PWR ISL6266A P39
VGA CORE MAX8792 P41
+1.05V UP6111A P38

ATI-Park
VRAM DDRIII 512MB P18-P23

PCIE 16X
EXT_LVDS
EXT_CRT
EXT_HDMI

SWITCH CIRCUIT P25
CRT P24
LVDS P24
HDMI P25
HDMI switch (PS8101T) P25

DDRIII
SO-DIMM 0
SO-DIMM 1
P16,P17

Dual Channel DDR3
667/800 MHz

NB Cantiga
(GM45/ PM45/ GL40)
P5, P6, P7, P8, P9, P10, P11

LVDS
RGB
INT_LVDS
INT_CRT
INT_HDMI

X4 DMI interface

HDD (SATA) *1 P26
ODD (SATA) P26

SATA0
SATA1

Ext USB Port x 2 USB 0,2 P27
Int USB Port x 1 USB 6 P27
Bluetooth USB3 P27
CCD USB11 P24

USB 2.0

SB ICH9M
P12,P13,P14,P15

X'TAL 32.768KHz

PCI-Express
PCIE-4
Mini Card WLAN P27

USB1
PCIE-6
X'TAL 25MHz

Media Cardreader (AU6437) USB2 P30
Giga-LAN BCM57780 P30

Azalia
LPC

Audio CODEC (272) P28

EC (WPC781) P33
X'TAL 32.768KHz

SPI ROM P33
Touch Pad P26
K/B COON. P33

Card Reader Connector P32
Transformer P31
RJ45 P31

Audio Amplifier G1453L P28
MIC Jack P29
Int. MIC P29
Int. Speaker P29

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Clock Generator(CLK)

02

Modfiy it 5/4

5/7 Modfiy

5/5 Add

5/5 modify

SLG8SP513VTR ,ICS9LPRS365BKLFT

	ICS9LRS3165BKLFT (ALPRS365000)	RTM875T-606 (AL000875000)	PULL HIGH	PULL DOWN
Pin 11	PCI2/TME	PCI2/TME internal PD	NO OVERCLOCKING (default)	NORMAL RUN
Pin 12	PCI-3	PCI-3/SRC5_EN internal PD	PIN37/38 IS SRC5	PIN37/38 IS PCI_STOP/CPU_STOP (default)
Pin 13	PCI-4/27M_SEL	PCI-4/27M_SEL internal PD	PIN 17/18 IS 27MHz	PIN 17/18 IS SRC/DOT (default)
Pin 14	PCIF-5/ITP_EN	PCIF-5/ITP_EN internal PD	PIN 46/47 IS CPUITP	PIN 46/47 IS SRC8 (default)

Frequence select

SEL2	SEL1	SEL0	CPU	SRC	PCI	
1	0	1	100	100	33	
0	0	1	133	100	33	Default
0	1	1	166	100	33	
0	1	0	200	100	33	
0	0	0	266	100	33	
1	0	0	333	100	33	
1	1	0	400	100	33	
1	1	1	Reserved			

5/22 modify

Clock Gen I2C

<MAIN>:ICS9LRS3165BKLFT QCI:ALPRS365000
<SECOND>:SLG8SP513VTR QCI:AL8SP513000
<SECOND>:RTM875N-606-VD-GRT QCI:AL000875000

REV:B 6/12

REV:B 6/11

PROJECT : ZQ5
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Size	Document Number	Rev
	CLOCK GENERATOR	1A
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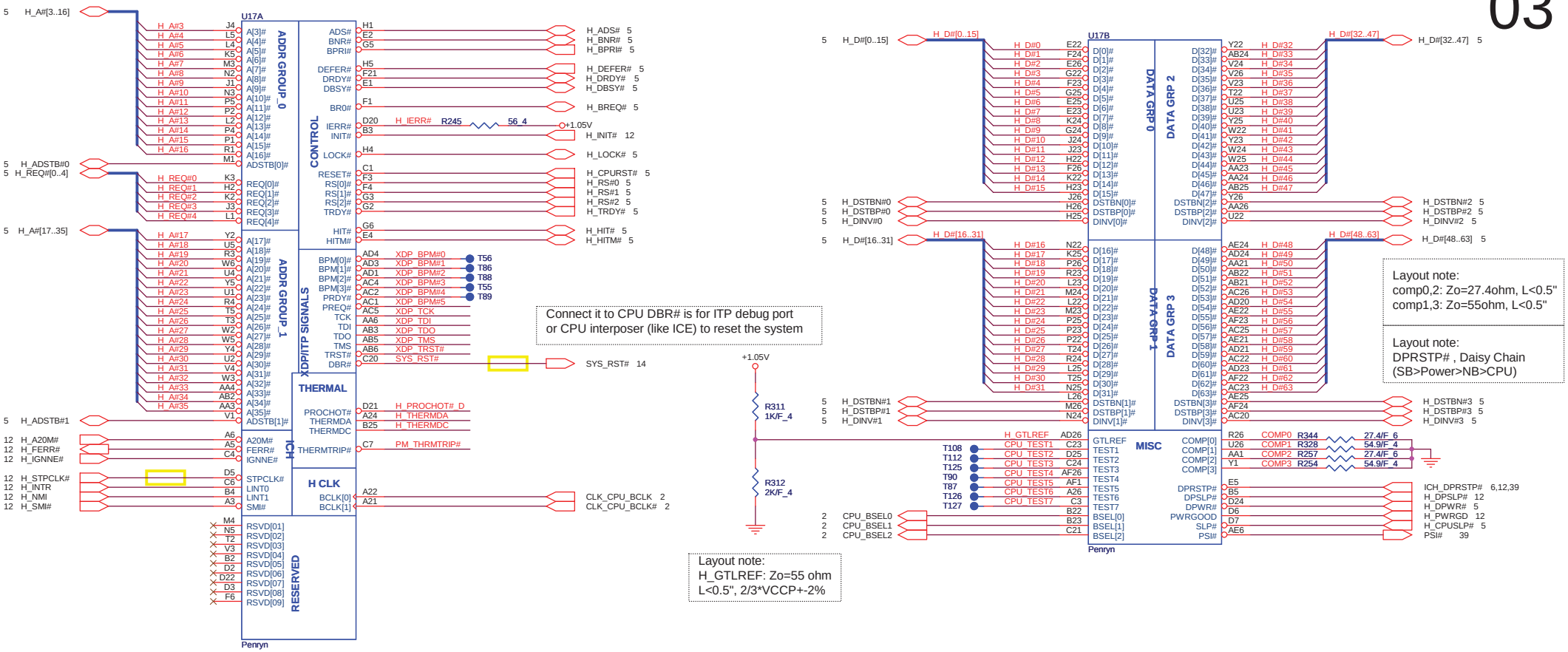
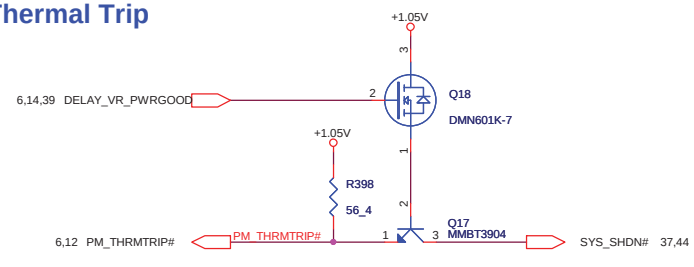
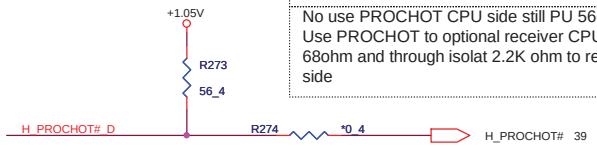


Thermal Trip



Processor hot

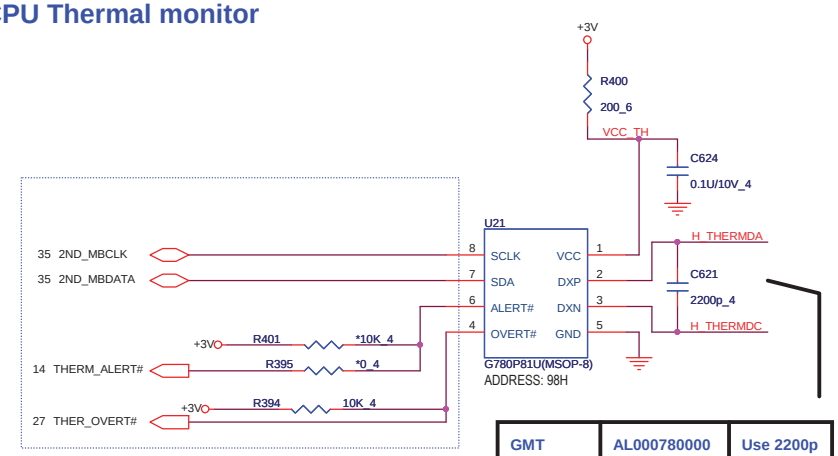


No use Thermal trip CPU side still PU 56ohm.
Use Thermal trip can share PU at SB side

No use PROCHOT CPU side still PU 56ohm.
Use PROCHOT to optional receiver CPU side PU 68ohm and through isolat 2.2K ohm to receiver side

CPU 1/2

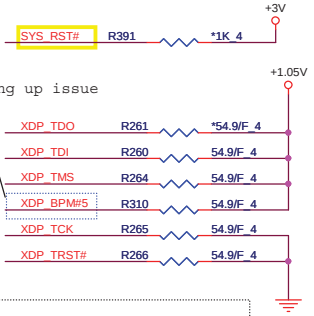
CPU Thermal monitor



4/20 Modify

GMT	AL000780000	Use 2200p
NS	AL095245000	Use 2200p
WINDBOND	AL83L771K01	Use 2200p

XDP PU/PD



XDP_DBRESET# and XDP_TDO reserve for XDP

PROJECT : ZQ5
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	CPU Host Bus	1A
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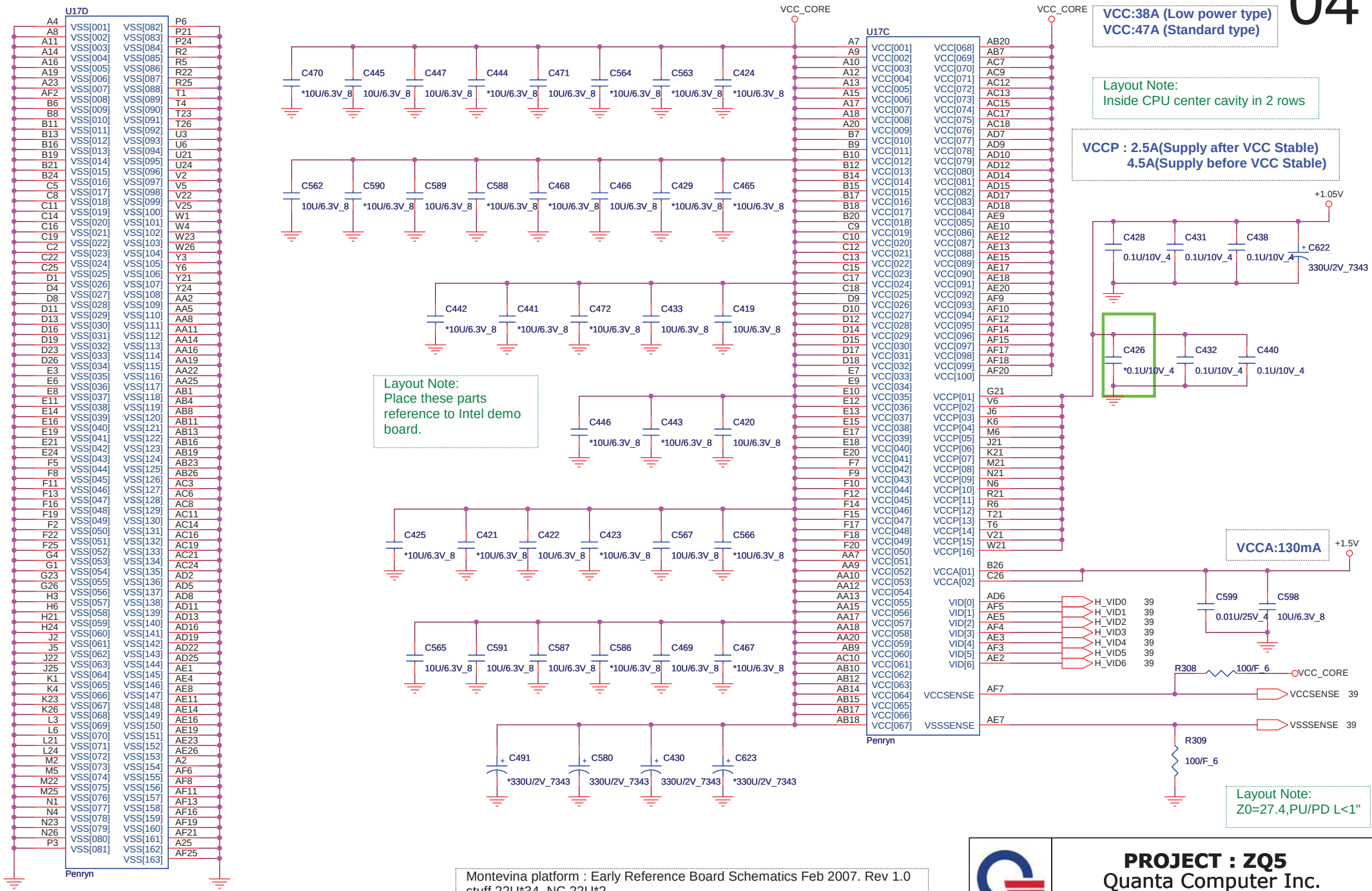
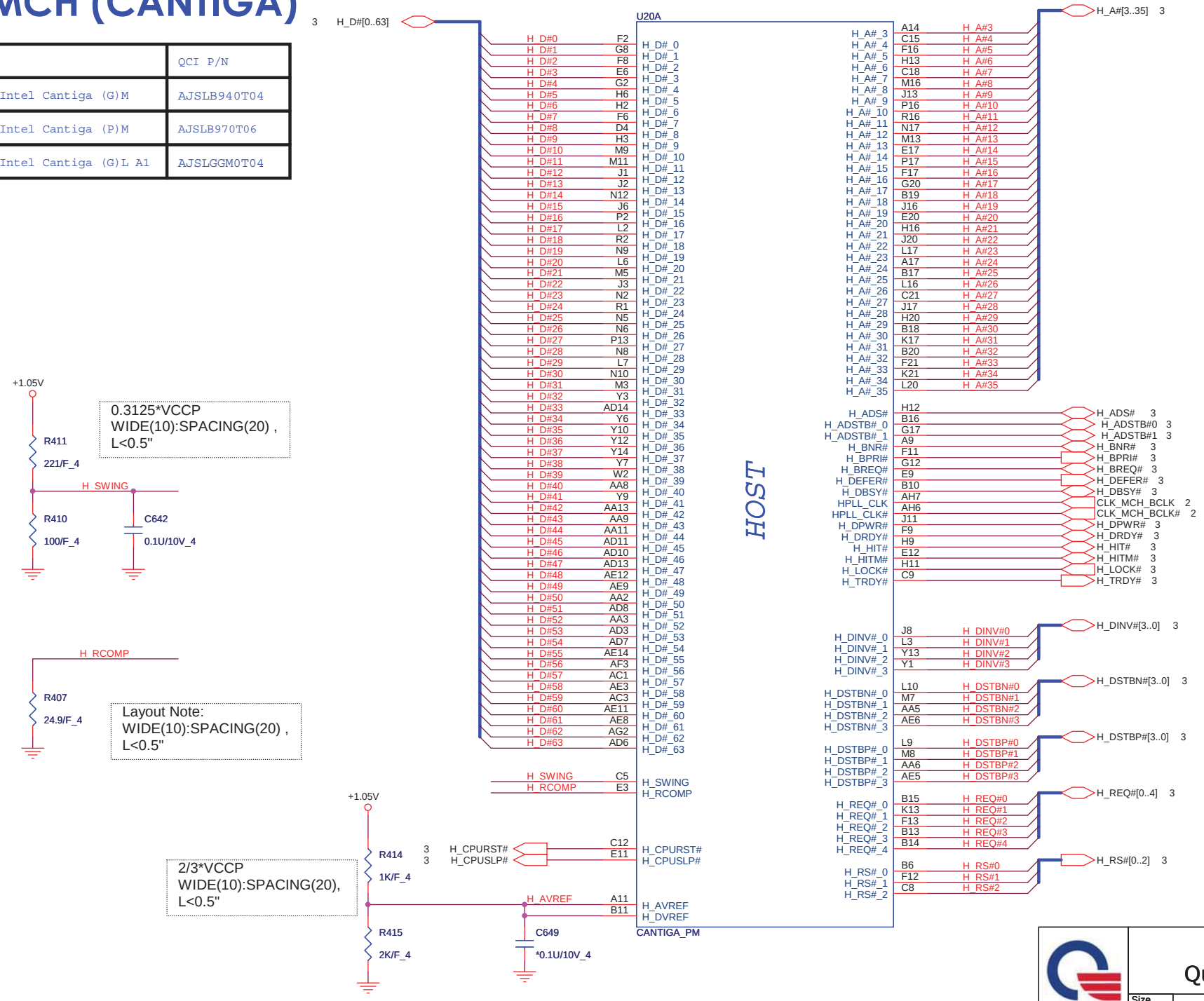

04
U17D
U17C
VCC_CORE
VCC:38A (Low power type)
VCC:47A (Standard type)
Layout Note:
Inside CPU center cavity in 2 rows
VCCP : 2.5A(Supply after VCC Stable)
4.5A(Supply before VCC Stable)
+1.05V
Layout Note:
Place these parts
reference to Intel demo
board.
VCCA:130mA
+1.5V
Layout Note:
Z0=27.4,PU/PD L<1"
Penryn
CPU 2/2
Montevina platform : Early Reference Board Schematics Feb 2007. Rev 1.0
stuff 22U*34, NC 22U*2
stuff 330U*2, NC330U*2
PROJECT : ZQ5
Quanta Computer Inc.
CPU Power
Monday, July 12, 2010
http://laptop-motherboard-schematic.blogspot.com/

GMCH (CANTIGA)

05

	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06
Intel Cantiga (G)L A1	AJSLGGM0T04



PROJECT : ZQ5
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	GMCH HOST	1A
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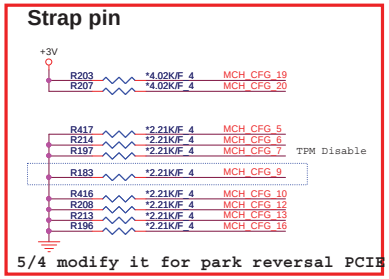
IV@
EV@

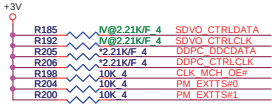
06

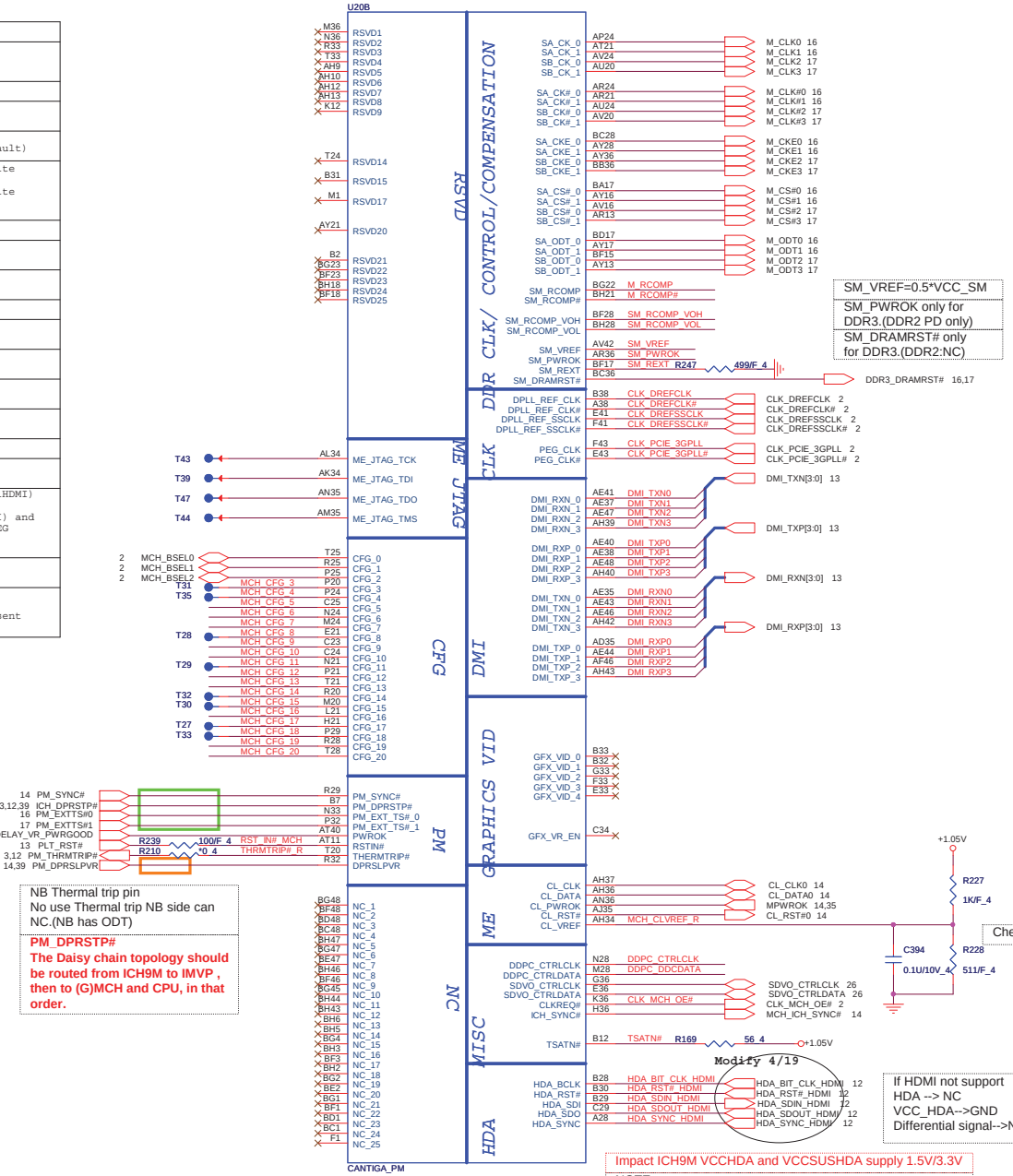
Strap table

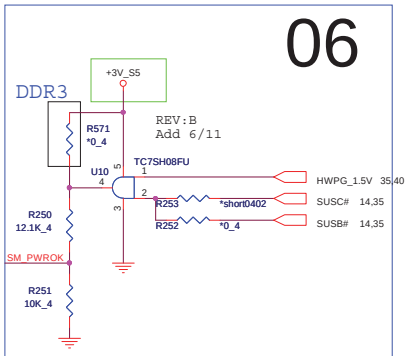
Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000= FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

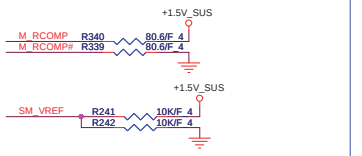
Strap pin

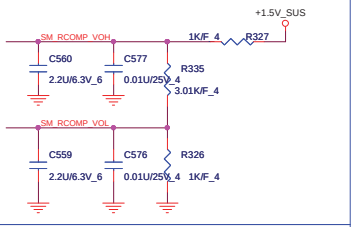












IV@

EV@ **IV&EV Dis/Enable setting**

If LVDS no use,all signal can NC

SP@

07

U20C

L<0.5" , If PCIE not support still connect to +VCC_PEG

+1.05V

T37 EXP_A_COMPX R209 49.9/F_4

T36

PEG_COMPI

PEG_COMPO

25 L_BKLT_CTRL L32 L_BKLT_CTRL

25 INT_LVDS_BLON G32 L_BKLT_EN

R201 IV@10K_4 L_CTRL_CLK M32 L_CTRL_CLK

+3V

R199 IV@10K_4 L_CTRL_DATA M33 L_CTRL_DATA

25 INT_LVDS_EDIDCLK K33 L_DDC_CLK

25 INT_LVDS_EDIDDATA J33 L_DDC_DATA

M29

25 INT_LVDS_DIGON R188 IV@2.37K/F_4 C44 L_VDD_EN

B43 LVDS_IBG

E37 LVDS_VBG

E38 LVDS_VREFH

LVDS_VREFL

25 INT_TXLCLKOUT- INT_TXLCLKOUT- C41 LVDSA_CLK#

25 INT_TXLCLKOUT+ INT_TXLCLKOUT+ C40 LVDSA_CLK

B37 LVDSB_CLK#

A37 LVDSB_CLK

25 INT_TXLOUT0- INT_TXLOUT0- H47 LVDSA_DATA#_0

25 INT_TXLOUT1- INT_TXLOUT1- E46 LVDSA_DATA#_1

25 INT_TXLOUT2- INT_TXLOUT2- G40 LVDSA_DATA#_2

A40 LVDSA_DATA#_3

25 INT_TXLOUT0+ INT_TXLOUT0+ H48 LVDSA_DATA_0

25 INT_TXLOUT1+ INT_TXLOUT1+ D45 LVDSA_DATA_1

25 INT_TXLOUT2+ INT_TXLOUT2+ F40 LVDSA_DATA_2

B40 LVDSA_DATA_3

A41 LVDSB_DATA#_0

H38 LVDSB_DATA#_1

G37 LVDSB_DATA#_2

J37 LVDSB_DATA#_3

B42 LVDSB_DATA_0

G38 LVDSB_DATA_1

F37 LVDSB_DATA_2

K37 LVDSB_DATA_3

SP@ **TV_A/B/C**
For IV: 75ohm
For EV:0ohm

R189 SP@75_4 INT_TV_COMP F25 TVA_DAC

R195 SP@75_4 INT_TV_Y/G H25 TVB_DAC

R194 SP@75_4 INT_TV_C/R K25 TVC_DAC

H24 TV_RTN

C31 TV_DCONSEL_0

E32 TV_DCONSEL_1

25 INT_CRT_BLU INT_CRT_BLU E28 CRT_BLUE

25 INT_CRT_GRN INT_CRT_GRN G28 CRT_GREEN

25 INT_CRT_RED INT_CRT_RED J28 CRT_RED

G29 CRT_IRTN

H32

J32 CRT_DDC_CLK

25 INT_CRT_DDCCLK J29 CRT_DDC_DATA

25 INT_CRT_DDCDAT E29 CRT_HSYNC

25 INT_HSYNC L29 CRT_TVO_IREF

25 INT_VSYNC CRT_VSYNC

R426 IV@24.9_4 HSYNC_G

CRTIREF

R425 IV@24.9_4 VSYNC_G

6/14 Modify
REV:B

HSYNC/VSYNC serial R place close to NB

CRTIREF pull down for IV cantiga 1k ohm/F

Discrete STUFFED.

HSYNC_G

VSYNC_G

R413 EV@0_4

R412 EV@0_4

CANTIGA_PM

PCI-EXPRESS GRAPHICS

SDVO

LVDS

PEG_RX#_0 H44 PEG_RXN0

PEG_RX#_1 J46 PEG_RXN1

PEG_RX#_2 L44 PEG_RXN2

PEG_RX#_3 L40 PEG_RXN3

PEG_RX#_4 N41 PEG_RXN4

PEG_RX#_5 P48 PEG_RXN5

PEG_RX#_6 N44 PEG_RXN6

PEG_RX#_7 T43 PEG_RXN7

PEG_RX#_8 U43 PEG_RXN8

PEG_RX#_9 Y43 PEG_RXN9

PEG_RX#_10 Y48 PEG_RXN10

PEG_RX#_11 Y36 PEG_RXN11

PEG_RX#_12 AA43 PEG_RXN12

PEG_RX#_13 AD37 PEG_RXN13

PEG_RX#_14 AC47 PEG_RXN14

PEG_RX#_15 AD39 PEG_RXN15

PEG_RXN[15:0] 18

Can support reversal routing.If CFG9=1, PCI Express is normal operation. If CFG9=0, then PEG_TXP0 becomes PEG_TXP15, PEG_TXP1 becomes PEG_TXP14, PEG_TXP2 becomes PEG_TXP13, etc. similarly for PEG_RXP[15:0] and PEG_RXN[15:0]

PEG_RX_0 H43 PEG_RXP0

PEG_RX_1 J44 PEG_RXP1

PEG_RX_2 L43 PEG_RXP2

PEG_RX_3 L41 PEG_RXP3

PEG_RX_4 N40 PEG_RXP4

PEG_RX_5 P47 PEG_RXP5

PEG_RX_6 N43 PEG_RXP6

PEG_RX_7 T42 PEG_RXP7

PEG_RX_8 U42 PEG_RXP8

PEG_RX_9 Y42 PEG_RXP9

PEG_RX_10 W47 PEG_RXP10

PEG_RX_11 Y37 PEG_RXP11

PEG_RX_12 AA42 PEG_RXP12

PEG_RX_13 AD36 PEG_RXP13

PEG_RX_14 AC48 PEG_RXP14

PEG_RX_15 AD40 PEG_RXP15

PEG_RXP[15:0] 18,26

PEG_TX#_0 J41 C_PEG_TXN0 C309 0.1U/10V_4 PEG_TXN0

PEG_TX#_1 M46 C_PEG_TXN1 C323 0.1U/10V_4 PEG_TXN1

PEG_TX#_2 M47 C_PEG_TXN2 C629 0.1U/10V_4 PEG_TXN2

PEG_TX#_3 M40 C_PEG_TXN3 C332 0.1U/10V_4 PEG_TXN3

PEG_TX#_4 M42 C_PEG_TXN4 C330 EV@.1U/10V_4 PEG_TXN4

PEG_TX#_5 R48 C_PEG_TXN5 C626 EV@.1U/10V_4 PEG_TXN5

PEG_TX#_6 N38 C_PEG_TXN6 C336 EV@.1U/10V_4 PEG_TXN6

PEG_TX#_7 T40 C_PEG_TXN7 C339 EV@.1U/10V_4 PEG_TXN7

PEG_TX#_8 U37 C_PEG_TXN8 C351 EV@.1U/10V_4 PEG_TXN8

PEG_TX#_9 U40 C_PEG_TXN9 C353 EV@.1U/10V_4 PEG_TXN9

PEG_TX#_10 Y40 C_PEG_TXN10 C356 EV@.1U/10V_4 PEG_TXN10

PEG_TX#_11 AA46 C_PEG_TXN11 C369 EV@.1U/10V_4 PEG_TXN11

PEG_TX#_12 AA37 C_PEG_TXN12 C376 EV@.1U/10V_4 PEG_TXN12

PEG_TX#_13 AA40 C_PEG_TXN13 C377 EV@.1U/10V_4 PEG_TXN13

PEG_TX#_14 AD43 C_PEG_TXN14 C391 EV@.1U/10V_4 PEG_TXN14

PEG_TX#_15 AC46 C_PEG_TXN15 C384 EV@.1U/10V_4 PEG_TXN15

PEG_TXN[15:0] 18,26

PEG_TX_0 J42 C_PEG_TXP0 C311 0.1U/10V_4 PEG_TXP0

PEG_TX_1 L46 C_PEG_TXP1 C318 0.1U/10V_4 PEG_TXP1

PEG_TX_2 M48 C_PEG_TXP2 C632 0.1U/10V_4 PEG_TXP2

PEG_TX_3 M39 C_PEG_TXP3 C334 0.1U/10V_4 PEG_TXP3

PEG_TX_4 M43 C_PEG_TXP4 C324 EV@.1U/10V_4 PEG_TXP4

PEG_TX_5 R47 C_PEG_TXP5 C627 EV@.1U/10V_4 PEG_TXP5

PEG_TX_6 N37 C_PEG_TXP6 C338 EV@.1U/10V_4 PEG_TXP6

PEG_TX_7 T39 C_PEG_TXP7 C344 EV@.1U/10V_4 PEG_TXP7

PEG_TX_8 U36 C_PEG_TXP8 C346 EV@.1U/10V_4 PEG_TXP8

PEG_TX_9 U39 C_PEG_TXP9 C355 EV@.1U/10V_4 PEG_TXP9

PEG_TX_10 Y39 C_PEG_TXP10 C363 EV@.1U/10V_4 PEG_TXP10

PEG_TX_11 Y46 C_PEG_TXP11 C365 EV@.1U/10V_4 PEG_TXP11

PEG_TX_12 AA36 C_PEG_TXP12 C371 EV@.1U/10V_4 PEG_TXP12

PEG_TX_13 AA39 C_PEG_TXP13 C382 EV@.1U/10V_4 PEG_TXP13

PEG_TX_14 AD42 C_PEG_TXP14 C396 EV@.1U/10V_4 PEG_TXP14

PEG_TX_15 AD46 C_PEG_TXP15 C387 EV@.1U/10V_4 PEG_TXP15

PEG_TXP[15:0] 18,26

IV&EV Dis/Enable setting

<5/31>Montevina_Schematics_Checklist_Rev0_8
a)For TVOUT Disabled, TV_DCONSEL[1:0] Connect to GND. But design guide Rev0.7 show NC.What is correct.
b)For CRT DAC Disable, CRT_DDC_CLK, CRT_DDC_DATA . CRT_HSYNC, CRT_VSYNCThese signals should be connected to GND. But design guide Rev0.7 show NC, Intel suggest follow Design guide.

<check list>	<check list>
For EV@	For IV@
CRT R/G/B 0ohm to GND	CRT R/G/B 150ohm to GND
CRTIREF 0ohm to GND	CRTIREF 1Kohm to GND

CRTIREF
For IV: 1Kohm
For EV:0ohm

R186 SP@1K/F_4 CRTIREF

SP@

CRT_R/G/B
For IV: 150ohm
For EV:0ohm

R179 SP@150_4 INT_CRT_BLU

R178 SP@150_4 INT_CRT_GRN

R180 SP@150_4 INT_CRT_RED

PROJECT : ZQ5
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Size	Document Number	Rev
	GMCH VGA	1A
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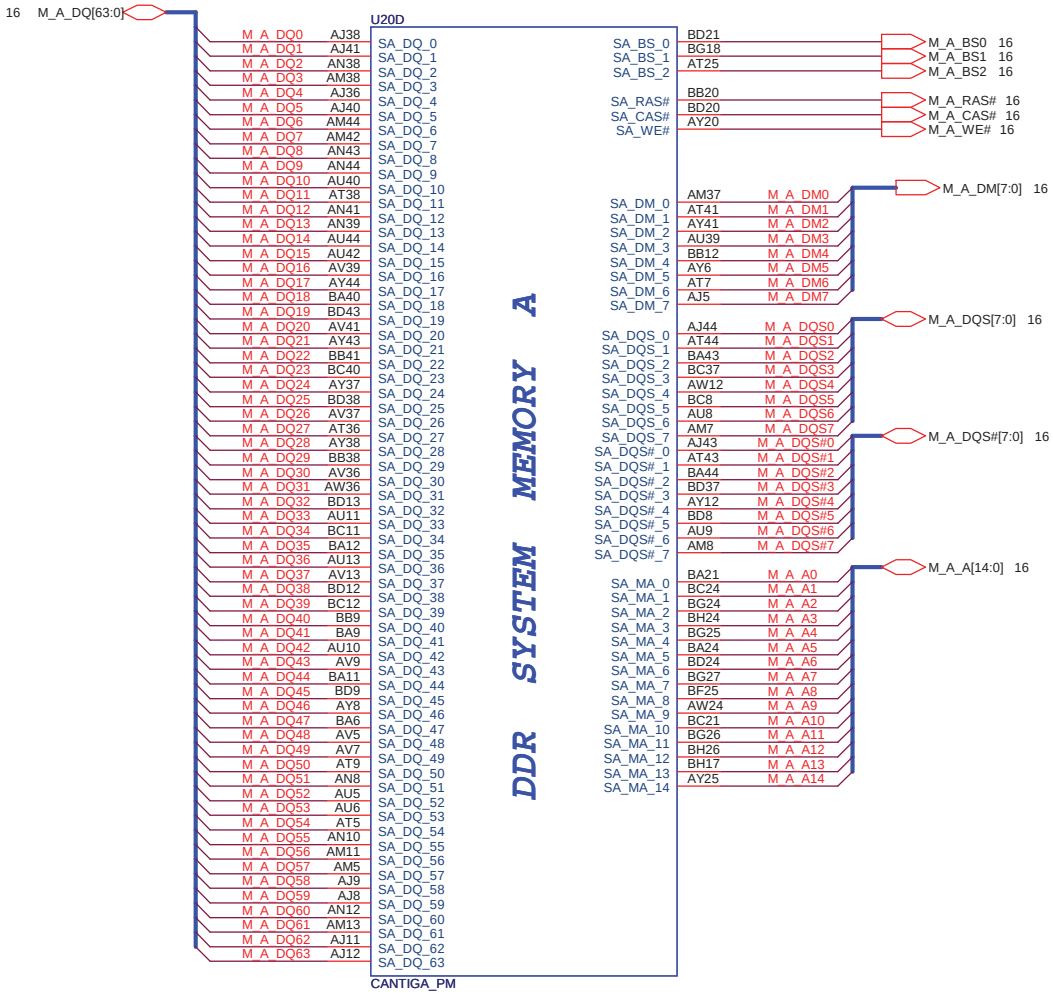

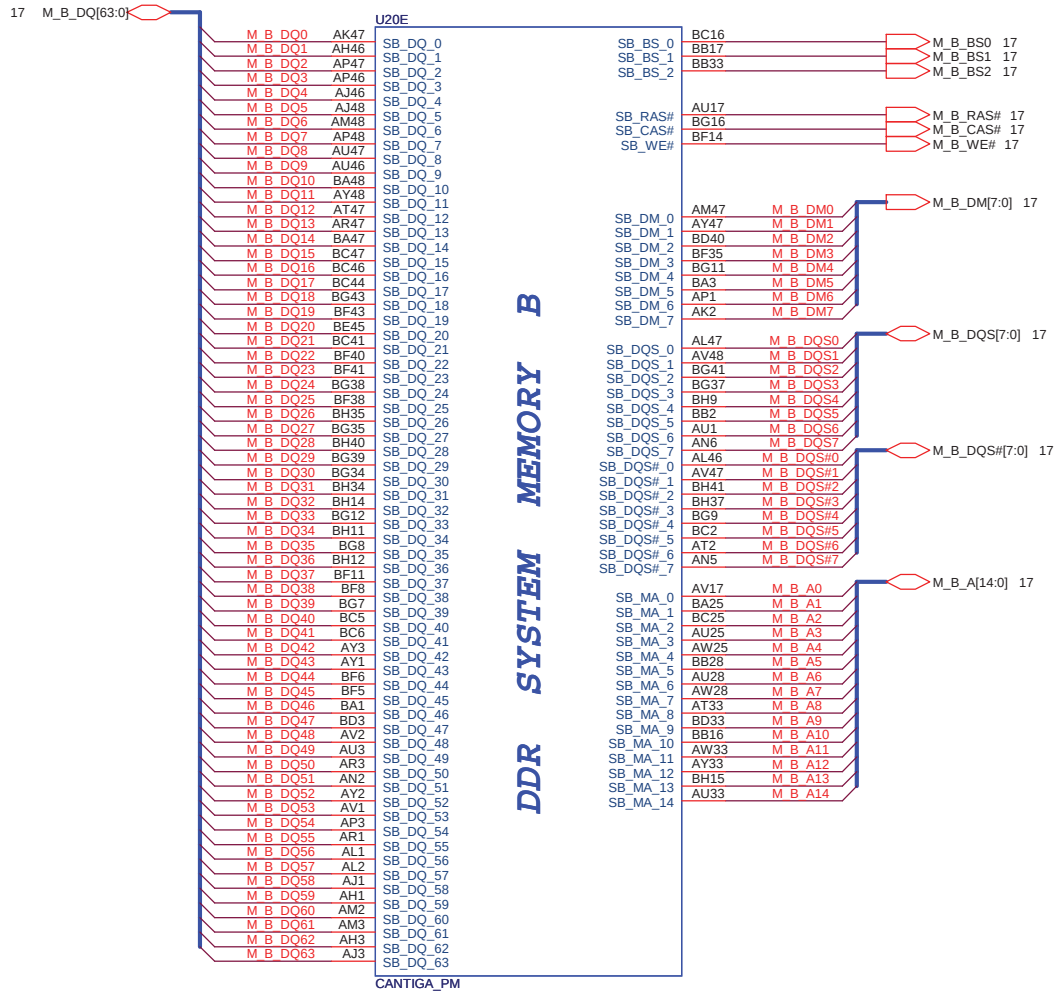

GMCH (CANTIGA)

PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH DDRII	1A
Date: Monday, July 12, 2010	Sheet 8 of 43	

IV@

SP@

Power consumption reference to Intel
644135 Cantiga chipset EDS Volume1.
Section 10

GM TDP 10.5~12W
GS TDP 7~8W
PM TDP 7W

Intel check list(Rev 0.8)
No description for VCC_SM bulk CAP
Intel CRB(Rev 0.7)
330U*1 Reserve near to power
330U*1 near to NB

Intel check list(Rev 0.8)
270U*1 near to power(+V1.05M).
270U*2 near to NB
Intel CRB(Rev 0.7)
270U*3 near to power(+V1.05M).
270U*1 near to NB
ESR=12m ohm

+1.5V_SUS
C561 22U/6.3V_8
C558 22U/6.3V_8
C414 0.1U/10V_4
C572 330U/2V_7343

U20G

VCC_SM(1.8V)
DDR2(800M)
3000mA_S0 , 1mA_S3
DDR2(667M) : 2600mA_S0
DDR3(1067M) : 4140mA_S0

VCC_SM: AP33 AN33 BH32 BG32 BF32 BD32 BC32 BB32 BA32 AY32 AW32 AV32 AU32 AT32 AR32 AP32 AN32 BH31 BG31 BF31 BG30 BH29 BG29 BF29 BD29 BC29 BB29 BA29 AY29 AW29 AV29 AU29 AT29 AR29 AP29
VCC_SM_1 … VCC_SM_35
BA36 BB24 BD16 BB21 AW16 AW13 AT13
VCC_SM_36/NC … VCC_SM_42/NC

VCC SM POWER

VCC_AXG_NCTF: W28 V28 W26 V26 W25 V25 W24 V24 W23 V23 AM21 AL21 AK21 W21 V21 U21 AM20 AK20 W20 U20 AM19 AL19 AK19 AJ19 AH19 AG19 AF19 AE19 AB19 AA19 Y19 W19 V19 U19 AM17 AK17 AH17 AG17 AF17 AE17 AC17 AB17 Y17 W17 V17 AM16 AL16 AK16 AJ16 AH16 AG16 AF16 AE16 AC16 AB16 AA16 Y16 W16 V16 U16
VCC_AXG_NCTF_1 … VCC_AXG_NCTF_60

VCC GFX NCTF

+1.05V_AXG

1.05V
Graphics core
VCC_AXG_NCTF
6326.84mA

Y26 AE25 AB25 AA25 AE24 AC24 AA24 Y24 AE23 AC23 AB23 AA23 AJ21 AG21 AE21 AC21 AA21 Y21 AH20 AF20 AE20 AC20 AB20 AA20 T17 T16 AM15 AL15 AE15 AJ15 AH15 AG15 AF15 AB15 AA15 Y15 V15 U15 AN14 AM14 U14 T14
VCC_AXG_1 … VCC_AXG_42

VCC GFX

Voltage regulator is shared between
the Graphics Core Rail,
VCCA_HPLL,VCCA_MPLL,VCCA_PEG_PLL,VCCD_PEG_PLL,
VCCA_SM_CK, VCCA_DPLLA, VCCA_DPLLB, VCCD_HPLL,
VCCA_SM, VCC_AXF

+1.05V_AXG
IV@
R235 IV@10/F_4 AJ14
R230 IV@10/F_4 AH14
VCC_AXG_SENSE
VSS_AXG_SENSE

VCC SM LF

AV44 VCC_SM_LF1
BA37 VCC_SM_LF2
AM40 VCC_SM_LF3
AV21 VCC_SM_LF4
AY5 VCC_SM_LF5
AM10 VCC_SM_LF6
BB13 VCC_SM_LF7

1.8V
Internal connect to power

C418 0.1U/10V_4
C403 0.1U/10V_4
C417 0.22U/6.3V_4
C416 0.22U/6.3V_4
C404 0.47U/6.3V_4
C415 1U/6.3V_4
C413 1U/6.3V_4

CANTIGA_PM

1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm and VSS_AXG_SENSE PD with 10ohm for Intel suggest

+1.05V
C375 0.1U/10V_4
C379 0.22U/6.3V_4
C359 0.22U/6.3V_4
C381 22U/6.3V_8
C631 330U/2V_7343

Place close to the GMCH

U20F

VCC_1 … VCC_12
AG34 AC34 AB34 AA34 Y34 V34 U34 AM33 AK33 AJ33 AG33 AF33
AE33 AC33 AA33 Y33 W33 V33 U33 AH28 AF28 AC28 AA28 AJ26 AG26 AE26 AC26 AH25 AG25 AF25 AG24 AJ23 AH23 AF23 T32
VCC_13 … VCC_35

VCC CORE POWER

+1.05V
IV@
R384 IV@ 8
R381 IV@ 8
R383 IV@ 8

IV&EV Dis/Enable setting
Design guide(Table 72)
For INT VGA diasble.VCC_AXG power can connect to GND

+1.05V_AXG
C602 IV@330U/2V_7343
C601 IV@330U/2V_7343
C399 IV@0.47U/6.3V_4
C392 SP@1U/10V_6
C367 IV@10U/6.3V_8
C380 IV@22U/6.3V_8
C393 IV@0.1U/10V_4
C410 IV@0.1U/10V_4
C370 IV@0.1U/10V_4

SP@

Place close to the GMCH
Cavity Capacitors

SP@:IV Sutff 1uf
EVstuff 0 ohm

Intel check list(Rev 0.8)
220U*2 near to NB(ESR=15m ohm)
Intel CRB(Rev 0.7)
270U*4 near to power(+V1.05S).
330U*2 near to NB

+1.05V
VCC_NCTF_1 … VCC_NCTF_44
AM32 AL32 AK32 AJ32 AH32 AG32 AE32 AC32 AA32 Y32 W32 U32 AM30 AL30 AK30 AH30 AG30 AF30 AE30 AC30 AB30 AA30 Y30 W30 V30 U30 AL29 AK29 AJ29 AH29 AG29 AE29 AC29 AA29 Y29 W29 V29 AL28 AK28 AL26 AK26 AK25 AK24 AK23

VCC NCTF POWER

CANTIGA_PM

VCC
VCC_NCTF
1210.34mA_EV
1930.4mA_IV
ME Engine
508.12mA
Total Max=2438.52mA

GMCH (CANTIGA)

PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH VCC,NCTF	1A
Date: Monday, July 12, 2010	Sheet 9 of 43	

Power consumption reference to Intel Cantiga chipset EDS Volume1. Section 10

IV@
EV@
SP@

If CRT have Flicker issue
STUFF 5.6 ohm

Modify 6/18
REV:B

5/12 UMA no stuff

External Graphics
(GMCH Integrated Graphics Disable)

VCCSYNC_CRT	GND
VCCA_CRT_DAC	GND
VCCD_LVDS	GND
VCC_TX_LVDS	GND
VCCA_LVDS	GND
VCCA_TVDAC	GND
VCCD_QDAC	GND
VCCA_DAC_BG	GND
VCC_AXG	GND
VCC_AXG_NCTF	GND

Power Net Name	Cantiga(V)
VCC_AXG_# VCC_AXG_NCTF_#	1.05V
VCCA_PEG_BG	1.5V
VCCA_DPLLA	1.05V
VCCA_DPLLB	1.05V
VCCA_SM_#	1.05V
VCCA_HPLL	1.05V
VCCA_MPLL	1.05V
VCC_SM_CK_#	1.05V
VCCA_PEG_PLL	1.05V
VCC_AXF_#	1.05V
VCCD_HPLL	1.05V

GMCH (CANTIGA)

PROJECT : ZQ5
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Size	Document Number	Rev
	GMCH POWER	1A
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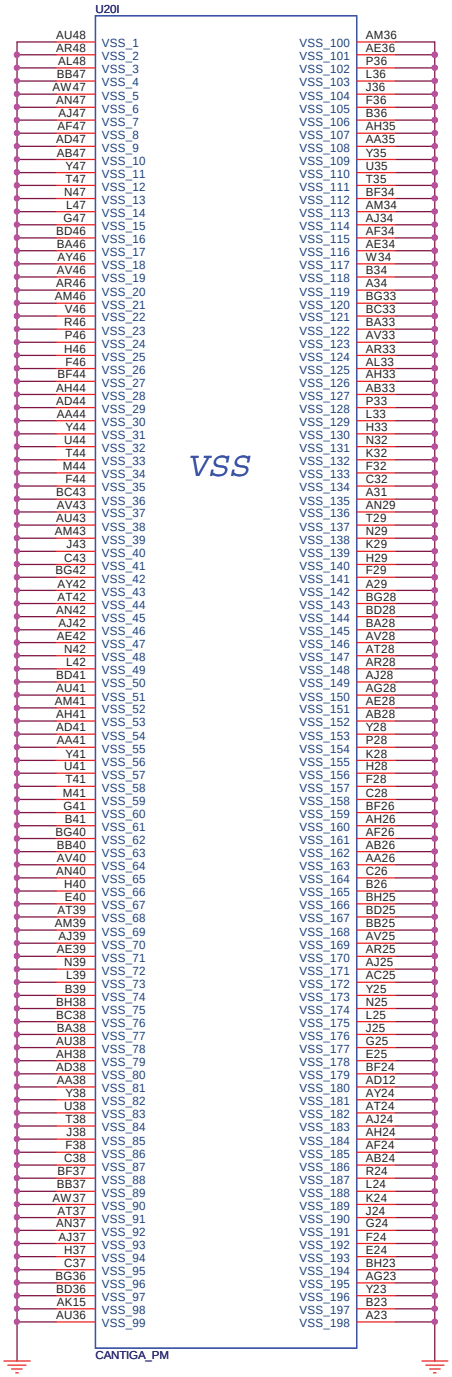

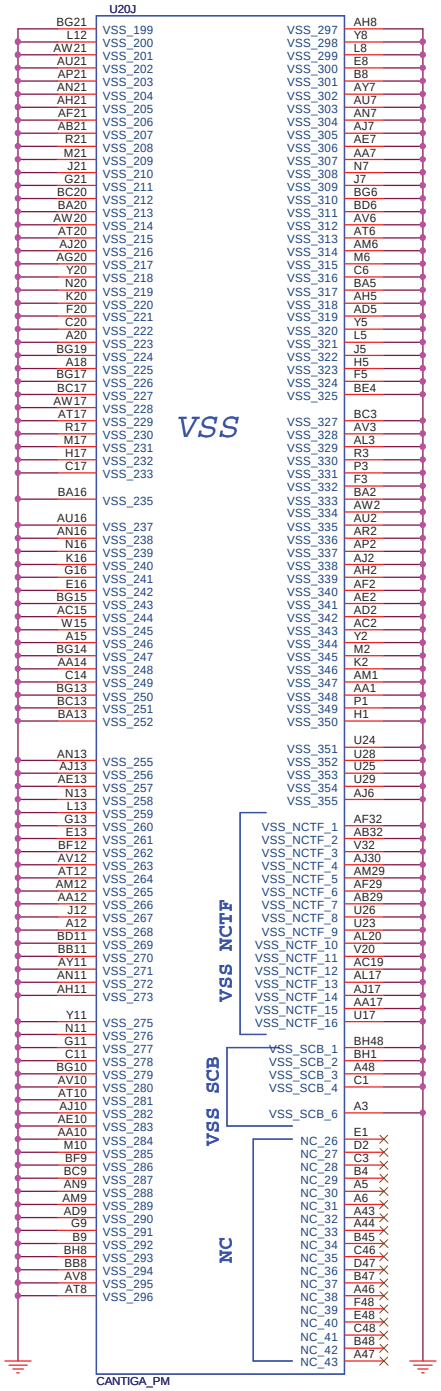

GMCH (CANTIGA)

PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH VSS	1A
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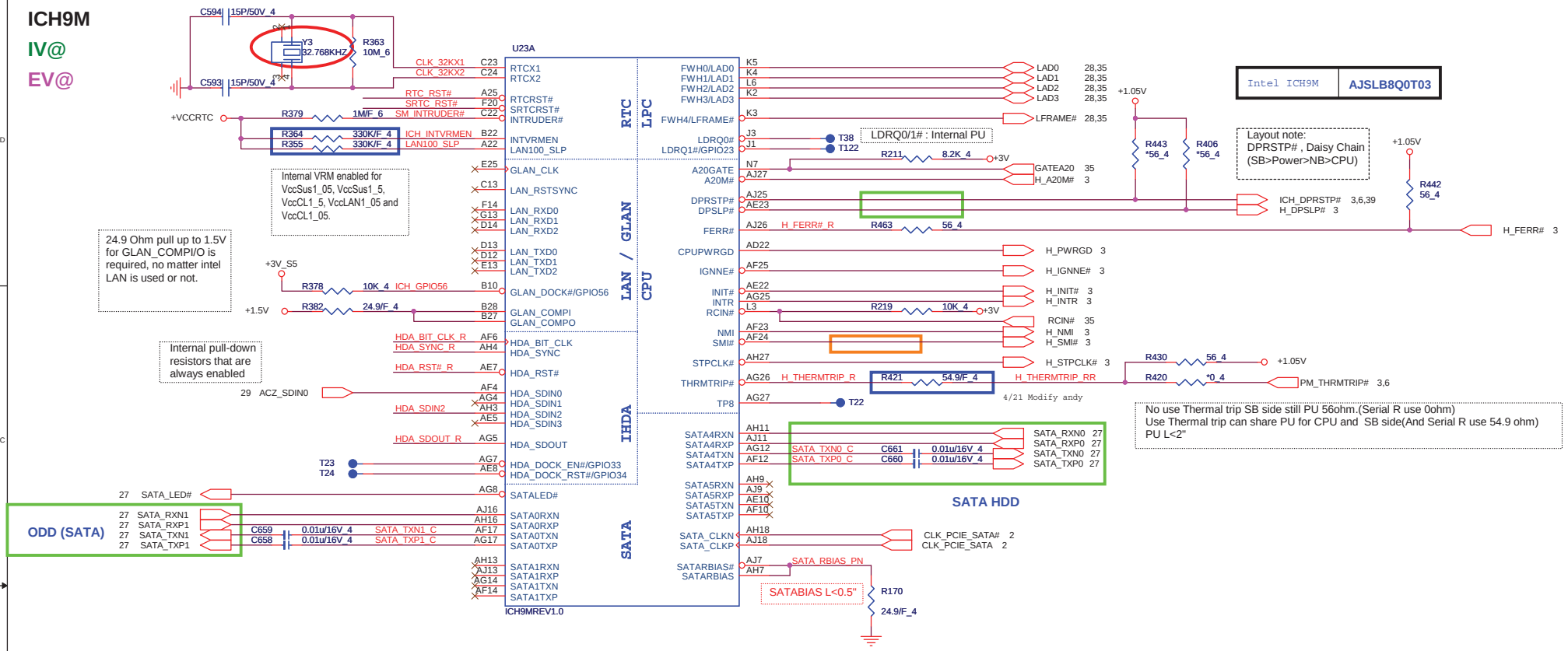
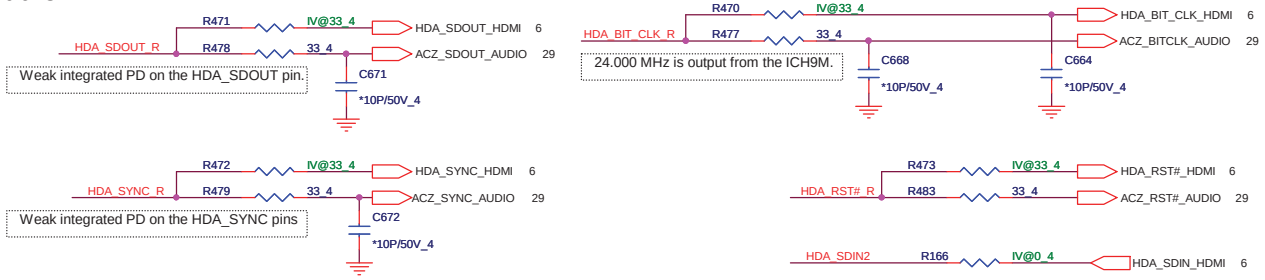
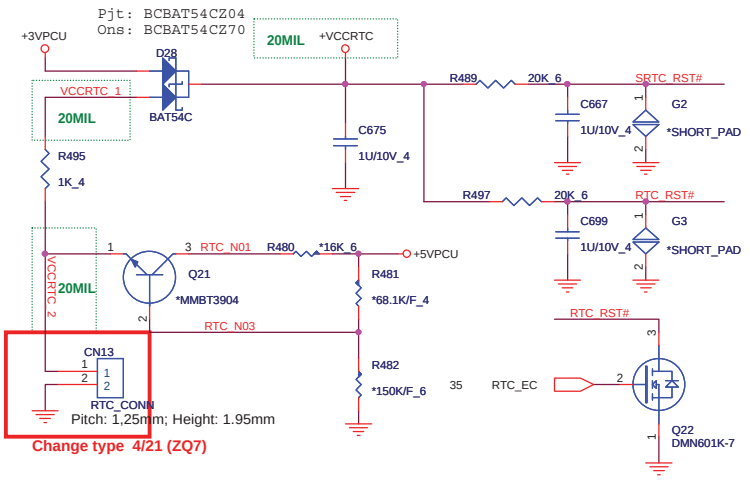
ICH9M
IV@
EV@



HD Audio



RTC



South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	ICH_TP3 / HDA_SDOUT: 0/0 RSVD; 0/1 Enter XOR Chain; 1/0 Normal opration(Default); 1/1 Set PCIE port config bit 1	14 ICH_TP3 — ICH_TP3 — R370 *1K_4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		HDA_SDOUT_R — R440 *1K_4 — +3V

PROJECT : ZQ5
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Size	Document Number	Rev
	ICH9M HOST	1A
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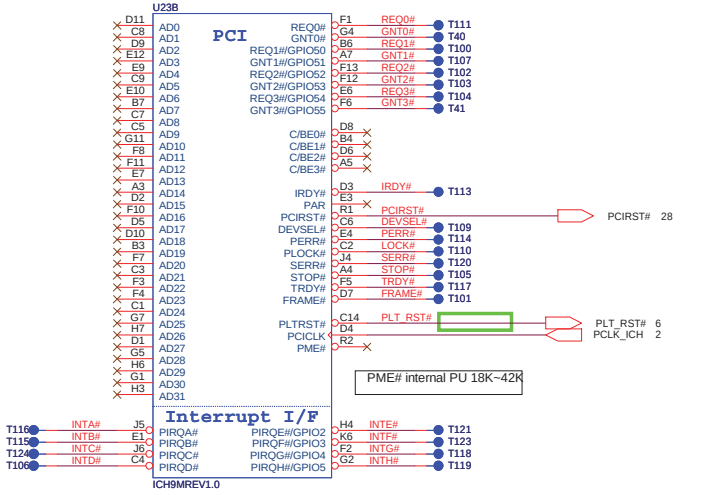

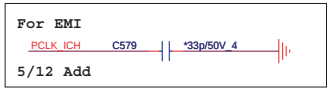

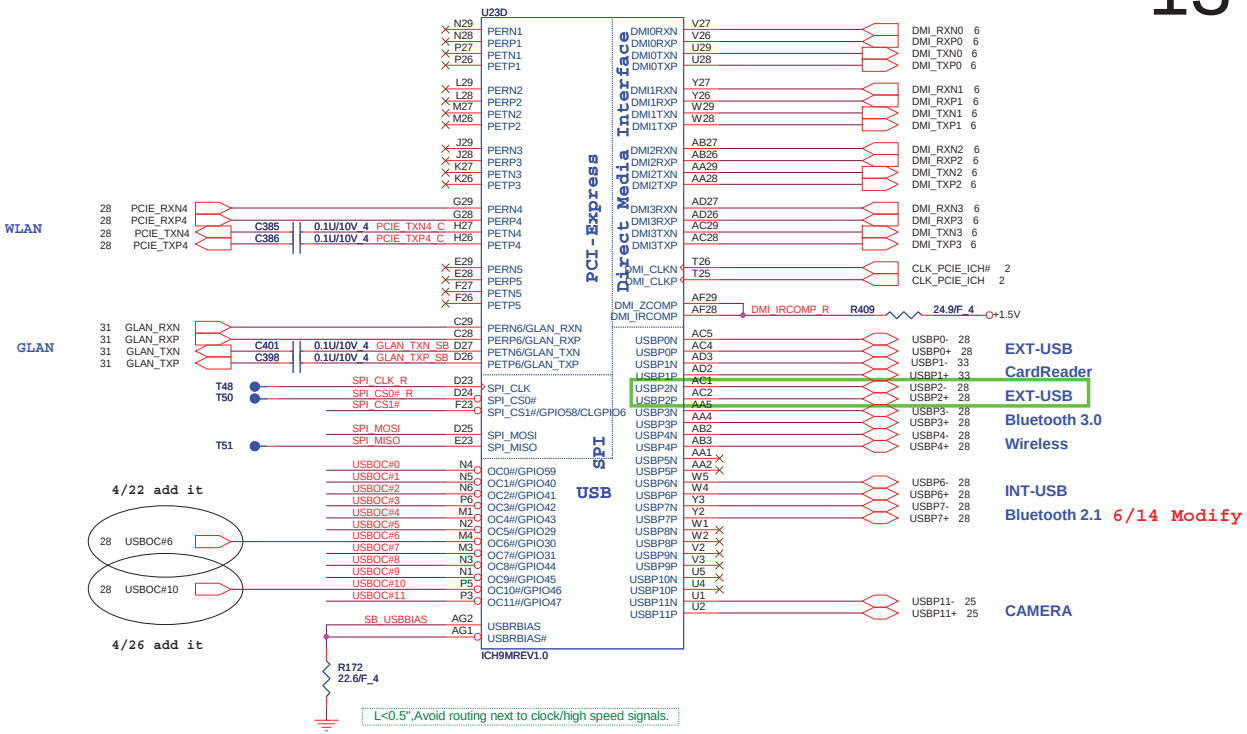

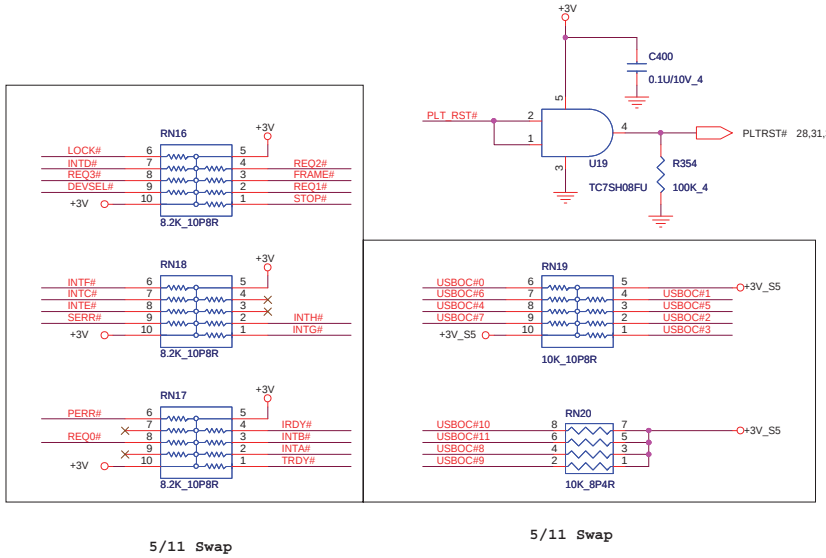

South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R237 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI R380 *10K_4 +3V_S5
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI	GNT0# R236 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1 / 0 / PCI 1 / 1 / **LPC(Default)**	SPI_CS1# R234 *1K_4

D3A:(1/31) ASF issue:when iAMT is not implemented,
ICH8M SMBus and SMLink should be connected together to support slave mode
Connect SMLINK0 to SMBCLK and SMLINK1 to SMBDATA (Add R474,R475 for debug use)

SATA[x]GP pins if unused require
8.2-k to 10-k pull-up to Vcc3_3 or
8.2-k to 10-k pull-down to ground

4/20 Modify

PWRBTN : 16 ms of internal debounce logic on this pin and internal PU 24K

Stuff at GEN

TPM Physical Presence for iTPM.

5/7 Modify

ZS2 Default not support IAMT. So this interface follow CRB/Checklist PU only

4/14 Modify

<Checklist ver0.8>
If integrated LAN is not used LAN_RST# tie it to GND.NC serial R from RSMRST#.
If Intel LAN is used with Wake On LAN, tie LAN_RST# to RSMRST# and NC 0ohm.

CL_PWROK must not assert after PWROK asserts for IAMT.
CL_PWROK to the NB and SB should be connected to existing PWROK inputs on the NB and SB on a platform with no IAMT

For EMI

CL VREF

VREF1 CRB connect to +3V_S5
Checklist connect to +3V(iAMT reserve)

<Checklist ver0.8>
The ICH9M Controller Link 1 VREF circuit is required only if Intel AMT is to be supported.

Add 4/19

Follow CHECK LIST V1.5

ICH PWROK

DELAY_VR_PWRGOOD need PU 2K to +3V.
ZS2 PU at power side

Resume RST

ZD1 INTEL FAE (08/17)
"Add RSMRST# isolation (important!!! See ww22 Santa Rosa MoW)"
Default stuff for Teenah(Interposer) chipset
ZS2 Intel FAE suggestion to add for to protect RTC/CMOS data from corruption when system encounters an abnormal power down sequence

M/B ID

Board ID	ID3	ID2	ID1	ID0
default	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0

South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R216 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R464 *1K_4

CLK Enable

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Size	Document Number: ICH9M GPIO — Rev 1A
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IV@

EV@

Power consumption reference to Intel ICH9 Family EDS Rev 1.6

PER INTEL SUGGESTION: CHANGE TO 100OHM & 1UF

2~3.456v 3.6uA_G3

5V 2mA

5V S0:2mA S3/4/5:1mA

1.5V 646mA

330 Ohms@ 100 MHz , 0805

1.5V 47mA

VCC1_5_A 1.5V 1342mA

1.5V 11mA

1.05V , Powered by VCC1_05 in S0

3.3V S0:19mA S3/4/5:78mA

If use SB MAC for LAN function. And support wake up need connect to relation power.

1.5V 23mA

1.5V 80mA

MODIFY follow ZR6

3.3V 1mA

1.05V 1634mA

1.5V 23mA

500 mA, 20%

1.05V 50mA

5 Ohms @ 100 MHz , 0.7A

1.05V 2mA

3.3V 308mA

3.3V S0:212mA S3/4/5:53mA

VCCSUS1_05 power by VCC1_05 in S0 / VCCSUS3_3 in S3/S4/S5
VCCSUS1_5 power by VCC1_5_A in S0 / VCCSUS3_3 in S3/S4/S5

5/10 change R8382 value to 12.1K

3.3V S0:19mA S3/4/5:73mA

VCCCL1_05 power by VCC1_05_A in S0
VCCCL1_5 power by VCC1_5_A in S0

If use SB MAC for LAN function. And support wake up need connect to relation power.

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

Support INT HDMI HDA interface. These power only support 1.5V.Device must to meet.

1.5V / 3.3V 11mA

2.5V / 3.3V S0:11mA S3/4/5:1mA

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

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Quanta Computer Inc.

Size	Document Number	Rev
	ICH9 POWER	1A
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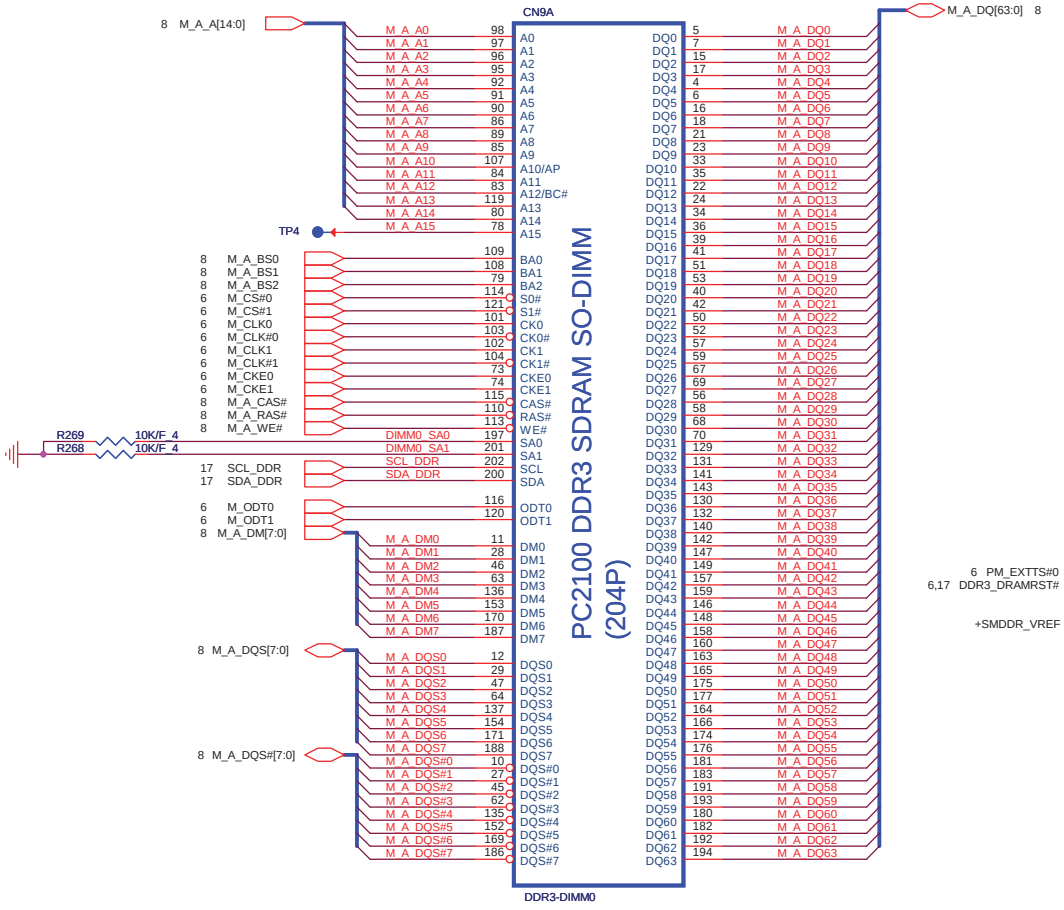
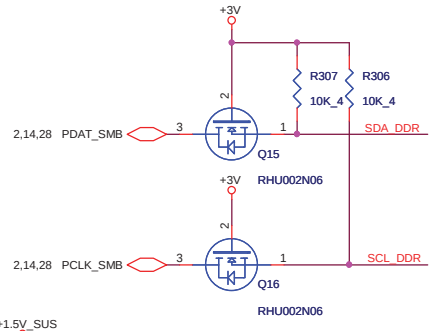
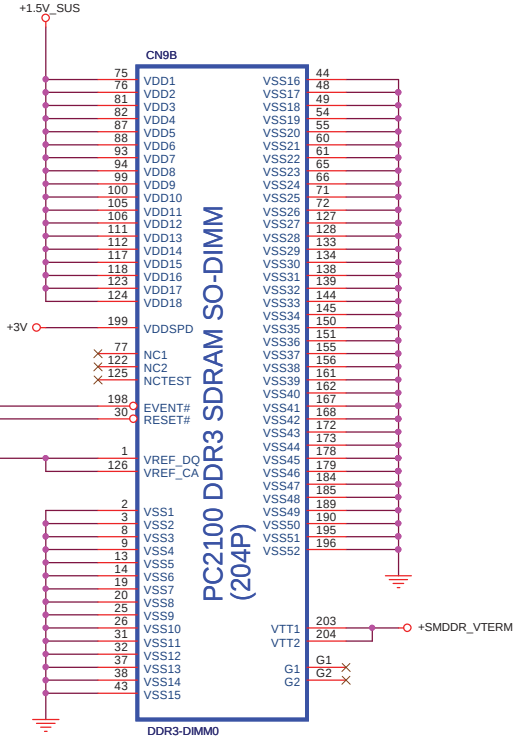
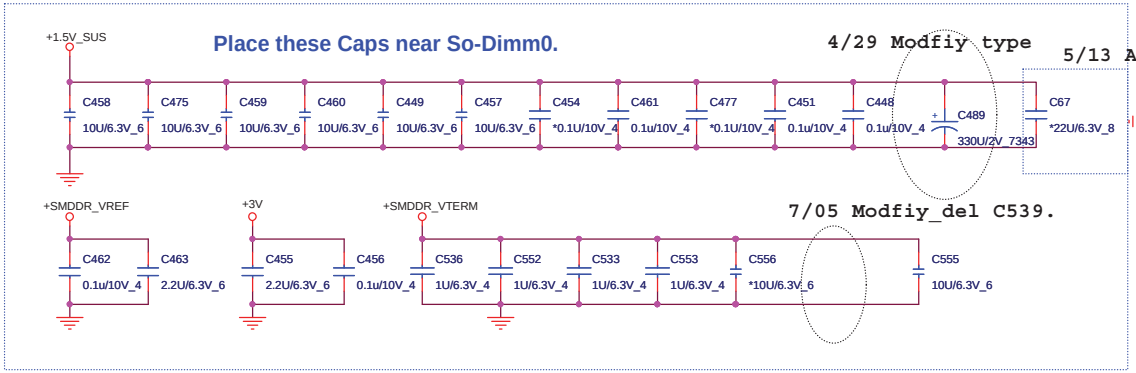
DDR3 (DDR)

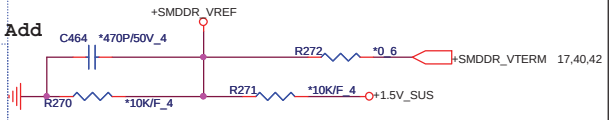
STD H=4.0 MM	QCI P/N
LTK	DGMK4000004
FOX	DGMK4000117











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Quanta Computer Inc.

Size	Document Number	Rev
	DDR3 DIMM-0(H=5.2)	1A
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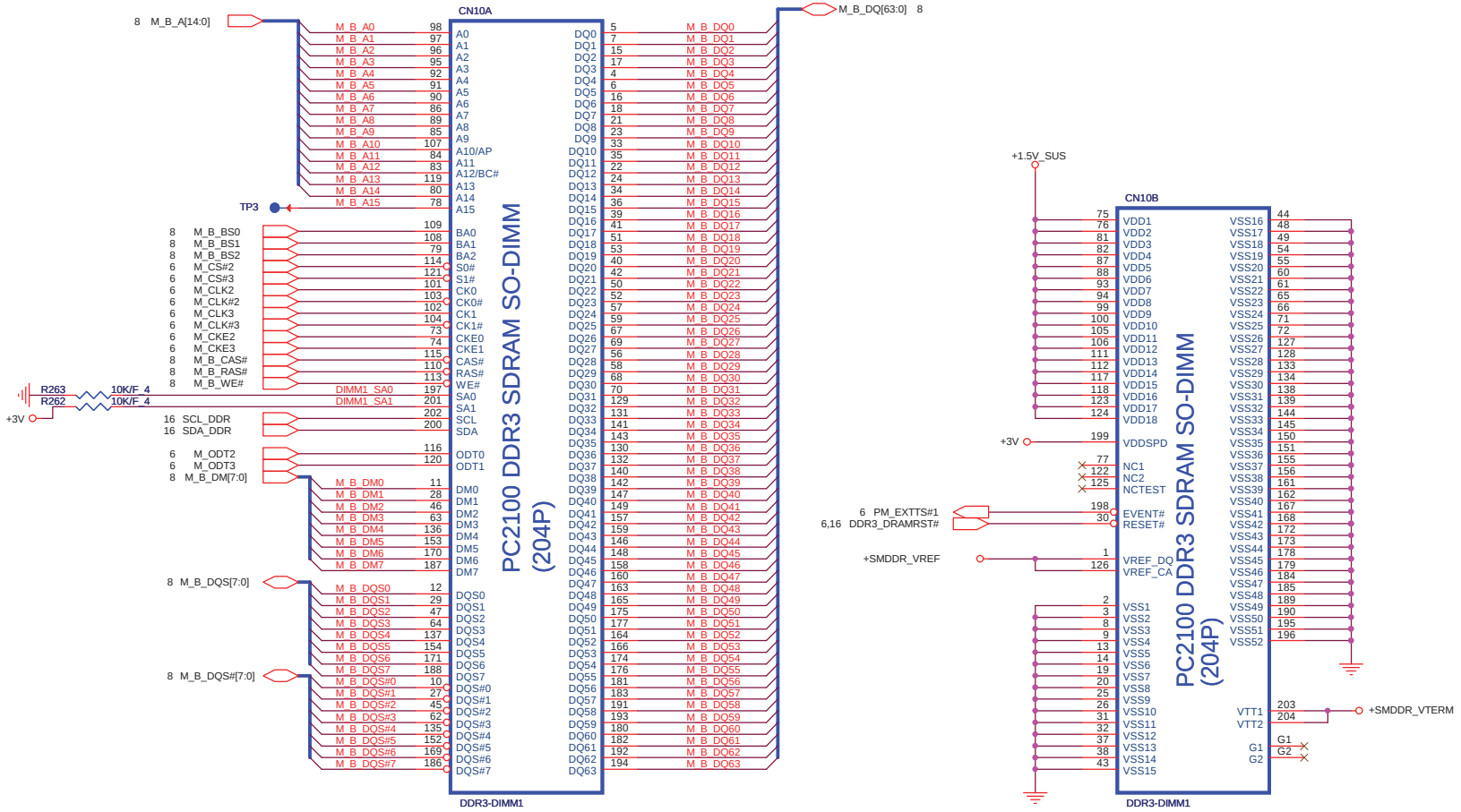
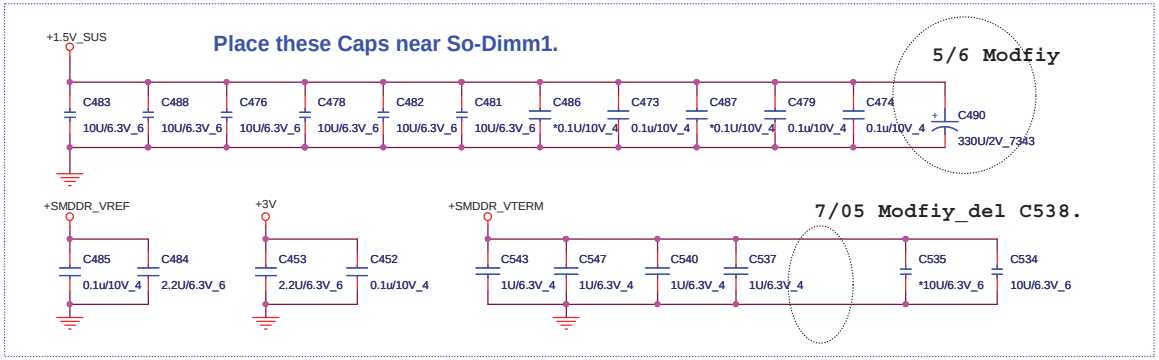
DDR3 (DDR)

STD H=8.0 MM	QCI P/N
LTK	DGMK4000097
FOX	DGMK4000130





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Quanta Computer Inc.

Size	Document Number	Rev
	DDR3 DIMM-1(H=9.2)	1A
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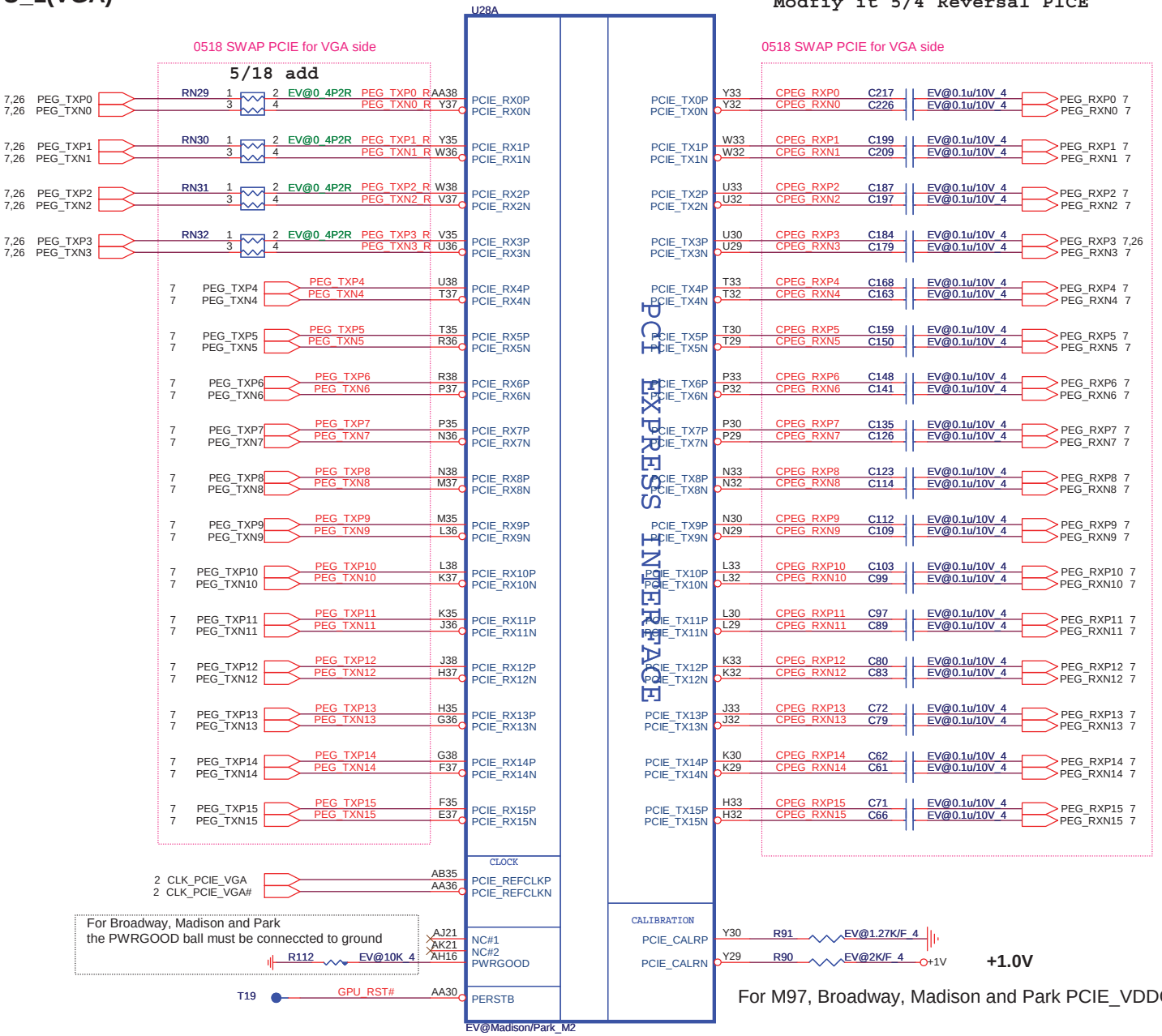
GPU_1(VGA)

Modfiy it 5/4 Reversal PICE

18

0518 SWAP PCIE for VGA side

5/18 add



0518 SWAP PCIE for VGA side

PCI EXPRESS INTERFACE

7,26 PEG_TXP[0..15] → PEG_TXP[0..15]
7,26 PEG_TXN[0..15] → PEG_TXN[0..15]
7,26 PEG_RXP[0..15] → PEG_RXP[0..15]
7 PEG_RXN[0..15] → PEG_RXN[0..15]

Item	Quanta P/N
Park	AJ077400T08
Robson	AJ007740T02

2 CLK_PCIE_VGA
2 CLK_PCIE_VGA#

For Broadway, Madison and Park
the PWRGOOD ball must be connecctd to ground

R112 EV@10K_4

T19 GPU_RST#

R91 EV@1.27K/F_4
R90 EV@2K/F_4 +1V

+1.0V

For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V

Quanta Computer Inc.
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Size	Document Number	Rev
	Madison/Park M2-PCIE I/F	1A
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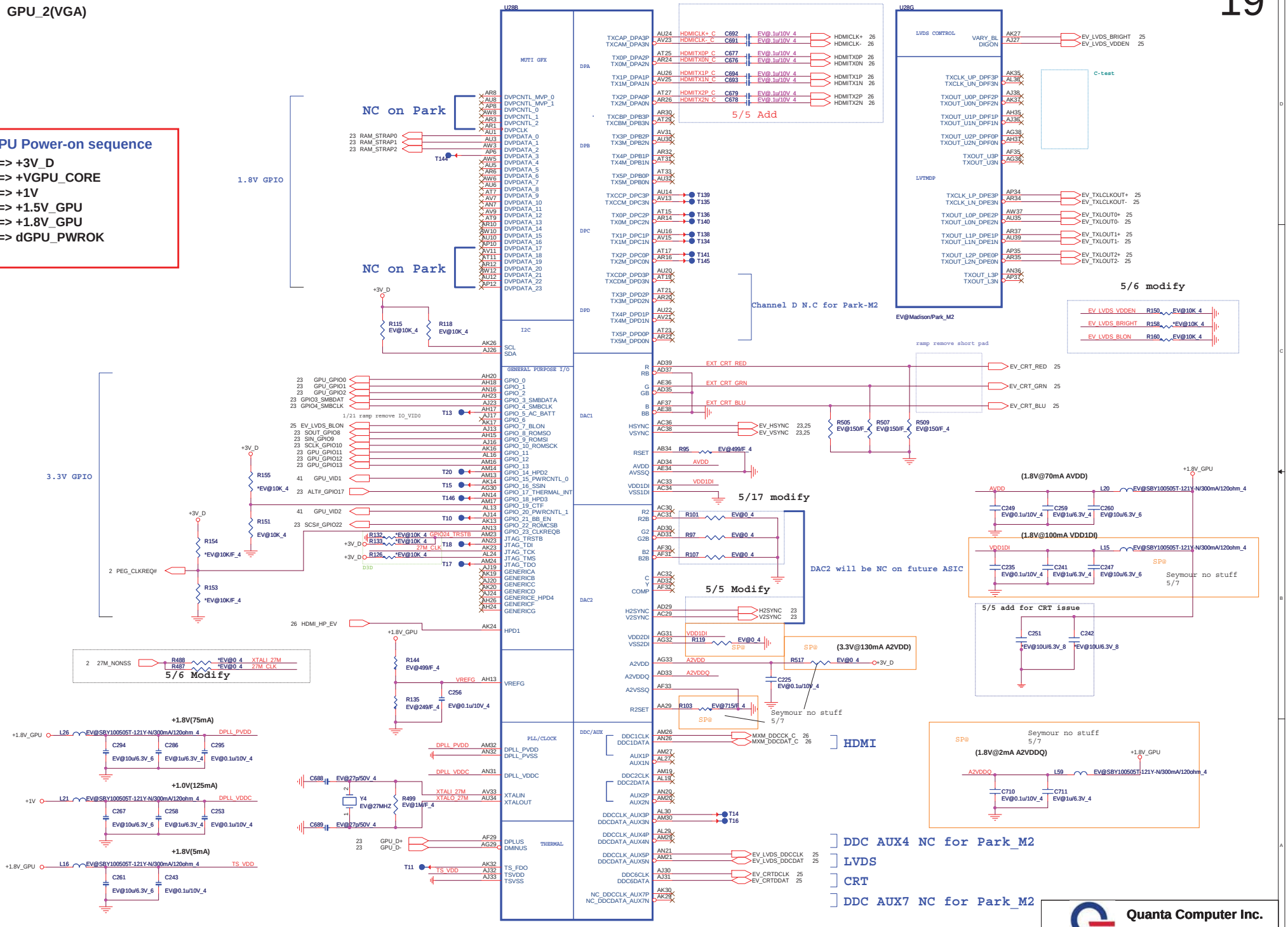
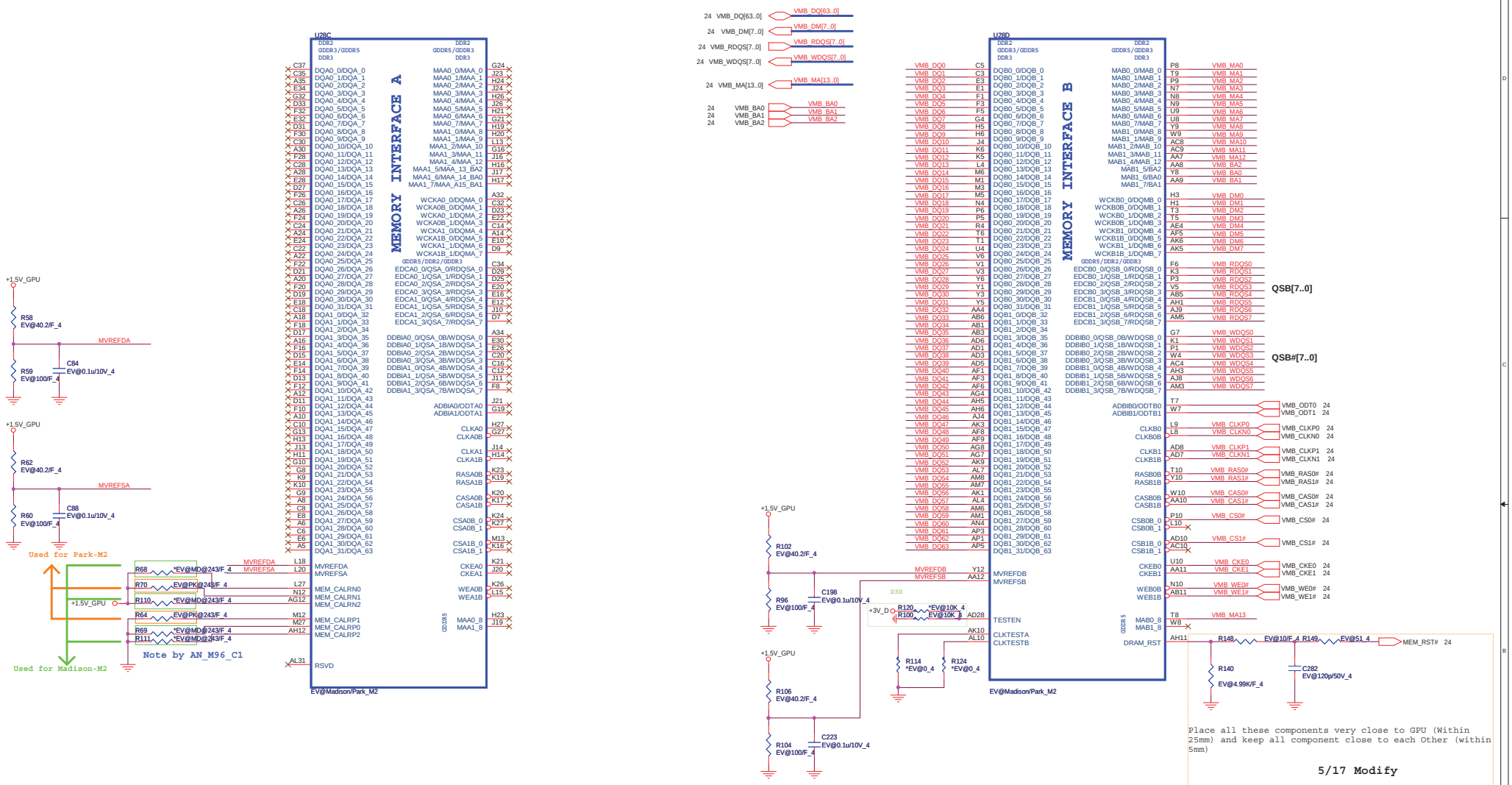
GPU_2(VGA)

GPU Power-on sequence

1 => +3V_D
2 => +VGPU_CORE
3 => +1V
4 => +1.5V_GPU
5 => +1.8V_GPU
6 => dGPU_PWROK



Park M2-channel B used(S3 package use Channel A)



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PROJECT : ZQ5

Size	Document Number	Rev
	Madison/Park M2-MEM I/F	1A

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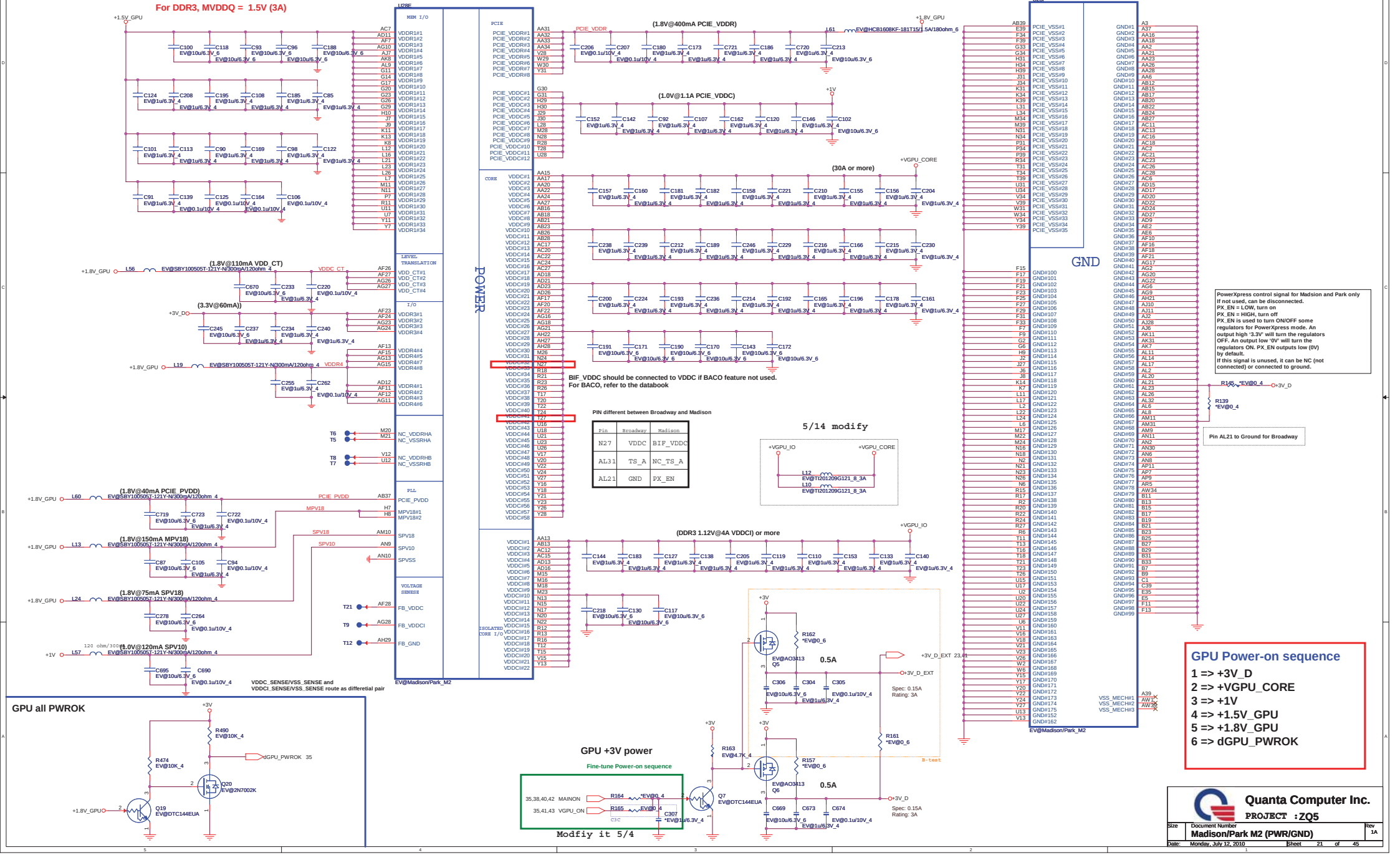
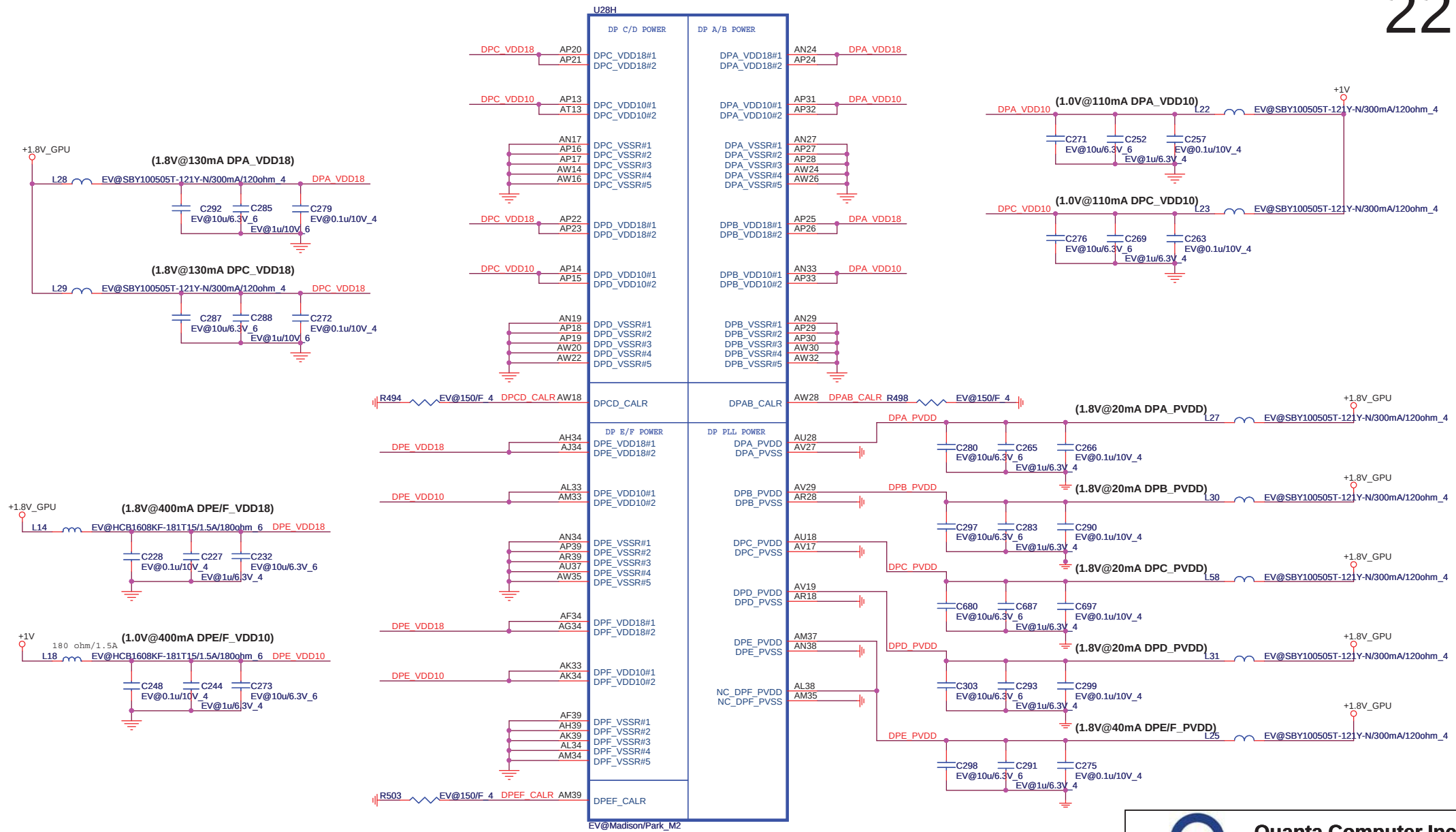
GPU_4(VGA)

For DDR3, MVDDQ = 1.5V (3A)



GPU_5(VGA)



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PROJECT : ZQ5

Size	Document Number	Rev
	Madison/Park M2 (DP_PWR/GND)	1A
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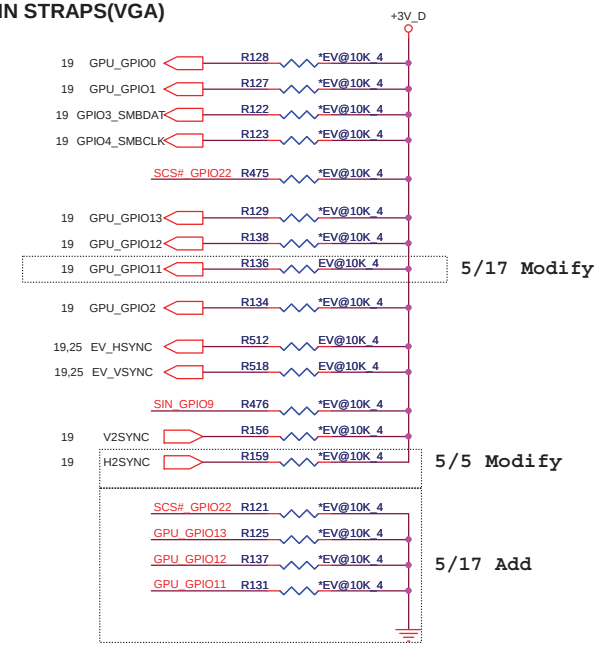
PIN STRAPS(VGA)



ROM Table	
Size of the primary memory apertures	CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
32 MB	011

ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

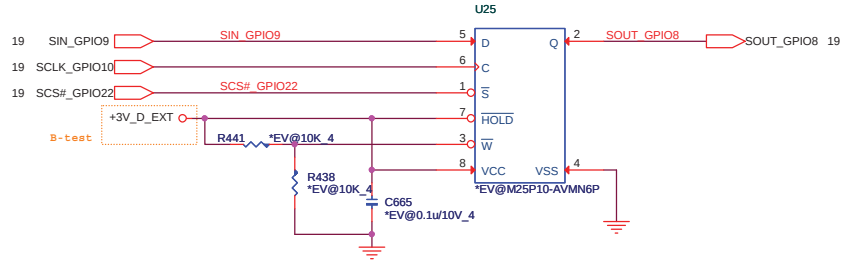
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

23

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	1	
ROMIDCFG(2:0)	GPIO[13:11]	Primary Memory Aperture size requested at PCI Configuration	001	table 3-35
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

EEPROM(VGA)

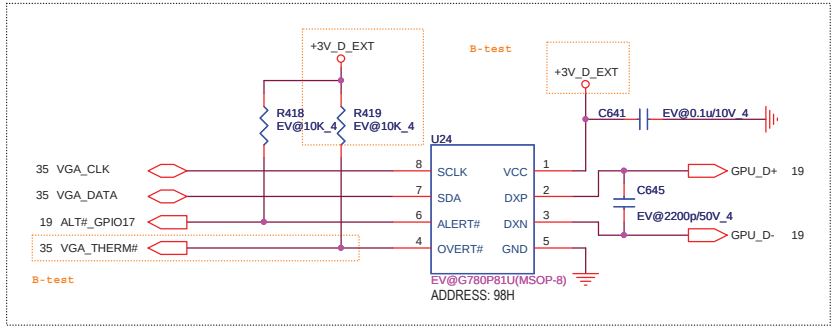


Thermal Sensor(VGA)

5/6 modify

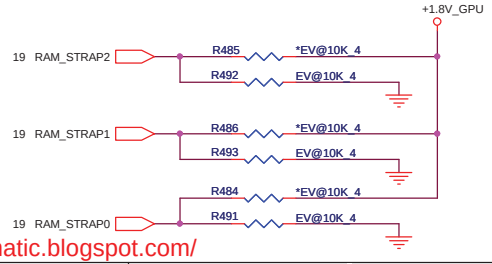
Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

USD0.16



DDR3 Memory Aperture size(GPU)

DDR3 Memory Aperture size					
Vendor	Vendor P/N	STN B/S P/N	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix			1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1	0	0
			1	0	1
Samsung					
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500 (128M*16)	0	0	1

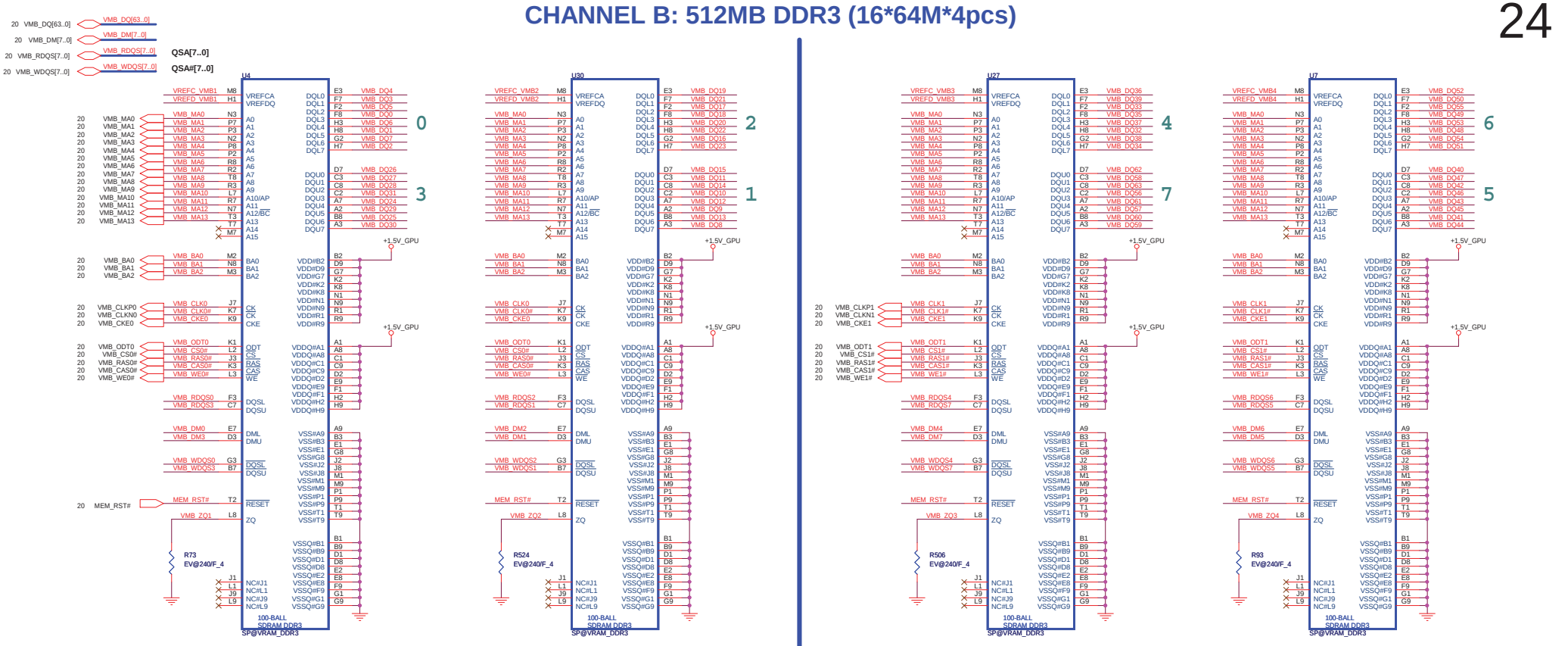


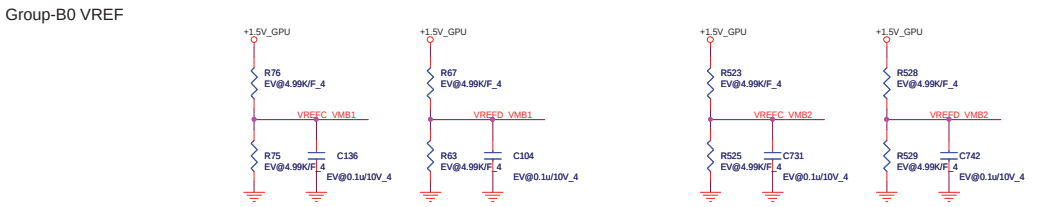
RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

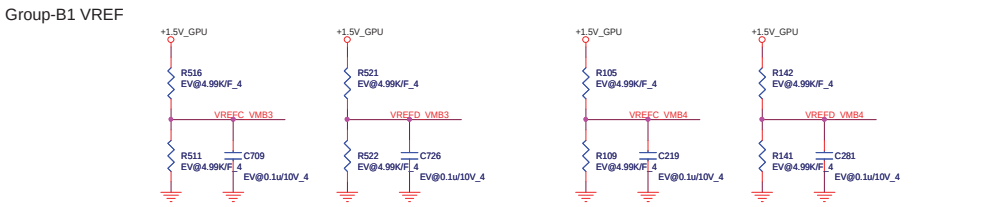
Quanta Computer Inc.
PROJECT : ZQ5

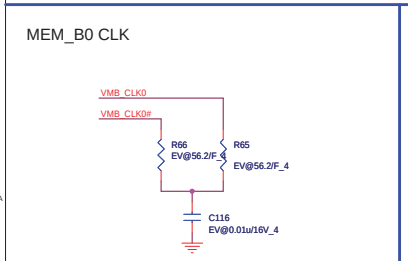
Size	Document Number	Rev
	Strip/Thermal	1A
Date: Monday, July 12, 2010	Sheet 23 of 45	

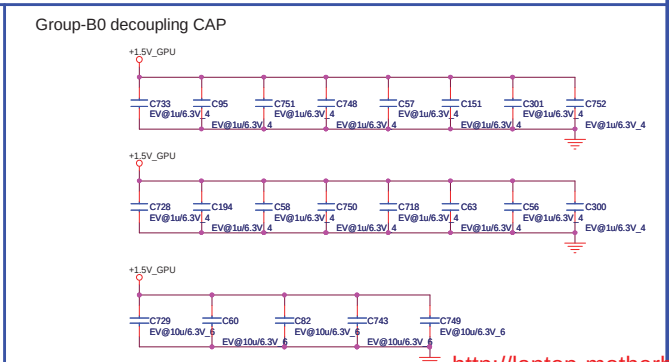
CHANNEL B: 512MB DDR3 (16*64M*4pcs)

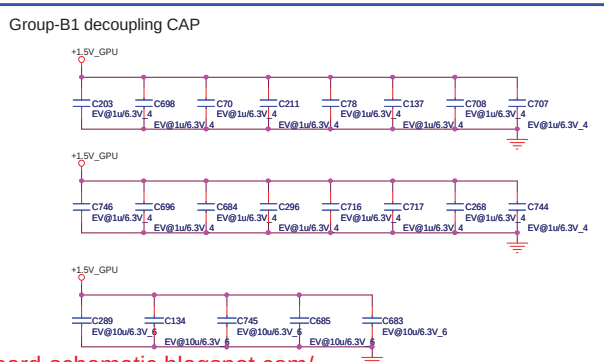


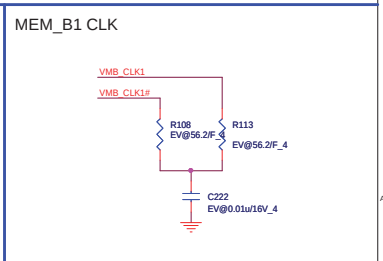












Quanta Computer Inc.

PROJECT : ZQ5

Size	Document Number	Rev
	MEMORY 2 channel B	1A

Date: Monday, July 12, 2010 Sheet 24 of 45

CRT Switch

IV@ --> iGPU only
EV@ --> dGPU only

iGPU only

7 INT_CRT_RED	INT_CRT_RED	R424	IV@0_4	VGA_RED
7 INT_CRT_GRN	INT_CRT_GRN	R422	IV@0_4	VGA_GRN
7 INT_CRT_BLU	INT_CRT_BLU	R423	IV@0_4	VGA_BLU
7 INT_VSYNC	INT_VSYNC	R434	IV@0_4	VSYNC
7 INT_HSYNC	INT_HSYNC	R435	IV@0_4	HSYNC
7 INT_CRT_DDCDAT	INT_CRT_DDCDAT	R427	IV@0_4	CRTDDATA
7 INT_CRT_DDCCLK	INT_CRT_DDCCLK	R428	IV@0_4	CRTDCLK

4/16

dGPU only

19 EV_CRT_RED	EV_CRT_RED	R433	EV@0_4	VGA_RED
19 EV_CRT_GRN	EV_CRT_GRN	R431	EV@0_4	VGA_GRN
19 EV_CRT_BLU	EV_CRT_BLU	R432	EV@0_4	VGA_BLU
19,23 EV_VSYNC	EV_VSYNC	R455	EV@0_4	VSYNC
19,23 EV_HSYNC	EV_HSYNC	R456	EV@0_4	HSYNC
19 EV_CRTDDAT	EV_CRTDDAT	R436	EV@0_4	CRTDDATA
19 EV_CRTDCLK	EV_CRTDCLK	R437	EV@0_4	CRTDCLK

CRT

updatefootprint 4/19 ZQ2

12/29 Modify

F2 SMD1206P110TFT +5V → +5V_CRT → D33 SSM22LLPT → CRTVDD5

C791 .1u/10V_4

VGA_RED → L3 BK1608L680_6 → CRT_R1
VGA_GRN → L2 BK1608L680_6 → CRT_G1
VGA_BLU → L1 BK1608L680_6 → CRT_B1

R4 150/F_4, R3 150/F_4, R2 150/F_4, C7 5p/50V_4, C6 5p/50V_4, C5 5p/50V_4, C1 5p/50V_4, C2 5p/50V_4, C3 5p/50V_4

REV:B 6/14

CN20 CRT: CRT_R1, CRT_G1, CRT_B1, DDCDAT_1, CRTHSYNC, CRTVSYNC, DDCCLK_1 → T1

35 CRT_SENSE# → R553 10K_4 → +3V; D32 BAS316 → CRT_SEN#; R1 *0_4; C4 2.2u/6.3V_6

4/14 Modify

+3V: C8 .1u/10V_4, C786 0.22u/25V_6, C9 .1u/10V_4

U33 CM2009-02QR

1	VCC_SYNC	SYNC_OUT2	16
7	VCC_DDC	SYNC_OUT1	14
8	BYP		
2	VCC_VIDEO	SYNC_IN2	15
		SYNC_IN1	13
3	VIDEO_1	DDC_IN1	10
4	VIDEO_2	DDC_IN2	11
5	VIDEO_3		
		DDC_OUT1	9
6	GND	DDC_OUT2	12

CRTVDD5, CRT_BYP, CRT_R1, CRT_G1, CRT_B1

CRT_VSYNC2 → R11 15_4 → CRTVSYNC
CRT_HSYNC2 → R14 15_4 → CRTHSYNC
VSYNC → HSYNC
CRTDCLK → R21 2.7K_4
CRTDDATA → R22 2.7K_4
DDCCLK_1
DDCDAT_1

REV:B 6/14

+3V → R545 2.7K_4, R547 2.7K_4

C779 *.1u/10V_4 CRTVDD5
C11 *10p/50V_4 CRTVSYNC
C15 *10p/50V_4 CRTHSYNC
C774 10p/50V_4 DDCCLK_1
C777 10p/50V_4 DDCDAT_1

LVDS

iGPU only

5/11 Swap net

7 INT_TXLCLKOUT-	INT_TXLCLKOUT-	RN24	3	4 IV@0_4P2R	TXLCLKOUT-
7 INT_TXLCLKOUT+	INT_TXLCLKOUT+		1	2	TXLCLKOUT+
7 INT_TXLOUT0-	INT_TXLOUT0-	RN21	1	2 IV@0_4P2R	TXLOUT0-
7 INT_TXLOUT0+	INT_TXLOUT0+		3	4	TXLOUT0+
7 INT_TXLOUT1-	INT_TXLOUT1-	RN22	1	2 IV@0_4P2R	TXLOUT1-
7 INT_TXLOUT1+	INT_TXLOUT1+		3	4	TXLOUT1+
7 INT_TXLOUT2-	INT_TXLOUT2-	RN23	1	2 IV@0_4P2R	TXLOUT2-
7 INT_TXLOUT2+	INT_TXLOUT2+		3	4	TXLOUT2+
7 INT_LVDS_EDIDDATA	INT_LVDS_EDIDDATA	RN7	1	2 IV@0_4P2R	LCD_EDIDDATA
7 INT_LVDS_EDIDCLK	INT_LVDS_EDIDCLK		3	4	LCD_EDIDCLK

4/29 Modify it

dGPU only

5/11 Swap net

19 EV_TXLCLKOUT-	EV_TXLCLKOUT-	RN28	1	2 EV@0_4P2R	TXLCLKOUT-
19 EV_TXLCLKOUT+	EV_TXLCLKOUT+		3	4	TXLCLKOUT+
19 EV_TXLOUT0-	EV_TXLOUT0-	RN25	3	4 EV@0_4P2R	TXLOUT0-
19 EV_TXLOUT0+	EV_TXLOUT0+		1	2	TXLOUT0+
19 EV_TXLOUT1-	EV_TXLOUT1-	RN26	3	4 EV@0_4P2R	TXLOUT1-
19 EV_TXLOUT1+	EV_TXLOUT1+		1	2	TXLOUT1+
19 EV_TXLOUT2-	EV_TXLOUT2-	RN27	3	4 EV@0_4P2R	TXLOUT2-
19 EV_TXLOUT2+	EV_TXLOUT2+		1	2	TXLOUT2+
19 EV_LVDS_DDCDAT	EV_LVDS_DDCDAT	RN6	3	4 EV@0_4P2R	LCD_EDIDDATA
19 EV_LVDS_DDCCLK	EV_LVDS_DDCCLK		1	2	LCD_EDIDCLK

4/29 Modify it

+3V: C725 .1u/10V_4, C724 1000p/50V_4

INVCC0: C121 4.7u/25V_8, C167 1000p/50V_4

5/6 Modify

R98 *0_8 → LCDVCC; C231 *1000p/50V_4, C250 *1000p/50V_4

CN14 → LVDS

INVCC0, LCDVCC_L, R515 2.2K_4 LCD_EDIDCLK, R516 2.2K_4 LCD_EDIDDATA
TXLOUT0-, TXLOUT0+, TXLOUT1-, TXLOUT1+, TXLOUT2-, TXLOUT2+, TXLCLKOUT-, TXLCLKOUT+
USBP11- R, USBP11+ R
CCD_PWR
LVDS_BRIGHT L55 → LVDS_BRIGHT_R → BL_ON → SBY100505T-121Y-N

5/21 change Connector

Brightness

19 EV_LVDS_BRIGHT	R454	*EV@0_4	LVDS_BRIGHT
7 L_BKLT_CTRL	R453	IV@0_4	
35 CONTRAST	R452	EV@0_4	

VIN → 2A → R72 *0_8, R71 *0_8 → INVCC0; C115 *1000p/50V_4, C177 *1000p/50V_4

LCD_ON (LCD Power)

Stuff R713 on 2 CH.
Stuff R712 on 1 CH.

+3V, +5V → R147 0_6, R152 *0_1206

4/20 Modify

U8 AAT4280-4: IN, IN, ON/OFF, OUT, GND, GND

LCDVCC_R, LVDS_VDDEN → C302 1U/6.3V_4

C254 *.1u/10V_4, C174 *2.2u/10V_8, C201 .1u/10V_4, C202 0.01U/25V_4, C175 22u/6.3V_8 → LCDVCC

5/5 Add

R130 100K_4

Item	QCI P/N
AAT	AL004280001
GMT	AL005243001

19 EV_LVDS_VDDEN → R117 EV@0_4
7 INT_LVDS_DIGON → R116 IV@0_4 → LVDS_VDDEN

Backlight Control

+3V: R191 10K_4, R167 10K_4

BL_ON → D10 BAS316 → LID591# 14,35

BL# → Q9 2N7002D → Q10 DTC144EU → EC_FPBACK# 35

LVDS_BLON → Q8 2N7002D; R168 100K_4

19 EV_LVDS_BLON → R174 EV@0_4
7 INT_LVDS_BLON → R177 IV@0_4 → LVDS_BLON

Lid Switch (HSR)

+3VPCU: R193 *470K_4 → LID591#; C342 1u/10V_4 → +3VPCU

HE1 PT3661-BB SOT23_123-2_8-1_9

PT3661-BB (PLC) : AL003661003
ME268-002 (FCE) : AL000268000

4/22 add it

CCD

5/6 Modfiy

+3V → R146 *0_8 → CCD_PWR; C274 *1000p/50V_4, C700 *1000p/50V_4

Close to USB

USBP11-, USBP11+ → RN8 0_4P2R → USBP11- R, USBP11+ R; L17 *DLW21HN900SQ2L

5/24 Modify it

PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	CRT/LVDS/CAMERA/LID	1A
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iGPU HDMI LEVEL SHIFTER

IV@ --> iGPU only

EV@ --> dGPU only

REV:B 6/15

from MCH 4/20

U1

Active Buffer

REV:B 6/15

IV@PS8101T

5/7 Modify part number

For PS8101T

from MCH

Control by pin4 HPDEN_R

Equalization Control		
PC1 PIN4	PC0 PIN3	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB

PC0 internal PD
PC1 internal PD
DDCBUF_EN internal PD
CFG internal PD
DDC_EN internal PU

SP@SN75DP139
1.Pin34 HPDINV for 8101T Stuff R32
2.Stuff R24
3.R25 change 3.9K (CS23902FB14)

5/7 Add

HP-detect for PS8101 only

Item	QCI P/N
PS8101TQFN48GTR	AL008101001
PS8101QFN48GTR	AL008101000
SN75DP139RGZR	AL000139000

4/20 Modify

OE# control for power saving

To dGPU HPD

SDVO I2C Control

5/24 Add it

CSP@HDMI SDVO I2C For IV: 2.2K ohm For ES:4.7K ohm

CSP@HDMI SDVO I2C For IV: 2.2K ohm For ES:4.7K ohm

GPU Switchable Graphic HDMI source

To Discrete

4/29 Modify

Close to HDMI connector

6/15 Swap

From Discrete

From GMCH (iHDMI)

5/11 Swap

Close to NB couple cap & PCIE RESARRAY

HDMI connector

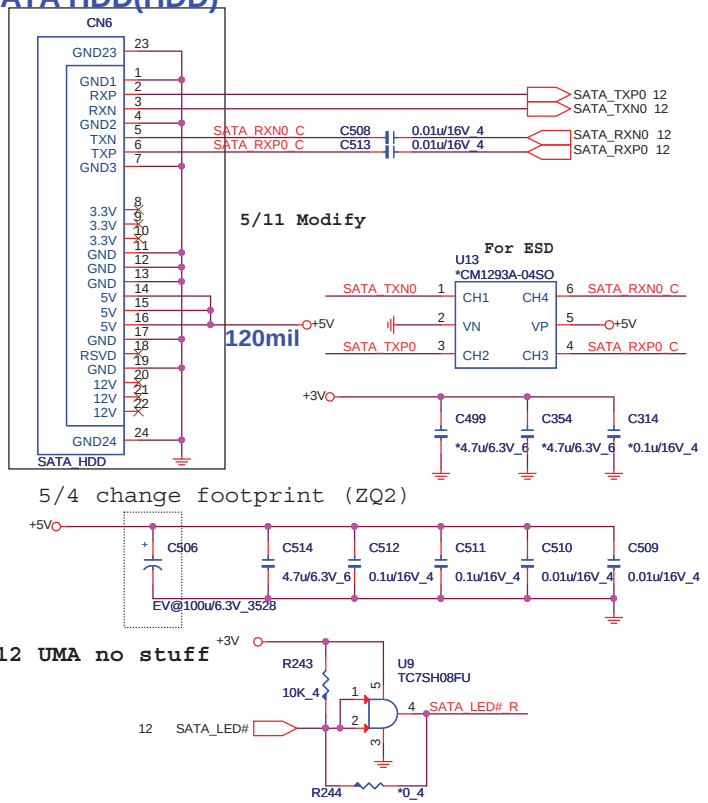
updatefootprint 4/19 ZQ2

1/11 Add C928 by EMI.

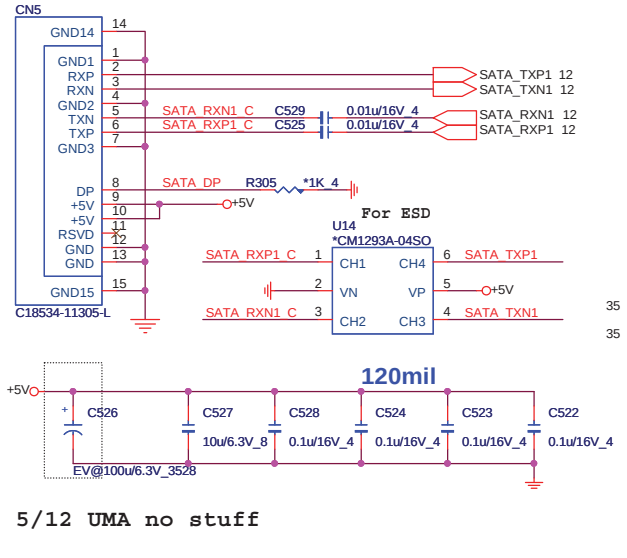
12/29 Modify

PROJECT : ZQ5		
Quanta Computer Inc.		
Size	Document Number: HDMI (PS8101)	Rev 1A
Date: Monday, July 12, 2010	Sheet 26 of 43	

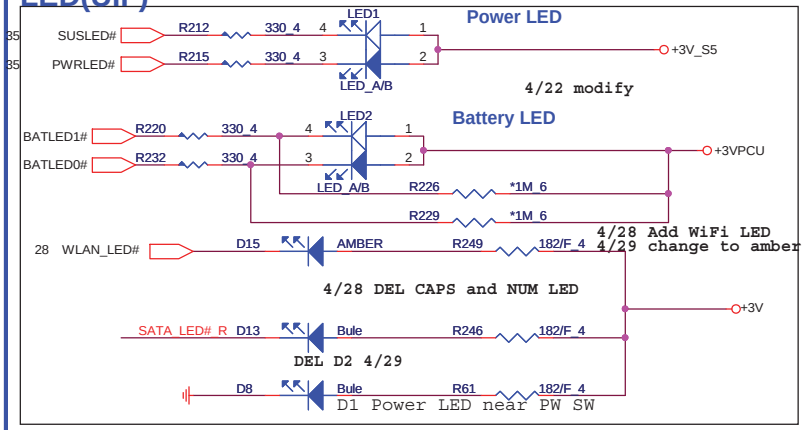
SATA HDD(HDD)



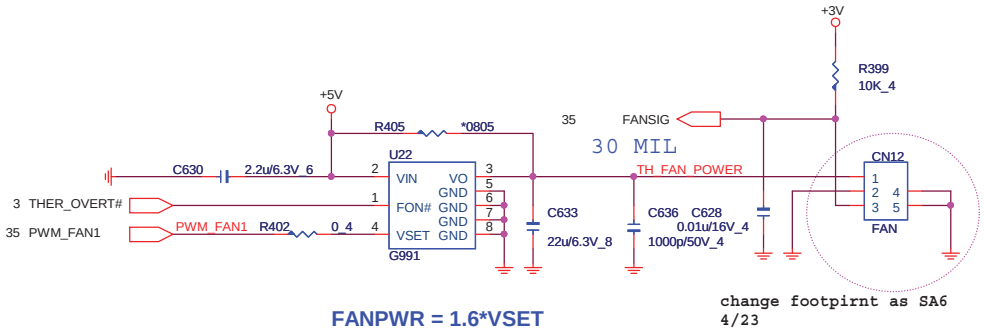
SATA ODD(ODD)



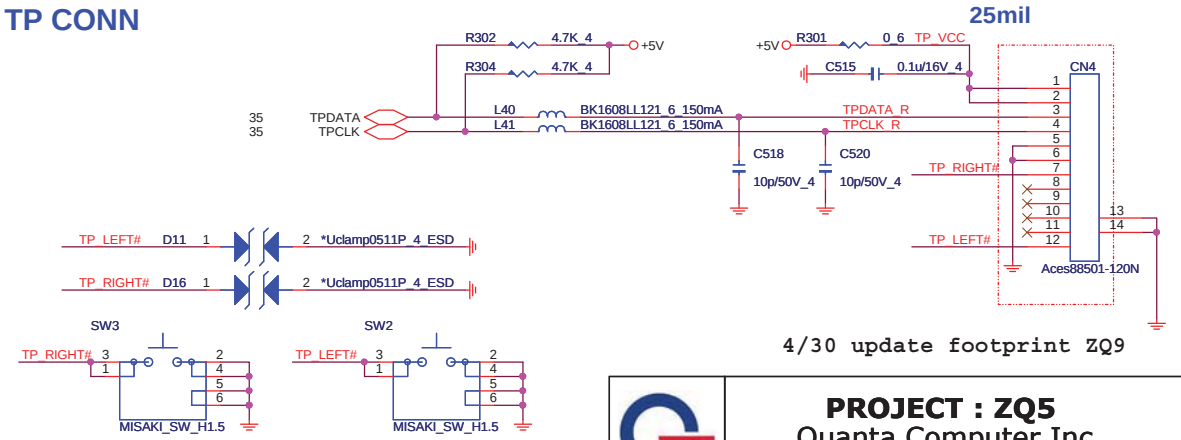
LED(UIF)



FAN(THM)



TP CONN

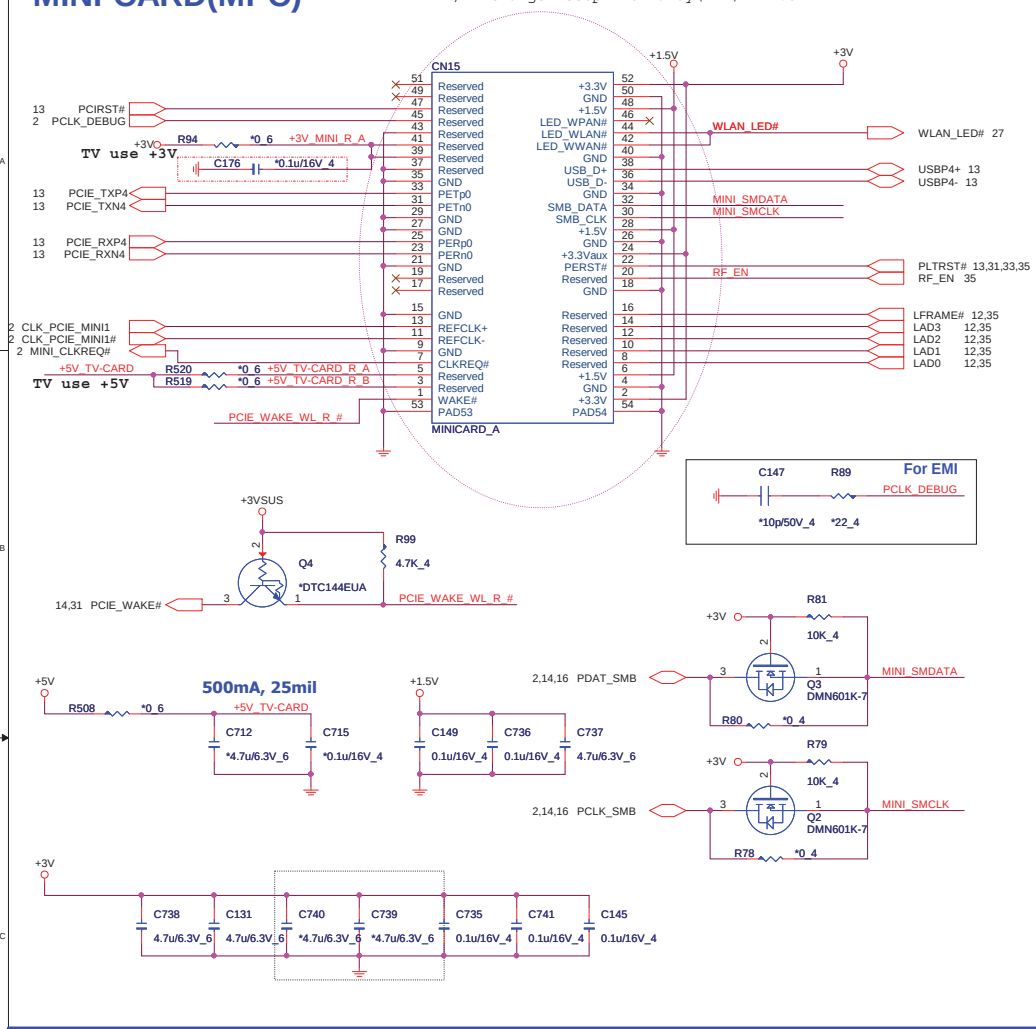


PROJECT : ZQ5
Quanta Computer Inc.

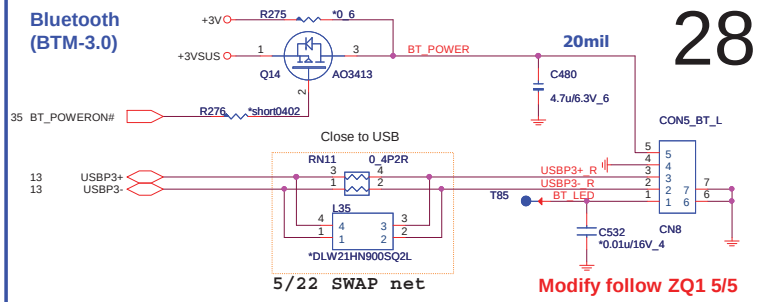
Size	Document Number	Rev
	HDD/ODD/LED/SW/TP/FAN/MMB	1A
Date: Monday, July 12, 2010	Sheet 27 of 43	

MINI-CARD(MPC)

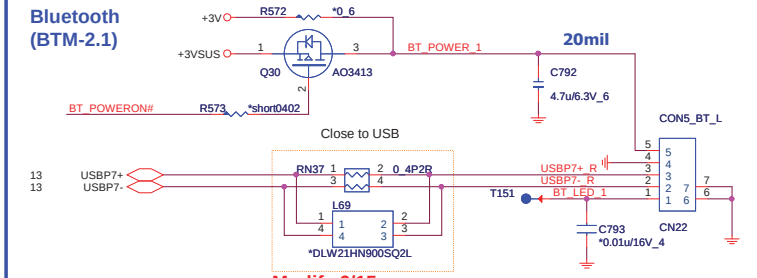
4/21 change footprint andy(ZYD) H=7.0



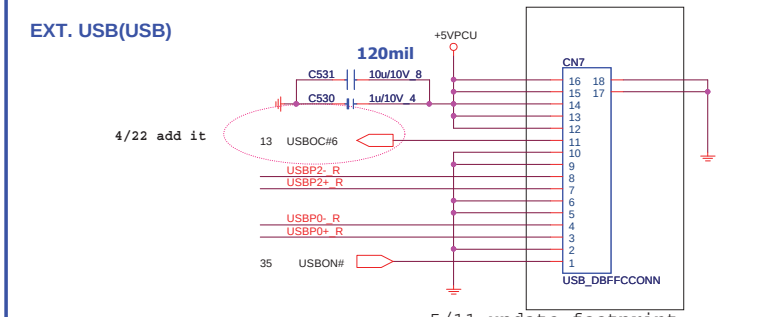
Bluetooth (BTM-3.0)

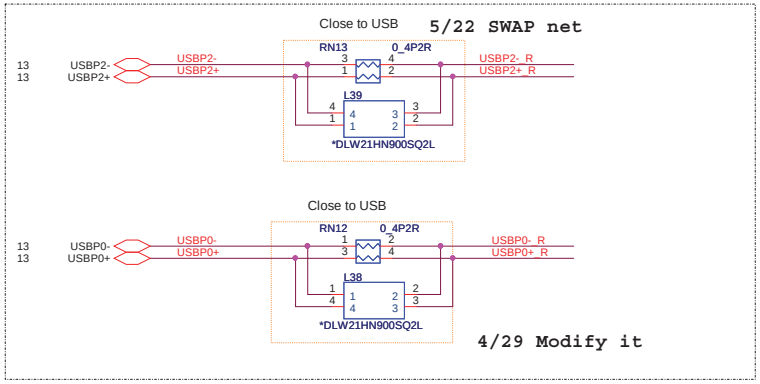


Bluetooth (BTM-2.1)



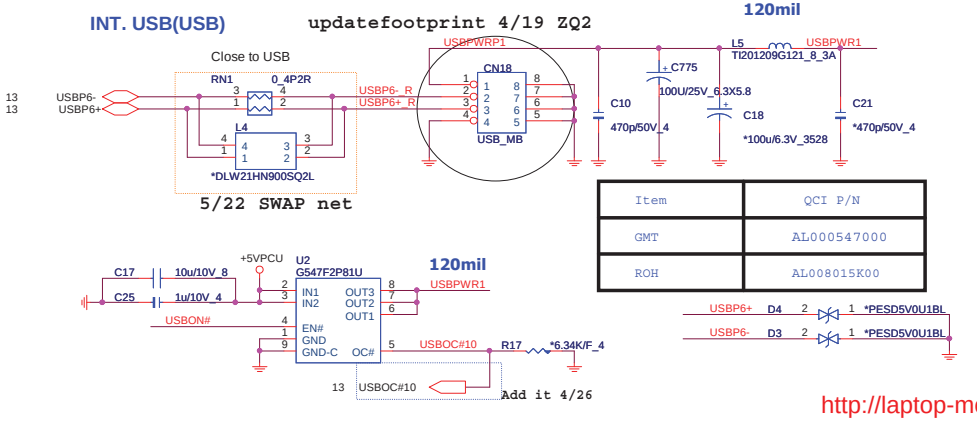
EXT. USB(USB)





INT. USB(USB)

updatefootprint 4/19 ZQ2



Item	QCI P/N
GMT	AL000547000
ROH	AL008015K00

PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	MINI/USB/BT/HOLE	1A
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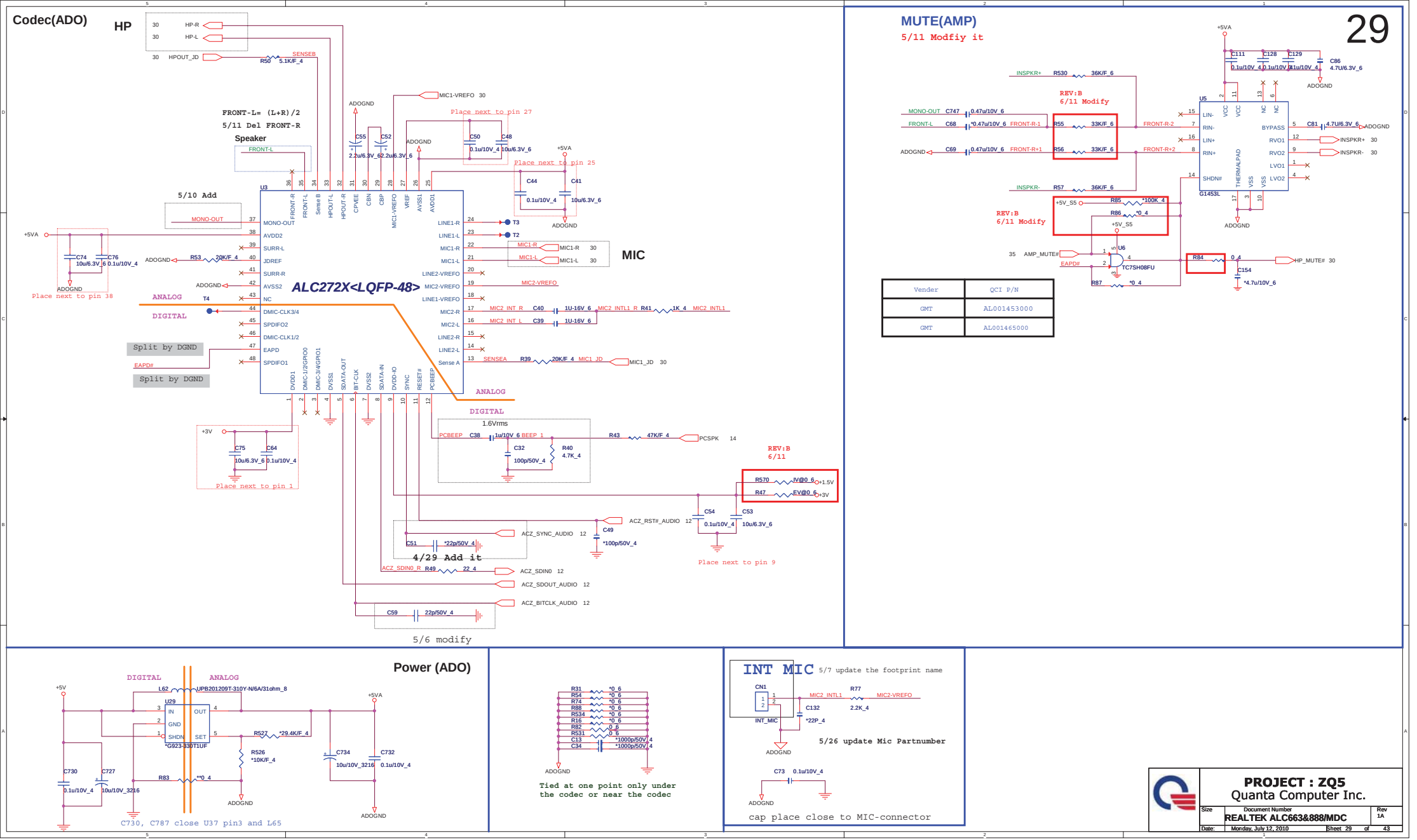
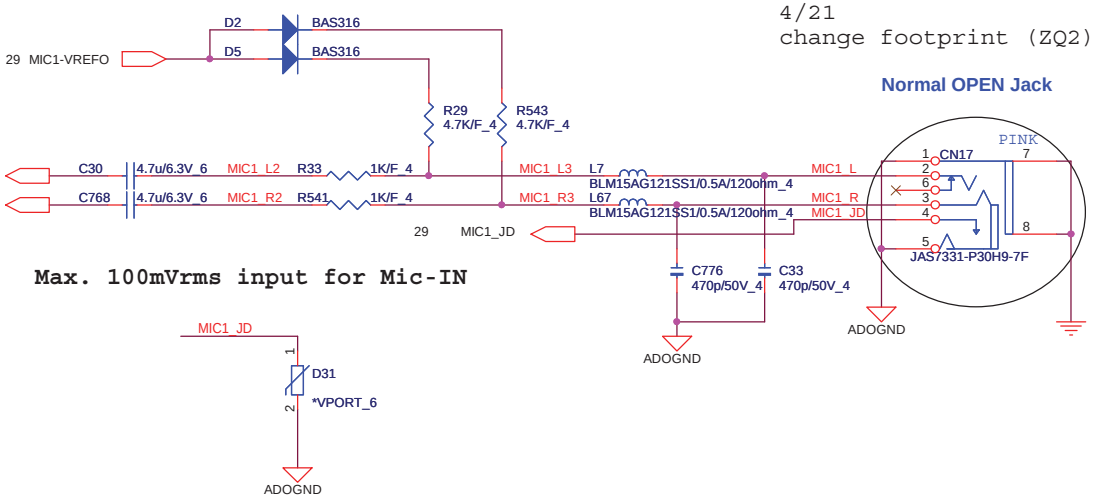


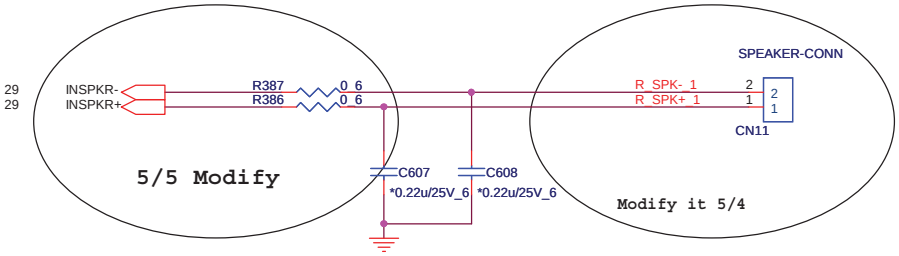
MIC



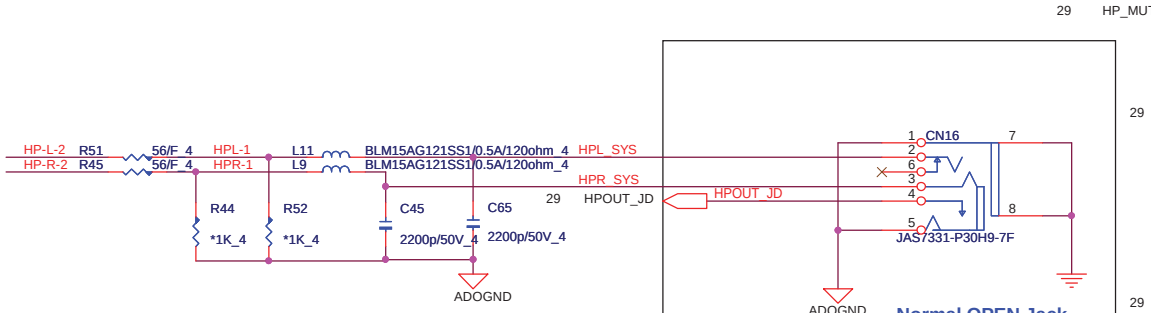
4/21
change footprint (ZQ2)

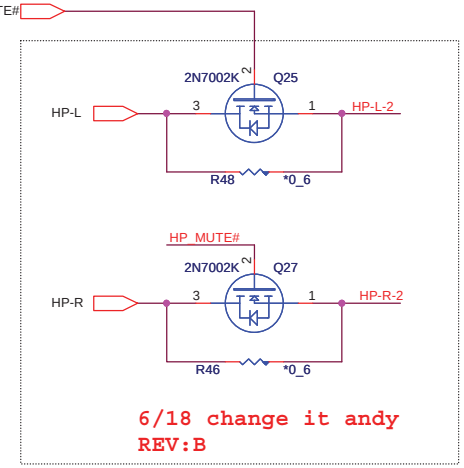
Normal OPEN Jack

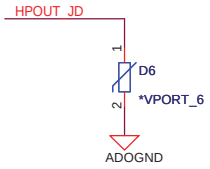
Internal Speaker



HP/SPDIF

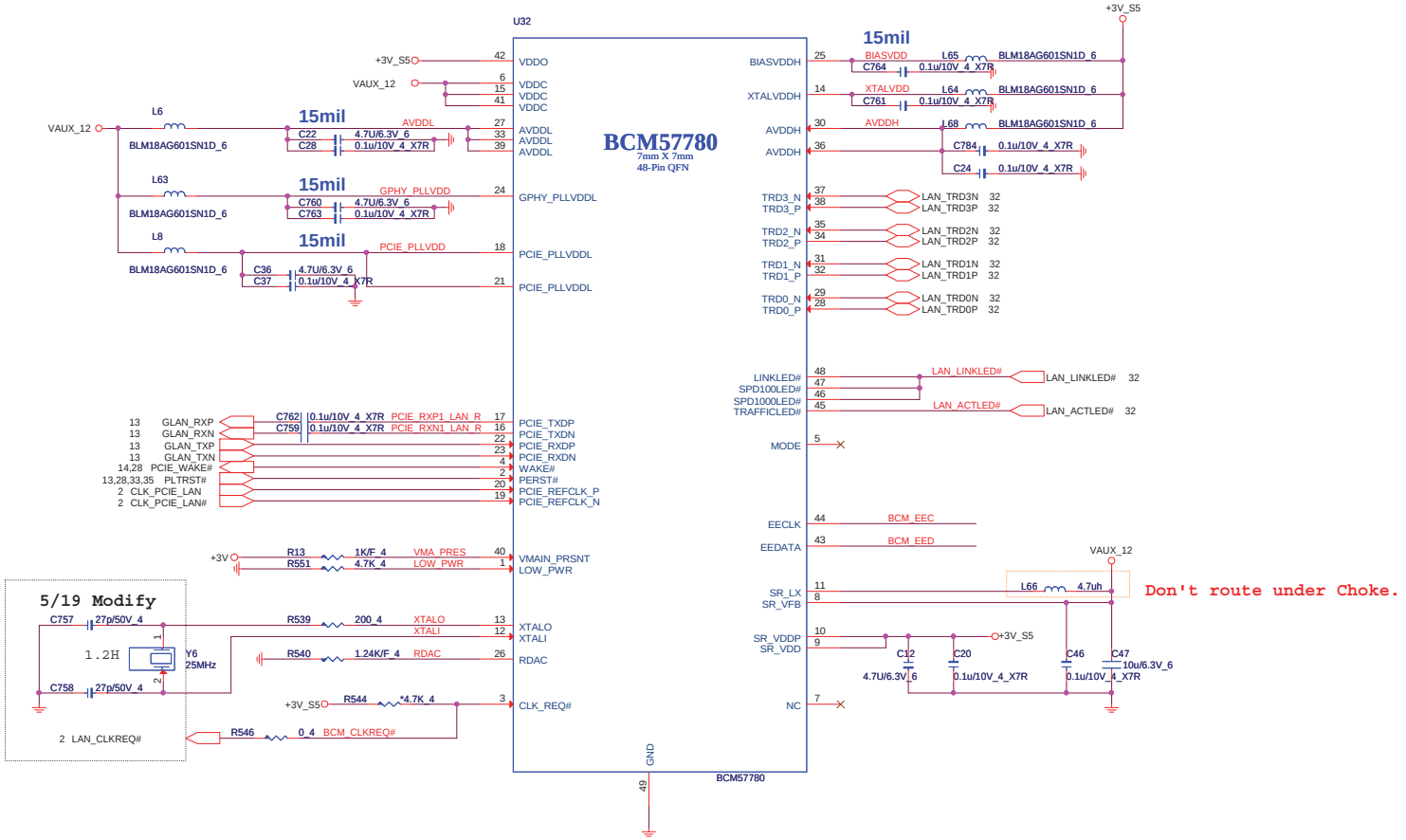




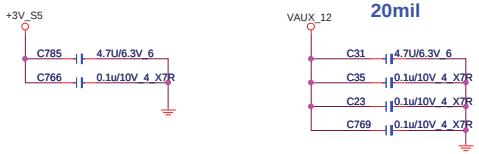


PROJECT : ZQ5
Quanta Computer Inc.

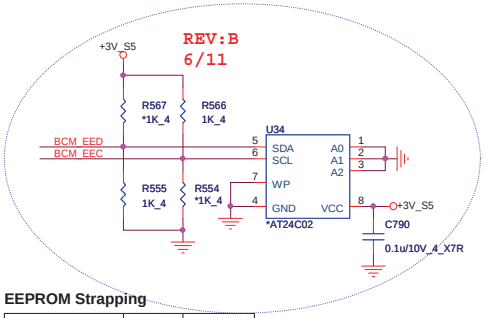
Size	Document Number	Rev
	AMP /AUDIO JACK CONN	1A
Date: Monday, July 12, 2010	Sheet 30 of 43	



LAN POWER



EEPROM



EEPROM Strapping

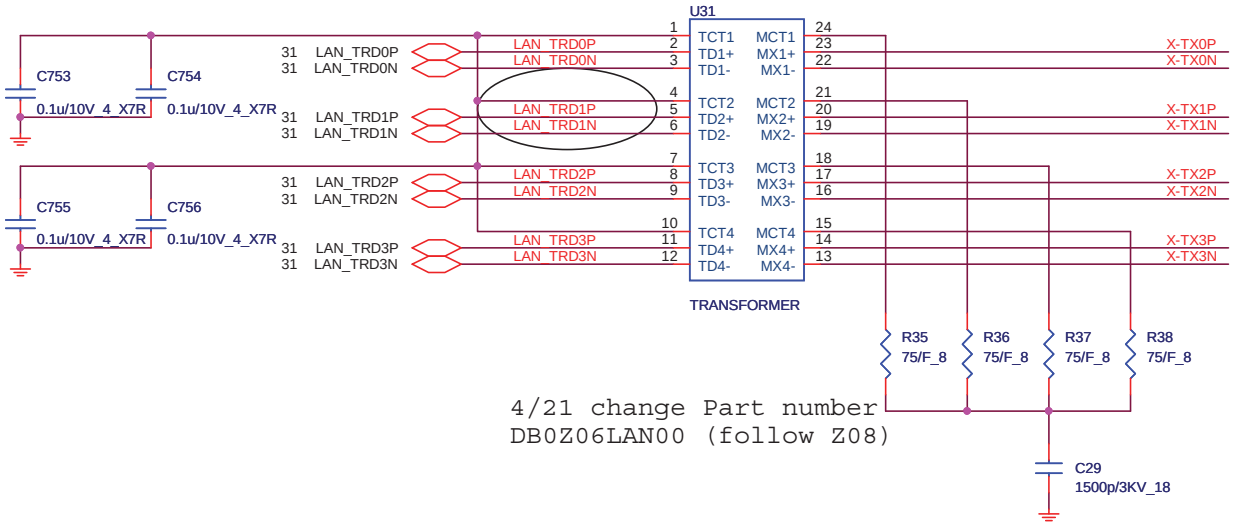
EEPROM Type	EECLK	EEDATA
24LC02	1	1
Internal	1	0

PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	GLAN BCM57780	1A
Date: Monday, July 12, 2010	Sheet 31 of 43	

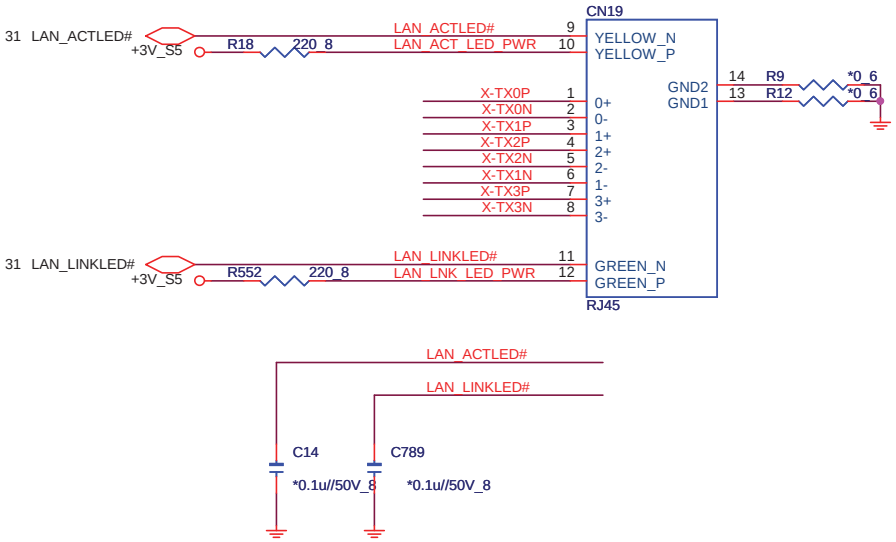
TRANSFORMER

4/27 modify it

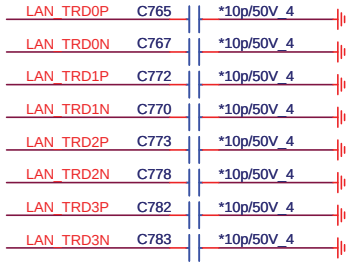


4/21 change Part number
DB0Z06LAN00 (follow Z08)

RJ45 Conn



For EMI



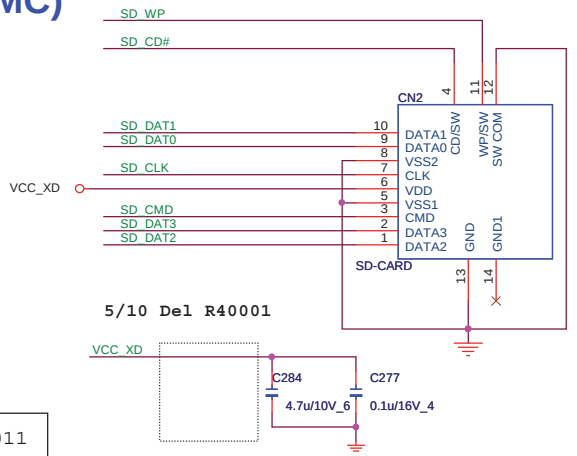
PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	LAN Transformer and RJ45	1A
Date: Monday, July 12, 2010	Sheet 32 of 43	

CARD READER Controller

33

2 IN 1 CARD READER (SD/MMC)



5/10 modify

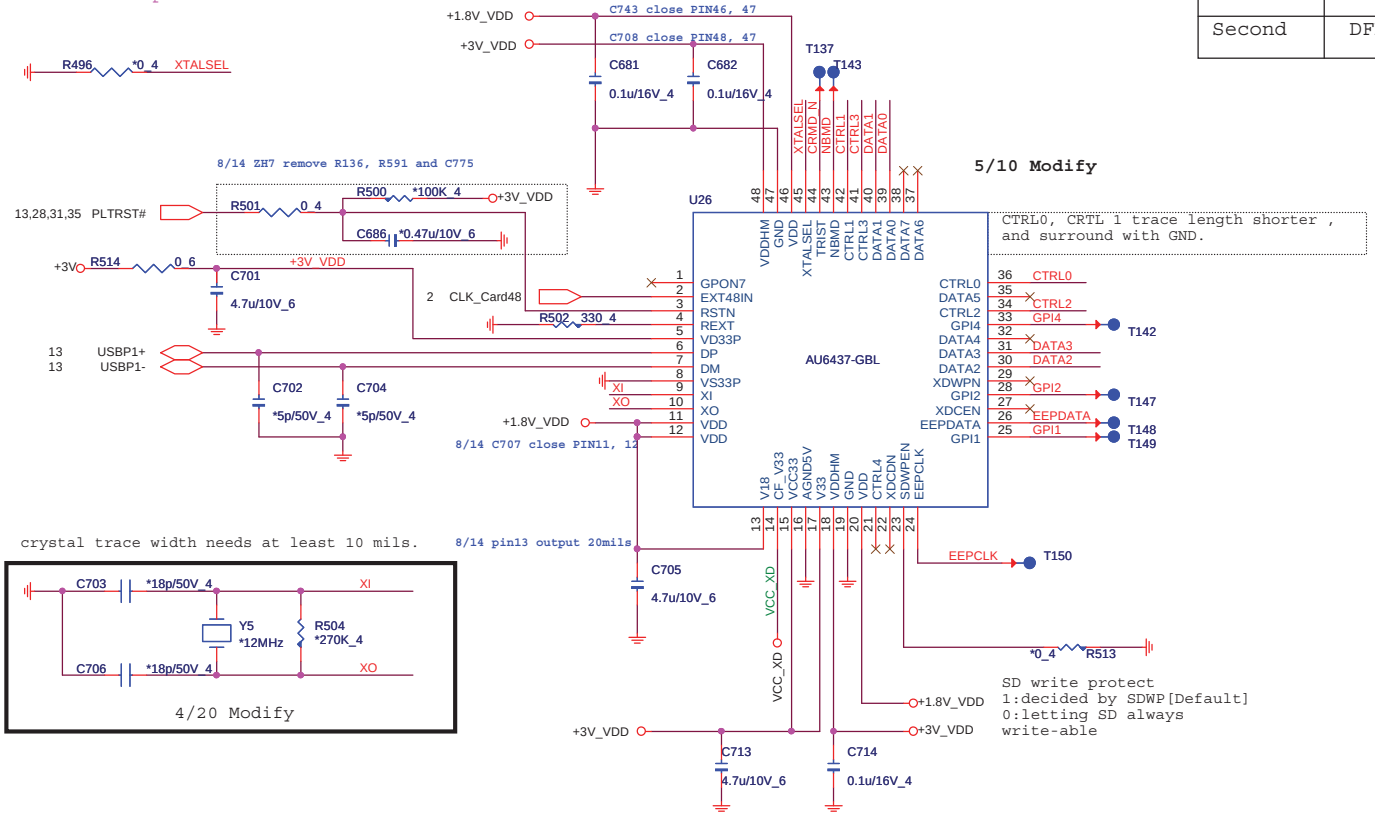
5/10 Del R40001

Close to CN14 pin 14 & pin23
4.7u CAP close to pin23

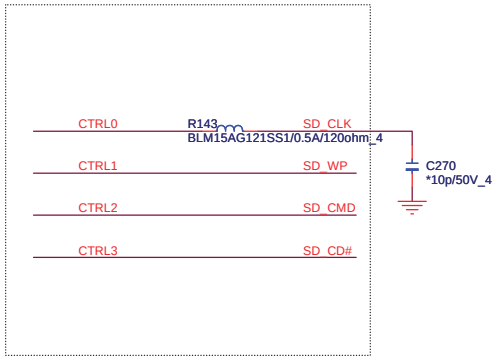
5/10 change Card Redaer conn
footpirnt sdcard-sdsn09-08-xa-11p-smt

Main	DFHS11FR011
Second	DFHS11FR033

Clock input selection
'1' for 48MHz input [Default,Internal PU]
'0' for 12MHz input



Close to connector



PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	AU6433 CardReader	1A
Date: Monday, July 12, 2010	Sheet 33 of 43	

(OTH)

HOLE10
*H-C315D118P2

HOLE4
*H-C315D118P2

HOLE13
*H-C315D118P2

HOLE12
H-C256D161P2

HOLE16
H-C256D161P2

HOLE8
H-C256D161P2

HOLE17
H-C197D87P2

HOLE9
*H-TC205BC276D146P2

HOLE6
*H-TC205BC276D146P2

HOLE7
*H-TC205BC276D146P2

5/21 Modify

HOLE15
HG-C315D154P2

HOLE5
*HG-C315D110P2

5/25 Modify

5/21 Modify

HOLE20
*H-C315I178D118P2

HOLE19
*HG-C315D118P2

HOLE1
*HG-C315D118P2

HOLE21
*HG-C315D118P2

HOLE3
*HG-C315D118P2

HOLE11
*HG-C315D118P2

HOLE2
*HG-C315D118P2

HOLE14
*H-C1417D1417N

7/08 Add for ME.

HOLE22
*h-o94x134d94x134n

7/08 Modify for ESD issue.

HOLE18
*H-C315I178D118P2

+3V_S5 — C427 — *0.1u/10V_4

+1.5V_SUS — C503 — *1000p/50V_4

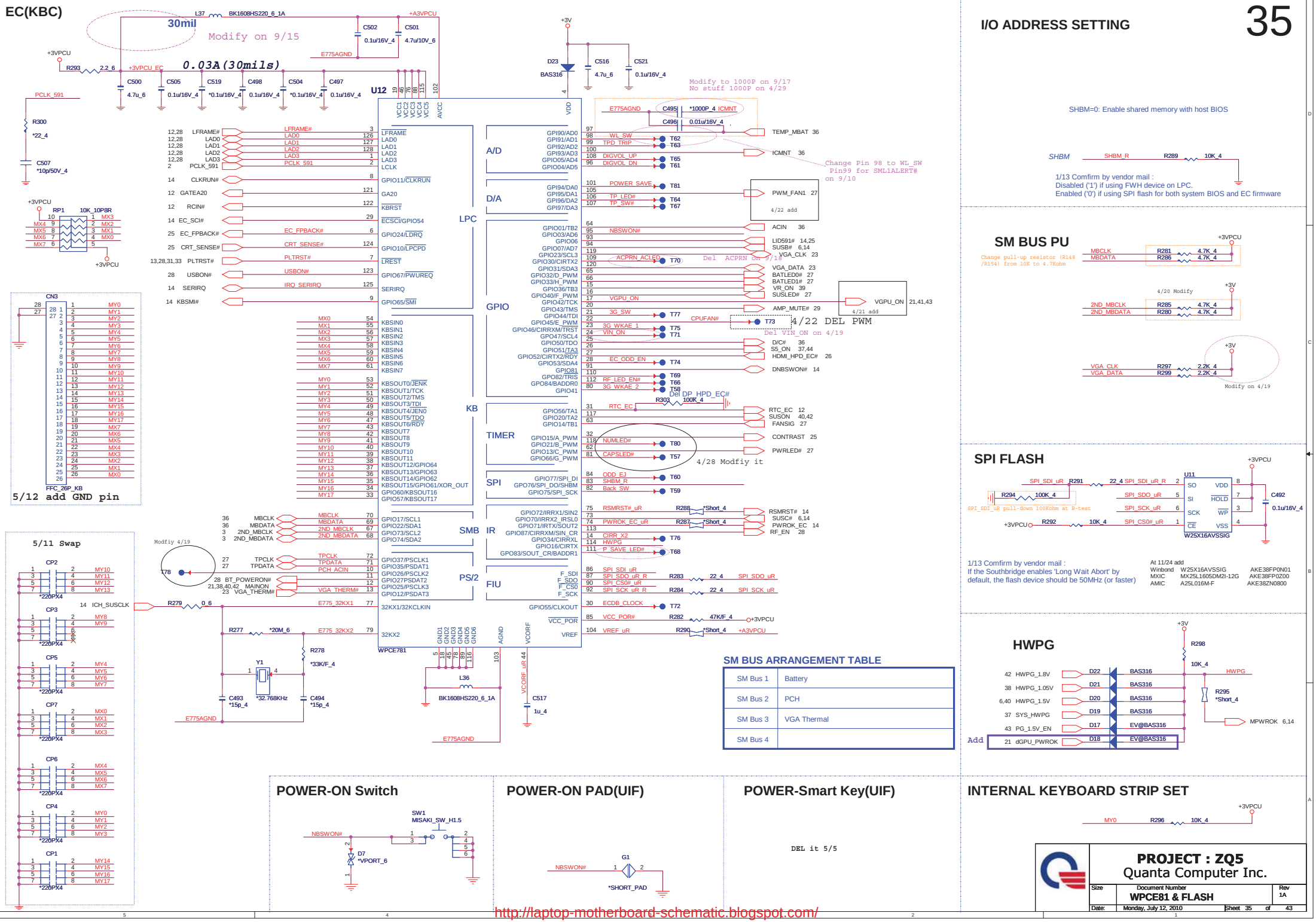
+1.05V — C368 — *1000p/50V_4

+VGPU_CORE — C77 — *1000p/50V_4

For EMI(EMI)

PROJECT : ZQ5 Quanta Computer Inc.		
Size	Document Number MINI/USB/BT/HOLE	Rev 1A
Date: Monday, July 12, 2010	Sheet 34 of 43	

EC(KBC)



I/O ADDRESS SETTING

35

SHBM=0: Enable shared memory with host BIOS

SHBM — SHBM_R — R289 — 10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU

Change pull-up resistor (R148 /R154) from 10K to 4.7Kohm

MBCLK — R281 — 4.7K_4
MBDATA — R286 — 4.7K_4

4/20 Modify

2ND_MBCLK — R285 — 4.7K_4
2ND_MBDATA — R280 — 4.7K_4

VGA_CLK — R297 — 2.2K_4
VGA_DATA — R299 — 2.2K_4

Modify on 4/19

SPI FLASH

1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

At 11/24 add

Winbond	W25X16AVSSIG	AKE38FP0N01
MXIC	MX25L1605DM2I-12G	AKE38FP0Z00
AMIC	A25L016M-F	AKE38ZN0800

HWPG

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	VGA Thermal
SM Bus 4	

POWER-ON Switch

POWER-ON PAD(UIF)

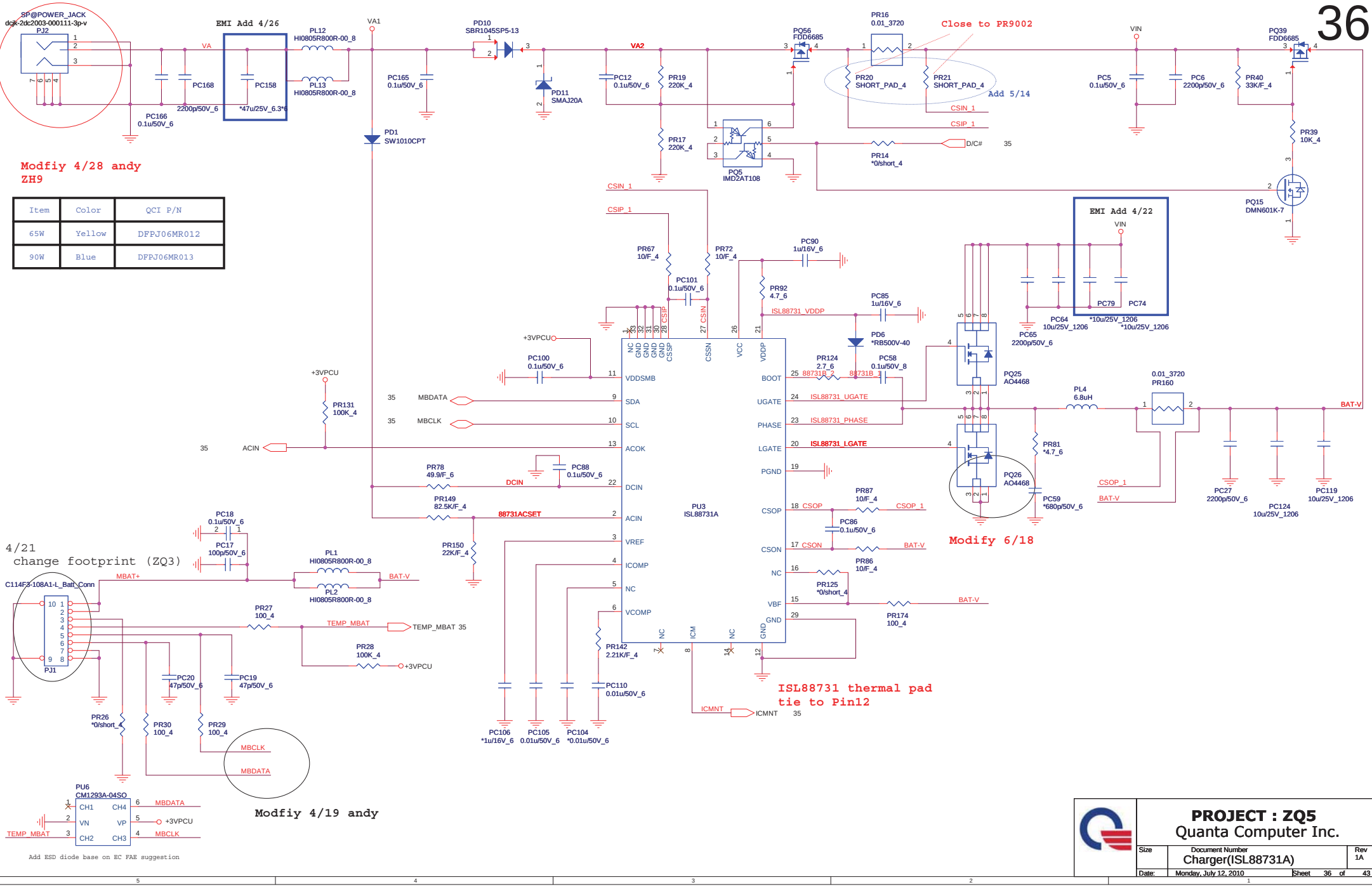
POWER-Smart Key(UIF)

DEL it 5/5

INTERNAL KEYBOARD STRIP SET

PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	WPCE81 & FLASH	1A
Date: Monday, July 12, 2010	Sheet 35 of 43	



PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	Charger(ISL88731A)	1A
Date: Monday, July 12, 2010	Sheet 36 of 43	

SUSD → SUSD 42
MAIND → MAIND 40,42

3,44 SYS_SHDN# → PR169 *0/short_4

VL → PR156 39K/F_4 → 3V5V_EN → PR143 *0/short_4
3V5V_EN → PR168 *0/short_4 → 5V_EN
3V_EN

VIN → PC94 100u/25V_6X7.7
PC26 2.2n/50V_6
PC127 *10u/25V_1206
PC25 10u/25V_1206

OCP:7A
5.4A
+5VPCU

Change footprint 5/14
Modify 6/18

PQ14 AO4468 (5V_DH)
PQ13 AO4710 (5V_DL)
PL8 2.2uH_7X7X3 (5V_LX)
PR167 *0_4
PR175 *4.7_6
PD2 *SX34
PC21 0.1u/50V_6
PC128 *680p/50V_6
PC23 *10u/25V_1206
PR44 *0/short_4
PC134 330u/6.3V_6X5.7
+5VPCU_FB

PU4 RT8206B
BYP, OUT1, FB1, ILIM1, PGOOD1, EN1, DH1, LX1, PAD, PAD, PAD
LDOREFIN, LDO, VIN, NC, ONLDO, VCC, TON, REF
REFIN2, ILIM2, OUT2, SKIP#, PGOOD2, EN2, DH2, LX2
PAD, PAD, PAD, BST1, LDO, PVCC, NC, GND, PGND, DL2, BST2

8206_ONLDO
DDPWRGD_R
5V_EN
3V_EN
SKIP
REF
REFIN2

PR43 169K/F_4
PR158 390K_4
PR159 150K_4
PC117 0.1u/50V_6
PC116 0.01u/16V_4
PC122 4.7u/10V_8
PR153 *0/short_4
PR157 *0/short_4
PC111 1u/16V_6
PC109 0.1u/50V_6
PR151 *0_6
PR148 *0_4
PR57 220K/F_4
PR164 1/F_6
PR152 1/F_6
PC108 0.1u/50V_6
PC121 0.1u/50V_6

PR46 *0_6
PC43 0.1u/50V_6
PC112 1u/16V_6
PR170 *0/short_6
PD3 CHN217
PD4 CHN217
PC48 0.1u/50V_6
PC42 0.1u/50V_6
PR50 *0/short_6
PR80 22_8
PR77 *200K/F_4
PC51 0.1u/50V_6
PR47 *39K/F_4

OCP:7A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
~2.525A
Iocp=7-(2.525/2)=5.74A
Vth=5.74A*14.2mOhm=0.08147V
R(Ilim)=(81.47mV*10)/5uA=163K
I_peak(choke)=11.187A

OCP:9A
7A
+3VPCU

Change footprint 5/14
Modify 6/18

PQ21 AO4468 (3V_DH)
PQ22 AO4710 (3V_DL)
PL3 2.2uH_7X7X3 (3V_LX)
PD5 *SX34
PR91 *4.7_6
PC63 *680p/50V_6
PR140 *0_4
PC95 0.1u/50V_6
PC84 330u/6.3V_6X5.7
PR146 *0/short_4
PR147 *0_4
+3VPCU_OUT
PR141 *0_4
PR55 *0_4
PR56 *0/short_4

OCP:9A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)=1.9A
Iocp=9-(1.9/2)=8.05A
Vth=8.05A*14.2mOhm=0.11431V
R(Ilim)=(114.31mV*10)/5uA=228.62K
I_peak(choke)=11.479A

PR144 *100K/F_4
PR145 *0/short_4
DDPWRGD_R → SYS_HWPG 35

VIN → PR34 1M_6 → PR33 1M_6 → PQ7 DTC144EU
35,44 S5_ON
+3V_S5 → PR36 22_8 → PQ10 DMN601K-7
+5V_S5 → PR35 22_8 → PQ11 DMN601K-7
+15V → PR32 1M_6
VIN → PR31 *1M_6
S5D → PQ8 AO3404 → +5V_S5
PQ9 DMN601K-7
PC22 *2.2n/50V_4

0.002A

+5VPCU → PQ42 AO4468 (MAIND) → +5V
2.4A

+3VPCU → PQ28 AO4468 (MAIND) → +3V
4.01A

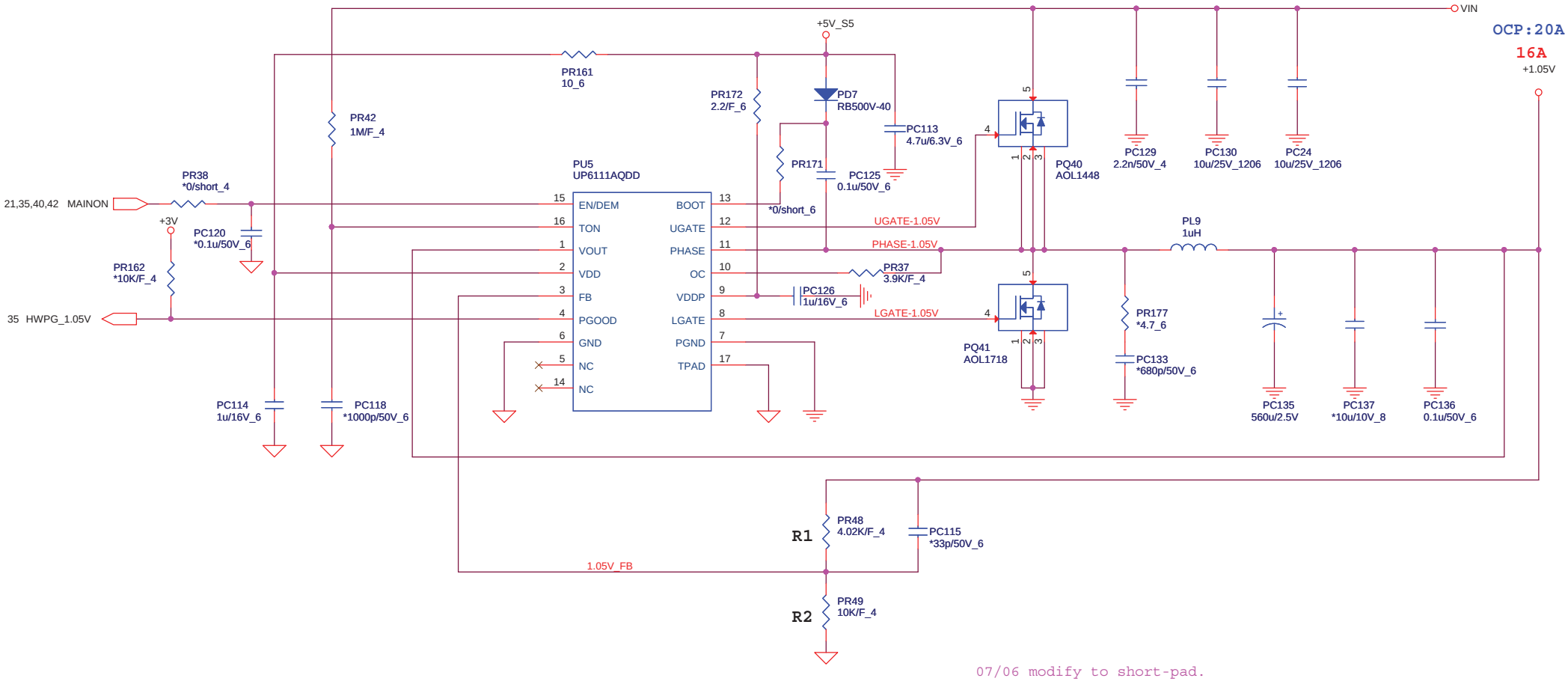
Modfiy 4/19 andy
+3VPCU → PQ24 AO4468 (S5D) → +3V_S5
2.8A

+3VPCU → PQ23 AO3404 (SUSD) → +3VSUS
0.21A

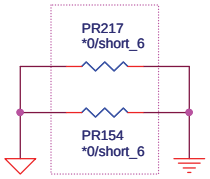
PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	SYSTEM 5V/3V (RT8206)	1A
Date: Monday, July 12, 2010	Sheet 37 of 43	

[PWM]



07/06 modify to short-pad.

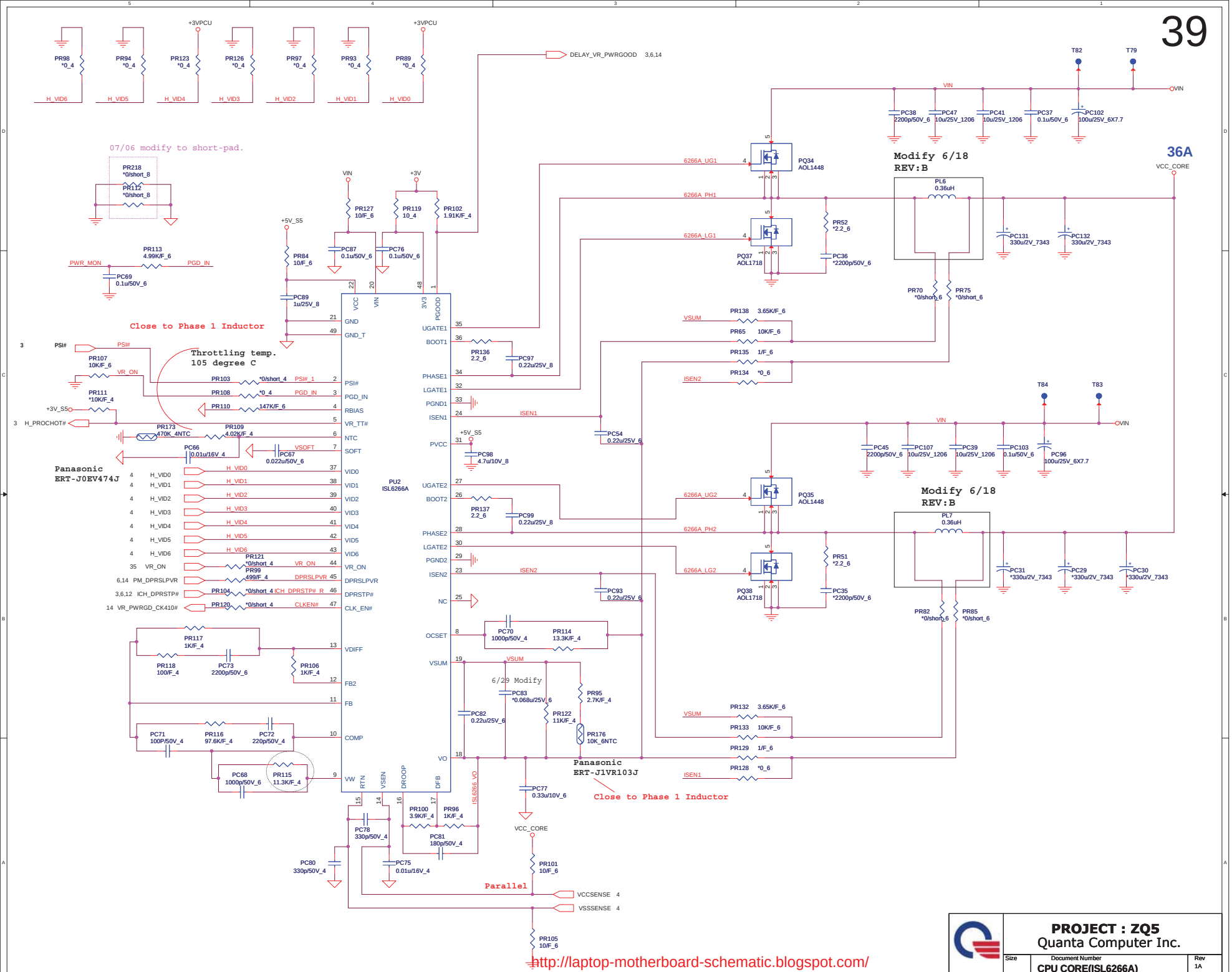


TON=3.85p*RTON*Vout/(Vin-0.5)
Frequency=Vout/(Vin*TON)
TON=3.85p*1M*1/(Vin-0.5)
Frequency=1/(0.0036767)=272K

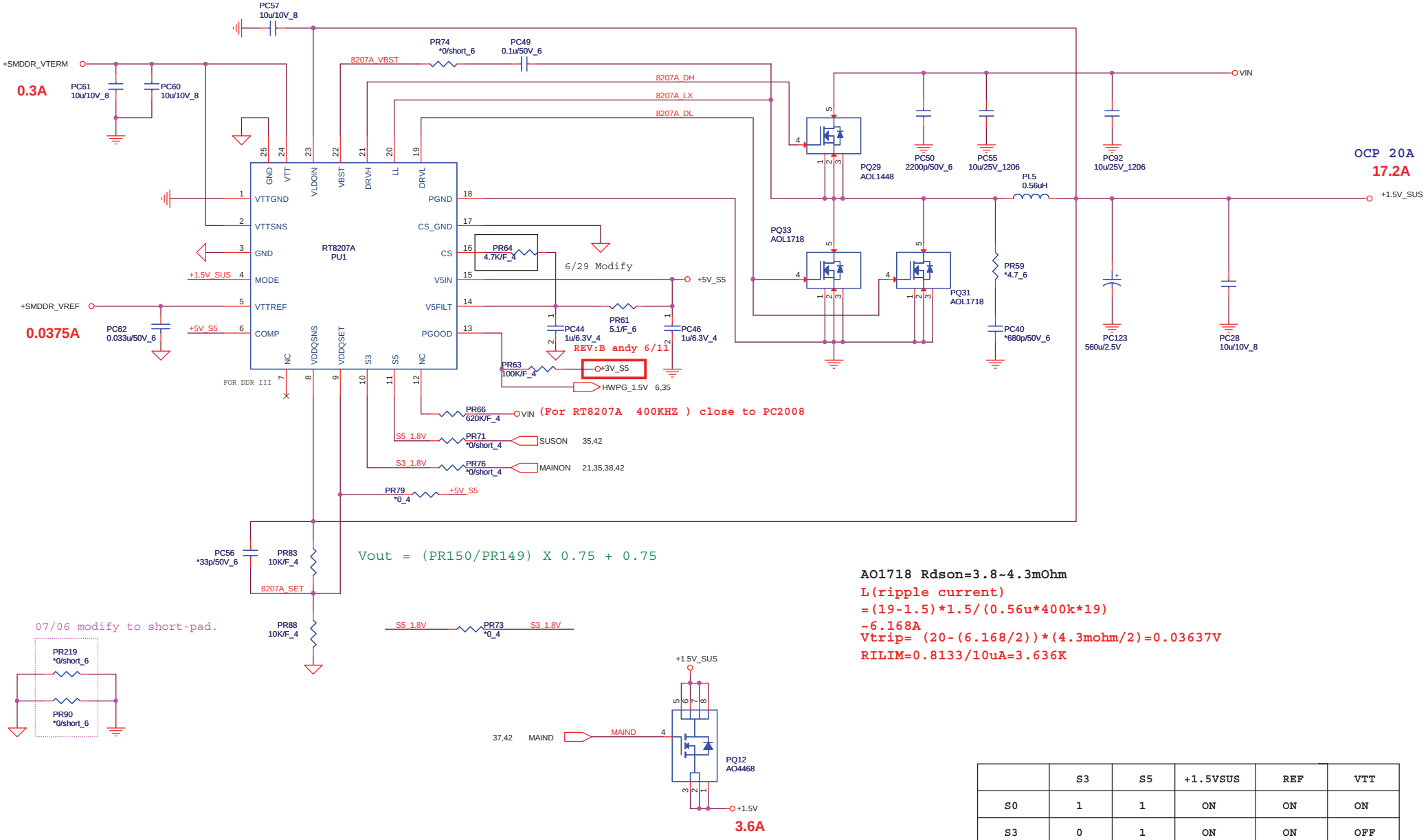
L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.647A
RILIM=4.3mohm*20-1.823/20uA=3.907Kohm
I(choke)peak=23.647A

PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	+1.05V (UP6111A)	1A
Date: Monday, July 12, 2010	Sheet 38 of 43	



PROJECT : ZQ5		
Quanta Computer Inc.		
Size	Document Number	Rev
	CPU CORE(ISL6266A)	1A
Date: Monday, July 12, 2010	Sheet 39 of 43	



AO1718 Rdson=3.8~4.3mOhm

L(ripple current)
=(19-1.5)*1.5/(0.56u*400k*19)
~6.168A

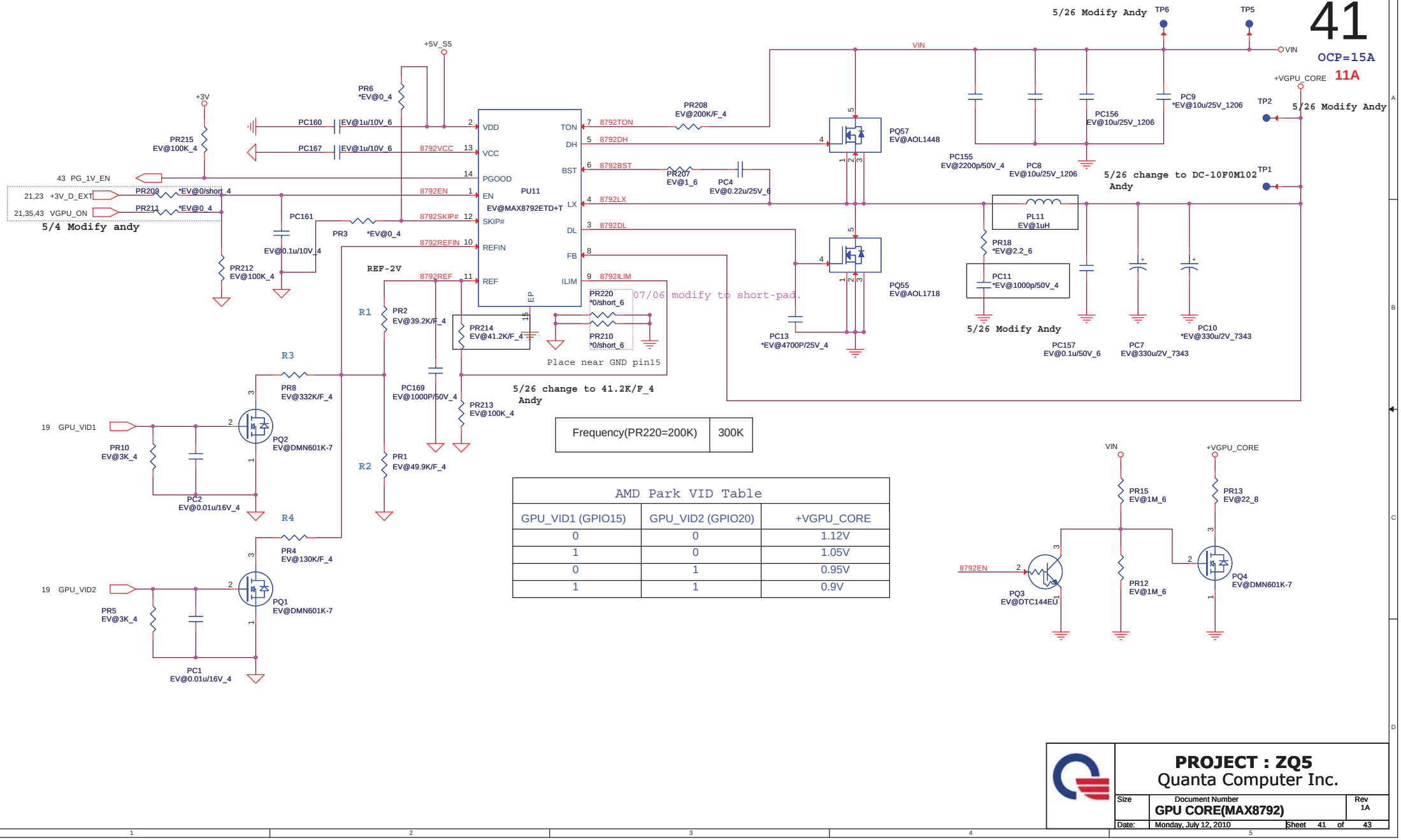
Vtrip= (20-(6.168/2))*(4.3mohm/2)=0.03637V

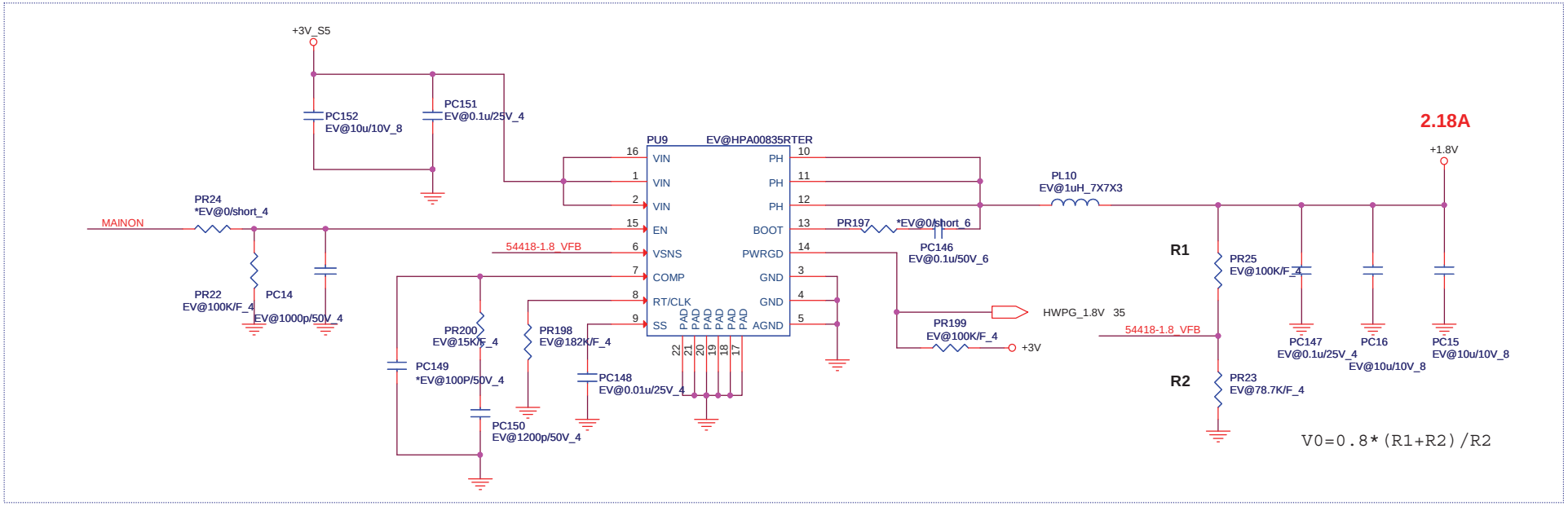
RILIM=0.8133/10uA=3.636K

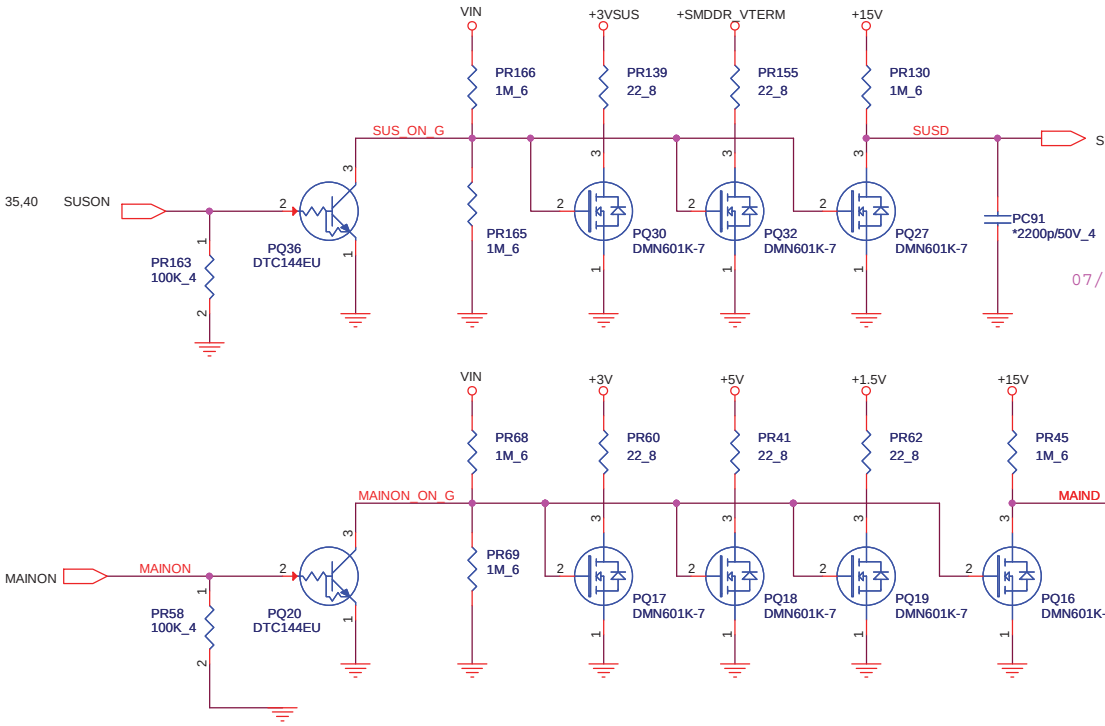
	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

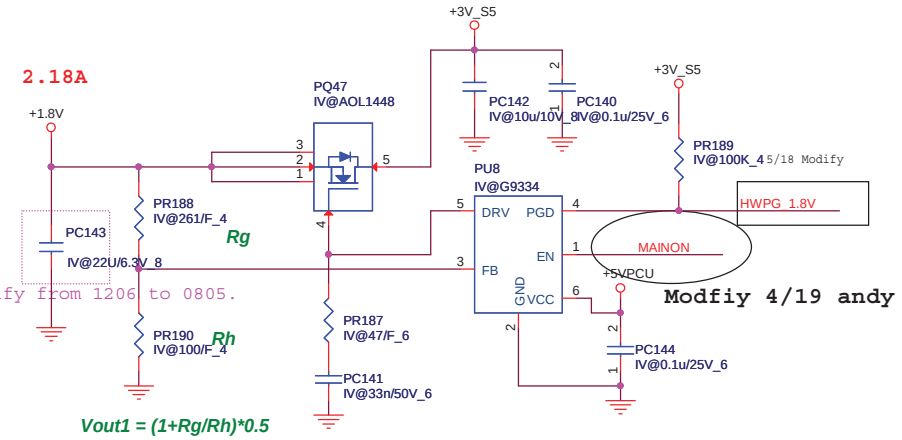
PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A
Date: Monday, July 12, 2010	Sheet 40 of 43	



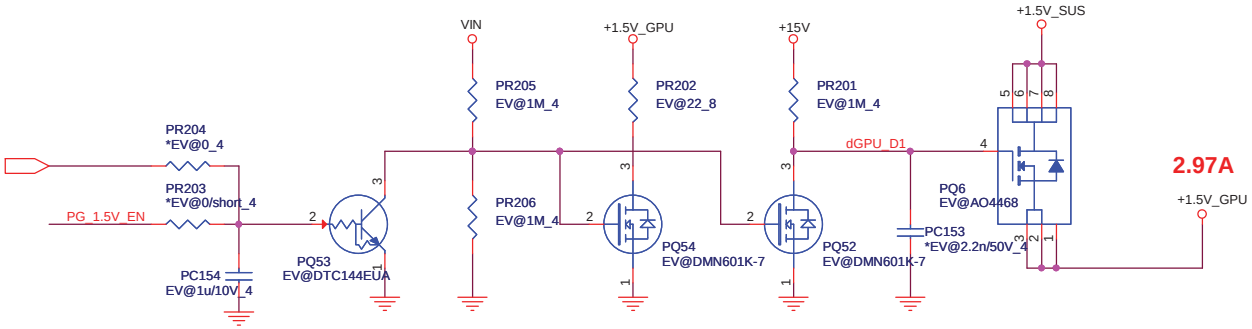


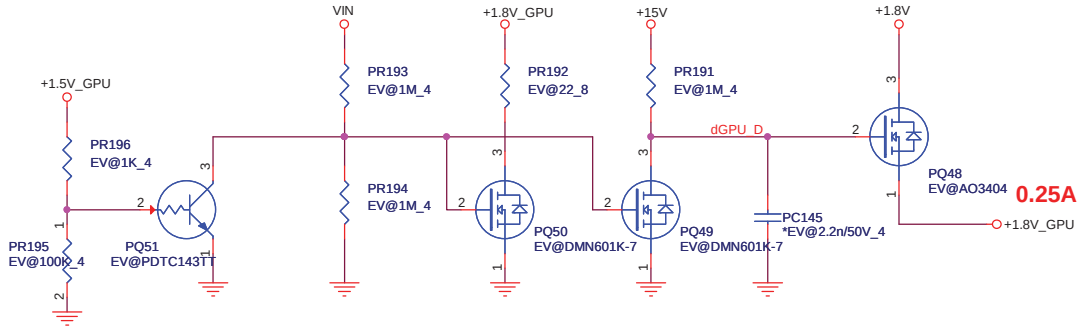


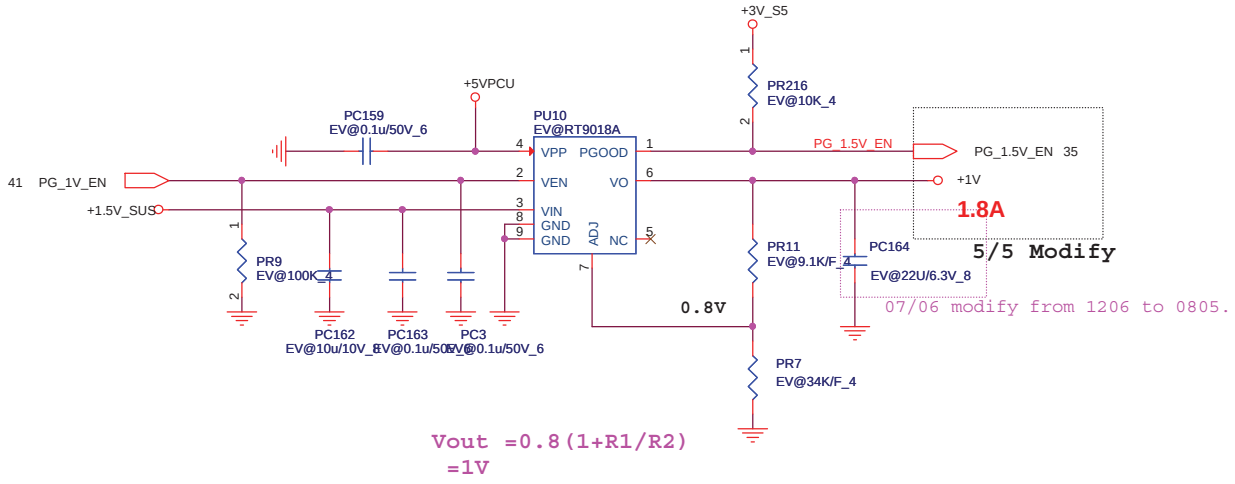


PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	VCCP 1.8V(UP6111A)	1A
Date: Monday, July 12, 2010	Sheet 42 of 43	



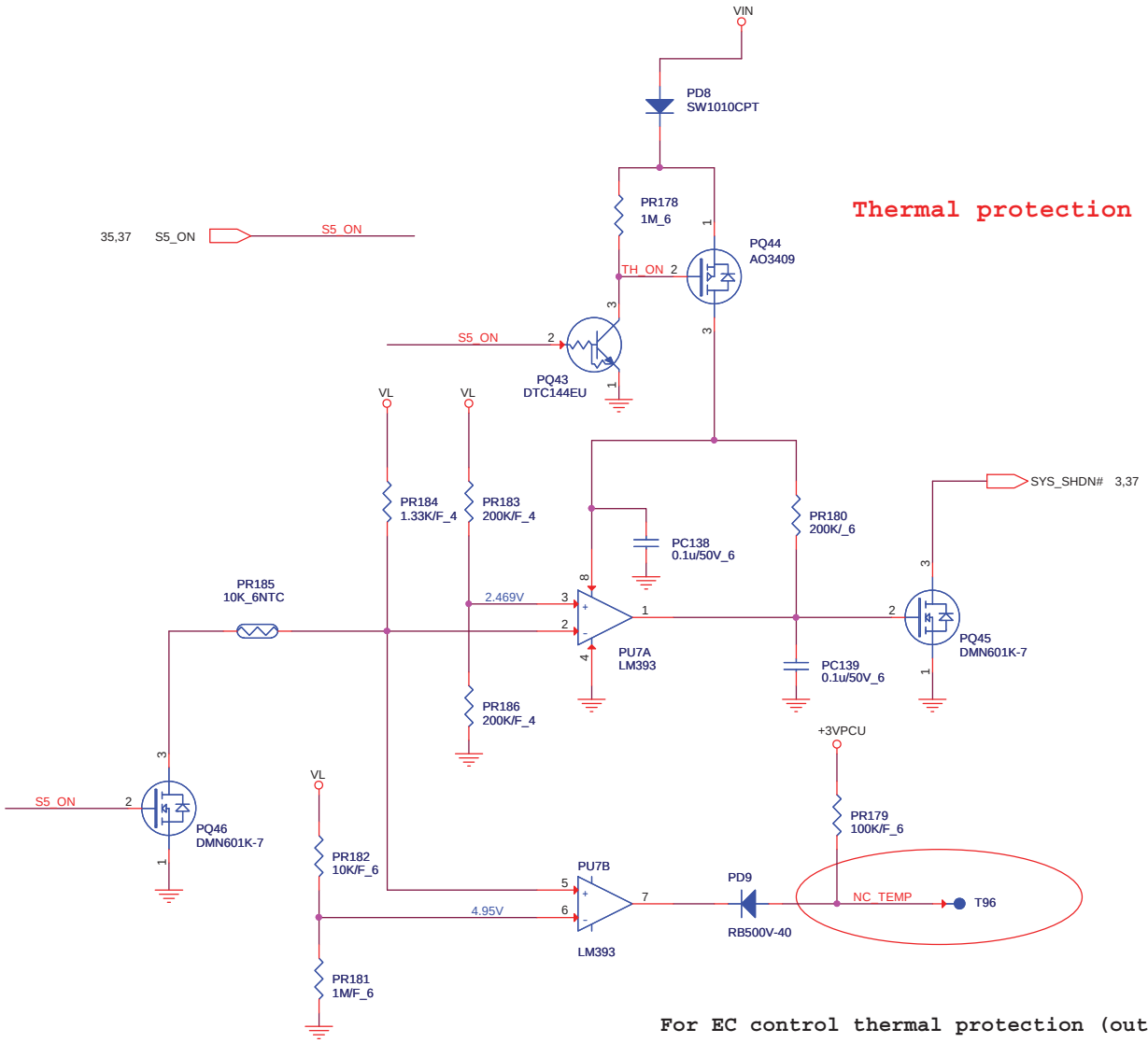




PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	GPU_POWER	1A
Date: Monday, July 12, 2010	Sheet 43 of 43	

Thermal protection



For EC control thermal protection (output 3.3V)

PROJECT : ZQ5 Quanta Computer Inc.		
Size	Document Number: Thermal Protection	Rev: 1A
Date: Monday, July 12, 2010	Sheet 44 of 43	

MODEL: REV

CHANGE LIST

MODEL / PAGE	ZR6 MB FROM	ZR6 MB TO
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	
16	1A	
17	1A	
18	1A	
19	1A	
20	1A	
21	1A	
22	1A	
23	1A	
24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	
31	1A	
32	1A	
33	1A	
34	1A	
35	1A	
36	1A	
37	1A	
38	1A	
39	1A	
40	1A	
41	1A	
42	1A	
43	1A	
44	1A	
45	1A	

ZQ5 MB

A *First release*

C

1.Page40:change HWPG_1.5V pull up to +3V_S5 for S3 issue
2.Page29:Add R570 pull up +1.5V for uma Audio I/O
3.Page26:Swap HDMI Lane2 for HDMI issue
4.Page31:U34 and R567 no stuff ,R555 stuff it for LAN ID issue
5.Page02:Q12 and Q13 change Part number from BAM700200F6 to BAM700200H2
6.Page29:R55 and R56 change Part number to CS33303F911(33K) for Audio
7.Page29:change R86 and U6 Pin5 pull up to +5V_S5
8.Page29:change R84 value to 0 ohm
9.Page30:change Q25 and Q27 Part number to BAM70020002 as ZYB
10.Page25:L1,L2,L3 change to CX8LL680001
11.Page25:C1,C2,C3,C5,C6,C7 change to CH-5006JBD4
12.Page25:R11,R14 change to CS01502JB12
13.Page28:Add another BT circuit (USB port5),Add Q30,RN37,C792,CN22
14.Page07:Change R425,R426 to CS02492FB29 for CRT issue
15.Page13:Change BT 2.1 to USB port 7
16.Page28:Change BT 2.1 to USB port 7
17.Page25:chage 0805 to SHORT Pad R71,R72,R98,R146
18.Page29:Stuff R84 U6 and no stuff R86 for Audio bobo noise
19.Page10:change R171 and R429 to bead CX8PG181001
20.Page30:stuff Q25 and Q27 and no stuff R46 R48 for Audio bobo noise
21.Page40:Add PR219
22.Page38:Add PR217
23.Page41:Add PR220
24.Page39:Add PR218
25.Page36: Change PR16 (0.01/F_7520) to CS+0108GL13 (0.01_3720)
26.Page41: DEL JP1 and JP4
27.Page39: DEL JP2 and JP3
28.Page38:change PR171,PR38 to short Pad
29.Page36:change PR125,PR14,PR26 to short Pad
30.Page37:change PR143,PR145,PR146,PR153,PR157,PR168,PR169,PR170,PR50,PR44,PR56 to short Pad
31.Page39:change PR120,PR121,PR104,PR103,PR70,PR75,PR82,PR85 to short Pad
32.Page40:change PR71,PR76,PR74 to short Pad
33.Page41:change PR209 to short Pad (EV@)
34.Page42:change PR24,PR197 to short Pad (EV@)
35.Page43:change PR203 to short Pad (EV@)
36.Page36:Change PQ26 to AO4468 (P/N：BAM44680003)
37.Page37:PD2 and PD5 no stuff
38.Page39:PC29 and PC31 no stuff
39.Page36:PJ1 change Part number to DFHD08MR140

D

01.Page39:PC83 no stuff
02.Page39:Change PR64 to CS24702FB10
03.Page16: Del C539 (*10U/6.3V_6).
04.Page17: Del C538 (*10U/6.3V_6).
05.Page38: Change AGND (0 ohm) to Short Pad(0603): PR154、PR217.
06.Page40: Change AGND (0 ohm) to Short Pad(0603): PR219、PR90.
07.Page41: Change AGND (0 ohm) to Short Pad(0603): PR210、PR220.
08.Page39:Change AGND (0 ohm) to Short Pad(0805): PR112,PR218.
09.Page43:Change PC164 (22uF/10V_1206) to CH6221M9A07 (22uF/6.3V_0805)
10.Page42:Change PC143 (22uF/10V_1206) to CH6221M9A07 (22uF/6.3V_0805)
11.Page34:Modify HOLE18 to dummy net.
12.Page34:Add HOLE22 for ME.

MB Assy' P/N: 31ZQ5MB0000 | Project :ZQ5 MB | Document No.:

Approved by : Andy_Lin | Drawing by :Andy Chen | DATE: 2009/03/04

PROJECT : ZQ5
Quanta Computer Inc.

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