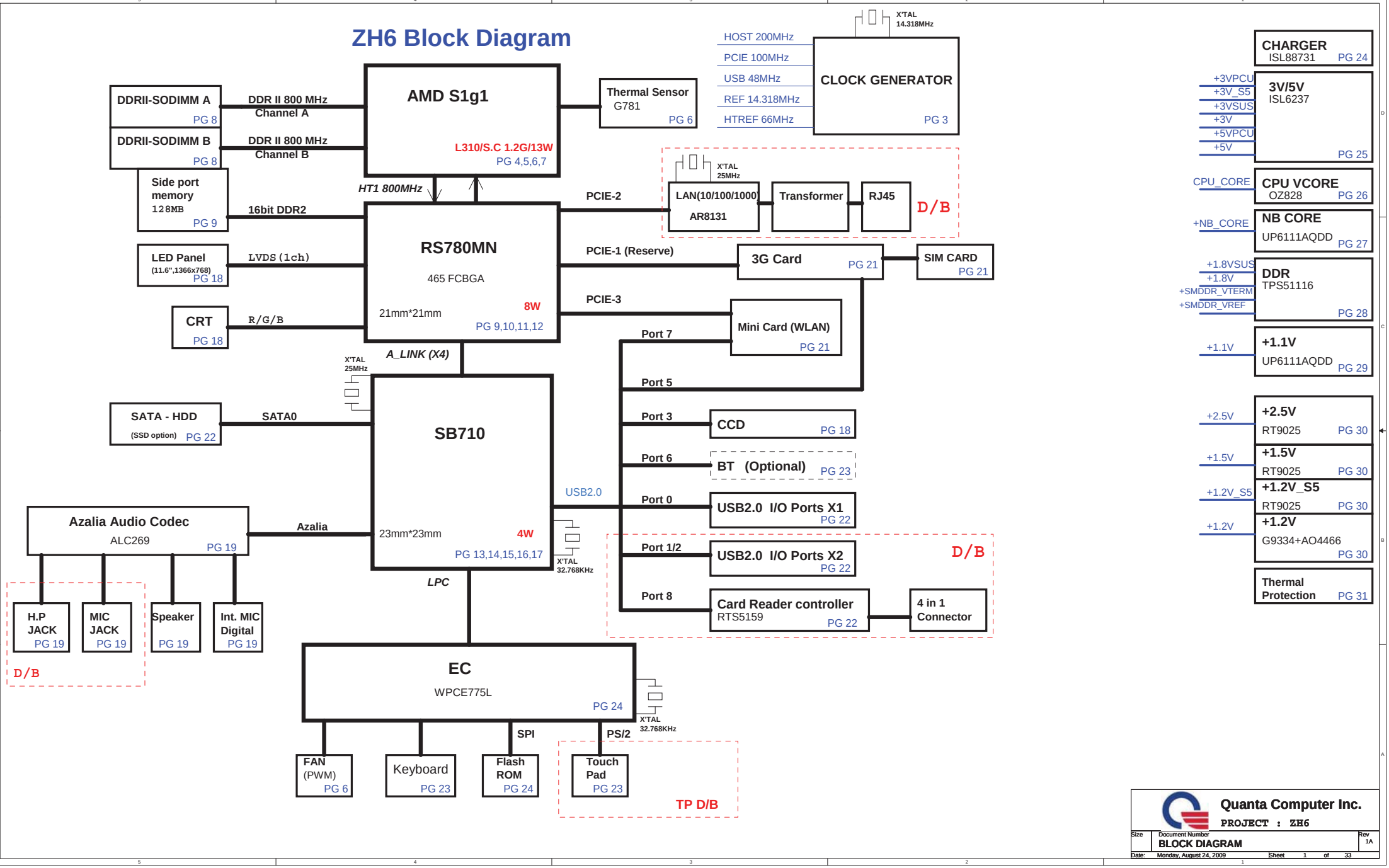
ZH6 Block Diagram



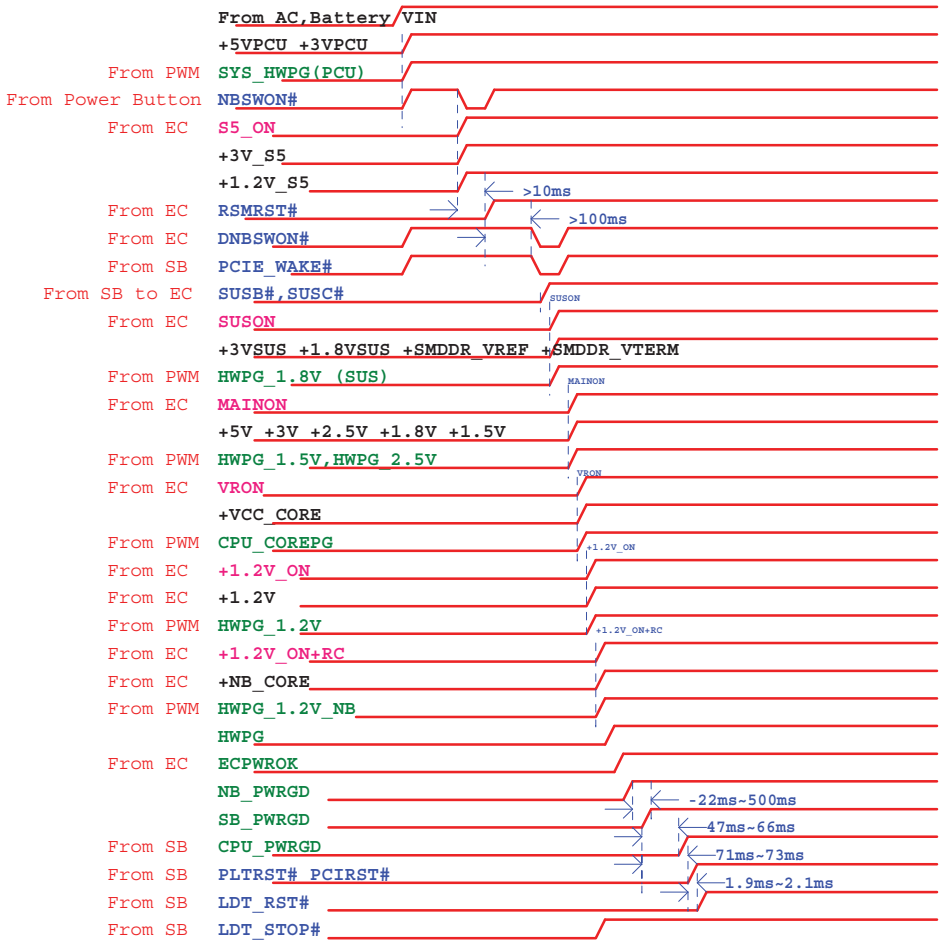
Quanta Computer Inc.

PROJECT : ZH6

Size	Document Number	Rev
	BLOCK DIAGRAM	1A

Date: Monday, August 24, 2009 Sheet 1 of 33

ZH6 Power On Sequence



*Note: EC will sampling SUSB# & SUSC# every 5ms.

BOM naming rule

Items	Function	Name	Description
1	3G Module	3G@	
2	HDT debug function	HDT@	
3			
4			
5			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			

AMD SB710 SMBUS Table

	CLK GEN	RAM	Mini Card (WLAN)
SB710 SDATA0/SCLK0(+3V)	V	V	V
SB710 SDATA1/SCLK1(+3V_S5)			
Power Plane	+3V	+3V	+3V
MOS CKT	Reserve	Reserve	Reserve

EC SMBUS Table

	Battery	CPU thermal Sensor	EC EEPROM
EC775 SDATA1/SCLK1(+3VPCU)	V		
EC775 SDATA2/SCLK2(+3VPCU)		V	
EC775 SDATA3/SCLK3(+3VPCU)			V
EC775 SDATA4/SCLK4(+3VPCU)			
Power Plane	+3VPCU	+3V	+3VPCU
MOS CKT	X	X	X

Quanta Computer Inc.
PROJECT : ZH6
Size | Document Number: SYSTEM INFORMATION | Rev 1A
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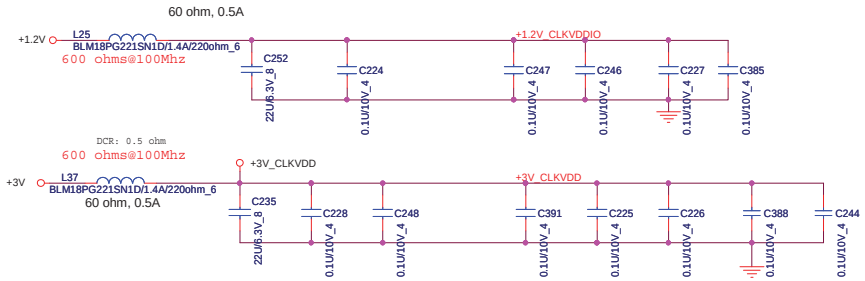
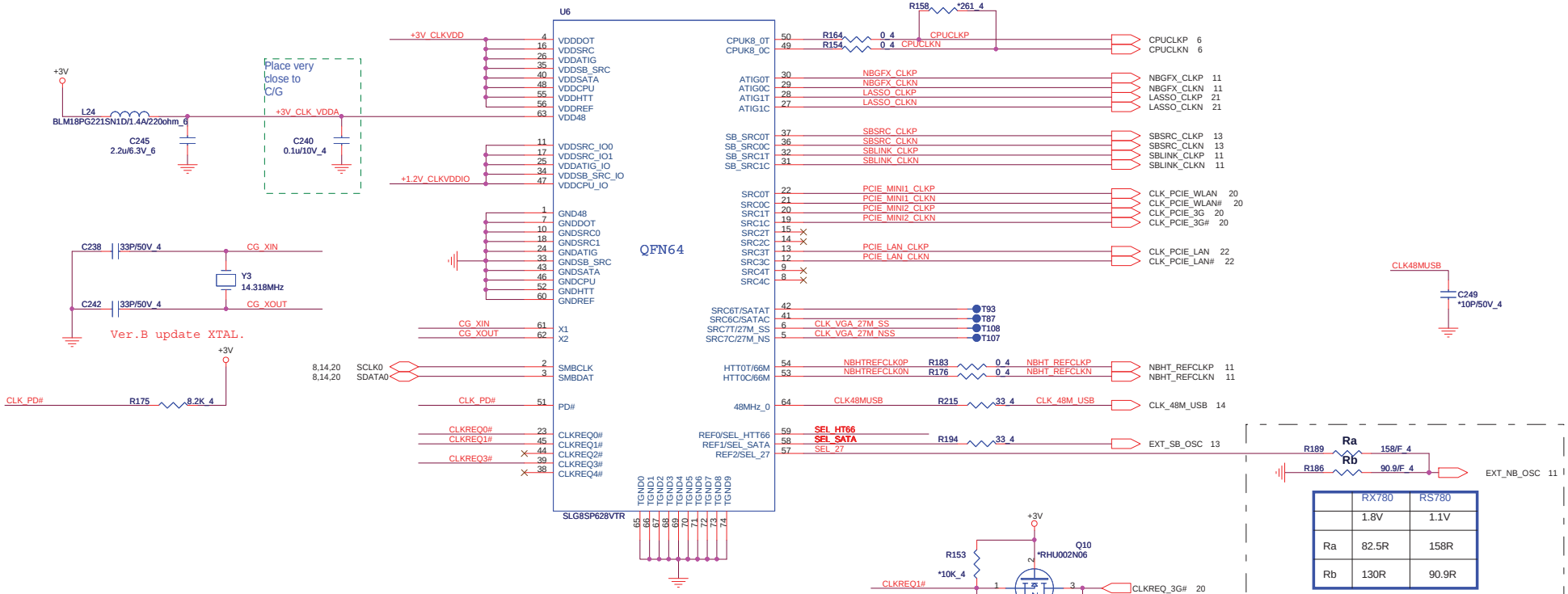
Clock Generator(CLK)



CLOCKS name	UMA	DISCRETE	Clock pin function
NBGFX_CLKP NBGFX_CLKN	RP49 STUFF	RP49 STUFF	to NB for VGA reference clock
EXT_GFX_CLKP EXT_GFX_CLKN	RP48 NC	RP48 STUFF	to M86-M external reference clock
NBGPP_CLKP NBGPP_CLKN	RP43 NC	RP43 NC	to NB for RX780 for PCIEX2 interface reference clock only RS780 is internal share with AC-LINK clock,RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP51 STUFF	RP51 STUFF	to NB for AC-LINK reference clock

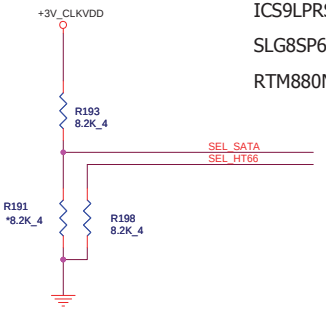
EMI reserved



	RX780	RS780
	1.8V	1.1V
Ra	82.5R	158R
Rb	130R	90.9R

RES CHIP 130 1/16W +-1%(0402)L-F -->CS11302FB15
RES CHIP 158 1/16W +-1%(0402) -->CS11582FB00
RES CHIP 90.9 1/16W +-1%(0402) -->CS09092FB15
RES CHIP 82.5 1/16W +-1%(0402) -->CS08252FB11

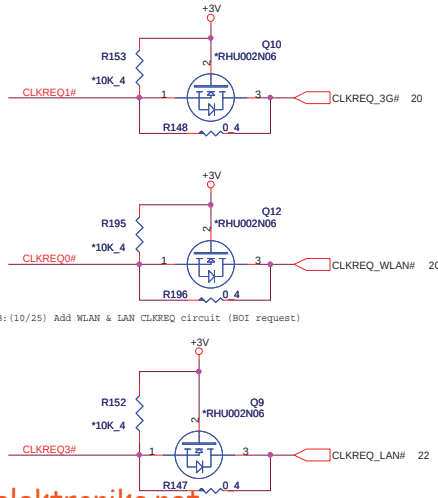
Clock chip has internal serial terminations
for differencial pairs, external resistors are
reserved for debug purpose.



ICS9LPRS480 P/N : ALPRS480000

SLG8SP628 P/N : AL8SP628000

RTM880N-796 P/N : AL000880000



B:(10/25) Add WLAN & LAN CLKREQ circuit (BOI request)

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock

* default

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Size | Document Number: CLOCK GENERATOR | Rev 1A

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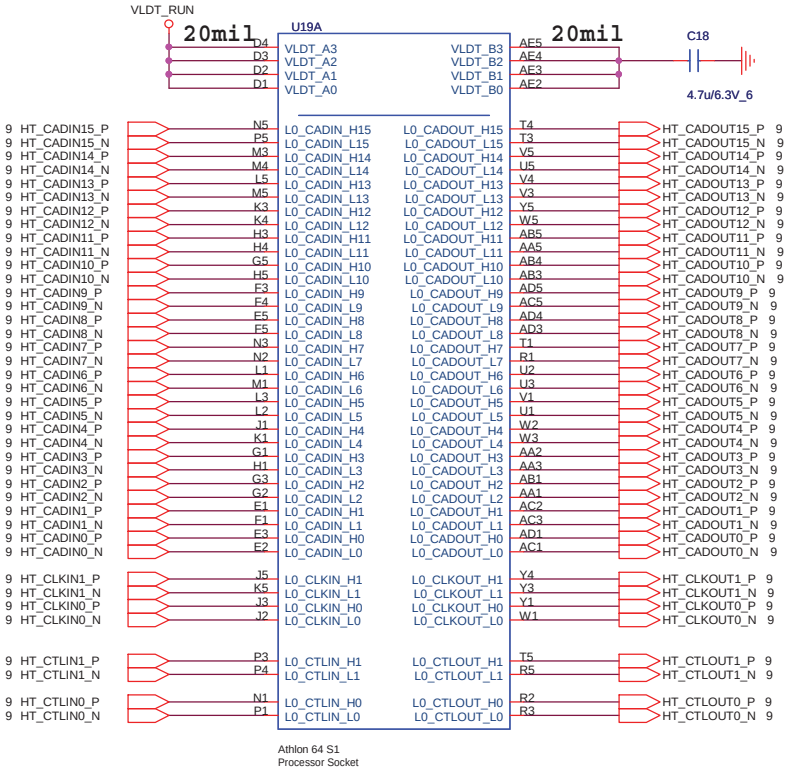
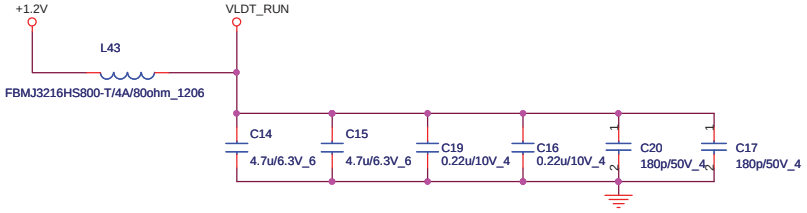
(CPU)





Power name	Description	Voltage
VLDT_A/B	HyperTransport I/O ring power supply	1.2V

Quanta Computer Inc.

PROJECT : ZH6

Size	Document Number	Rev
	TURION 64 HT I/F	1A

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(CPU)

Processor DDR2 Memory Interface

15-20mil

PLACE THEM CLOSE TO CPU WITHIN 1"

200mil

+1.8VSUS

+SMDDR_VTERM

CPU_M_VREF

R82 2K/F_4

R78 2K/F_4

C72 0.1u/10V_4

C76 1000p/50V_4

R37 39.2/F_4

R39 39.2/F_4

T16

VTT_SENSE

M_ZN

M_ZP

U19B

MEMVREF

VTT_SENSE

MEMZN

MEMZP

VTT1 VTT2 VTT3 VTT4 VTT5 VTT6 VTT7 VTT8 VTT9

MA0_CS_L3 MA0_CS_L2 MA0_CS_L1 MA0_CS_L0

MA0_CLK_H2 MA0_CLK_L2 MA0_CLK_H1 MA0_CLK_L1

MB0_CS_L3 MB0_CS_L2 MB0_CS_L1 MB0_CS_L0

MB0_CLK_H2 MB0_CLK_L2 MB0_CLK_H1 MB0_CLK_L1

MB_CKE1 MB_CKE0 MA_CKE1 MA_CKE0

MB0_ODT1 MB0_ODT0 MA0_ODT1 MA0_ODT0

MA_ADD15 MA_ADD14 MA_ADD13 MA_ADD12 MA_ADD11 MA_ADD10 MA_ADD9 MA_ADD8 MA_ADD7 MA_ADD6 MA_ADD5 MA_ADD4 MA_ADD3 MA_ADD2 MA_ADD1 MA_ADD0

MB_ADD15 MB_ADD14 MB_ADD13 MB_ADD12 MB_ADD11 MB_ADD10 MB_ADD9 MB_ADD8 MB_ADD7 MB_ADD6 MB_ADD5 MB_ADD4 MB_ADD3 MB_ADD2 MB_ADD1 MB_ADD0

MA_BANK2 MA_BANK1 MA_BANK0

MB_BANK2 MB_BANK1 MB_BANK0

MA_RAS_L MA_CAS_L MA_WE_L

MB_RAS_L MB_CAS_L MB_WE_L

DDR II: CMD/CTRL/CLK
Athlon 64 S1
Processor Socket

M_CLKOUT0 C58 1.5p/50V_4 M_CLKOUT0#

M_CLKOUT1 C55 1.5p/50V_4 M_CLKOUT1#

M_B_CLKOUT0 C74 1.5p/50V_4 M_B_CLKOUT0#

M_B_CLKOUT1 C67 1.5p/50V_4 M_B_CLKOUT1#

U19C

MB_DATA63 … MB_DATA0

MA_DATA63 … MA_DATA0

MB_DM7 … MB_DM0

MA_DM7 … MA_DM0

MB_DQS_H7 … MB_DQS_L0

MA_DQS_H7 … MA_DQS_L0

DDR: DATA
Athlon 64 S1
Processor Socket

To SODIMM socket A (near)

+SMDDR_VTERM

C167 4.7u/6.3V_6 C70 4.7u/6.3V_6 C107 4.7u/6.3V_6 C51 4.7u/6.3V_6 C43 0.22u/10V_4 C61 0.22u/10V_4 C185 0.22u/10V_4 C186 0.22u/10V_4 C173 1000p/50V_4 C52 1000p/50V_4 C46 1000p/50V_4 C48 1000p/50V_4 C168 180p/50V_4 C54 180p/50V_4 C201 180p/50V_4 C106 180p/50V_4

Power name	Description	Voltage
VTT	VTT Power	0.9V

http://hobi-elektronika.net

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PROJECT : ZH6

Size	Document Number	Rev
	TURION 64 DDRII I/F	1A
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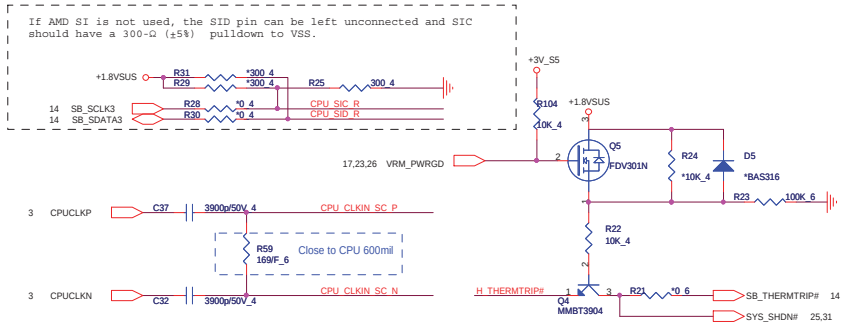
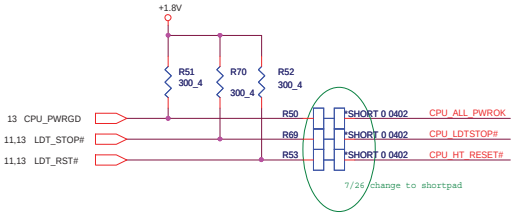
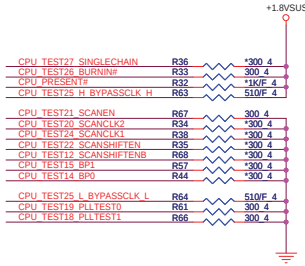
ATHLON Control and Debug

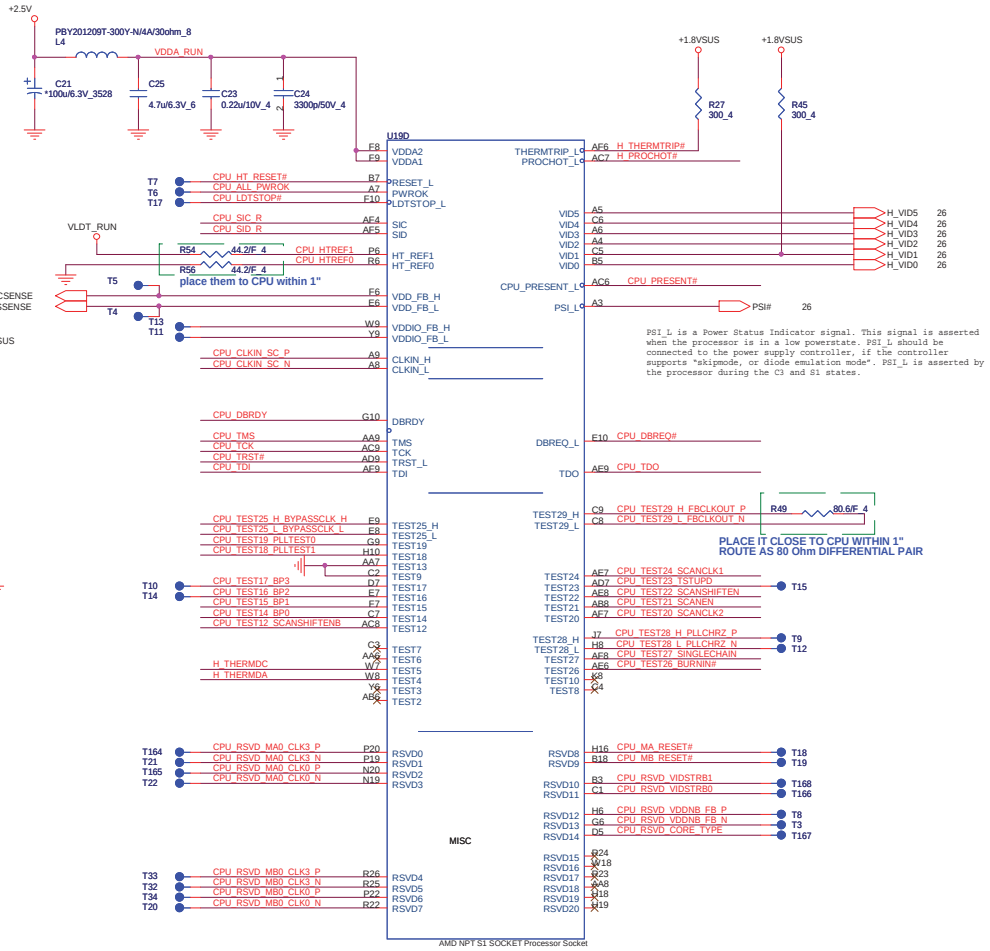
(CPU)

If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pulldown to VSS.

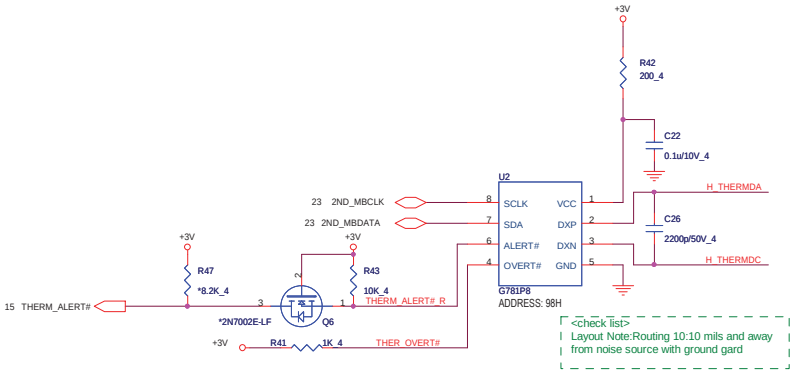




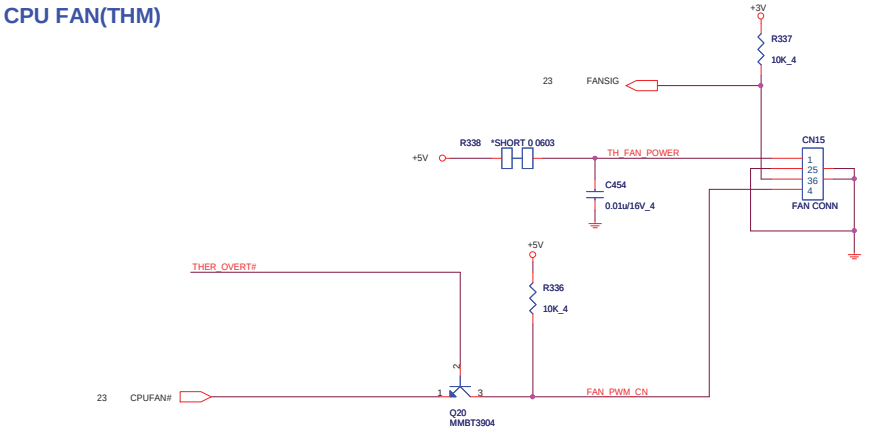


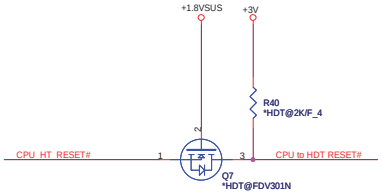


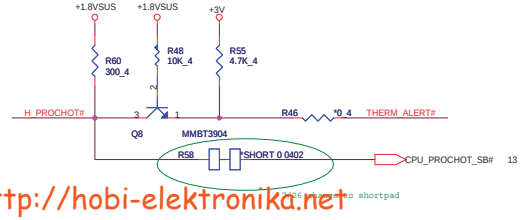
CPU Thermal monitor(THM)

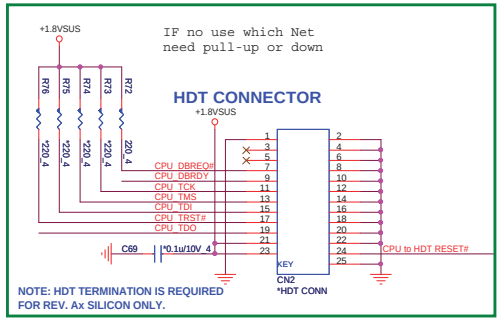


CPU FAN(THM)









Power name	Description	Voltage
VDDA	Filtered PLL supply voltage	2.5V

Quanta Computer Inc.

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Size	Document Number	Rev
	TURION 64 CTRL & DEBUG	1A

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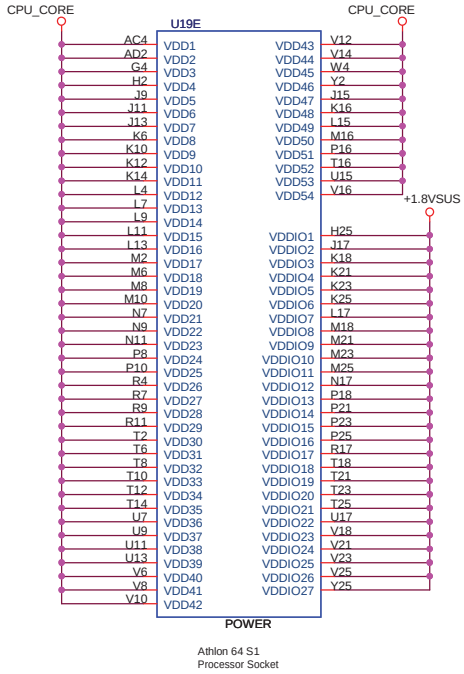
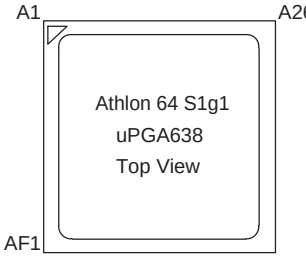
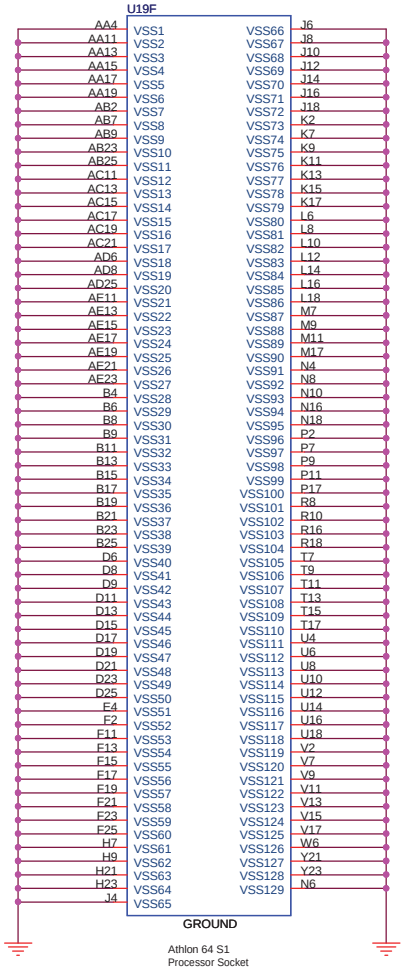
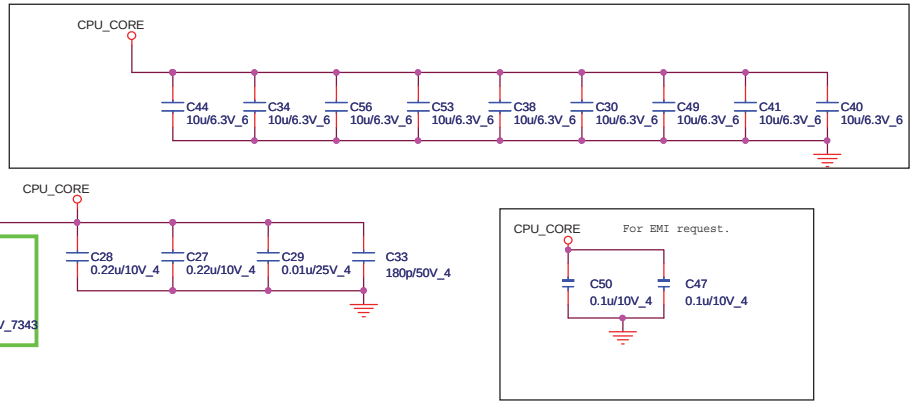
PROCESSOR POWER AND GROUND(CPU)



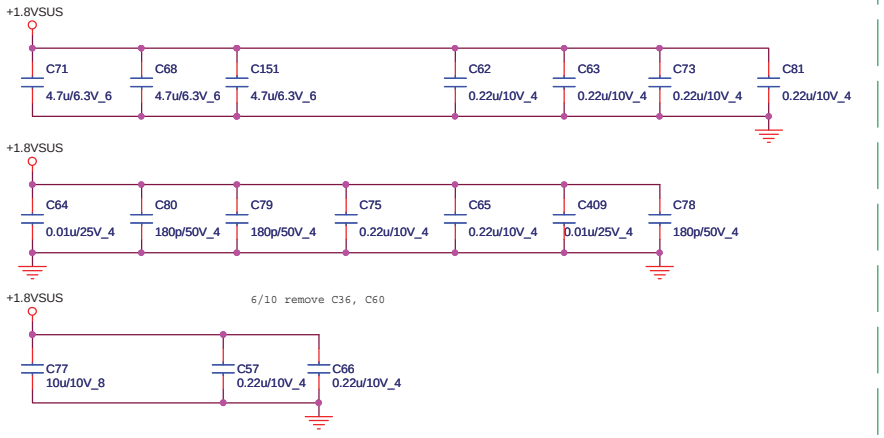




BOTTOMSIDE DECOUPLING



DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE



Power name	Description	Voltage
VDD	Core power supply	1.05V
VDDIO	DDR SDRAM I/O ring power supply	1.8V

Quanta Computer Inc.
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Size	Document Number	Rev
	TURION 64 PWR & GND	1A
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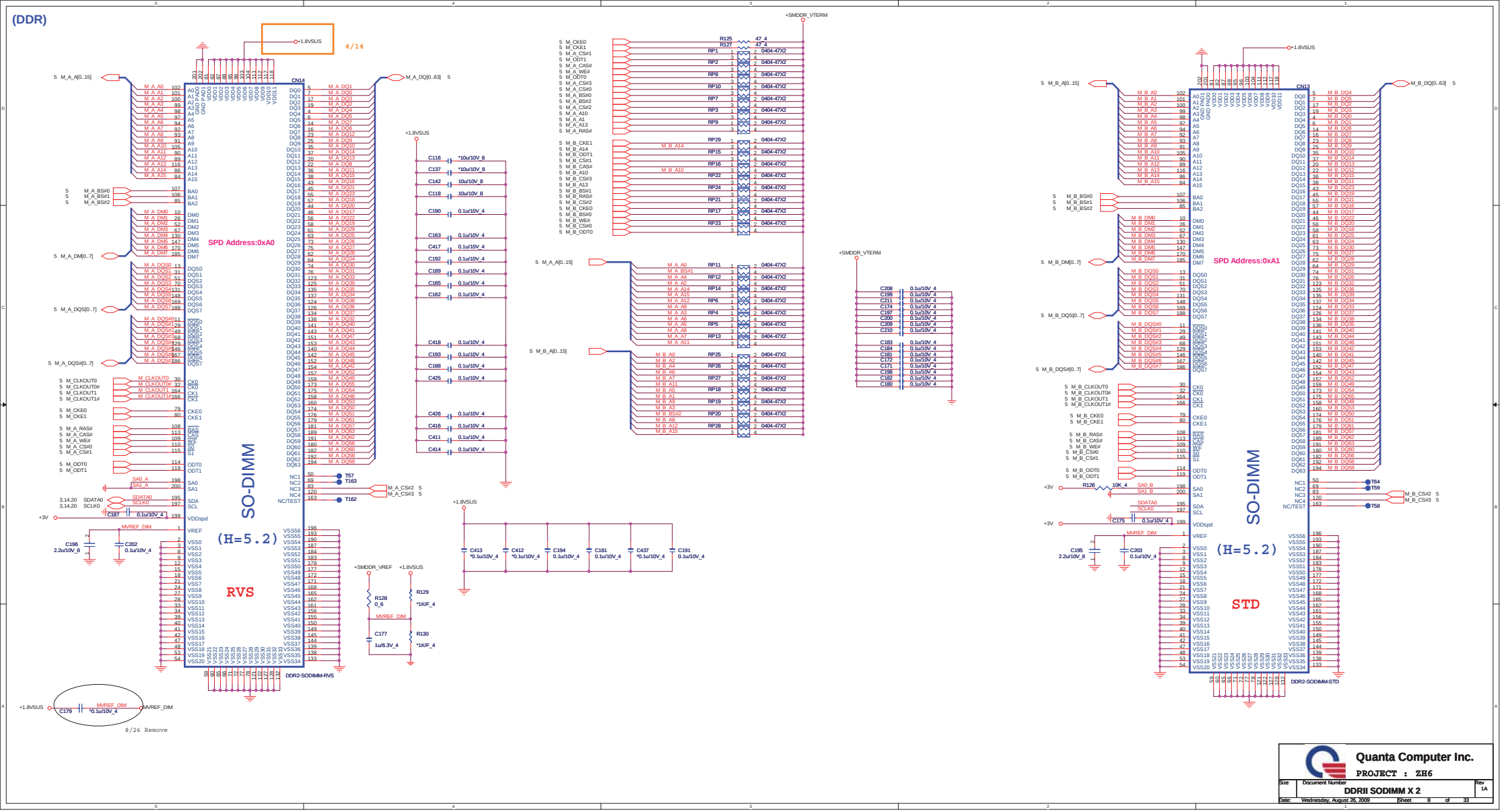
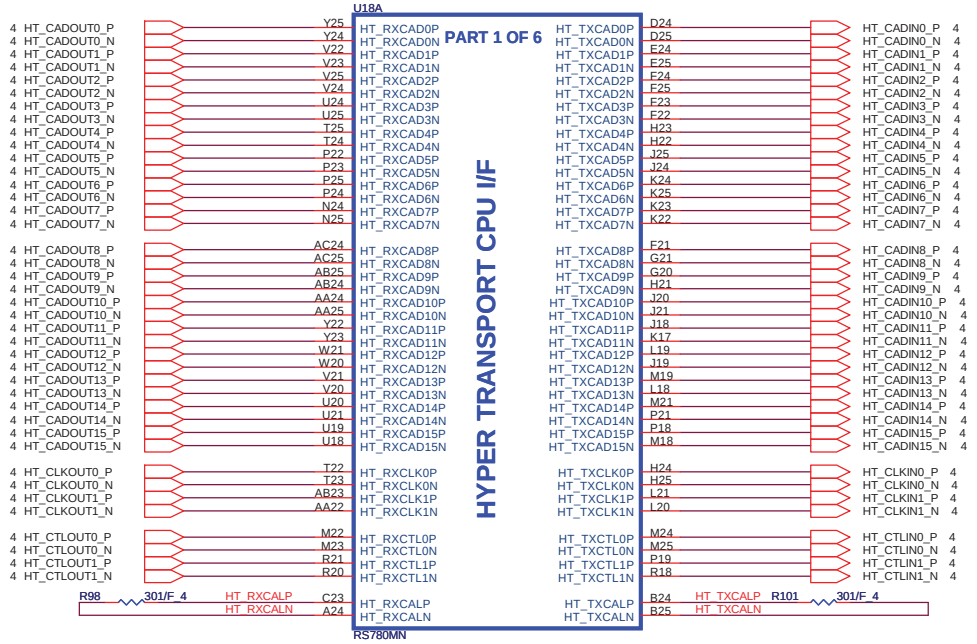


RS780(CLG)

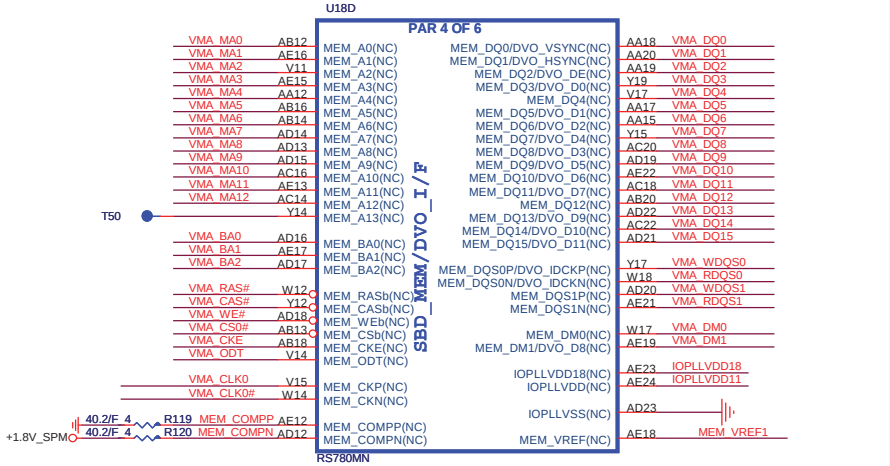


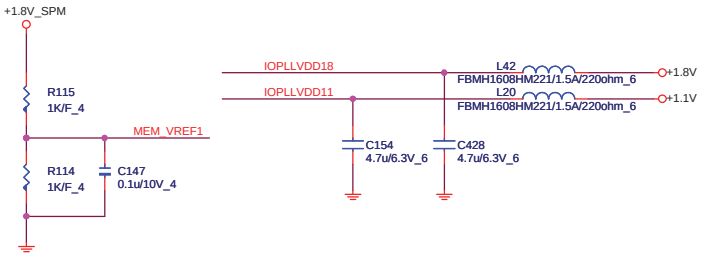
signals	RS780	RX780
HT_TXCALP	R2364 301 ohm 1%	R2364 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R2365 301 ohm 1%	R2365 1.21k ohm 1%
HT_RXCALN		

RS780(CLG)

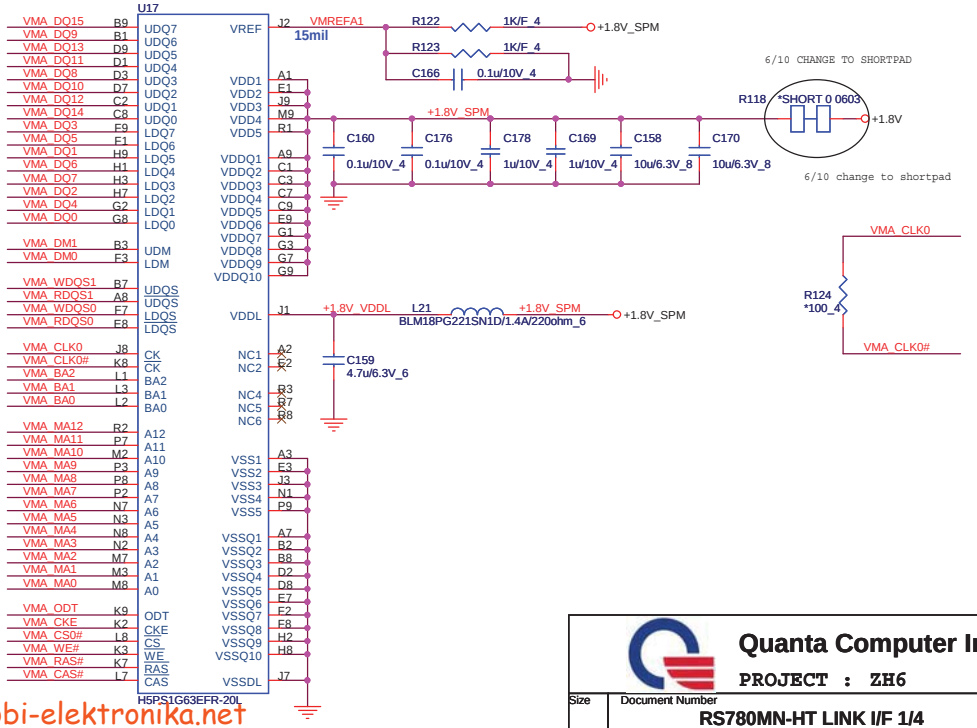
SIDE-PORT Reserved

This block is for UMA RS780 only , RX780 NC





SPM(CLG)



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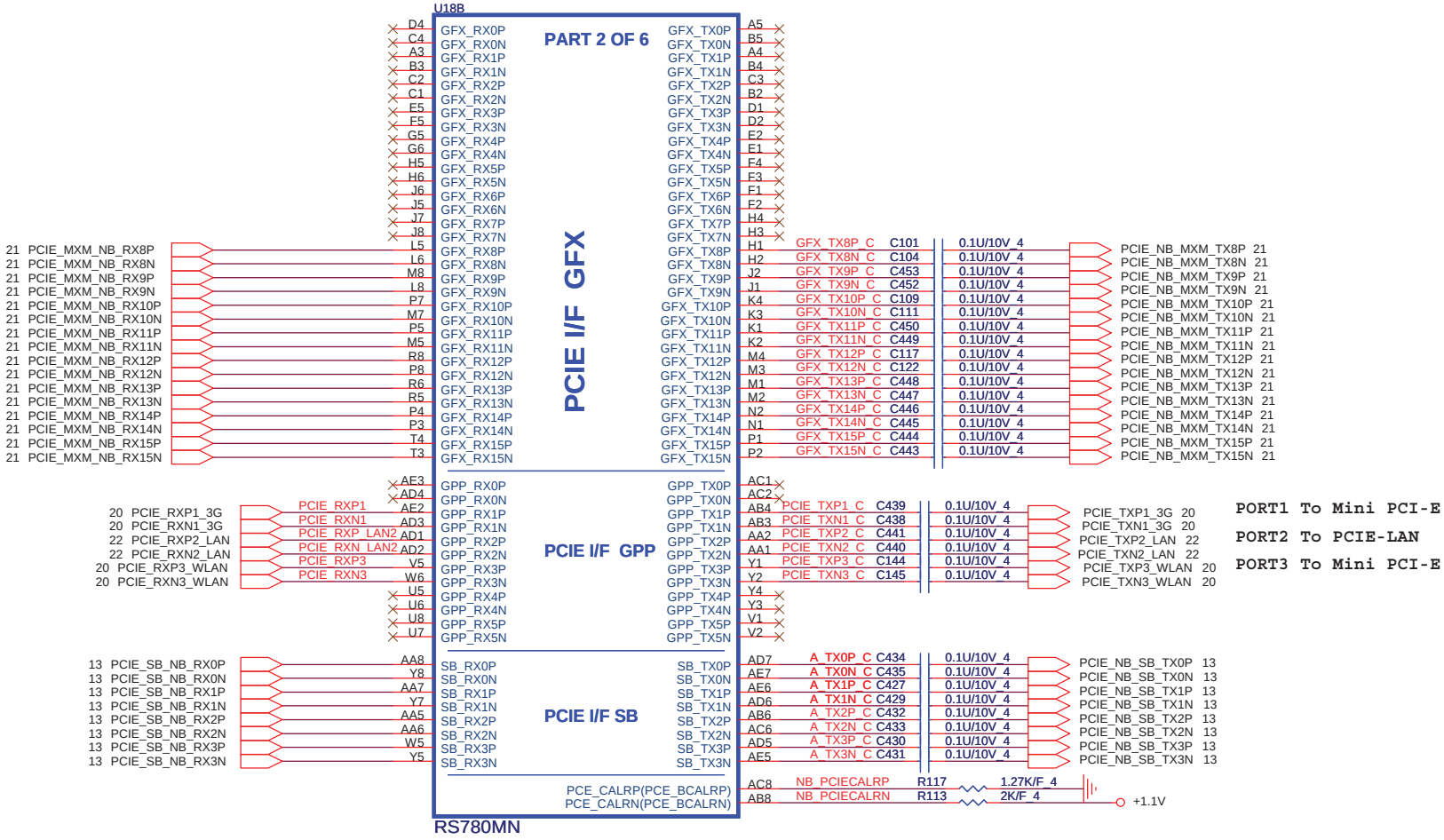
PROJECT : ZH6

Size	Document Number	Rev
	RS780MN-HT LINK I/F 1/4	1A
Date: Monday, August 24, 2009	Sheet 9 of 33	



RX780/RS740/RS780 difference table (PCIE LINK)

	RX780/RS780
NB_PCIECALRP	1.27K (GND)
GPP4	GPP4
GPP5	GPP5

Quanta Computer Inc.

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Size	Document Number	Rev
	RS780MN-HT LINK I/F 1/4	1A
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RS780(CLG)

RX780: Powered from the 1.8-V rail
and driven by SB600 LDT_RST#, or
SB700 LDT_RST# or A_RST#.
RS780: Powered from the 3.3-V rail
and driven by SB600 LDT_RST#, or
SB700 LDT_RST# or A_RST#.

7/26 change to shortpad

13 NB_PLTRST#
6,13 LDT_RST#
R85 *SHORT 0 0402
R86 *0_4
NB_RST# IN
C92 *1000P/16V_4

RS780

North Bridge RESET

ESD Reserved

NB_PWRGD_IN
C95 *1000P/16V_4

+3V R90 *4.7K_4 HDTV_DET

U18C

PART 3 OF 6

CRT/TVOUT
PLL PWR
LVTM
PM
CLOCKs
MIS.

+3V_AVDD_NB F12 AVDD1(NC)
F12 AVDD2(NC)
+1.8V_AVDDDI_NB F14 AVDDDI(NC)
G15 AVSSDI(NC)
+1.8V_AVDDQ_NB H15 AVDDQ(NC)
H14 AVSSQ(NC)

F17 C_Pr(DFT_GPIO5)
F17 Y(DFT_GPIO2)
F15 COMP_Pb(DFT_GPIO4)

18 CRT_R R110 140/F_4 G18 RED(DFT_GPIO0)
18 CRT_G R109 150/F_4 G17 REDb(NC)
18 CRT_B R107 150/F_4 F18 GREEN(DFT_GPIO1)
F18 GREENb(NC)
F19 BLUE(DFT_GPIO3)
F19 BLUEb(NC)

18 HSYNC A11 DAC_HSYNC(PWM_GPIO4)
18 VSYNC B11 DAC_VSYNC(PWM_GPIO6)
18 CRT_DDCDAT E8 DAC_SDA(PCE_TCALRN)
18 CRT_DDCCLK F8 DAC_SCL(PCE_RCALRN)

R108 715/F_6 DAC_RSET_NB G14 DAC_RSET(PWM_GPIO1)

+1.1V_PLLVDD A12 PLLVDD(NC)
+1.8V_PLLVDD18 D14 PLLVDD18(NC)
B12 PLLVSS(NC)

+1.8V_VDDA18HTPLL H17 VDDA18HTPLL

+1.8V_VDDA18PCIEPLL D7 VDDA18PCIEPLL1
E7 VDDA18PCIEPLL2

NB_RST# IN D8 SYSRESETb
17 NB_PWRGD_IN NB_PWRGD_IN A10 POWERGOOD
NB_LDT_STOP# C10 LDTSTOPb
NB_ALLOW_LDTSTOP C12 ALLOW_LDTSTOP

3 NBHT_REFCLKP NBHT_REFCLKP C25 HT_REFCLKP
3 NBHT_REFCLKN NBHT_REFCLKN C24 HT_REFCLKN

3 EXT_NB_OSC 7/26 change to shortpad R79 *SHORT 0 0402 NB_REFCLK_P E11 REFCLK_P/OSCIN(OSCIN)
R80 *SHORT 0 0402 NB_REFCLK_N F11 REFCLK_N(PWM_GPIO3)
+1.1V R87 4.7K_4 R84 4.7K_4

NBGFX_CLKP T2 GFX_REFCLKP
3 NBGFX_CLKP NBGFX_CLKN T1 GFX_REFCLKN
3 NBGFX_CLKN

U1 GPP_REFCLKP
U2 GPP_REFCLKN

3 SBLINK_CLKP SBLINK_CLKP V4 GPPSB_REFCLKP(SB_REFCLKP)
3 SBLINK_CLKN SBLINK_CLKN V3 GPPSB_REFCLKN(SB_REFCLKN)

18 INT_LVDS_EDIDDATA A9 I2C_DATA
18 INT_LVDS_EDIDCLK B9 I2C_CLK
HDTV_DET B8 DDC_DATA/AUX0N(NC)
T29 RS740_DFT_GPIO0 A8 DDC_CLK/AUX0P(NC)
B7 AUX1P(NC)
A7 AUX1N(NC)

27 +NB_CORE_ON 7/26 change to shortpad R91 *SHORT 0 0402 STRP_DATA B10 STRP_DATA
G11 RSVD
R100 150/F_4 RS780_AUX_CAL C8 AUX_CAL(NC)

add by checklist

RS780MN

TXOUT_L0P(NC) A22
TXOUT_L0N(NC) B22
TXOUT_L1P(NC) A21
TXOUT_L1N(NC) B21
TXOUT_L2P(NC) B20
TXOUT_L2N(DBG_GPIO0) A20
TXOUT_L3P(NC) A19
TXOUT_L3N(DBG_GPIO2) B19

TXOUT_U0P(NC) B18
TXOUT_U0N(NC) A18
TXOUT_U1P(PCIE_RESET_GPIO3) A17
TXOUT_U1N(PCIE_RESET_GPIO2) B17
TXOUT_U2P(NC) D20
TXOUT_U2N(NC) D21
TXOUT_U3P(PCIE_RESET_GPIO5) D18
TXOUT_U3N(NC) D19

TXCLK_LP(DBG_GPIO1) B16 LA_CLK
TXCLK_LN(DBG_GPIO3) A16 LA_CLK#
TXCLK_UP(PCIE_RESET_GPIO4) D16
TXCLK_UN(PCIE_RESET_GPIO1) D17

VDDLTP18(NC) A13 +1.8V_VDDLTP18_NB
VSSLTP18(NC) B13

VDDLT18_1(NC) A15 +1.8V_VDDLT_18_NB
VDDLT18_2(NC) B15
VDDLT33_1(NC) A14
VDDLT33_2(NC) B14

VSSLT1(VSS) C14
VSSLT2(VSS) D15
VSSLT3(VSS) C16
VSSLT4(VSS) C18
VSSLT5(VSS) C20
VSSLT6(VSS) E20
VSSLT7(VSS) C22

LVDS_DIGON(PCE_TCALRP) E9
LVDS_BLON(PCE_RCALRP) E7
LVDS_ENA_BL(PWM_GPIO2) G12

TMDS_HPD(NC) D9
HPD(NC) D10
TVCLKIN(PWM_GPIO5) D12 SUS_STAT# NB R85 *SHORT 0 0402 SUS_STAT# 14
7/26 change to shortpad
THERMALDIODE_P AE8
THERMALDIODE_N AD8
TESTMODE D13 TEST_EN R106 1.82K/F_4

INT_TXLOUT0+ 18
INT_TXLOUT0- 18
INT_TXLOUT1+ 18
INT_TXLOUT1- 18
INT_TXLOUT2+ 18
INT_TXLOUT2- 18
INT_TXLCLKOUT+ 18
INT_TXLCLKOUT- 18
INT_LVDS_DIGON 18
INT_LVDS_PWM 18
INT_LVDS_BLON 18

RX780 -->NC / RS780 --- ADD

+3V L6 BLM18PG221SN1D/1.4A/220ohm_6 +3V_AVDD_NB C82 2.2U/6.3V_6
AVDD-DAC Analog
not applicable to RX780

+1.1V L9 BLM18PG221SN1D/1.4A/220ohm_6 +1.1V_PLLVDD C91 2.2U/6.3V_6
PLLVDD - Graphics PLL
not applicable to
RX780

+1.8V L7 BLM18PG221SN1D/1.4A/220ohm_6 +1.8V_PLLVDD18 C89 10U/6.3V_8 C87 2.2U/6.3V_6
8/18 for Monitor test waterflow issue
PLLVDD18 - Graphics PLL
not applicable to RX780

+1.8V R83 *SHORT 0 0603 +1.8V_AVDDDI_NB C84 2.2U/6.3V_6
AVDDI-DAC Digital
not applicable to RX780

BLM18PG221SN1D/1.4A/220ohm_6 L5 +1.8V_AVDDQ_NB C83 2.2U/6.3V_6
AVDDQ-DAC Bandgap Reference
not applicable to RX780

+1.8V L13 BLM18PG221SN1D/1.4A/220ohm_6 +1.8V_VDDLTP18_NB C98 2.2U/6.3V_6
VDDLTP18 - LVDS or DVI/HDMI PLL
not applicable to RX780

BLM21PG221SN1D/1.4A/220ohm_6 L11 +1.8V_VDDLT_18_NB C93 4.7U/6.3V_6 C96 0.1U/10V_4
VDDLT18 - LVDS or
DVI/HDMI digital
not applicable to
RX780

Enables Debug Bus acess
through memory T/O pads and GPIO.
0 : Enable RS780 , Default
1 : Disable RS780
(RS780 use VSYNC#)

RS780

VSYNC R97 3K_4 +3V

Indicates if memory Side port
is available or not
0: available RS780 , Default
1: Not available RS780
(RS780 use HSYNC#)

RS780

HSYNC R99 *3K_4 +3V
R102 3K_4

For extrnal EEPROM Debug only

RS780/RX780

STRP_DATA R95 *10K/F_4 +3V
R94 *10K/F_4

+1.8V
VDDA18PCIEPLL -PCIE PLL
L10 BLM18PG221SN1D/1.4A/220ohm_6 20mils width +1.8V_VDDA18PCIEPLL C90 2.2U/6.3V_6

VDDA18HTPLL -HT LINK PLL
L8 BLM18PG221SN1D/1.4A/220ohm_6 20mils width +1.8V_VDDA18HTPLL C88 2.2U/6.3V_6

6,13 LDT_STOP# NB_LDT_STOP#

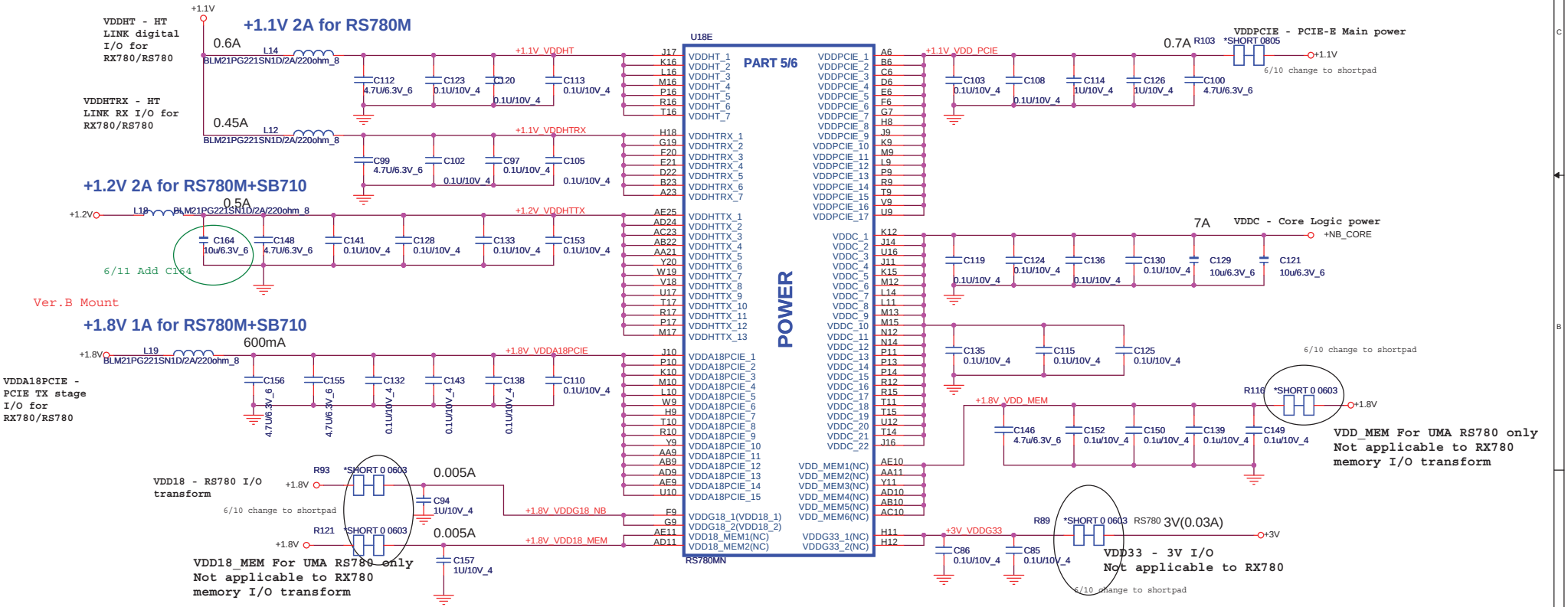
+1.8V R96 1K_4
13 ALLOW_LDTSTOP NB_ALLOW_LDTSTOP

Quanta Computer Inc.
PROJECT : ZH6

Size	Document Number	Rev
	RS780MN-SYSTEM I/F 3/4	1A
Date: Monday, August 24, 2009	Sheet 11 of 33	

RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVDD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVDD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVDD18	NC	+1.8V	VDDLT33	NC	NC



Quanta Computer Inc.

PROJECT : ZH6

Size	Document Number	Rev
	RS780MN-POWER 4/4	1A

Date: Monday, August 24, 2009 Sheet 12 of 33

RS710(CLG)

PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO U600

To RS780

SB700
Part 1 of 5

PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC

PCIE_PVDD-- PCIE PLL POWER

40mA

100MHZ

AMD Errata suggestion
to use external 25MHZ

20MIL

SB710

ESD Reserved

*SHORT 0 0402

Maybe can remove

RTC(RTC)

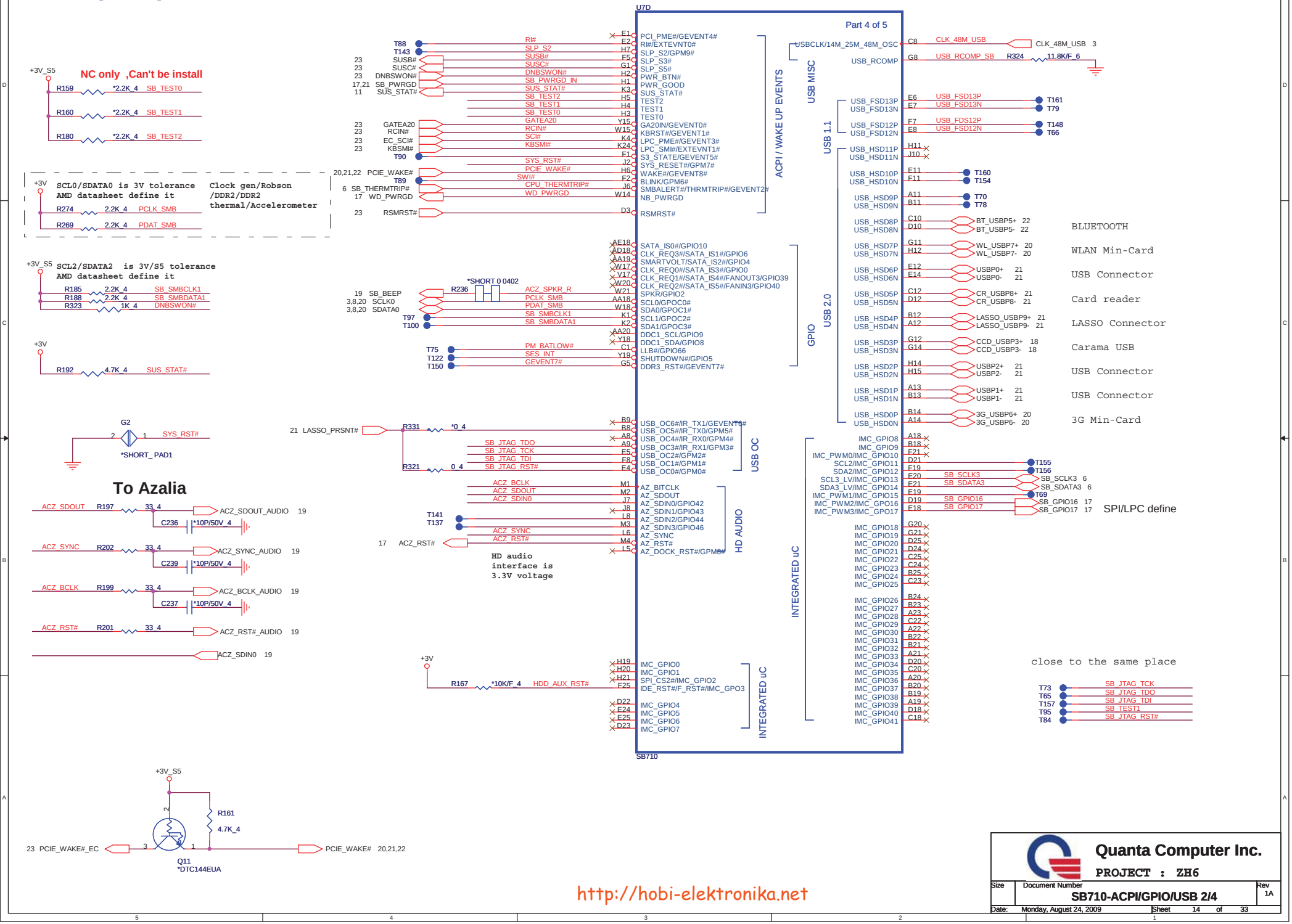
CN10
RTC_CONN

Q18
MMBT3904

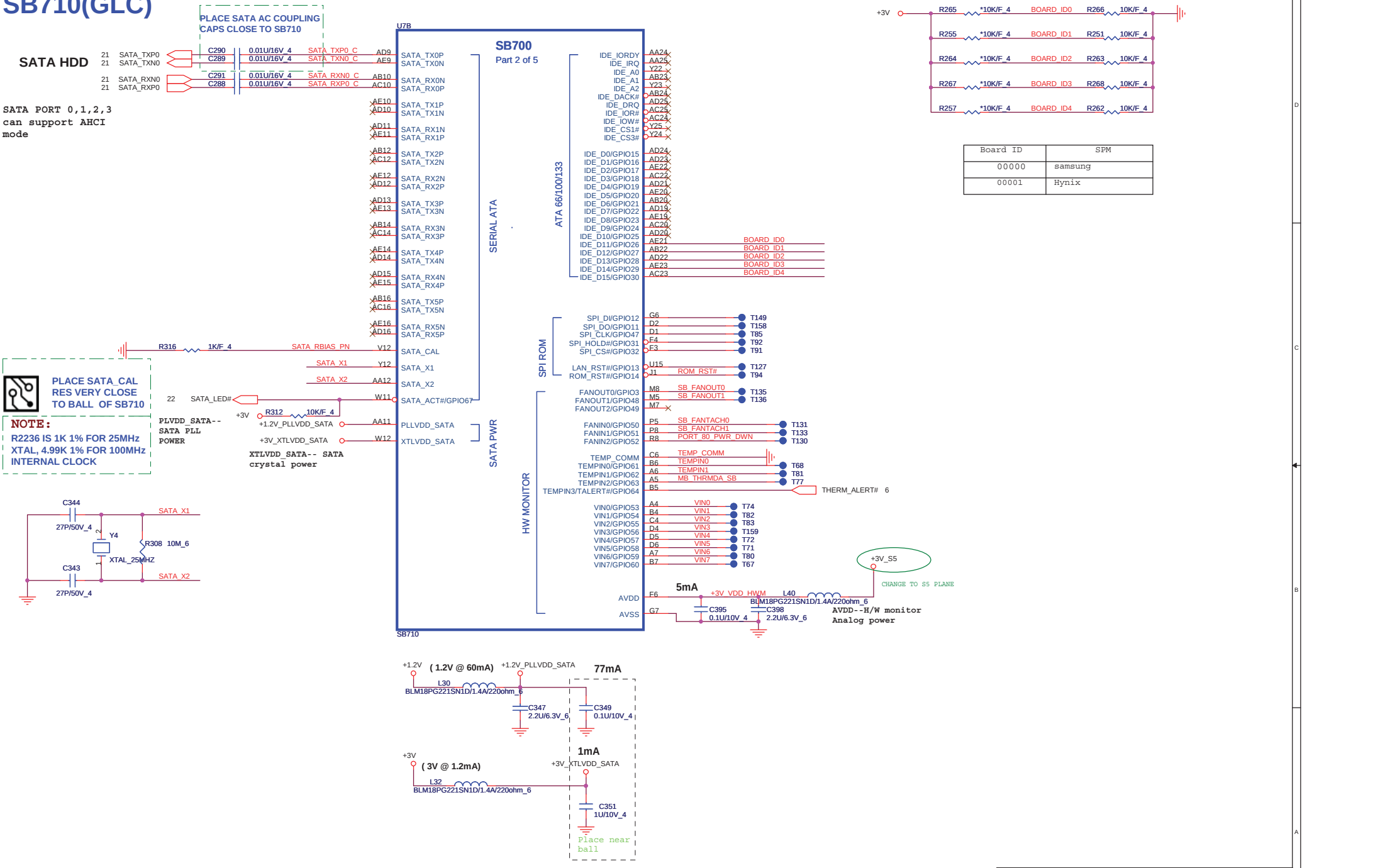
*SHORT_PAD

Quanta Computer Inc.		
PROJECT : ZH6		
Size	Document Number	Rev
	SB710-PCIE/PCI/CPU/LPC 1/4	1A
Date: Monday, August 24, 2009	Sheet 13 of 33	

SB710(GLC)


U7D
Part 4 of 5
SB710
ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
INTEGRATED uC
NC only ,Can't be install
SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
Clock gen/Robson
/DDR2/DDR2
thermal/Accelerometer
SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it
*SHORT_PAD1
To Azalia
HD audio
interface is
3.3V voltage
BLUETOOTH
WLAN Min-Card
USB Connector
Card reader
LASSO Connector
Carama USB
USB Connector
USB Connector
3G Min-Card
SPI/LPC define
close to the same place
Q11
*DTC144EUA
http://hobi-elektronika.net
Quanta Computer Inc.
PROJECT : ZH6
SB710-ACPI/GPIO/USB 2/4
Monday, August 24, 2009
Sheet 14 of 33

SB710(GLC)



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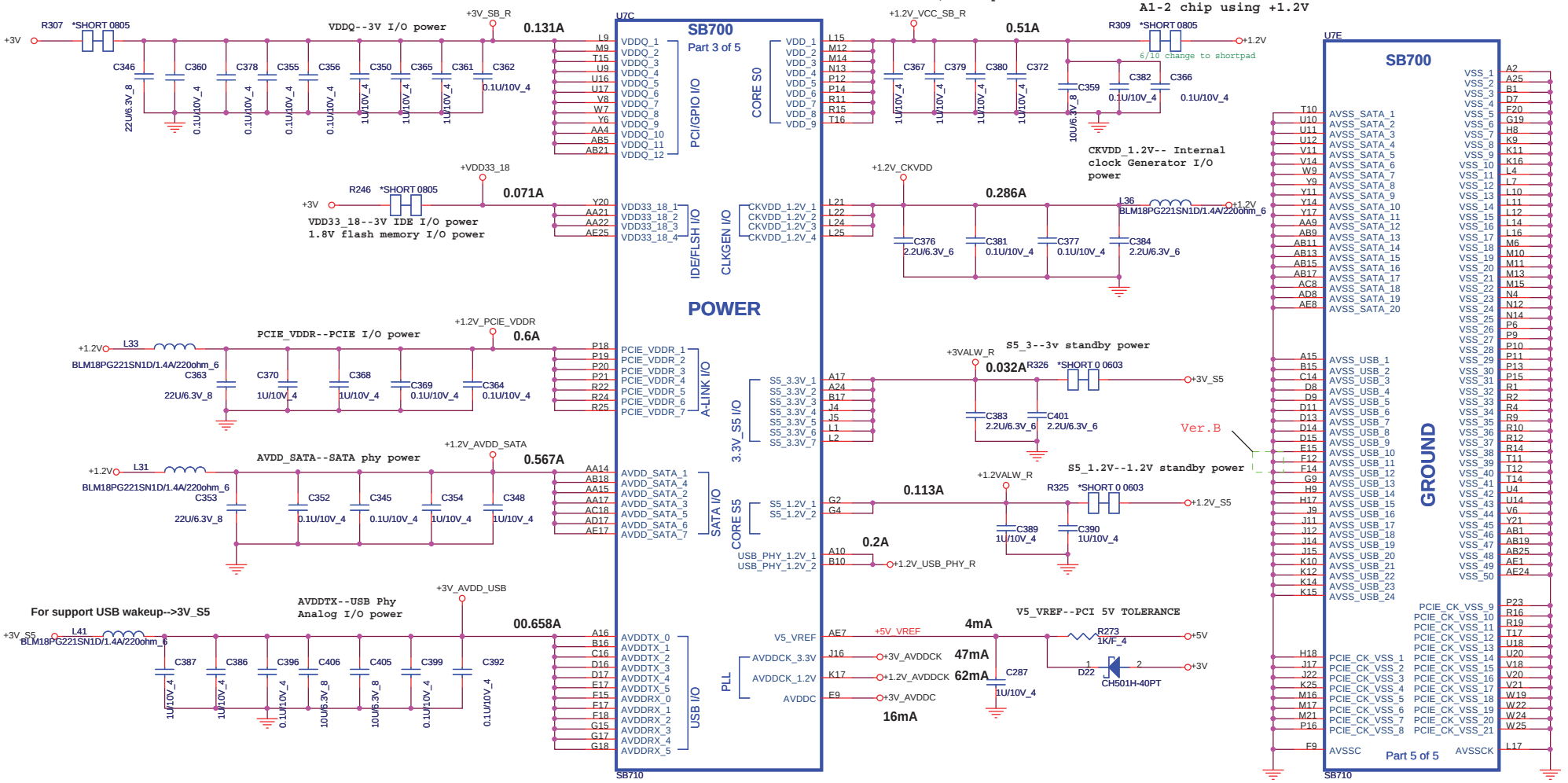
Quanta Computer Inc.			
PROJECT : ZH6			
Size	Document Number		Rev
	SB710-SATA/IDE/HWM/SPI 3/4		1A
Date: Monday, August 24, 2009	Sheet 15 of 33		

EC C-07 2/20 Del R465 and Add R237 for SB source.

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



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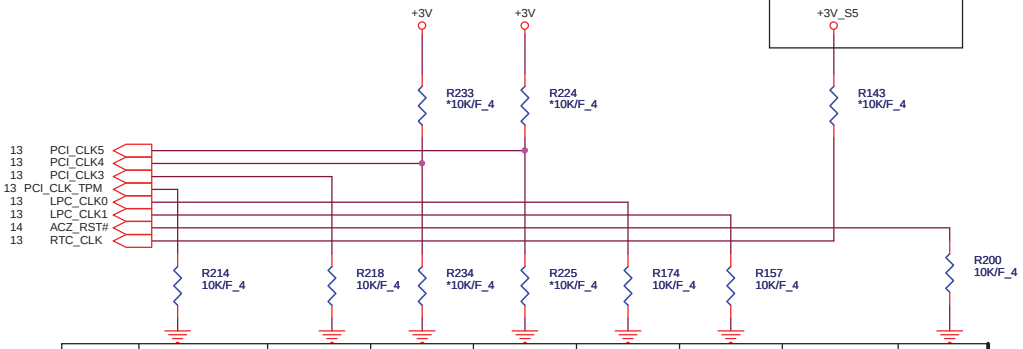
Quanta Computer Inc.		
PROJECT : ZH6		
Size	Document Number: SB710-PWR/DECOUPLING 4/4	Rev: 1A
Date: Monday, August 24, 2009	Sheet 16 of 33	

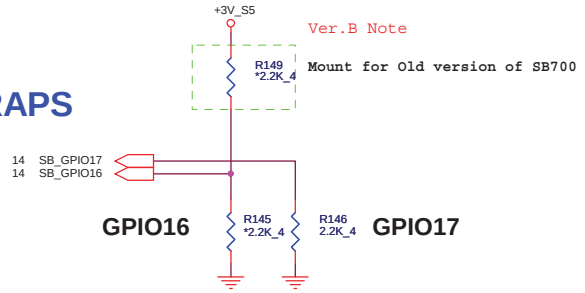
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

It must ready refore RSMRST#

REQUIRED STRAPS



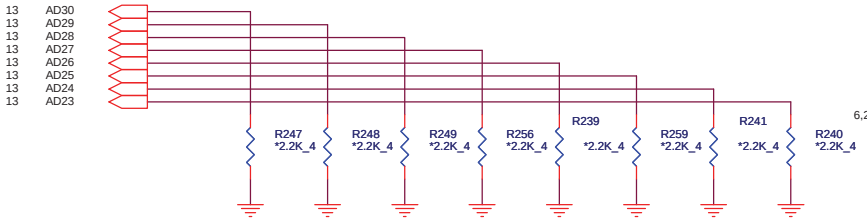
	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE (IMC)	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE (IMC) DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT

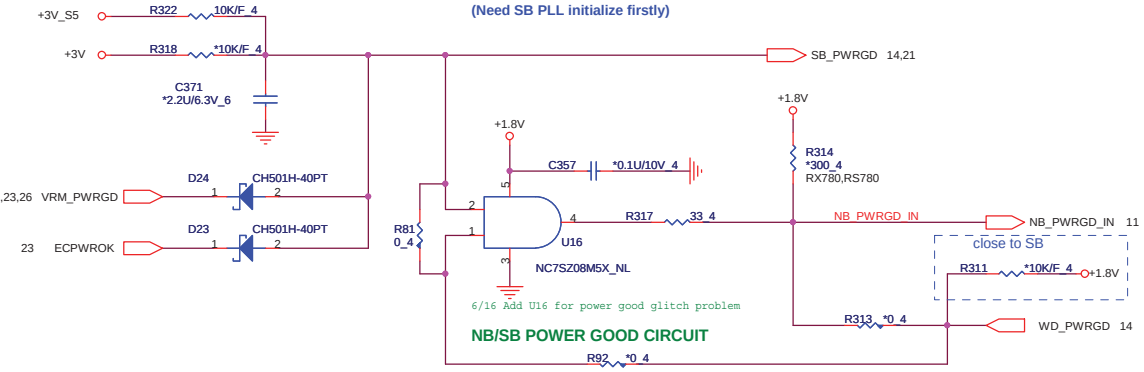


TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

DEBUG STRAPS

SB710 HAS 15K INTERNAL PU FOR PCI_AD[28:23]





	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD29	PCI_AD30
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED		
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS		RESERVED	RESERVED

AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

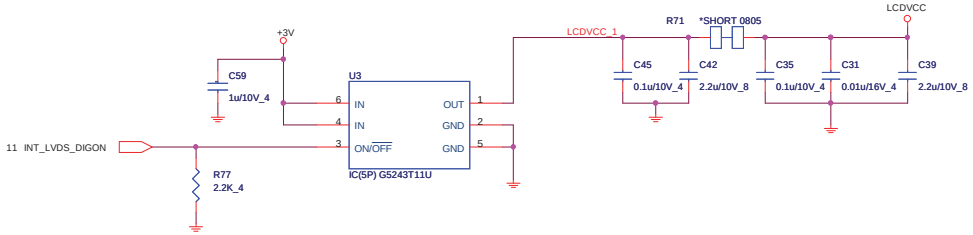
Quanta Computer Inc.

PROJECT : ZH6

Size	Document Number	Rev
	SB710-STRAPS/PWRGD	1A

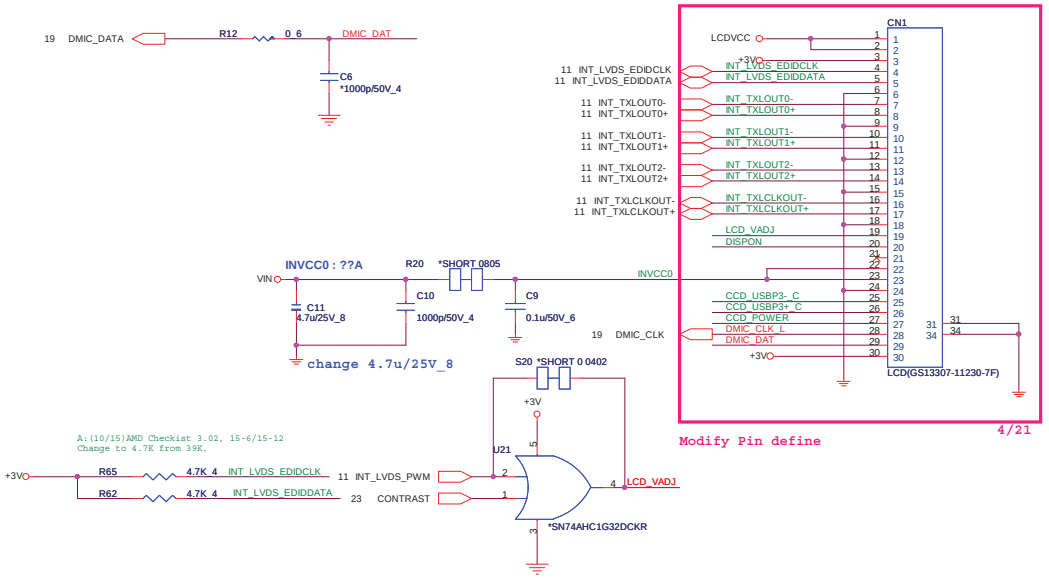
Date: Monday, August 24, 2009 Sheet 17 of 33

Panel Power(LDS)

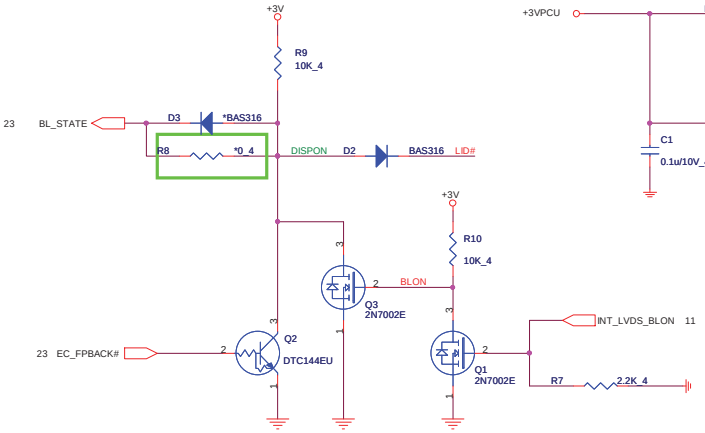


LVDS Connector(LDS)

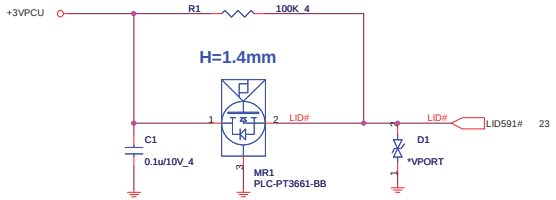
LED_VDD(From LCD_VCC) :
4A(Rush current) 0.31A(Typ)



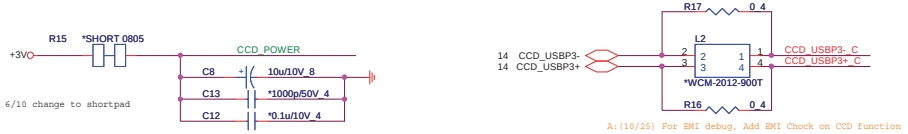
Backlight(LDS)



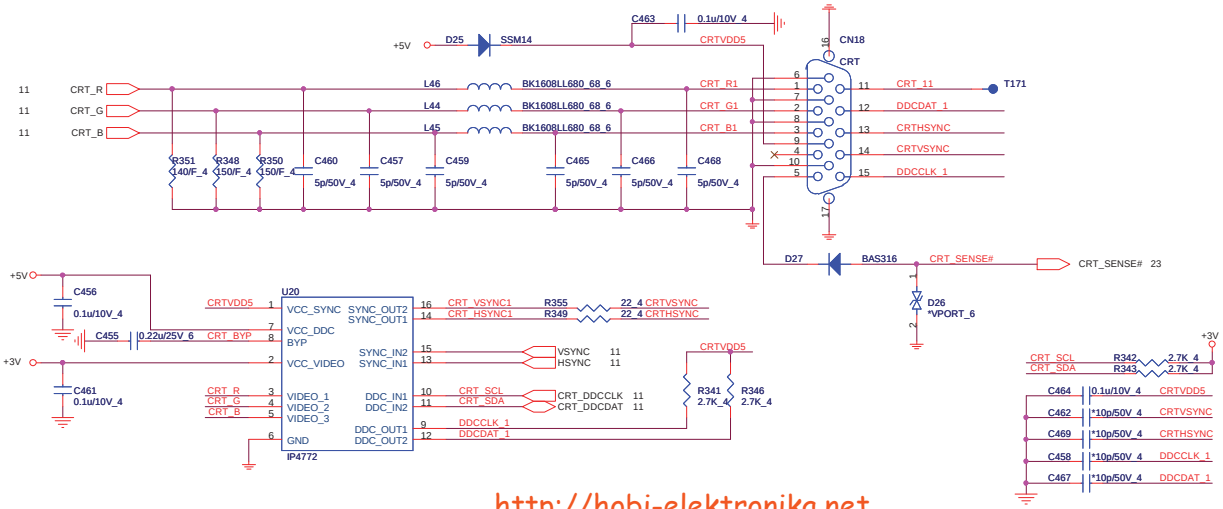
HALL SENSOR (HSR)



CAMERA Module (CMOS sensor)(CCD)



CRT (CRT)



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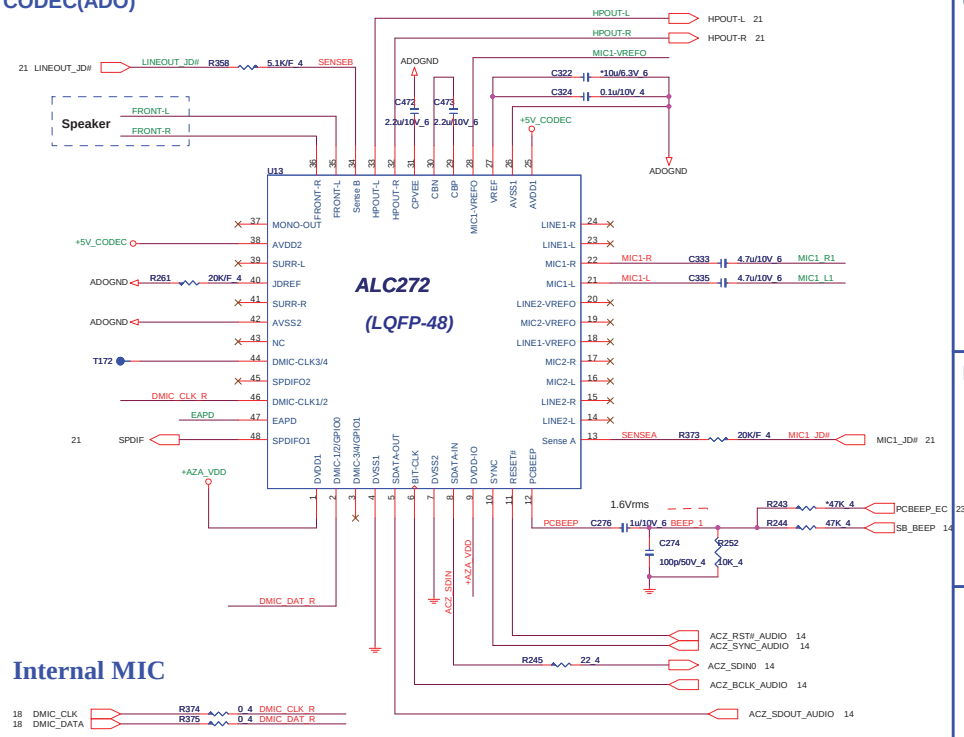
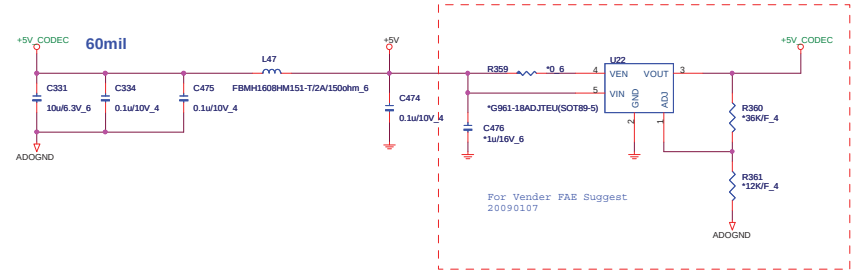
Quanta Computer Inc.
PROJECT : ZH6

Size	Document Number	Rev
	LED PANEL/LID/CCD/CRT	1A
Date: Monday, August 24, 2009	Sheet 18 of 33	

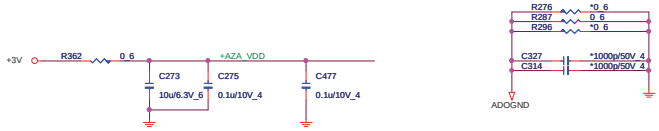
CODEC(ADO)

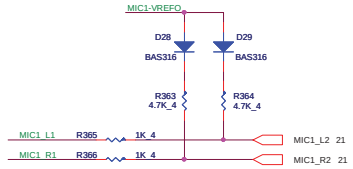


Codec Power(ADO)

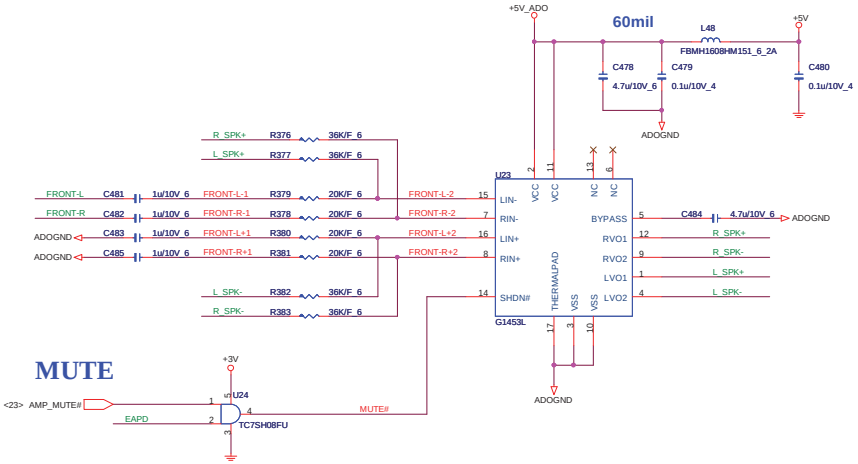


HDA Power(ADO)





Speaker Amplifier(AMP)



Speaker(AMP)

Quanta Computer Inc.
PROJECT : ZH6

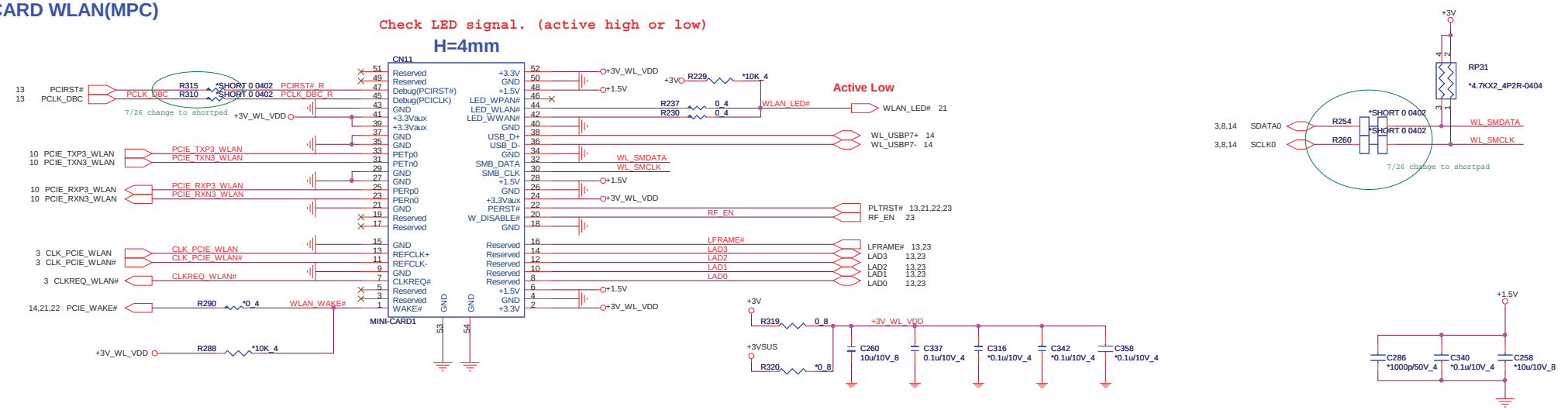
Size	Document Number	Rev
	AL272/AMP/MIC/LINE-OUT	1A

Date: Monday, August 24, 2009 Sheet 19 of 33

MINI-CARD WLAN(MPC)

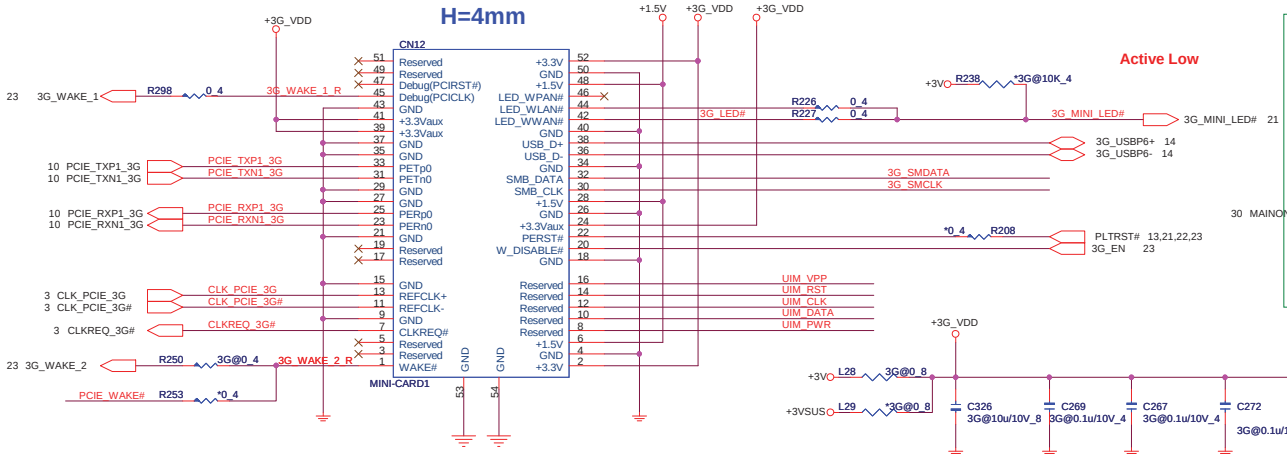
Check LED signal. (active high or low)

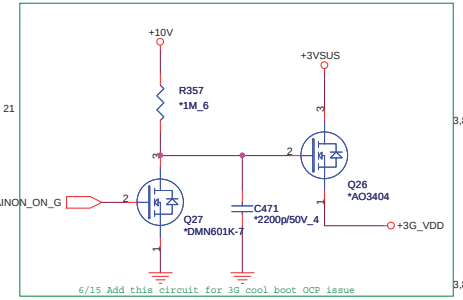
H=4mm

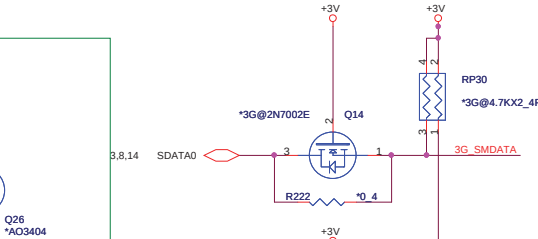


MINI-CARD 3G(MNC)

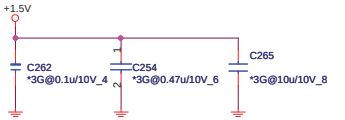
H=4mm





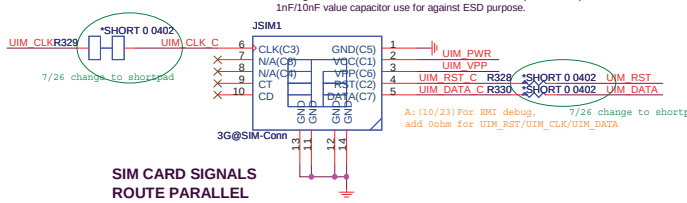


A:(10/17)FAE confirm:
3G module need +3VSUS and no need +1.5V and no need SMBUS

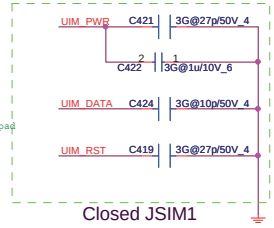


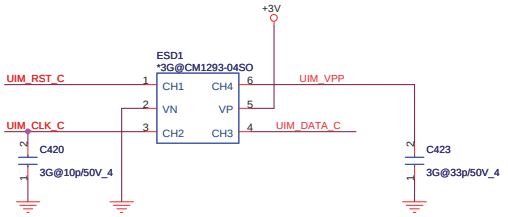
SIM CARD(RFM)

The value of the capacitor is suggest by Siemens HQ expert.
For against 900MHz RF interference. The value of capacitor is 27pF.
For against 1800MHz RF interference. The value of capacitor is 10pF.
1nF/10nF value capacitor use for against ESD purpose.



SIM CARD SIGNALS
ROUTE PARALLEL

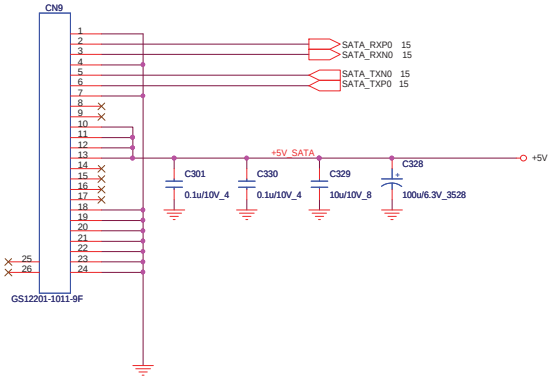




Quanta Computer Inc.		
PROJECT : ZH6		
Size	Document Number	Rev
	Mini-Card/WL/3G/SIM	1A
Date: Monday, August 24, 2009	Sheet 20 of 33	

2.5" SATA HDD OR SSD(HDD)

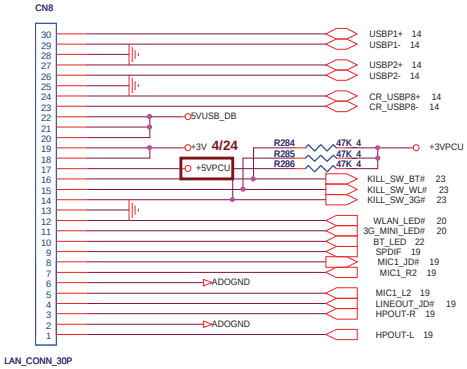
Check SATA HDD in AVL for +3V

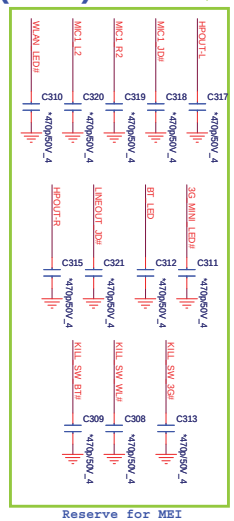


Audio, Cardreader ,Kill SW DB (AMP)

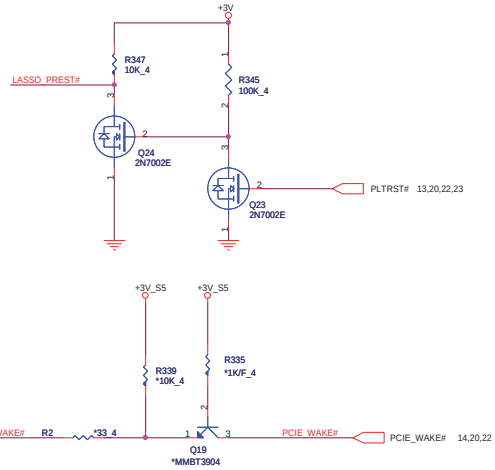
4/20

1pin=0.5A (ACES)

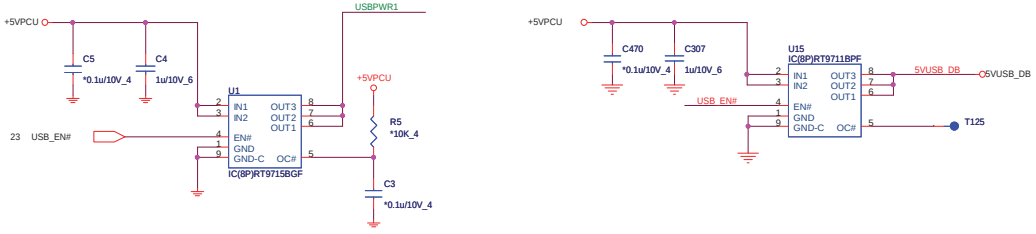




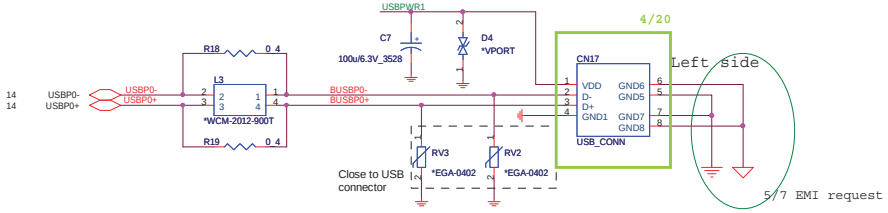
5VUSB_DB	USB PWR	2A	2A
+3V	Card reader	250mA	275mA



(USB)

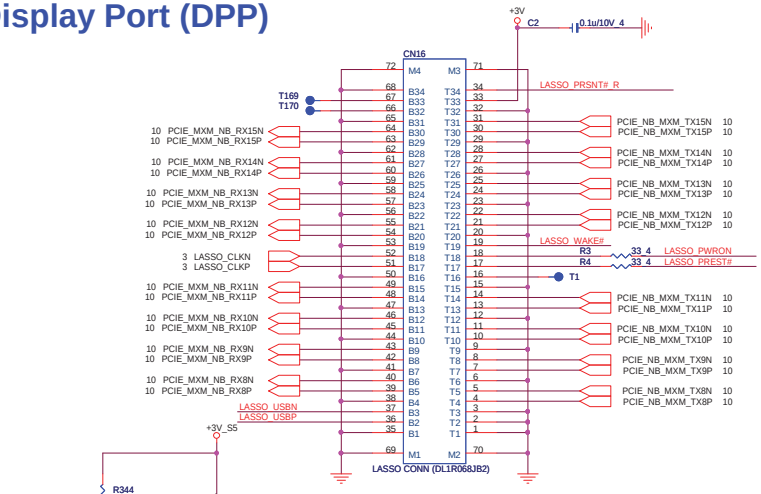


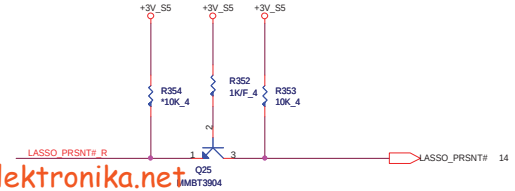
Please reserve Cin = 1uF(stuff),Cout = 10uF(don't stuff) for Richtek RT9711BPF
Please reserve Cin = 4.7uF(stuff),Cout = 10uF(don't stuff) for GMT solution



Placed common mode chokes within 1.0" of the USB connectors

Display Port (DPP)





Quanta Computer Inc.

PROJECT : ZH6

Size	Document Number	Rev
	SATA HDD / AUDIO / LASSO	1A

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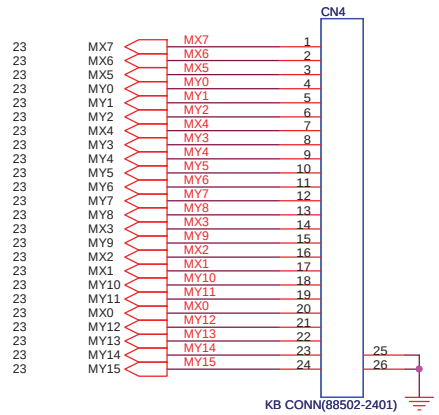
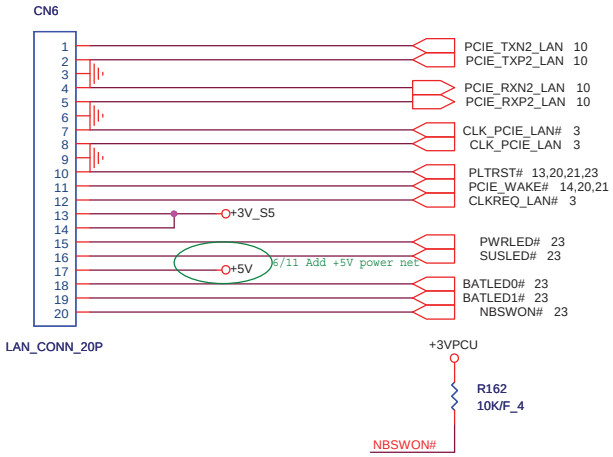
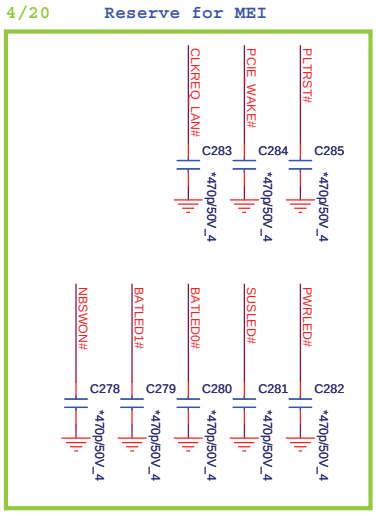
Keyboard(KBC)

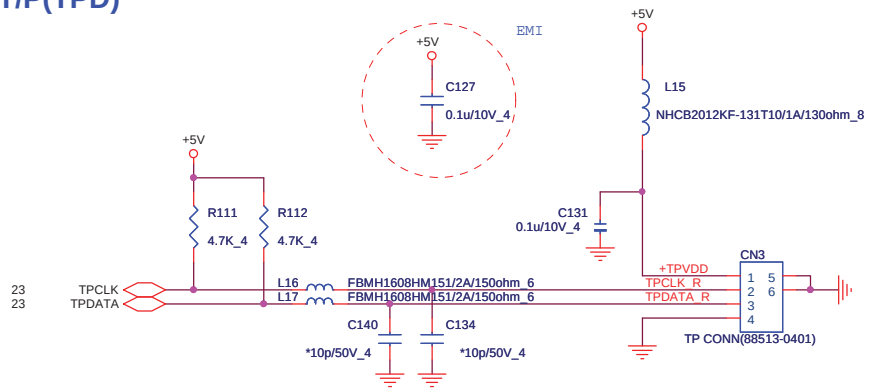


LAN , USBx2 D/B CONNECTER(LAN)

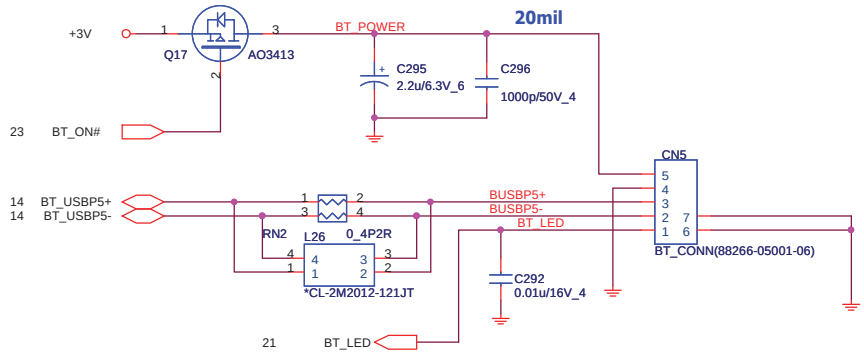




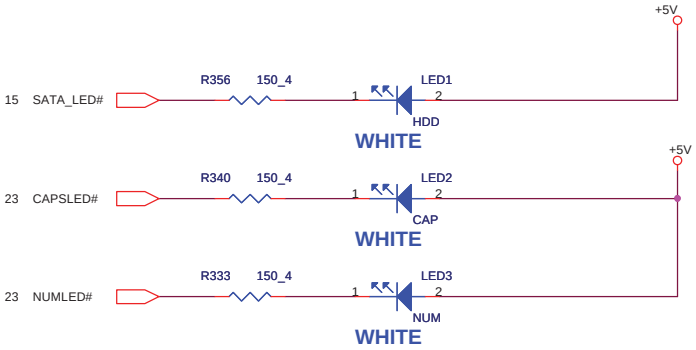
T/P(TPD)



BT(BTM)



LED(UIF)



Quanta Computer Inc.

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Size	Document Number	Rev
	TP/ USB/ KB / LED	1A
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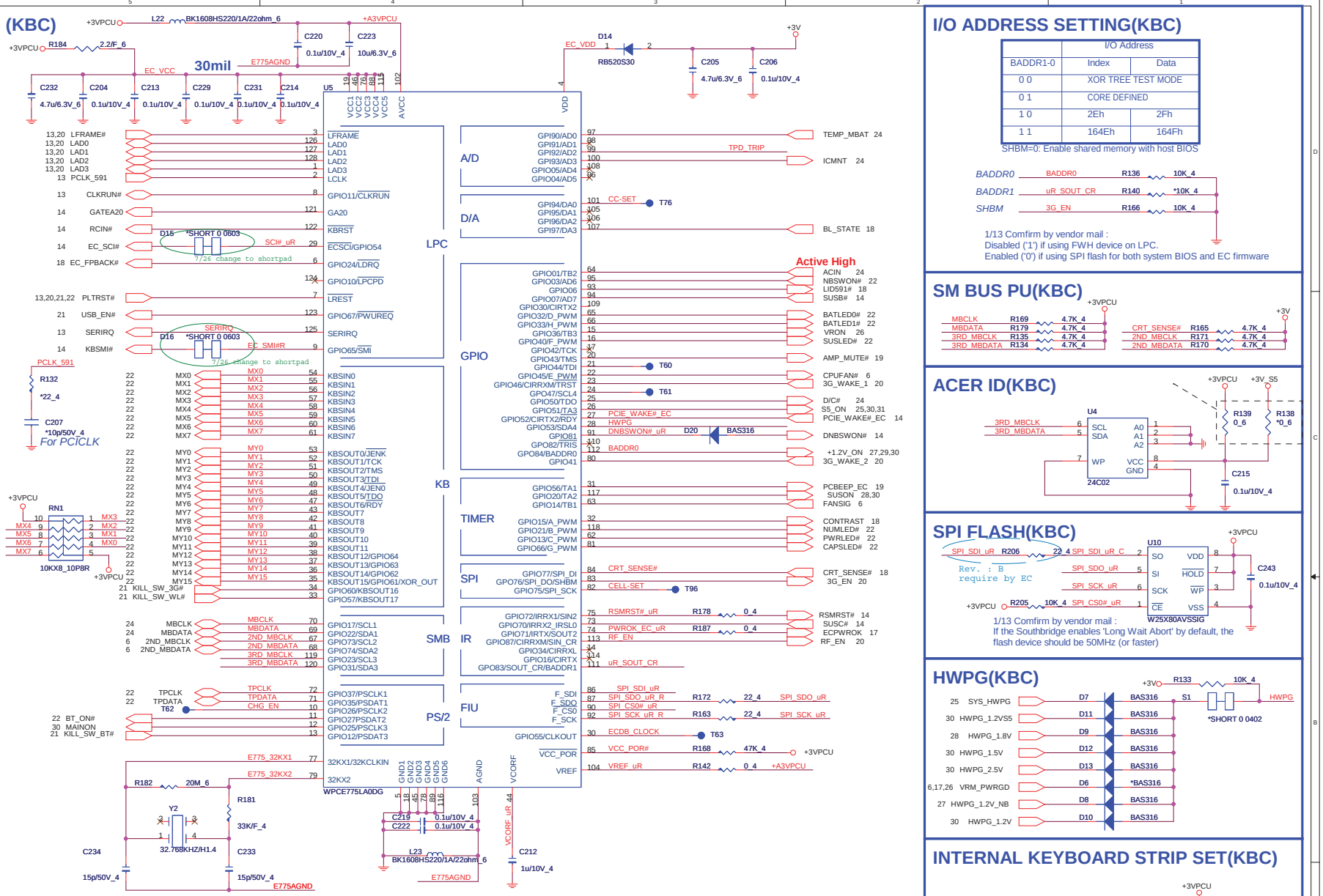
R=3.3-3(Forward V)/20m(condition I)=60 ohm



I/O ADDRESS SETTING(KBC)

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU(KBC)

ACER ID(KBC)

SPI FLASH(KBC)

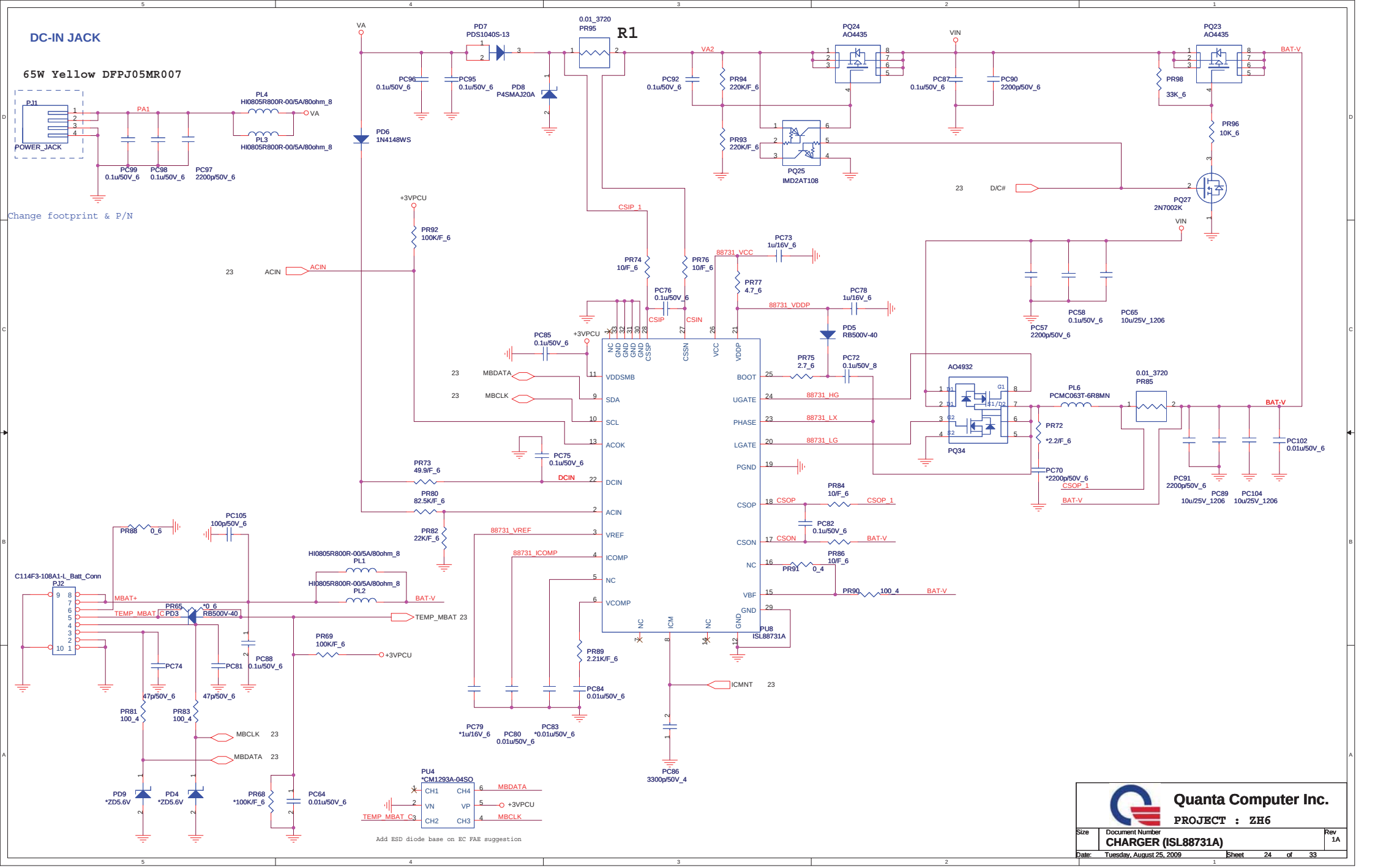
Rev. : B require by EC

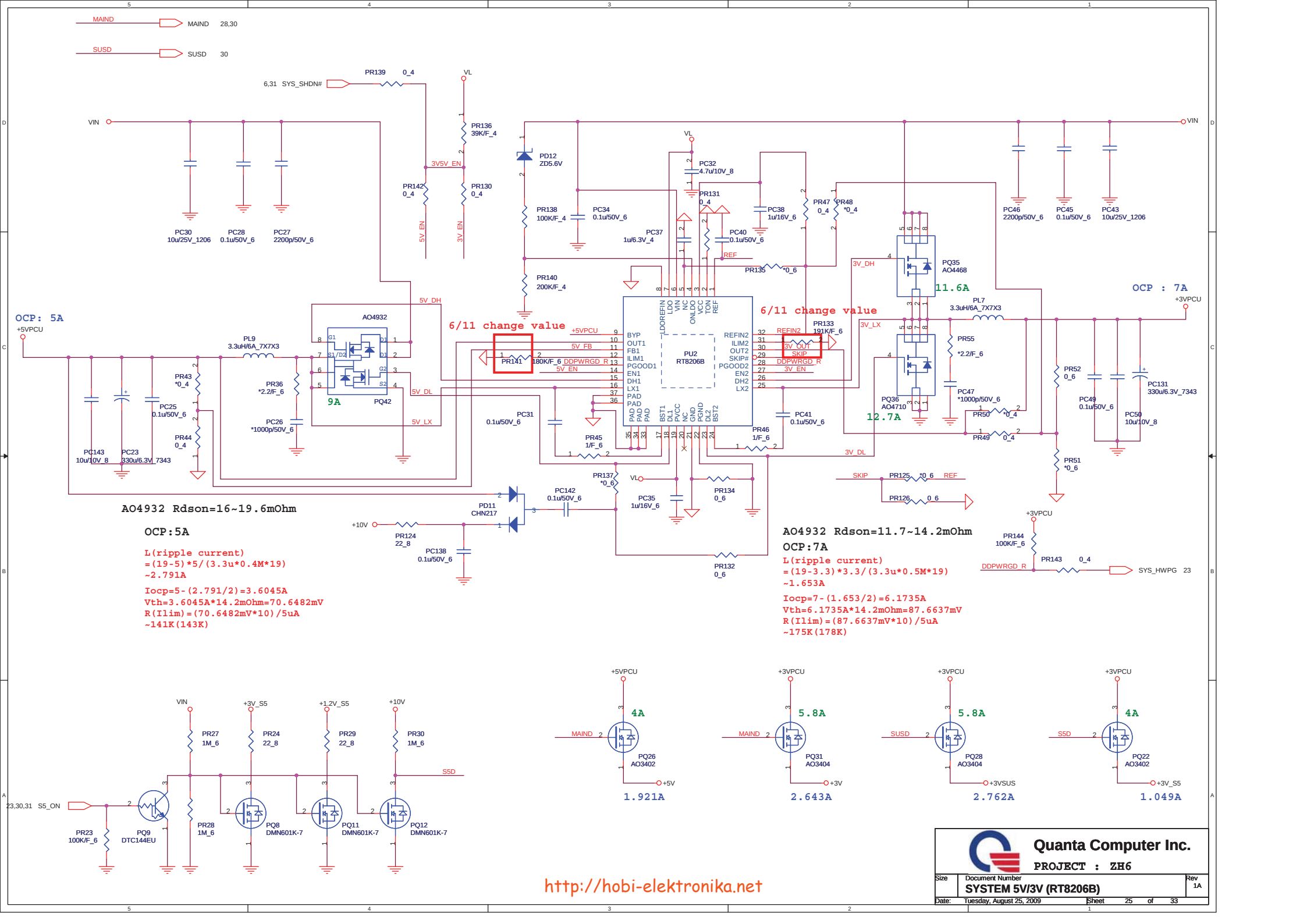
1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

HWPG(KBC)

*SHORT 0 0402

INTERNAL KEYBOARD STRIP SET(KBC)




MAIND
MAIND 28,30
SUSD
SUSD 30
6,31 SYS_SHDN#
PR139 0_4
VL
VIN
PR136 39K/F_4
PR142 0_4
PR130 0_4
3V5V_EN
5V_EN
3V_EN
PC30 10u/25V_1206
PC28 0.1u/50V_6
PC27 2200p/50V_6
PD12 ZD5.6V
PR138 100K/F_4
PC34 0.1u/50V_6
PC32 4.7u/10V_8
PR131 0_4
PC38 1u/16V_6
PR47 0_4
PR48 *0_4
PC37 1u/6.3V_4
PC40 0.1u/50V_6
REF
PR135 *0_6
PR140 200K/F_4
PC46 2200p/50V_6
PC45 0.1u/50V_6
PC43 10u/25V_1206
OCP: 5A
+5VPCU
PL9 3.3uH/6A_7X7X3
AO4932
5V_DH
5V_DL
5V_LX
9A
PQ42
PR43 *0_4
PR44 0_4
PR36 *2.2/F_6
PC26 *1000p/50V_6
PC25 0.1u/50V_6
PC143 10u/10V_8
PC23 330u/6.3V_7343
6/11 change value
PR141 180K/F_6
DDPWRGD_R
5V_FB
5V_EN
PU2 RT8206B
LDOREFIN LDO VIN NC ONLDO VCC TON REF
BYP OUT1 FB1 ILIM1 PGOOD1 EN1 DH1 LX1 PAD PAD PAD
REFIN2 ILIM2 OUT2 SKIP# PGOOD2 EN2 DH2 LX2
BST1 DL1 PVCC NC GND PSN DL2 BST2
PC31 0.1u/50V_6
PR45 1/F_6
PR46 1/F_6
PC41 0.1u/50V_6
PR133 191K/F_6
REFIN2
3V_OUT
SKIP
3V_EN
3V_DH
3V_LX
3V_DL
PQ35 AO4468
PQ36 AO4710
11.6A
12.7A
OCP : 7A
PL7 3.3uH/6A_7X7X3
PR55 *2.2/F_6
PC47 *1000p/50V_6
PR50 *0_4
PR49 0_4
PR52 0_6
PR51 *0_6
PC49 0.1u/50V_6
PC50 10u/10V_8
PC131 330u/6.3V_7343
PR137 *0_6
PC35 1u/16V_6
PR134 0_6
PR132 0_6
PC142 0.1u/50V_6
PD11 CHN217
+10V
PR124 22_8
PC138 0.1u/50V_6
SKIP
PR125 *0_6
REF
PR126 0_6
AO4932 Rdson=16~19.6mOhm
OCP:5A
L(ripple current)
=(19-5)*5/(3.3u*0.4M*19)
~2.791A
Iocp=5-(2.791/2)=3.6045A
Vth=3.6045A*14.2mOhm=70.6482mV
R(Ilim)=(70.6482mV*10)/5uA
~141K(143K)
AO4932 Rdson=11.7~14.2mOhm
OCP:7A
L(ripple current)
=(19-3.3)*3.3/(3.3u*0.5M*19)
~1.653A
Iocp=7-(1.653/2)=6.1735A
Vth=6.1735A*14.2mOhm=87.6637mV
R(Ilim)=(87.6637mV*10)/5uA
~175K(178K)
+3VPCU
PR144 100K/F_6
PR143 0_4
DDPWRGD_R
SYS_HWPG 23
VIN
+3V_S5
+1.2V_S5
+10V
PR27 1M_6
PR24 22_8
PR29 22_8
PR30 1M_6
S5D
23,30,31 S5_ON
PR23 100K/F_6
PQ9 DTC144EU
PR28 1M_6
PQ8 DMN601K-7
PQ11 DMN601K-7
PQ12 DMN601K-7
+5VPCU
4A
MAIND
PQ26 AO3402
+5V
1.921A
5.8A
PQ31 AO3404
+3V
2.643A
SUSD
PQ28 AO3404
+3VSUS
2.762A
S5D
PQ22 AO3402
+3V_S5
1.049A
http://hobi-elektronika.net
Quanta Computer Inc.
PROJECT : ZH6
Size
Document Number
SYSTEM 5V/3V (RT8206B)
Rev 1A
Date: Tuesday, August 25, 2009
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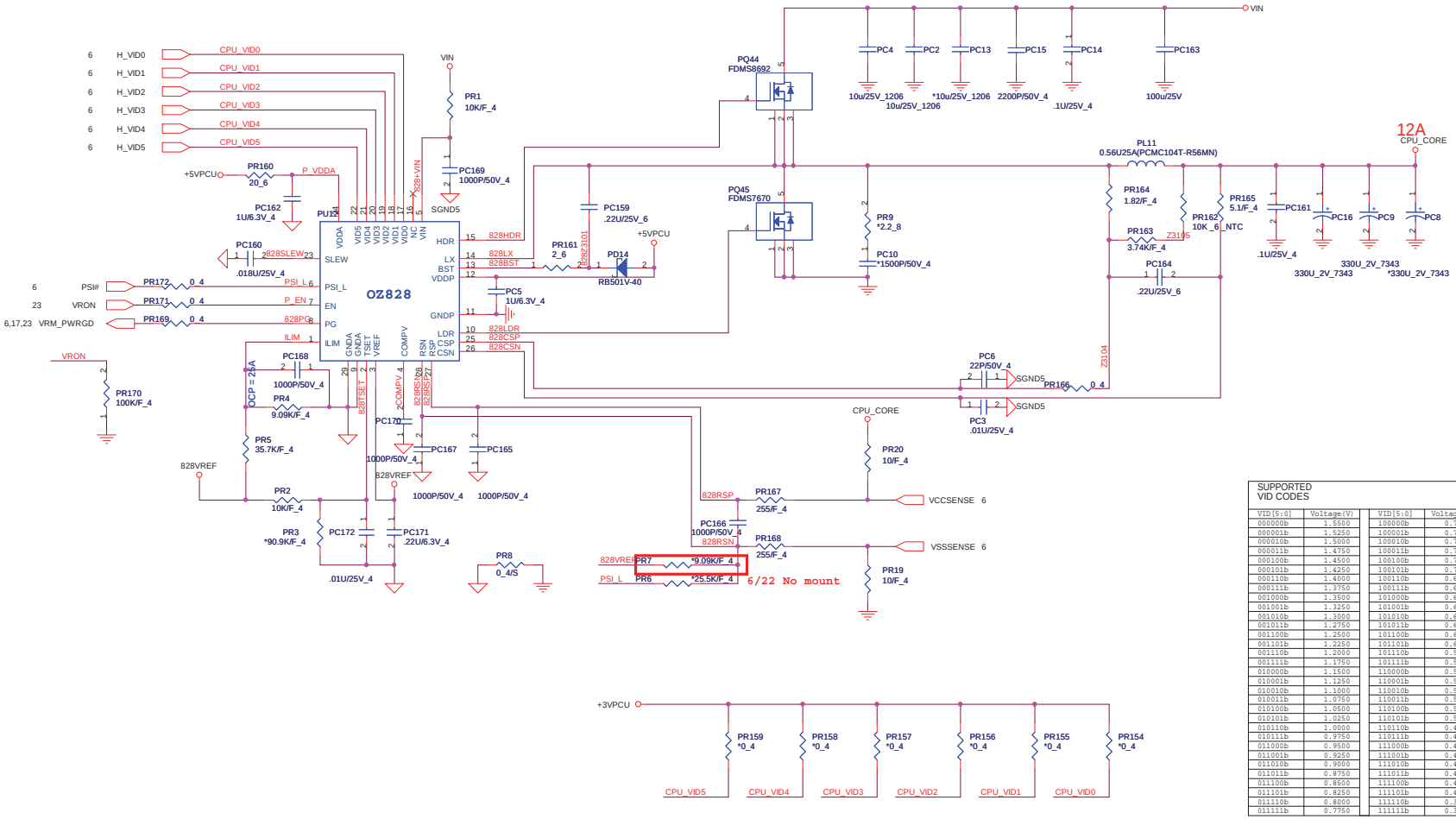

SUPPORTED VID CODES

VID[5:0]	Voltage(V)	VID[5:0]	Voltage(V)
000000b	1.5500	100000b	0.7625
000001b	1.5250	100001b	0.7500
000010b	1.5000	100010b	0.7375
000011b	1.4750	100011b	0.7250
000100b	1.4500	100100b	0.7125
000101b	1.4250	100101b	0.7000
000110b	1.4000	100110b	0.6875
000111b	1.3750	100111b	0.6750
001000b	1.3500	101000b	0.6625
001001b	1.3250	101001b	0.6500
001010b	1.3000	101010b	0.6375
001011b	1.2750	101011b	0.6250
001100b	1.2500	101100b	0.6125
001101b	1.2250	101101b	0.6000
001110b	1.2000	101110b	0.5875
001111b	1.1750	101111b	0.5750
010000b	1.1500	110000b	0.5625
010001b	1.1250	110001b	0.5000
010010b	1.1000	110010b	0.5375
010011b	1.0750	110011b	0.5250
010100b	1.0500	110100b	0.5125
010101b	1.0250	110101b	0.5000
010110b	1.0000	110110b	0.4875
010111b	0.9750	110111b	0.4750
011000b	0.9500	111000b	0.4625
011001b	0.9250	111001b	0.4500
011010b	0.9000	111010b	0.4375
011011b	0.8750	111011b	0.4250
011100b	0.8500	111100b	0.4125
011101b	0.8250	111101b	0.4000
011110b	0.8000	111110b	0.3875
011111b	0.7750	111111b	0.3750

Quanta Computer Inc.
PROJECT : ZH6

Size	Document Number	Rev
	CPU CORE(OZ828)	1A

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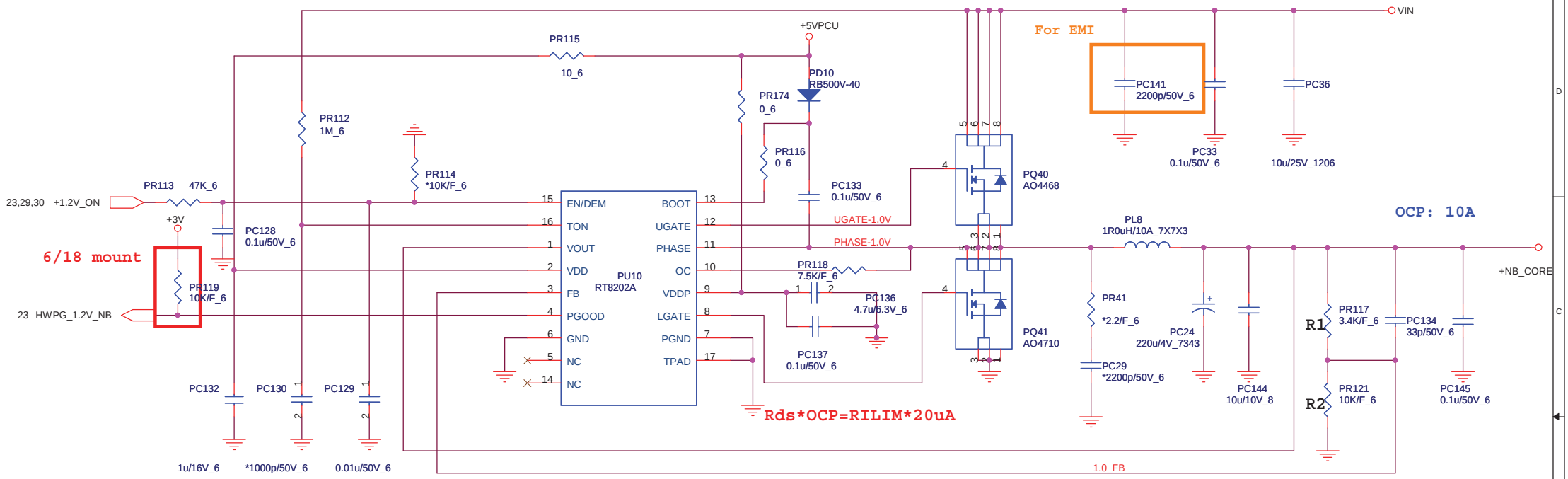


TON=3.85p*RTON*Vout/(Vin-0.5)
Frequency=Vout/(Vin*TON)

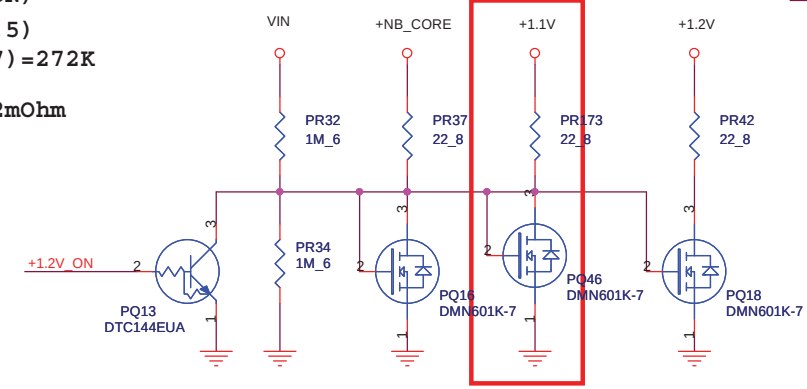
TON=3.85p*1M*1/(Vin-0.5)
Frequency=1/(0.0036767)=272K

AO4710 Rdson=11.7~14.2mOhm

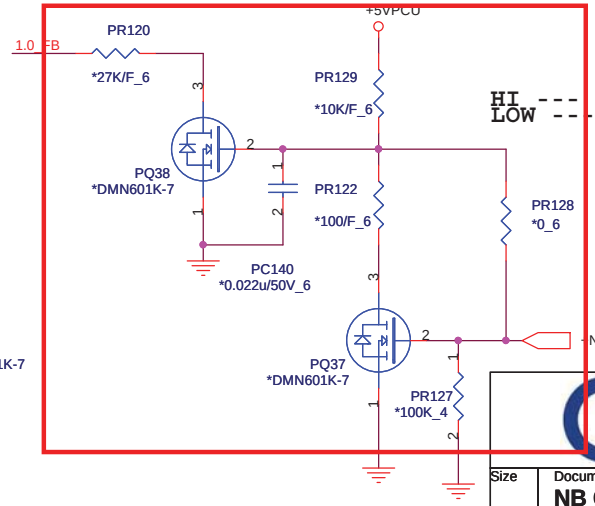
L(ripple current)
=(19-1)*1/(1u*272k*19)
~3.483A

14.2m*10=RILIM*20uA
RILIM=7.1K(7.5K)

6/16 add



VOUT=(1+R1/R2)*0.75



Quanta Computer Inc.
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Size	Document Number	Rev
	NB CORE(RT8202A)	1A
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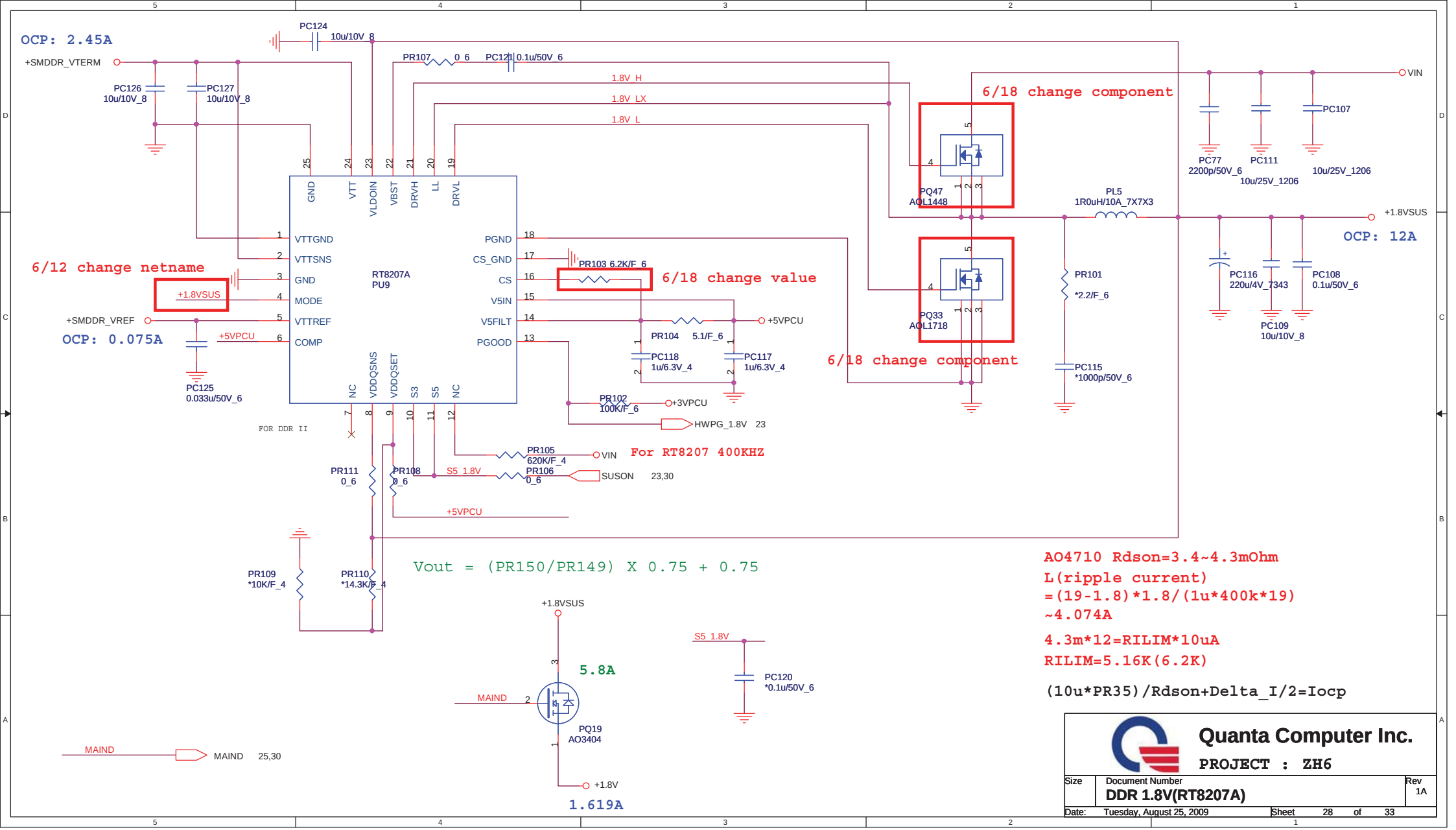

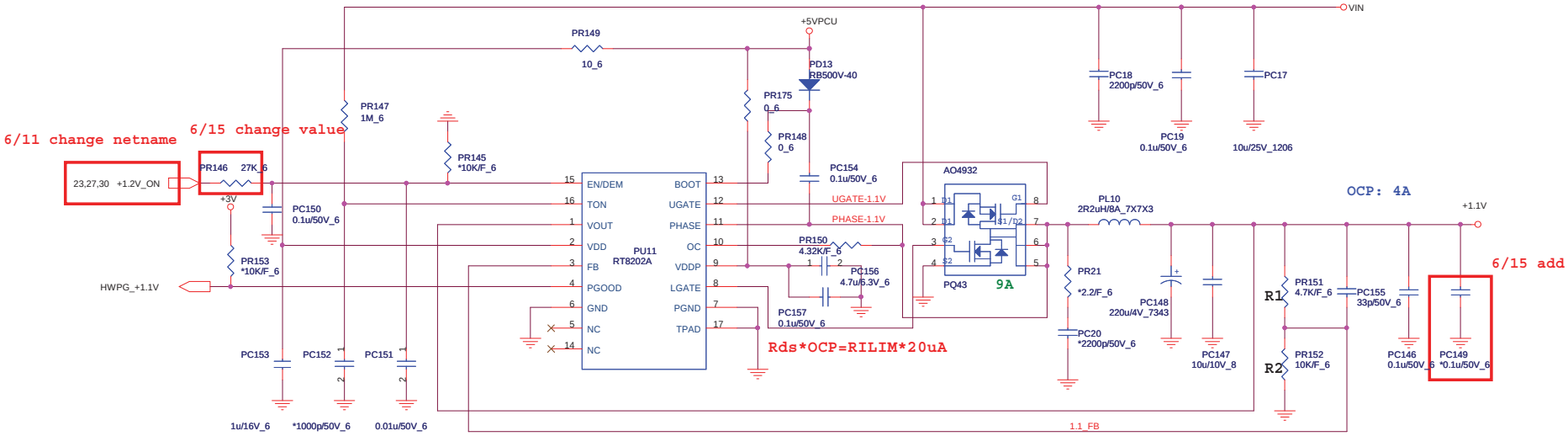

VOUT=(1+R1/R2)*0.75

TON=3.85p*1M*1/(Vin-0.5)
Frequency=1/(0.0036767)=272K

AO4932 Rdson=16~19.6mOhm

L(ripple current)
=(19-1.1)*1.1/(2.2u*272k*19)
~1.732A

19.6m*4=RILIM*20uA
RILIM=3.92K(4.32K)

Quanta Computer Inc.		
PROJECT : ZH6		
Size	Document Number: +1.1V(RT8202A)	Rev: 1A
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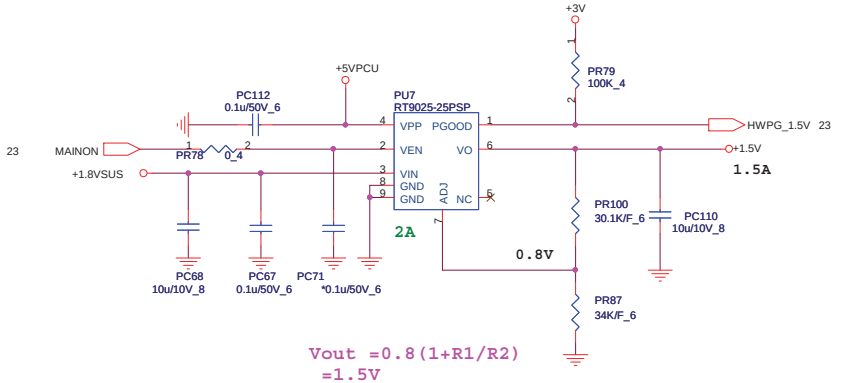
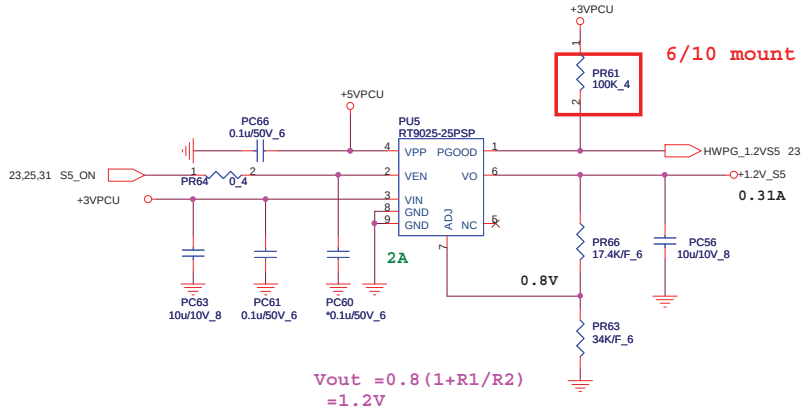
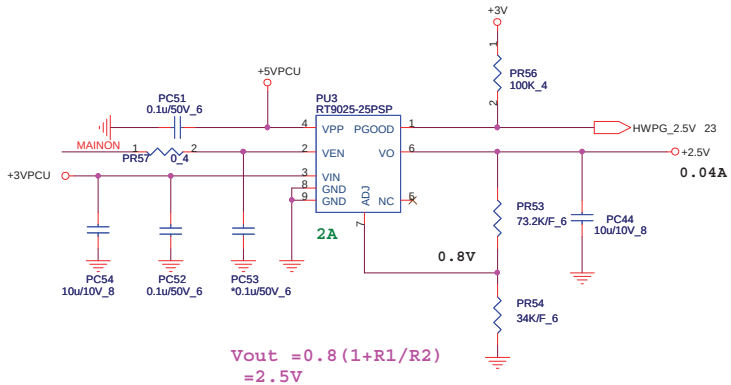
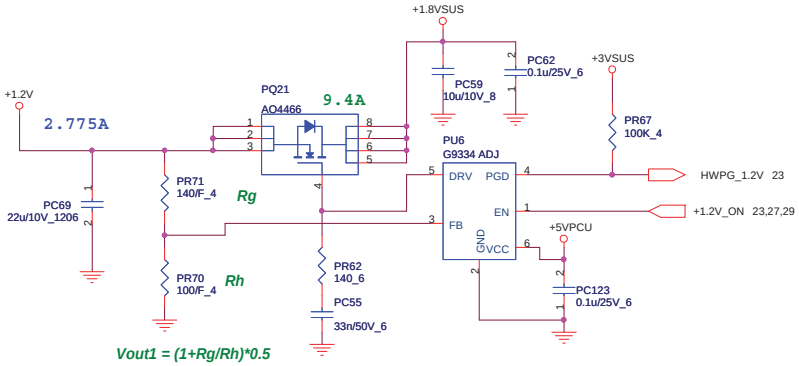
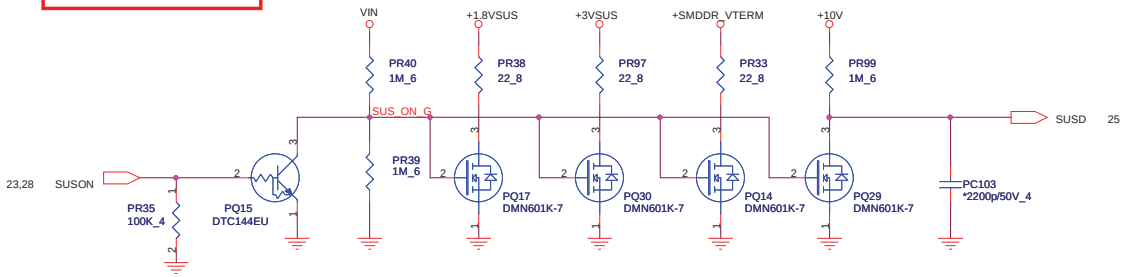




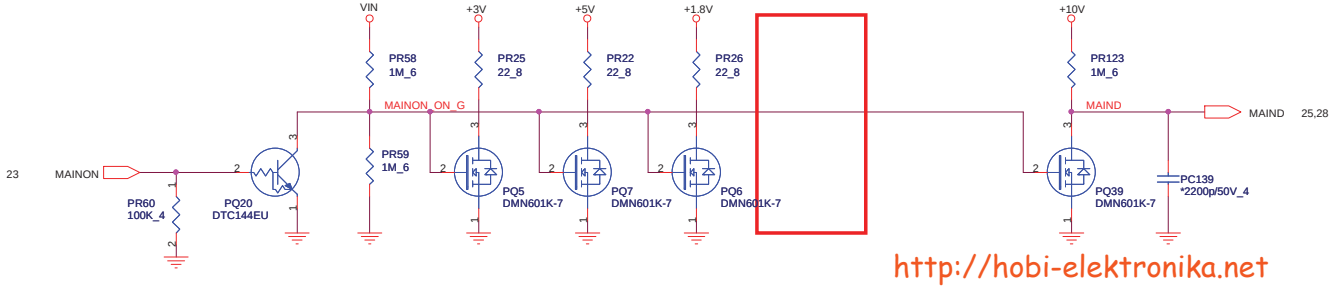




6/18 Add



6/15 remove +1.1V



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Size	Document Number	Rev
	Discharge (2.5V/1.5V/1.2V)	1A

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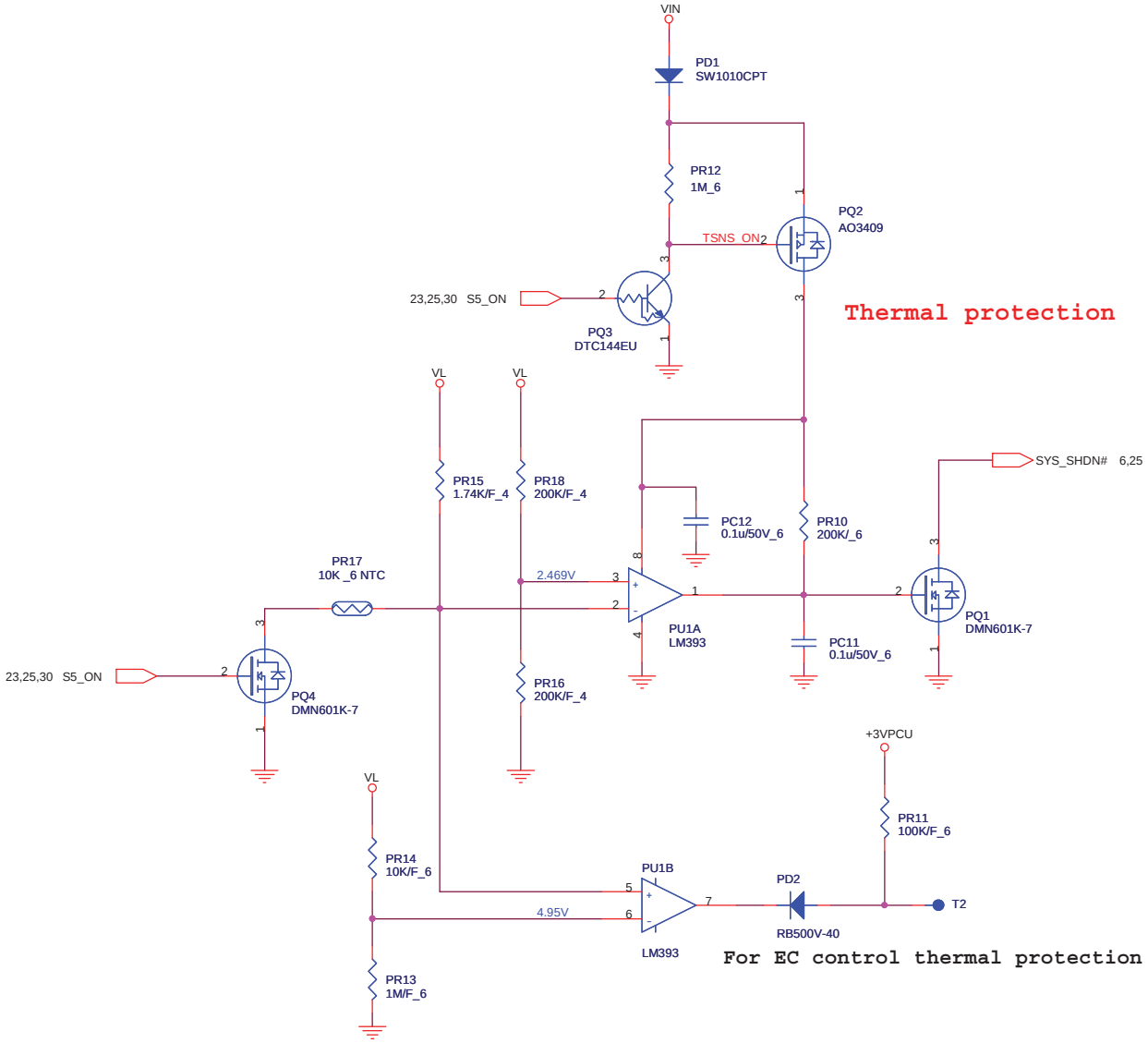

Quanta Computer Inc.		
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Size	Document Number: Thermal protect	Rev 1A
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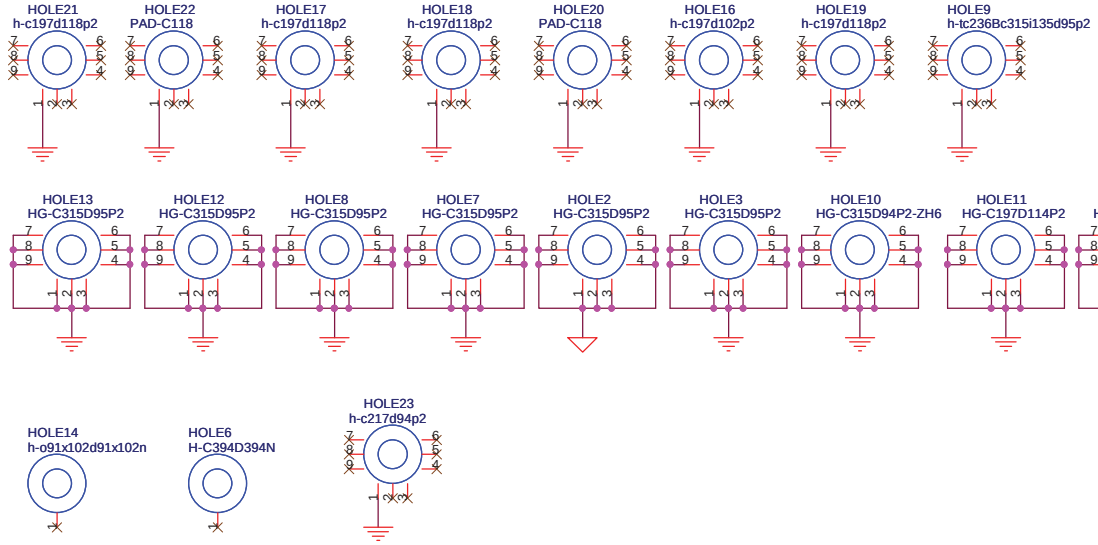
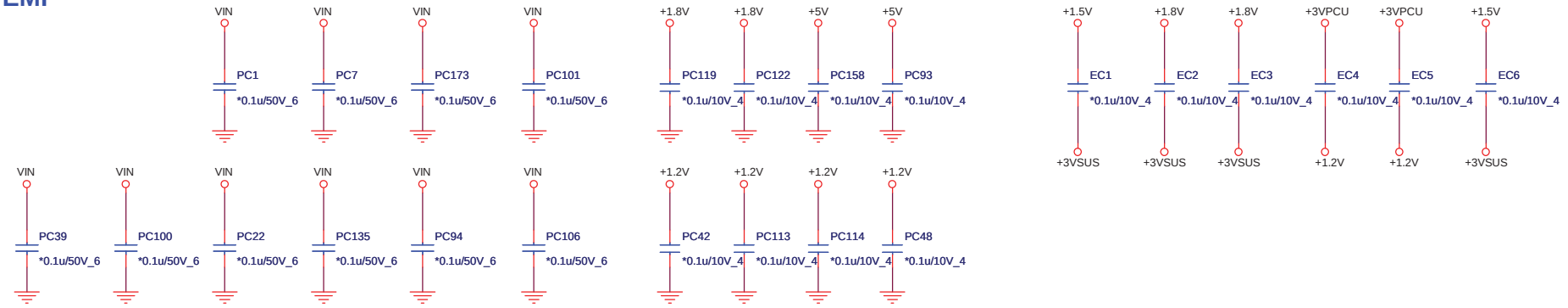


EMI



Quanta Computer Inc.		
PROJECT : ZH6		
Size	Document Number: HOLE /EMI	Rev: 1A
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Model	REV	DATE	CHANGE LIST	NOTE
ZH6		20090326	Page 30: Evan Wang add a Power source of +1.1V Page 22: add LED circuit	
		20090331	Page 3: add R5349~5356 & C32455	
		20090401	Page 20 : add LASSO circuit	
		20090402	Page 23 : remove WLAN LED and SW conn circuit Page 22 : remove LED circuit Page 19 : Change AMPLIFIER G1453L to G1431P2U circuit	
		20090403	Page 23 : add CN5021 LAN conn circuit Page 22 : Modify CN7 USB ,LAN circuit to LED , Kill SW circuit	
		20090406	Page 18 : add HALL SENSOR circuit	
		20090408	Page 23 : CN4 4Pin change to 6Pin Page 08 : add CN5022 SO-DIMM circuit	
		20090410	Page 19 : Change codec ALC272 to ALC269 Page 20 : Change LAN RTL8103L to AR8131	
		20090413	Page 20 : Change SATA CONN to 10 pin (85203-10021) Page 23 : add CAPS,SATA,NUM LED circuit	
		20090414	Page 20 : remove LAN chip (AR8131) circuit to DB board	
		20090416	Page 18 : Change LVDS CONN CN1 Pin define Page 11 : remove R2368,R2073 Page 09 : remove C57 & change R34 to 0ohm	
		20090420	Page 21 : add EMI CAP C32554~C32562 Page 22 : add EMI CAP C32563~C32570 Page 23: add BT_SW and WL/3G_SW circuit (SW1,SW2,R5438,R5437,C79,C80,C82)	
		20090423	Page 32 : add EMI CAP PC5042~PC5049 for EMI Page 19 : modify SPDIF pin place Page 14 : modify USB port define	
		20090423	Page 21 : Modify CN7 +3VPCU to +5VPCU	
		20090427	Page 05 : add CAP C32574,C32575	
		20090429	Page 23 : remove S2 ,EC_PROCHOT ,INT_LVDS_DIGON&INT_LVDS_BLON singal Page 21: CN5024 modify pin define Page 22: change CAP ,NUM LED lamp input voltage to +3V	
		20090611	Page 12: Add C164 for VDDHTTX noise reduction Page 14: Lasso_Present reserve U7.B8 in SB	
		20090615	Page 17: Add U16 for NB_PWRGD_IN glitch issue Page 21: change HDD connector to cable type	
		20090712	Page 6: Add R104 for VRM_PWRGD pull high Page 19: Change codec to ALC272 Page 23: Change R184 to 2.2ohm for ESD solusion	
		20090824	Page 32: Reserve EC1~EC6 for RF noise reduction Page 27: Add PR174 for IC EOS issue Page 29: Add PR175 for IC EOS issue	

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	Change List01	1A

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