PWA : Y507R
PWB : Y509R
SCH : Y510R

Calpella Intel Discrete Block Diagram

VER : D3A

SYSTEM POWER

PCH REGULATOR +1.05V_PCH PG 49	SYS VR +5V_ALW2/+3.3V_ALW +5V_ALW/+15V_ALW PG 51	VGA Core +VCC_GFX_CORE +1.1V_GFX_PCIE PG 52
DDR3 VR +1.5V_SUS/+0.75V_DDR_VTT PG 47	CPU VR +1.1V_VTT PG 48	REGULATOR +1.8V_RUN PG 46
Load Switch +5V_SUS/+3.3V_SUS/+5V_RUN/ +3.3V_RUN/+1.5V_RUN/ +1.5V_GDDR PG 54	VCC Core +VCC_CORE PG 50	VGA VDDCI +VDDCI PG 53

POWER

- AC/BATT CONNECTOR PG 55
- BATT CHARGER PG 45

CLOCK SLG8SP585V (QFN-64) PG 15

FAN & THERMAL EMC1422 (8P TSSOP) PG 37

Clarksfield (Qual Core) (989 PGA) PG 3,4,5,6

DDR3-SODIMM1 PG 13 — 800 / 1066 MHZ DDR III

DDR3-SODIMM2 PG 14 — 800 / 1066 MHZ DDR III

PCIEx16

AMD M96XT PCI EXPRESS GFX (962 FCBGA) PG 17,18,19,20

- HDMI → HDMI CONN. PG 23
- DP → DISPLAYPORT PG 23
- LVDS → Panel Connector PG 24
- VGA → CRT CONN. PG 25

DDR3 x 8 (1G, 64Mx16 bit) (100P FBGA) PG 21,22

GPU THERMAL ANALOG DEVICES ADM1032 (8 MSOP) 3 x 3 mm PG 20

DMI x 4

Ibex Peak-M PG 7,8,9,10,11,12

IHDA

AUDIO IDT 92HD73C (56 LQFP) 9 x 9 mm PG 38

- Subwoofer CONN PG 40
- Subwoofer AMP MAXIM MAX9759 (16 Pin TQFN) PG 40
- MIC
- Internal Speaker
- Amplifier TI TPA6040A4 (32 Pin QFN) PG 39
- HP2
- HP1
- Amplifier TI TPA4411MRTJR (20 Pin QFN) PG 39

- Camera + D-MIC PG 35 — USB2.0 [11]
- TV CONN PG 33 — USB2.0 [9]
- USB CONN — USB2.0 x 2 [0:1]
- USB/eSATA Combo PG 33 & eSATA board — USB2.0 [8]
- SATA-ODD PG 34 — SATA2 [A5]
- SATA-HDD PG 34 — SATA2 [A1]
- 1394 CONN PG 27 — SATA2 [A0]
- CardReader CONN PG 27 — PCIE [5]

PC Card/1394 RICOH R5U230 (48 Pin QFN) 6 x 6 mm PG 26

- PCIE [1] / USB2.0 [5] → WWAN MINI-CARD PG 32
- PCIE [2] / USB2.0 [4] → WLAN Half MINI-CARD PG 31
- PCIE [3] / USB2.0 [6] → UWB/BT MINI-CARD PG 32
- PCIE [4] / USB2.0 [7] → Express Card PG 28 → Express Switch RICOH R5538D001 (20 QFN) 4 x 4 mm PG 28
- PCIE [6] → LAN Broadcom BCM5784M (68P QFN) PG 41 → Magnetic PG 42 → RJ45 PG 42

LPC

SIO ITE ITE8512E (128 Pin LQFP) 16 x 16 mm PG 29

SPI

SMBus [2]

PS/2

- PAD & SCREW & SPRING PG 44
- System Reset Circuit PG 43
- To IO Board (USB*2/ MIC/ HP2/ HP1/ LED) PG 40
- To Daughter Board (Power Button/Speaker/ KB LED/Touch PAD/ Media Button) PG 35

- SPI ROM 2MB (8 Pin SO8W) PG 30
- Keyboard PG 35
- CIR PG 30
- Touchpad
- Media Button
- LED PG 36
- RTC PG 30

RM5 MB PCB (rev D)

QUANTA COMPUTER

Title	BLOCK DIAGRAM		
Size	Document Number Calpella		Rev 3A
Date:	Thursday, August 20, 2009	Sheet 1 of 61	

Table of Contents

Power States

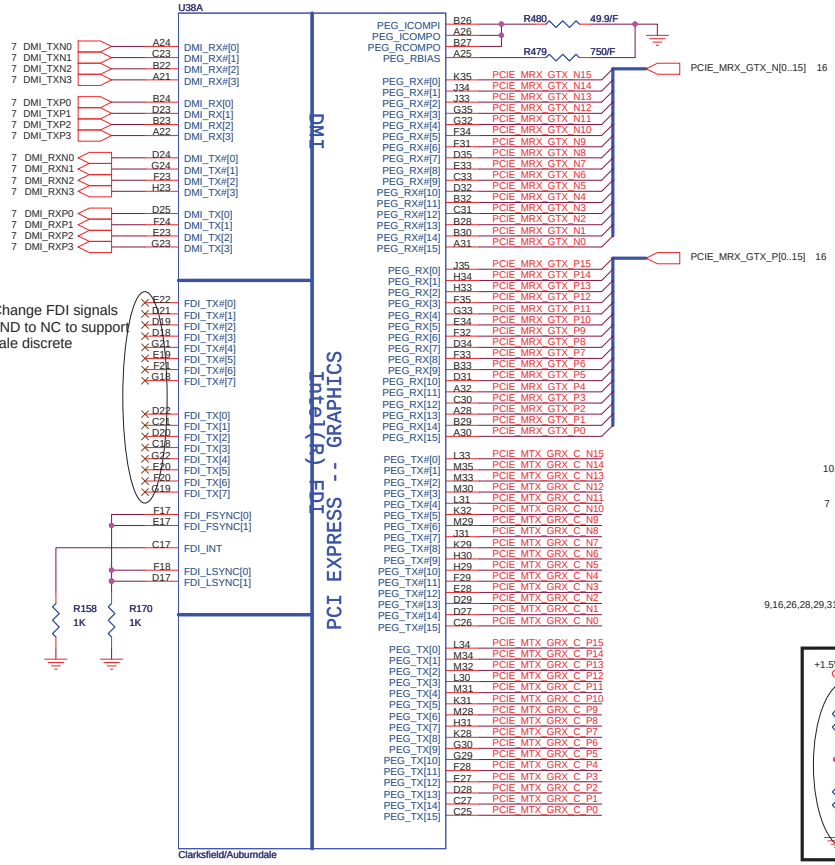
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51,52,53	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	8,11,29,30	RTC		S0~S5
+3.3V_ALW	+3.3V	3,29,30,34,35,36,43,45,51,54,55	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	24,33,34,35,47,51,52,54	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	24,34,51,54	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	41,42	LAN POWER	AUX_ON	
+5V_SUS	+5V	11,46,48,49,52,53,54	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	7,8,9,10,11,20,24,28,29,42,43,46,47,48, 49,52,53,54	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.5V_SUS	+1.5V	3,5,13,14,47,52,54	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,54	SODIMM POWER	SUS_ON	
+5V_RUN	+5V	11,18,23,25,33,35,36,37,38,50,54	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	7,8,9,10,11,13,14,15,18,23,24,26,28,29,30,31, 32,33,34,35,36,37,38,39,40,41,50,52,54,56	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	5,11,17,18,19,46,54	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	28,31,32,54	PCH POWER	1.5V_RUN_ON	
+1.1V_VTT	+1.1V	3,5,10,11,48,50,56	CPU POWER	RUN_ON	
+1.05V_PCH	+1.05V	8,9,11,15,49	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.5V	5,50	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	34	Module Power	MODC_EN#	
+5V_HDD	+5V	34	HDD Power	HDDC_EN#	
+5V_ALW2	+5V	35,36,51,54,55	LED power source	LDO output	

GND PLANE	PAGE	DESCRIPTION
AGND	38,39,40	
AGND_DC/DC	51	
AGND_VCORE	50	
GND	ALL	

QUANTA COMPUTER

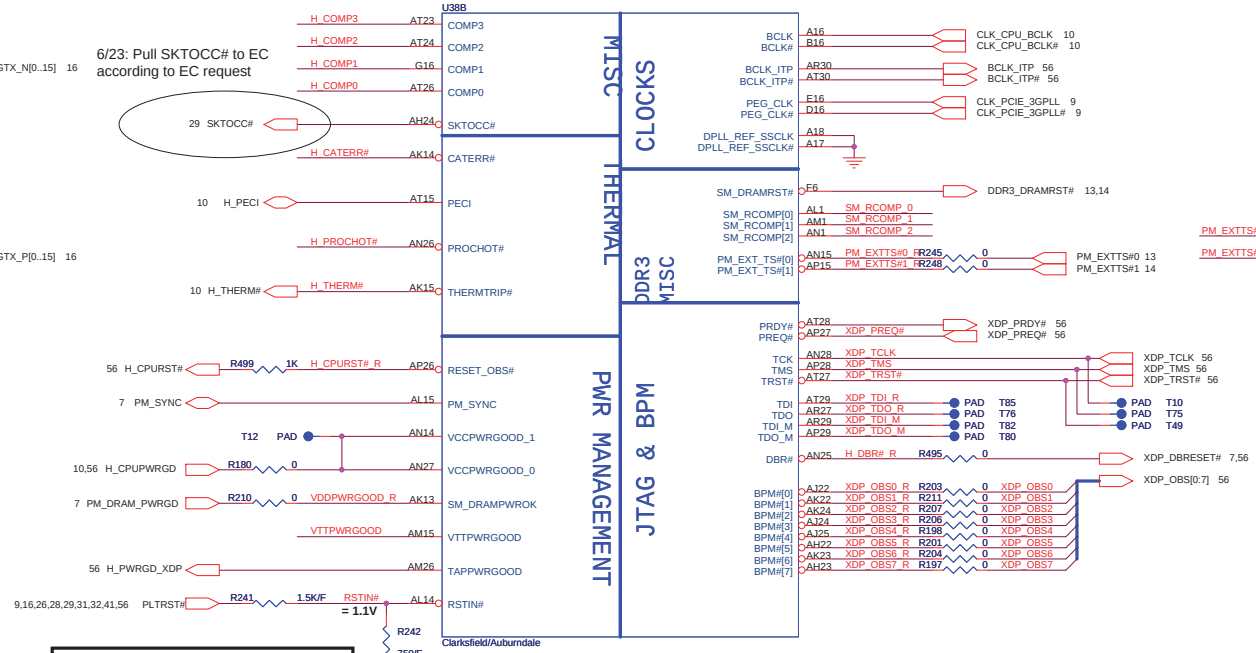
Title	FRONTPAGE	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 2 of 61	

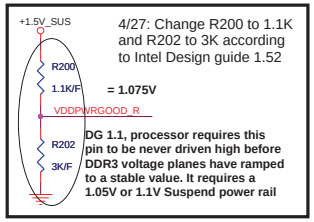
AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)

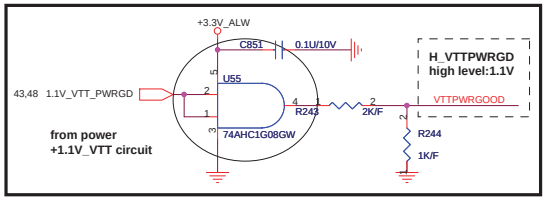


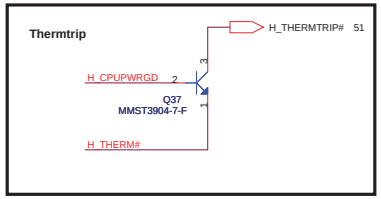
5/14: Change FDI signals from GND to NC to support Arrandale discrete

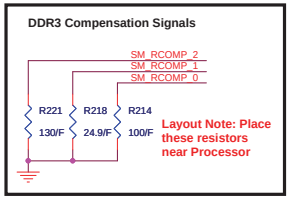
AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



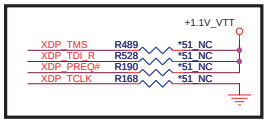


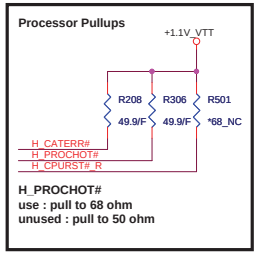


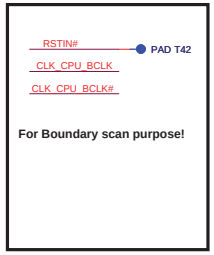


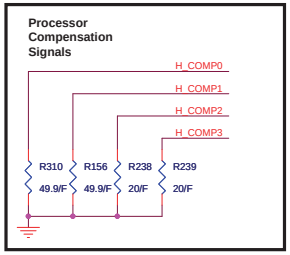


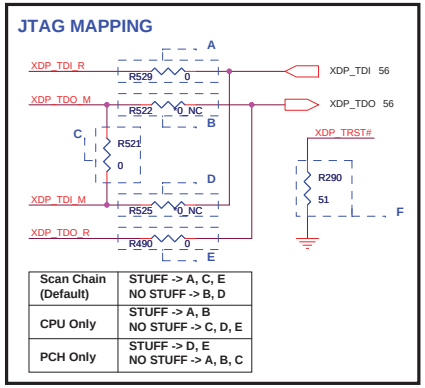
5/3: Added buffer to prevent power good voltage to fluctuate









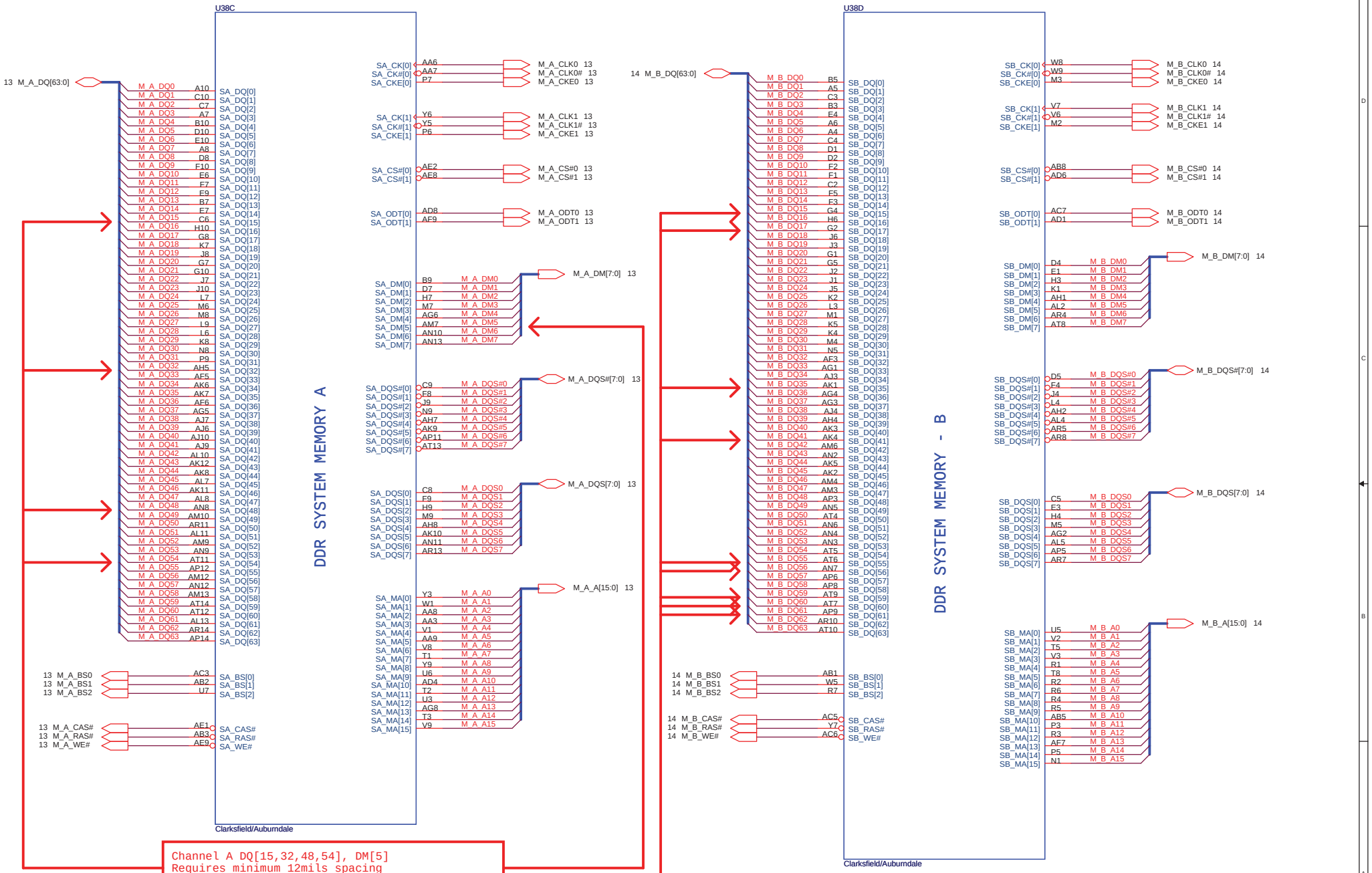


Scan Chain (Default)	STUFF -> A, C, E NO STUFF -> B, D
CPU Only	STUFF -> A, B NO STUFF -> C, D, E
PCH Only	STUFF -> D, E NO STUFF -> A, B, C

QUANTA COMPUTER

Title	CPU 1/4(PEG/DMI)		
Size	Document Number RM5		Rev 3A
Date: Thursday, August 20, 2009		Sheet 3 of 61	

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.

QUANTA COMPUTER

Title	CPU 2/4(DDR)	
Size	Document Number RM5	Rev 3A
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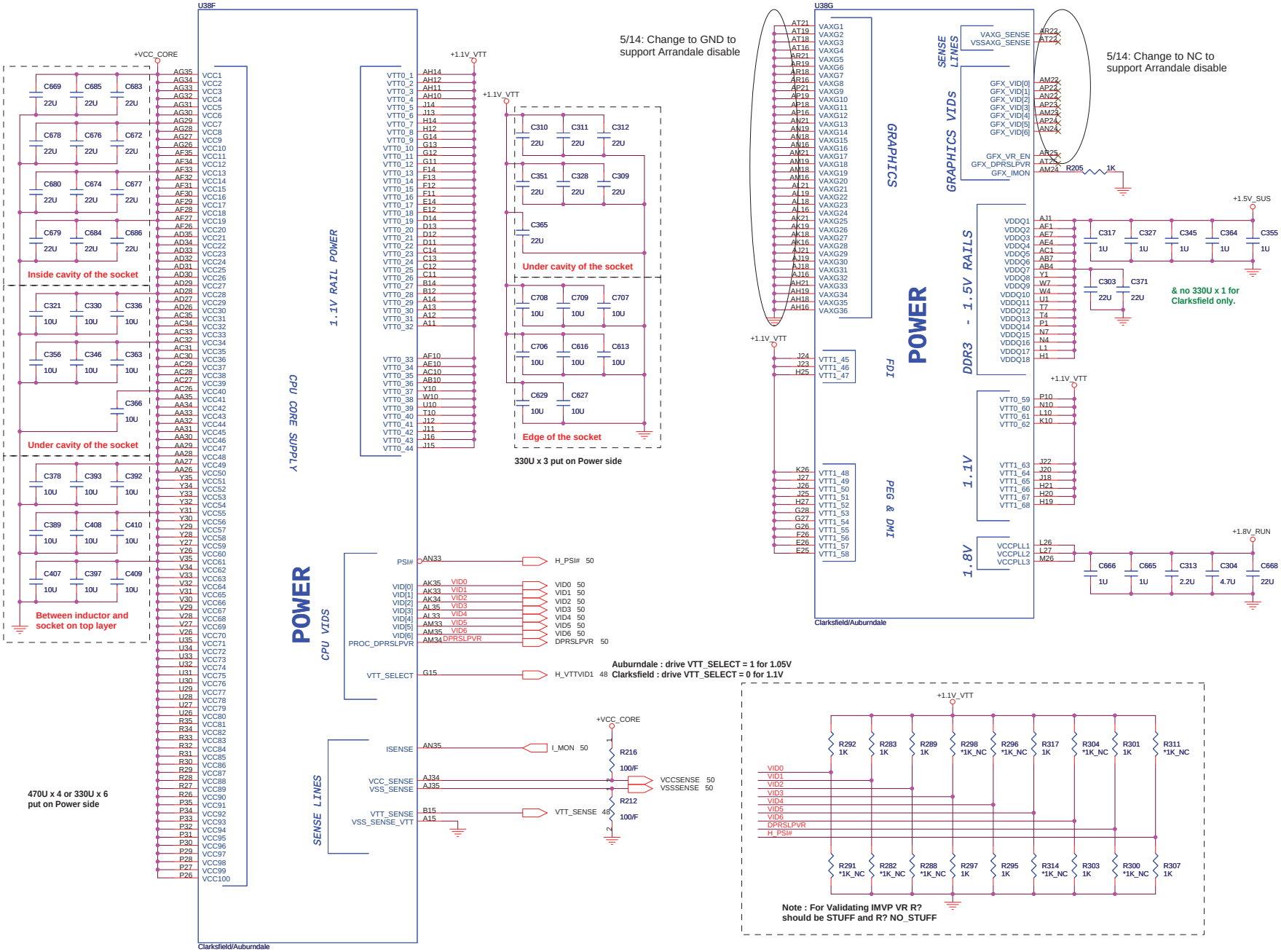
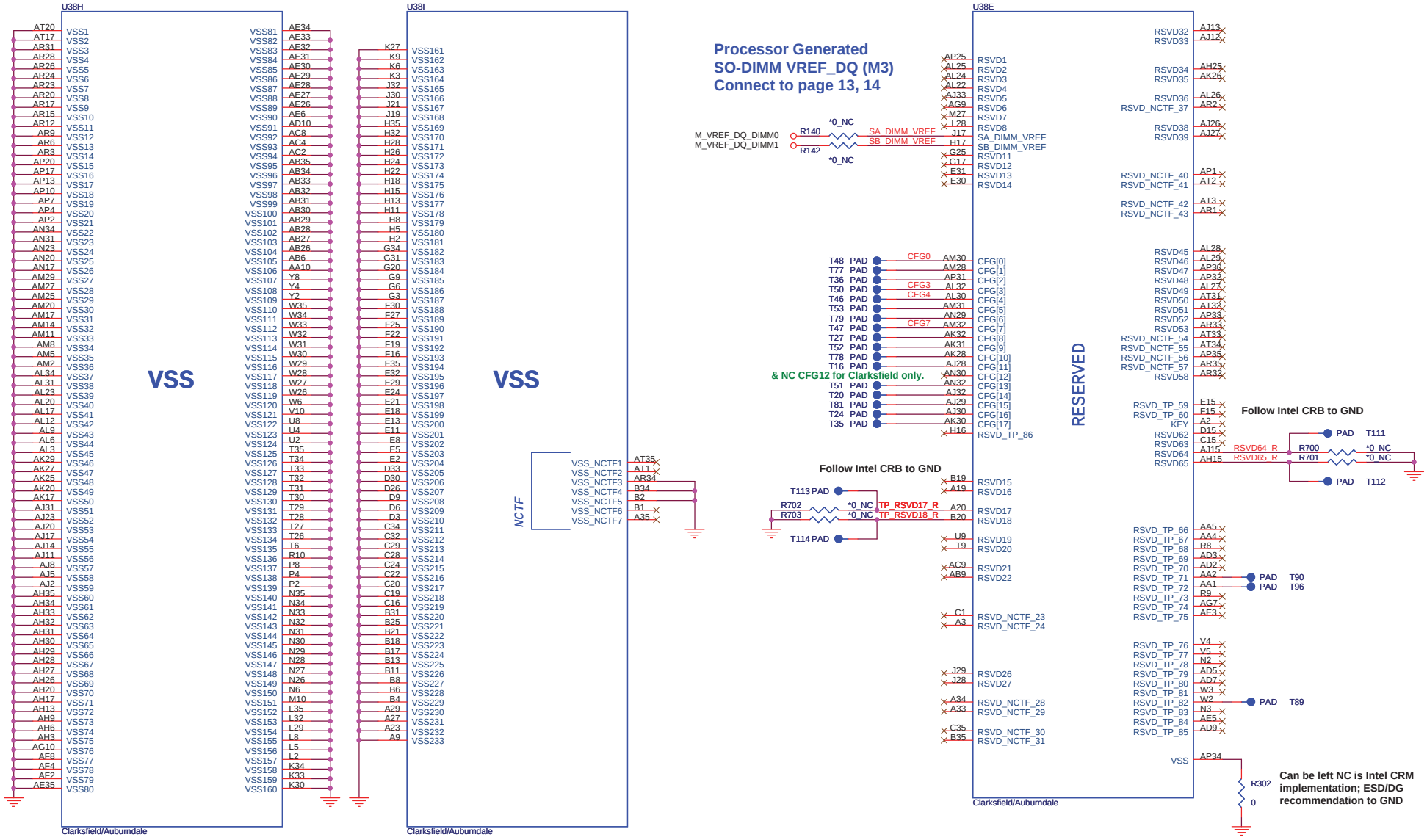
AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)



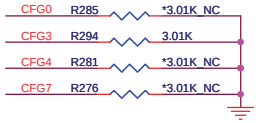
AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Scott_0630:Change R294 footprint from RC0402-C to RC0402



The Clarksfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG0 (PCI-Epress Configuration Select)	**Single PEG (Default)**	**Bifurcation enabled**
CFG3 (PCI-Epress Static Lane Reversal)	**Normal Operation (Default)**	**Lane Numbers Reversed**
CFG4 (Display Port Presence)	**Disabled; No Physical Display Port attached to Embedded Diplay Port (Default)**	**Enabled; An external Display port device is connected to the Embedded Display port**
CFG7 Clarksfield (only for early samples pre-ES1)	**Common motherboard design**	**For early samples pre-ES1 CFD (Default)**

QUANTA COMPUTER

Title	CPU 4/4(GND_RESV)	
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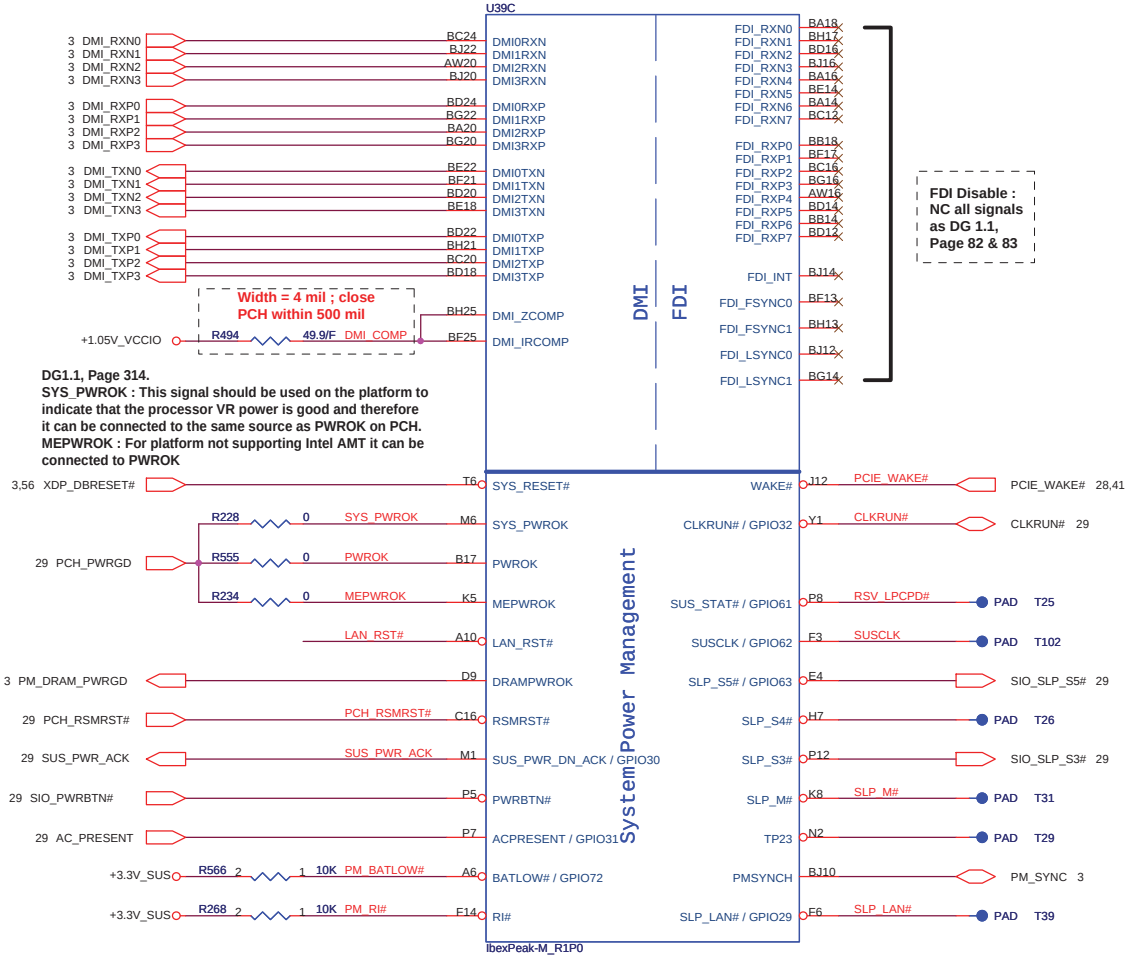
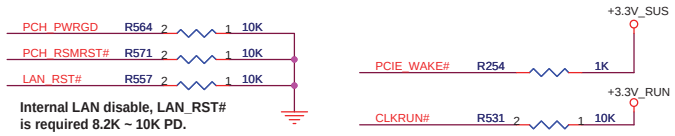
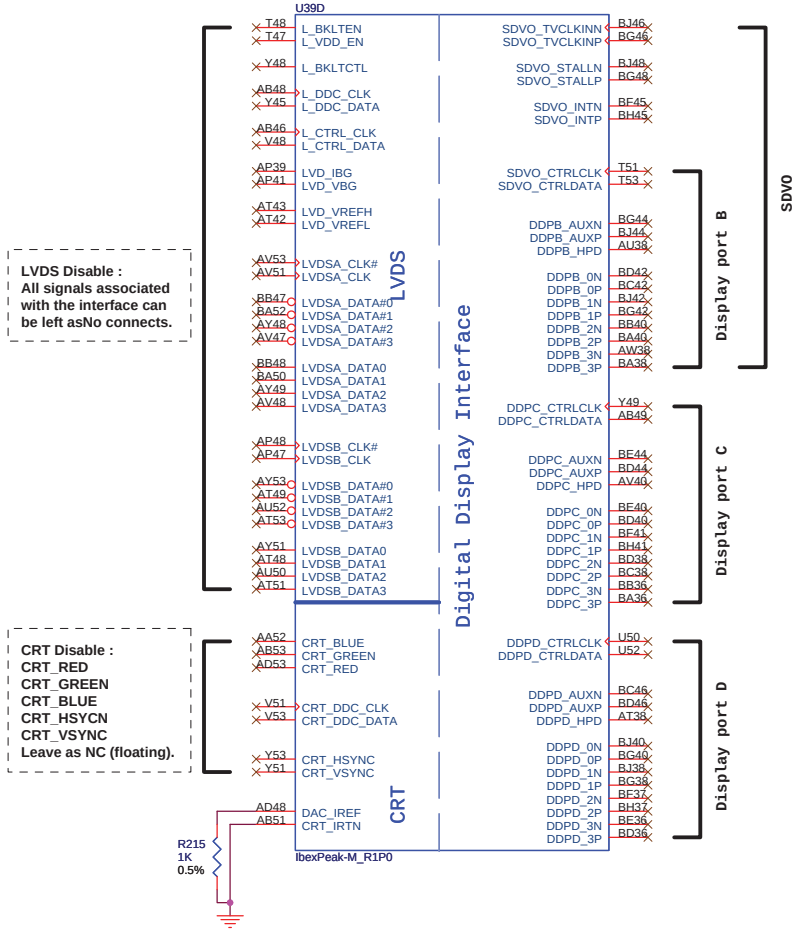
IBEX PEAK-M (DMI,FDI,GPIO)





IBEX PEAK-M (LVDS,DDI)



QUANTA COMPUTER

Title	PCH 1/6(DMI_VIDEO)	
Size	Document Number RM5	Rev 3A
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IBEX PEAK-M (HDA,JTAG,SATA)

+RTC_CELL

R570 1M

R568 20K

R574 20K

Cap values depend on Xtal

C701 15P/50V

Y3 32.768KHZ

C696 15P/50V

R552 10M

RTC_X1

RTC_X2

C700 1U/10V

C699 1U/10V

RTC_RST#

SRTC_RST#

SM_INTRUDER#

+RTC_CELL R556 330K PCH_INVRMEN

INTVRMEN(Internal Voltage Regulator Enable) :
This signal enables the internal 1.05 V regulators.
This signal must be always pulled-up to VccRTC.

U39A

RTC: RTCX1 B13, RTCX2 D13, RTCRST# C14, SRTCRST# D17, INTRUDER# A16, INTVRMEN A14

LPC: FWH0 / LAD0 D33, FWH1 / LAD1 B33, FWH2 / LAD2 C32, FWH3 / LAD3 A32, FWH4 / LFRAME# C34, LDRQ0# A34, LDRQ1# / GPIO23 F34, SERIRQ AB9

PAD T92, PAD T34

LPC_LAD0 29,32
LPC_LAD1 29,32
LPC_LAD2 29,32
LPC_LAD3 29,32
LPC_LFRAME# 29,32
IRQ_SERIRQ 29

38 ICH_AZ_CODEC_BITCLK R562 33 ACZ_BIT_CLK
C703 *27P/50V_NC
38 ICH_AZ_CODEC_SYNC R273 33 ACZ_SYNC
29,38 ICH_AZ_CODEC_RST# R561 33 ACZ_RST#
38 ICH_AZ_CODEC_SDOUT R573 33 ACZ_SDOUT

Place all series terms close to PCH (within 500 mil) except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

IHDA: ACZ_BIT_CLK A30 HDA_BCLK, ACZ_SYNC D29 HDA_SYNC, SPKR P1 HDA_SPKR, ACZ_RST# C30 HDA_RST#, G30 HDA_SDIN0, F30 HDA_SDIN1, E32 HDA_SDIN2, F32 HDA_SDIN3, ACZ_SDOUT B29 HDA_SDO, GPIO33 H32 HDA_DOCK_EN# / GPIO33, J30 HDA_DOCK_RST# / GPIO13

38 SPKR
38 ICH_AZ_CODEC_SDIN0
T37 PAD
T40 PAD
T43 PAD
35 KB_LED_DET

SATA: SATA0RXN AK7, SATA0RXP AK6, SATA0TXN AK11, SATA0TXP AK9, SATA1RXN AH6, SATA1RXP AH5, SATA1TXN AH9, SATA1TXP AH8, SATA2RXN AF11, SATA2RXP AF9, SATA2TXN AF7, SATA2TXP AF6, SATA3RXN AH3, SATA3RXP AH1, SATA3TXN AE3, SATA3TXP AE1, SATA4RXN AD9, SATA4RXP AD8, SATA4TXN AD6, SATA4TXP AD5, SATA5RXN AD3, SATA5RXP AD1, SATA5TXN AB3, SATA5TXP AB1, SATAICOMPO AF16, SATAICOMPI AF15, SATALED# T3, SATA0GP / GPIO21 Y9, SATA1GP / GPIO19 V1

SATA_RX0- 34
SATA_RX0+ 34
SATA_TX0-_C 34
SATA_TX0+_C 34
HDD

SATA_RX1- 34
SATA_RX1+ 34
SATA_TX1-_C 34
SATA_TX1+_C 34
ODD

Notes : Put AC Coupling Cap. near device side. As DG1.1, Page 299, the series capacitors may be placed at any point on the traces between PCH and the Serial ATA connector. However, it is recommended that they should be close to the connector for optimal signal quality

SATA_RX5- 33
SATA_RX5+ 33
SATA_TX5-_C 33
SATA_TX5+_C 33
E-SATA

Notes : FIS-based Port Multiplier support on SATA Ports 4 and 5 in AHCI/RAID mode.

within 500 mils of the PCH
SATA_COMP R213 37.4/F +1.05V_PCH

PU 10K to +3.3V_RUN at Page 38

SATA_ACT# 36

R188 10K
R537 10K
+3.3V_RUN

JTAG: T93 PAD PCH_JTAG_TCK_BUF M3 JTAG_TCK, T88 PAD PCH_JTAG_TMS K3 JTAG_TMS, T97 PAD PCH_JTAG_TDI K1 JTAG_TDI, T99 PAD PCH_JTAG_TDO J2 JTAG_TDO, T95 PAD PCH_JTAG_RST# J4 TRST#

SPI: 30 PCH_SPI_CLK BA2 SPI_CLK, 30 PCH_SPI_CS0# AV3 SPI_CS0#, T13 PAD AY3 SPI_CS1#, 30 PCH_SPI_SI AY1 SPI_MOSI, 30 PCH_SPI_SO AV1 SPI_MISO

IbexPeak-M_R1P0

No Reboot strap.

SPKR	Low = Default. High = No Reboot.

+3.3V_RUN R545 *1K_NC SPKR

Scott_0630:Change R545 footprint from RC0402-C to RC0402.

R261 *1K_NC GPIO33

Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode.This signal should be only asserted lowthrough an external pull-down in manufacturing or debug environments ONLY.

6/2: Change R261 from 10K_NC to 1K_NC according to Intel design guide 1.51

6/2: NC JTAG resistors as PCH is in QT stage

+3.3V_SUS

Res. of TDI near PCH

R236 *200_NC
R251 *200_NC
R263 *200_NC
R259 *20K_NC

PCH_JTAG_TMS
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_RST#

R546 *100_NC
R547 *100_NC
R549 *100_NC
R548 *10K_NC

Scott_0707: Reserver PCH_JTAG_RST# circuit as review.

NC all Res. when PCH is production stage.

Res. of TDO
PCH ES1 stage : NC
PCH ES2 stage : pop

Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

Scott_0703 : Note : Delete pull up 1.05V according to Intel change notice! (Reserved for debug purpose)

PCH_JTAG_TCK_BUF
R544 51

QUANTA COMPUTER

Title	PCH 2/6(SATA_SPI)	
Size	Document Number RM5	Rev 3A
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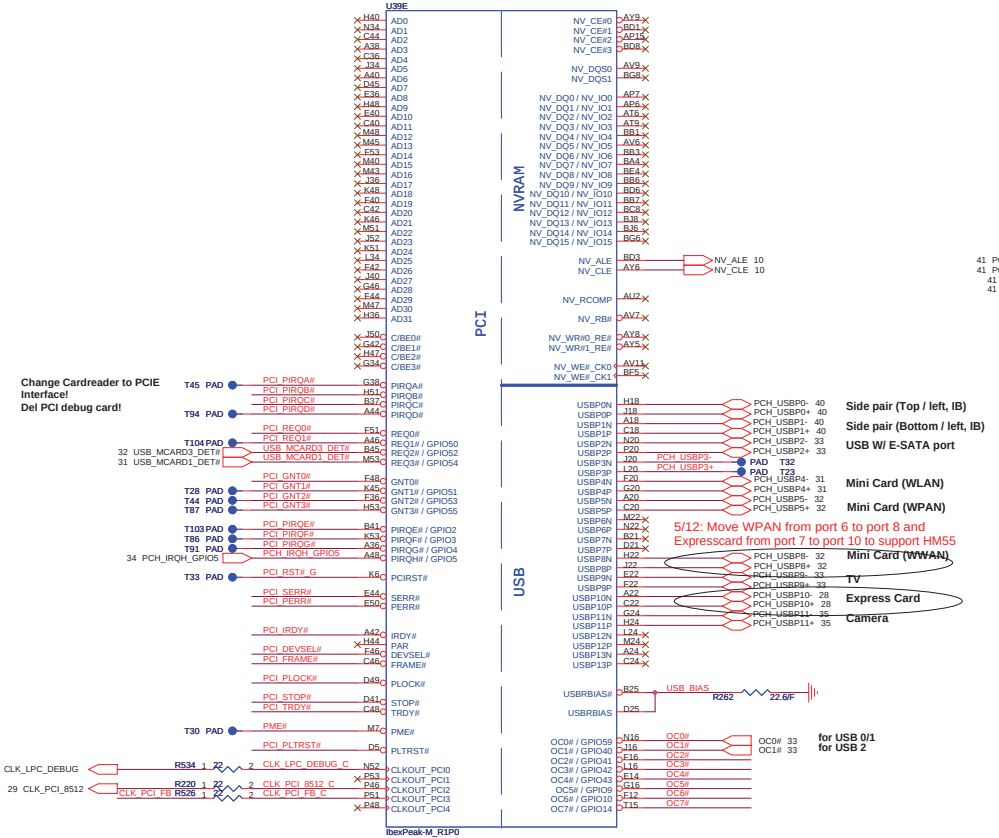
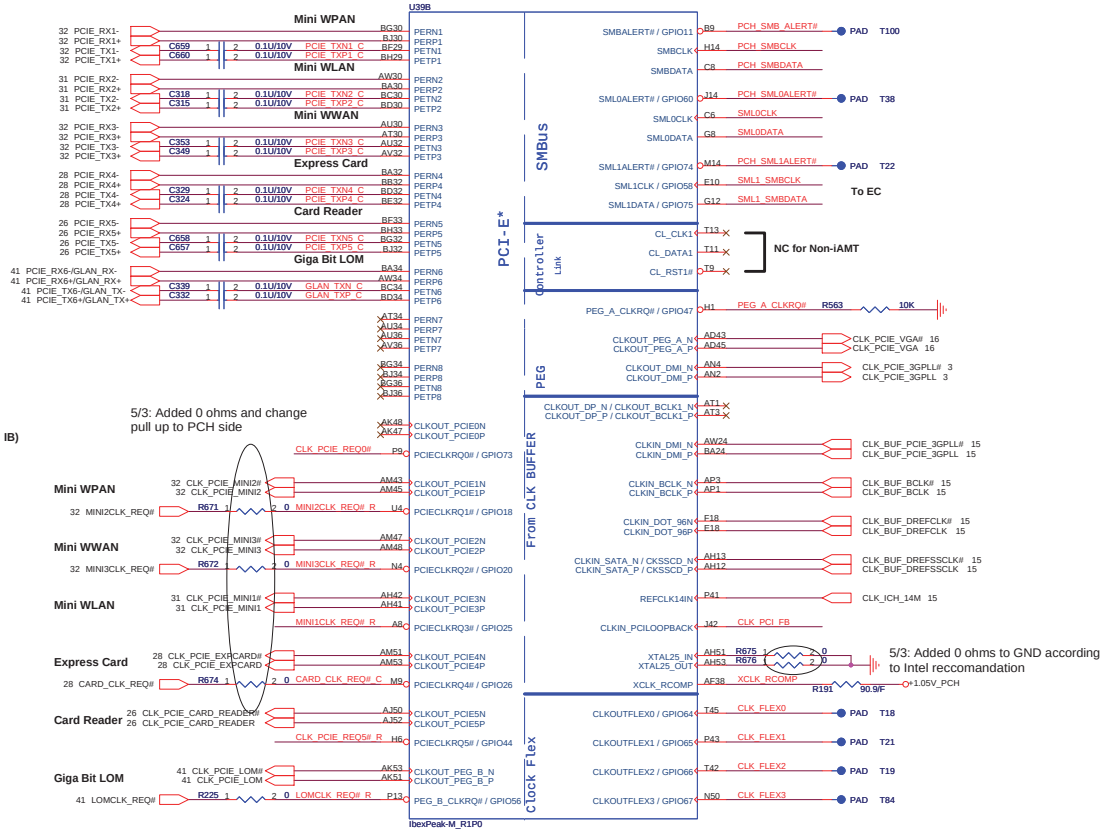
IBEX PEAK-M (PCI,USB,NVRAM)



IBEX PEAK-M (PCI-E,SMBUS,CLK)



5/13: Added MOSFET Q81 to prevent leakage from 3.3V_SUS to cardreader during S3

5/4: Added MOSFET Q80 to prevent leakage from 3.3V_SUS to cardreader during S3

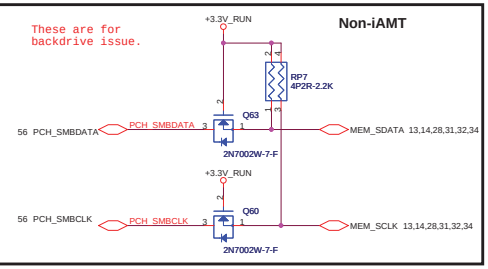
5/12: Depop R226 and R229 as BIOS decided to boot from SPI ROM connected to PCH

5/19: Update BIOS strap table

Boot BIOS Strap		
PCI_GNT1#	PCI_GNT0#	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT3#	0 = A16 swap override/Top-Block Swap Override enabled 1 = Default

4/28: Change polarity to prevent leakage



QUANTA COMPUTER

Title	PCH 3/6(PCI_SMBUS_CLK)	
Size	Document Number RM5	Rev 3A
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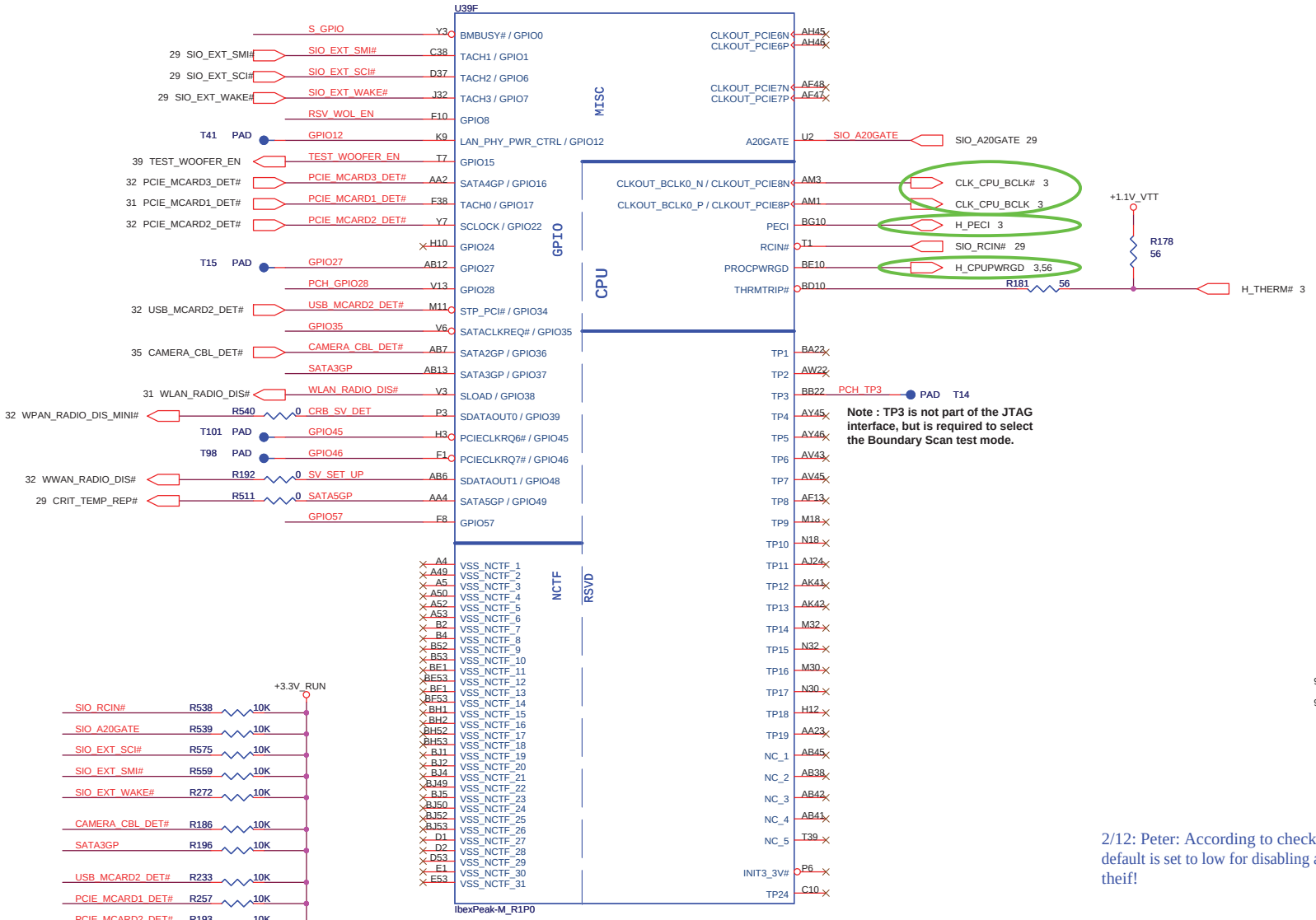
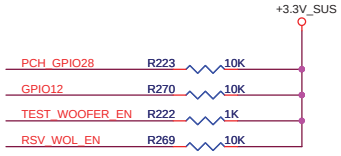
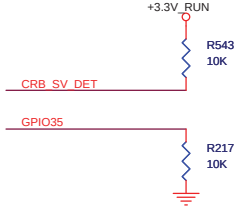
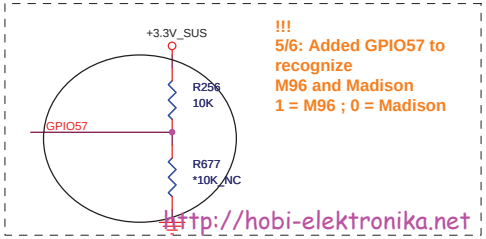
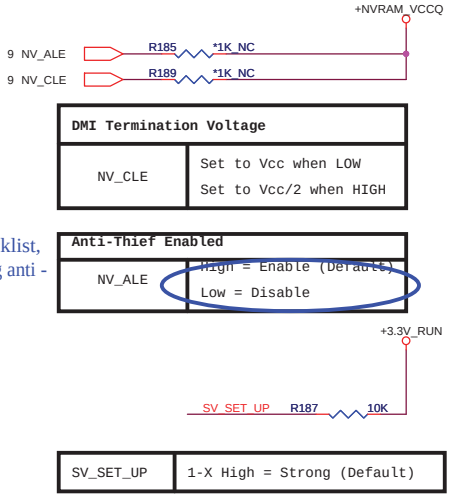
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)











2/12: Peter: According to checklist, default is set to low for disabling anti - theif!

QUANTA COMPUTER

Title	PCH 4/6(GPIO)	
Size	Document Number RM5	Rev 3A
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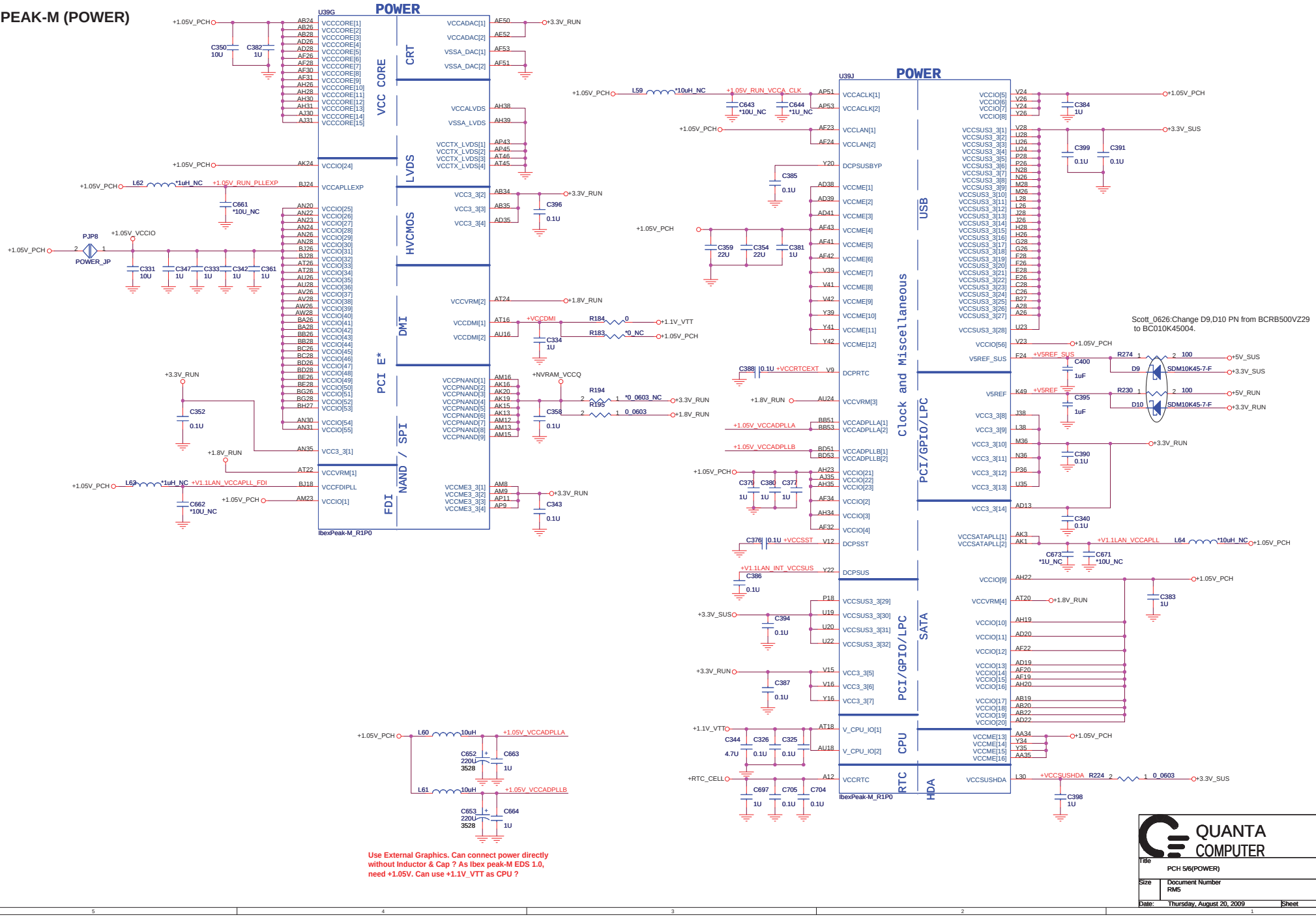
IBEX PEAK-M (POWER)



QUANTA COMPUTER

Title	PCH 5/6(POWER)	
Size	Document Number RM5	Rev 3A
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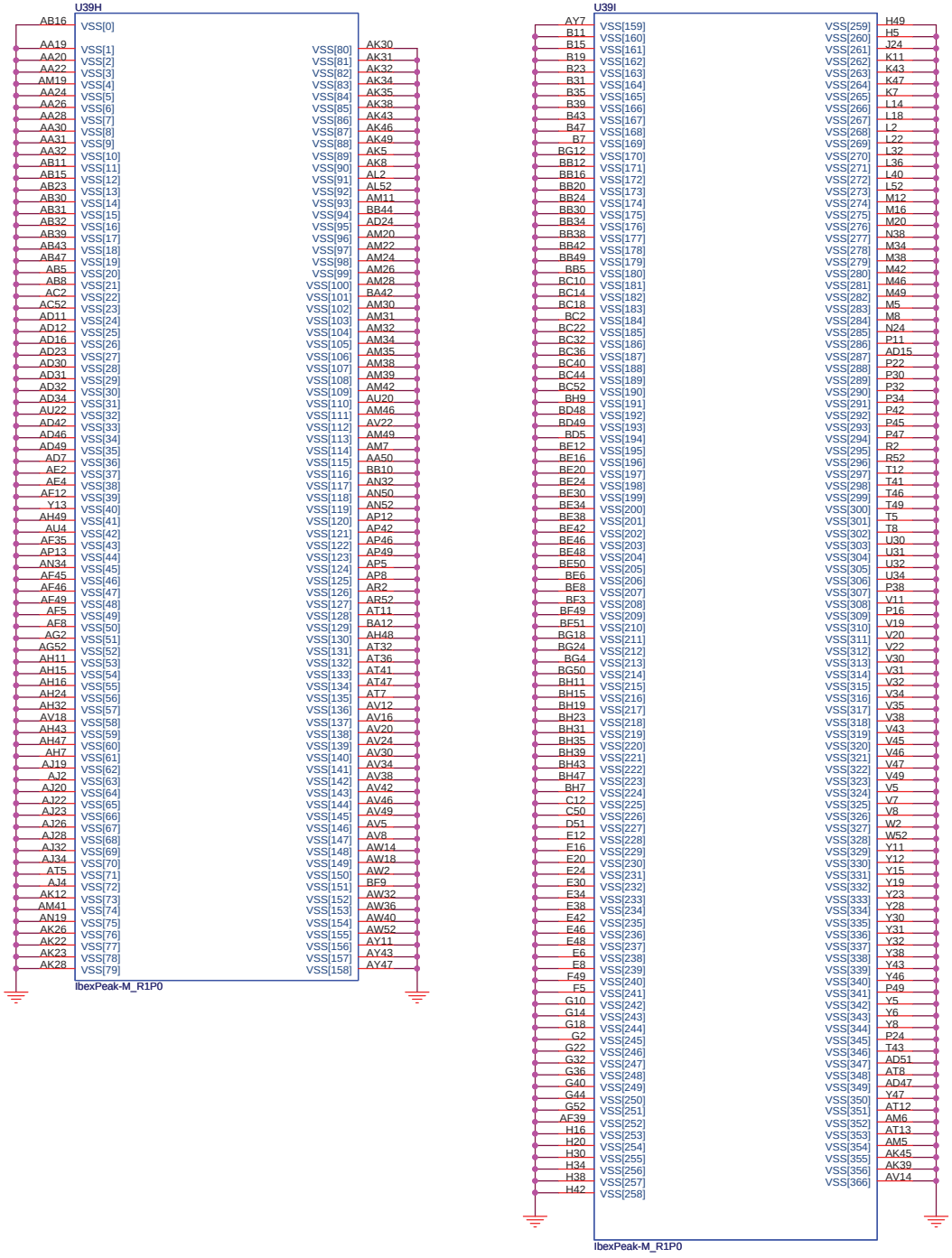
IBEX PEAK-M (GND)



QUANTA COMPUTER

Title	PCH 6/6(GND)	
Size	Document Number RM5	Rev 3A
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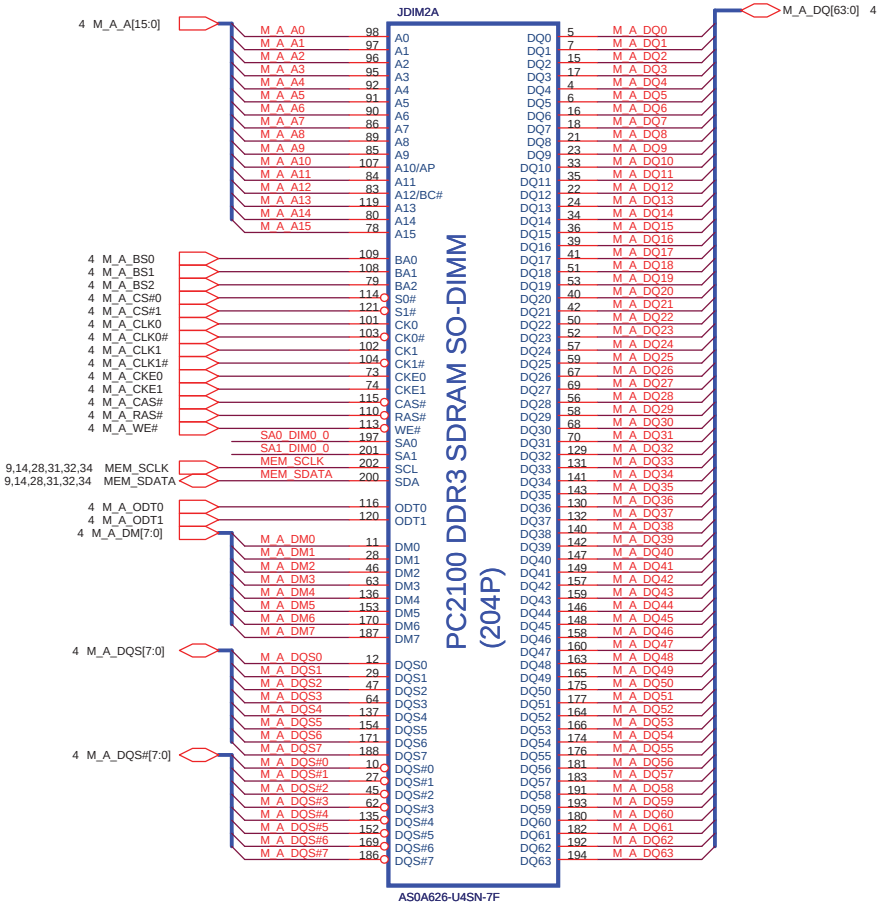
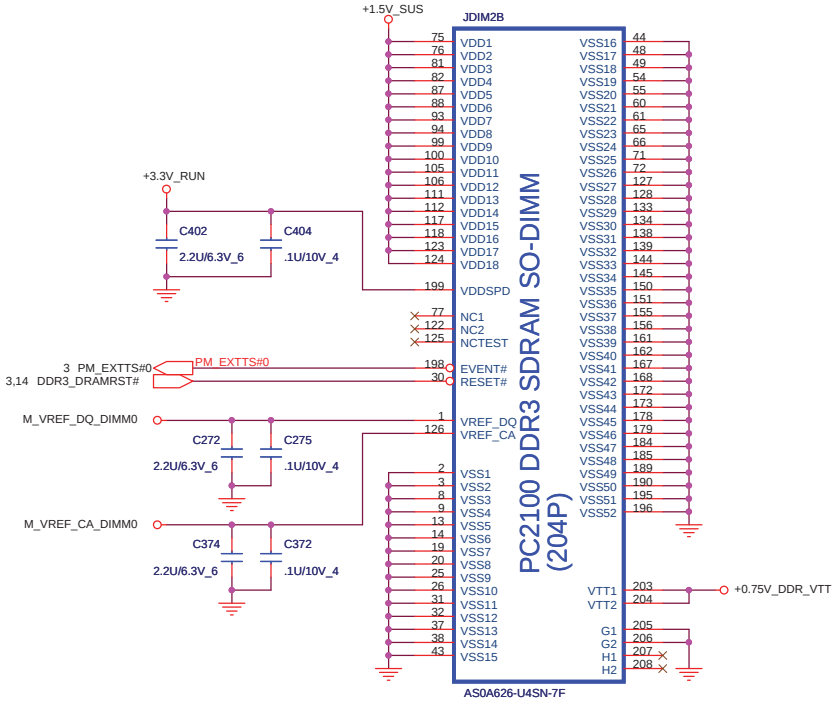
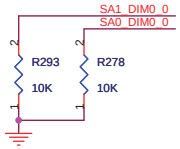
5/13: Change connector from Tyco to Foxconn to avoid shortage



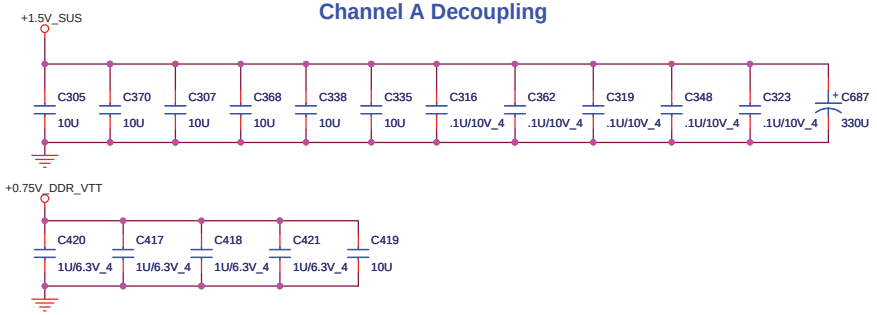
Channel A





Note:
If SA1_DIM0 = 0, SA0_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA1_DIM0 = 0, SA0_DIM0 = 1
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Channel A Decoupling



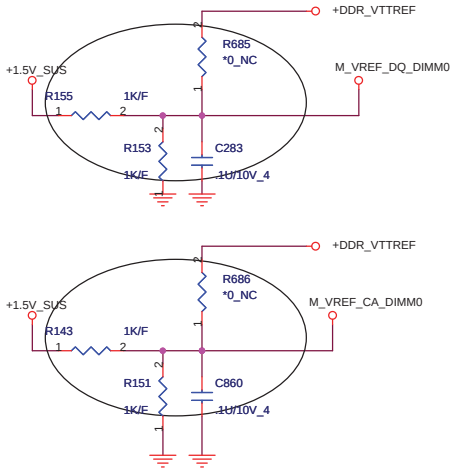
For CH A SO-DIMM VREF_DQ for M2

Delete according to Intel Design Change

M1 VREF

5/18: Separate voltage divider for M_VREF_DQ_DIMM0 and M_VREF_CA_DIMM0 to follow Intel CRB design

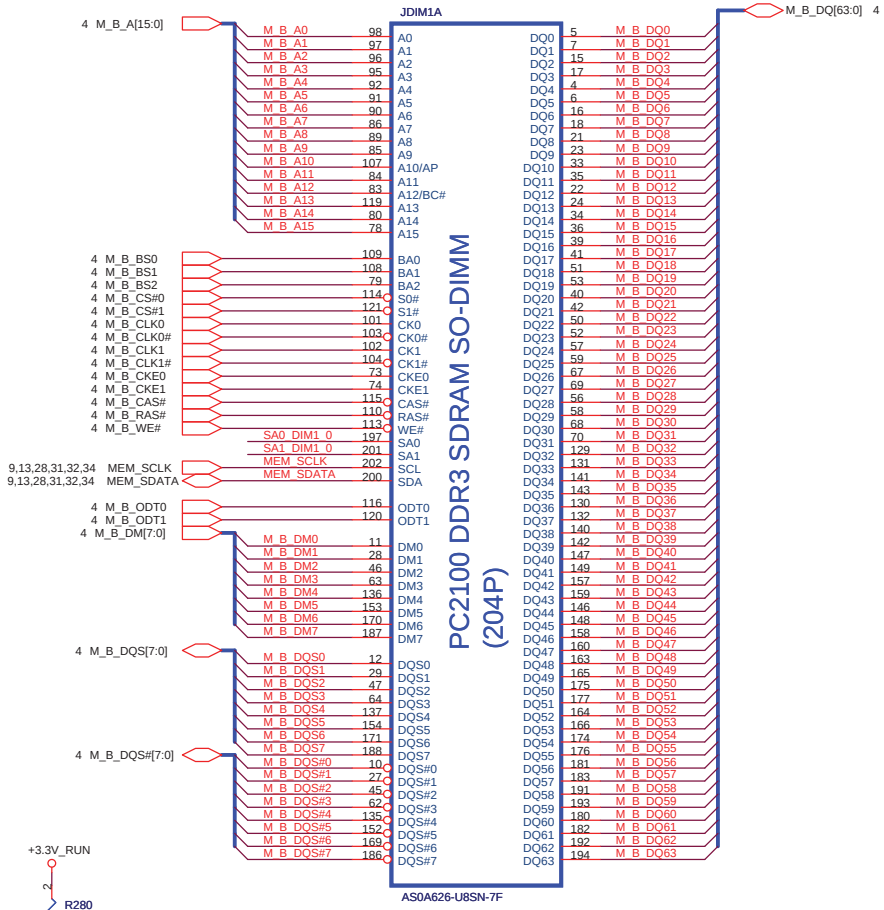
6/02: Change M1 from voltage regulator to voltage divider

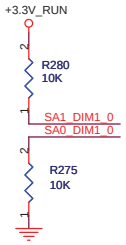


QUANTA COMPUTER

Title	DDR3 DIMM-A	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 13 of 61	

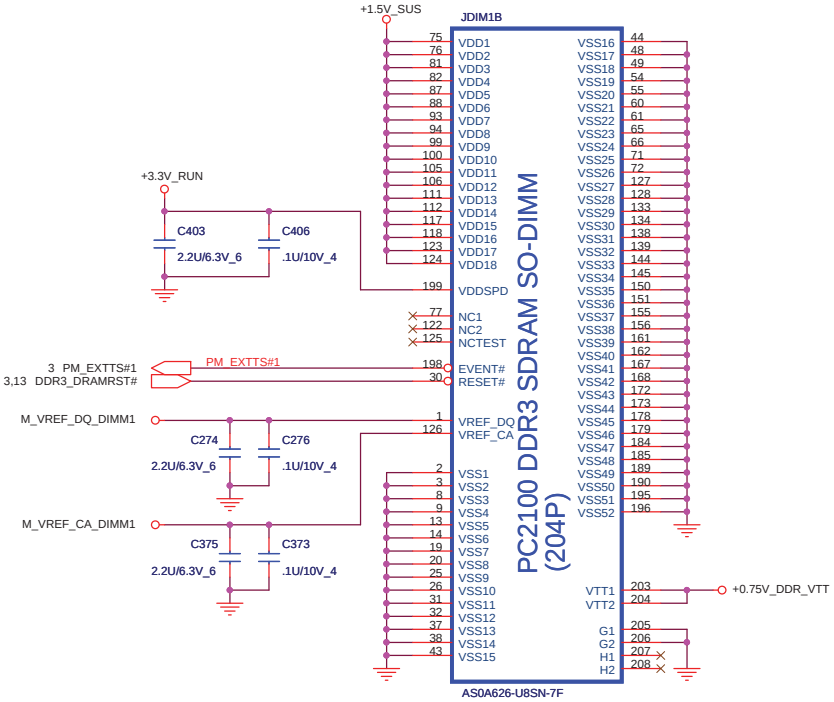
5/13: Change connector from Tyco to Foxconn to avoid shortage



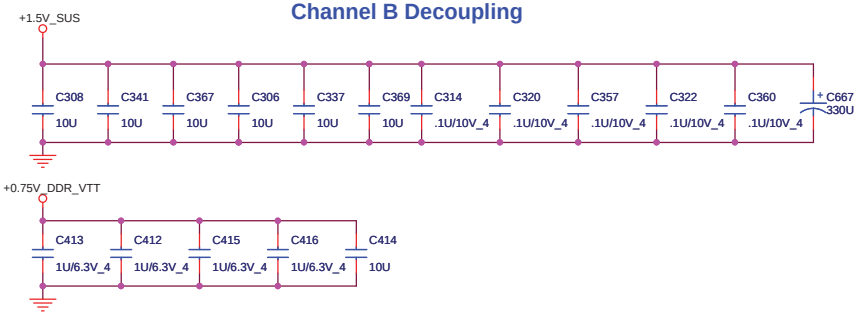


Note:
If SA1_DIM1 = 1, SA0_DIM1 = 0
SO-DIMMA SPD Address is 0xA4
SO-DIMMA TS Address is 0x34
If SA1_DIM1 = 1, SA0_DIM1 = 1
SO-DIMMA SPD Address is 0xA6
SO-DIMMA TS Address is 0x36

Channel B



Channel B Decoupling



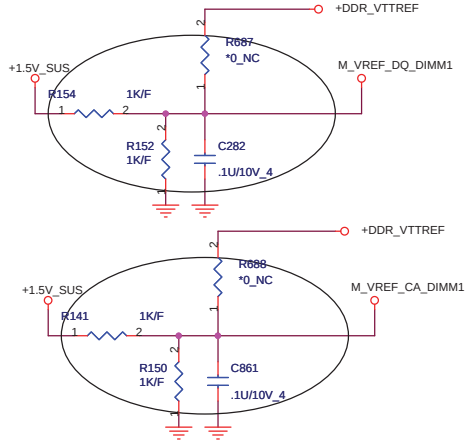
For CH B SO-DIMM VREF_DQ for M2

Delete according to Intel Design Change

M1 VREF

5/18: Separate voltage divider for M_VREF_DQ_DIMM1 and M_VREF_CA_DIMM1 to follow Intel CRB design

6/02: Change M1 from voltage regulator to voltage divider



QUANTA COMPUTER

Title	DDR3 DIMM-B	
Size	Document Number RM5	Rev 3A
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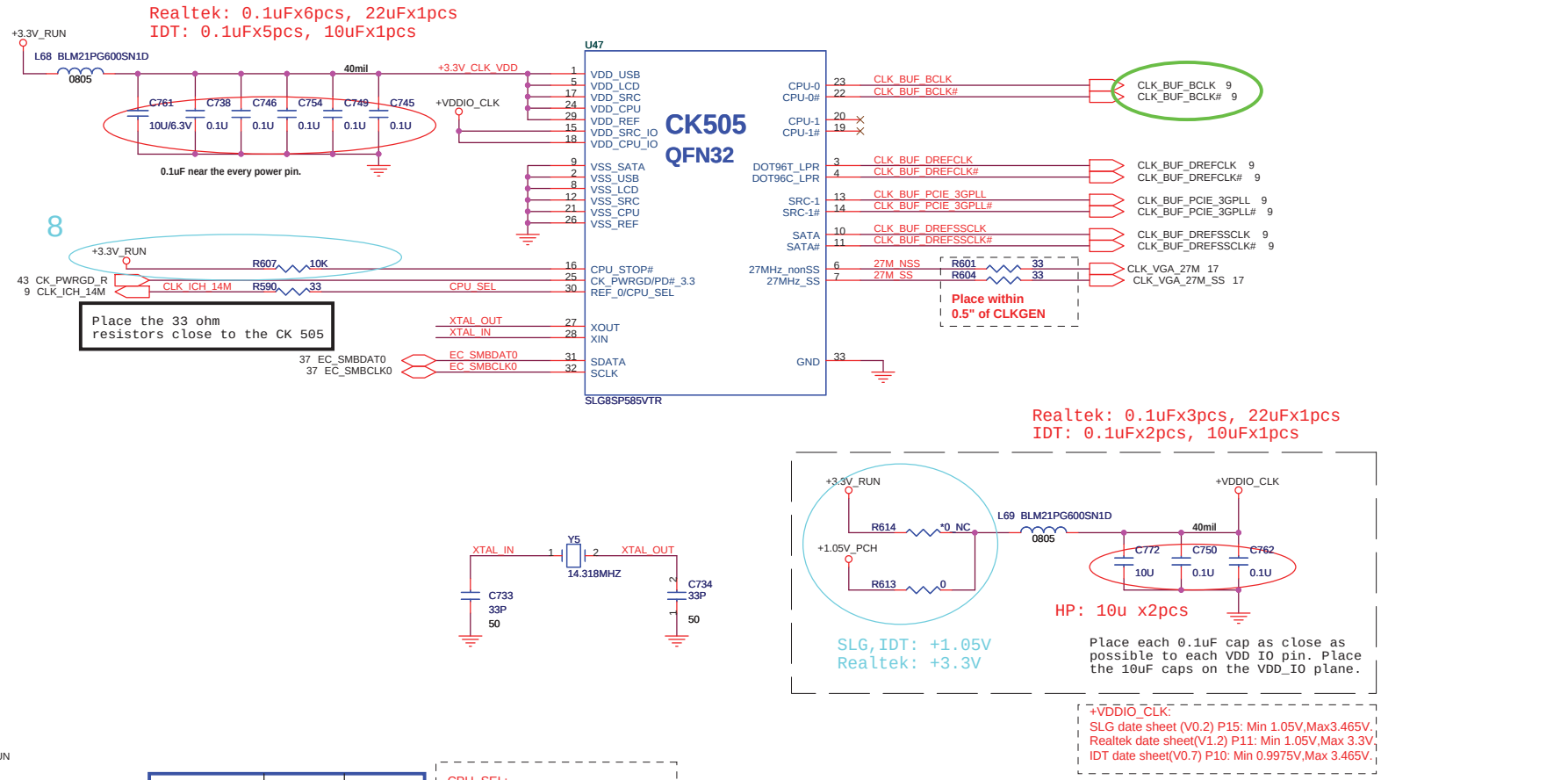

QUANTA COMPUTER

Title	CLOCK GENERATOR	
Size	Document Number RM5	Rev 3A
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ASIC	PN	100-CK	QCI P/N
M96-M2 XT A13	216-0729051	100-CK3186	AJ072900T08
M97-M2 LP A11	216-0731001	100-CG1806	AJ073100T01

U29A

3 PCIE_MTX_GRX_P[0..15]
3 PCIE_MTX_GRX_N[0..15]

PCIE_MRX_GTX_P[0..15] 3
PCIE_MRX_GTX_N[0..15] 3

PCIE_MTX_GRX_P0	AA38	PCIE_RX0P	PCIE_TX0P	Y33	PCIE_MRX_GTX_C_P0	PCIE_MRX_GTX_C_P0	C189	0.1U	PCIE_MRX_GTX_P0
PCIE_MTX_GRX_N0	Y37	PCIE_RX0N	PCIE_TX0N	Y32	PCIE_MRX_GTX_C_N0	PCIE_MRX_GTX_C_P1	C188	0.1U	PCIE_MRX_GTX_P1
PCIE_MTX_GRX_P1	Y35	PCIE_RX1P	PCIE_TX1P	W33	PCIE_MRX_GTX_C_P1	PCIE_MRX_GTX_C_P2	C205	0.1U	PCIE_MRX_GTX_P2
PCIE_MTX_GRX_N1	W36	PCIE_RX1N	PCIE_TX1N	W32	PCIE_MRX_GTX_C_N1	PCIE_MRX_GTX_C_P3	C176	0.1U	PCIE_MRX_GTX_P3
PCIE_MTX_GRX_P2	W38	PCIE_RX2P	PCIE_TX2P	U33	PCIE_MRX_GTX_C_P2	PCIE_MRX_GTX_C_P4	C212	0.1U	PCIE_MRX_GTX_P4
PCIE_MTX_GRX_N2	V37	PCIE_RX2N	PCIE_TX2N	U32	PCIE_MRX_GTX_C_N2	PCIE_MRX_GTX_C_P5	C204	0.1U	PCIE_MRX_GTX_P5
PCIE_MTX_GRX_P3	V35	PCIE_RX3P	PCIE_TX3P	U30	PCIE_MRX_GTX_C_P3	PCIE_MRX_GTX_C_P6	C218	0.1U	PCIE_MRX_GTX_P6
PCIE_MTX_GRX_N3	U36	PCIE_RX3N	PCIE_TX3N	U29	PCIE_MRX_GTX_C_N3	PCIE_MRX_GTX_C_P7	C216	0.1U	PCIE_MRX_GTX_P7
PCIE_MTX_GRX_P4	U38	PCIE_RX4P	PCIE_TX4P	T33	PCIE_MRX_GTX_C_P4	PCIE_MRX_GTX_C_P8	C222	0.1U	PCIE_MRX_GTX_P8
PCIE_MTX_GRX_N4	T37	PCIE_RX4N	PCIE_TX4N	T32	PCIE_MRX_GTX_C_N4	PCIE_MRX_GTX_C_P9	C211	0.1U	PCIE_MRX_GTX_P9
PCIE_MTX_GRX_P5	T35	PCIE_RX5P	PCIE_TX5P	T30	PCIE_MRX_GTX_C_P5	PCIE_MRX_GTX_C_P10	C230	0.1U	PCIE_MRX_GTX_P10
PCIE_MTX_GRX_N5	R36	PCIE_RX5N	PCIE_TX5N	T29	PCIE_MRX_GTX_C_N5	PCIE_MRX_GTX_C_P11	C221	0.1U	PCIE_MRX_GTX_P11
PCIE_MTX_GRX_P6	R38	PCIE_RX6P	PCIE_TX6P	P33	PCIE_MRX_GTX_C_P6	PCIE_MRX_GTX_C_P12	C245	0.1U	PCIE_MRX_GTX_P12
PCIE_MTX_GRX_N6	P37	PCIE_RX6N	PCIE_TX6N	P32	PCIE_MRX_GTX_C_N6	PCIE_MRX_GTX_C_P13	C247	0.1U	PCIE_MRX_GTX_P13
PCIE_MTX_GRX_P7	P35	PCIE_RX7P	PCIE_TX7P	P30	PCIE_MRX_GTX_C_P7	PCIE_MRX_GTX_C_P14	C249	0.1U	PCIE_MRX_GTX_P14
PCIE_MTX_GRX_N7	N36	PCIE_RX7N	PCIE_TX7N	P29	PCIE_MRX_GTX_C_N7	PCIE_MRX_GTX_C_P15	C251	0.1U	PCIE_MRX_GTX_P15
PCIE_MTX_GRX_P8	N38	PCIE_RX8P	PCIE_TX8P	N33	PCIE_MRX_GTX_C_P8	PCIE_MRX_GTX_C_N0	C194	0.1U	PCIE_MRX_GTX_N0
PCIE_MTX_GRX_N8	M37	PCIE_RX8N	PCIE_TX8N	N32	PCIE_MRX_GTX_C_N8	PCIE_MRX_GTX_C_N1	C179	0.1U	PCIE_MRX_GTX_N1
PCIE_MTX_GRX_P9	M35	PCIE_RX9P	PCIE_TX9P	N30	PCIE_MRX_GTX_C_P9	PCIE_MRX_GTX_C_N2	C207	0.1U	PCIE_MRX_GTX_N2
PCIE_MTX_GRX_N9	L36	PCIE_RX9N	PCIE_TX9N	N29	PCIE_MRX_GTX_C_N9	PCIE_MRX_GTX_C_N3	C171	0.1U	PCIE_MRX_GTX_N3
PCIE_MTX_GRX_P10	L38	PCIE_RX10P	PCIE_TX10P	L33	PCIE_MRX_GTX_C_P10	PCIE_MRX_GTX_C_N4	C215	0.1U	PCIE_MRX_GTX_N4
PCIE_MTX_GRX_N10	K37	PCIE_RX10N	PCIE_TX10N	L32	PCIE_MRX_GTX_C_N10	PCIE_MRX_GTX_C_N5	C195	0.1U	PCIE_MRX_GTX_N5
PCIE_MTX_GRX_P11	K35	PCIE_RX11P	PCIE_TX11P	L30	PCIE_MRX_GTX_C_P11	PCIE_MRX_GTX_C_N6	C219	0.1U	PCIE_MRX_GTX_N6
PCIE_MTX_GRX_N11	J36	PCIE_RX11N	PCIE_TX11N	L29	PCIE_MRX_GTX_C_N11	PCIE_MRX_GTX_C_N7	C217	0.1U	PCIE_MRX_GTX_N7
PCIE_MTX_GRX_P12	J38	PCIE_RX12P	PCIE_TX12P	K33	PCIE_MRX_GTX_C_P12	PCIE_MRX_GTX_C_N8	C223	0.1U	PCIE_MRX_GTX_N8
PCIE_MTX_GRX_N12	H37	PCIE_RX12N	PCIE_TX12N	K32	PCIE_MRX_GTX_C_N12	PCIE_MRX_GTX_C_N9	C208	0.1U	PCIE_MRX_GTX_N9
PCIE_MTX_GRX_P13	H35	PCIE_RX13P	PCIE_TX13P	J33	PCIE_MRX_GTX_C_P13	PCIE_MRX_GTX_C_N10	C231	0.1U	PCIE_MRX_GTX_N10
PCIE_MTX_GRX_N13	G36	PCIE_RX13N	PCIE_TX13N	J32	PCIE_MRX_GTX_C_N13	PCIE_MRX_GTX_C_N11	C220	0.1U	PCIE_MRX_GTX_N11
PCIE_MTX_GRX_P14	G38	PCIE_RX14P	PCIE_TX14P	K30	PCIE_MRX_GTX_C_P14	PCIE_MRX_GTX_C_N12	C246	0.1U	PCIE_MRX_GTX_N12
PCIE_MTX_GRX_N14	F37	PCIE_RX14N	PCIE_TX14N	K29	PCIE_MRX_GTX_C_N14	PCIE_MRX_GTX_C_N13	C248	0.1U	PCIE_MRX_GTX_N13
PCIE_MTX_GRX_P15	F35	PCIE_RX15P	PCIE_TX15P	H33	PCIE_MRX_GTX_C_P15	PCIE_MRX_GTX_C_N14	C250	0.1U	PCIE_MRX_GTX_N14
PCIE_MTX_GRX_N15	F37	PCIE_RX15N	PCIE_TX15N	H32	PCIE_MRX_GTX_C_N15	PCIE_MRX_GTX_C_N15	C252	0.1U	PCIE_MRX_GTX_N15

PCI EXPRESS INTERFACE

CLOCK

9 CLK_PCIE_VGA
9 CLK_PCIE_VGA#
AB35 PCIE_REFCLKP
AA36 PCIE_REFCLKN

!!! Park, Madison : Pop 0 Ohm
M96: depop 0 ohm

R426 *0_NC

AJ21 NC#1
AK21 NC#2
AH16 PWRGOOD

AA30 PERSTB

3,9,26,28,29,31,32,41,56 PLTRST#
R100 0 PERST#

CALIBRATION

PCIE_CALRP Y30 R101 1.27K
PCIE_CALRN Y29 R99 2K/F +PCIE_VDDC

216-0729051(M96-M2 XT)

QUANTA COMPUTER

Title	M96XT_PCIE		
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Memory Straps		RAM_ TYPE_CFG3	RAM_ TYPE_CFG2	RAM_ TYPE_CFG1	RAM_ TYPE_CFG0
800 MHz 512MB(32M*16) Hynix_Tiva die	H5TQ5163MFR-12	1	1	1	1
reserve for Qimonda		1	1	1	0
reserve for Samsung		1	1	0	1
800 MHz 1GB(64M*16) Hynix_Orion die	H5TQ1G63BFR-12C	1	0	1	1
800 MHz 1GB(64M*16) Qimonda_A1 die	IDGH1G-04A1F1C-16X	1	0	1	0
800 MHz 1GB(64M*16) Samsung_E die	K4W1G1646E-HC12	1	0	0	1

Note : Required Frequency = 800 MHz

MEMORY APERTURE SIZE SELECT			
MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0
256MB	0	0	1
64MB	0	1	0

CONFIGURATION STRAPS			
STRAPS	PIN	DESCRIPTION	SET
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0 = 50% Tx output swing 1 = Full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = Disable ; 1 = Enable	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0
GPIO_5_AC_BATT (M96-M2)	GPIO5	1 = AC (Performance mode) 0 = Battery saving mode	1
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 = Disable ; 1 = Enable	0
AUD[1] AUD[0]	VGAHSYNC VGAVSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	11
VIP_DEVICE_STRAP_EN	BIOS_ROM_EN	VIP Device Strap Enable 0 = Disable ; 1 = Enable	0

VRAM TYPE

APERTURE SIZE

!!! NC when M92-M2

Layout Note: Place 150 ohm termination resistors close to ATI CHIP.

(1.8V @ 70mA AVDD)

(1.8V @ 45mA VDD1DI)

(1.8V @ 40mA VDD2DI)

(1.8V @ 20mA A2VDDQ)

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

(1.8V @ 120mA DPLL_PVDD)

!!! (1.1V @ 150mA DPLL_VDDC) (1.0V @ 150mA DPLL_VDDC for M97)

(1.8V @ 20mA TSVDD)

Reserve 0 ohm for Dual mode DDC/AUX

HDMI

DP

LVDS

CRT

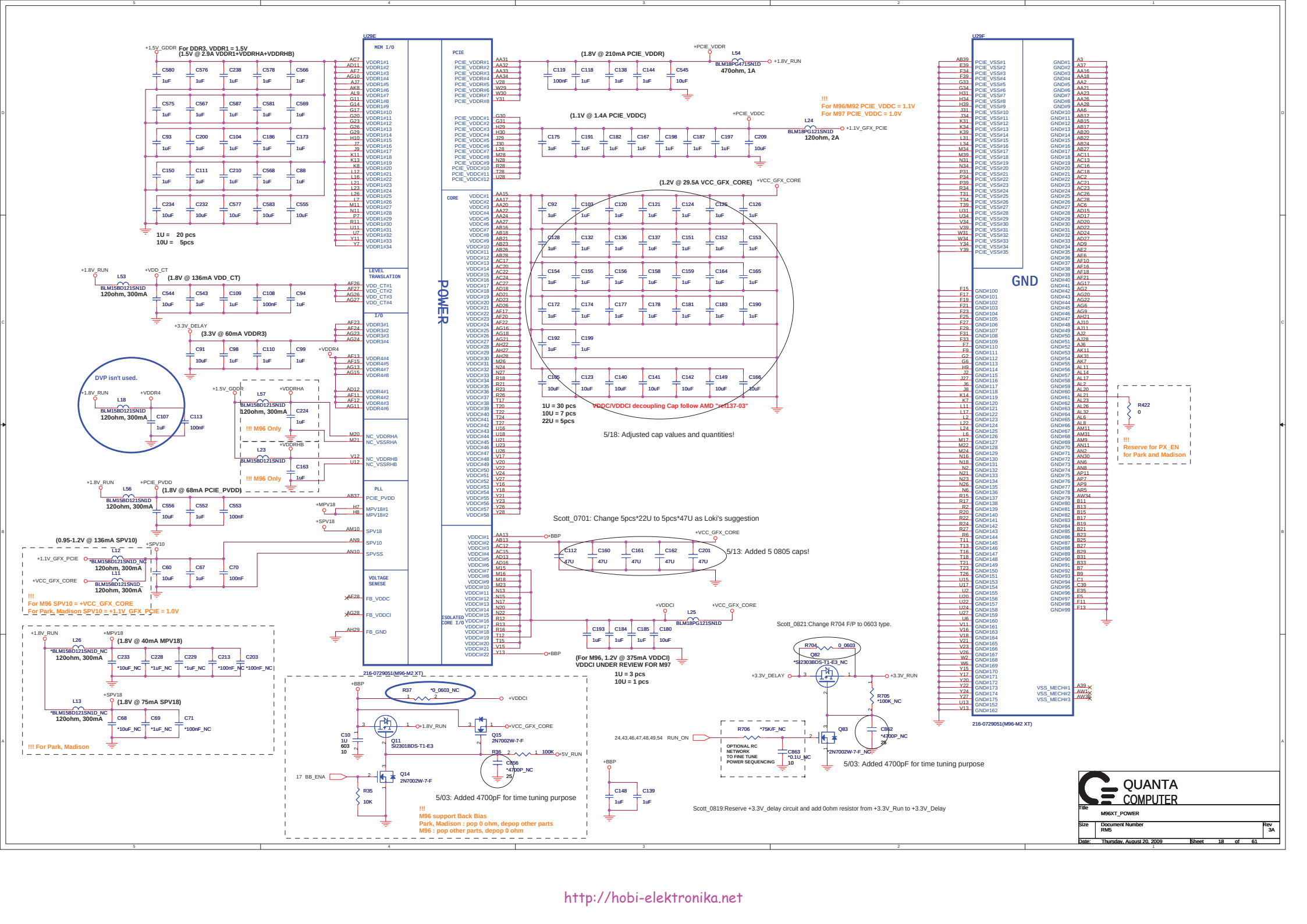
DDC6CLK/DDC6DATA support internal HDCP(High-bandwidth Digital Content Protection) function.

Scott_0703:Delete Spread Spectrum XTAL circuit as placement required of thermal issue.

216-0729051(M96-M2 XT)

QUANTA COMPUTER

Title	M96XT_IO & STRAP	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 17 of 61	



!!!
For M96/92, DPx_VDD10 = 1.1V
For M97 DPx_VDD10 = 1.0V

DPC & DPD aren't used.

U29H

DP C/D POWER | DP A/B POWER

+DPC_VDD18
AP20 DPC_VDD18#1
AP21 DPC_VDD18#2
+1.1V_GFX_PCIE
AP13 DPC_VDD10#1
AT13 DPC_VDD10#2
C55 *100nF_NC
AN17 DPC_VSSR#1
AP16 DPC_VSSR#2
AP17 DPC_VSSR#3
AW14 DPC_VSSR#4
AW16 DPC_VSSR#5
+DPD_VDD18
AP22 DPD_VDD18#1
AP23 DPD_VDD18#2
+1.1V_GFX_PCIE
AP14 DPD_VDD10#1
AP15 DPD_VDD10#2
C57 *100nF_NC
AN19 DPD_VSSR#1
AP18 DPD_VSSR#2
AP19 DPD_VSSR#3
AW20 DPD_VSSR#4
AW22 DPD_VSSR#5

DPA_VDD18#1 DPA_VDD18#2 ← +DPA_VDD18 (AN24, AP24)
DPA_VDD10#1 DPA_VDD10#2 ← +DPA_VDD10 (AP31, AP32) (1.1V @ 200mA DPA_VDD10)
L48 BLM15BD121SN1D 120ohm, 300mA
C519 100nF, C520 1uF, C521 10uF
+1.1V_GFX_PCIE
DPA for HDMI
DPA_VSSR#1 DPA_VSSR#2 DPA_VSSR#3 DPA_VSSR#4 DPA_VSSR#5 ← AN27 AP27 AP28 AW24 AW26

DPB_VDD18#1 DPB_VDD18#2 ← +DPB_VDD18 (AP25, AP26)
DPB_VDD10#1 DPB_VDD10#2 ← +DPB_VDD10 (AN33, AP33) (1.1V @ 200mA DPB_VDD10)
L16 BLM15BD121SN1D 120ohm, 300mA
C78 100nF, C77 1uF, C83 10uF
+1.1V_GFX_PCIE
DPB for DP
DPB_VSSR#1 DPB_VSSR#2 DPB_VSSR#3 DPB_VSSR#4 DPB_VSSR#5 ← AN29 AP29 AP30 AW30 AW32

!!! For M97 Only

+DPA_VDD18 (1.8V @ 110mA DPA_VDD18)
L15 *BLM15BD121SN1D_NC 120ohm, 300mA
C80 *100nF_NC, C74 *1uF_NC, C73 *10uF_NC
+1.8V_RUN

+DPB_VDD18 (1.8V @ 110mA DPB_VDD18)
L14 *BLM15BD121SN1D_NC 120ohm, 300mA
C79 *100nF_NC, C75 *1uF_NC, C72 *10uF_NC
+1.8V_RUN

+DPC_VDD18
R59 1 *0_NC 2 +1.8V_RUN
C82 *100nF_NC

+DPD_VDD18
R58 1 *0_NC 2 +1.8V_RUN
C81 *100nF_NC

(1.8V @ 400mA DPE_VDD18; 200mA for DPE/DPF respectively)
+DPE_VDD18
+1.8V_RUN → L19 BLM18PG600SN1D ~~60ohm, 500mA~~
C97 10uF, C95 1uF, C96 100nF

0504: Change L19 for low DCR 0.1ohm as AMD suggest.

150/F R425 AW18

DPCD_CALR | DPAB_CALR

DP E/F POWER | DP PLL POWER

DPE_VDD18#1 DPE_VDD18#2 ← AH34 AJ34
+DPE_VDD10
DPE_VDD10#1 DPE_VDD10#2 ← AL33 AM33

DPA_PVDD DPA_PVSS ← AW28 R424 150/F, AU28 AV27
+DPA_PVDD (1.8V @ 20 mA DPA_PVDD)
L49 BLM15BD121SN1D 120ohm, 300mA
C534 100nF, C532 1uF, C529 10uF
+1.8V_RUN

DPB_PVDD DPB_PVSS ← AV29 AR28
+DPB_PVDD (1.8V @ 20 mA DPB_PVDD)
L50 BLM15BD121SN1D 120ohm, 300mA
C537 100nF, C533 1uF, C531 10uF
+1.8V_RUN

DPE & DPF for LVDS

DPE_VSSR#1 DPE_VSSR#2 DPE_VSSR#3 DPE_VSSR#4 DPE_VSSR#5 ← AN34 AP39 AR39 AU37 AW35

DPC & DPD aren't used.
+1.8V_RUN
C535 *100nF_NC
C536 *100nF_NC

DPC_PVDD DPC_PVSS ← AU18 AV17
DPD_PVDD DPD_PVSS ← AV19 AR18

+DPE_VDD18
DPF_VDD18#1 DPF_VDD18#2 ← AE34 AG34

(1.1V @ 200mA DPE_VDD10; 100mA for DPE/DPF respectively)
+DPE_VDD10
+1.1V_GFX_PCIE → L17 BLM15BD121SN1D 120ohm, 300mA
C86 10uF, C84 1uF, C85 100nF
DPF_VDD10#1 DPF_VDD10#2 ← AK33 AK34

DPE_PVDD DPE_PVSS ← AM37 AN38
+DPE_PVDD (1.8V @ 40mA DPE_PVDD; 20mA for DPE/DPF respectively)
L55 BLM15BD121SN1D 120ohm, 300mA
C549 100nF, C548 1uF, C547 10uF
+1.8V_RUN

NC_DPF_PVDD NC_DPF_PVSS ← AL38 AM35

DPF_VSSR#1 DPF_VSSR#2 DPF_VSSR#3 DPF_VSSR#4 DPF_VSSR#5 ← AF39 AH39 AK39 AL34 AM34

150/F R438 AM39

DPEF_CALR

216-0729051(M96-M2 XT)

QUANTA COMPUTER

Title	M96XT_DP POWER	
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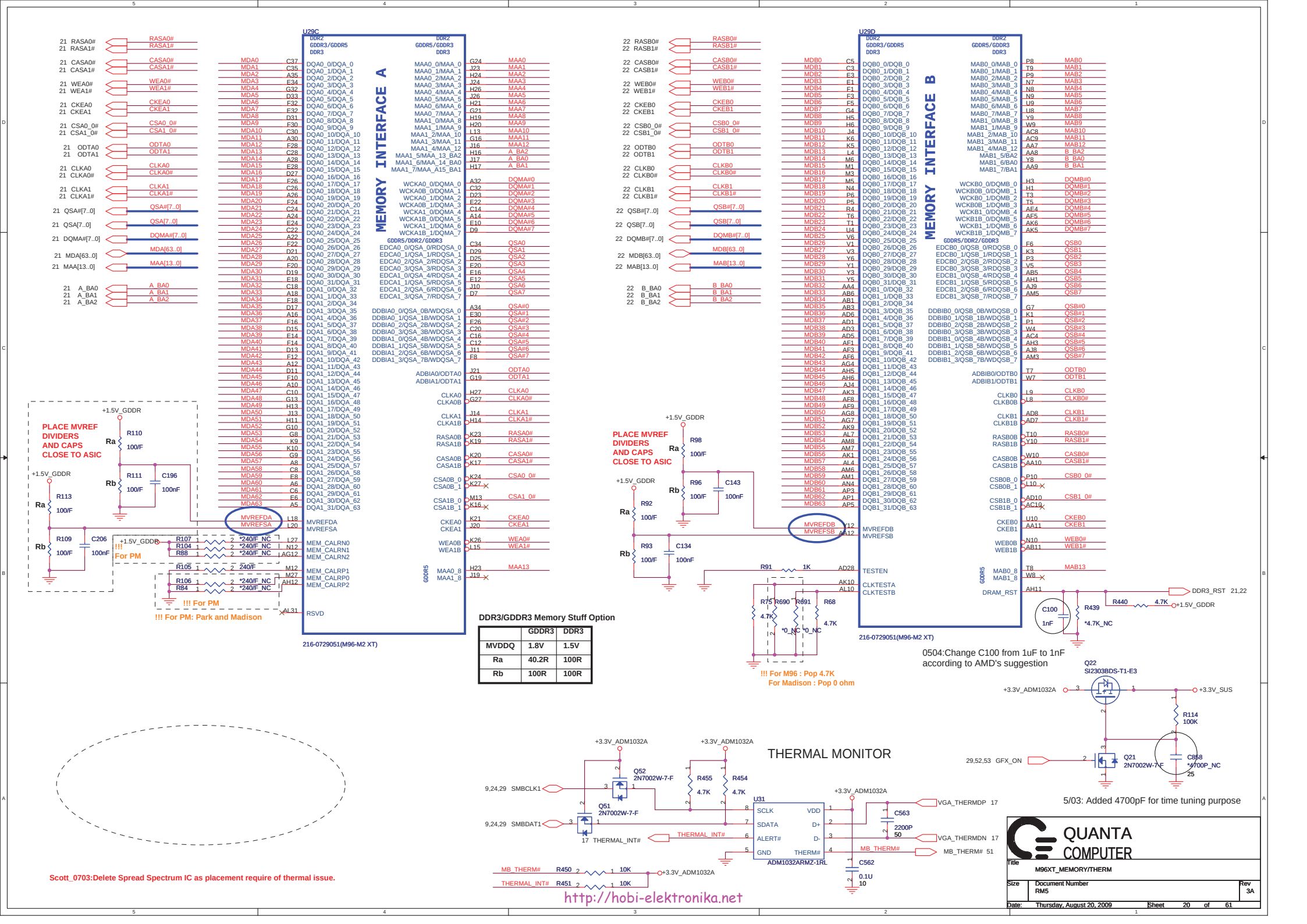
U29C
MEMORY INTERFACE A
DDR2 GDDR3/GDDR5 DDR3
DDR2 GDDR5/GDDR3 DDR3
216-0729051(M96-M2 XT)
U29D
MEMORY INTERFACE B
216-0729051(M96-M2 XT)
PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC
!!! For PM
!!! For PM: Park and Madison
!!! For M96 : Pop 4.7K
For Madison : Pop 0 ohm
DDR3/GDDR3 Memory Stuff Option
MVDDQ 1.8V 1.5V
Ra 40.2R 100R
Rb 100R 100R
0504:Change C100 from 1uF to 1nF according to AMD's suggestion
5/03: Added 4700pF for time tuning purpose
THERMAL MONITOR
ADM1032ARMZ-1RL
Scott_0703:Delete Spread Spectrum IC as placement require of thermal issue.
http://hobi-elektronika.net
QUANTA COMPUTER
Title M96XT_MEMORY/THERM
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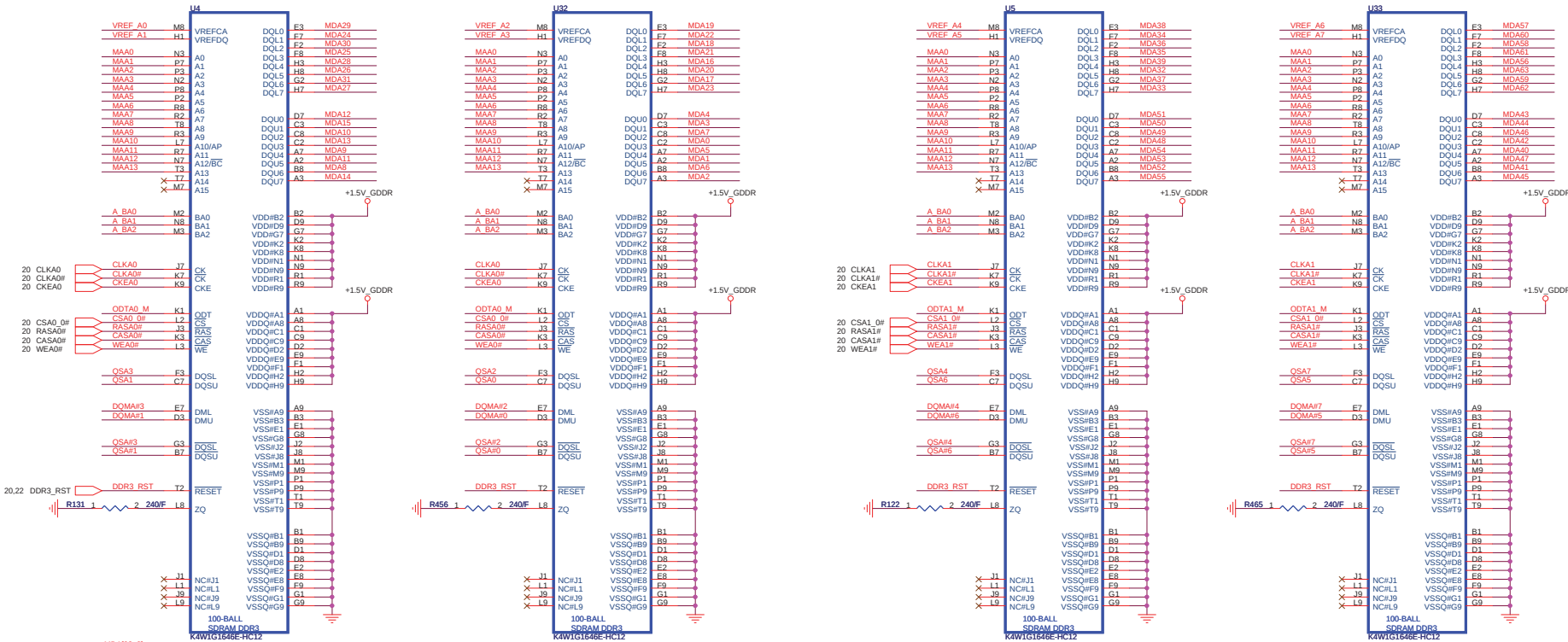
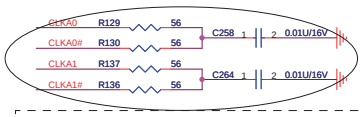
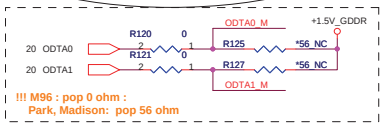
DDR3 64MX16, CH A : 512MB



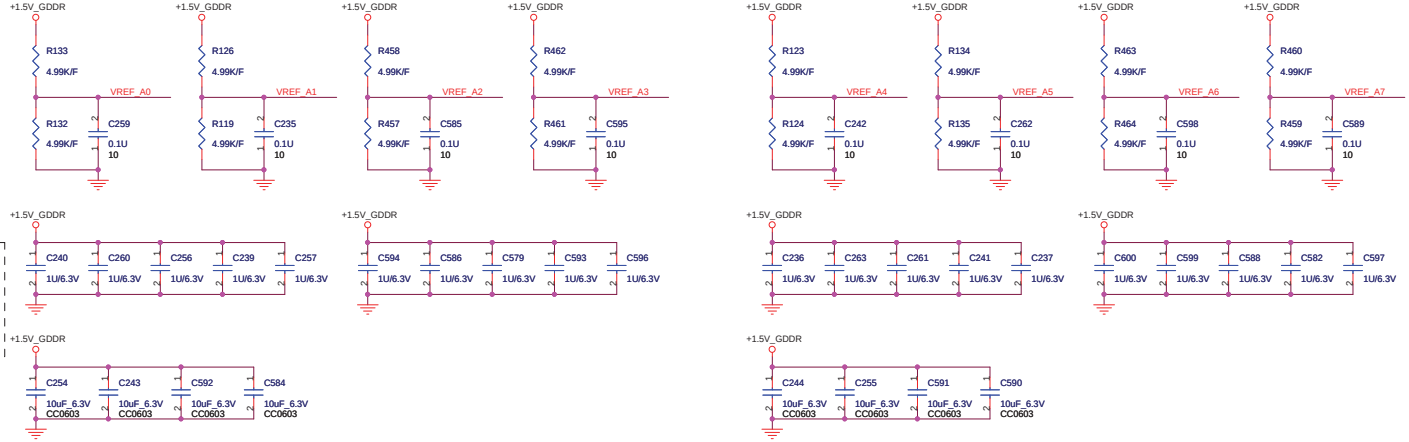
20 MDA[63..0]
20 MAA[13..0]
20 QSA#[7..0]
20 QSA[7..0]
20 DQMA#[7..0]
20 A_BA[2..0]

Placement has to be close to VRAM





!!! M96 : pop 0 ohm :
Park, Madison: pop 56 ohm



QUANTA COMPUTER

Title	M96XT_DDR3_A_512M	
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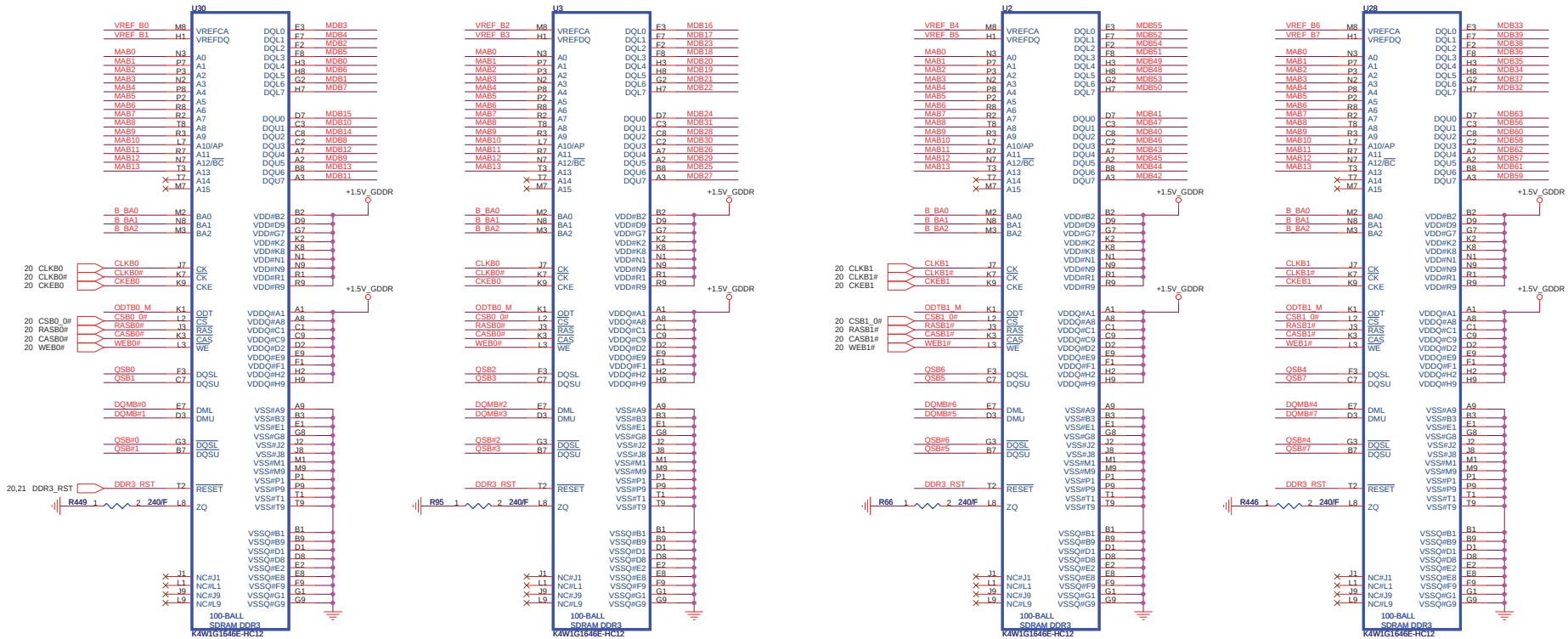
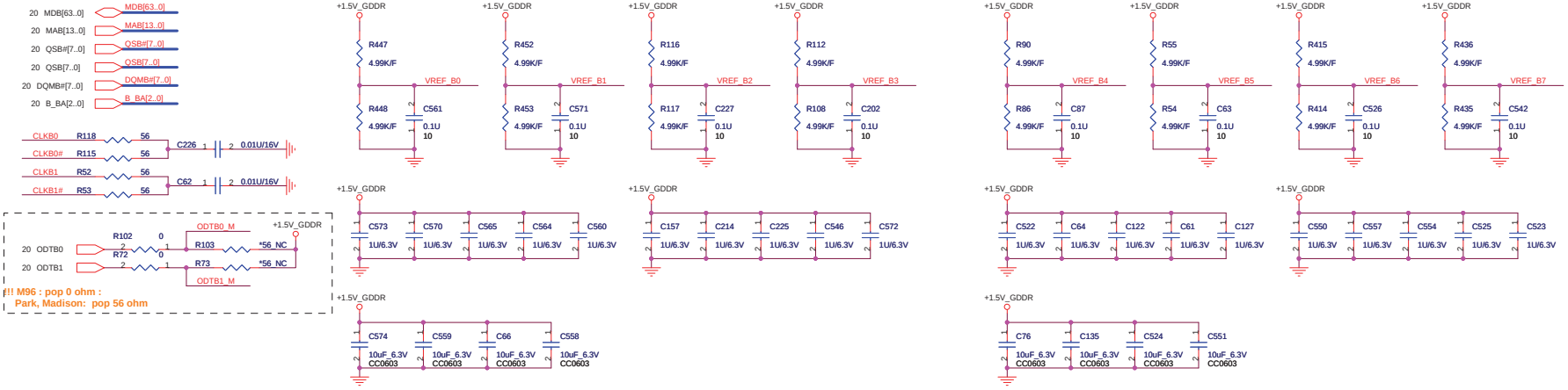
DDR3 64MX16, CH B : 512MB





!! M96 : pop 0 ohm :
Park, Madison: pop 56 ohm

QUANTA COMPUTER

Title	M96XT_DDR3_B_512M	
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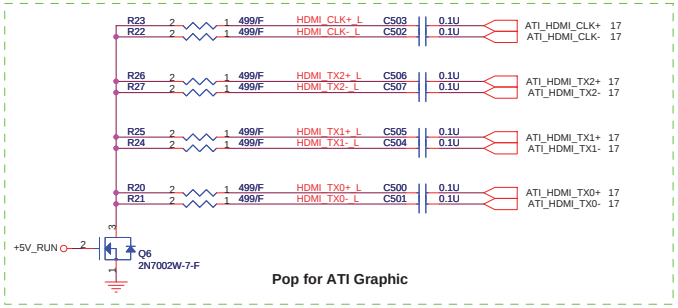
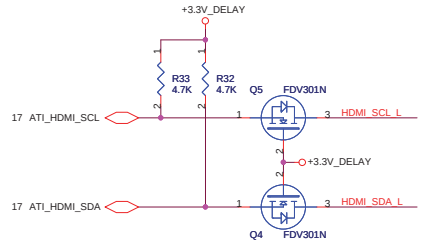
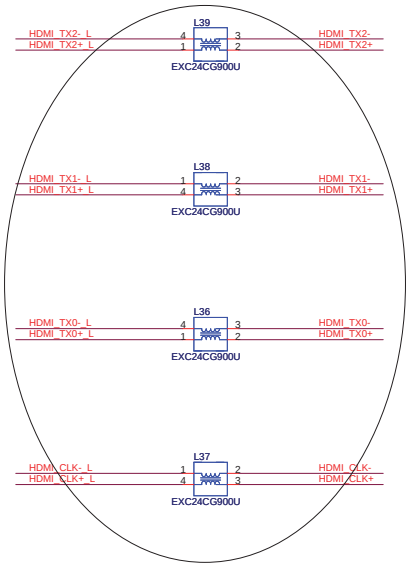
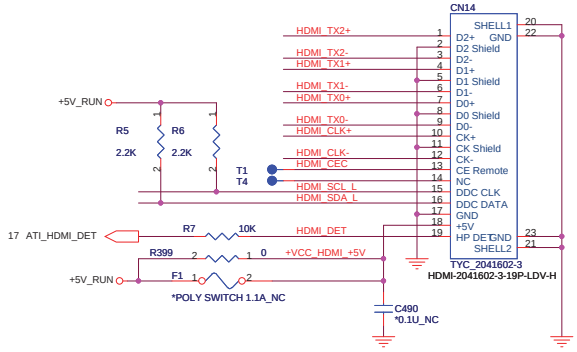


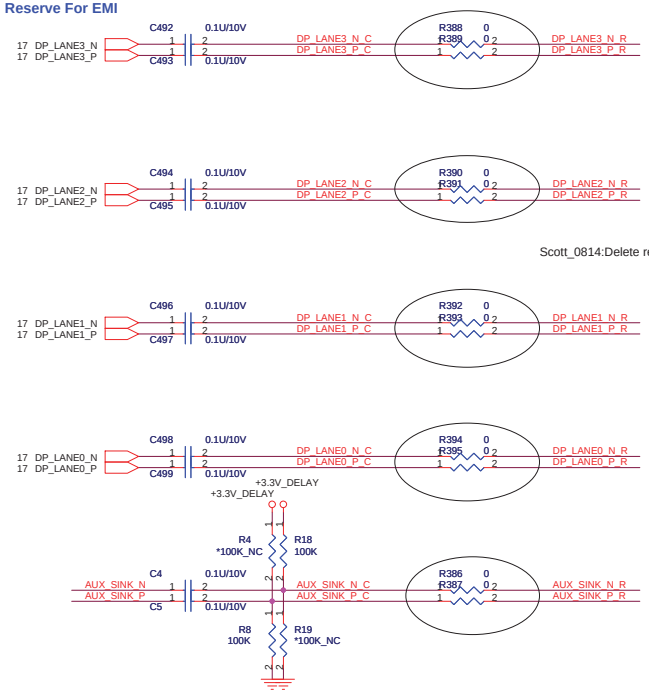
Pop for ATI Graphic







Reserve For EMI

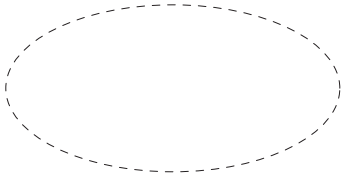


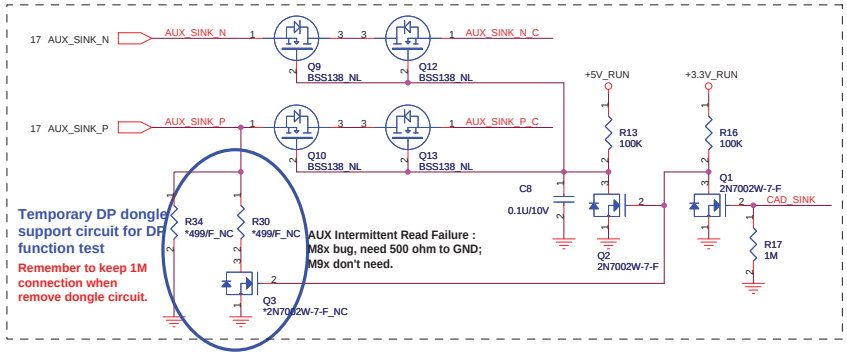
Scott_0814:Delete 0ohm reserve resistors as confirm with EMI.

Delete EMI ESD IC for EMI asked HDMI signals link to CONN directly.

Scott_0814:Delete reserve choke as confirm with EMI.

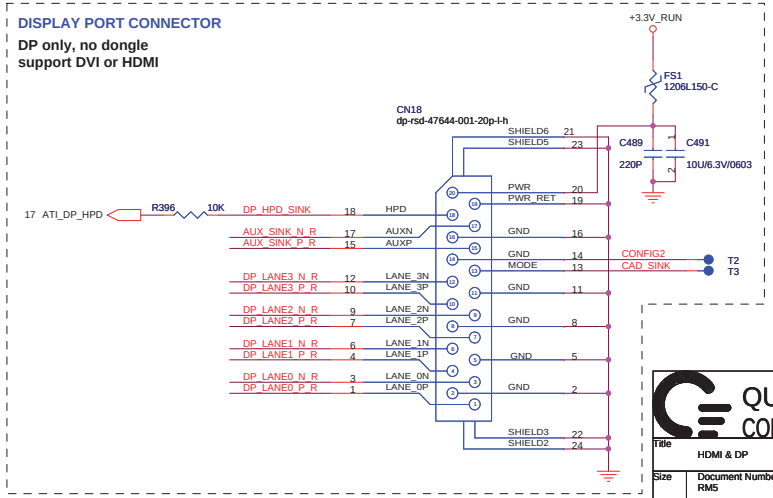
Scott_0703:Delete ESD Clamp U23,U24,U25 as EMI suggestion.





DISPLAY PORT CONNECTOR

DP only, no dongle support DVI or HDMI



Title	HDMI & DP		
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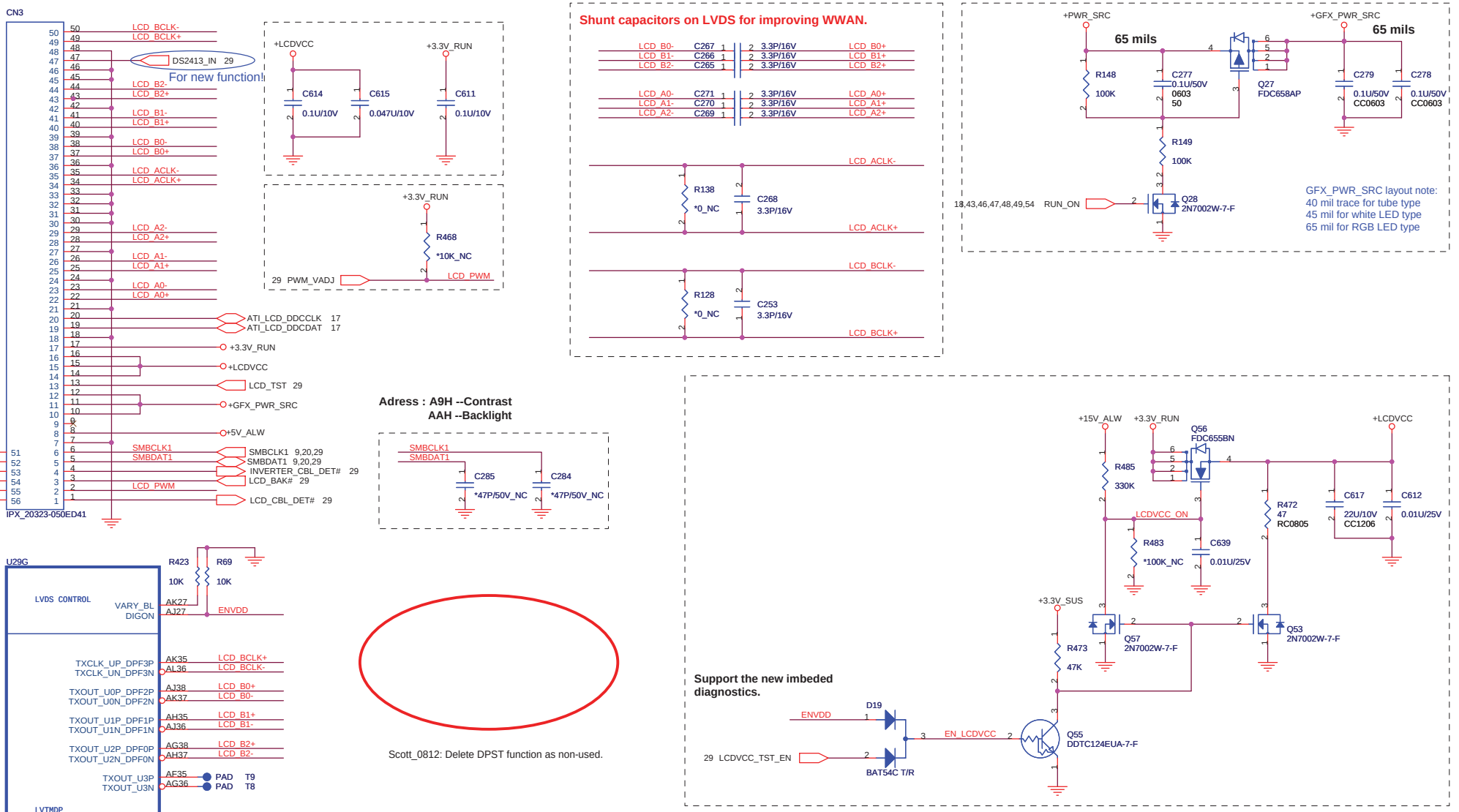

Title	M96XT_LVDS & LCD CONN	
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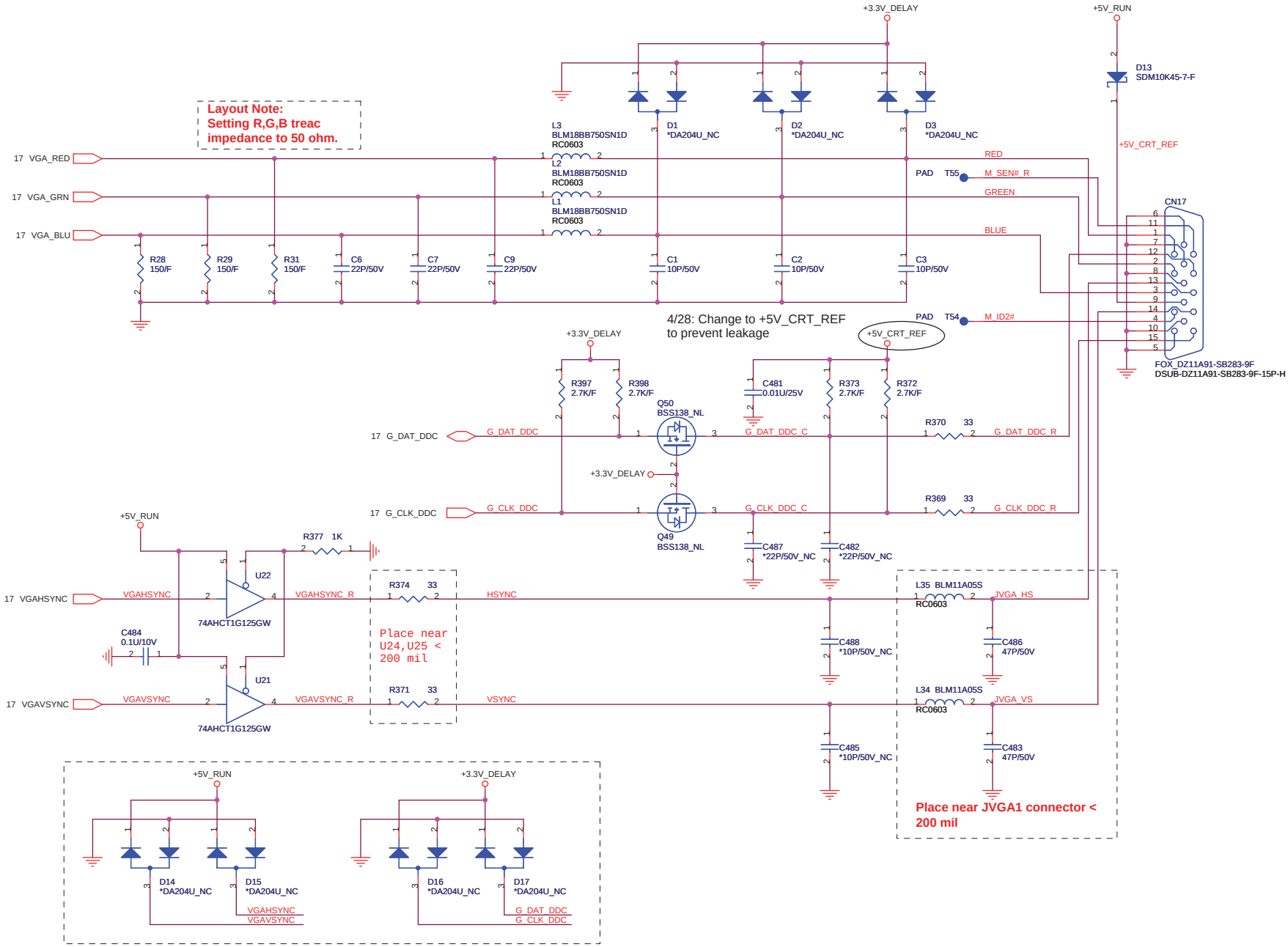
QUANTA COMPUTER



QUANTA COMPUTER		
Title	CRT CONN	
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Place close U23

Close to RU230
Shield GND Required

4/30: Change C812 to 27pF
Change C813 to 22pF

5/13: Reseved 100P
cap for EMI concern!

5/18: Added 10K pull-up to avoid floating signal
when powering up cardreader IC

MFIO Pin Assignment Table

MFIO	SD8	MS8	XD
00	WP	BS	D7
01	D1	-	D6
02	D0	D1	D5
03	D7	-	D4
04	D6	D5	D3
05	**CLK**	D0	D2
06	-	-	D1
07	D5	D4	D0
08	CMD	D2	WP#
09	D4	D6	WE#
10	D3	D3	ALE
11	D2	-	CLE
12	-	-	CE#
13	-	D7	RE#
14	-	**CLK**	R/B#

Title	CardReader (5C833)		
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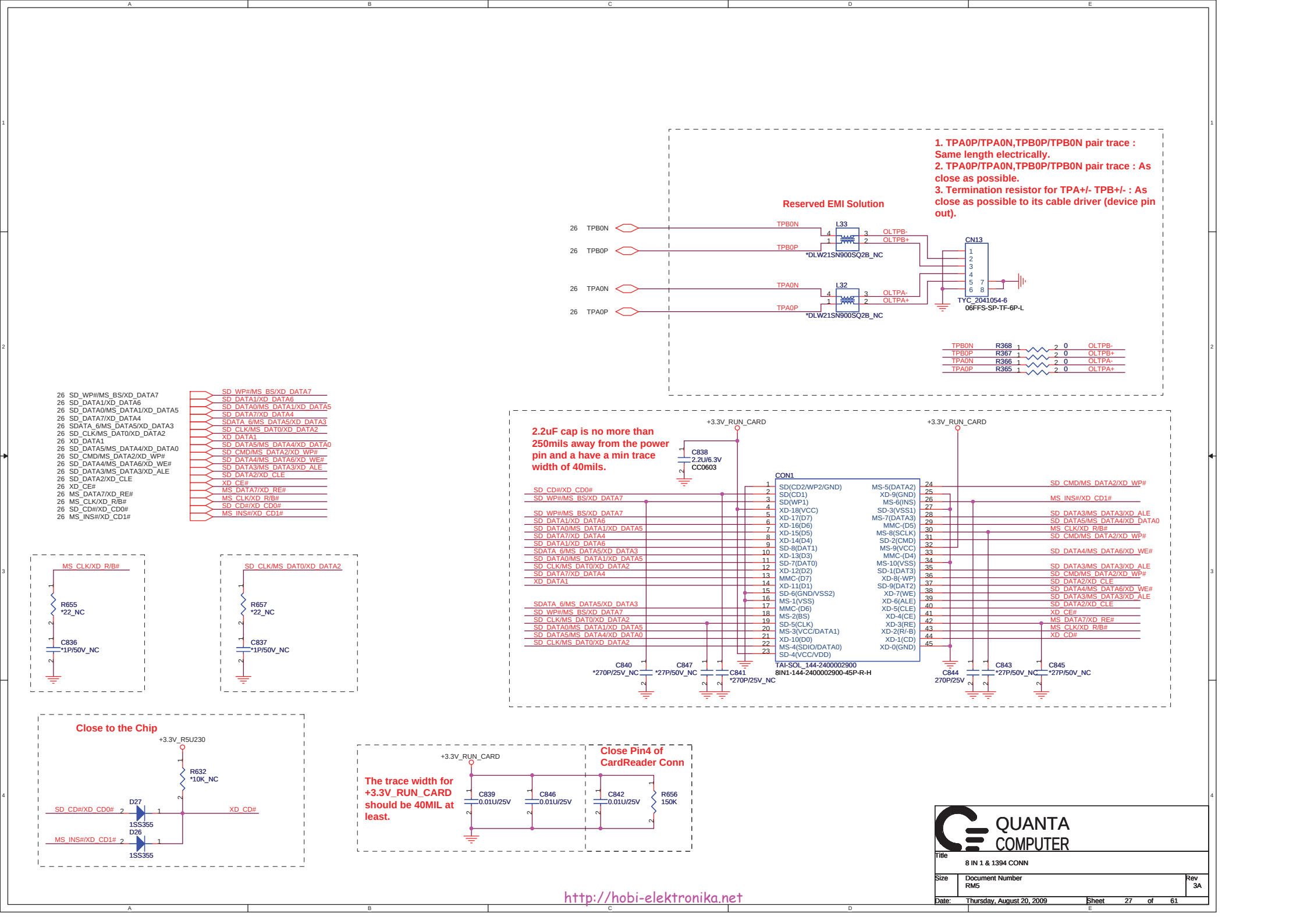
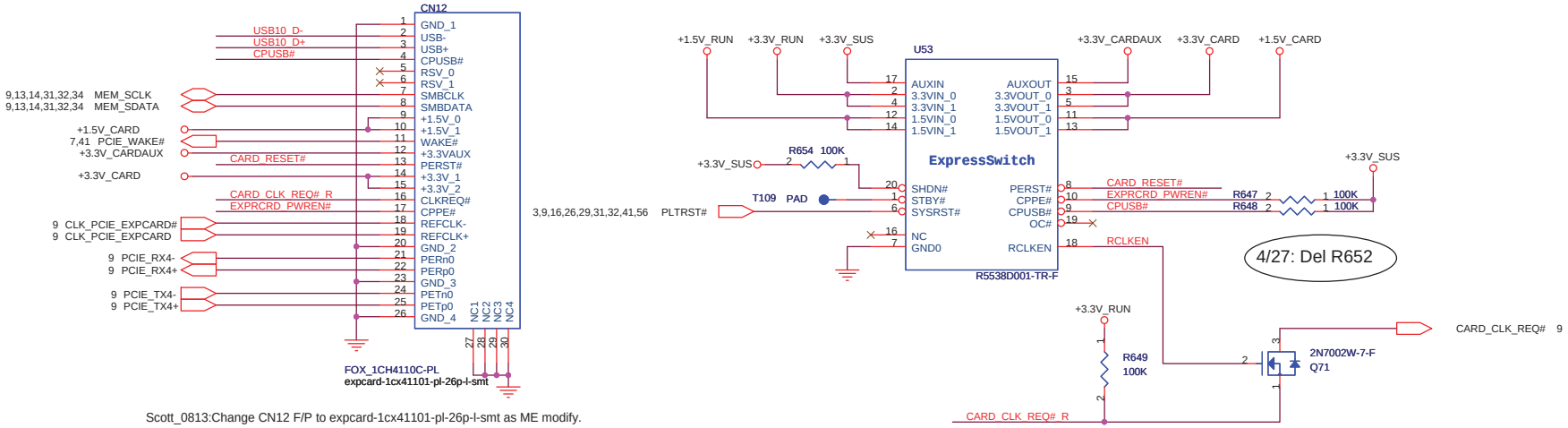
QUANTA COMPUTER



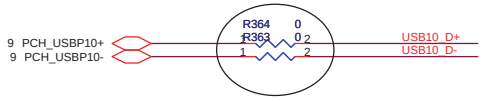
Express Card

+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.

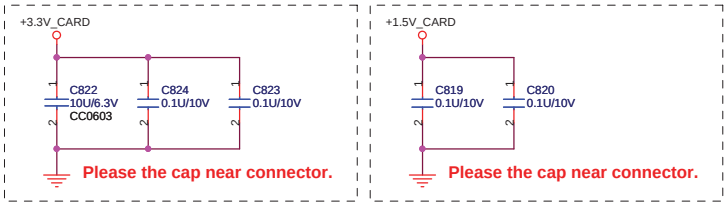


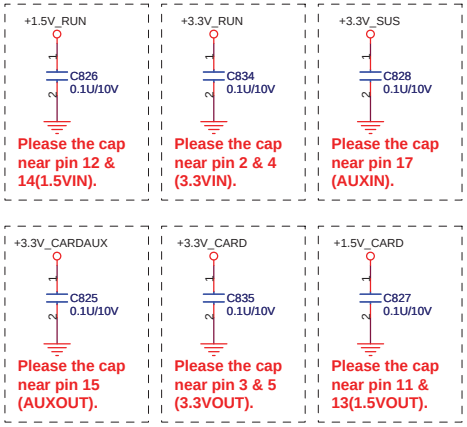
Scott_0813:Change CN12 F/P to expcard-1cx41101-pl-26p-l-smt as ME modify.

PCI-Express TX and RX direct to connector.



Scott_0814:Delete L31 as confirm with EMI.





QUANTA COMPUTER

Title	EXPRESS CARD	
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ITE8512E LQFP-128L

U40

35 KSO[0..16]
35 KSI[0..7]

50 IMVP_PWRGD

+3.3V_ALW
C695 10U
C688 0.1U
C681 0.1U
C689 0.1U
C690 0.1U
6.3 10 10 10 10
603
Place these caps close to ITE8512.

KSO16 KSO15 KSO14 KSO13 KSO12 KSO11 KSO10 KSO9 KSO8 KSO7 KSO6 KSO5 KSO4 KSO3 KSO2 KSO1 KSO0
KSO17/GPC5 KSO16/GPC3 KSO15 KSO14 KSO13 KSO12/SLCT KSO11/ERR KSO10/PE KSO9/BUSY KSO8/ACK KSO7/PD7 KSO6/PD6 KSO5/PD5 KSO4/PD4 KSO3/PD3 KSO2/PD2 KSO1/PD1 KSO0/PD0

KSI7 KSI6 KSI5 KSI4 KSI3 KSI2 KSI1 KSI0
KSI7 KSI6 KSI5 KSI4 KSI3/SLIN KSI2/INIT KSI1/AFD KSI0/STB

KEYBOARD

VBAT1 VCC
+3.3V_RUN
VSTBY1 VSTBY2 VSTBY3 VSTBY4 VSTBY5 VSTBY6
+3.3V_ALW
+RTC_CELL
C694 0.1U
10

ADC/DAC

ADC0/GPI0 ADC1/GPI1 ADC2/GPI2 ADC3/GPI3 ADC4/GPI4 ADC5/GPI5 ADC6/GPI6 ADC7/GPI7
HWPG
LCD_CBL_DET#
INVERTER_CBL_DET#
SIO_SLP_S5#

DAC0/GPJ0 DAC1/GPJ1 DAC2/GPJ2 DAC3/GPJ3 DAC4/GPJ4 DAC5/GPJ5
D20 SDMK0340L-7-F

HWPG 43
IMVP6_PROCHOT# 50
SUS_PWR_ACK 7
LCD_CBL_DET# 24
INVERTER_CBL_DET# 24
PBAT_PRES# 55
IINP 45
SIO_SLP_S5# 7
CRIT_TEMP_REP# 10
SIO_EXT_WAKE# 10
LAN_DISABLE 41
AUDIO_AVDD_ON 39
PCH_RSMRST# 7
SIO_PWRBTN# 7

NC RP22 with new MMB firmware V35 which have internal PU(5.6K) at MMB IC

Scott_0821:Delete SKTOCC# PH as SKTOCC# has been tie to GND on processor package

SMBDAT0 SMBCLK0 RP2 2.2KX2
SMBDAT1 SMBCLK1 RP3 10KX2
SMBDAT2 SMBCLK2 RP4 *10KX2_NC
SIO_SLP_S5# R512 *100K_NC
USB_CHG_DET# R510 100K
BREATH_PWLED# R569 100K
BREATH_LED# R553 100K
BAT_LED# R554 100K
USB_SIN_SIDE_EN# R341 100K

+3.3V_SUS
AC_PRESENT R535 10K
SUS_PWR_ACK R515 10K

+3.3V_RUN
LCD_BAK# R551 *10K_NC
IRQ_SERIRQ R567 10K
LCD_CBL_DET# R514 100K
INVERTER_CBL_DET# R513 100K
IMVP_VR_ON R509 *100K_NC
SUS_ON R524 100K
HWPG R661 100K

6/23: Pull SKTOCC# from CPU to EC according to EC request

3,9,16,26,28,31,32,41,56 PLTRST#
9 CLK_PCI_8512
8,32 LPC_LFRAME#
8,32 LPC_LAD0
8,32 LPC_LAD1
8,32 LPC_LAD2
8,32 LPC_LAD3
CLK_PCI_8512
LPCRST/WUI4/GPD2 LPCCLK LFRAME LAD0 LAD1 LAD2 LAD3

7 CLKRUN#
8 IRQ_SERIRQ
10 SIO_EXT_SMI#
10 SIO_EXT_SCI#
10 SIO_A20GATE
24 LCD_TST
IRQ_SERIRQ
D23 SDMK0340L-7-F
D24 SDMK0340L-7-F
D21 SDMK0340L-7-F
CLKRUN/GPH0/ID0 SERIRQ ECSMI/GPD4 ECSCI/GPD3 GA20/GPB5 LPCPD/WUI6/GPE6

10 SIO_RCIN#
D22 SDMK0340L-7-F
WRST#
24 LCD_BAK#
LCD_BAK#
KBRST/GPB6 WRST PWUREQ/GPC7

39 NB_MUTE#
8,38 ICH_AZ_CODEC_RST#
L80HLAT/GPE0 L80LLAT/WUI7/GPE7

LPC

PWM0/GPA0 PWM1/GPA1 PWM2/GPA2 PWM3/GPA3 PWM4/GPA4 PWM5/GPA5 PWM6/GPA6 PWM7/GPA7
BREATH_LED#
BREATH_PWLED#
BAT_LED#
BREATH_LED# 36
BREATH_PWLED# 36
FAN1_PWM 37
PWM_VADJ 24
BAT_LED# 36
KB_BACKLITE_EN 35
USBP0_BUS_SW_CB 33
BEEP 38

TACH0/GPD6 TACH1/GPD7
FAN1_TACH 37
PANEL_BKEN 17

TMRI0/WUI2/GPC4 TMRI1/WUI3/GPC6
LID_SW# 35,36
SIO_SLP_S3# 7

PWM

RXD/GPB0 TXD/GPB1 CRX0/GPC0 CTX0/GPB2 CRX1/GPH1/ID1 CTX1/GPH2/ID2
DS2413_IN 24
SKTOCC# 3
CIRRX 30
RUN_ON_1 43
HDDC_EN 34
IMVP_VR_ON
IMVP_VR_ON 50

IR/UART

CHARGE, BAT,CLK & THERMAL
PCH & LCD & VGA THERMAL
MMB ONLY!!

37,45,55 SMBCLK0
37,45,55 SMBDAT0
9,20,24 SMBCLK1
9,20,24 SMBDAT1
35 SMBCLK2
35 SMBDAT2
SMBCLK0 SMBDAT0 SMBCLK1 SMBDAT1 SMBCLK2 SMBDAT2
SMCLK0/GPB3 SMDAT0/GPB4 SMCLK1/GPC1 SMDAT1/GPC2 SMCLK2/GPF6 SMDAT2/GPF7

SMBUS

FLFRAME/GPG2/LF FLRST/GPG0/TM FLAD3/GPG6
SUS_ON
SUS_ON 47,54
KB_DET# 35
CAP_LED# 35

FLAD2/SO FLAD1/SI FLAD0/SCE FLCLK
EC_FLASH_SPI_DO 30
EC_FLASH_SPI_DIN 30
EC_FLASH_SPI_CS# 30
EC_FLASH_SPI_CLK 30

LPC/FWH FLASH

EGAD/GPE1 EGCS/GPE2 EGCLK/GPE3
PCH_PWRGD
PCH_PWRGD 7
5V_ALW_ON 51
GFX_ON 20,52,53

EGPC

GPH3/ID3 GPH4/ID4 GPH5/ID5 GPH6/ID6 GPG1/ID7
USB_L_SIDE_EN#
BID0
BID1
BID2
USB_L_SIDE_EN# 33
MODC_EN 34

GPIO

36 LED_MASK#
33 USB_CHG_DET#
USB_CHG_DET#
PS2CLK0/GPF0 PS2DAT0/GPF1

55 PS_ID
35 MEDIA_INT#
PS2CLK1/GPF2 PS2DAT1/GPF3

35 CLK_TP_SIO
35 DAT_TP_SIO
PS2CLK2/GPF4 PS2DAT2/GPF5

PS/2

RI1/WUI0/GPD0 RI2/WUI1/GPD1 WUI5/GPE5
USB_SIN_SIDE_EN#
USB_SIN_SIDE_EN# 33
ACAV_IN 45
MMB_ISSP 35

RING/PWRFAIL/LPCRST/GPB7
AC_PRESENT 7

PWRSW/GPE4
MAIN_PWR_SW# 35

GINT/GPD5
LCDVCC_TST_EN 24

ITE8512_XTAL1
ITE8512_XTAL2
CK32K
CK32KE

ITE8512IX_JX
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7

+3.3V_ALW
L66 BLM18AG121SN1D 603
C682 0.1U 10
L65 603 BLM18AG121SN1D

AVCC AVSS

IT8512E/KX-L
LQFP128-16X16-4-FX2

CLK_PCI_8512
R550 10
C702 2.2P
50

32KHz Clock.
ITE8512_XTAL2
Y4
ITE8512_XTAL1
C692 18P 50
32.768KHZ
C691 18P 50

ITE8512IX_JX
C693 0.1U 10

ITE8512IX Populate R735 0 ohms.
ITE8512JX Populate R735 to 0.1uF, & De-pop Cap 1uF.

37,51 THERM_STP#
D28 SDMK0340L-7-F
WRST#
+3.3V_ALW
R643 100K
C821 1U

http://hobi-elektronika.net

Board ID Straps

Clarksfield
Arrandale
+3.3V_ALW
R507 10K
R523 *10K_NC
R518 10K
R516 10K
R508 *10K_NC
R520 10K
R519 *10K_NC
R517 *10K_NC
BID0
BID1
BID2
USB_L_SIDE_EN#

CPU_IDENTIFY (USB_L_SIDE_EN#)
1 = Clarksfield. ; 0 = Arrandale.

BID2	BID1	BID0	RM5
0	0	0	SSI(X00)
0	0	1	PT(X01)
0	1	0	ST(X02)
0	1	1	QT(X03)
1	0	0	
1	0	1	

QUANTA COMPUTER

Title	SIO (ITE8512)	
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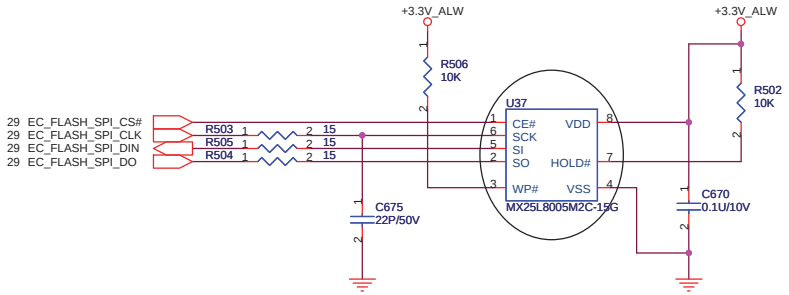
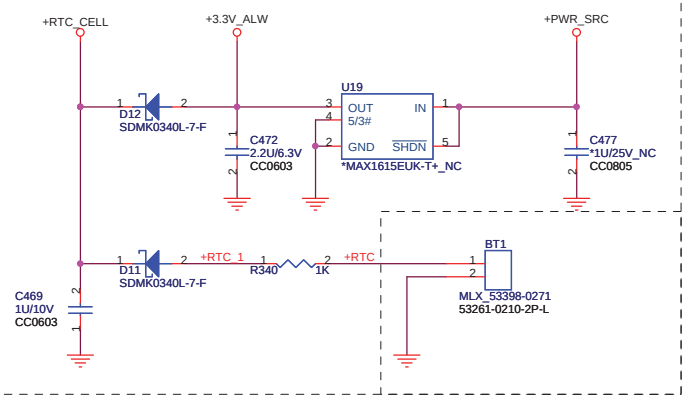
Date:	Thursday, August 20, 2009	Sheet 29 of 61

EC SPI ROM, 8Mbit (1M Byte)

5/12: Change U37 from 2MB to 1MB according to BIOS request!

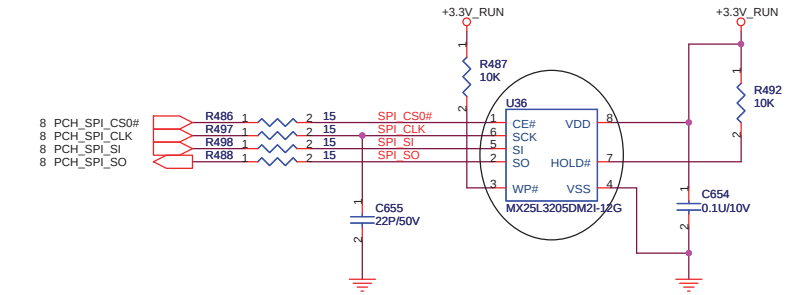


RTC BATTERY

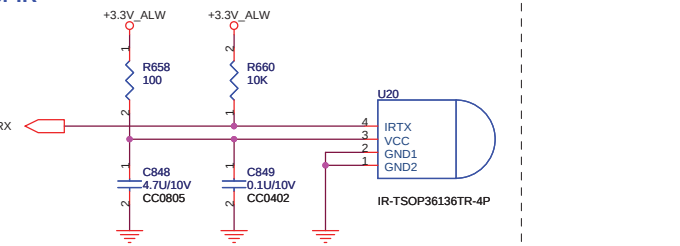


PCH SPI ROM, (4M Byte)

5/12: Change U36 from 2MB to 4MB according to BIOS request!



Consumer IR



QUANTA COMPUTER

Title	FLASH/ RTC/ CIR	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 30 of 61	

MiniCard WLAN Connector

Mini Card Nut

H21
Mini Card Align (h6.6)

5/15: Change WAKE# to NC as it is not required

MINI1CLK_REQ#
C698
220P/50V

CN24

32 COEX2_WLAN_ACTIVE	1	WAKE#	3.3V_1 2
32 COEX1_BT_ACTIVE_MINI	3	RESERVED_1	GND0 4
9 MINI1CLK_REQ#	5	RESERVED_2	1.5V_1 6
MINI1CLK_REQ#	7	CLKREQ#	UIM_PWR 8
	9	GND1	UIM_DATA 10
9 CLK_PCIE_MINI1#	11	REFCLK-	UIM_CLK 12
9 CLK_PCIE_MINI1	13	REFCLK+	UIM_RESET 14
	15	GND2	UIM_VPP 16
	17	UIM_C8	GND3 18
	19	UIM_C4	W_DISABLE# 20
	21	GND4	PERST# 22
9 PCIE_RX2-	23	PERn0	3.3VAUX1 24
9 PCIE_RX2+	25	PERp0	GND5 26
	27	GND6	1.5V_2 28
	29	GND7	SMB_CLK 30
9 PCIE_TX2-	31	PETn0	SMB_DATA 32
9 PCIE_TX2+	33	PETp0	GND8 34
	35	GND9	USB_D- 36
10 PCIE_MCARD1_DET#	37	RESERVED_3	USB_D+ 38
	39	RESERVED_4	GND10 40
	41	RESERVED_5	LED_WWAN# 42
	43	RESERVED_6	LED_WLAN# 44
	45	RESERVED_7	LED_WPAN# 46
	47	RESERVED_8	1.5V_3 48
	49	RESERVED_9	GND11 50
	51	RESERVED_10	3.3V_2 52

1759513-1
MIPCIEXP-1775838-1-52P

PCI-Express TX and RX direct to connector

+3.3V_RUN
+1.5V_RUN

C853 100P 50 NPO
PLTRST# 3,9,16,26,28,29,32,41,56
WLAN_RADIO_OFF#
+3.3V_RUN
MEM_SCLK 9,13,14,28,32,34
MEM_SDATA 9,13,14,28,32,34
USB4_D-
USB4_D+
USB_MCARD1_DET# 9
PAD T106
LED_WLAN_OUT# 36
PAD T105

5/03: Added 100p to PLTRST# and PCIE_WAKE# according to EMI request

Reserved PAD for EMI

USB4_D-
USB4_D+
L70
*DLW21SN900SQ2B_NC
PCH_USBP4- 9
PCH_USBP4+ 9
R708 0
R709 0

Suport for WoW

WLAN_RADIO_OFF#
D25
SDMK0340L-7-F
WLAN_RADIO_DIS# 10
R612
*0_NC

Prevent backdrive when WoW is enabled.

Place caps close to connector.

+1.5V_RUN
C434 0.047U/10V
C779 0.047U/10V

+3.3V_RUN
C460 0.1U/10V
C767 0.047U/10V
C456 0.1U/10V
C457 0.047U/10V
C449 4.7U/10V CC0805

QUANTA COMPUTER

Title	MINI-CARD (WLAN)	
Size	Document Number RM5	Rev 3A
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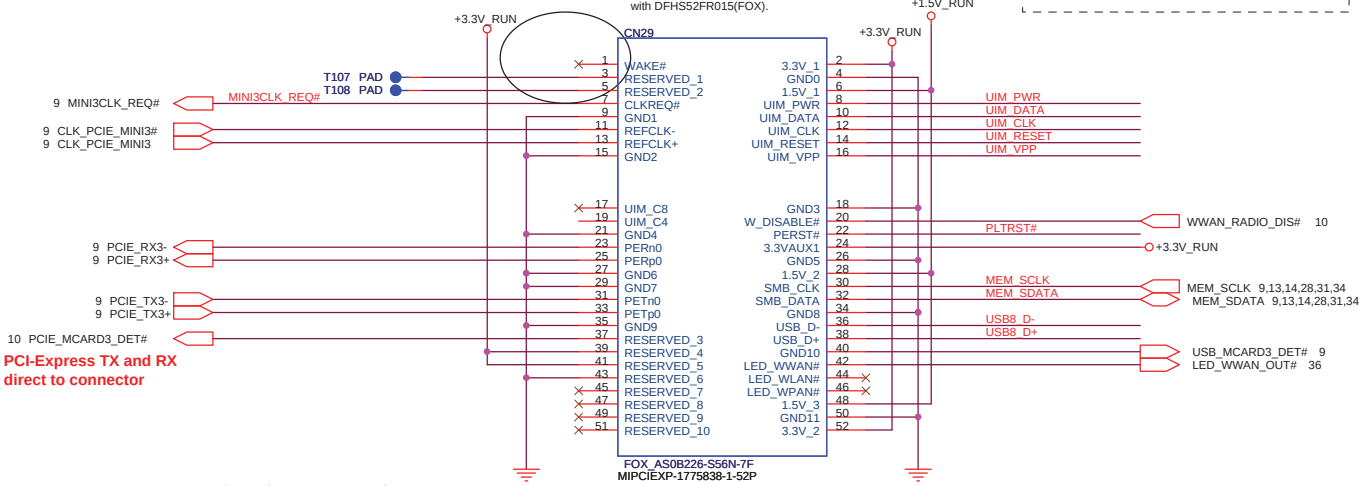
5/13: Pull up WAKE# to 3.3V_RUN so as to avoid leakage

5/15: Change WAKE# to NC as it is not required

5/08: Swap WWAN and WPAN according to antenna team's suggestion

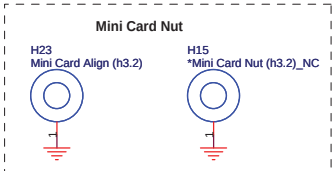
MiniCard WWAN Connector

Scott_0123:Change CN31 PN with DFHS52FR015(FOX).

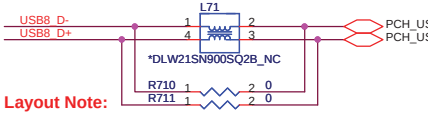


PCI-Express TX and RX direct to connector

Mini Card Nut

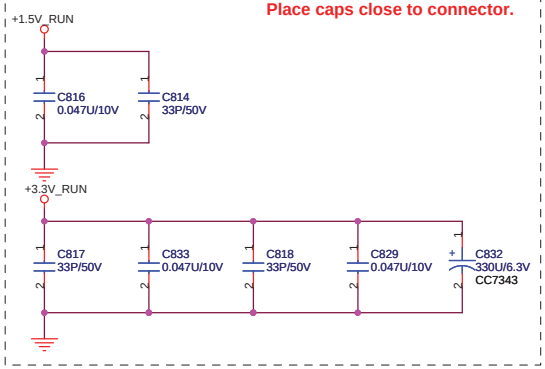


Reserve For EMI

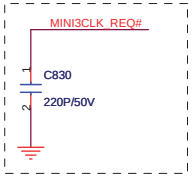


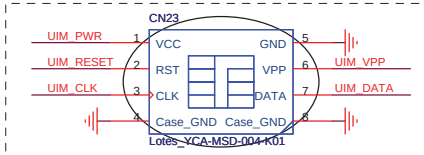
Layout Note:
R240 and R244 close to choke as possible to minimize stubs.

Place caps close to connector.



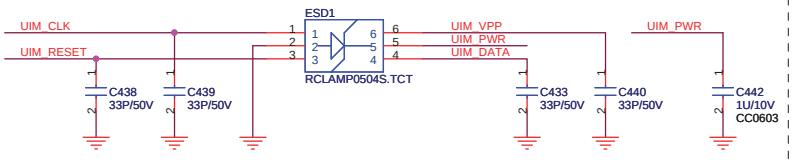
5/13: Change SIM card connector to Lotes



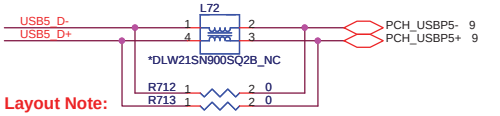


Place as close as possible to JMINI connector

layout note:10 mil trace and 20 mil space for SIM card and UIM_PWR use 20mil

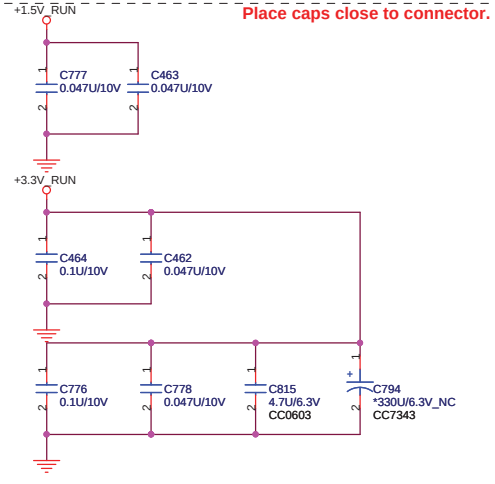


Reserve For EMI



Layout Note:
R240 and R244 close to choke as possible to minimize stubs.

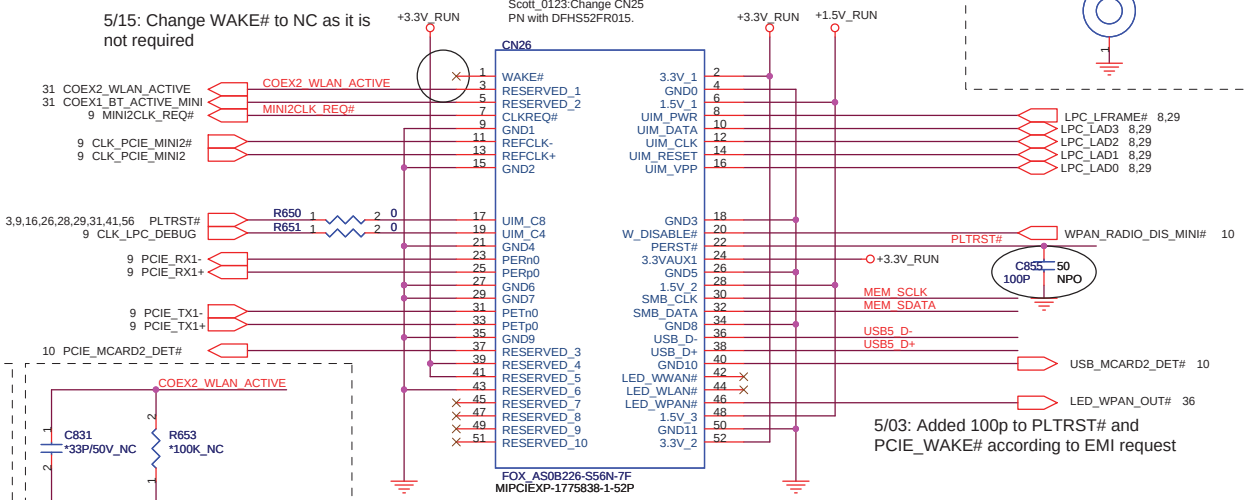
Place caps close to connector.



MiniCard Robson, BT. UWB Connector

5/15: Change WAKE# to NC as it is not required

Scott_0123:Change CN25 PN with DFHS52FR015.



Mini Card Nut

5/03: Added 100p to PLTRST# and PCIE_WAKE# according to EMI request

QUANTA COMPUTER

Title	MINI-CARD (WPAN,WWAN)	
Size	Document Number RM5	Rev 3A
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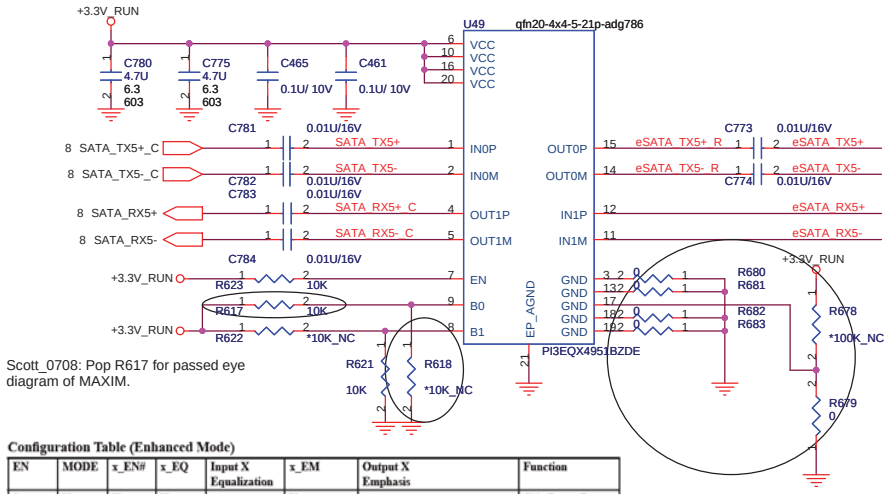
eSATA Re-driver IC



Scott_0708: Pop R617 for passed eye diagram of MAXIM.

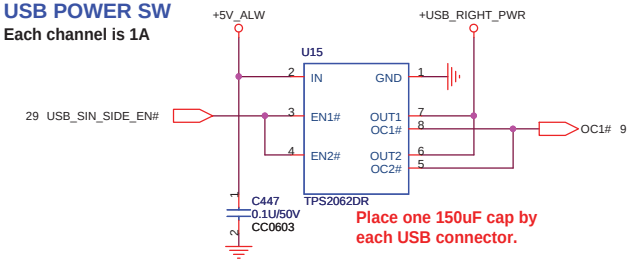
Configuration Table (Enhanced Mode)

EN	MODE	x_EN#	x_EQ	Input X Equalization	x_EM	Output X Emphasis	Function
0	X	X	X	n/a	X	n/a	Chip Power Down
1	1	1	X	n/a	X	n/a	Chip enabled, Channel x disabled
1	1	0	0	2.5dB	1.1K to 15K resistor	Resistor Controlled, 6dB to 0dB (1)	Chip and channel enabled, low input equalization
1	1	0	1	6.5dB	1.1K to 15K resistor	Resistor Controlled, 6dB to 0dB (1)	Chip and channel enabled, high input equalization

5/11: Reserved 0 ohms for Pericom enhanced mode select
5/12: Change IC to Pericom as Maxim failed EA test
6/23: NC according to Pericom reccomandation!

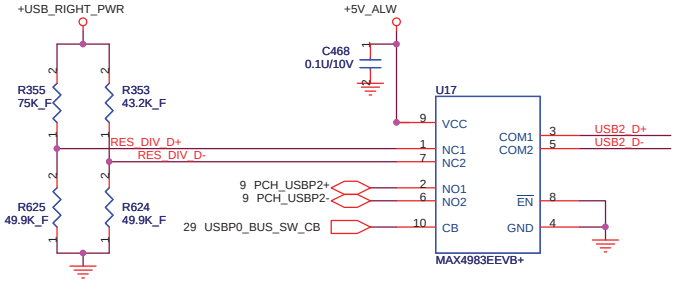
USB POWER SW

Each channel is 1A

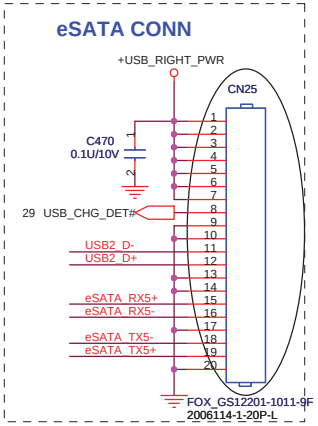


Place one 150uF cap by each USB connector.

USB Power Share



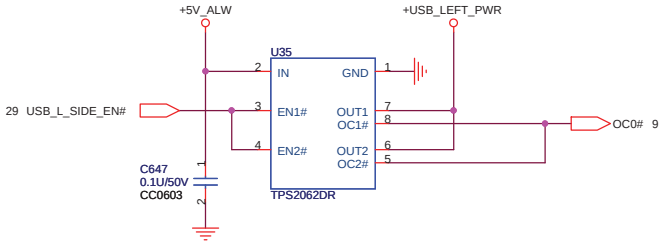
eSATA CONN



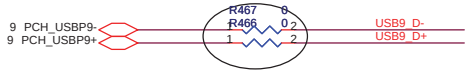
5/13: Change Connector to Foxconn to avoid material shortage for Tyco

USB POWER SW

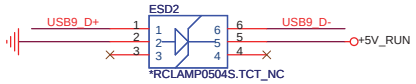
Each channel is 1A

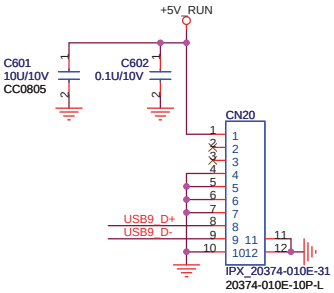


TV module

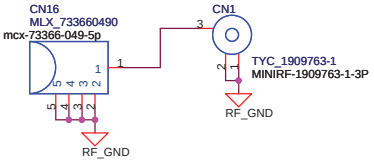


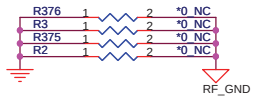
Scott_0814:Delete L58 as confirm with EMI.

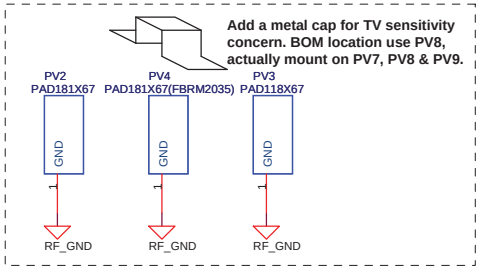




TV RF Jack & Microwave connector







QUANTA COMPUTER

Title	USB & eSATA & TV	
Size	Document Number RM5	Rev 3A
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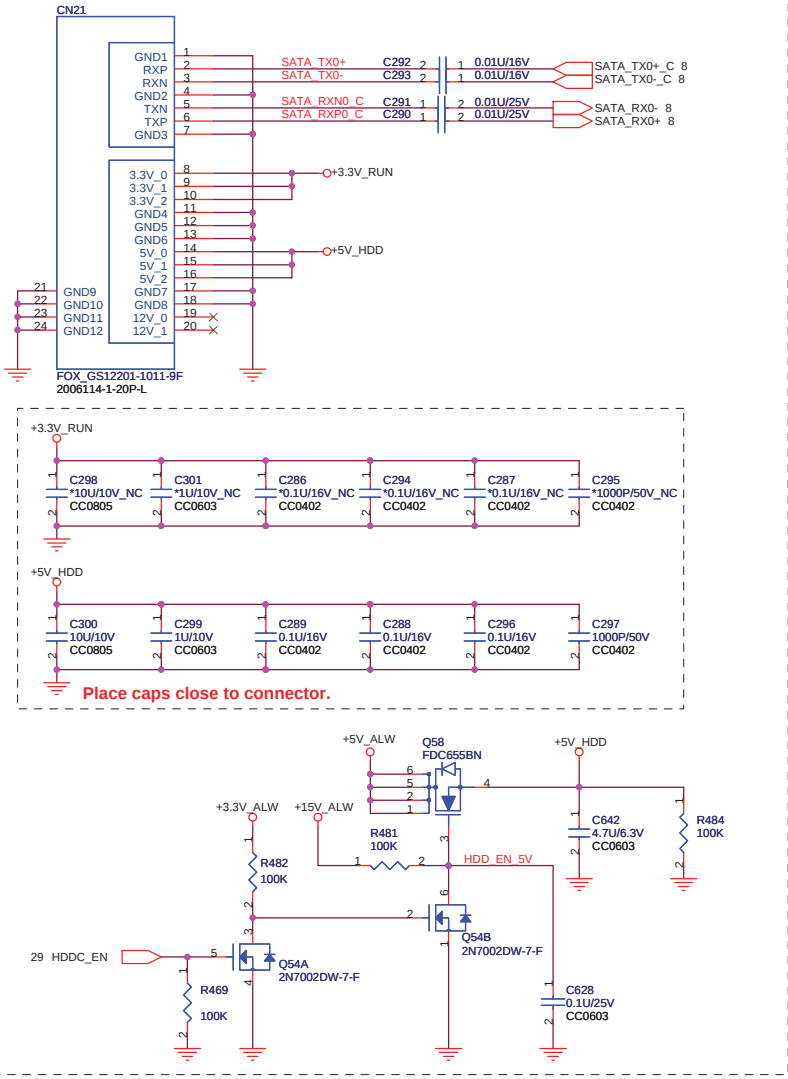
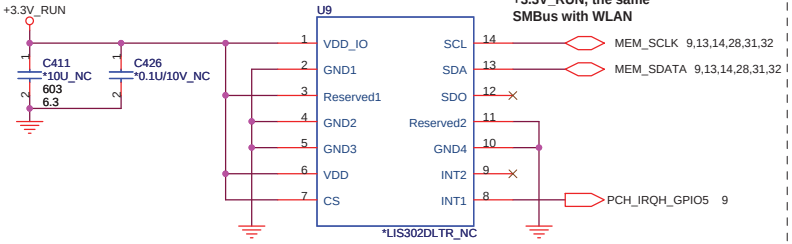
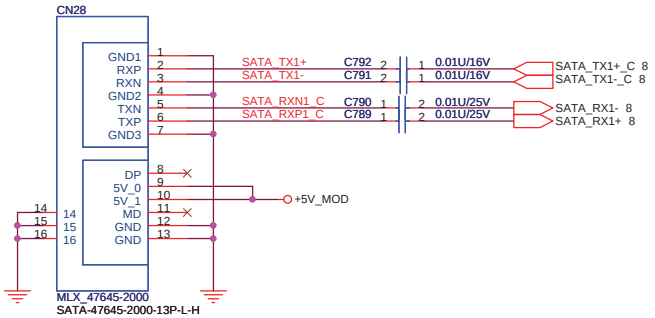
SATA Connector

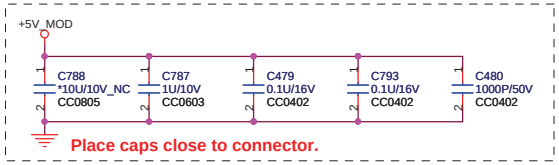


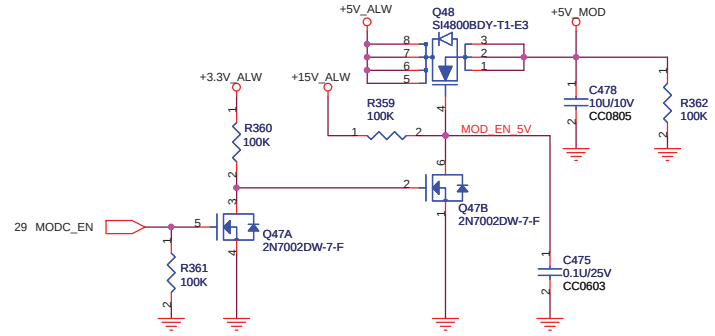
3-axis Fall Sensor (HDD data protector)



ODD Connector







QUANTA COMPUTER

Title	HDD & ODD (SATA)	
Size	Document Number RM5	Rev 3A
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To Daughter Board connector

Solid White = System On, Normal Activity
Off= System off (system off or hibernate);
"Breathing White " = System in Standby (S3);

Power Button
Speaker
KB LED
Touch Pad
Media Button

Scott_0123:Change CN8 PN with DFHD32MR003(With mylar)

CN9
FOX_QB5RF321-1203-8F
gb5rf341-12037f-32p-l

36 BREATH_PWRLED_INT
POWER_SW_IN0#
39 AUD_SPK_L1
39 AUD_SPK_L2
39 AUD_SPK_R1
39 AUD_SPK_R2
R588 200K/F
R594 100K
8 KB_LED_DET
29 KB_BACKLITE_EN
+5V_RUN
29 DAT_TP_SIO
29 CLK_TP_SIO
+3.3V_ALW
SMBDAT2_MMB
+5V_ALW
+MMB_PWR
SMBCLK2_MMB
MEDIA_INT#
29 MEDIA_INT#

Power Button

+3.3V_ALW
D29 *DA204U_NC
R666 100K
R668 10K
POWER_SW_IN0#
MAIN_PWR_SW# 29
C850 1U/10V CC0603

Hall Switch

+3.3V_ALW
C626 0.1U/10V
"MEDIA_INT#" PU at MB side
R599 100K
MEDIA_INT#
U7
VDD
VSS
OUT
EM-6781-T3
LID_SW#
LID_SW# 29,36

Active high for ISSP reset

Q44 SI2303BDS-T1-E3
+5V_ALW2
+MMB_PWR
C405 0.1U/10V
R287 10K
R279 100
R284 100K
+3.3V_ALW
29 MMB_ISSP
Q39 2N7002W-7-F
Q40 2N7002W-7-F

+MMB_PWR
Q42 2N7002W-7-F
R286 *20K_NC
R299 *20K_NC
29 SMBDAT2
SMBDAT2_MMB
Q43 2N7002W-7-F
29 SMBCLK2
SMBCLK2_MMB

NC R620 & R621 with new MMB firmware V35 which have internal PU(5.6K) at MMB IC

KEYBOARD CONNECTOR

29 KSI[0..7]
29 KSO[0..16]
R493 100K
+3.3V_ALW
29 KB_DET#
CN7
GND1
GND2
KSI7 KSI6 KSI4 KSI2 KSI5 KSI1 KSI3 KSI0
KSO5 KSO7 KSO6 KSO8 KSO3 KSO4 KSO1 KSO2 KSO0 KSO12 KSO16 KSO15 KSO13 KSO14 KSO9 KSO11 KSO10
CAP_LED_L
HRS_FH28-60(30)SB-1SH(86)
FH28-30SB-1SH-30P-R

+3.3V_ALW
+3.3V_ALW
+5V_RUN
R265 100K
29 CAP_LED#
Q41 2N7002W-7-F
Q38 DDTA114YUA-7-F
47k
10K
R253 150
CAP_LED_L

CP2 100PX4
CP1 100PX4
CP4 100PX4
CP3 100PX4
CP6 100PX4
CP5 100PX4
50 NPO 1206
C656 100P/50V
KSI7
100P CAPS close to KB connector

5/03: Populate according to EMI request!
5/12: Change from CA110084N04 to CA110084N39 due to material shortage!

Array Microphone & Camera

Scott_0814:Delete L29 as confirm with EMI.

+3.3V_RUN +3.3V_RUN +3.6V_RUN
R628 100K
L30 BLM11A05S RC0603
L28 *BLM11A05S_NC RC0603

The GND (pin 8) for DMIC is defined as AGND. Connect with GND at MB, but separate AGND & GND at coaxial cable & CCD module.

9 PCH_USBP11+
9 PCH_USBP11-
R358
R357
USB11_D+
USB11_D-
CAM_VCC
CN10
IPX_20374-010E-31
20374-010E-10P-L

38 DMIC_DATA
38 DMIC_CLK
10 CAMERA_CBL_DET#
R627 0/0603 RC0603
R626 22/0603 RC0603
DMIC_DATA_R
DMIC_CLK_R

C785 *33P/50V_NC
C786 *33P/50V_NC
C471 10U/10V CC0805

+5V_RUN
U16
IN
OUT
EN
GND
NC/FB
*TPS76301DBVR_NC
+3.6V_RUN
C459 *1U/10V_NC CC0603
R351 *100K/F_NC
C467 *27P/50V_NC
R352 *49.9K/F_NC
C466 *4.7U/6.3V_NC CC0603

QUANTA COMPUTER

Title	KB/ CCD/ UI	
Size	Document Number RM5	Rev 3A
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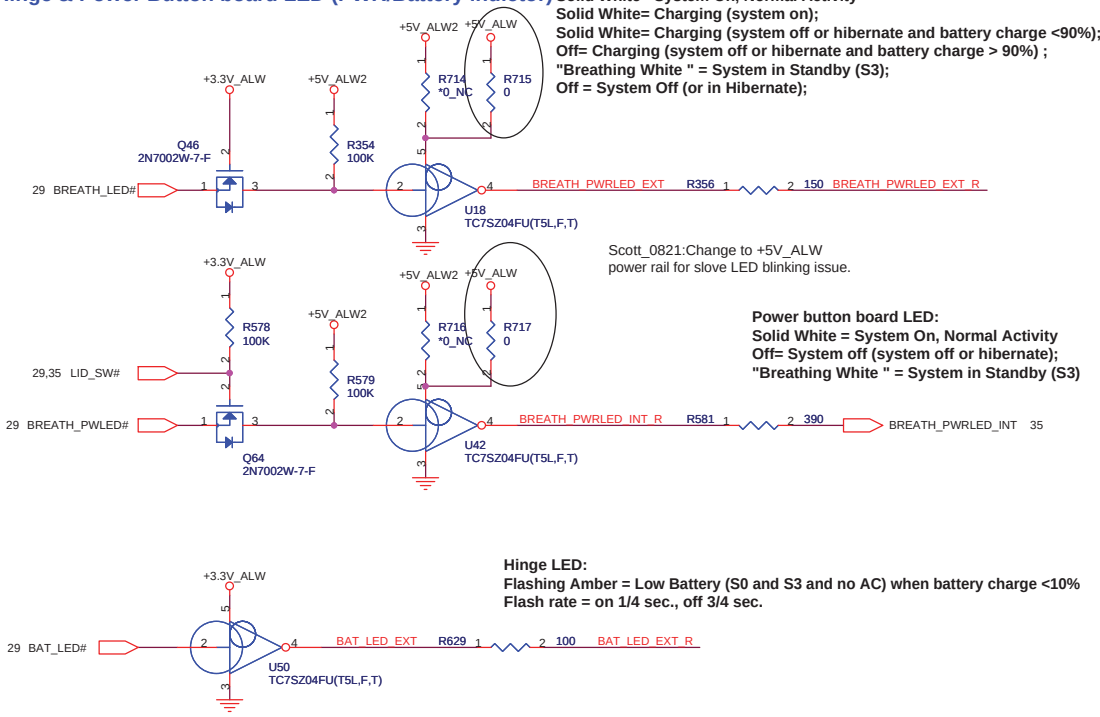
Hinge & Power Button board LED (PWR/Battery indictor)



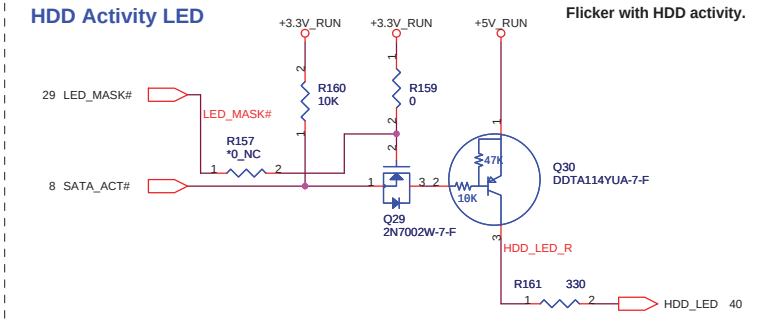
Hinge LED
Solid White= System On, Normal Activity
Solid White= Charging (system on);
Solid White= Charging (system off or hibernate and battery charge <90%);
Off= Charging (system off or hibernate and battery charge > 90%) ;
"Breathing White " = System in Standby (S3);
Off = System Off (or in Hibernate);

Scott_0821:Change to +5V_ALW
power rail for slove LED blinking issue.

Power button board LED:
Solid White = System On, Normal Activity
Off= System off (system off or hibernate);
"Breathing White " = System in Standby (S3)

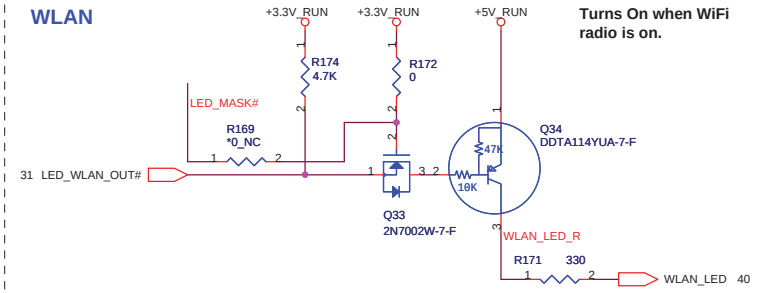
Hinge LED:
Flashing Amber = Low Battery (S0 and S3 and no AC) when battery charge <10%
Flash rate = on 1/4 sec., off 3/4 sec.

HDD Activity LED



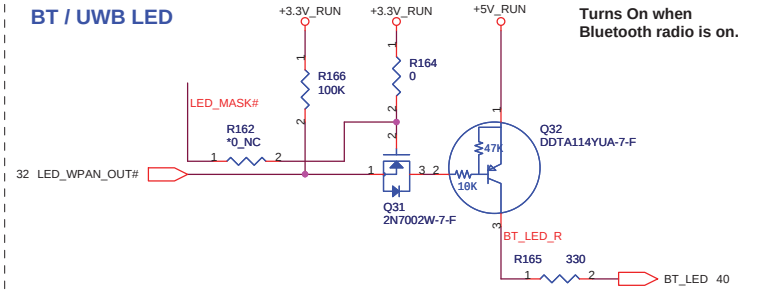
Flicker with HDD activity.

WLAN



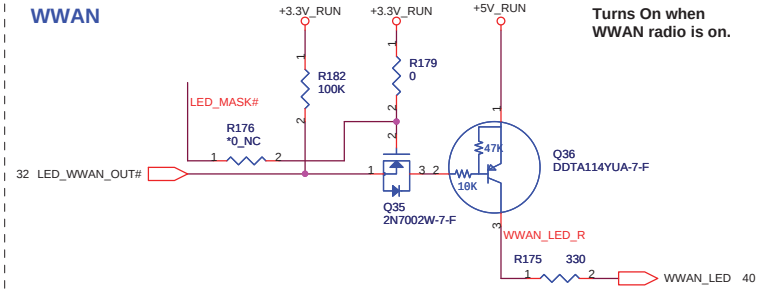
Turns On when WiFi radio is on.

BT / UWB LED



Turns On when Bluetooth radio is on.

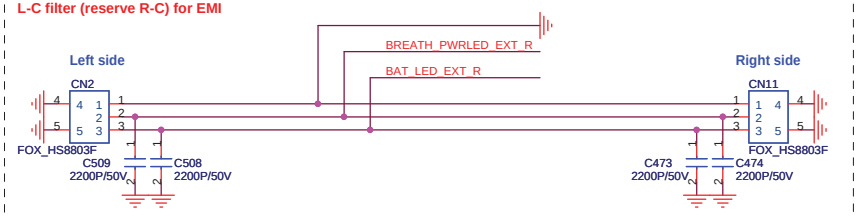
WWAN



Turns On when WWAN radio is on.

Hinge LED (PWR/Battery indictor)

L-C filter (reserve R-C) for EMI

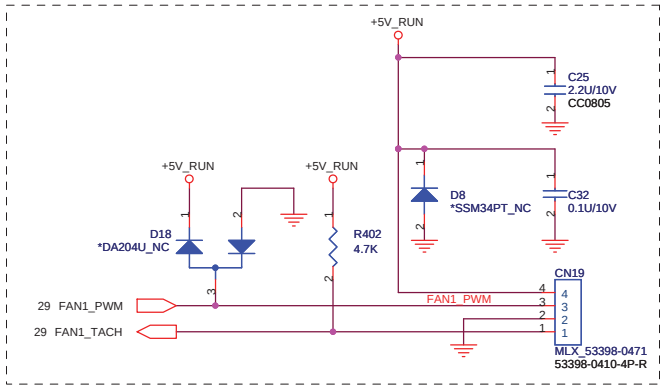


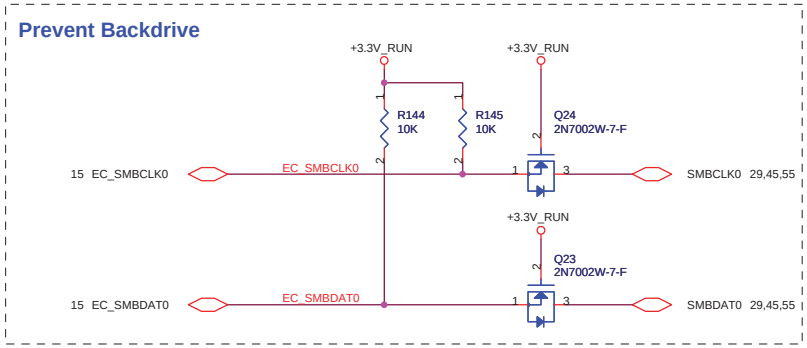
Solid White= System On, Normal Activity
Solid White= Charging (system on);
Solid White= Charging (system off or hibernate and battery charge <90%);
Off= Charging (system off or hibernate and battery charge > 90%);
"Breathing White " = System in Standby (S3);
Off = System Off (or in Hibernate);

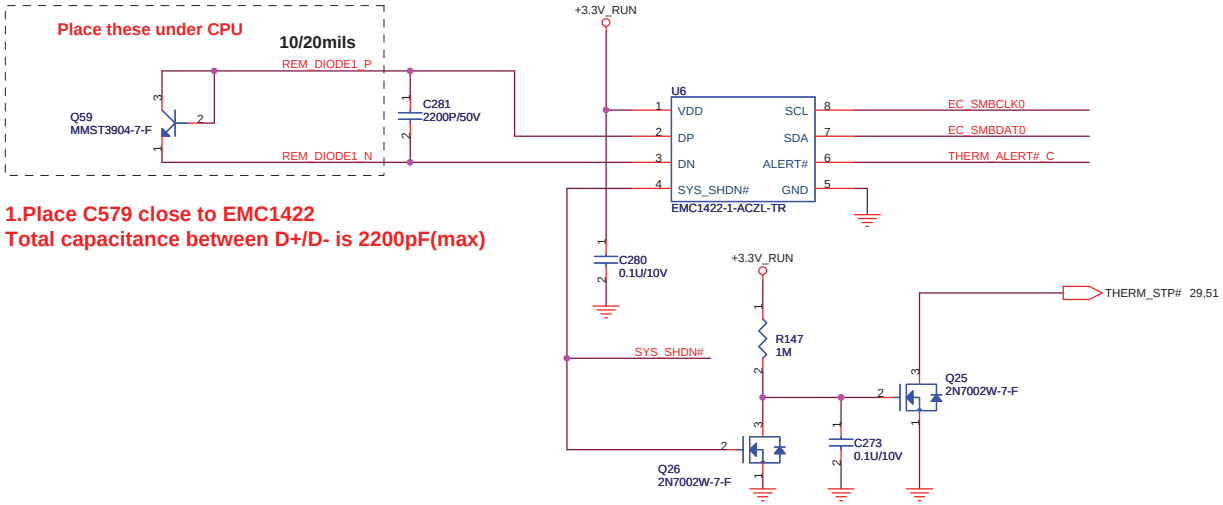
Flashing Amber = Low Battery (S0 and S3 and no AC) when battery charge <10%
Flash rate = on 1/4 sec., off 3/4 sec.

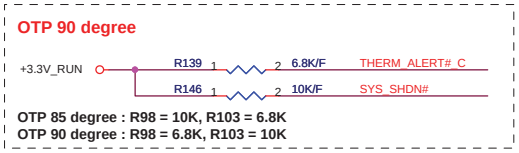
QUANTA COMPUTER

Title	LED	
Size	Document Number RM5	Rev 3A
Date: Friday, August 21, 2009	Sheet 36 of 61	



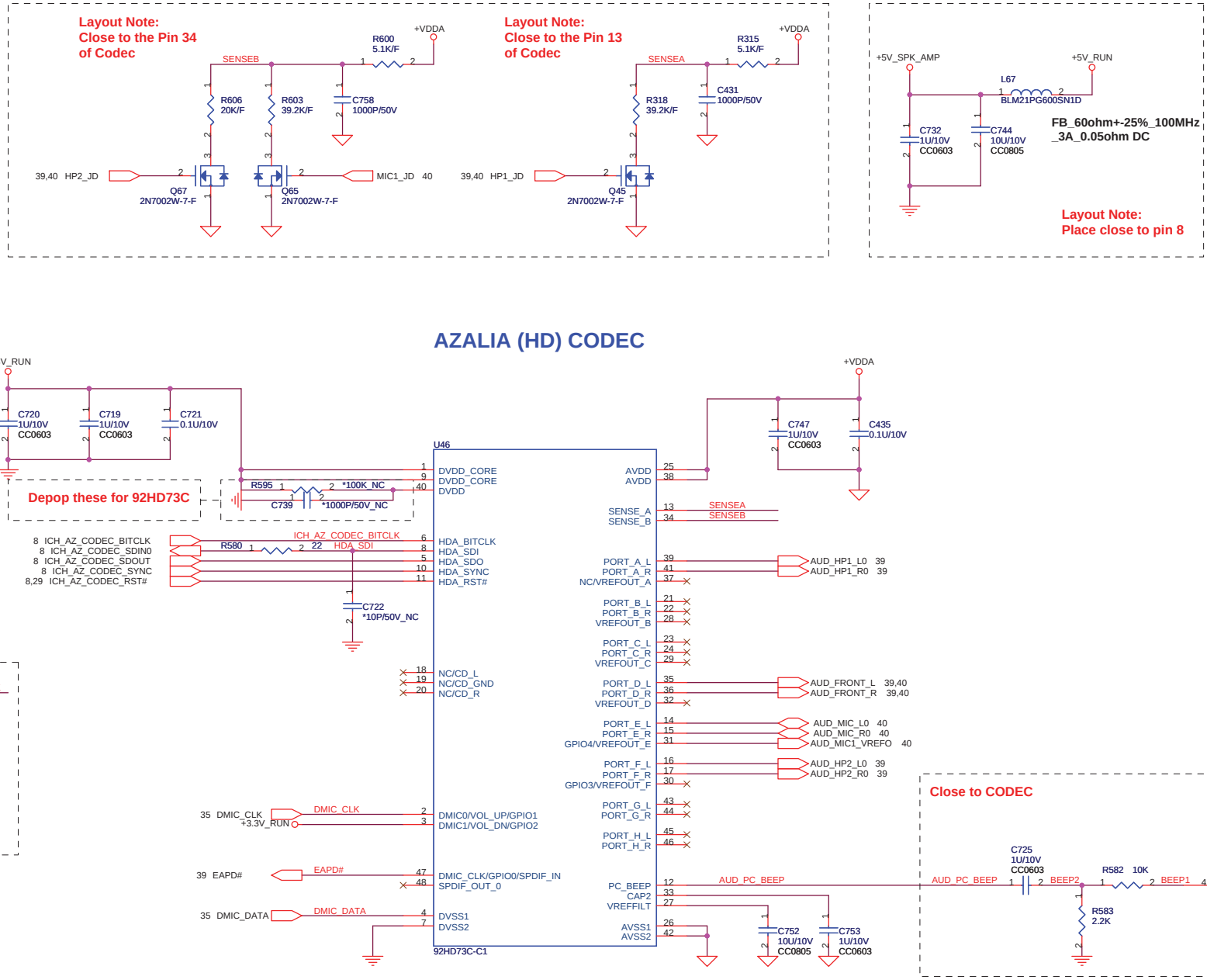






QUANTA COMPUTER

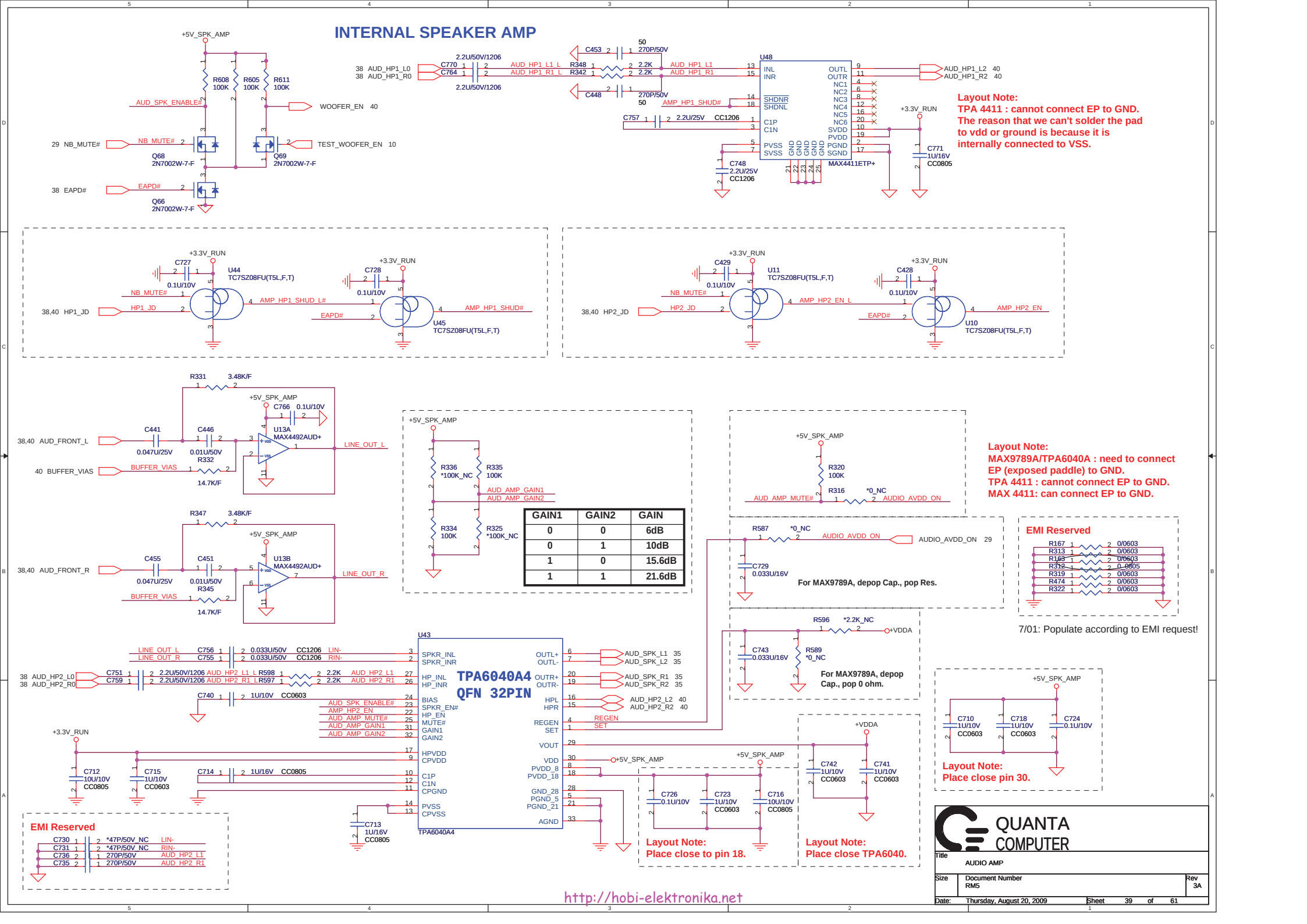
Title	FAN /THERMAL	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 37 of 61	



QUANTA COMPUTER

Title	AZELIA CODEC (92HD73C)	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 38 of 61	

INTERNAL SPEAKER AMP



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QUANTA COMPUTER

Title	AUDIO AMP	
Size	Document Number RM5	Rev 3A
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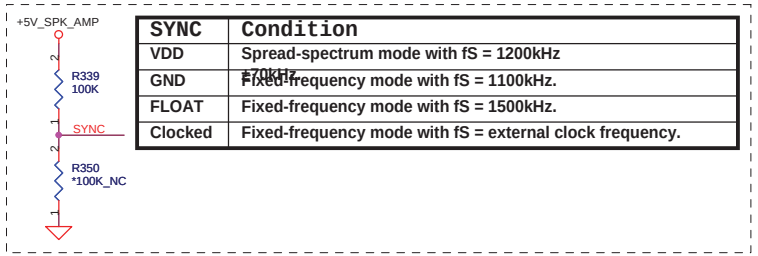
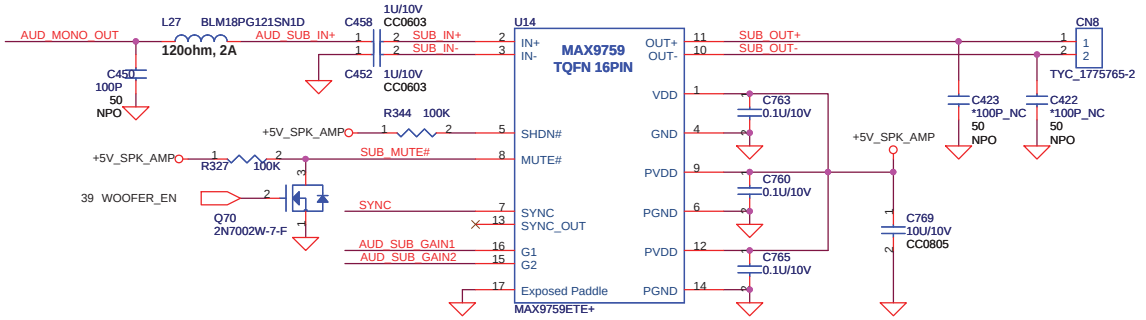
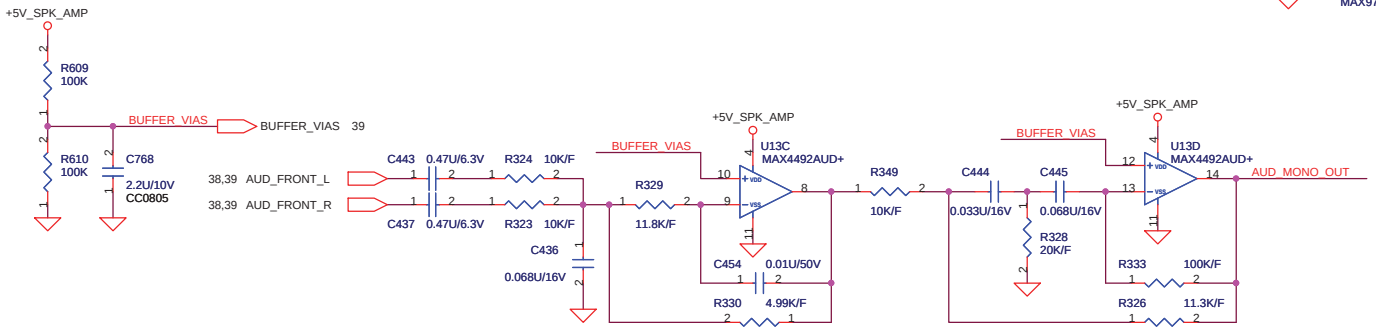
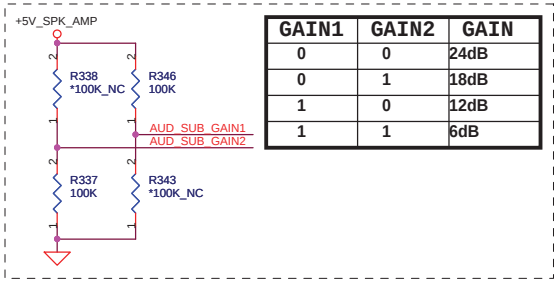
INTERNAL SUBWOOFER AMP



SYNC	Condition
VDD	Spread-spectrum mode with fS = 1200kHz ±70kHz
GND	Fixed-frequency mode with fS = 1100kHz.
FLOAT	Fixed-frequency mode with fS = 1500kHz.
Clocked	Fixed-frequency mode with fS = external clock frequency.

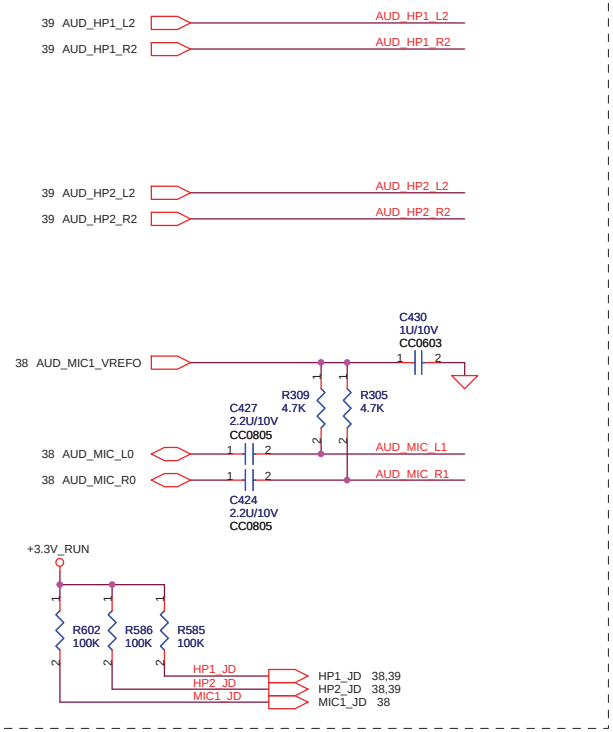




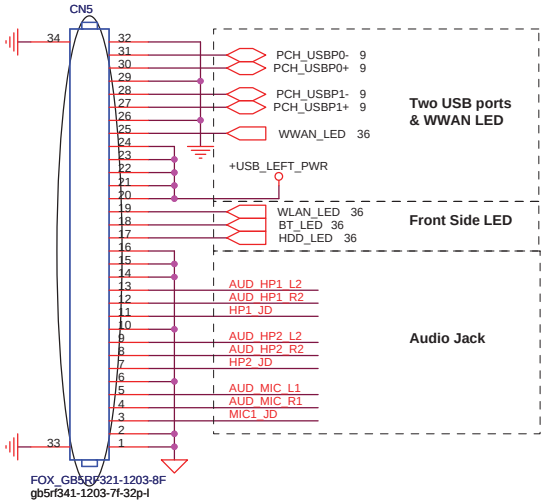


GAIN1	GAIN2	GAIN
0	0	24dB
0	1	18dB
1	0	12dB
1	1	6dB

Ambient Parts of Headphone & MIC Jack

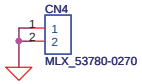


To IB(IO Board) connector



Scott_0123:Change CN5 PN with DFHD32MR003 (FOX).

Adding additional AGND



QUANTA COMPUTER

Title	IB CONN & SUBWOOFER	
Size	Document Number RM5	Rev 3A
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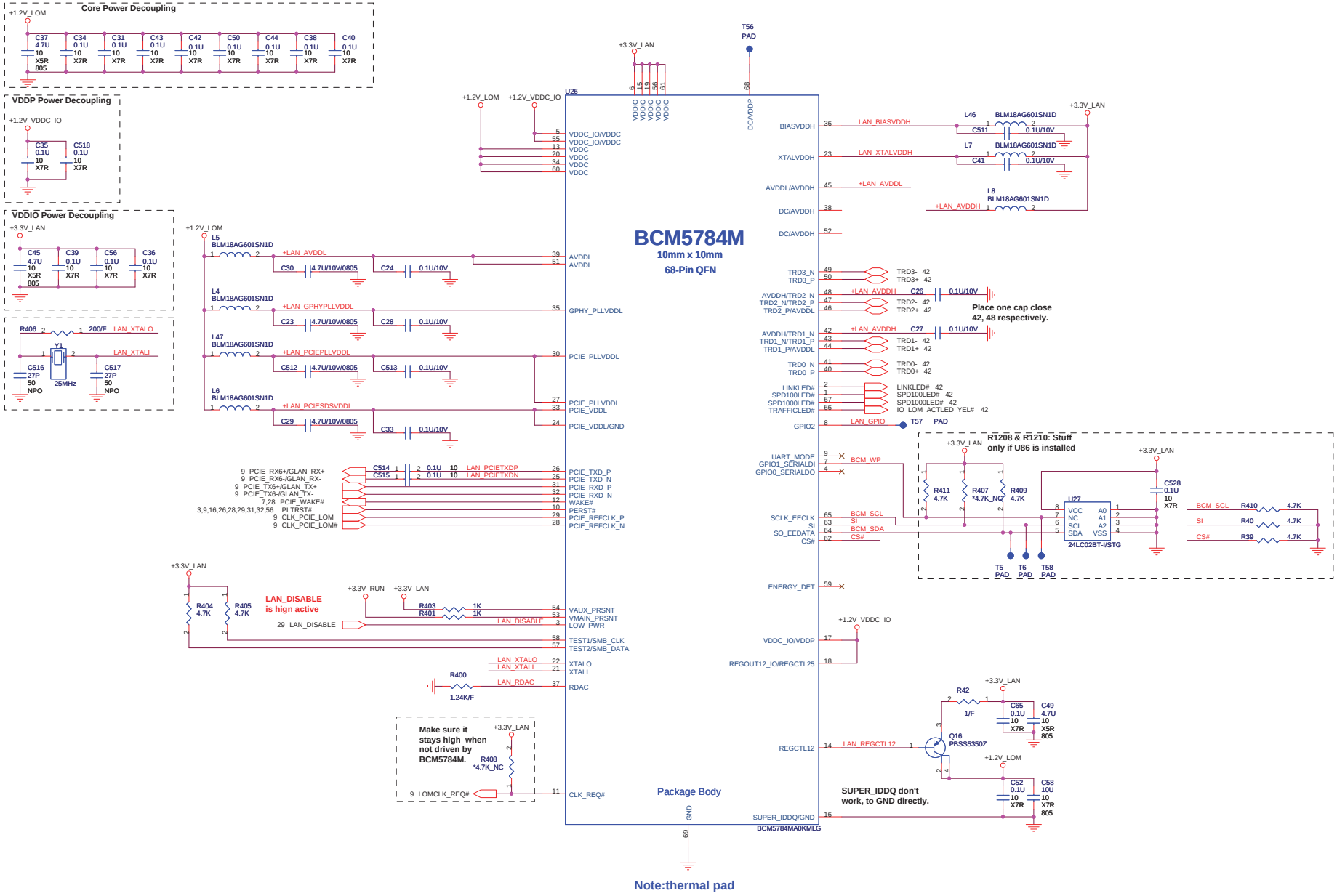

QUANTA COMPUTER

Title	LAN (BCM5784M)	
Size	Document Number RM5	Rev 3A
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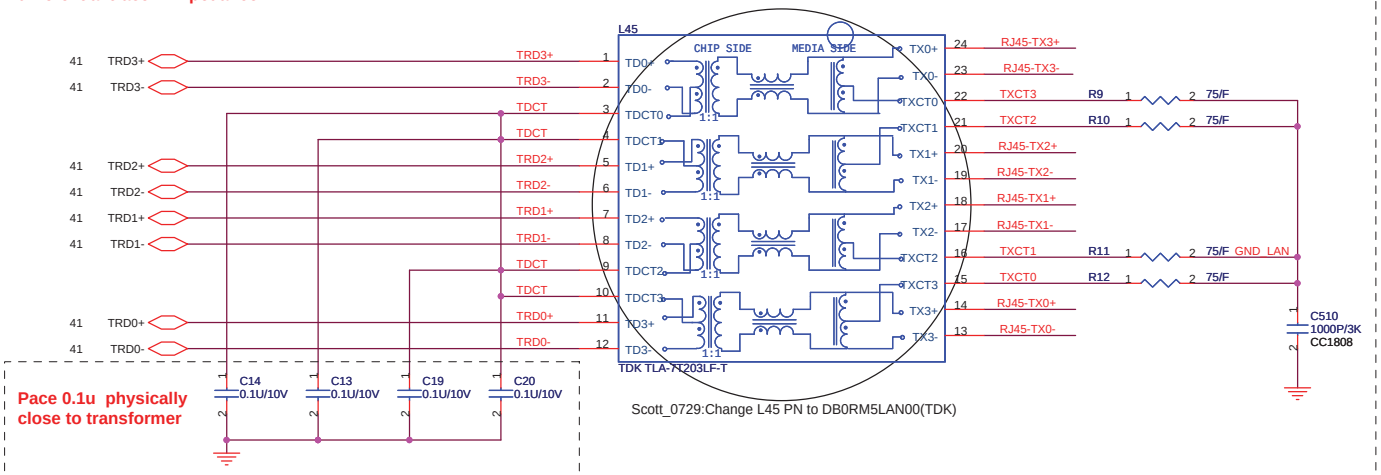
TRANSFORMER

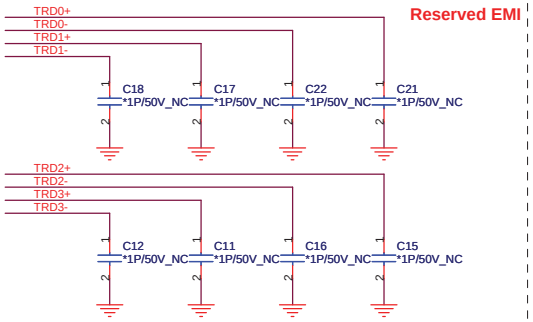
Layout Note:
Route TRD+/- pairs with 100 ohm differential trace immpedance.



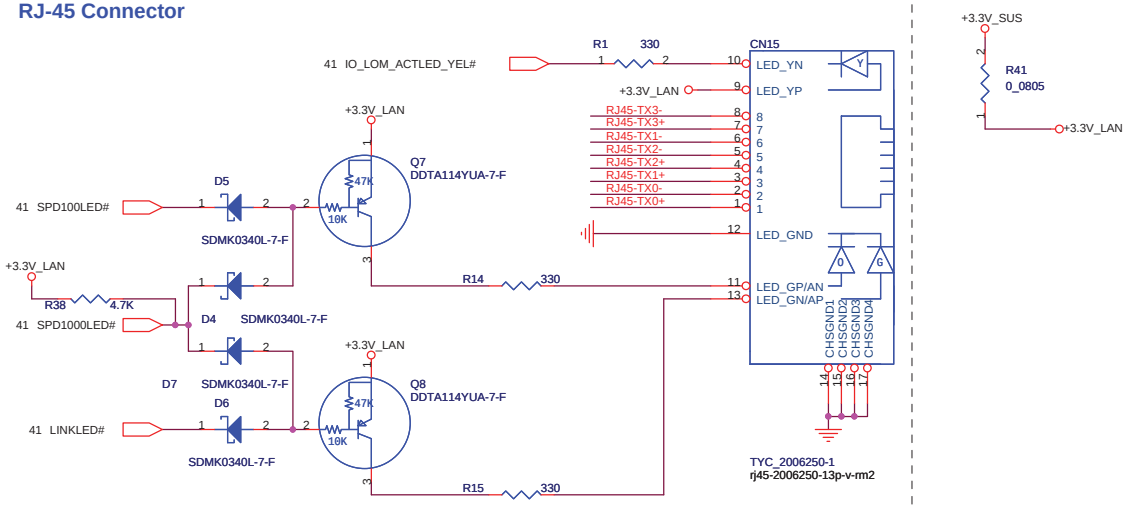
Pace 0.1u physically close to transformer

Scott_0729:Change L45 PN to DB0RM5LAN00(TDK)

Reserved EMI

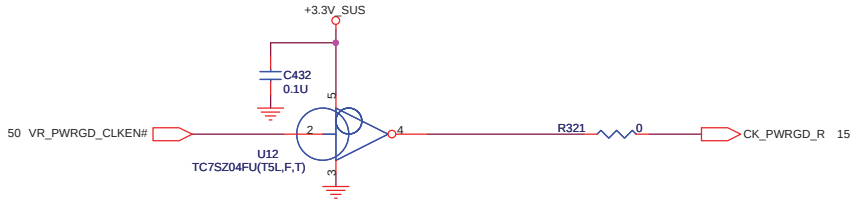


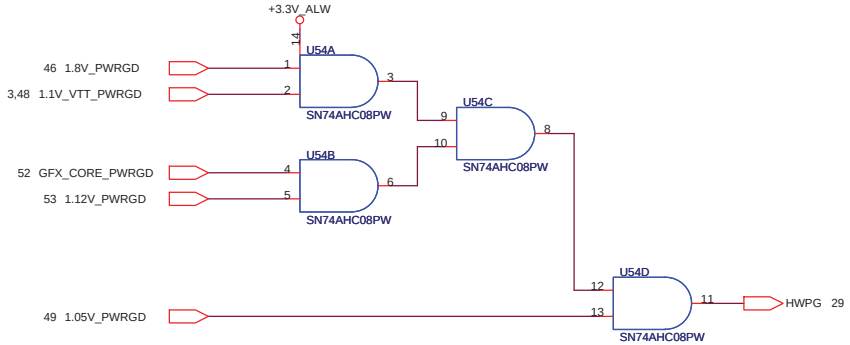
RJ-45 Connector

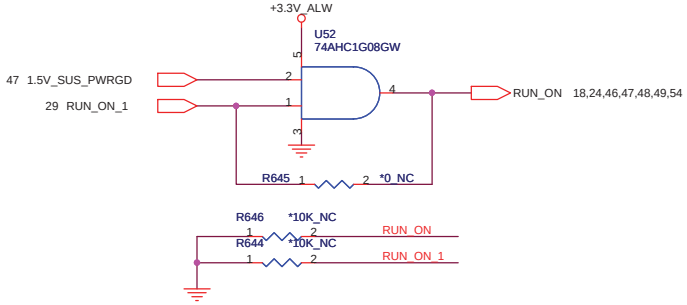


QUANTA COMPUTER

Title	LAN SWITCH	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 42 of 61	



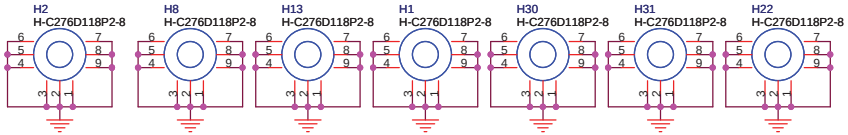




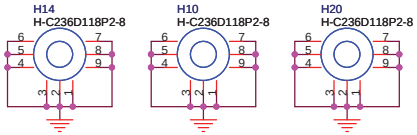
QUANTA COMPUTER

Title	System Reset Circuit	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 43 of 61	

H-C276D118P2-8 * 7

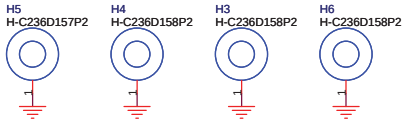


H-C236D118P2-8 * 3

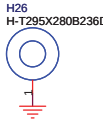


h-c236d197p2 * 1

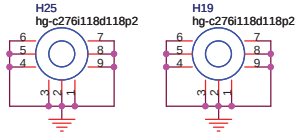
H-C236D158P2 * 4



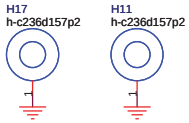
H-T295X280B236D118P2 * 1



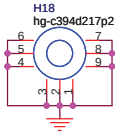
hg-c276i118d118p2 * 2



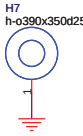
h-c236d157p2 * 2



h-c394d260p2 * 1



H-C394D260P2-8 * 1

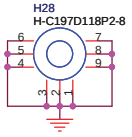


Scott_0731: change H7 & H18 footprint as ME change

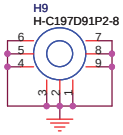
Scott_0812:Delete H7 Pin2~Pin9 for layout requite.

h-c236d236n * 2

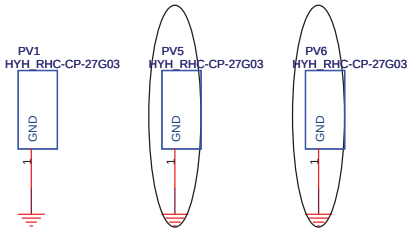
H-C197D118P2-8 * 1



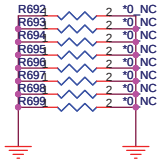
H-C197D91P2-8 * 1



h-o205x157d138x91p2 * 1



Scott_0701:: Added PV6 according to EMI's suggestion



Scott_0703:Add 8pcs 0ohm resistors R692~R699 for thermal issue as EMI concern.

Scott_0707: Reserver R692~R699.

QUANTA COMPUTER

Title	PAD & SCREW & SPRING	
Size	Document Number RM5	Rev 3A
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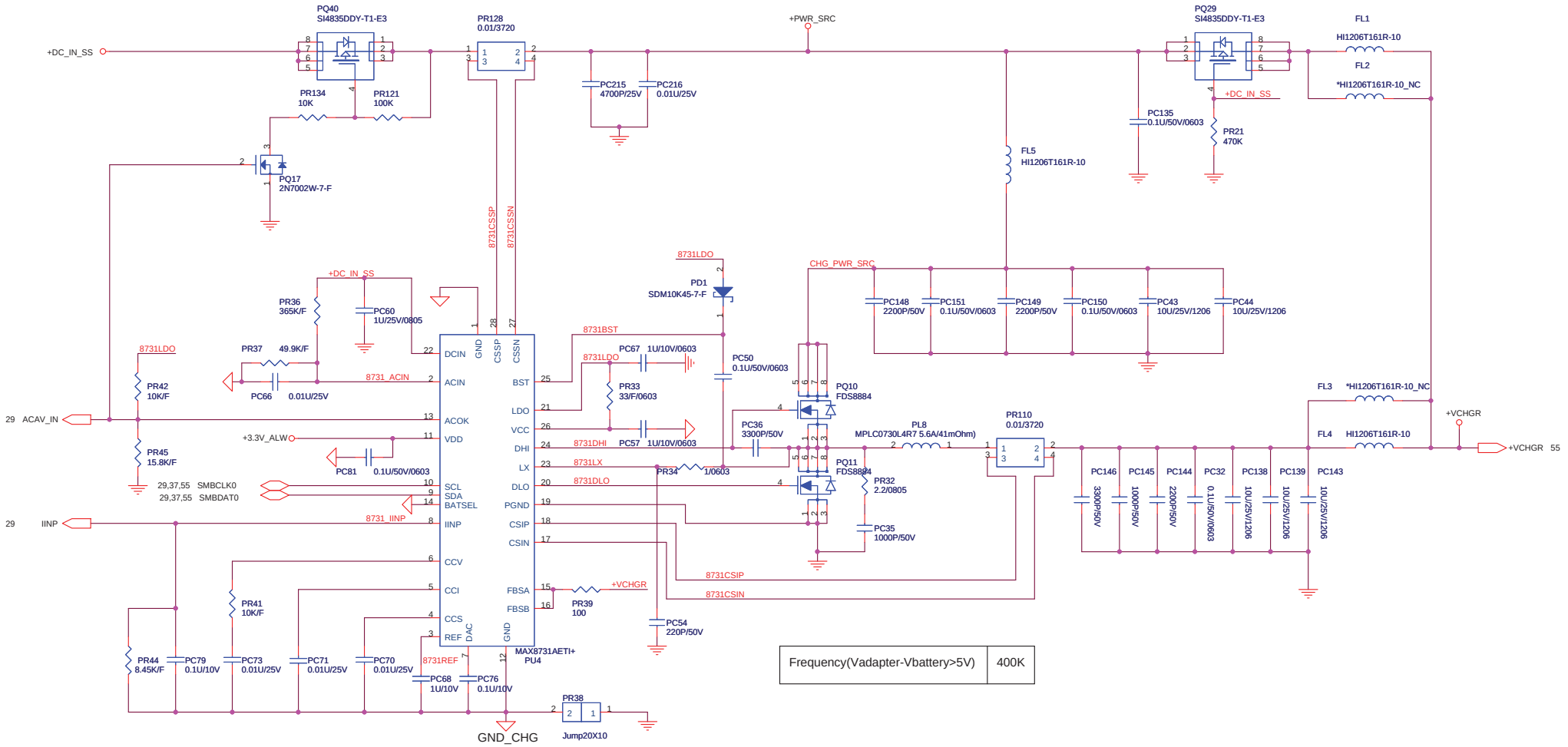
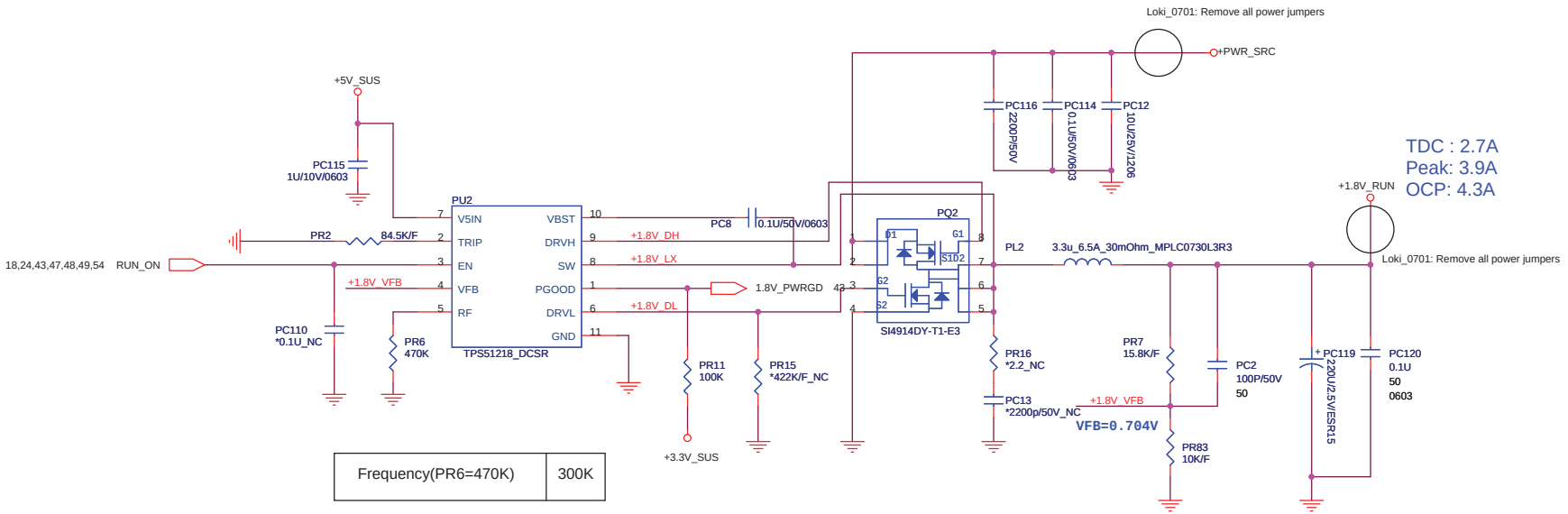


Frequency(Vadapter-Vbattery>5V)	400K

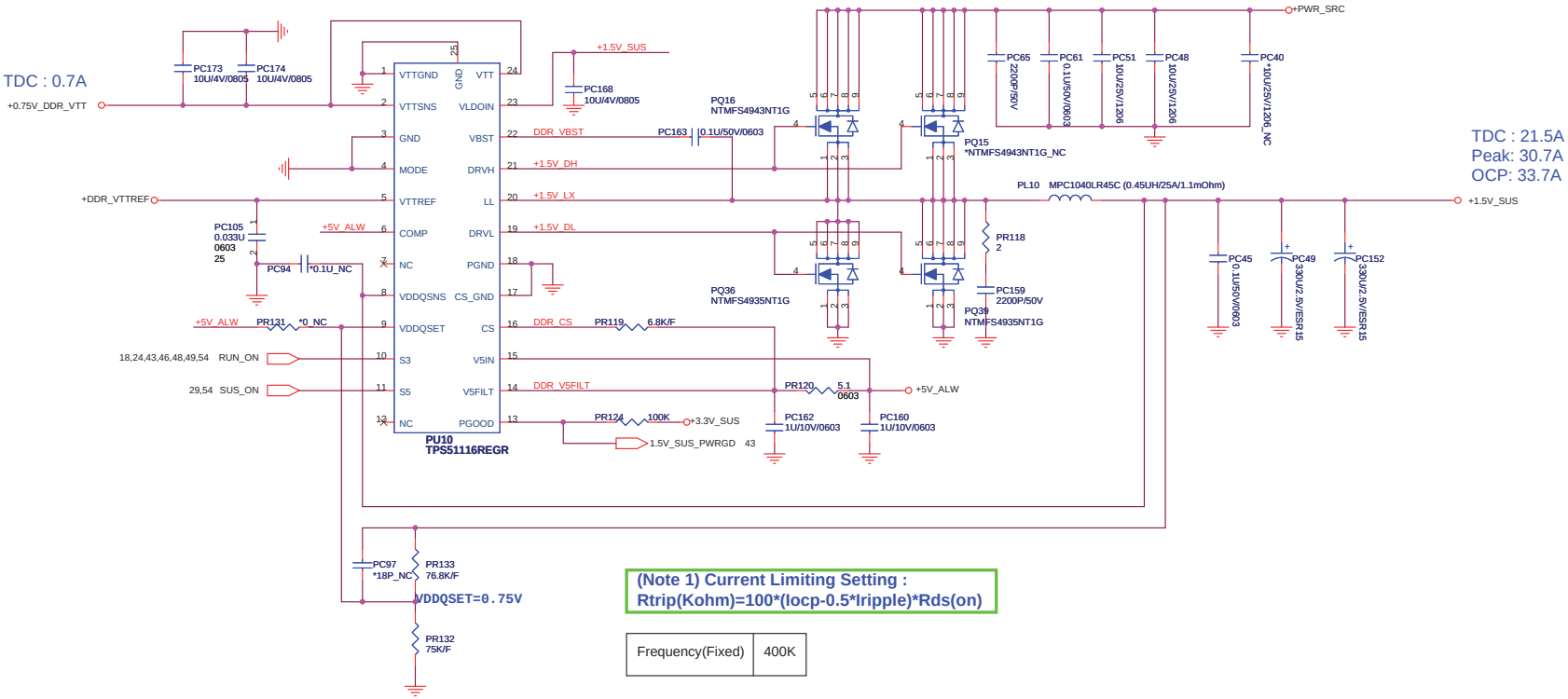
QUANTA COMPUTER

Title	CHARGER (MAX8731A)	
Size	Document Number RM3	Rev 3A
Date:	Sheet 45 of 61	

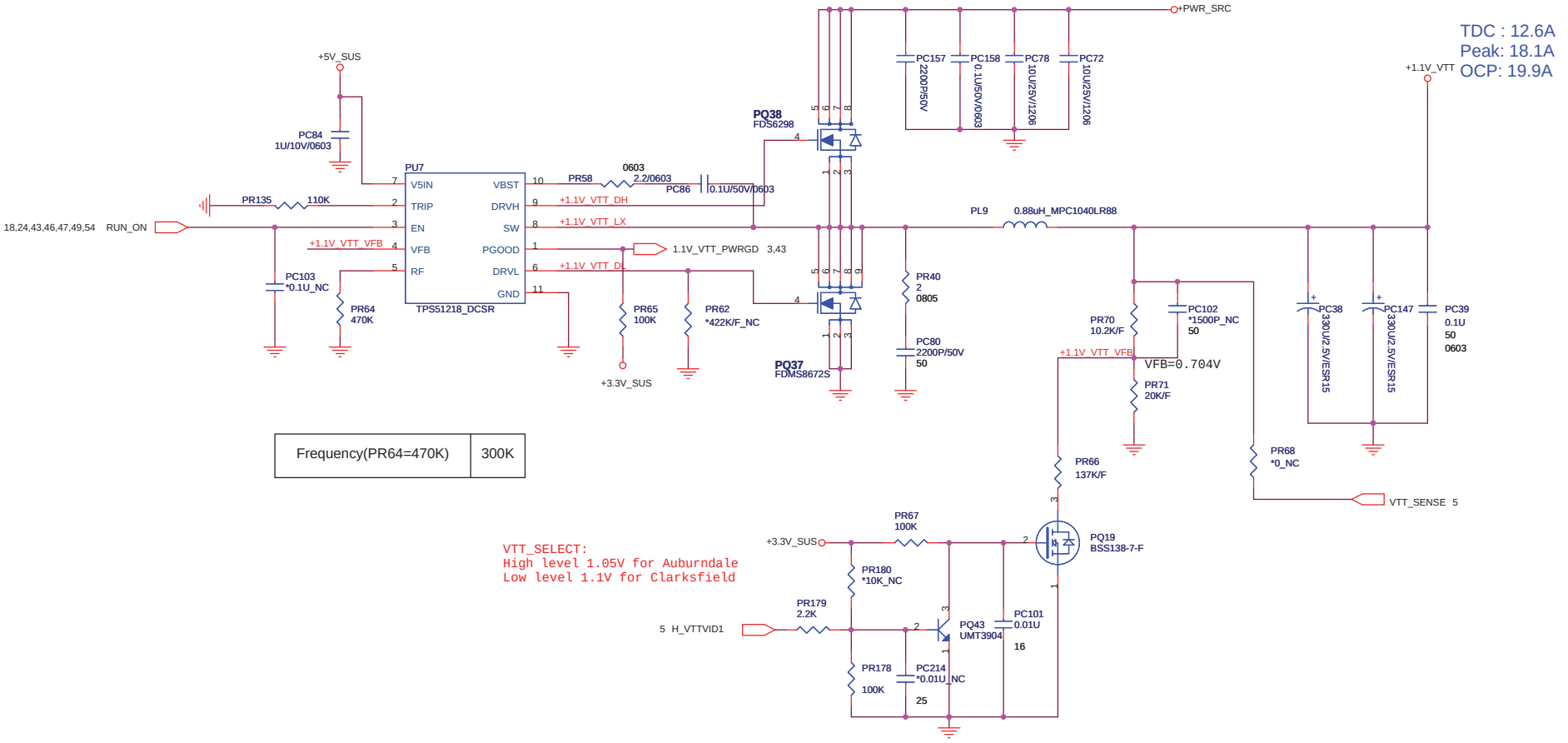
2005/4/21

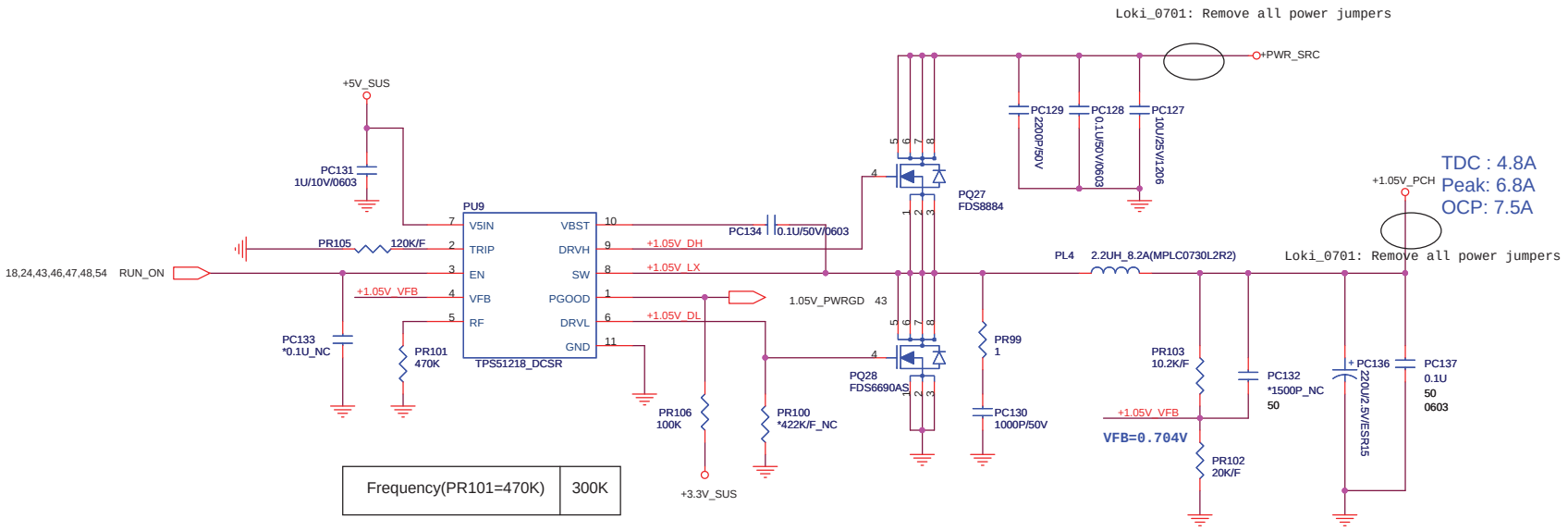


Title	+1.8V_RUN(TPS51218)	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 46 of 61	



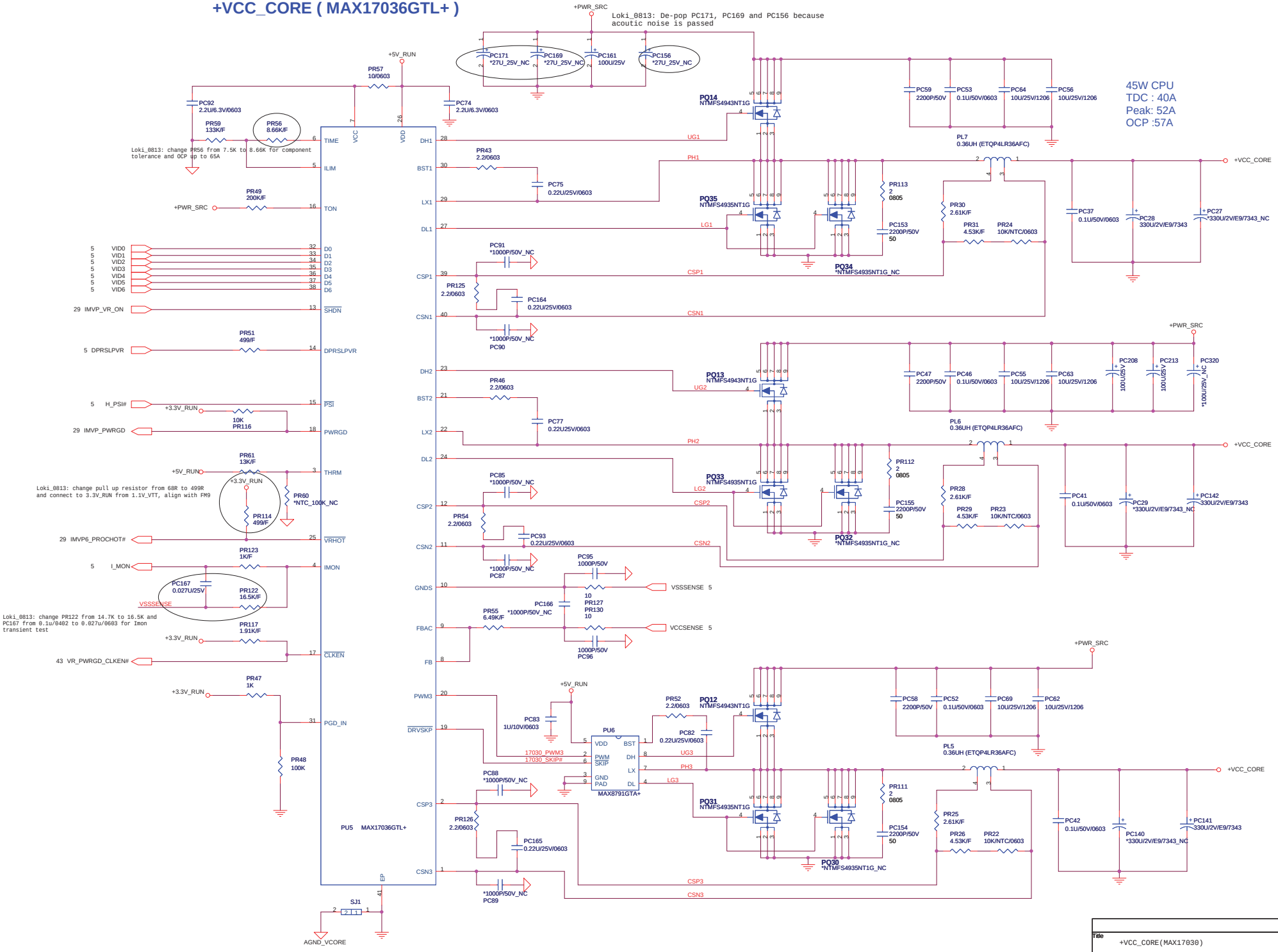
Title	+1.5V_SUS/+0.75V_VTT(TPS51218)	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 47 of 61	





Title	+1.05V_PCH(TPS51218)
Size	Document Number RM5 — Rev 3A
Date:	Thursday, August 20, 2009 — Sheet 49 of 61

+VCC_CORE (MAX17036GTL+)



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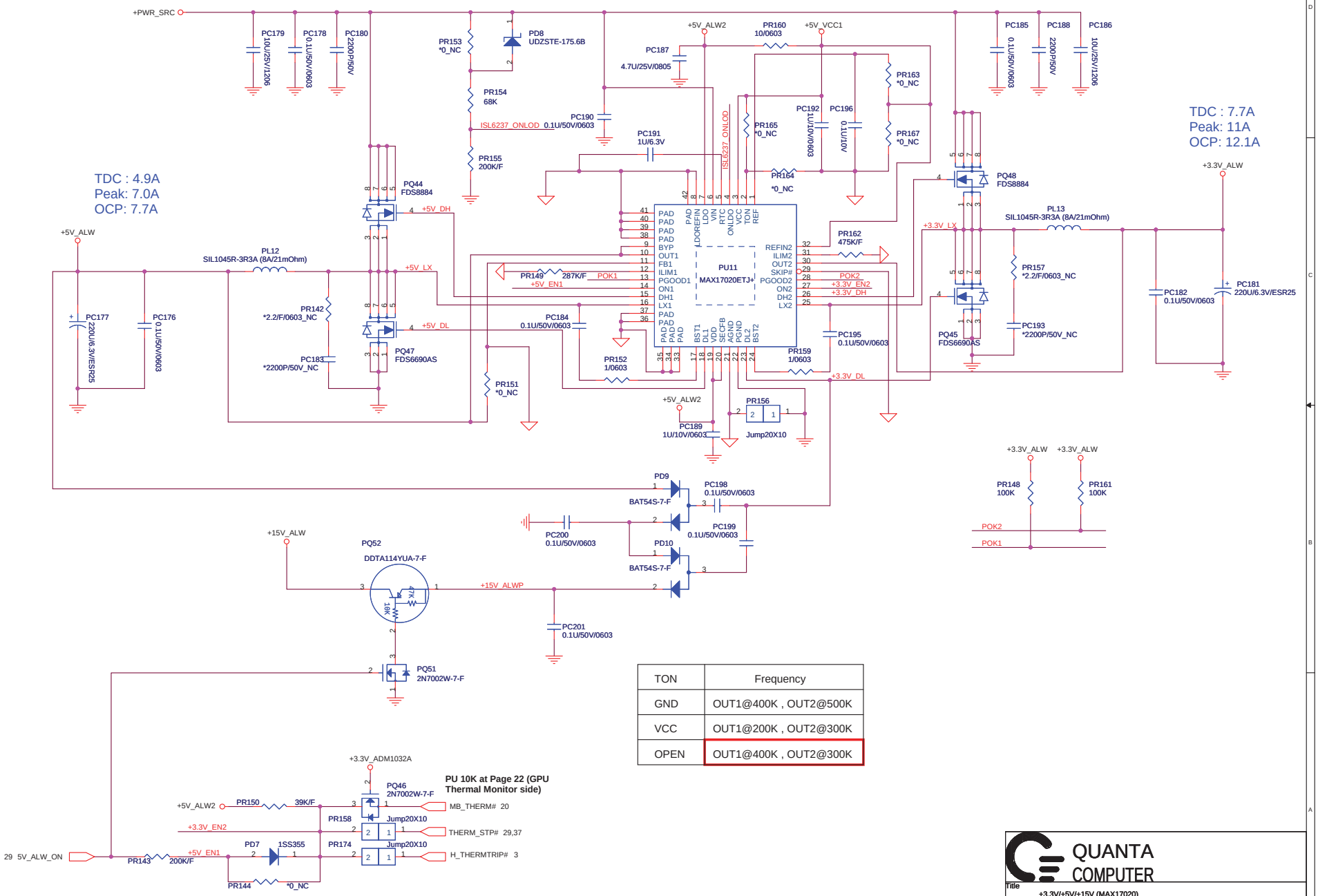
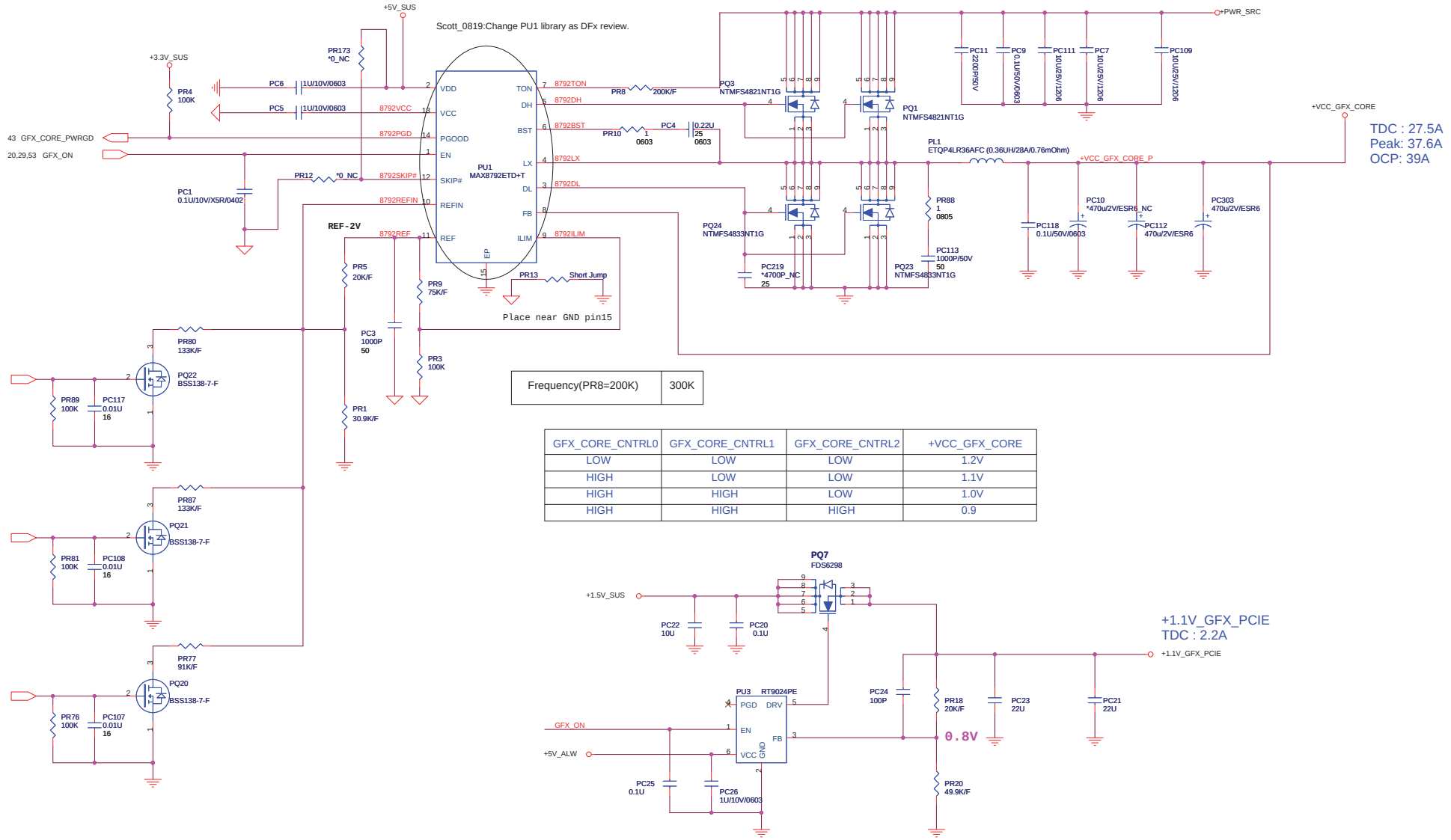
Title	+VCC_CORE(MAX17030)	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 50 of 61	



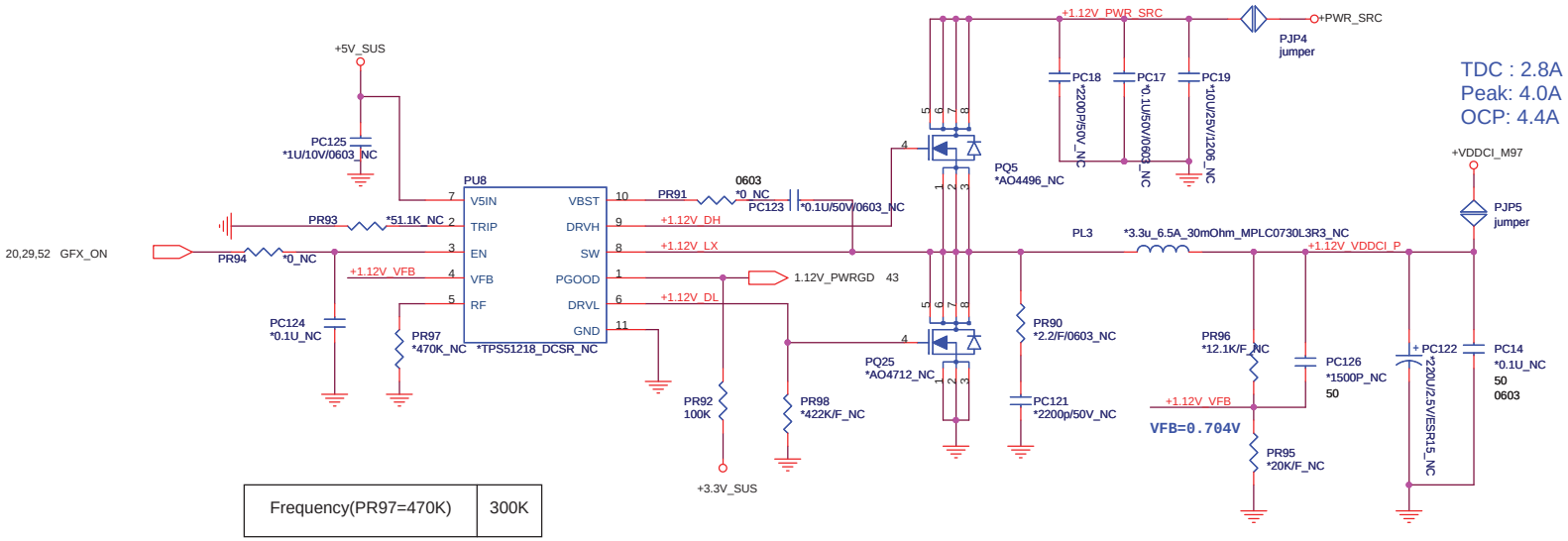
TON	Frequency
GND	OUT1@400K , OUT2@500K
VCC	OUT1@200K , OUT2@300K
OPEN	OUT1@400K , OUT2@300K

QUANTA COMPUTER

Title	+3.3V/+5V/+15V (MAX17020)		
Size	Document Number RM5		Rev 3A
Date:	Thursday, August 20, 2009	Sheet 51 of 61	

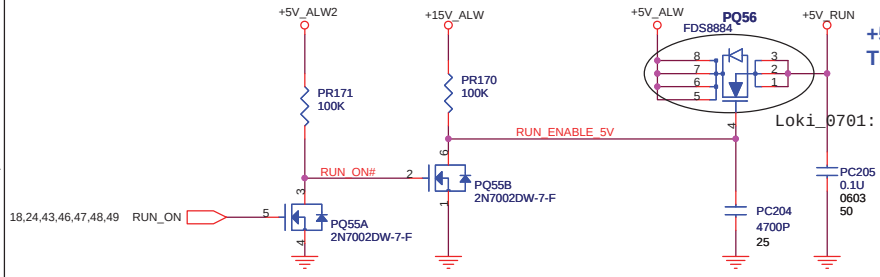


Title	+VGA_M97(MAX8792)		
Size	Document Number RM5		Rev 3A
Date: Thursday, August 20, 2009	Sheet 52 of 61		



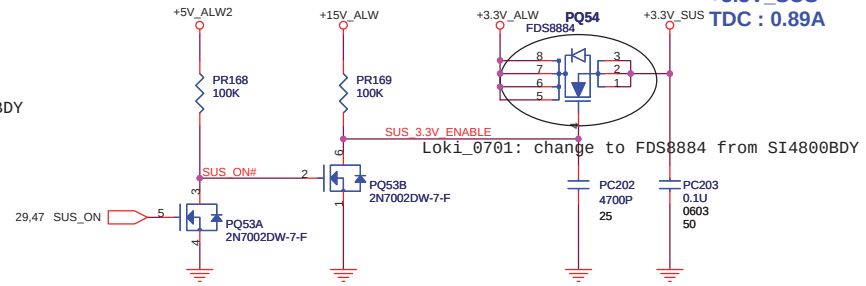
Frequency(PR97=470K)	300K

Title	+VDDCI_M97(TPS51218)	
Size	Document Number RM5	Rev 3A
Date: Thursday, August 20, 2009	Sheet 53 of 61	



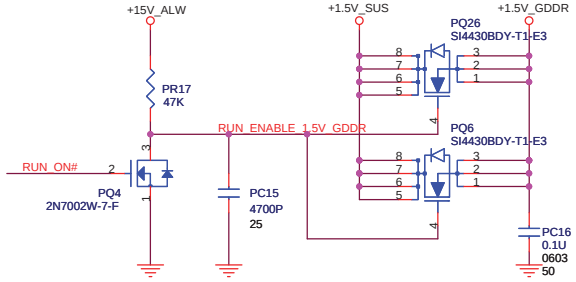
+5V_RUN
TDC :0.791A

Loki_0701: change to FDS8884 from SI4800BDY

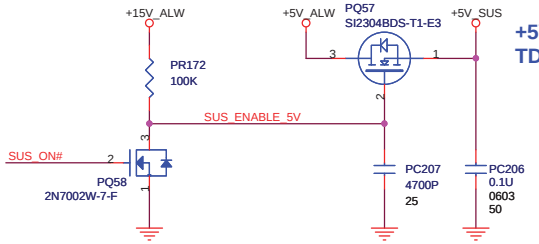


+3.3V_SUS
TDC : 0.89A

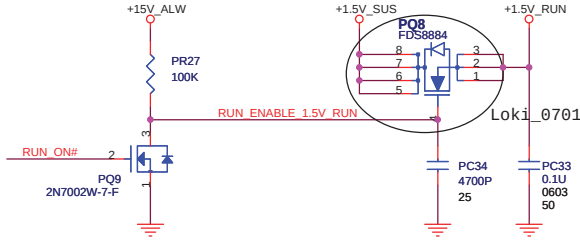
Loki_0701: change to FDS8884 from SI4800BDY



+1.5V_GDDR
TDC : 8.68A

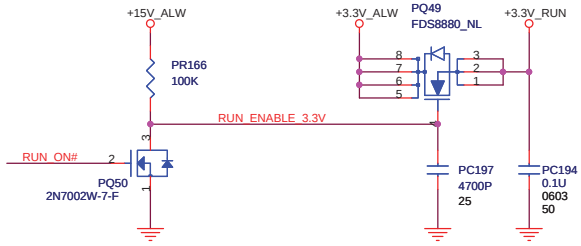


+5V_SUS
TDC : 42mA



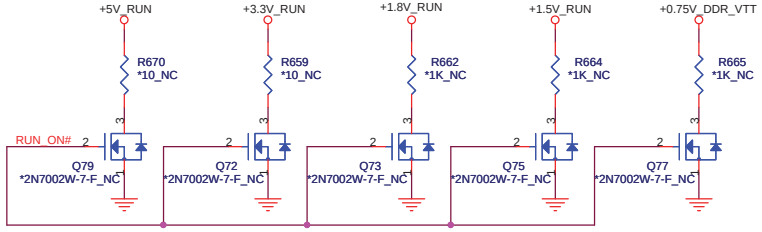
+1.5V_RUN
TDC : 1.05A

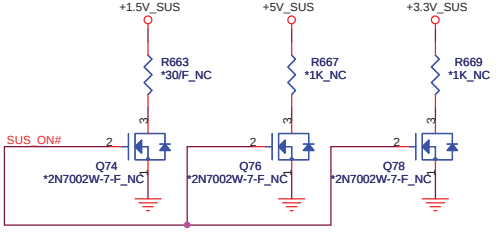
Loki_0701: change to FDS8884 from SI4800BDY



+3.3V_RUN
TDC : 6A

Reserve discharge path





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Title	RUN POWER SW	
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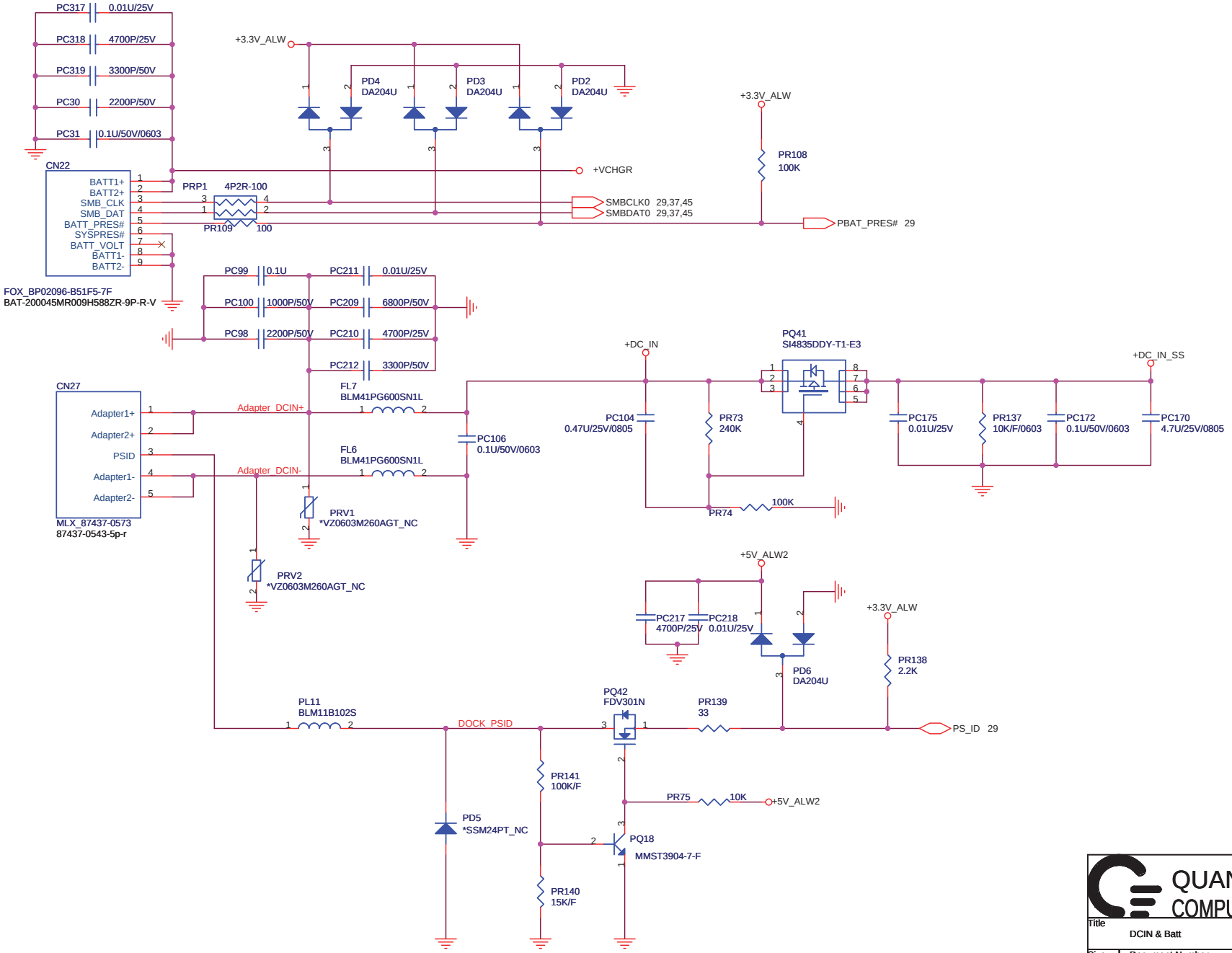

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Title	DCIN & Batt	
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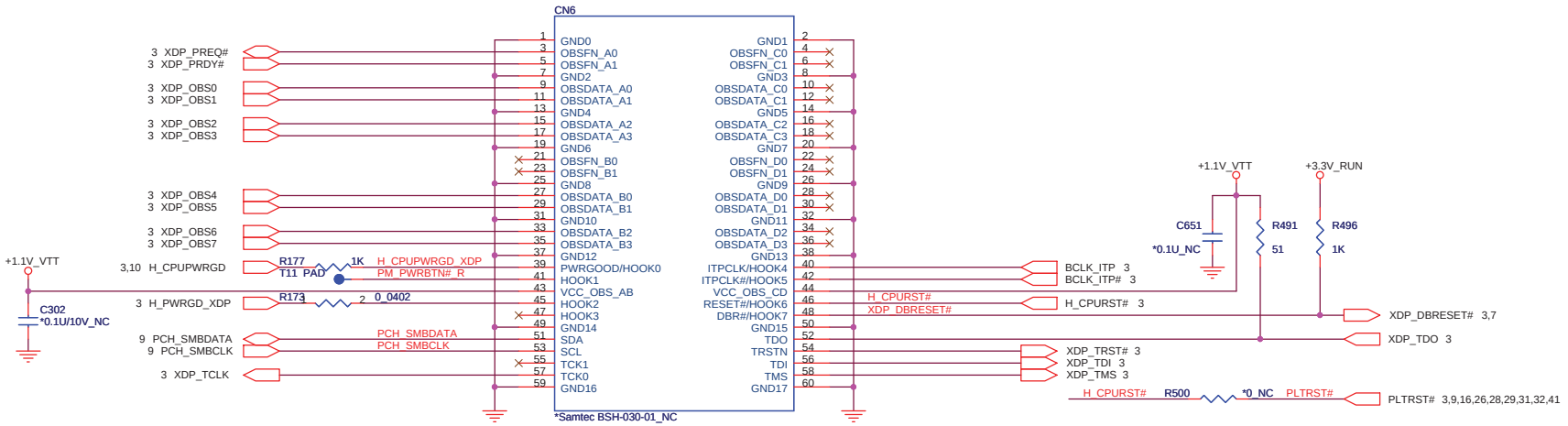
CPU XDP



PCH XDP

DEL PCH XDP as FM9 confirmed with
Intel that its not necessary!

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Title	XDP Connector	
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RM5 Power Design Block Diagram 2009/02/25

(1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
Bat : +VCHGR -> +PWR_SRC
(2) +5V_ALW2, +3.3V_ALW
(3) MAIN_PWR_SW#
(4) 5V_ALW_ON
(5) +5V_ALW -> +15V_ALW
(6) SUS_ON
(7) All SUS power & PWRGD
(8) SIO_PWRBTN#, PCH_RSMRST#
(9) SIO_SLP_S5#, SIO_SLP_S3#
(10) RUN_ON_1, RUN_ON, GFX_RUN_ON
(11) All RUN power & PWRGD
(12) HWPG
(13) IMVP_VR_ON
(14) IMVP_PWRGD
(15) CLK_PWRGD
(16) RESET_OUT#
(17) PCH_PWRGD
(18) H_CPUPWRGD
(19) PLTRST#

Power Jack
Adapter input
+DC_IN (1)
SI4835
+DC_IN_SS (1)
SI4835
+PWR_SRC (1)
Charger
MAX8731A
Page 45
+VCHGR (1)
Battery
SI4835
+PWR_SRC (1)

+5V_VCC1 (from +5V_ALW2)
SYSTEM POWER
MAX17020
Page 51
LDO
VR
+5V_ALW2 (2)
+3.3V_ALW (2)
+5V_ALW (5)
POK2 (+3.3V_ALW)
POK1 (+5V_ALW)
(2) +5V_ALW2(for +3.3V_ALW)
(4) 5V_ALW_ON
+5V_ALW
Diode & Cap
Page 51
+15V_ALW (5)

+5V_SUS
PCH CORE POWER
TPS51218
Page 49
VR
+1.05V_PCH (11)
1.05V_PWRGD (11)
(10) RUN_ON

+5V_SUS
VGA POWER
MAX8792ETD+
Page 52
VR
+VCC_GFX_CORE (11)
GFX_CORE_PWRGD (11)
(10) GFX_RUN_ON

+5V_ALW
DDR POWER
TPS51116
Page 47
VR
LDO
+1.5V_SUS (7)
1.5V_SUS_PWRGD (7)
+0.75V_DDR_VTT (11)
(6) SUS_ON
(10) RUN_ON

+5V_SUS
Graphics
TPS51218
Page 53
VR
+VDDCI (11)
1.12V_PWRGD (11)
(10) GFX_RUN_ON

+5V_SUS
CPU Mem Control
TPS51218
Page 48
VR
+1.1V_VTT (11)
1.1V_VTT_PWRGD (11)
(10) RUN_ON

+5V_SUS
Graphics
TPS51218
Page 46
VR
+1.8V_RUN (11)
1.8V_PWRGD (11)
(10) RUN_ON

+5V_RUN
+3.3V_RUN
CPU POWER
MAX17030
TWO PHASE SOLUTION
Page 50
VR
+VCC_CORE (15)
IMVP_PWRGD (15)
(14) IMVP_VR_ON

(5) +5V_ALW
S12304
Page 54
+5V_SUS (7)
(6) SUS_ON

(2) +3.3V_ALW
SI4800
Page 54
+3.3V_SUS (7)
(6) SUS_ON

(5) +5V_ALW
SI4800
Page 54
+5V_RUN (11)
(10) RUN_ON

(2) +3.3V_ALW
FDS8880
Page 54
+3.3V_RUN (11)
(10) RUN_ON

(7) +1.5V_SUS
SI4430
Page 54
+1.5V_GDDR (11)
(10) RUN_ON

(7) +1.5V_SUS
SI4430
Page 54
+1.5V_RUN (11)
(10) RUN_ON

Reset Circuit
Page 43
(7) 1.5V_SUS_PWRGD
(10) RUN_ON_1
(7) 1.8V_PWRGD
(11) 1.1V_VTT_PWRGD
(11) 1.12V_PWRGD
(11) GFX_CORE_PWRGD
(11) 1.05V_PWRGD
(14) IMVP_PWRGD
(16) RESET_OUT#
74AHC1G08GW
RUN_ON (10)
SN74AHC08PW
HWPG (12)
74AHC1G08GW
PCH_PWRGD (17)

(3) MAIN_PWR_SW#
EC
IT8512
Page 31
5V_ALW_ON (4)
SUS_ON (6)
SIO_PWRBTN# (8)
PCH_RSMRST# (8)
SIO_SLP_S5# (9)
SIO_SLP_S3# (9)
RUN_ON_1 (10)
IMVP_VR_ON (13)
RESET_OUT# (16)
(12) HWPG
(14) IMVP_PWRGD

(17) PCH_PWRGD
PCH
Page 11~14
CLK_PWRGD (15)
CLK GEN
Page 17
H_CPUPWRGD (18)
PLTRST# (19)
CPU
Page 3~4

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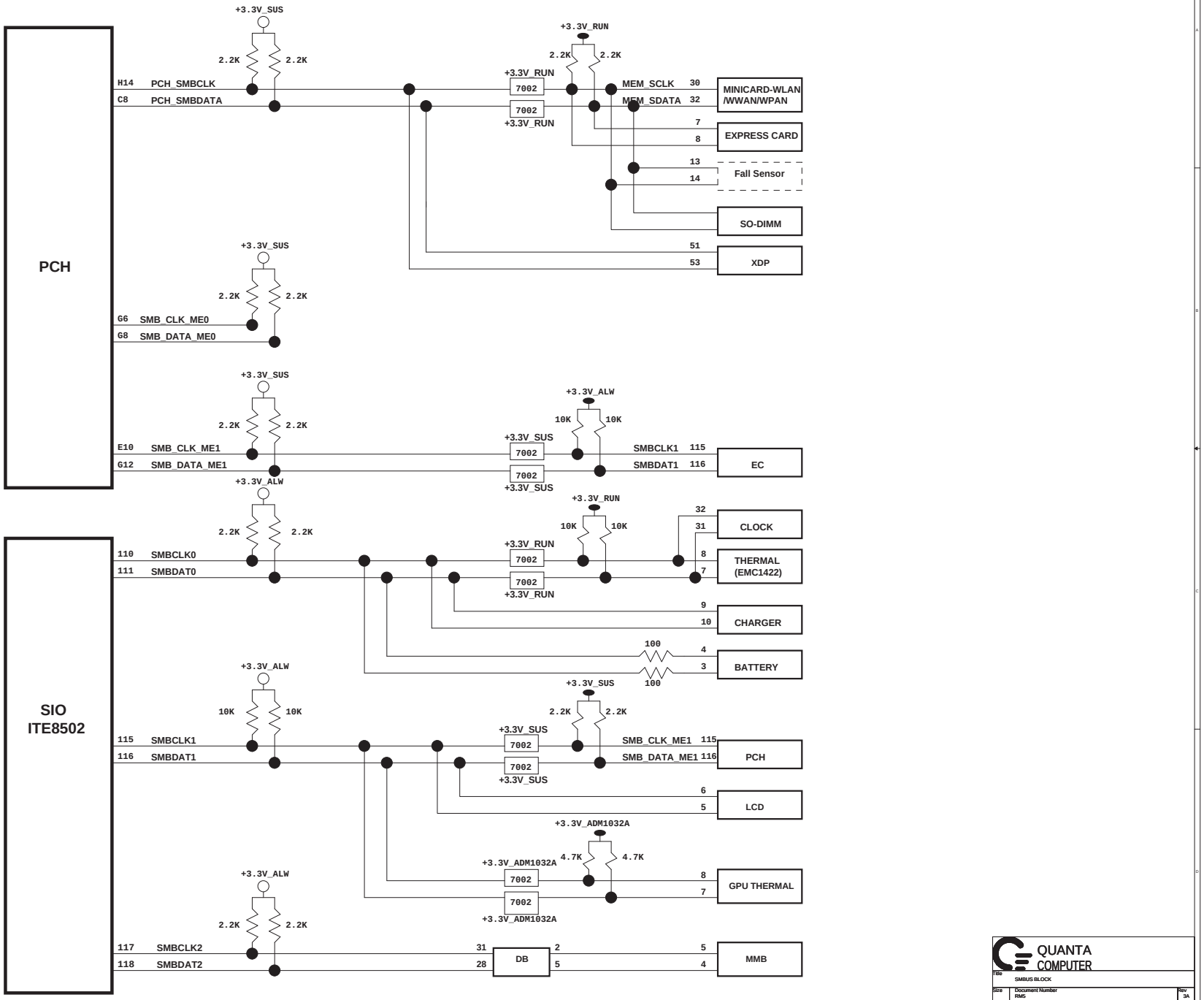

QUANTA COMPUTER

Title	SMBUS BLOCK		
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POWER STATES

State \ Signal	SLP_S3#	SLP_S4#	SLP_S5#	S4_STATE#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	N/A	HIGH	N/A	ON	ON	ON	ON
S3 (Suspend to RAM) / M-OFF	LOW	N/A	HIGH	N/A	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	N/A	HIGH	N/A	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	N/A	LOW	N/A	ON	OFF	OFF	OFF

PM TABLE

power plane / State	+RTC_CELL	+DC_IN +DC_IN_SS +PWR_SRC +CPU_PWR_SRC +5V_ALW2 +MMB_PWR +3.3V_ALW	+5V_ALW +15V_ALW +5V_SUS +3.3V_SUS +3.3V_LAN +3.3V_CARDAUX +1.8V_SUS +1.5V_SUS	+VCC_CORE +0.75V_DDR_VTT +1.05V_PCH +1.1V_GFX_PCIE +1.2V_LOM +1.5V_RUN +1.5V_CARD +1.8V_RUN +3.3V_RUN +3.3V_DELAY +3.3V_R5C833	+3.3V_RUN_CARD +3.3V_CARD +5V_RUN +LCDVCC +5V_HDD +5V_MOD +5V_SPK_AMP +VDDA +GFX_PWR_SRC
S0	ON	ON	ON	ON	
S3	ON	ON	ON	OFF	
S5 & S4 with AC or BAT	ON	ON	OFF	OFF	
no AC/Battery	ON	OFF	OFF	OFF	

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
NONE			

PCH IBEX PEAK-M	USB PORT#	DESTINATION
	0	Side pair Top / left
	1	Side pair Bottom / left
	2	USB W/ E-SATA port
	3	Reserved
	4	Mini Card (WLAN)
	5	Mini Card (WWAN)
	6	Reserved
	7	Reserved
	8	Mini Card (WPAN)
	9	TV
	10	Express Card
	11	Camera

PCH IBEX PEAK-M	PCI EXPRESS	DESTINATION
	Lane 1	Mini Card-1 WWAN
	Lane 2	Mini Card-2 WLAN
	Lane 3	Mini Card-3 WPAN
	Lane 4	Express Card
	Lane 5	Cardreader
	Lane 6	LOM

QUANTA COMPUTER

Title	Power statu	
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