Page	Title of schematic page	Rev.	Date
01	Page List	1A	
02	Block Diagram	1A	
03	Change List	1A	
04	SNB 1/4(HOST&PCIE)	1A	
05	SNB 2/4(DDR3 I/F)	1A	
06	SNB 3/4(POWER)	1A	
07	SNB 4/4(GND/Strap)	1A	
08	PCH 1/6(DMI/FDI/VIDEO)	1A	
09	PCH 2/6(SATA/RTC/HDA/LPC)	1A	
10	PCH 3/6(PCIE/USB/CLK/NV)	1A	
11	PCH 4/6(GPIO/CPU/STRAP)	1A	
12	PCH 5/6(POWER)	1A	
13	PCH 6/6 (GND)	1A	
14	DDR3 DIMM-0-STD	1A	
15	DDR3 DIMM-1-STD	1A	
16	WPCE791L & FLASH	1A	
17	CRT/LVDS/CAMERA	1A	
18	CARD READER(RTS5209)	1A	
19	HDMI Conn/BT/THERMAL	1A	
20	USB/TP/FAN	1A	
21	LAN (RTL8111E)	1A	
22	WLAN/HOLE	1A	
23	HDD/ODD/EMI	1A	
24	Audio CX20671	1A	
25	LED/RF/KB/PS	1A	
26	POWER +VCC_CORE (ISL95831)	1A	
27	POWER 3VPCU&5VPCU(PM6686)	1A	
28	POWER 1.5VSUS/VTT_MEM	1A	
29	POWER +1.05V(UP6128A)-15A	1A	
30	POWER +0.85V(APE8858)-6A	1A	
31	POWER VGA_CORE(OZ8111)--15A	1A	
32	POWER VCC1.8/Thermal	1A	
33	POWER(ADAPTER IN / CONN)	1A	
34	POWER CHARGER (ISL88731C)	1A	
35	NVIDIA GS2-64 PCIE&PW 1/4	1A	
36	NVIDIA GS2-64 TMDS&DAC 2/4	1A	
37	NVIDIA GS2-64 VRAM 3/4	1A	
38	NVIDIA GS2-64 VRAM 4/4	1A	
39	IO PORT LIST	1A	

* : No mount
E@ : For DIS GFX only
I@ : For INT GFX only

HK1 BLOCK DIAGRAM

DDR III — Dual Channel
P14~P15 — 1066/1333 MHz

intel
SandyBridge
PCI-E X16
DDR SYSTEM MEMORY
rPGA 988
(37.5mm X 37.5mm)
FDI
DMI
P4~P7

PCIE — 5GT/s

NVIDIA
N12M-GS2/N12P-GV
Package type : GB1b-64
P35 ~ P38

VRAM
1GB / 512MB
P37 ~ P38

2.7GT/s FDI
DMI X4 5GT/s

intel
<PCH>
FDI
DMI
SATA Gen3
SATA Gen2
iGFX
Interfaces
HDA
SPI
mBGA 989
(25mm X 25mm)
P6~P11

CougarPoint 0.7
USB

P21 HDD SATA0

P21 ODD SATA3

Bluetooth P19
PORT5

Camera P17
PORT4

WiMax P22
PORT9

USB I/O P20
PORT0

USB I/O P20
PORT1

USB I/O P20
PORT2

USB I/O P20
PORT3

USB 2.0

INT_CRT
P17

INT_LVDS
P17

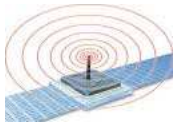
INT_HDMI
P19

5GT/s PCI-Express Gen2
PCIE6
PCIE1
PCIE4

Giga-LAN
RTL8111E
P21

RJ45

P21



WLAN/Widi/BT P22
BT Combo : Atheros WB195
WiMAX : Kelsey Peak KSP(612BNXHWG)
802.11bgn/Intel/KsP_1x2_BD

Card Reader
RTS5209
P18

MS
SD-XC

Audio CODEC
CX20671
P24

Azalia

HP Jack
MIC Jack
SPK
DMIC

P24

P24

P24

P24

SPI ROM
4MB
P9

SPI ROM
2MB

LPC

EC
NPCE791L/NPCE795L
P16

Wireless Switch
P25

Touch Pad
P20

Keyboard
P25

Power LED
Sleep LED
SATA LED
Battery LED
RF LED
SCROLED
CAPSLED
NUMLED
CARD LED

Button
QWA#
VAIO#
ASSIST#
Power SW

Note:
HM65 does not support USB 6 & 7
HM65 does not support SATA 2 & 3

Change List from PVT to MP

HK1_MB_SCH_PVT_001

P19-- R345 change to 48.7K.

Reason : Change thermal sensor temperature to 55 degree.
Possible Risk: No.

P19-- R208 change to 27.4K for UMA.

Reason : Change thermal sensor temperature to 82 degree.
Possible Risk: No.

HK1_MB_SCH_PVT_002

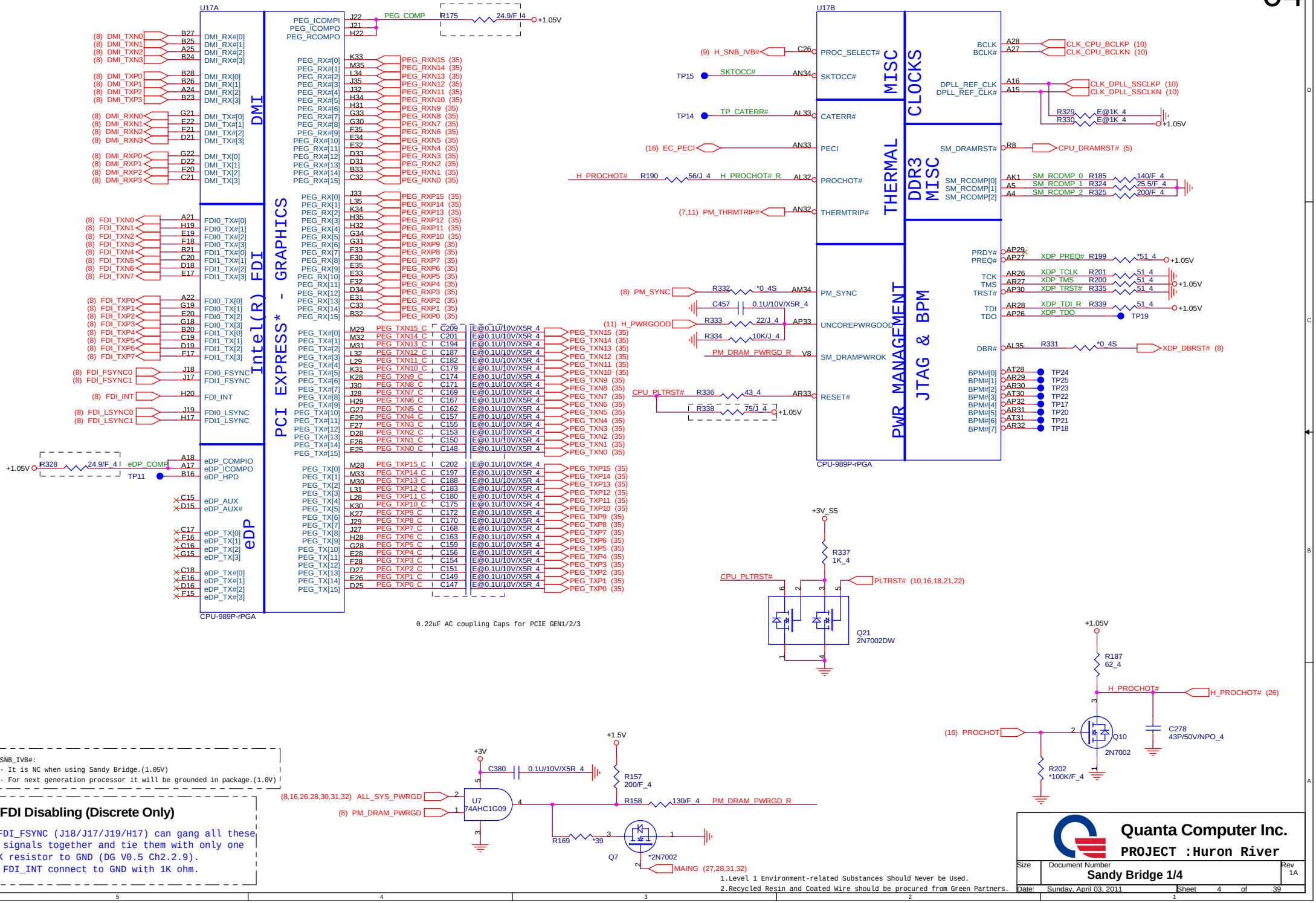
P16-- KR27 change value from 10K to 4.7K.
P33-- PD7 change value from uClamp3301D to CDSOD323-T03C.

Reason : for Battery ESD protact.
Possible Risk: No.

Sandy Bridge Processor (DMI,PEG,FDI)

Sandy Bridge Processor (CLK,MISC,JTAG)

04



Quanta Computer Inc.

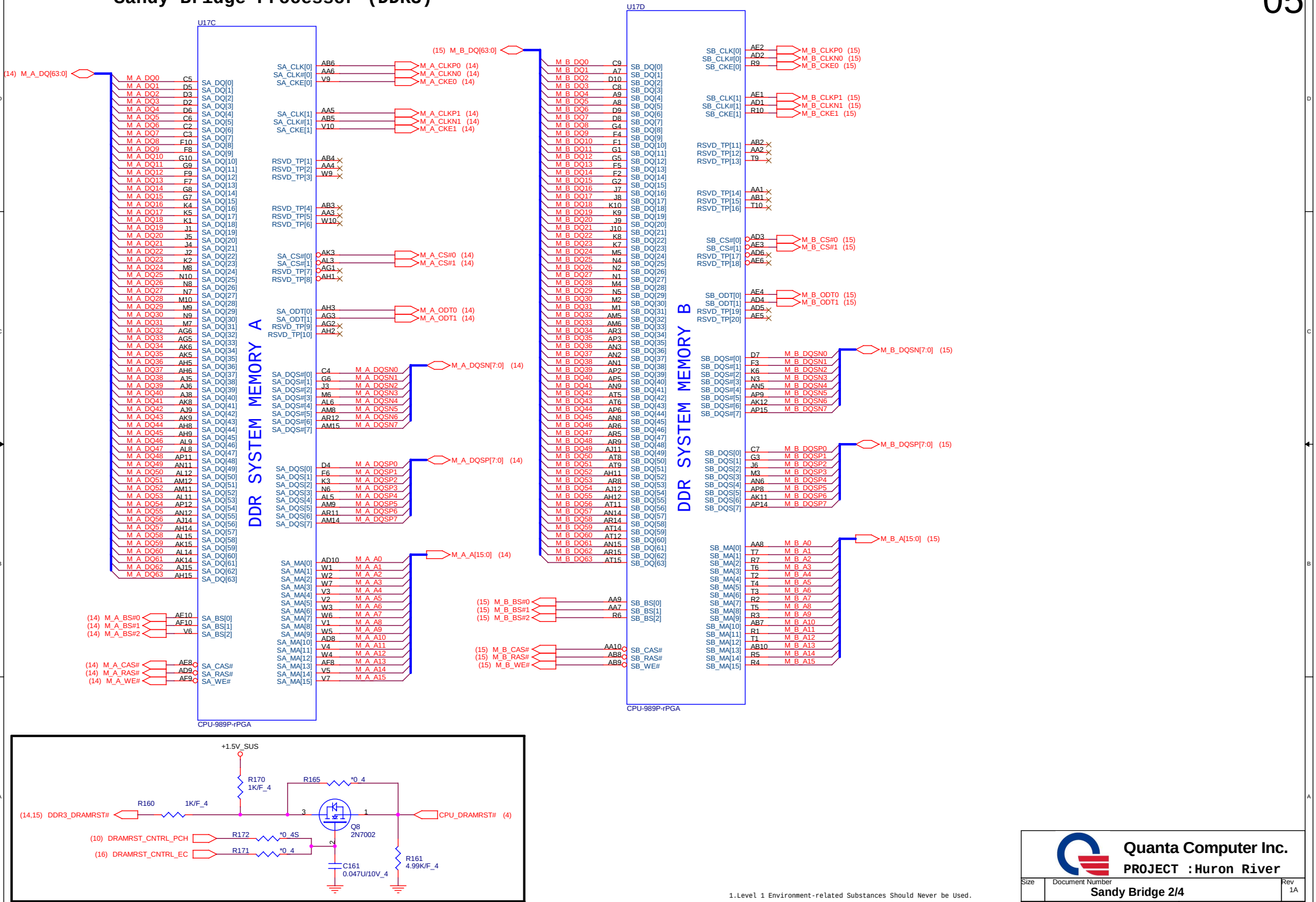
PROJECT : Huron River

Size	Document Number	Rev
	Sandy Bridge 1/4	1A

Date: Sunday, April 03, 2011 Sheet 4 of 39

Sandy Bridge Processor (DDR3)

05



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT :Huron River

Size	Document Number	Rev
	Sandy Bridge 2/4	1A
Date: Sunday, April 03, 2011	Sheet 5 of 39	

Sandy Bridge Processor (POWER)

06

CPU Core Power

SNB:55A

+VCC_CORE

C221 330U/2V/7343/ESR=9
C246 330U/2V/7343/ESR=9
C251 330U/2V/7343/ESR=9
C228 330U/2V/7343/ESR=9
PC415 390U/2.5V/6.3X6/ESR=10/SYPE

C253 *22U/6.3V/X5R_8
C262 10U/6.3V/X5R_8
C387 10U/6.3V/X5R_8
C225 10U/6.3V/X5R_8
C390 10U/6.3V/X5R_8
C393 10U/6.3V/X5R_8
C388 10U/6.3V/X5R_8
C275 *22U/6.3V/X5R_8
C252 *22U/6.3V/X5R_8
C277 22U/6.3V/X5R_8
C399 10U/6.3V/X5R_8
C243 10U/6.3V/X5R_8
C236 22U/6.3V/X5R_8
C396 10U/6.3V/X5R_8
C276 22U/6.3V/X5R_8
C206 10U/6.3V/X5R_8
C204 10U/6.3V/X5R_6
C237 10U/6.3V/X5R_6
C254 10U/6.3V/X5R_6
C263 10U/6.3V/X5R_6
C248 10U/6.3V/X5R_6
C238 10U/6.3V/X5R_6
C219 10U/6.3V/X5R_6
C218 10U/6.3V/X5R_6
C234 10U/6.3V/X5R_6
C217 10U/6.3V/X5R_6

HOLE1
*intel-CPU-bracket

U17F

POWER

CORE SUPPLY

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AE35 AE34 AE33 AE32 AE31 AE30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

CPU-989P-rPGA

PEG AND DDR

8.5A

+1.05V

VCCIO1 AH13
VCCIO2 AH10
VCCIO3 AC10
VCCIO4 Y10
VCCIO5 U10
VCCIO6 P10
VCCIO7 L10
VCCIO8 J14
VCCIO9 J13
VCCIO10 J12
VCCIO11 J11
VCCIO12 H14
VCCIO13 H12
VCCIO14 H11
VCCIO15 G14
VCCIO16 G13
VCCIO17 G12
VCCIO18 F14
VCCIO19 F13
VCCIO20 E12
VCCIO21 F11
VCCIO22 E14
VCCIO23 E12
VCCIO24 E11
VCCIO25 D14
VCCIO26 D13
VCCIO27 D12
VCCIO28 D11
VCCIO29 C14
VCCIO30 C13
VCCIO31 C12
VCCIO32 C11
VCCIO33 B14
VCCIO34 B12
VCCIO35 A14
VCCIO36 A13
VCCIO37 A12
VCCIO38 A11
VCCIO39
VCCIO40 J23

C198 *470U/2V_7343

C402 10U/6.3V/X5R_6
C397 10U/6.3V/X5R_6
C391 10U/6.3V/X5R_6
C211 10U/6.3V/X5R_6
C385 10U/6.3V/X5R_6
C386 10U/6.3V/X5R_6
C227 10U/6.3V/X5R_6
C260 10U/6.3V/X5R_6
C384 10U/6.3V/X5R_6
C392 10U/6.3V/X5R_6

C389 1U/10V/X5R_4
C247 1U/10V/X5R_4
C270 1U/10V/X5R_4
C250 1U/10V/X5R_4
C231 1U/10V/X5R_4
C220 1U/10V/X5R_4
C408 1U/10V/X5R_4
C406 1U/10V/X5R_4
C400 1U/10V/X5R_4
C398 1U/10V/X5R_4
C395 1U/10V/X5R_4
C241 1U/10V/X5R_4
C264 1U/10V/X5R_4
C191 1U/10V/X5R_4
C224 1U/10V/X5R_4
C208 1U/10V/X5R_4
C255 1U/10V/X5R_4
C242 1U/10V/X5R_4
C274 1U/10V/X5R_4

R174 *0_4S +1.05V

SVID

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 H_CPU_SVIDCLK
VIDSOUT AJ28 H_CPU_SVIDDAT

SENSE LINES

VCC_SENSE AJ35
VSS_SENSE AJ34

R183 100_4 +VCC_CORE
R188 100_4

VCC_SENSE (26)
VSS_SENSE (26)

VCCIO_SENSE B10
VSSIO_SENSE A10

VCCP_SENSE (29)
VSSP_SENSE (29)

+SMDDR_VREF
+VDDR_REF_CPU
R341 *0_8
Q22 2N7002K
(27,28) MAIND
MAIND
R340 100K/J_4

Sandy Bridge Processor (GRAPHIC POWER)

U17G

POWER

GRAPHICS

+VCC_GFX

22A

C268 I@330U/2V_7343
C411 I@330U/2V_7343
C409 *I@330U/2V_7343
C404 I@10U/6.3V/X5R_8
C403 I@10U/6.3V/X5R_8
C407 I@10U/6.3V/X5R_8
C280 I@22U/6.3V/X5R_8
C283 I@22U/6.3V/X5R_8
C291 I@22U/6.3V/X5R_8
C401 I@10U/6.3V/X5R_8
C284 *I@22U/6.3V_8
C290 I@22U/6.3V/X5R_8
C297 I@22U/6.3V/X5R_8
C405 I@10U/6.3V/X5R_8
C410 *I@22U/6.3V_8

R181 E@0_4

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

AT24 AT23 AT21 AT20 AT18 AT17 AR24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17

SENSE LINES

VAXG_SENSE AK35
VSSAXG_SENSE AK34

R191 I@10/F_4 +VCC_GFX
R198 I@10/F_4

VCC_AXG_SENSE (26)
VSS_AXG_SENSE (26)

VREF

SM_VREF AL1

+VDDR_REF_CPU
+VDDR_REF_CPU

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

DDR3 -1.5V RAILS

(4A)

+1.5V

VDDQ1 AF7
VDDQ2 AF4
VDDQ3 AF1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P7
VDDQ14 P4
VDDQ15 P1

C279 *330U/2V_7343

C229 10U/6.3V/X5R_6
C266 10U/6.3V/X5R_6
C215 10U/6.3V/X5R_6
C239 10U/6.3V/X5R_6
C210 10U/6.3V/X5R_6
C249 10U/6.3V/X5R_6

SA RAIL

SNB:6A

+0.85V

VCCSA1 M27
VCCSA2 M26
VCCSA3 L26
VCCSA4 J26
VCCSA5 J25
VCCSA6 J24
VCCSA7 H26
VCCSA8 H25

C199 10U/6.3V/X5R_6
C207 10U/6.3V/X5R_6
C192 10U/6.3V/X5R_6
C195 *10U/6.3V_6

1.8V RAIL

(1.2A)

+1.8V

C164 10U/6.3V/X5R_6
C166 1U/10V/X5R_4
C165 1U/10V/X5R_4
C186 *330U/2V_7343

VCCPLL1 B6
VCCPLL2 A6
VCCPLL3 A2

MISC

VCCSA_SENSE H23

(For +0.85V)
VCCUSA_SENSE (30)

FC_C22 VCCSA_VID1
C22 H_FC_C22 R168 10K/J_4
C24
VCCSA_SEL (30)

CPU-989P-rPGA

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK

+1.05V
Close to VR
R218 54.9/F_4
H_CPU_SVIDCLK R189 *0_4S VR_SVID_CLK (26)
(50 ohm)

SVID DATA

Place PU resistor close to CPU

+1.05V
R184 130/F_4
+1.05V
Close to VR
R347 130/F_4
H_CPU_SVIDDAT R186 *0_4S VR_SVID_DATA (26)
(50 ohm)

SVID ALERT

Place PU resistor close to CPU

+1.05V
R195 75/J_4
H_CPU_SVIDALRT# R192 43_4 R197 *0_4S VR_SVID_ALERT# (26)
(50 ohm)

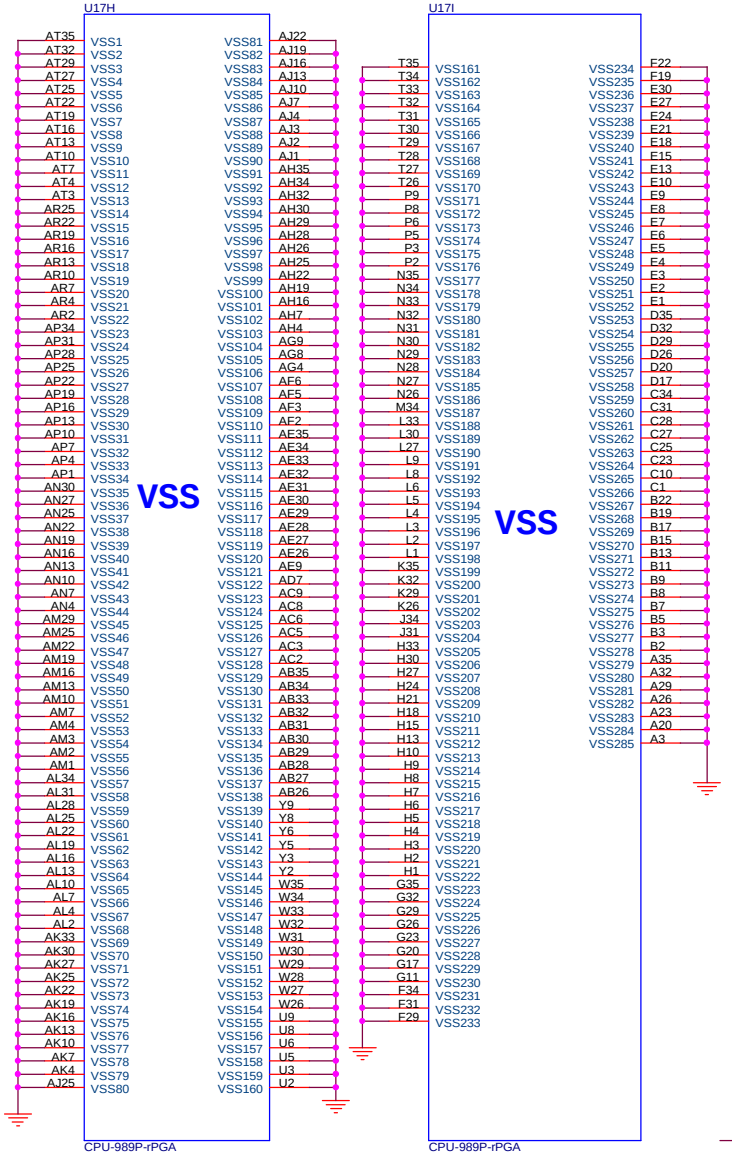
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT :Huron River

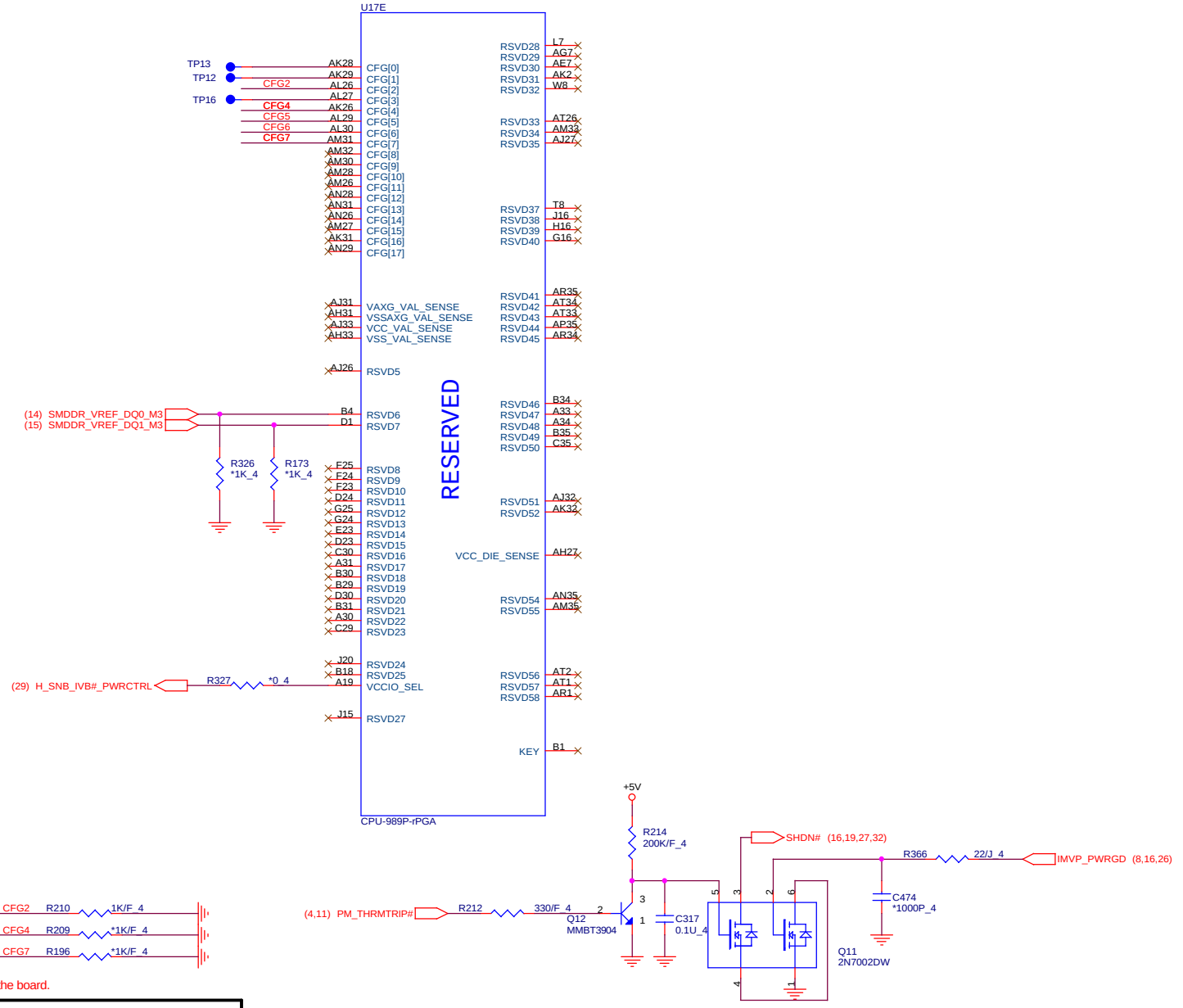
Size	Document Number	Rev
	Sandy Bridge 3/4	1A

Date: Monday, February 21, 2011 Sheet 6 of 39

Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	**Lane Reversed**
CFG4 (DP Presence Strap)	**Disable; No physical DP attached to eDP**	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	**PEG train immediately following xxRESETB de assertion**	PEG wait for BIOS training

CFG5 R194 *1K/F_4
CFG6 R193 *1K/F_4

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - X16 PEG interface
10: PEG x8 x8 bifurcation enableddisabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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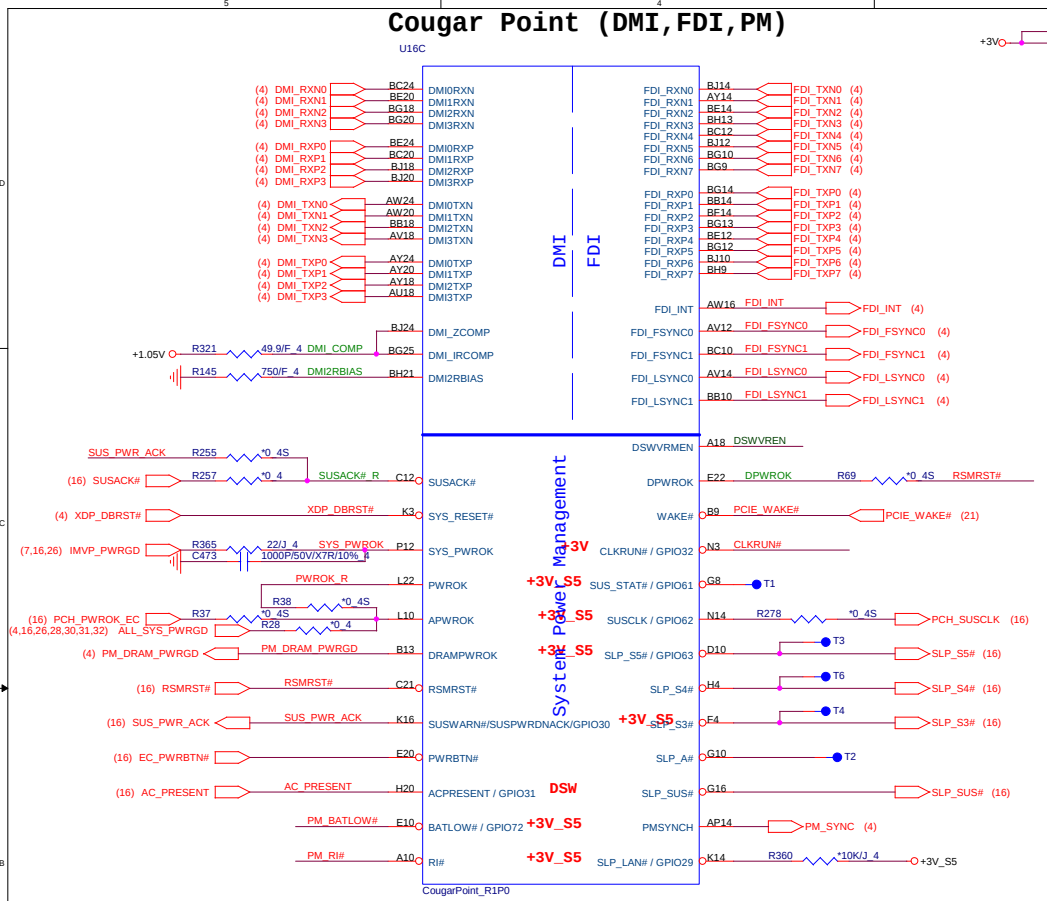
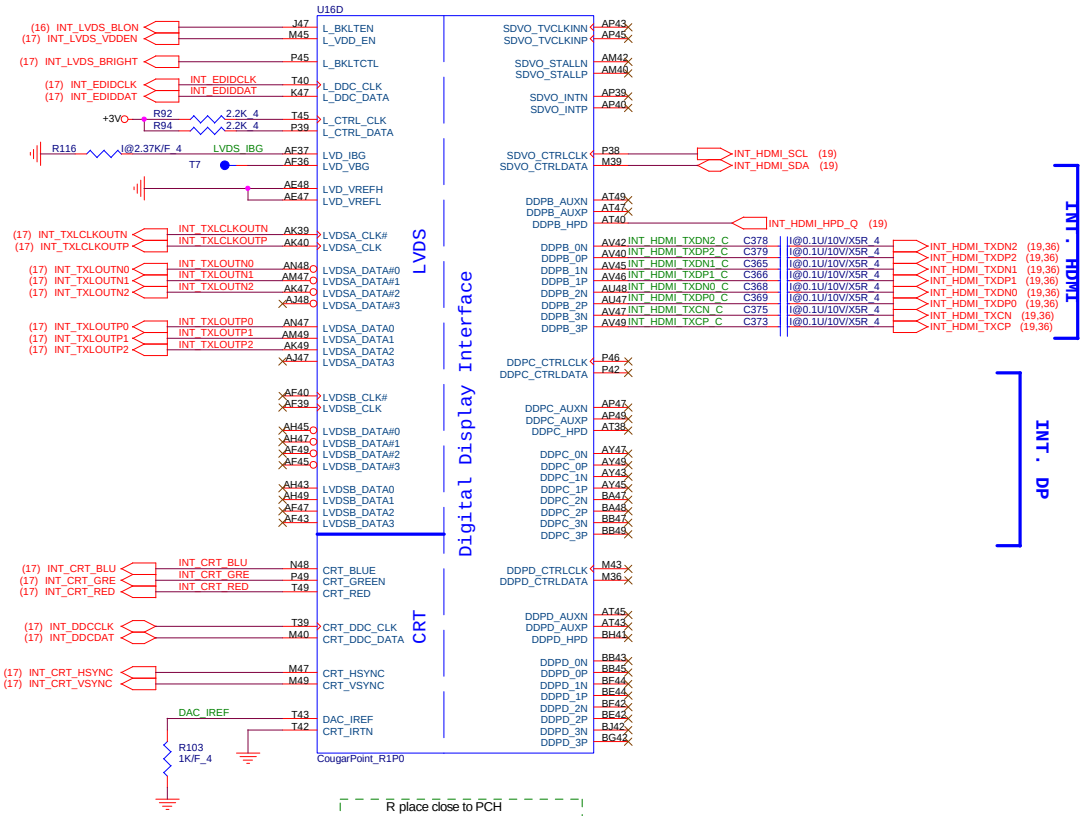
Quanta Computer Inc.
PROJECT :Huron River

Size	Document Number	Rev
	Sandy Bridge 4/4	1A
Date: Monday, February 21, 2011	Sheet 7 of 39	

Cougar Point (DMI,FDI,PM)



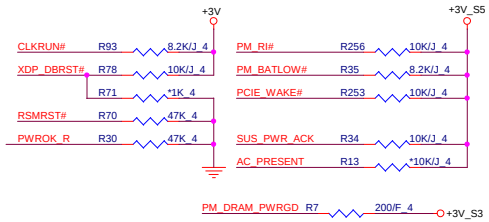
Cougar Point (LVDS,DDI)

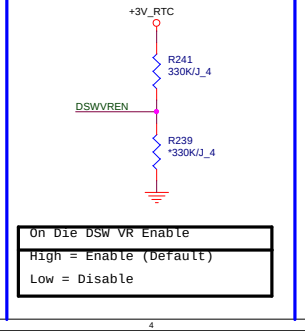


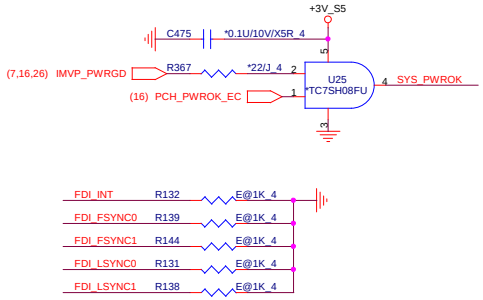
R place close to PCH

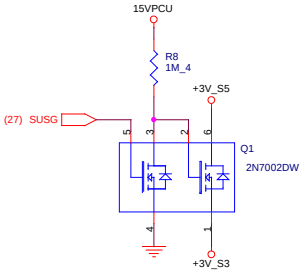
R90 I@150/F_4 INT_CRT_BLU
R95 I@150/F_4 INT_CRT_GRE
R100 I@150/F_4 INT_CRT_RED

PCH Pull-high/low(CLG)









1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT :Huron River

Size	Document Number	Rev
	Cougar Point 1/6	1A
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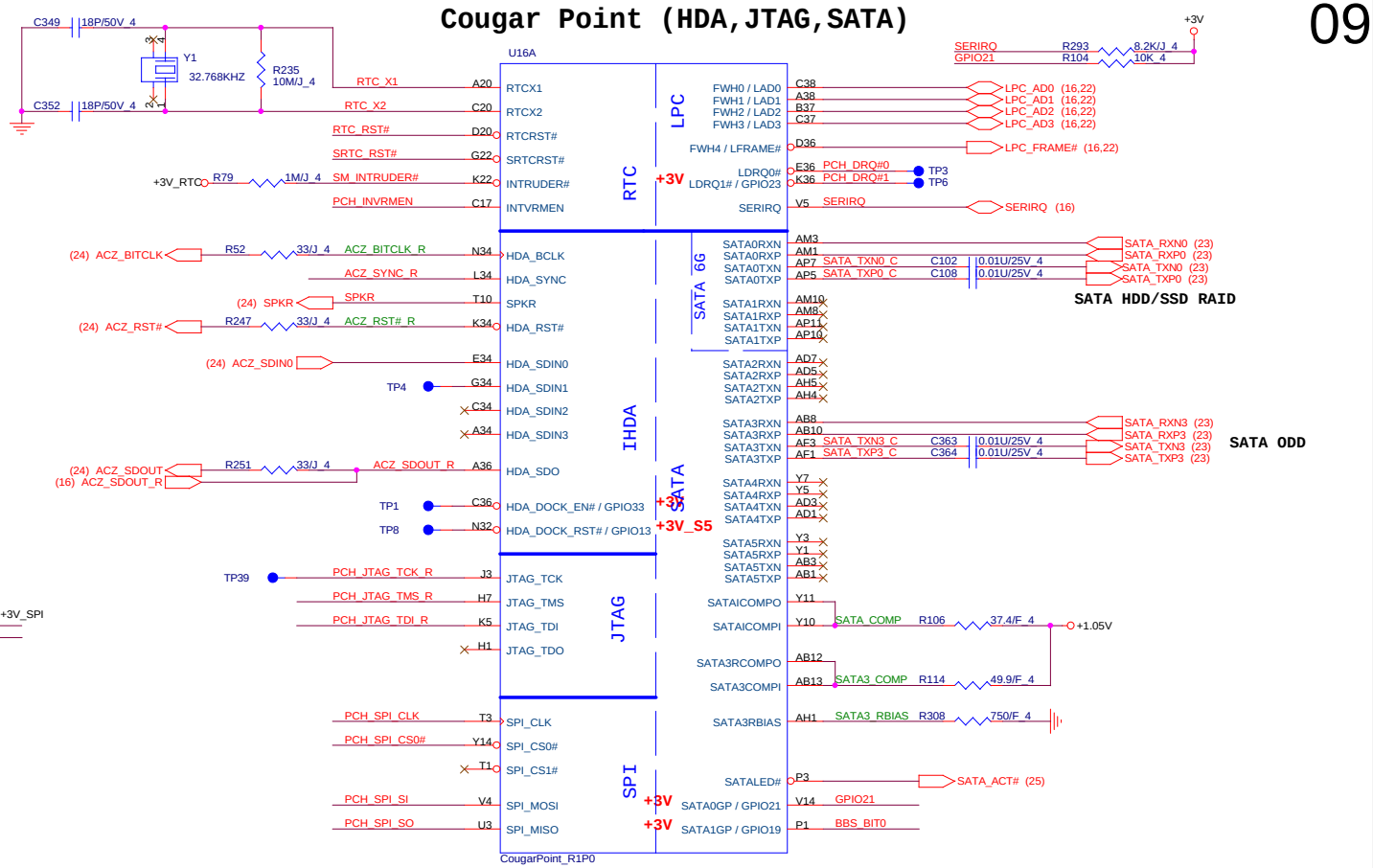
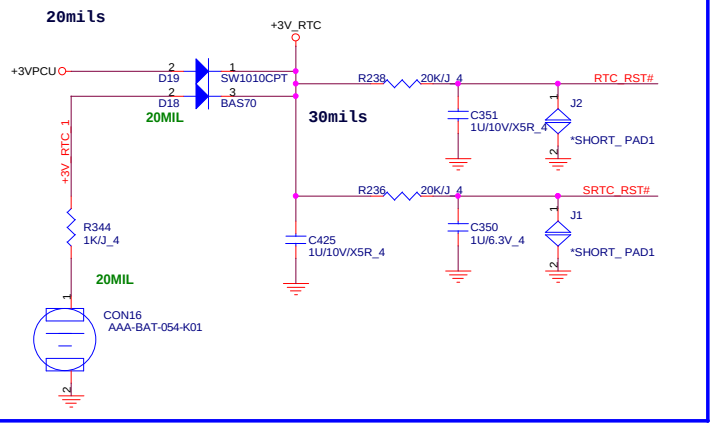
Cougar Point (HDA,JTAG,SATA)

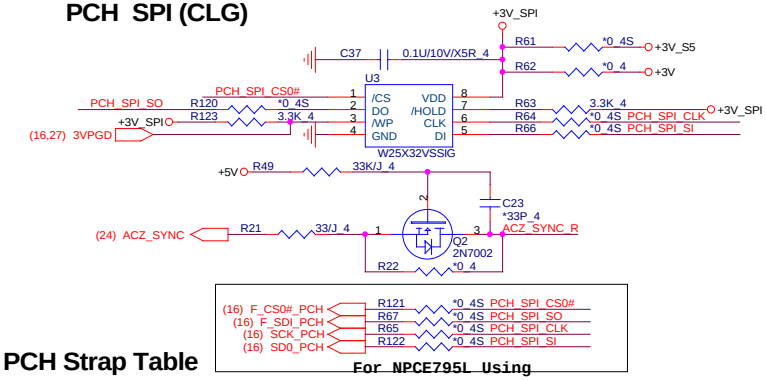


RTC Circuitry(RTC)



MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00

PCH SPI (CLG)

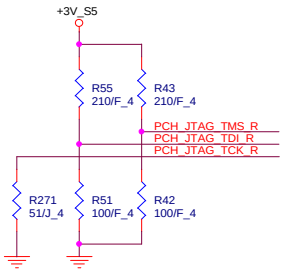


For NPCE795L Using

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	HK1/HK2 note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R105 *1K_4 SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R270 *1K_4 PCI_GNT3# (10)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R242 330K/J_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI *; 0 / 0 / LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R266 *1K_4 BBS_BIT1 (10) R289 *1K_4 BBS_BIT0
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Enabled	+3V R250 *1K_4 ACZ_SDOUT_R
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R140 2.2K_4 +1.8V R320 1K_4 NV_CLE (11) H_SNB_IVB# (4)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R91 *1K_4 PLL_ODVR_EN (11)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 R29 1K_4 ACZ_SYNC_R

PCH JTAG Debug (CLG)



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT :Huron River

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	Cougar Point 2/6	1A
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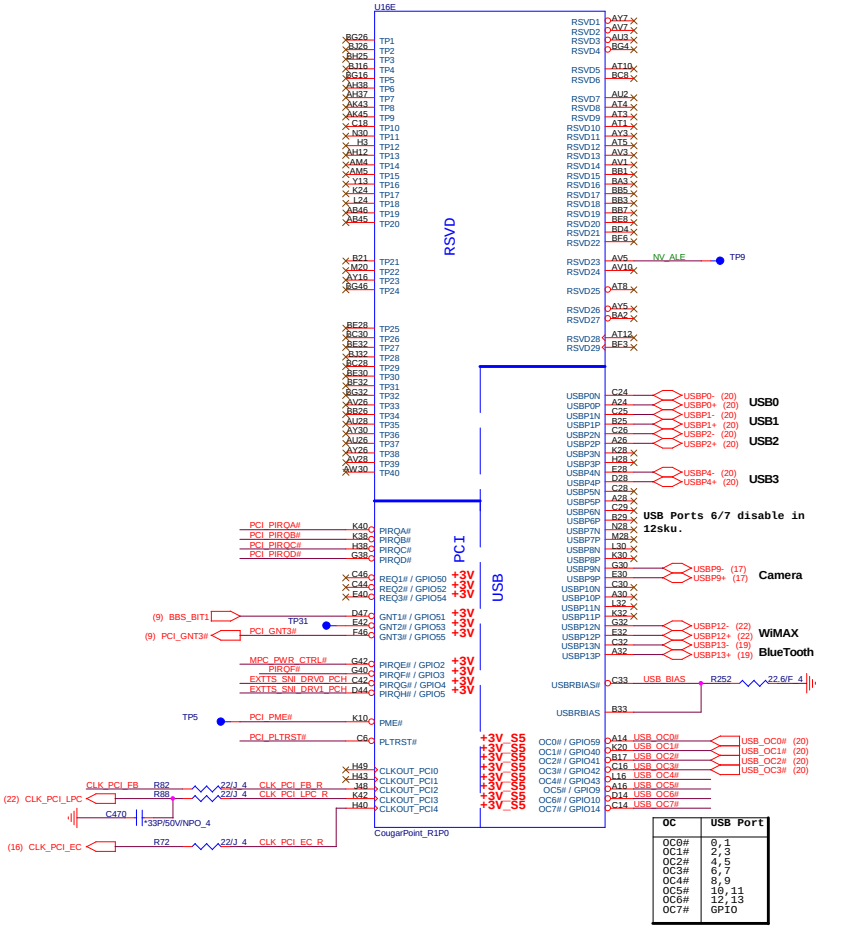
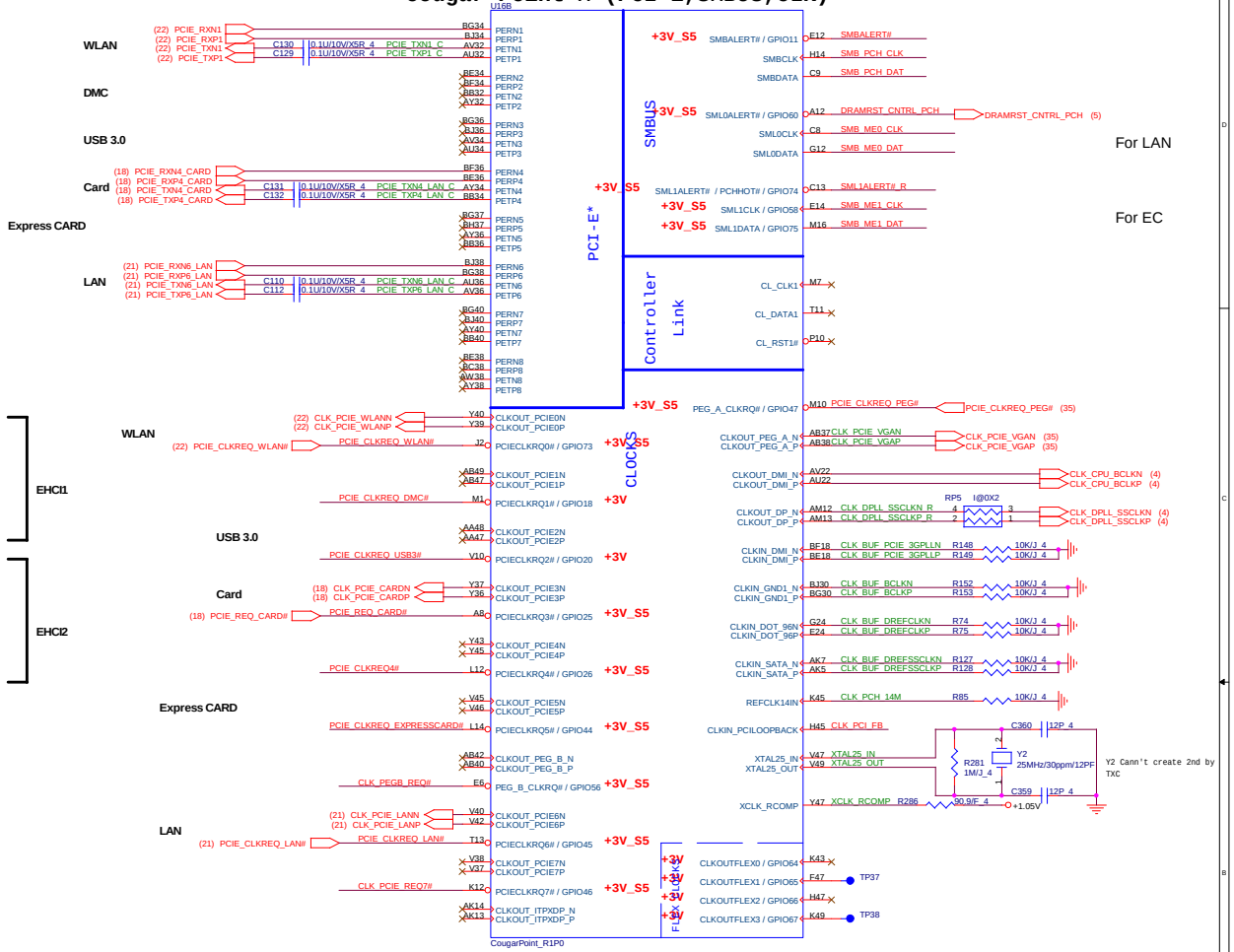
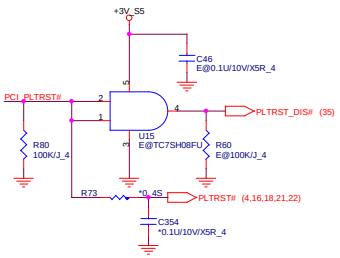
Cougar Point-M (PCI,USB,NVRAM)



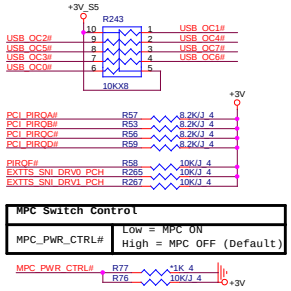
Cougar Point-M (PCI-E,SMBUS,CLK)



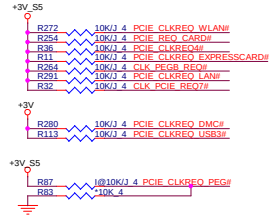
PLTRST#(CLG)



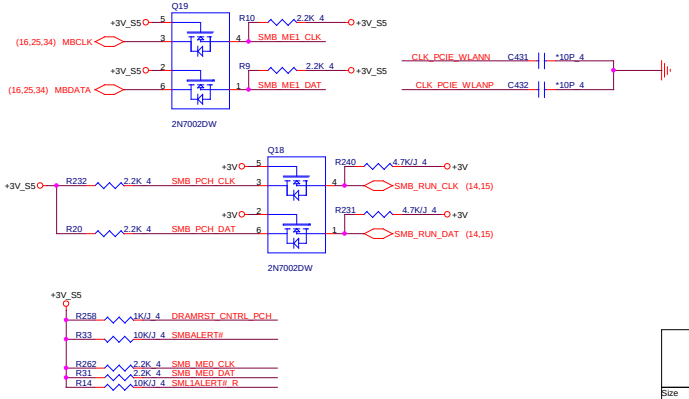
PCI/USBOC# Pull-up(CLG)



CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)



Quanta Computer Inc.	
PROJECT : Huron River	
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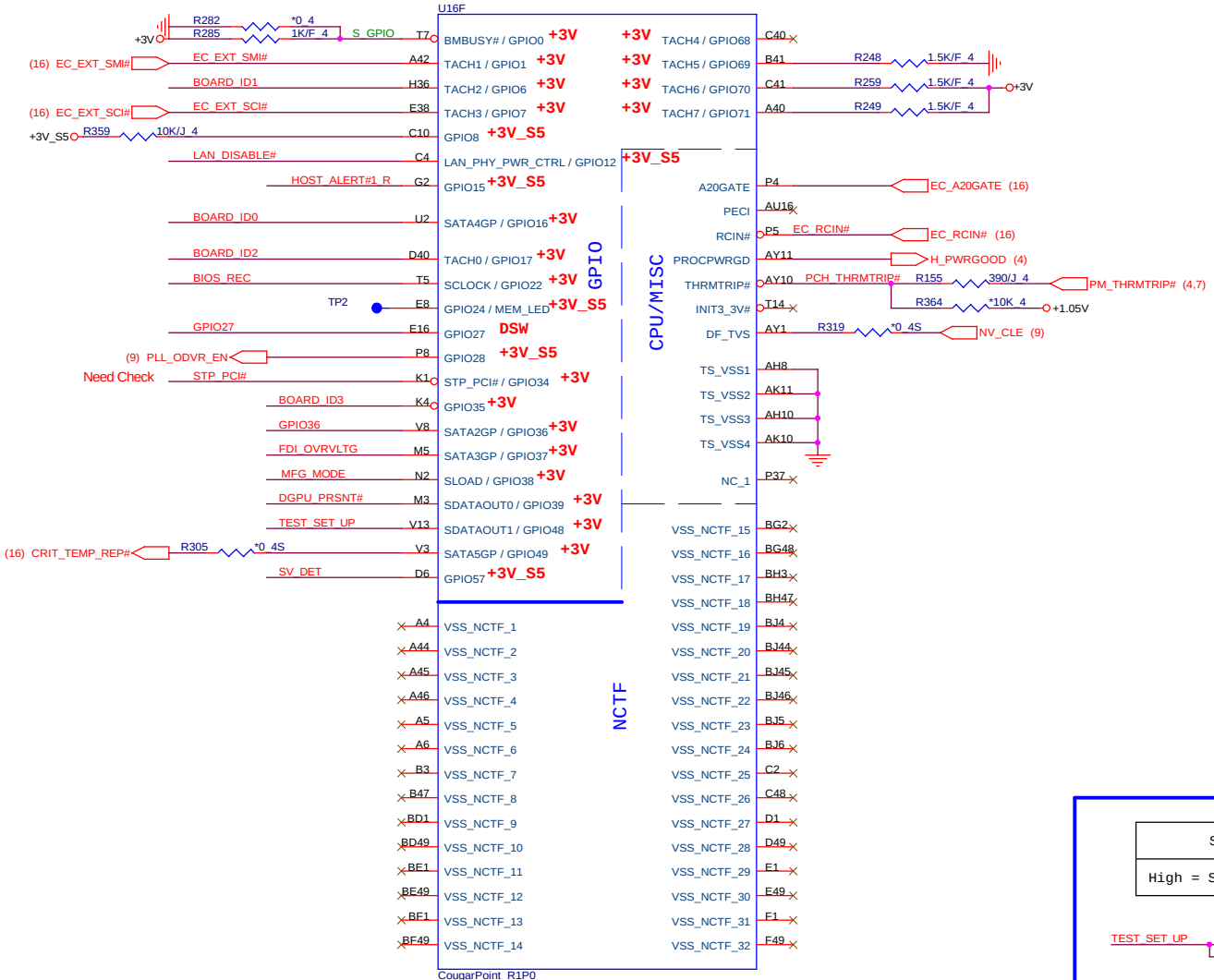
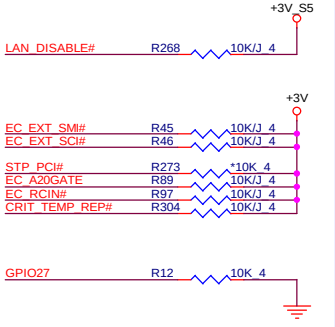
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Cougar Point (GPIO,VSS_NCTF,RSVD)



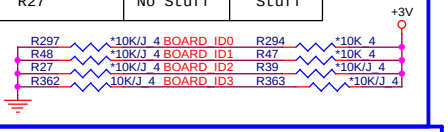
GPIO Pull-up/Pull-down(CLG)



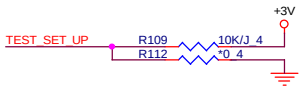
Board ID0 (N12M/N12P)	N12M	N12P
R294	Stuff	No Stuff
R297	No Stuff	Stuff

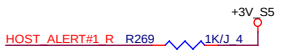
Board ID1 (VRAM Vendor)	Samaung	Hynix
R47	Stuff	No Stuff
R48	No Stuff	Stuff

Board ID2 (VRAM 1G/512M)	1G	512M
R39	Stuff	No Stuff
R27	No Stuff	Stuff



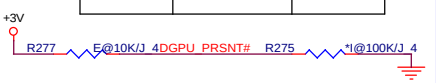
SV_SET_UP
High = Strong (Default)

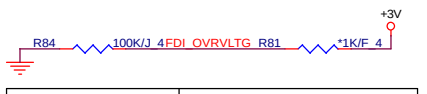




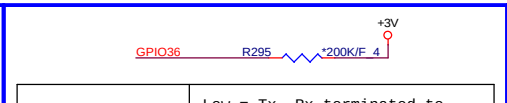
Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

PCBA SKU	Discrete	UMA
R277	Stuff	No Stuff
R275	No Stuff	Stuff

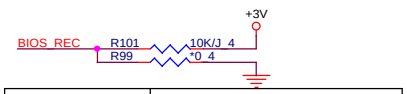




FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

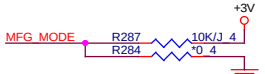


DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)



BIOS RECOVERY	High = Disable (Default) Low = Enable

MFG-TEST



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Quanta Computer Inc.
PROJECT :Huron River

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	Cougar Point 4/6	1A

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PCH5(CLG) COUGAR POINT (POWER)

Cougar Point-M (POWER)

POWER

VccCORE =1.3 A(60mils)

VCC CORE

CRT

LVDS

HVCMOS

DMI

VCCIO

DFT / SPI

FDI

(VccIO =2.925A (140mils))

1mA(8mils)

1mA(8mils)

60mA(10mils)

VCCDMI = 42mA(10mils)

VCCCLKDMI = 20mA(8mils)

VCCPNAND = 190 mA(15mils)

VCCSPI = 20mA(8mils)

VCCVRM: 1.8V (Destop) 02/20 del for Pre-ES1
1.5V (Mobile)

CougarPoint_R1P0

VccASW =1.01 A(60mils)

VCCDSW3_3= 3mA

65mA(10mils)

8mA(8mils)

VCCDIFFCLKN= 55mA(10mils)

VCCSSC= 95mA(10mils)

1mA(8mils)

VCCRTC<1mA(8mils)

Clock and Miscellaneous

USB

PCI/GPIO/LPC

SATA

CPU

MISC

RTC

HDA

VCCSUS3_3 = 119mA(15mils)

VCC5REFSUS=1mA

V5REF= 1mA

VCCSUS3_3 = 119mA(15mils)

VCCPCORE = 28mA(10mils)

VCCVRM= 114mA(15mils)

VCCME = 1.01A(60mils)

VCCSUSHDA= 10mA(8mils)

CougarPoint_R1P0

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Quanta Computer Inc.
PROJECT :Huron River

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	Cougar Point 5/6	1A
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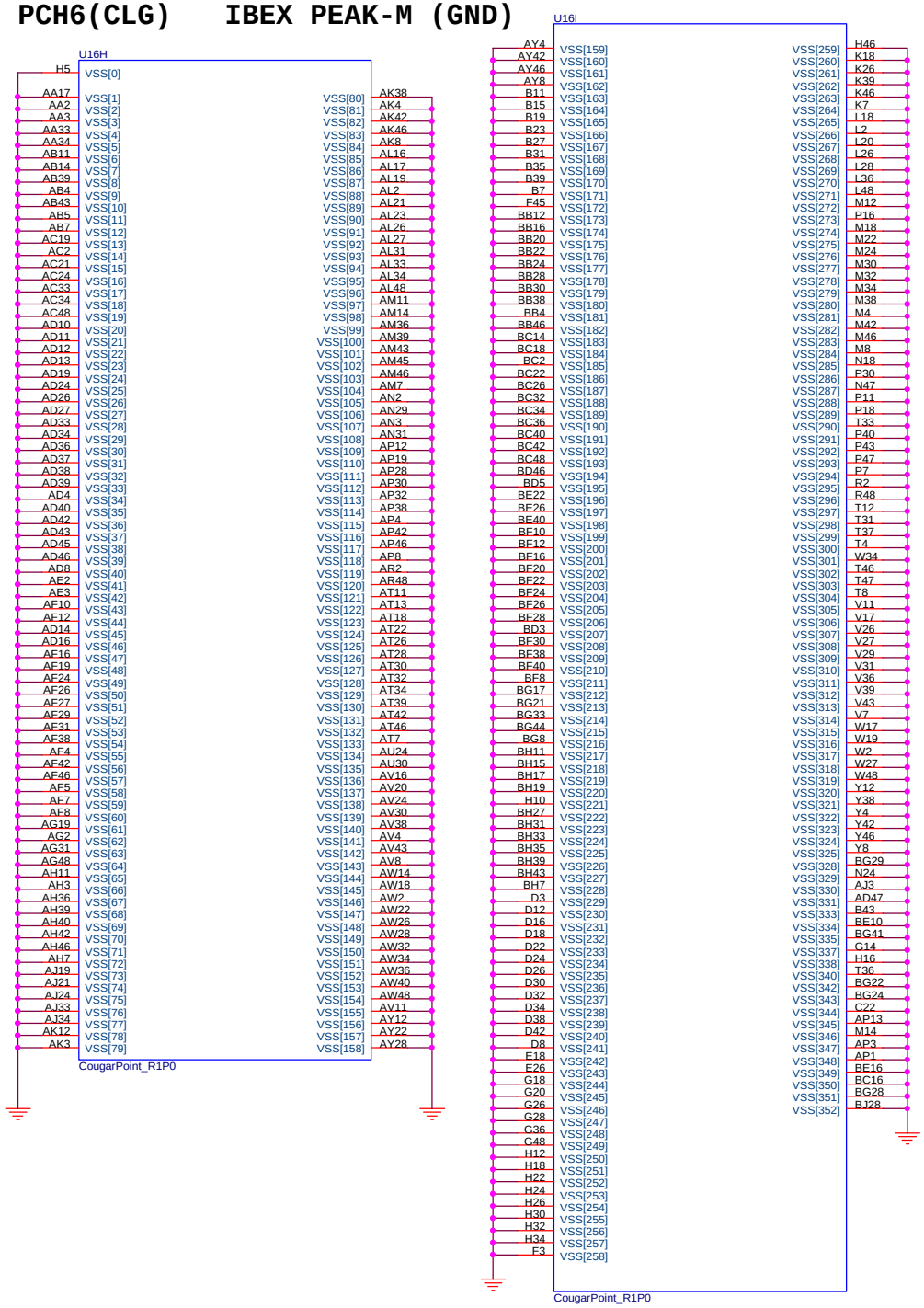
PCH6(CLG) IBEX PEAK-M (GND)



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Quanta Computer Inc.
PROJECT :Huron River

Size	Document Number	Rev
	Cougar Point 6/6	1A
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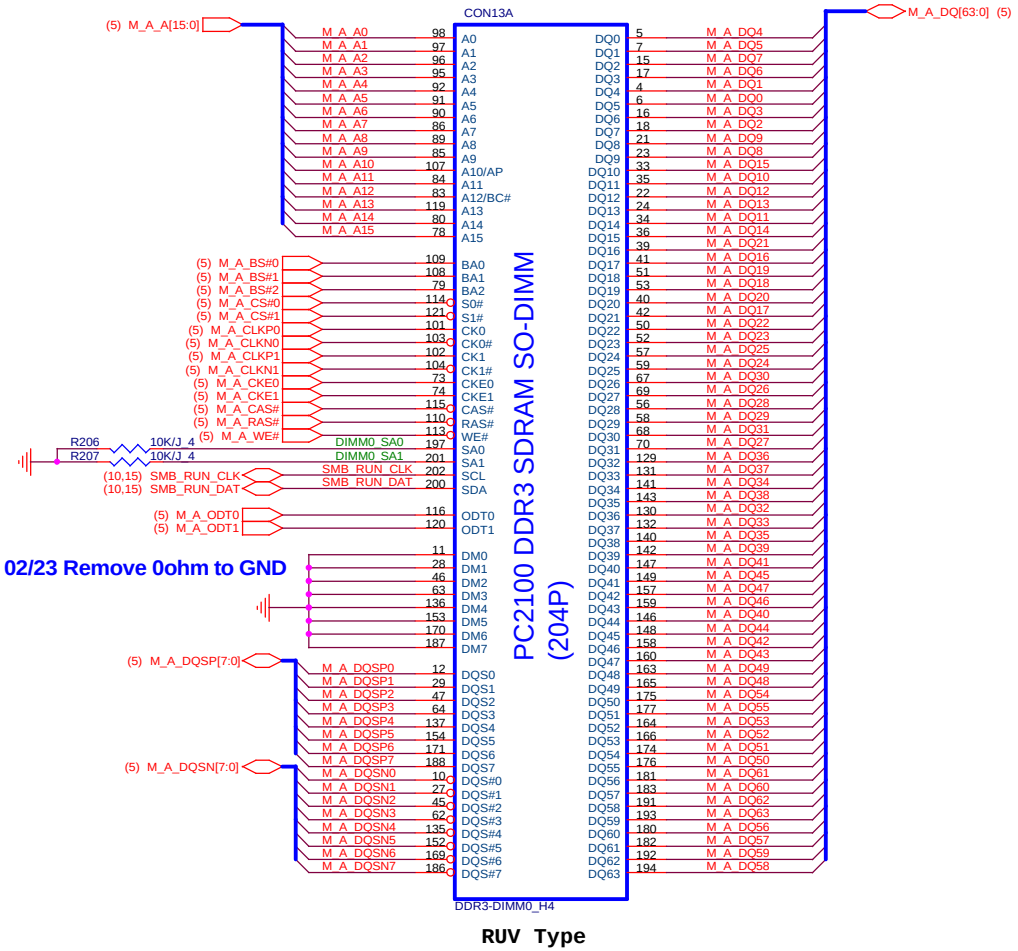

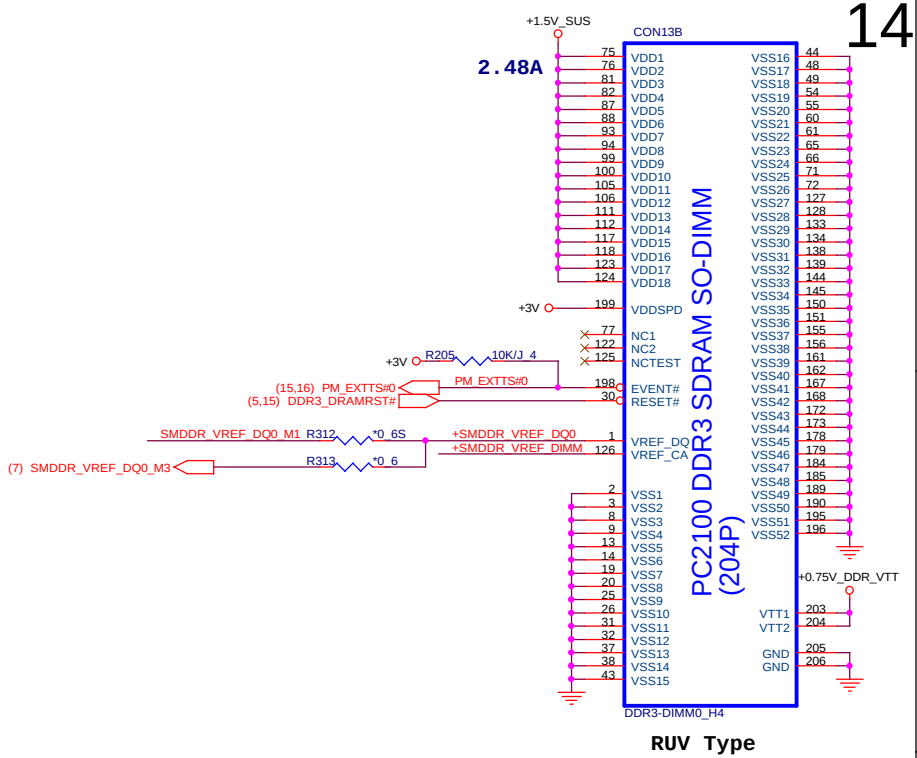

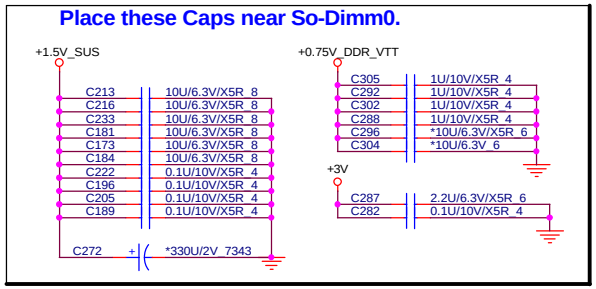

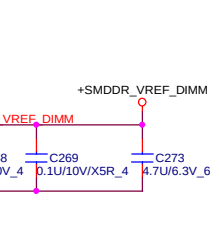

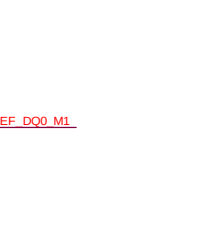

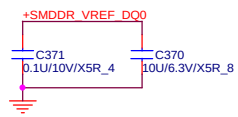

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Quanta Computer Inc.
PROJECT :Huron River

Size	Document Number	Rev
	DDRIII SO-DIMM-0	1A
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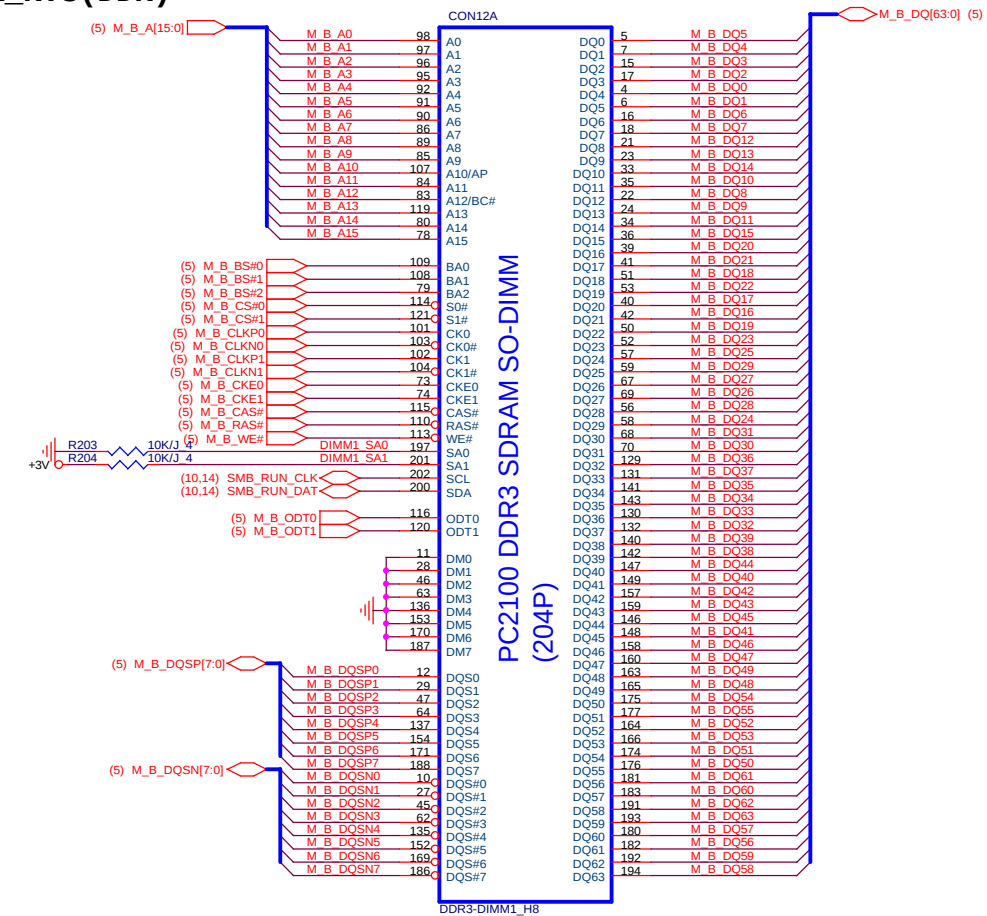
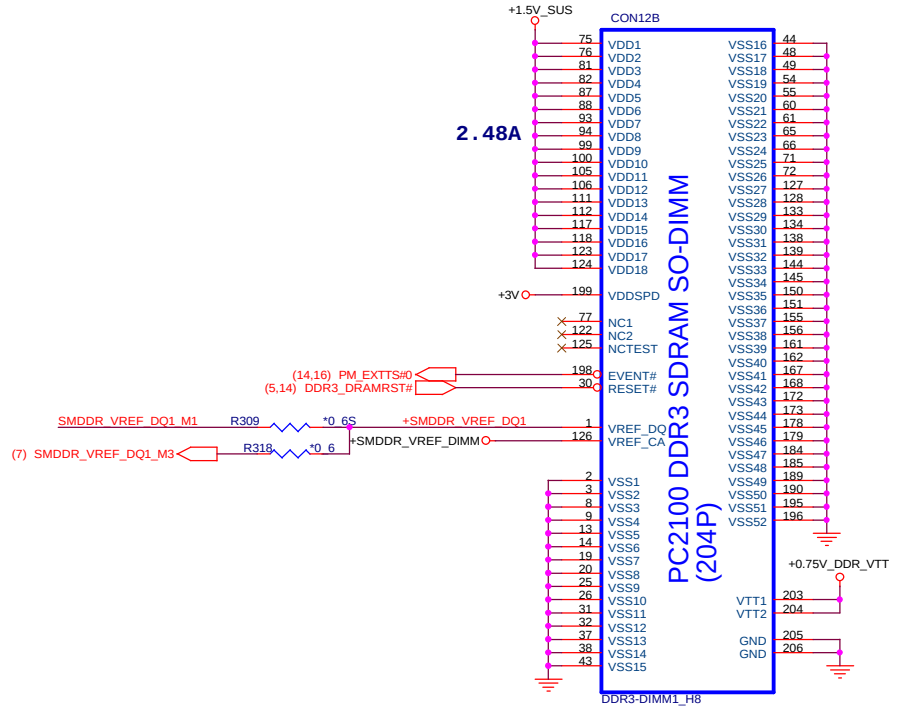
DDR_RVS(DDR)

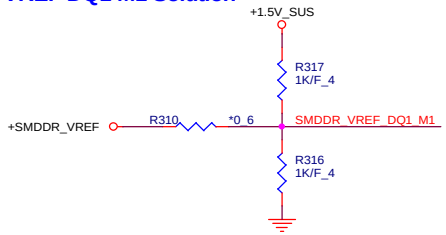


RUV Type

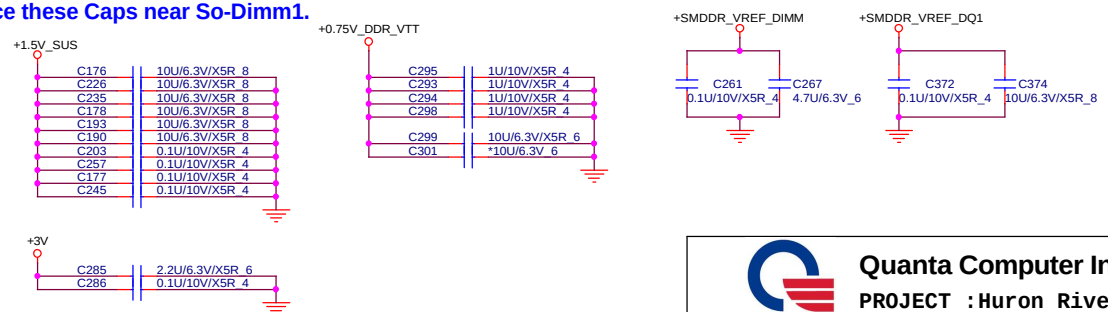


RUV Type

VREF DQ1 M1 Solution



Place these Caps near So-Dimm1.



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Quanta Computer Inc.
PROJECT :Huron River

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A
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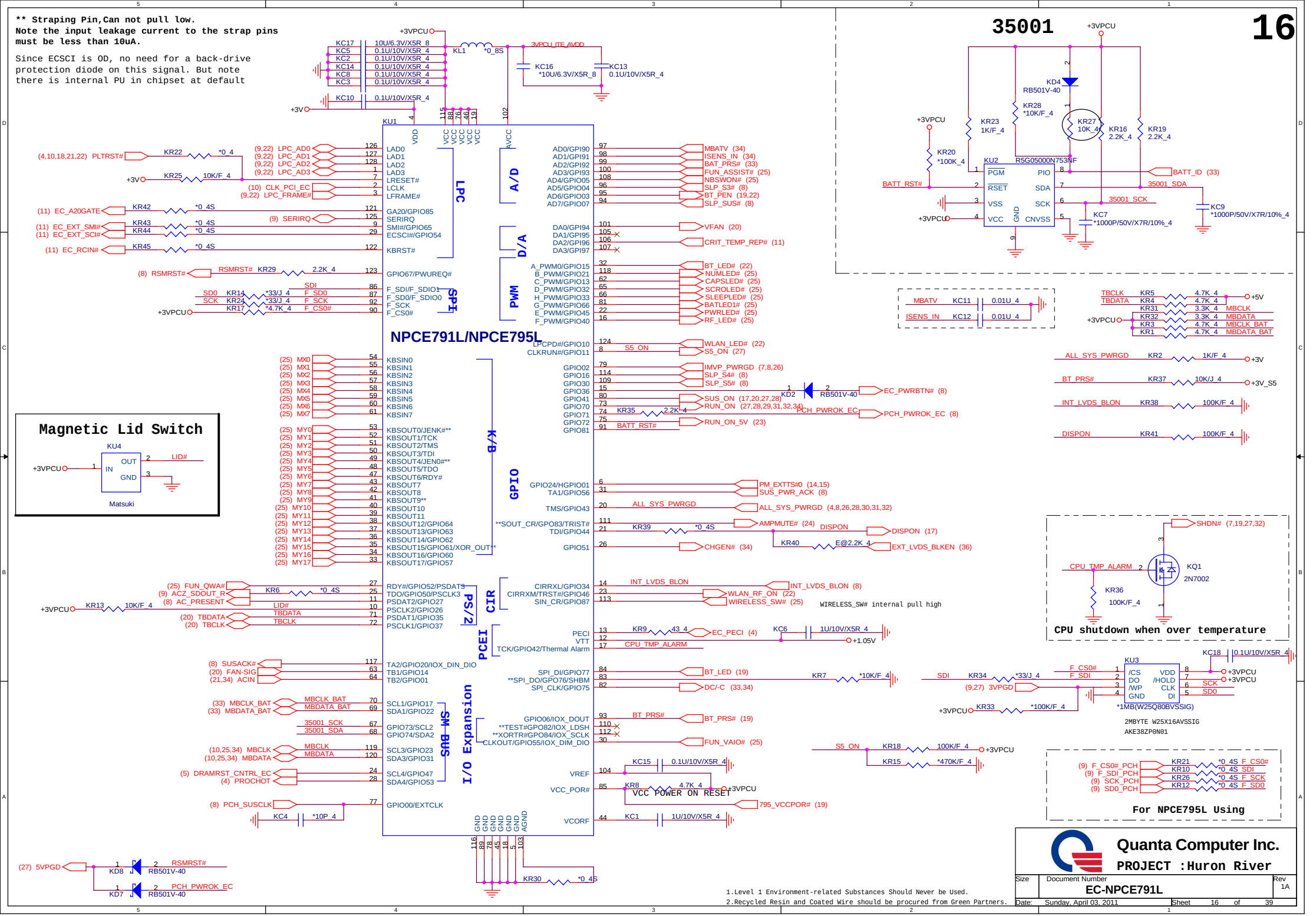
**** Straping Pin,Can not pull low.**
Note the input leakage current to the strap pins must be less than 10uA.

Since ECSCI is OD, no need for a back-drive protection diode on this signal. But note there is internal PU in chipset at default



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Quanta Computer Inc.
PROJECT :Huron River

Size	Document Number	Rev
	EC-NPCE791L	1A
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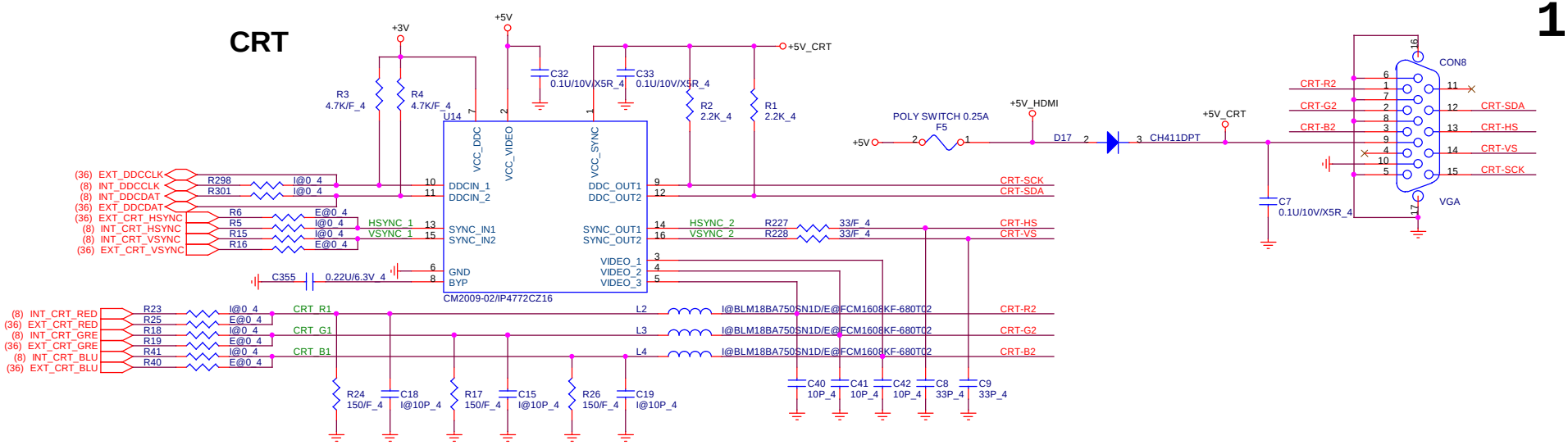
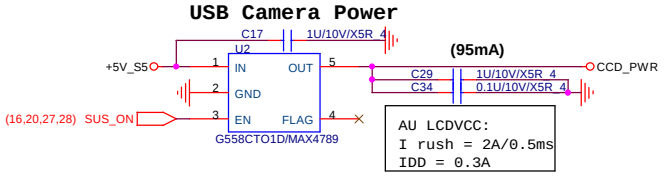
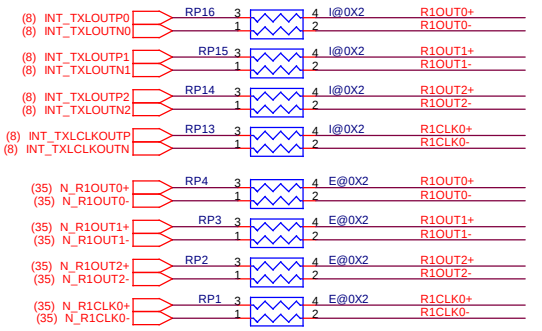
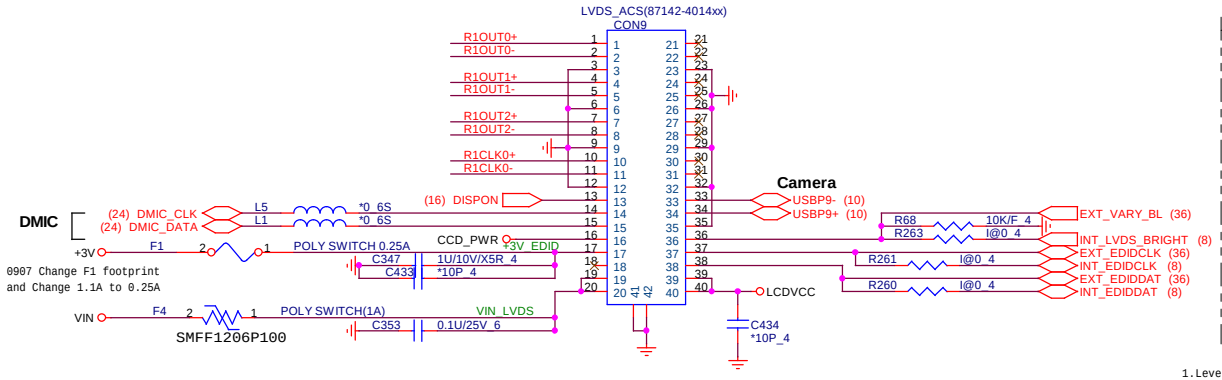
CRT



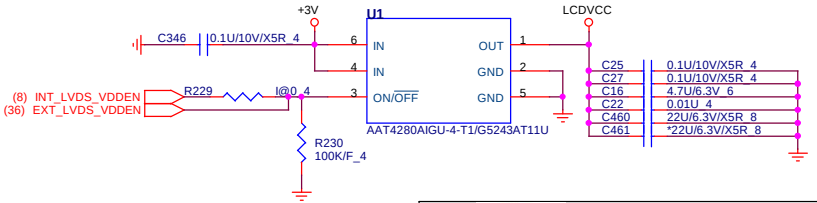
USB Camera Power







NB LVDS enable



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Quanta Computer Inc.
PROJECT :Huron River

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	CRT/LVDS	1A
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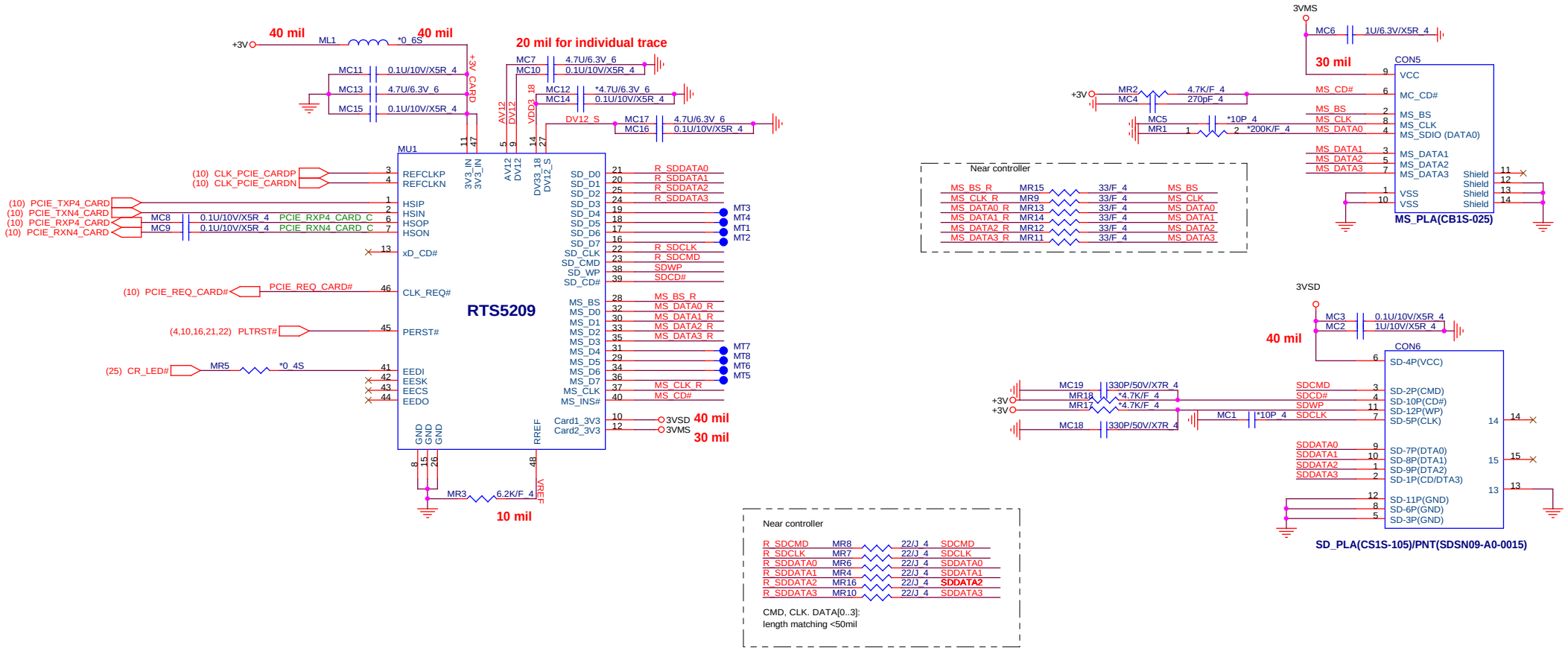

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Quanta Computer Inc.
PROJECT :Huron River

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	CARD	1A

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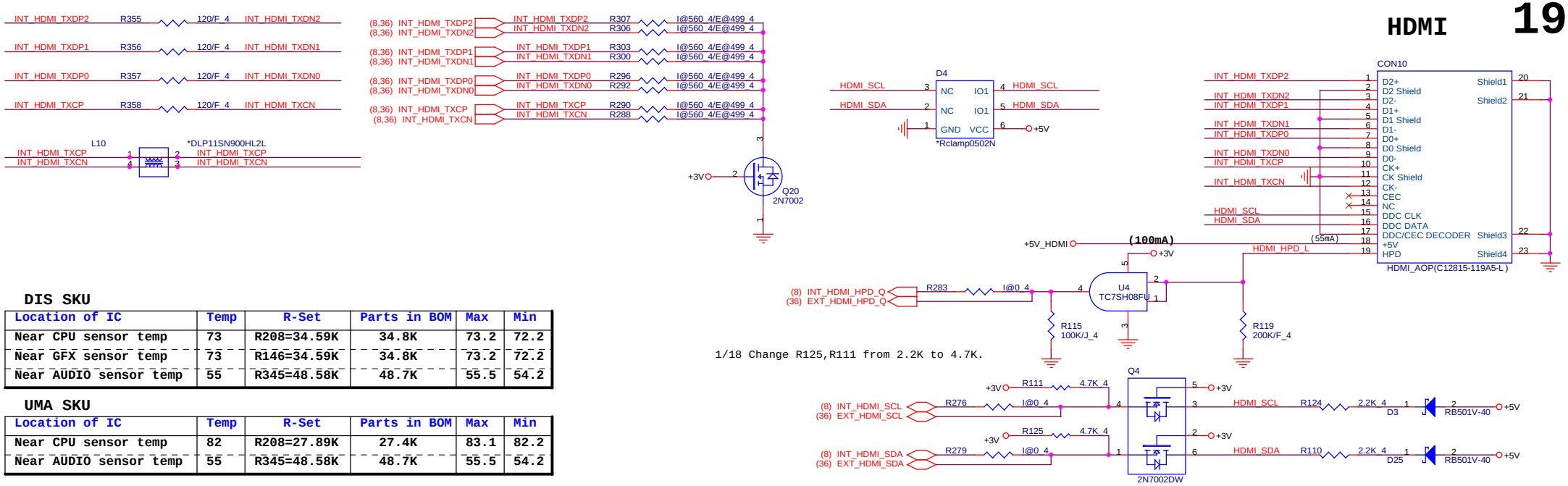
HDMI



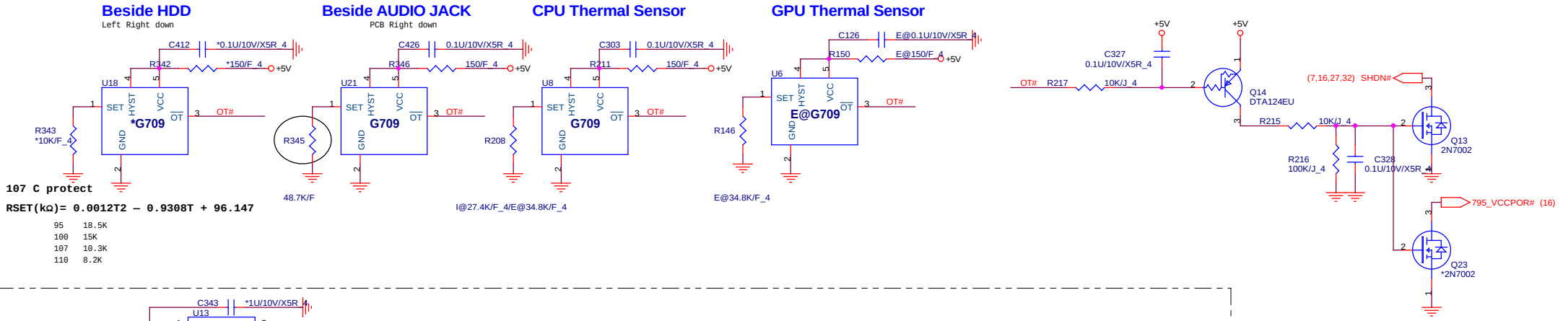
DIS SKU

Location of IC	Temp	R-Set	Parts in BOM	Max	Min
Near CPU sensor temp	73	R208=34.59K	34.8K	73.2	72.2
Near GFX sensor temp	73	R146=34.59K	34.8K	73.2	72.2
Near AUDIO sensor temp	55	R345=48.58K	48.7K	55.5	54.2

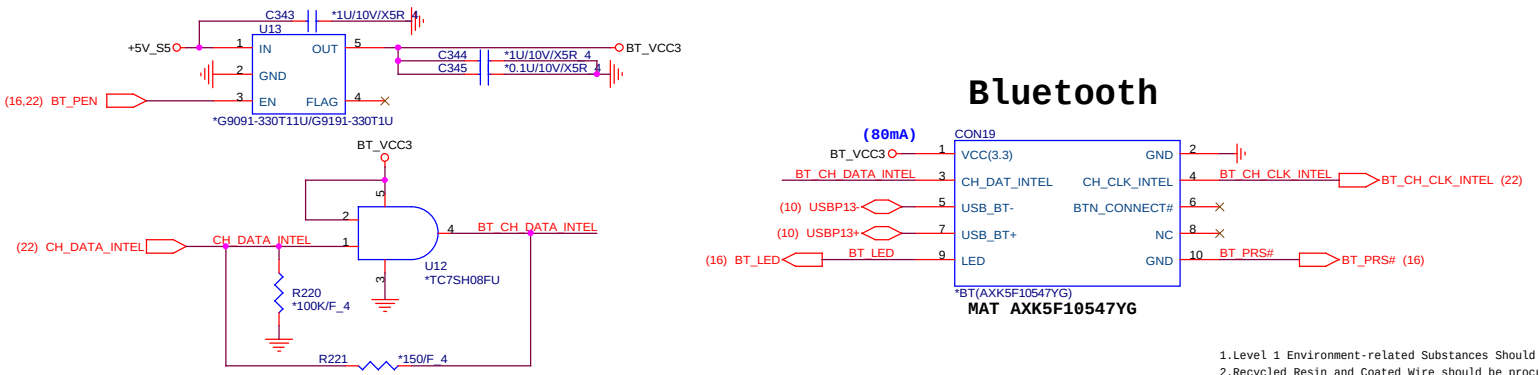
UMA SKU

Location of IC	Temp	R-Set	Parts in BOM	Max	Min
Near CPU sensor temp	82	R208=27.89K	27.4K	83.1	82.2
Near AUDIO sensor temp	55	R345=48.58K	48.7K	55.5	54.2

H/W Thermal Protect



Bluetooth



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Quanta Computer Inc.
PROJECT :Huron River

Size	Document Number	Rev
	HDMI/Bluetooth/Thermal IC	3A
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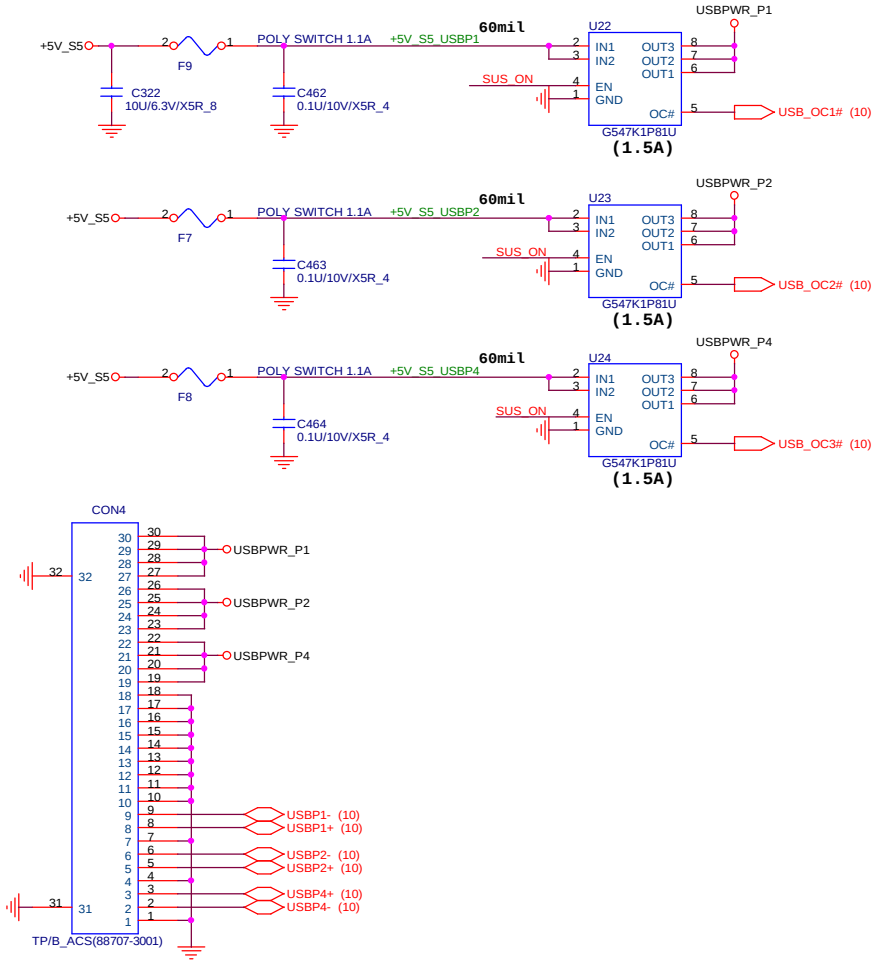
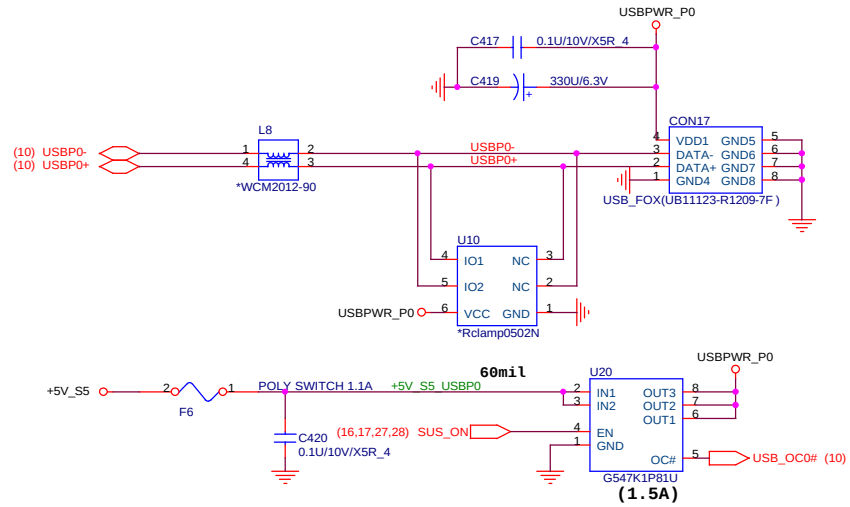
MB to USB board

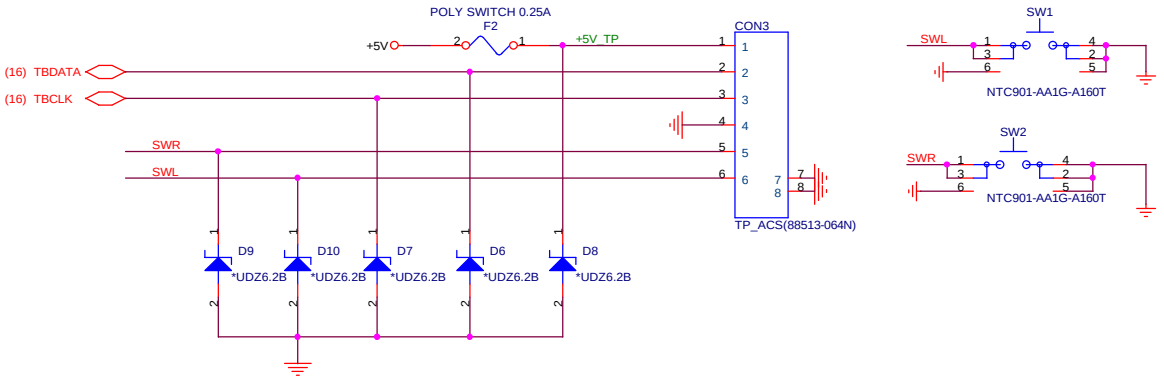


USB PORT 0

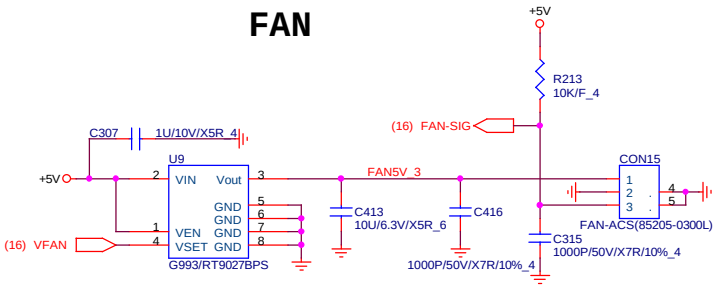


T/P Board to T/P

9/13 change F2 P/N from 0.12A to 0.25A



FAN

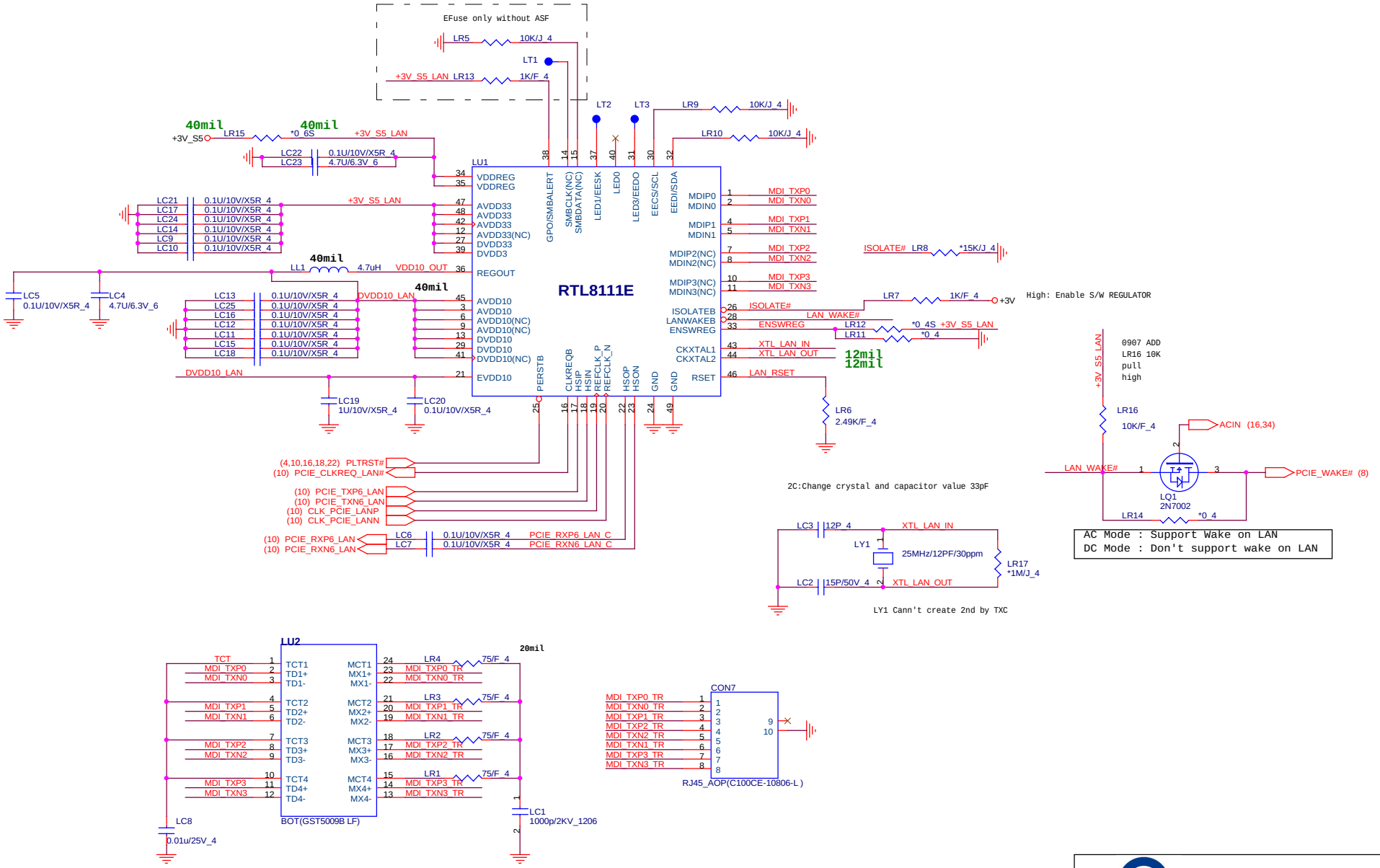


1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT :Huron River

Size	Document Number	Rev
	USB/TP/FAN	1A

Date: Monday, February 21, 2011 Sheet 20 of 39



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Quanta Computer Inc.
PROJECT : Huron River

Size	Document Number	Rev
	LAN RTL8111E	1A

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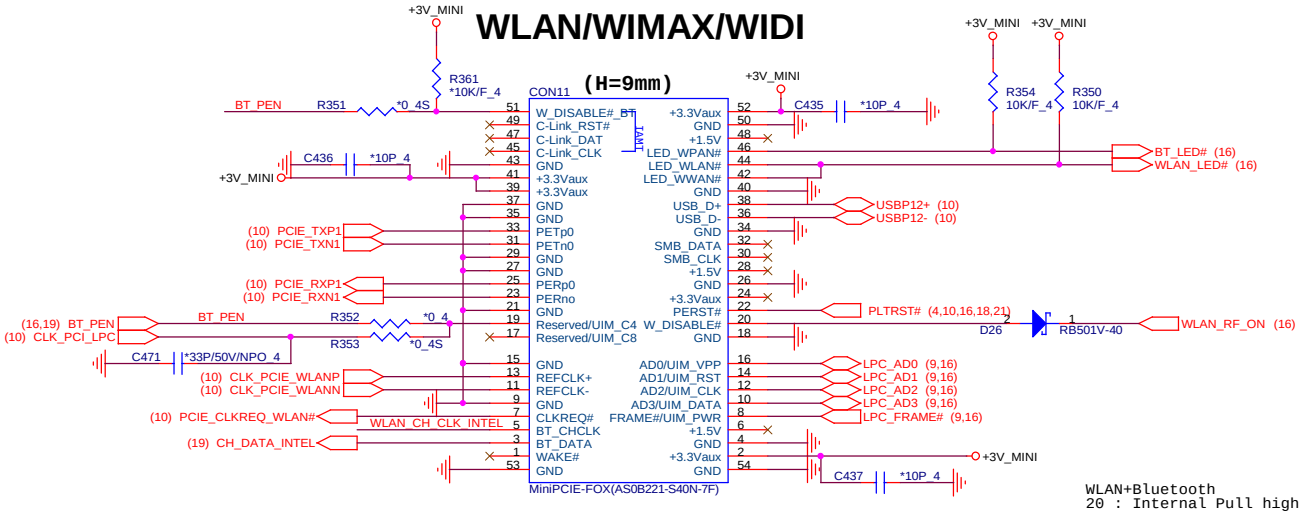
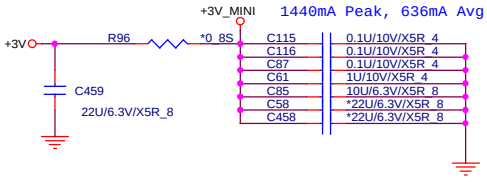
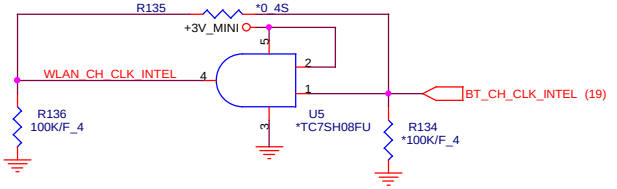
WLAN/WIMAX/WIDI







WLAN+Bluetooth
20 : Internal Pull high 25K ~ 58K

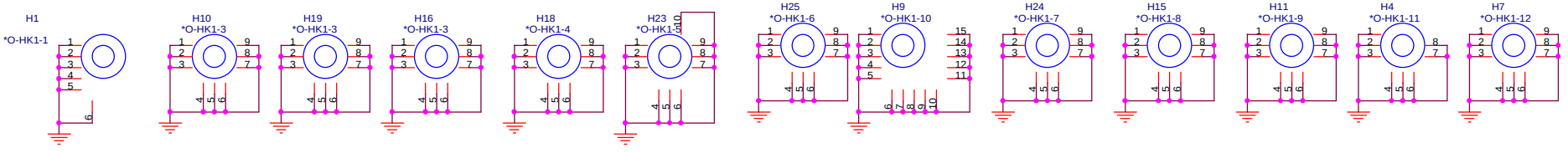
HOLE

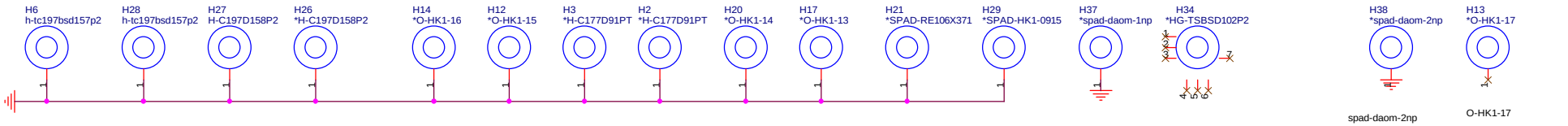
WLAN

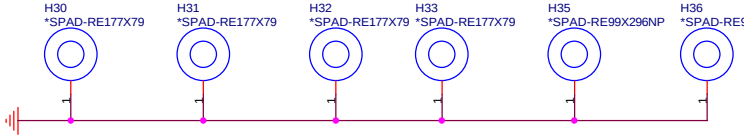
H8 H-C197D158P2

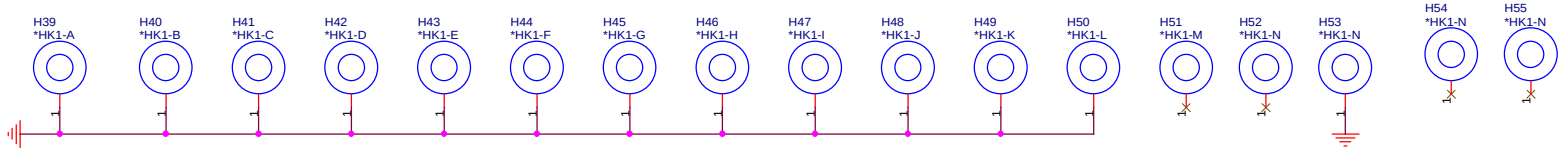
BT

H22 H-C157D102PB









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Quanta Computer Inc.
PROJECT :Huron River

Size	Document Number	Rev
	WLAN/WIMAX/WIDI	1A
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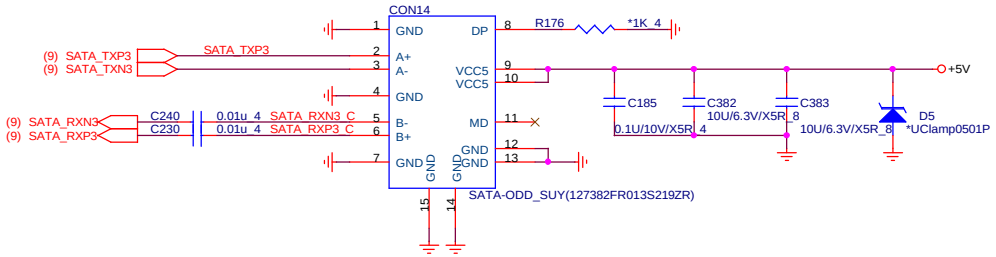
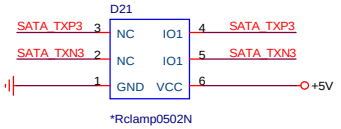
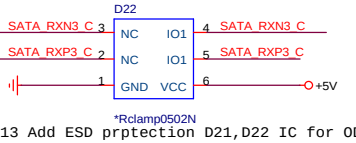
ODD CONNECTOR

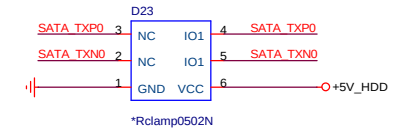
8/18 Change HDD 2nd source connector patt number

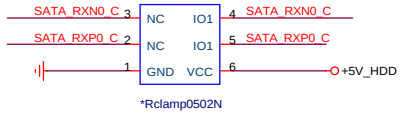






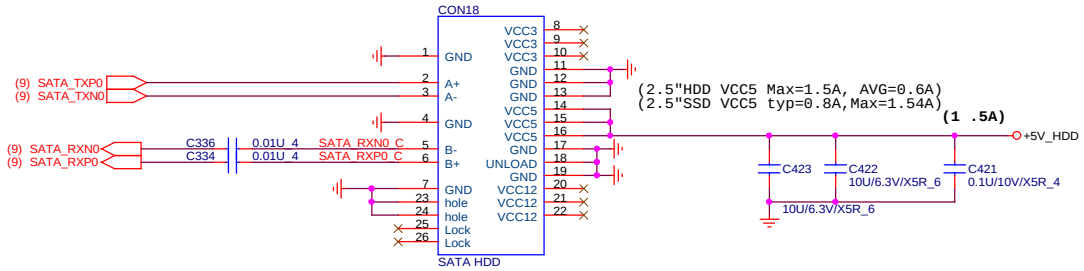
9/13 Add ESD prptection D21,D22 IC for ODD

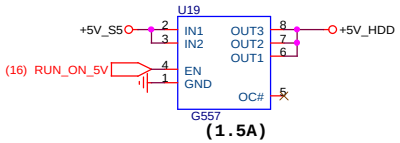




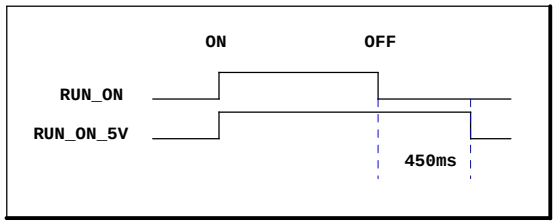
9/13 Add ESD prptection D23,D24 IC for HDD

HDD CONNECTOR

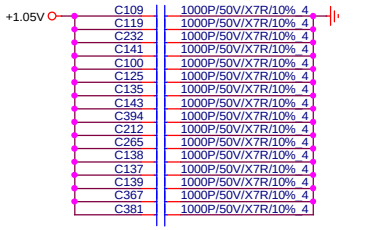


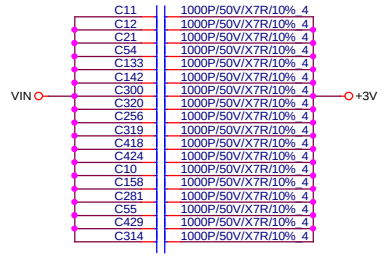


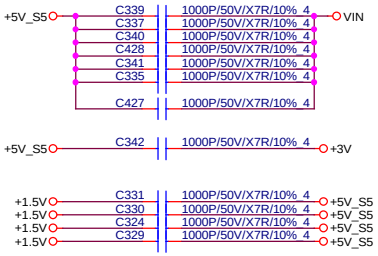
1/18 Change U19 from G547 to G557.

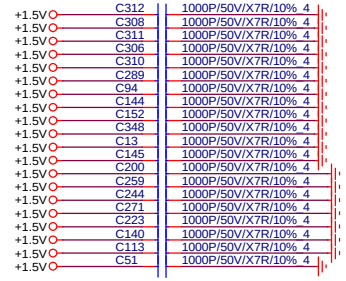


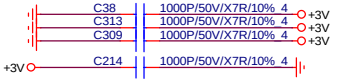
EMI

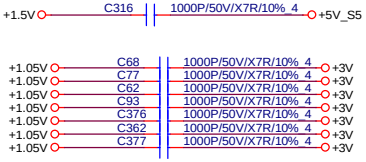


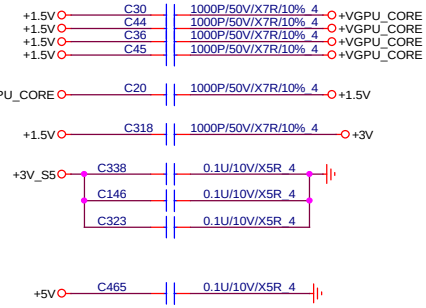


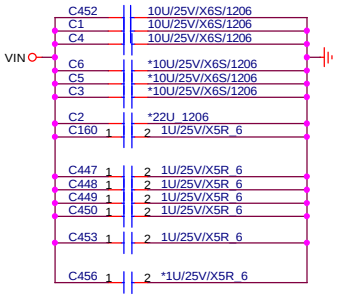


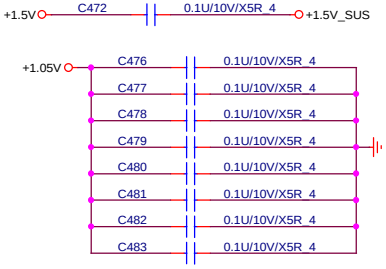


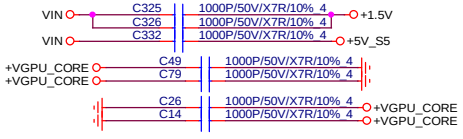












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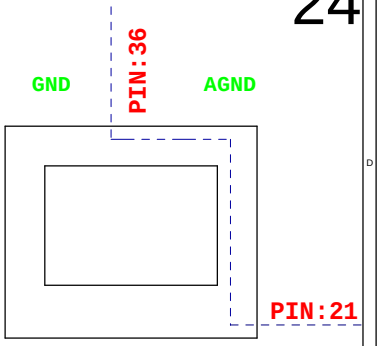
Quanta Computer Inc.
PROJECT :Huron River

Size	Document Number	Rev
	HDD/ODD	1A
Date: Monday, February 21, 2011	Sheet 23 of 39	

AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.
Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms).



CX20671-21Z

Digital Micphone

1/18 Change AL1,AL2,AL3,AL4 from 0ohm to short pad.

1/18 Change AL1~AL4 footprint from 0ohm to short pad

HP

MIC

INT Speaker

Speaker((85205-0400L))

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Quanta Computer Inc.
PROJECT : Huron River

Size	Document Number	Rev
	Audio Codec CX20671	1A
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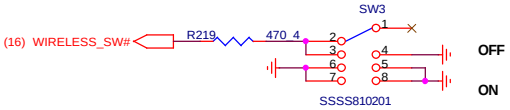
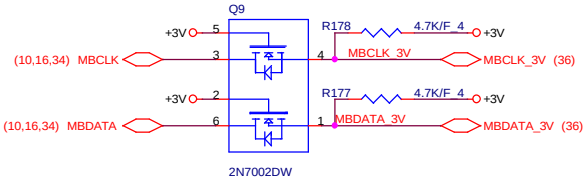
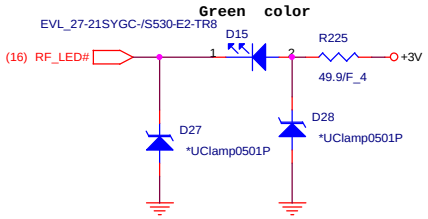
WIRELESS/Bluetooth SWITCH

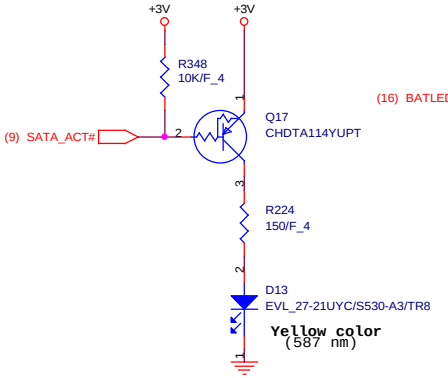




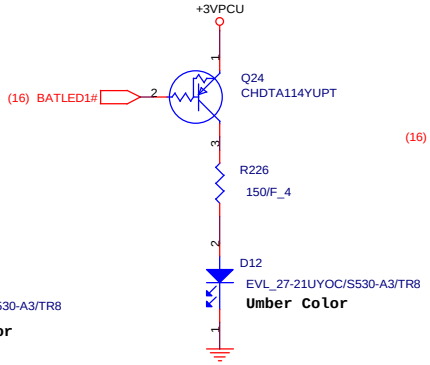
RF LED



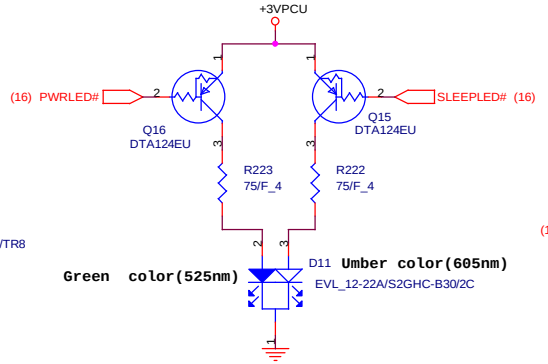
SATA LED



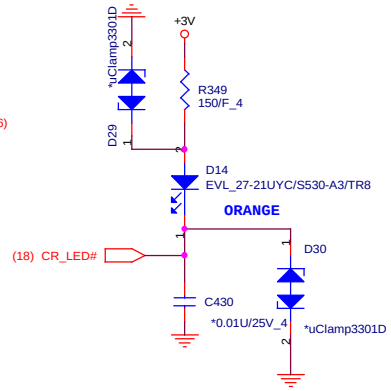
BATTERY LED



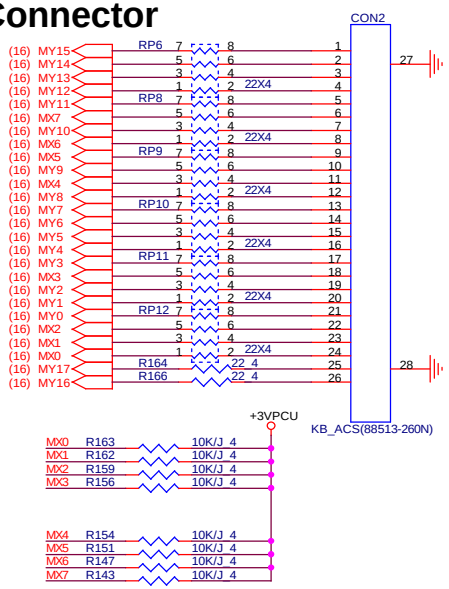
Power/Sleep LED



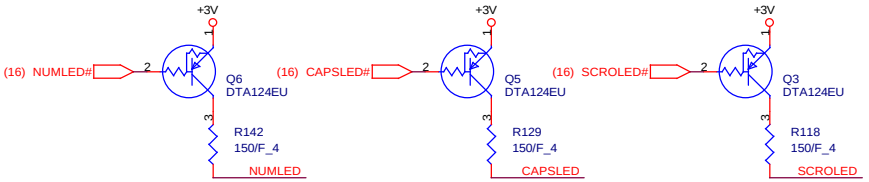
CARD LED

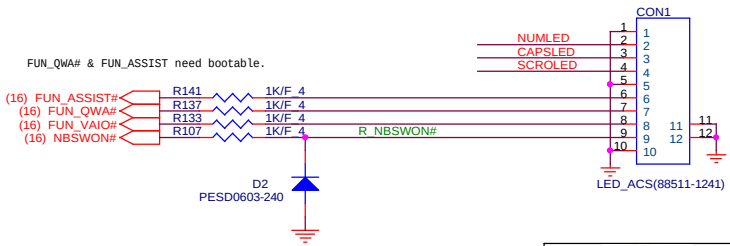


KEY BOARD Connector



Power SW Board Connector





1.Level 1 Environment-related Substances Should Never be Used.
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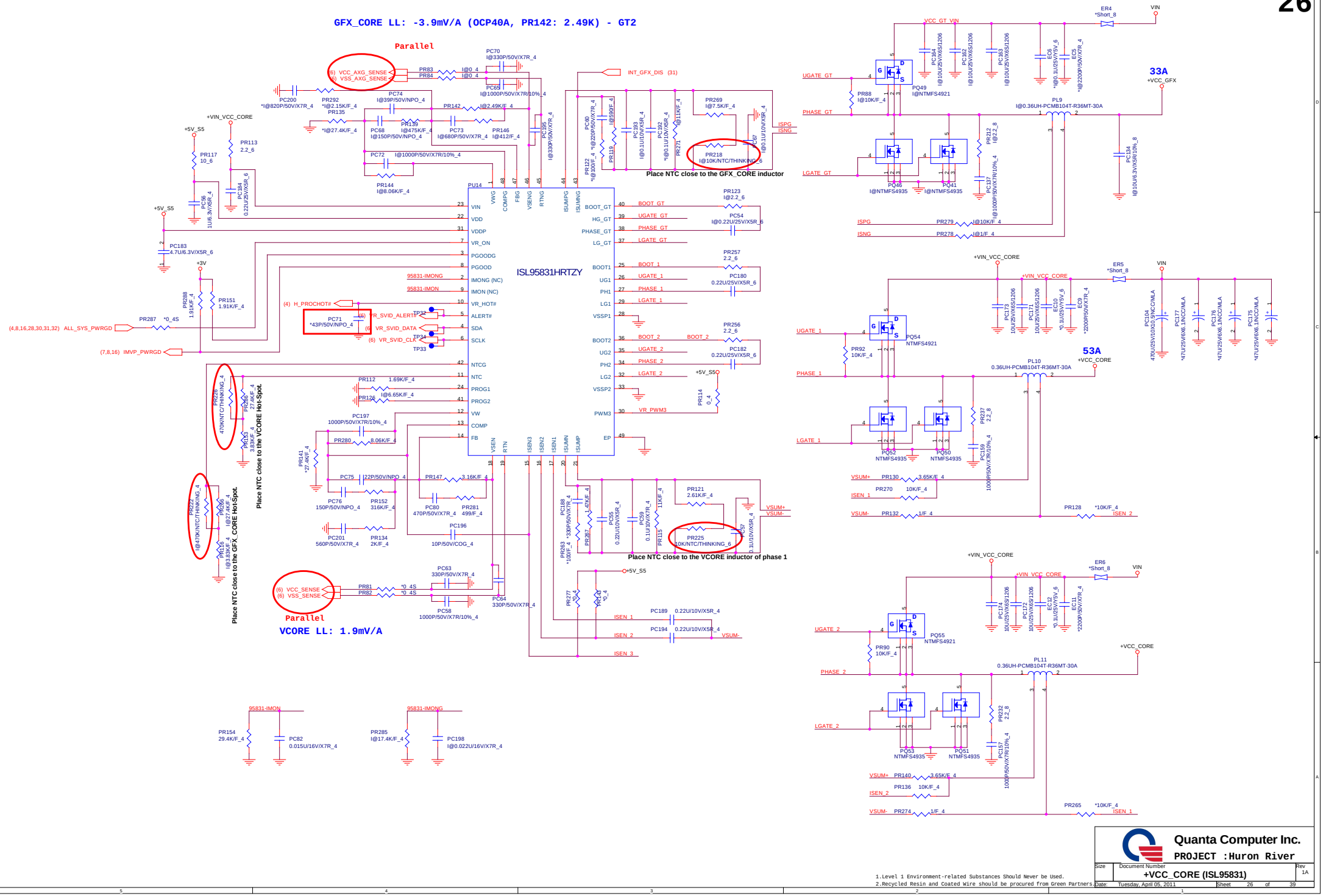
Quanta Computer Inc.
PROJECT :Huron River

Size	Document Number	Rev
	LED/RF/KB/PS	1A
Date:	Wednesday, April 06, 2011	Sheet 25 of 39

GFX_CORE LL: -3.9mV/A (OCP40A, PR142: 2.49K) - GT2



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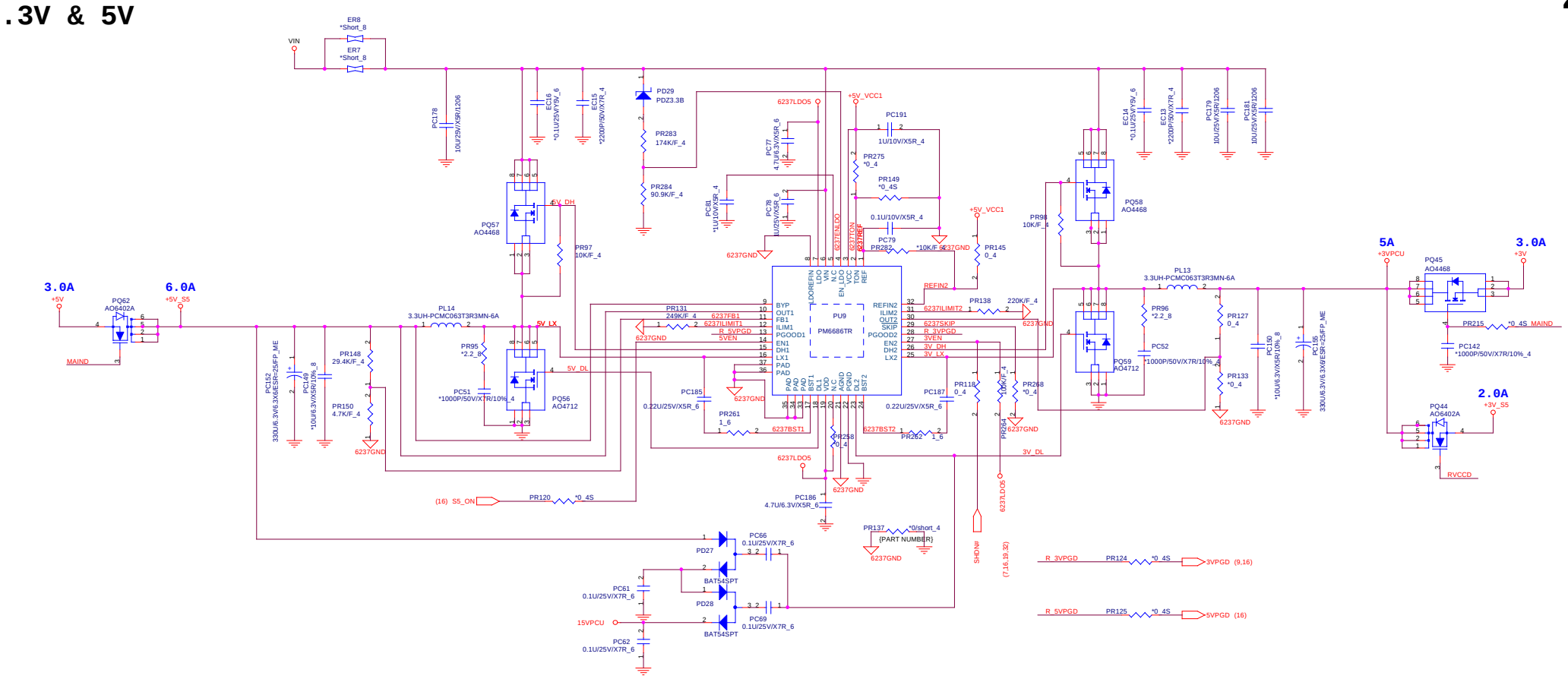
Quanta Computer Inc.
PROJECT :Huron River

Size	Document Number	Rev
	+VCC_CORE (ISL95831)	1A
Date: Tuesday, April 05, 2011	Sheet 26 of 39	

3.3V & 5V



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Quanta Computer Inc.
PROJECT : Huron River

Size	Document Number	Rev
	3VPCU&5VPCU(PM6686)	1A
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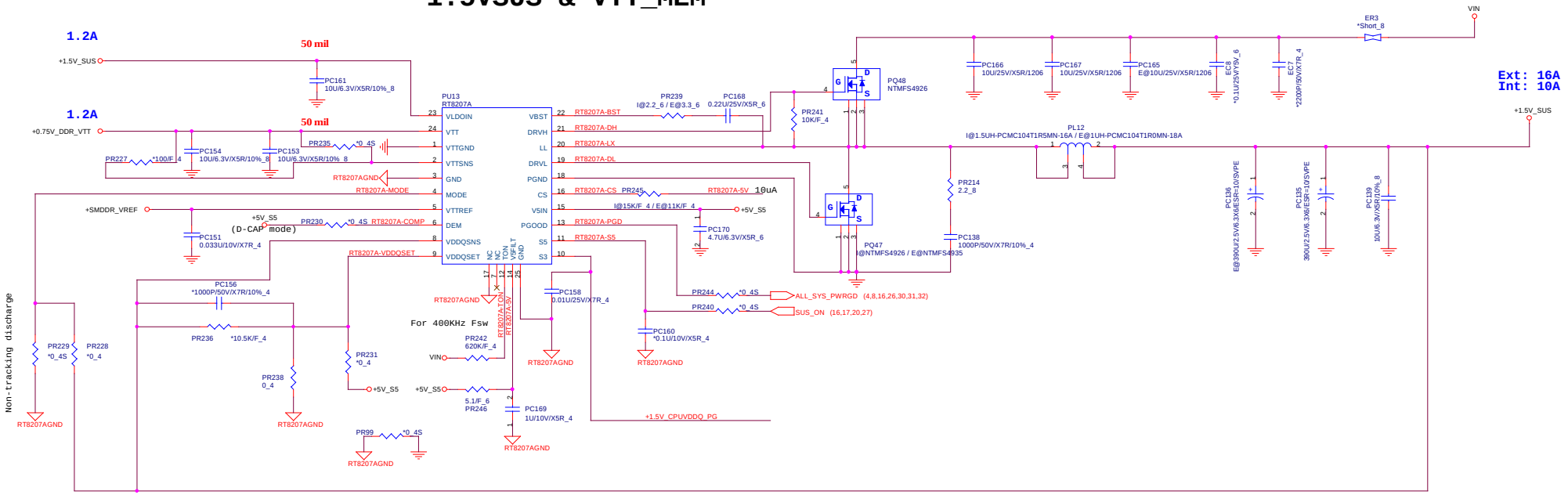
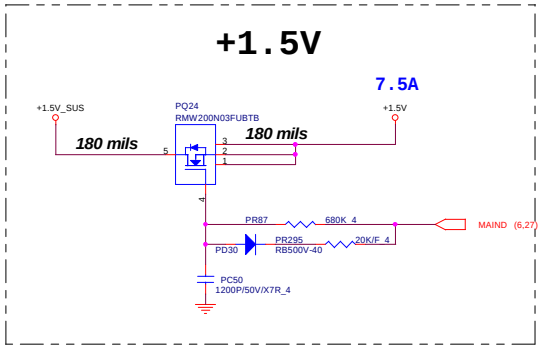
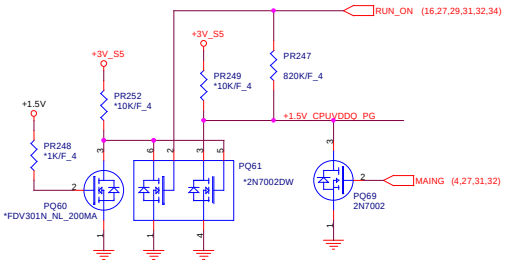
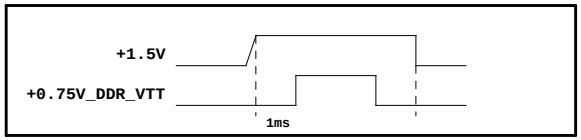
1.5VSUS & VTT_MEM









MODE	DISCHARGE MODE
+5V	No discharge
+1.5V	Tracking discharge
GND	Non-tracking discharge

VDDQSET	VDDQ(V)	VTTREF & VTT	NOTE
GND	1.5 fixed	VDDQSNS/2	DDR3
5V	1.8 fixed	VDDQSNS/2	DDR2
FB-Resistor	Adjustable	VDDQSNS/2	1.5V<VDDQ<3V

VTT = VTTREF = VDDQSNS/2 = 0.75V

STATE	S3	S5	1.5VSUS	VTTREF	VTT
S0	1	1	on	on	on
S3	0	1	on	on	off
S4/S5	0	0	off	off	off

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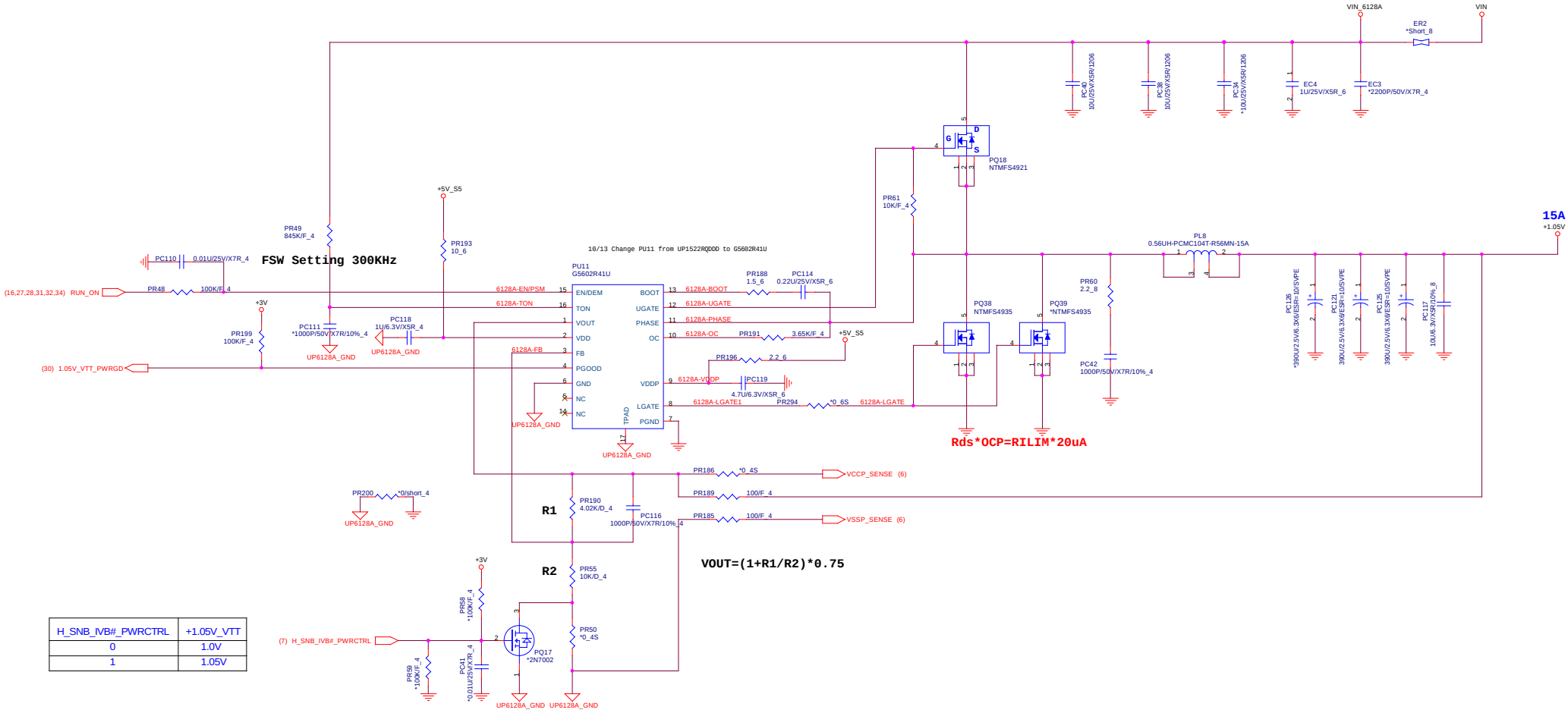
Quanta Computer Inc.
PROJECT : Huron River

Size	Document Number	Rev
	1.5VSUS/VTT_MEM	1A
Date: Tuesday, April 05, 2011	Sheet 28 of 39	

+1.05V / 15.0A



H_SNB_IVB#_PWRCTRL	+1.05V_VTT
0	1.0V
1	1.05V

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Quanta Computer Inc.
PROJECT : Huron River

Size	Document Number	Rev
	+1.05V (UP1522RQDD)-15A	1A

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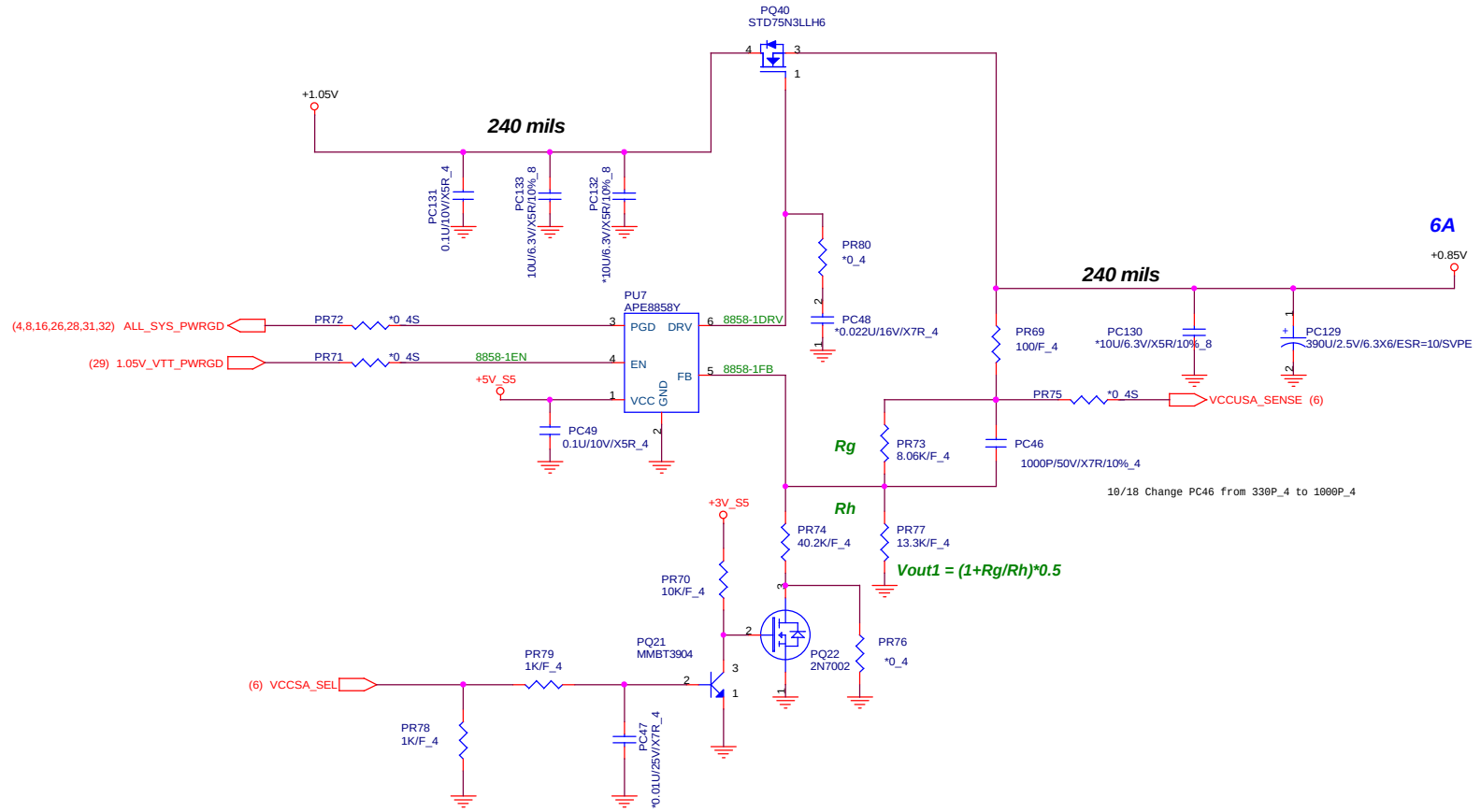
+0.85V



VID 0	VCCSA_SEL	+0.85V
0	0	0.9V
0	1	0.8V
1	0	0.75V
1	1	0.65V

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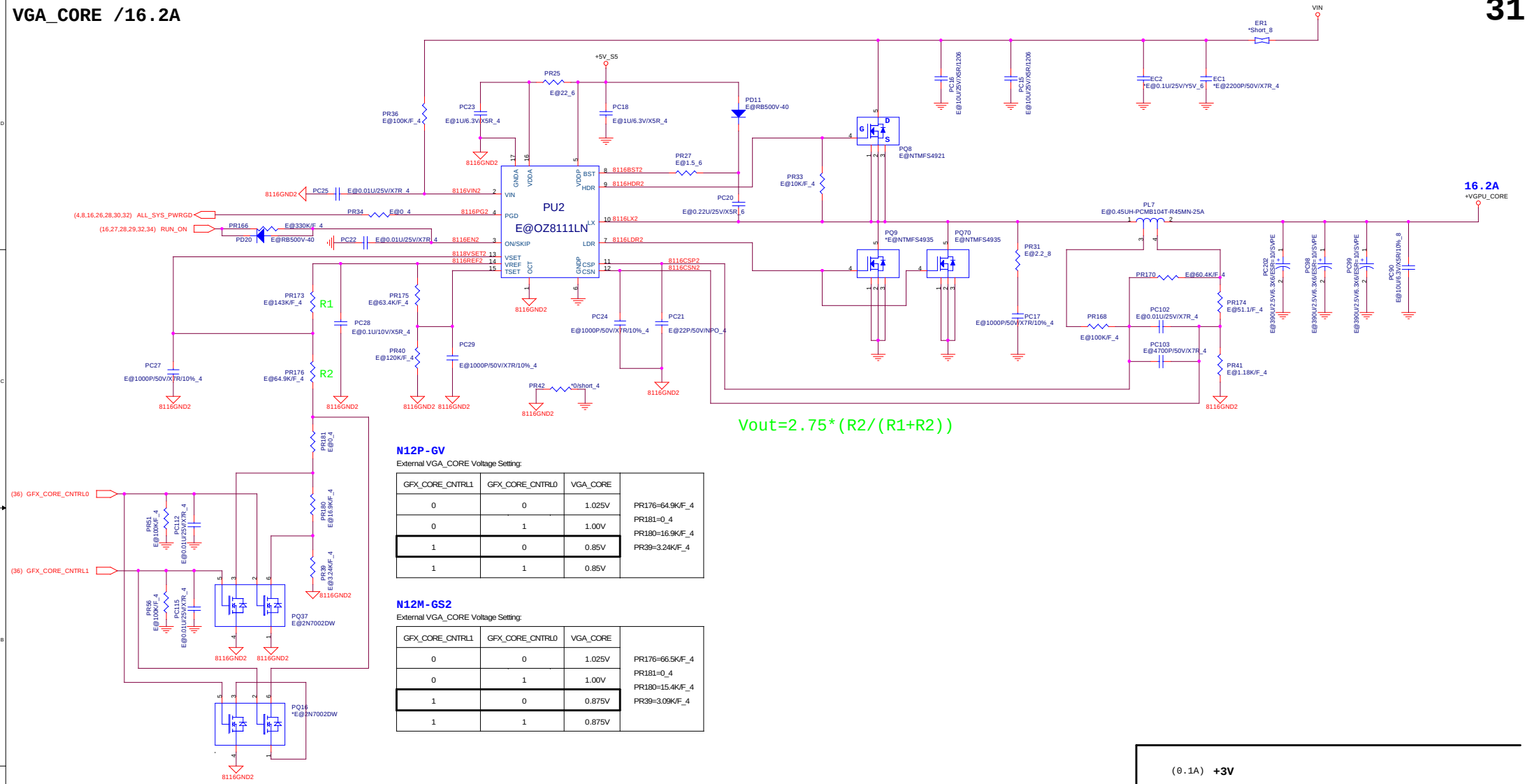
Quanta Computer Inc.
PROJECT : Huron River

Size	Document Number	Rev
	+0.85V(OZ8116LN)	1A
Date: Tuesday, April 05, 2011	Sheet 30 of 39	

VGA_CORE /16.2A



Vout=2.75*(R2/(R1+R2))

N12P-GV

External VGA_CORE Voltage Setting:

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	VGA_CORE	
0	0	1.025V	PR176=64.9K/F_4
0	1	1.00V	PR181=0_4
1	0	0.85V	PR180=16.9K/F_4
1	1	0.85V	PR39=3.24K/F_4

N12M-GS2

External VGA_CORE Voltage Setting:

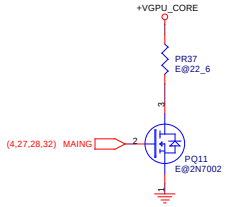
GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	VGA_CORE	
0	0	1.025V	PR176=66.5K/F_4
0	1	1.00V	PR181=0_4
1	0	0.875V	PR180=15.4K/F_4
1	1	0.875V	PR39=3.09K/F_4

(0.1A) **+3V**

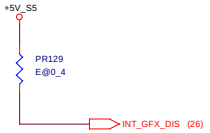
(2A) **+1.05V**

(6A) **+1.5V**

Dis-charge



UMA_GFX_DISABLE



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : Huron River

Size	Document Number	Rev
	VGA_CORE(OZ8111)-15A	1A

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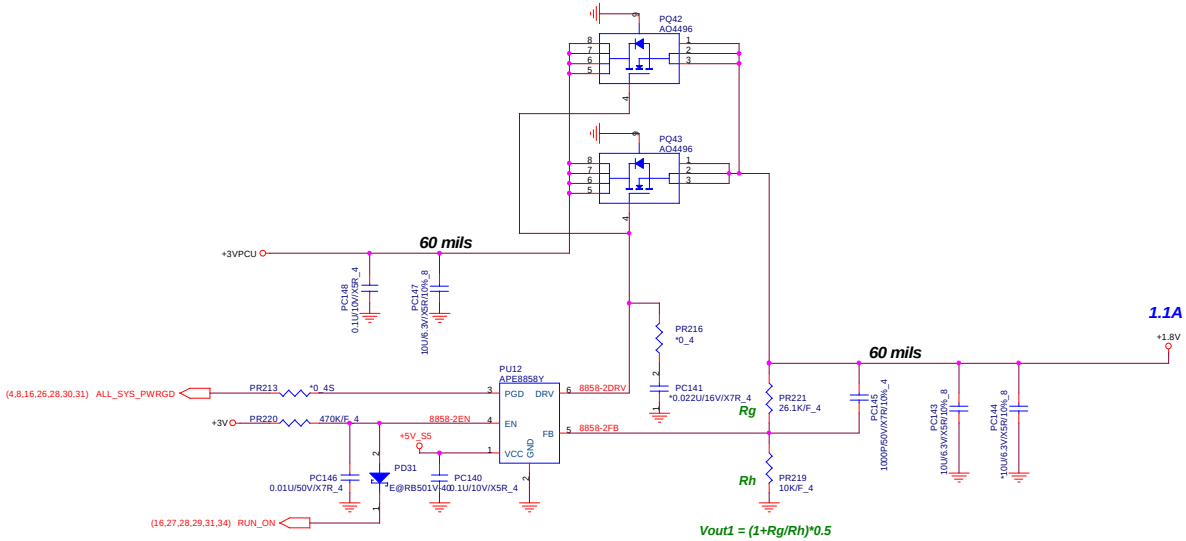
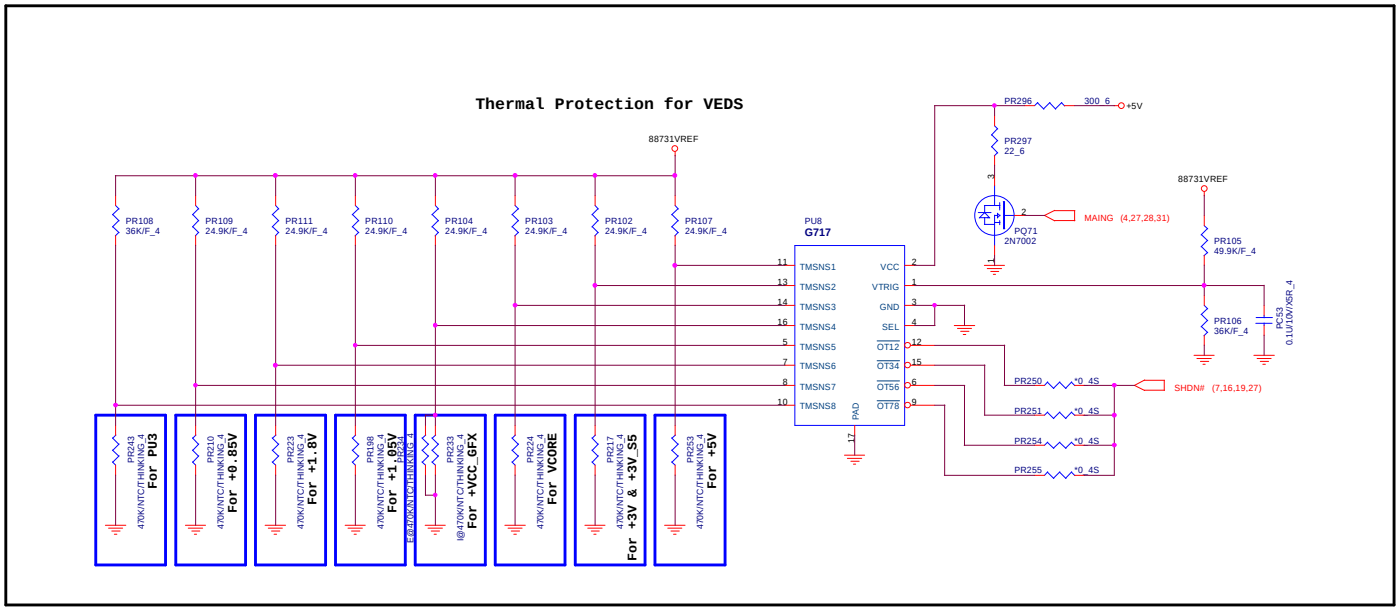
VCC1.8





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PROJECT : Huron River

Size	Document Number	Rev
	VCC1.8	1A
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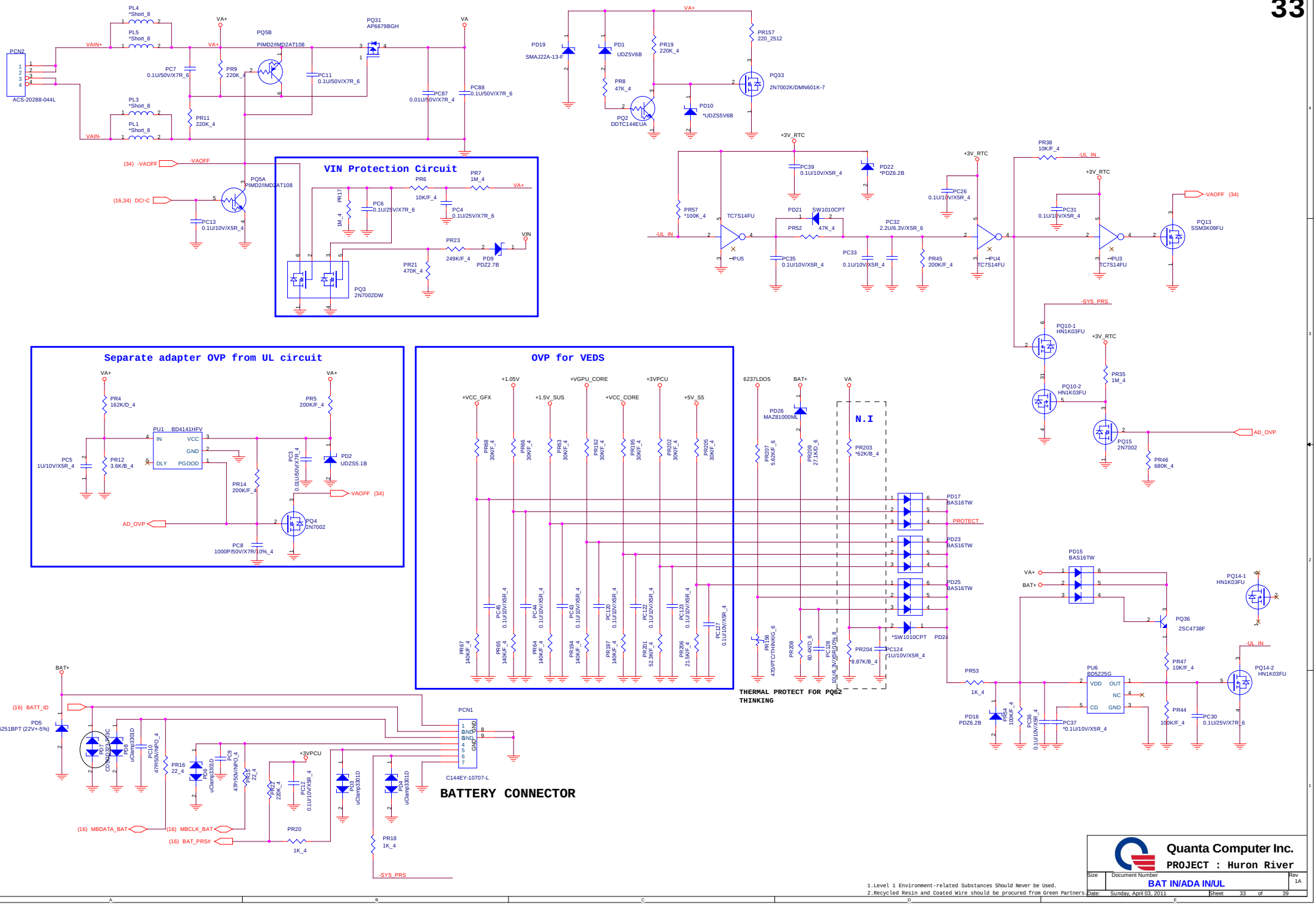

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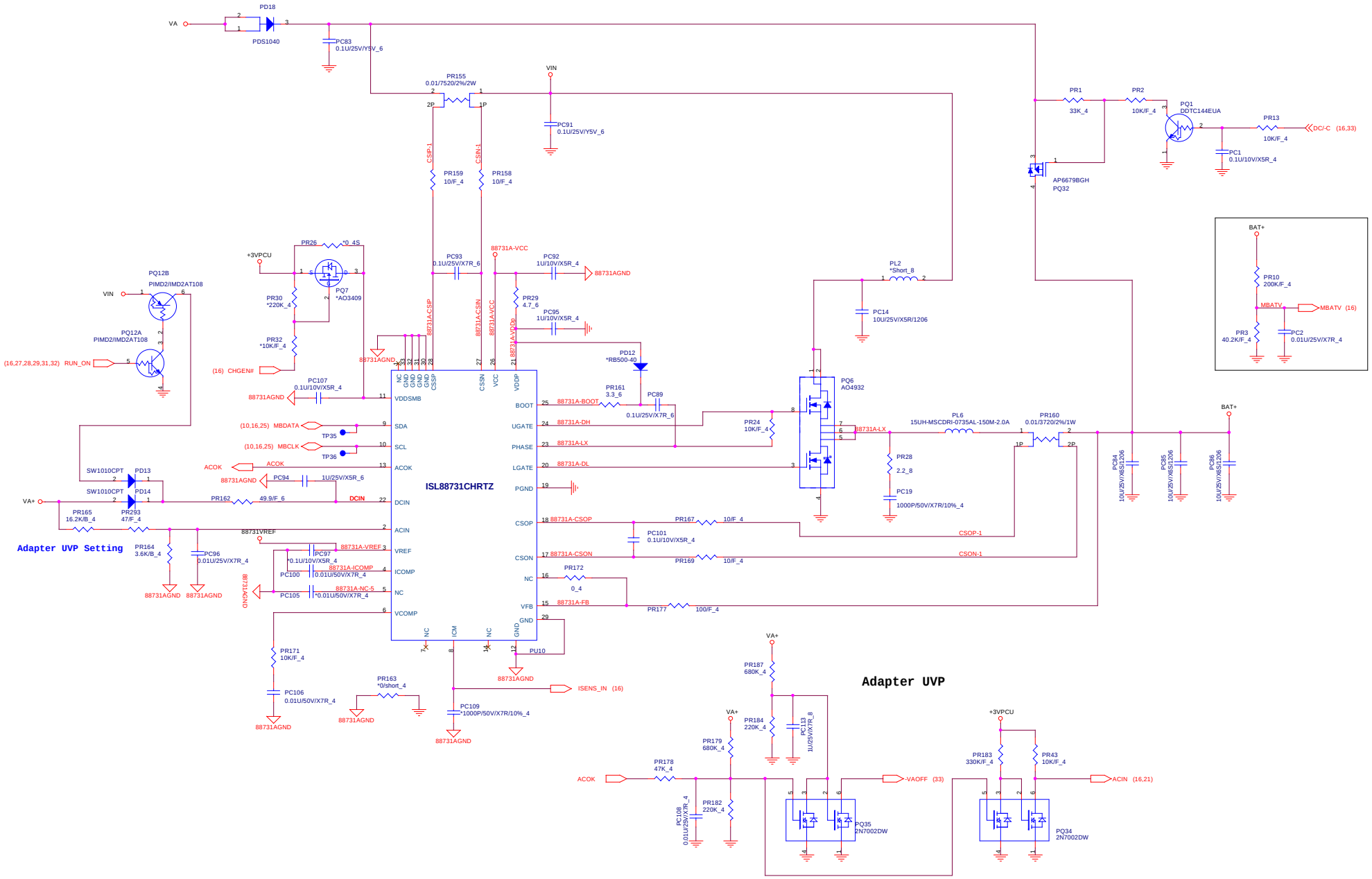
PROJECT : Huron River

Size	Document Number	Rev
	BAT IN/ADA IN/UL	1A
Date: Sunday, April 03, 2011	Sheet 33 of 39	



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PROJECT : Huron River

Size	Document Number	Rev
	CHARGER(ISL88731A)	1A
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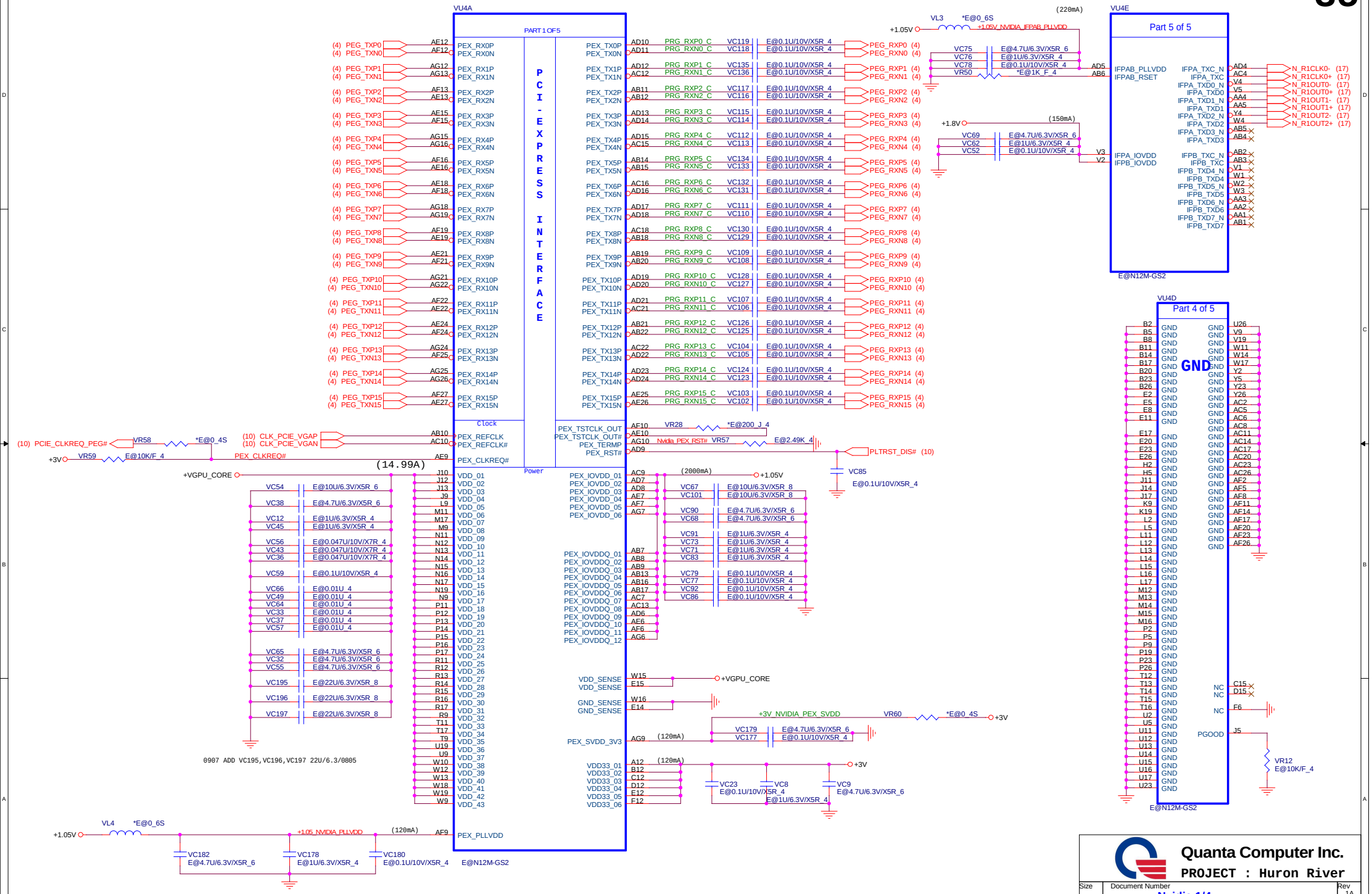

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PROJECT : Huron River

Size	Document Number	Rev
	Nvidia 1/4	1A

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N12P-GV

External VGA_CORE Voltage Setting:

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	VGA_CORE	
0	0	1.025V	PR176=64.9K/F_4
0	1	1.00V	PR181=0_4
1	0	0.85V	PR180=16.9K/F_4
1	1	0.85V	PR39=3.24K/F_4

N12M-GS2

External VGA_CORE Voltage Setting:

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	VGA_CORE	
0	0	1.025V	PR176=66.5K/F_4
0	1	1.00V	PR181=0_4
1	0	0.875V	PR180=15.4K/F_4
1	1	0.875V	PR39=3.09K/F_4

Logical Strap Bit Mapping

Resister Value	Pull to VDD	Pull to GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

N12M Strap Bit Define

Straps	Bit 3	Bit 2	Bit 1	Bit 0
ROM_SO	FB[1]	FB[1]	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG [3]	3GIO_PADCFG [2]	3GIO_PADCFG [1]	3GIO_PADCFG [0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33

for device ID

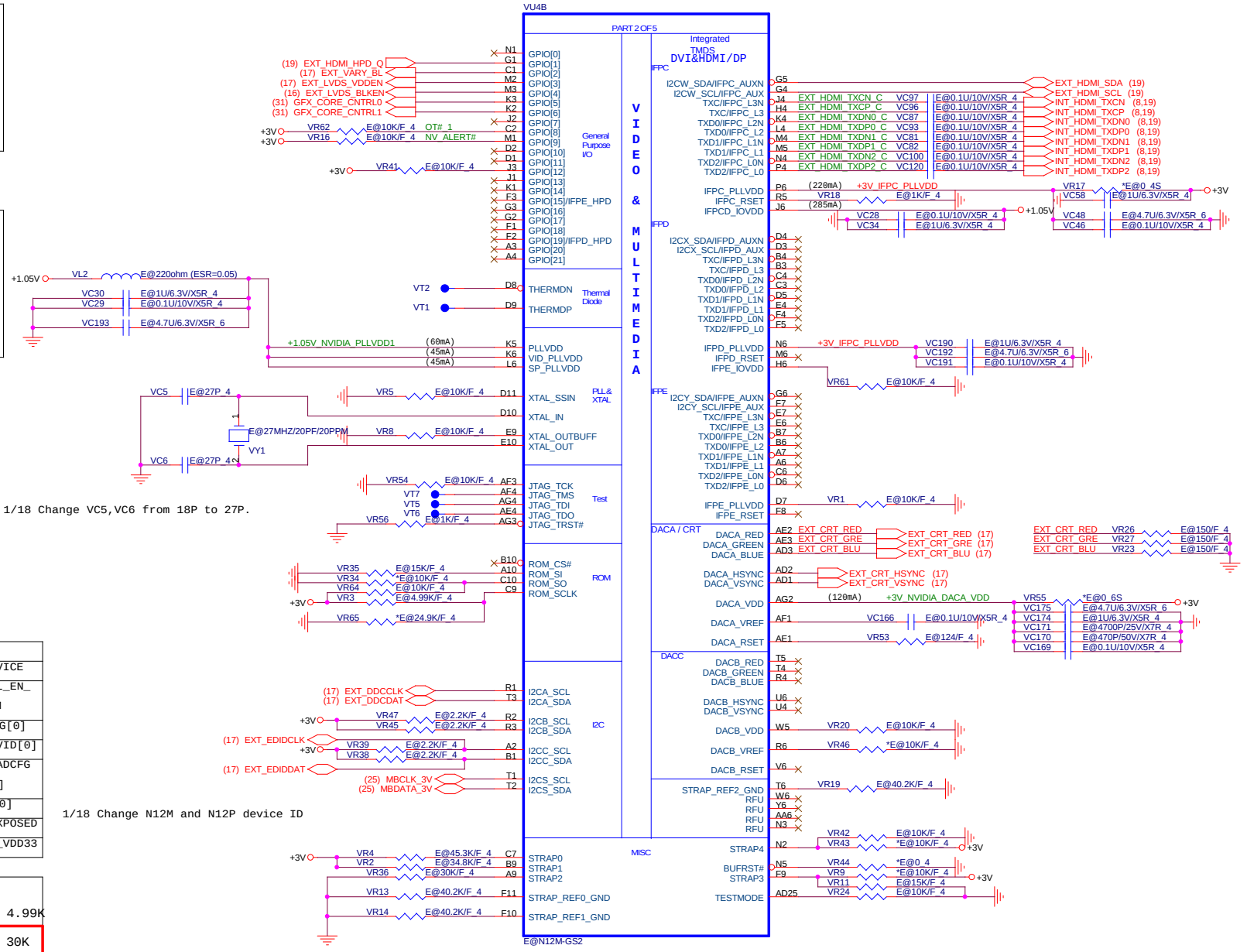
For N12P VR3 pull high 4.99K VR65 NC VR36 Pull down 4.99K

For N12M VR3 pull high 4.99K VR65 NC VR36 Pull down 30K

	VRAM Capacity	VRAM Vender	ID	VR35	P/N	P/N
N12M	64Mx16 DDR3	Hynix	0010	PD15K	H5TQ1G63DFR-12C	
		Samsung	0011	PD20K	K4W1G1646G-BC12	
	128Mx16 DDR3	Hynix	0110	PD35K	H5TQ2G63BFR-12C	
		Samsung	0111	PD45K	K4W2G1646C-HC12	

1/18 Change VC5,VC6 from 18P to 27P.

1/18 Change N12M and N12P device ID



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PROJECT : Huron River

Size	Document Number	Rev
	Nvidia 2/4	2A

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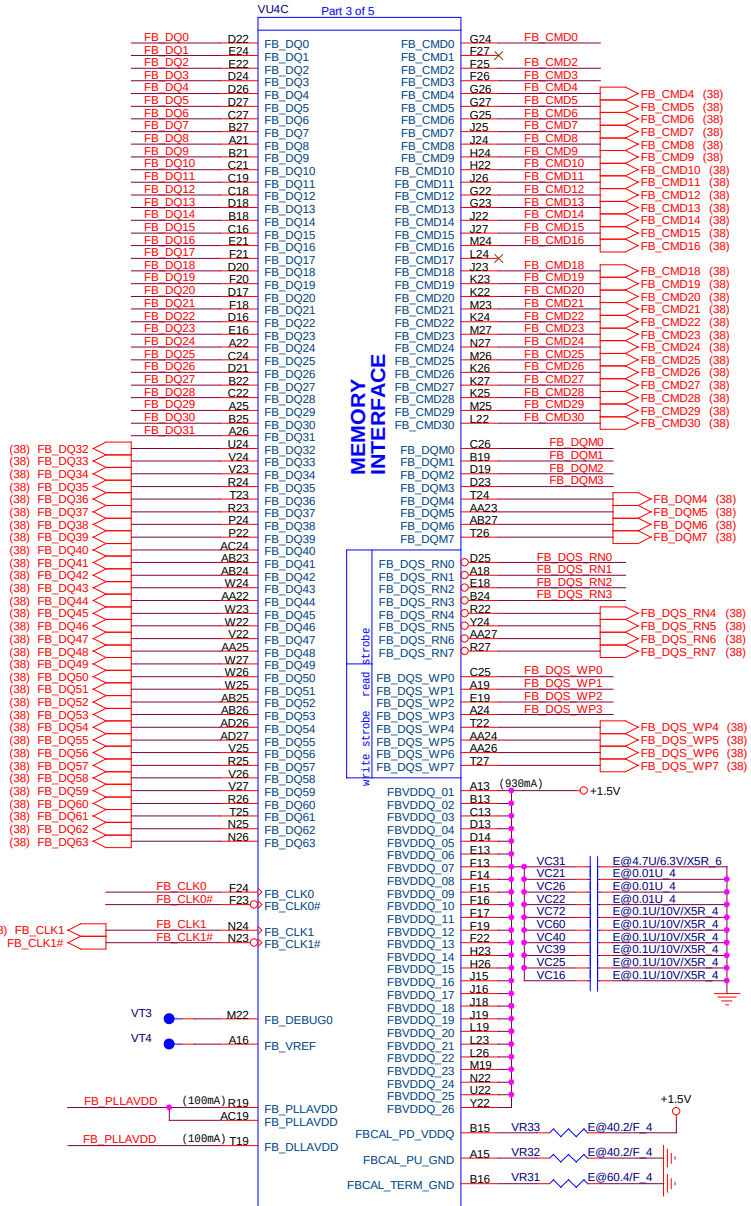
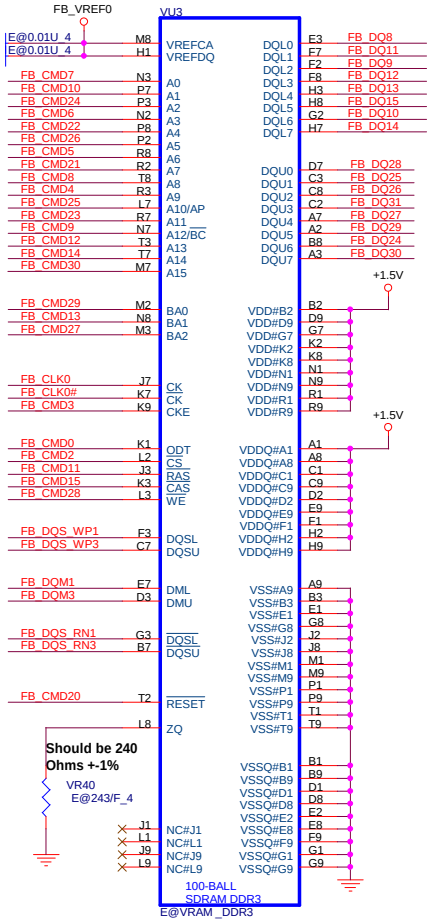
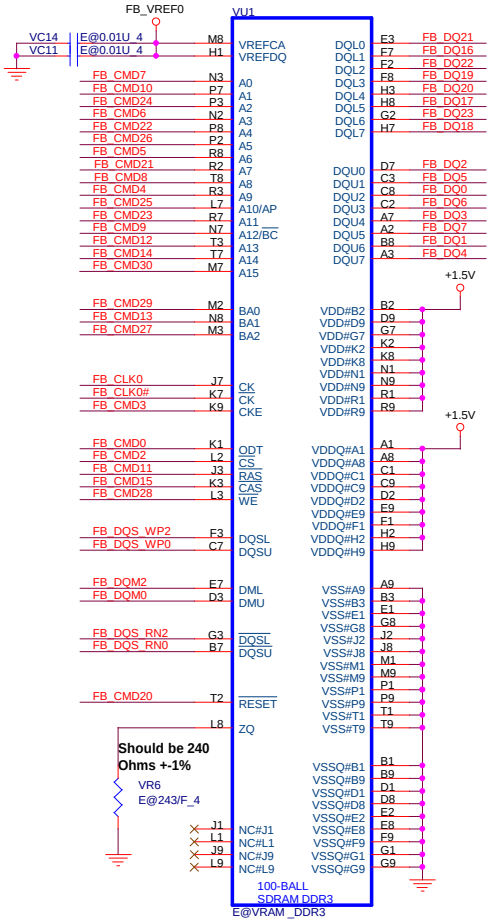
Down Side VRAM TOP/BOT

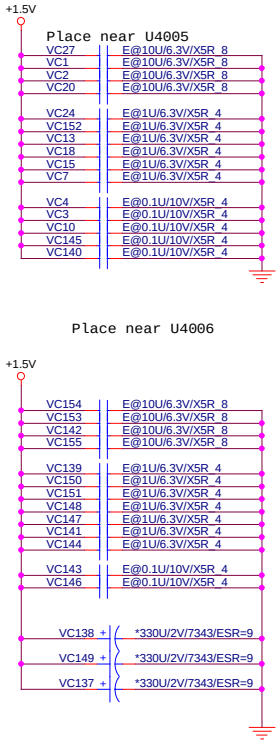
TOP

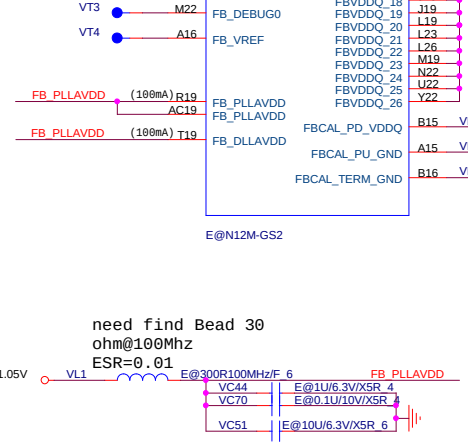


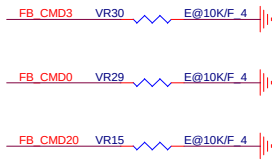


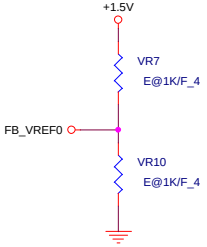
BOT

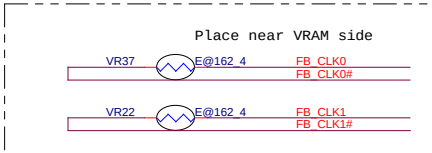












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PROJECT : Huron River

Size	Document Number	Rev
	VRAM 3/4	2A

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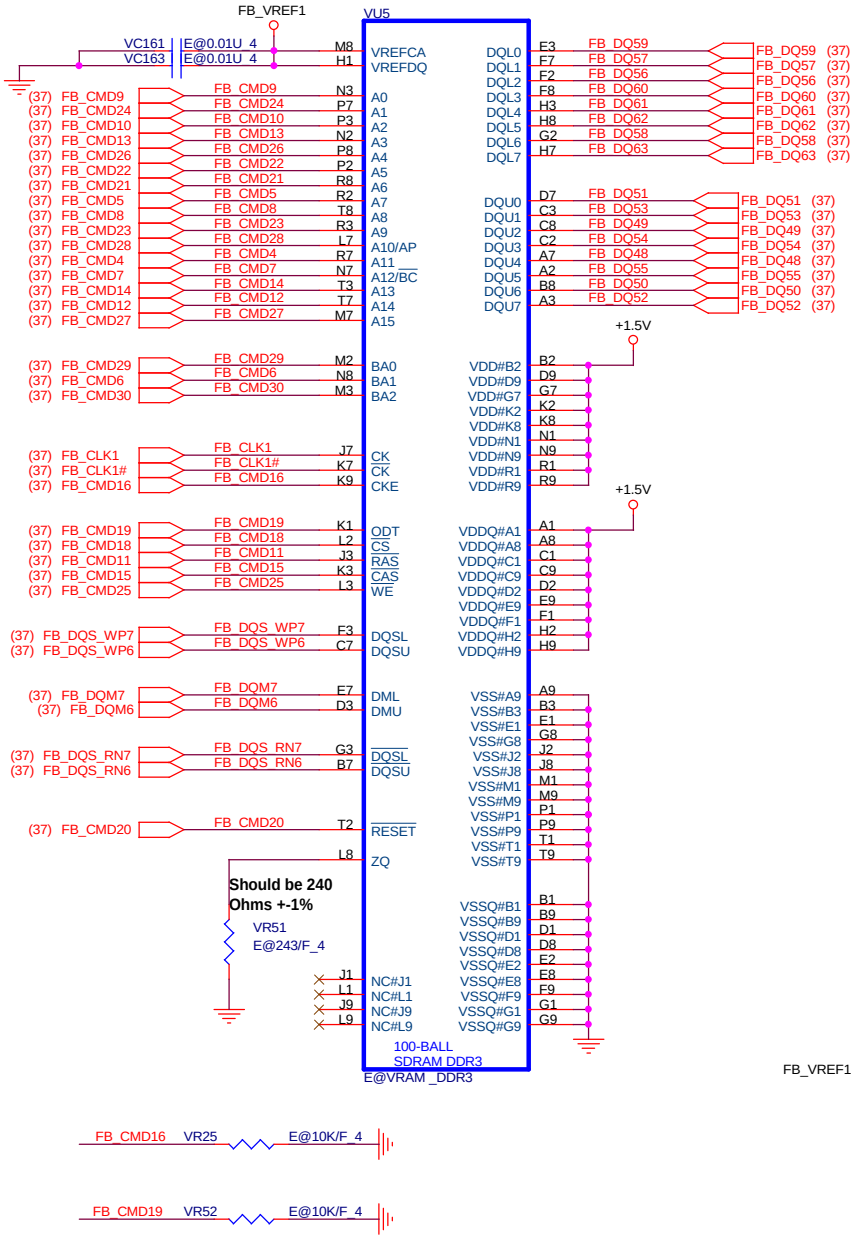
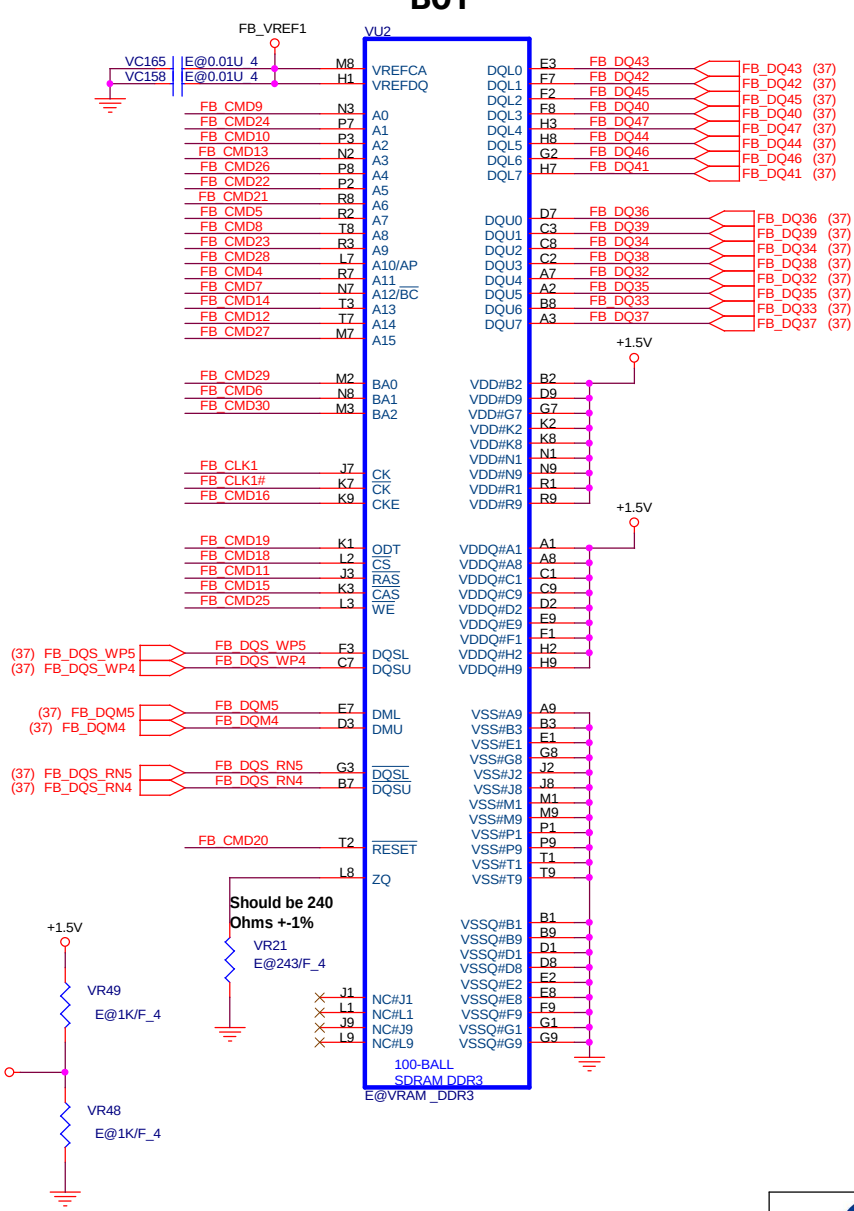
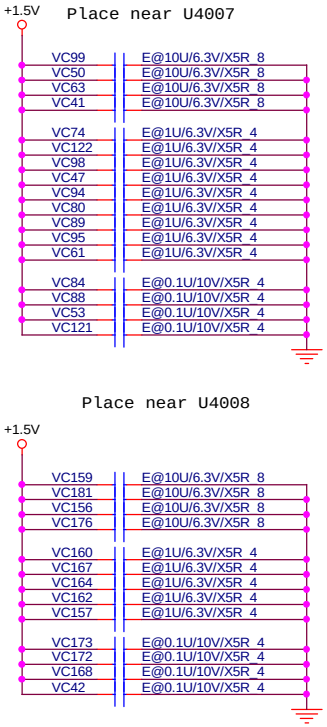
Up Side VRAM TOP/BOT

TOP



BOT





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PROJECT : Huron River

Size	Document Number	Rev
	VRAM 4/4	1A
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USB PORT Architecture for EVT	
PORT 0	IO Port
PORT 1	IO Port
PORT 2	IO Port
PORT 3	N/A
PORT 4	IO Port
PORT 5	N/A
PORT 6	N/A
PORT 7	N/A
PORT 8	N/A
PORT 9	Camera
PORT 10	N/A
PORT 11	N/A
PORT 12	WiMax
PORT 13	BlueTooth

PCIE BUS	
PORT 1	WLAN Port
PORT 2	N/A
PORT 3	N/A
PORT 4	CARD READER
PORT 5	N/A
PORT 6	GLAN(RTL8111E)
PORT 7	N/A
PORT 8	N/A

SM BUS	MBCLK/MBDATA
ISL88731CHRTZ	0001 001X
NVIDIA	1001 111X

SATA BUS	
PORT 0	HDD
PORT 1	N/A
PORT 2	N/A
PORT 3	ODD
PORT 4	N/A

Board ID0 (N12M/N12P)	N12M	N12P
R294	Stuff	No Stuff
R297	No Stuff	Stuff

Board ID1 (VRAM Vendor)	Samaung	Hynix
R47	Stuff	No Stuff
R48	No Stuff	Stuff

Board ID2 (VRAM 1G/512M)	1G	512M
R39	Stuff	No Stuff
R27	No Stuff	Stuff

	DGPU_PRSNT#(GPIO39)	BOARD_ID0 (GPIO16)	BOARD_ID1(GPIO6)	BOARD_ID2(GPIO17)
UMA	0	0	0	0
N12M-GS2_SAM_512MB	1	1	1	0
N12M-GS2-SAM_1GB	1	1	1	1
N12M-GS2-HYN_512MB	1	1	0	0
N12M-GS2-HYN_1GB	1	1	0	1
N12P-GV_SAM_512MB	1	0	1	0
N12P-GV-SAM_1GB	1	0	1	1
N12P-GV-HYN_512MB	1	0	0	0
N12P-GV-HYN1_1GB	1	0	0	1