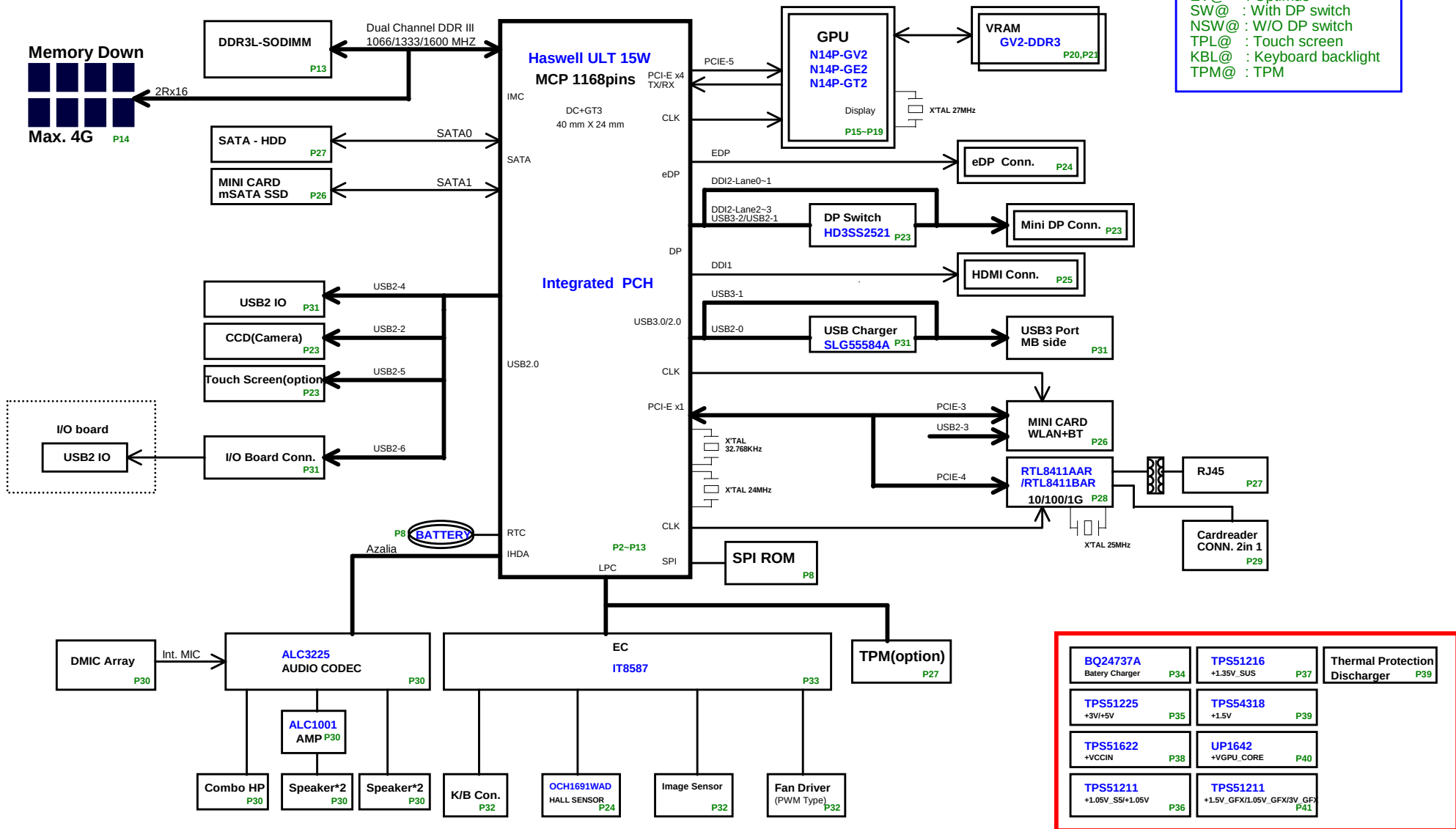


ZRQ_GDDR3 SHB ULT SYSTEM BLOCK DIAGRAM

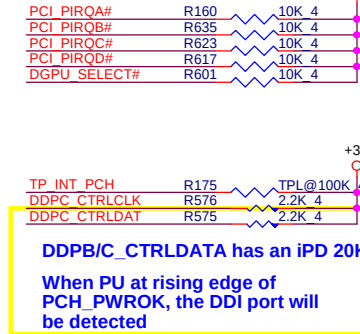
BOM

01

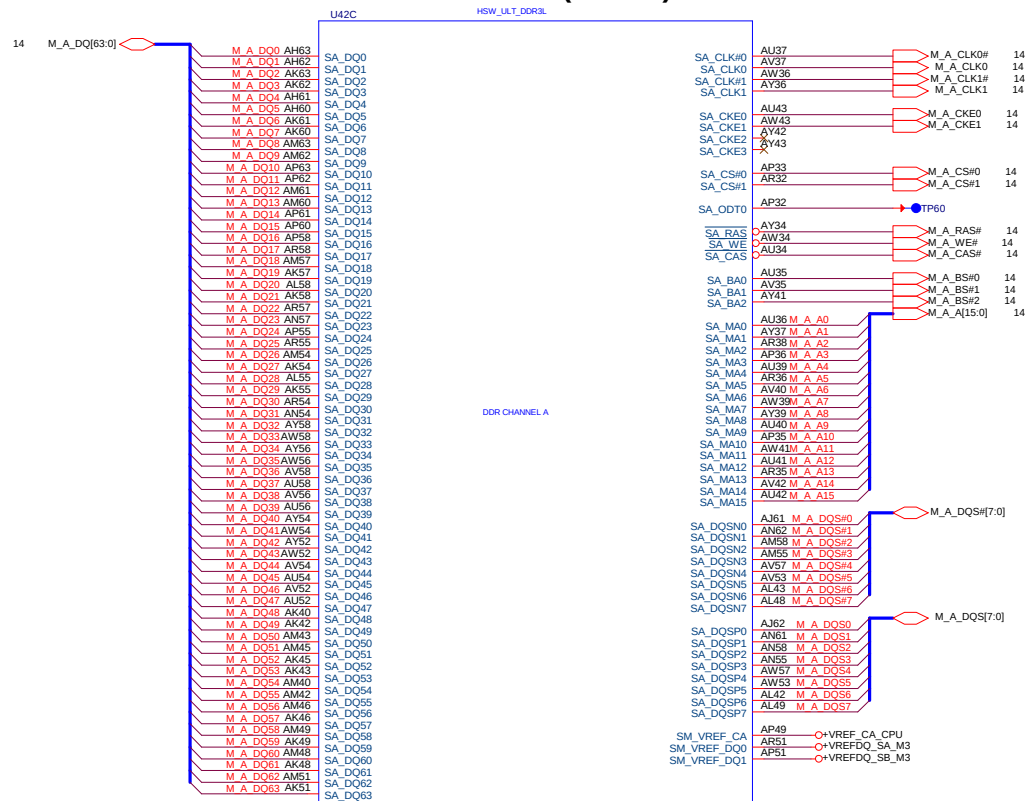
IV@ : iGPU
EV@ : Optimus
SW@ : With DP switch
NSW@ : W/O DP switch
TPL@ : Touch screen
KBL@ : Keyboard backlight
TPM@ : TPM



02

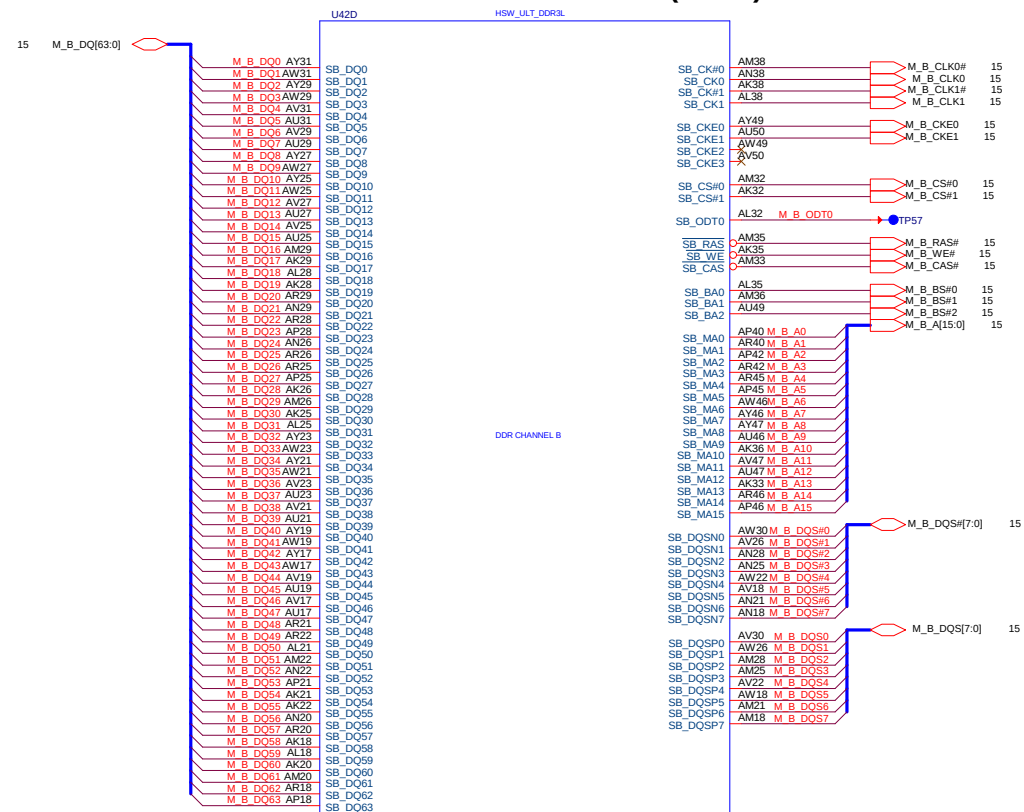


Haswell ULT (DDR3L)



3 OF 19

Haswell Processor (DDR3)



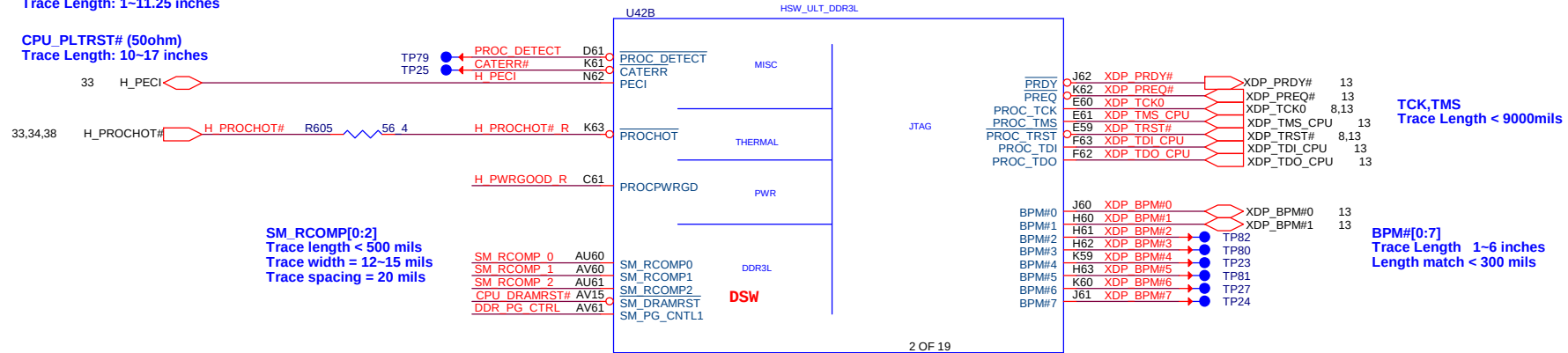
4 OF 19

Haswell ULT (SIDE BAND)

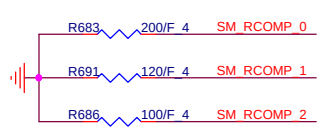
H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 inches

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

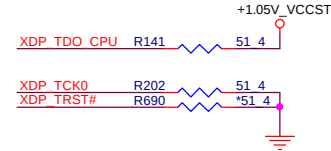
CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches



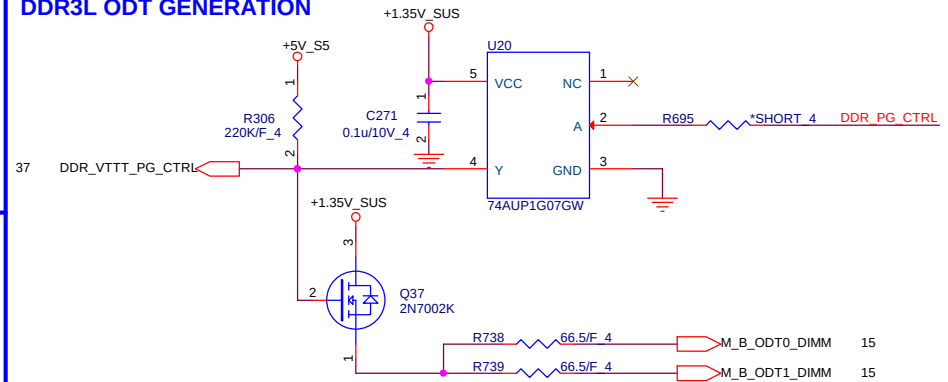
DRAM COMP



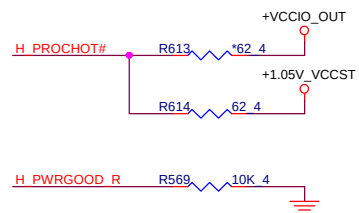
XDP PU/PD



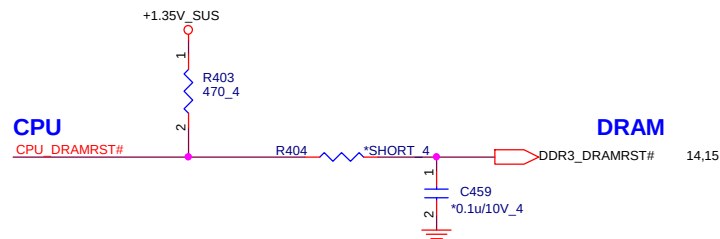
DDR3L ODT GENERATION



PU/PD of CPU



DRAMRST



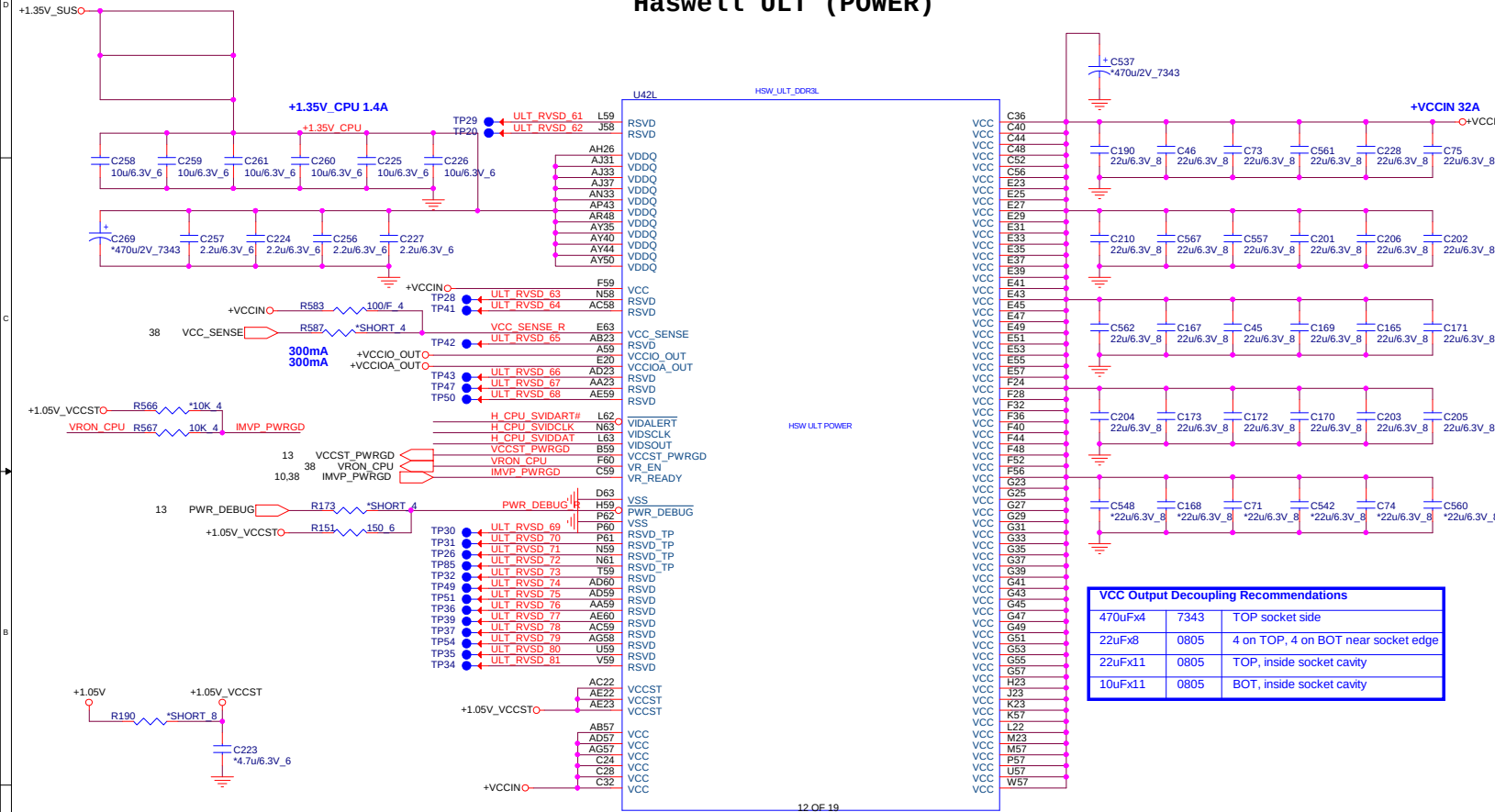
Quanta Computer Inc.

PROJECT : ZRQ

Size	Document Number	Rev
	Haswell 1/5 (PEG/DIM/FDI)	3A
Date:	Friday, April 12, 2013	Sheet 4 of 47

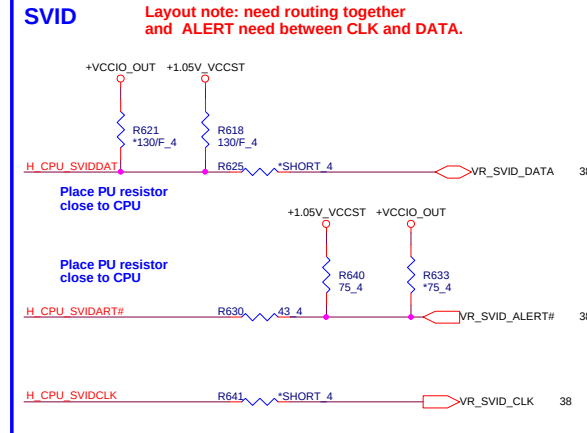
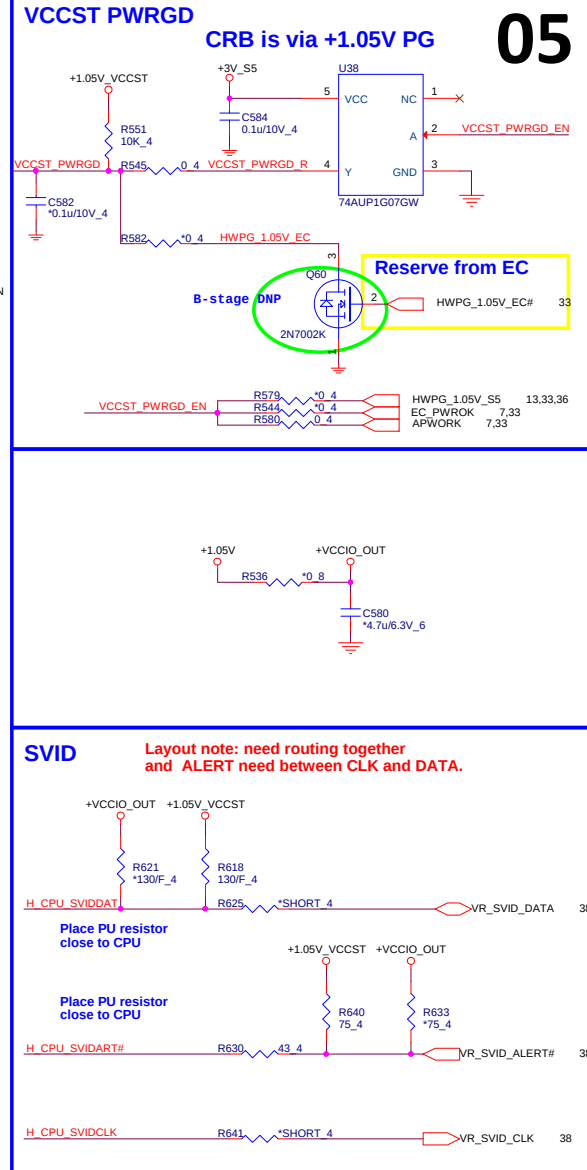
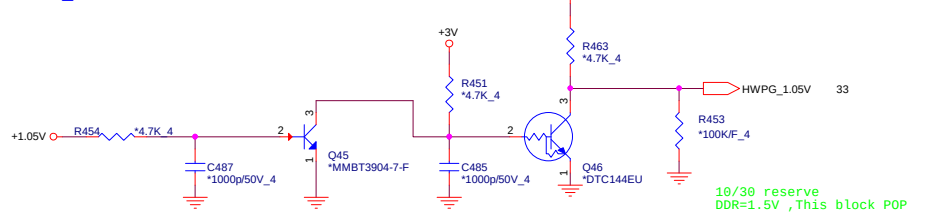
VDDQ Output Decoupling Recommendations			
330uFx2	7343	BOT socket side	
22uFx11	0805	5 on TOP, 6 on BOT inside socket cavity	
10uFx10	0805	5 on TOP, 5 on BOT inside socket cavity	

Haswell ULT (POWER)



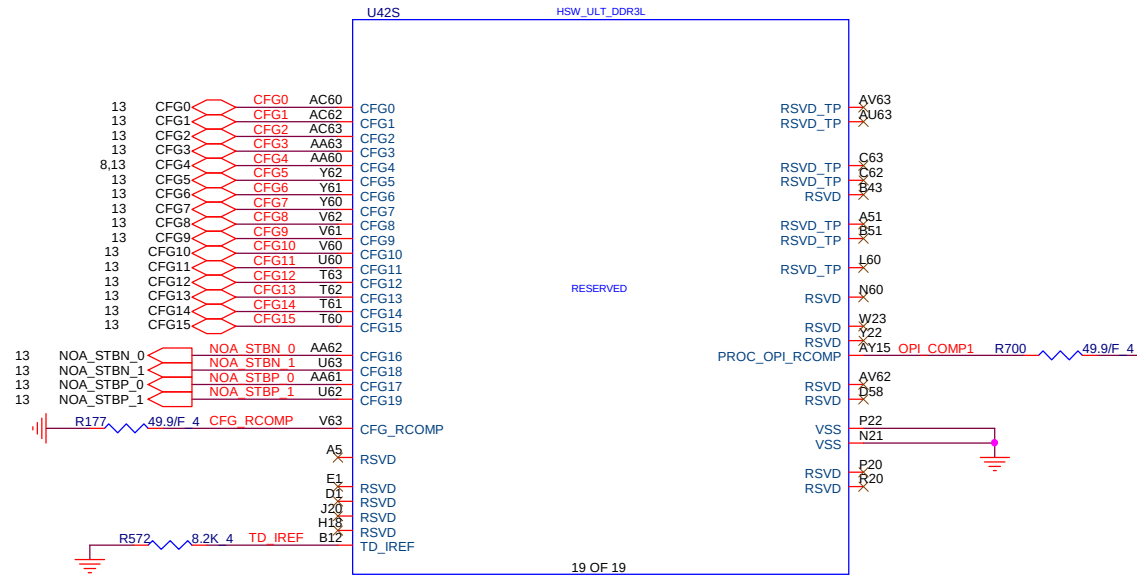
VCC Output Decoupling Recommendations			
470uFx4	7343	TOP socket side	
22uFx8	0805	4 on TOP, 4 on BOT near socket edge	
22uFx11	0805	TOP, inside socket cavity	
10uFx11	0805	BOT, inside socket cavity	

HWPG_1.05V for DDR=1.5V



Haswell ULT (CFG, RSVD)

06



Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R203 *1K 4
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R184 *1K 4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R192 *1K 4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R171 *1K 4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R172 *1K 4
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R183 *1K 4



Quanta Computer Inc.
PROJECT : ZRQ

Size	Document Number	Rev
	Haswell 5/5 (CFG/GND)	3A
Date: Friday, April 12, 2013	Sheet	6 of 47



5.33

APWORK

R413 0.4

APWROK R

Speed up 250ms to boot up for EC power on 250 ms

R414 10K_4

```
graph LR
    APWORK --- R413[R413 0.4]
    R413 --- APWROK_R[APWROK R]
    APWROK_R --- R414[R414 10K_4]
    R414 --- GND[Ground]
```

PCH ACPRESENT
 PCH BATLOW#
 PCIE LAN WAKE#
 PCH PWRBTN#

R259 *10K 4
 R262 *8.2K 4
 R264 *10K 4
 R261 *10K 4

R272 *10K 4
 R275 *8.2K 4
 R276 *1K 4
 R273 *10K 4

+3V_S5
 +3VP1U

Non Deep Sx

The schematic diagram illustrates the Non Deep Sx circuit. It features a 3V_S5 supply connected to a network of components. A capacitor C282 (0.33u/10V_6) is connected to the 3V_S5 supply. A resistor R302 (100K_4) is connected to the other end of C282. A resistor R300 (0.6) is connected to the 3V_S5 supply and the gate of MOSFET Q34 (AO3413). MOSFET Q34 is connected to the 3VCC_S5 supply. A resistor R303 (SHORT_6) is connected to the drain of Q34. MOSFET Q35 (2N7002K) is connected to the PCH_SLP_SUS# signal and ground.

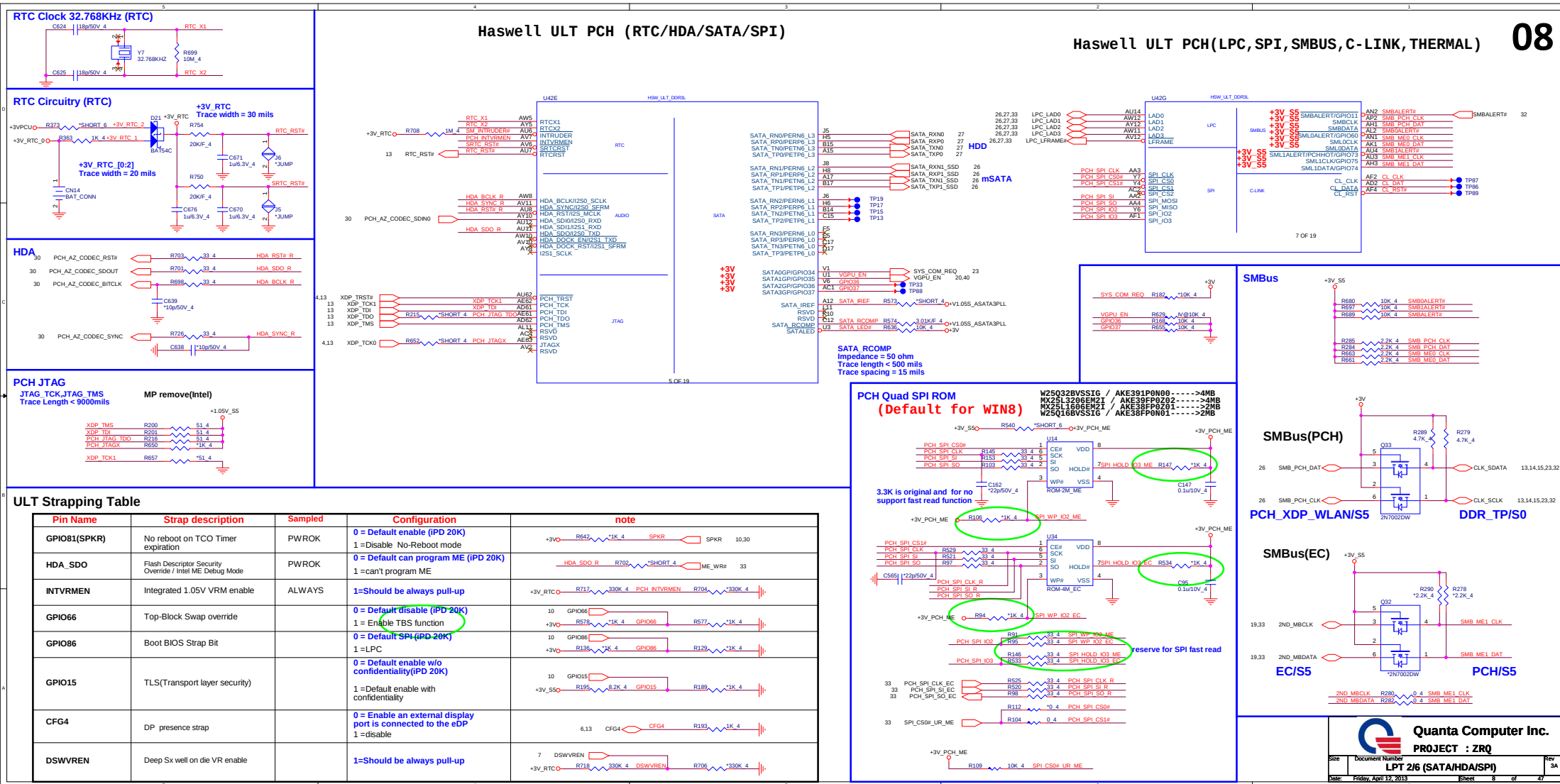


Quanta Computer Inc.
PROJECT : ZRQ

Size	Document Number	Rev
	LPT 1/6 (DMI/FDI/VGA)	3A
Date:	Friday, April 12, 2013	Sheet 7 of 47

Haswell ULT PCH(LPC, SPI, SMBUS, C-LINK, THERMAL)

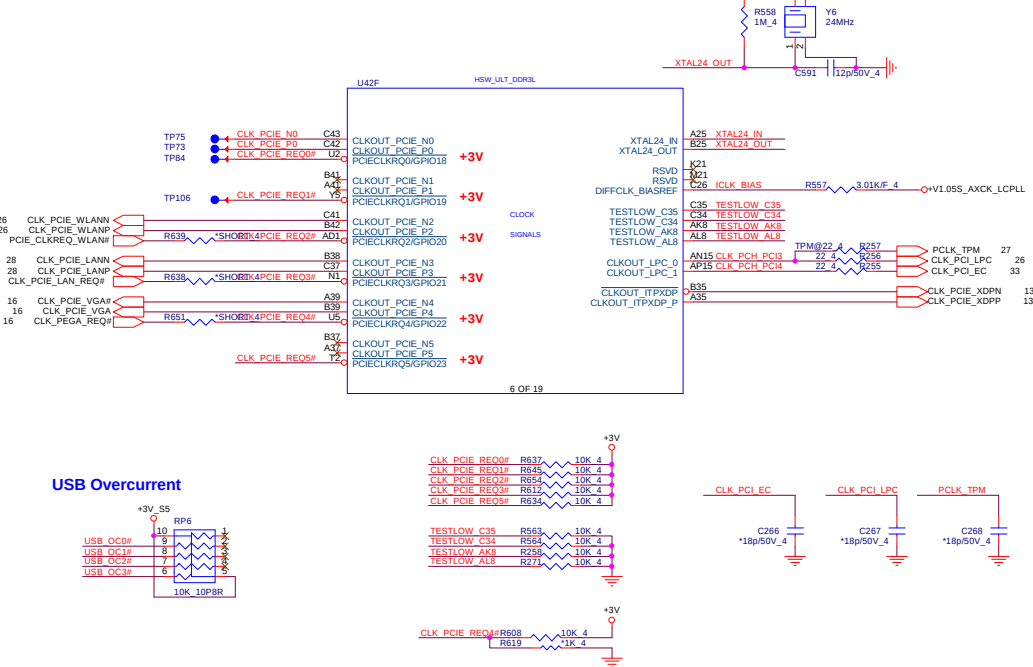
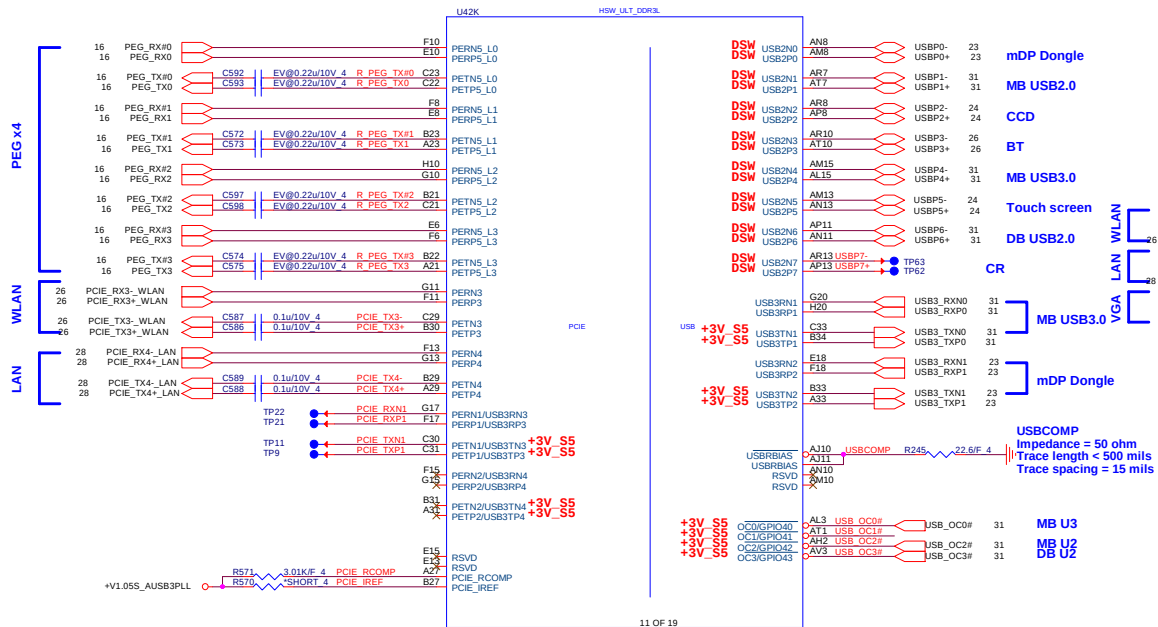
Haswell ULT PCH (RTC/HDA/SATA/SPI)



Haswell ULT PCH (PCIE,USB3.0,USB2.0)

Haswell ULT PCH (CLOCK)

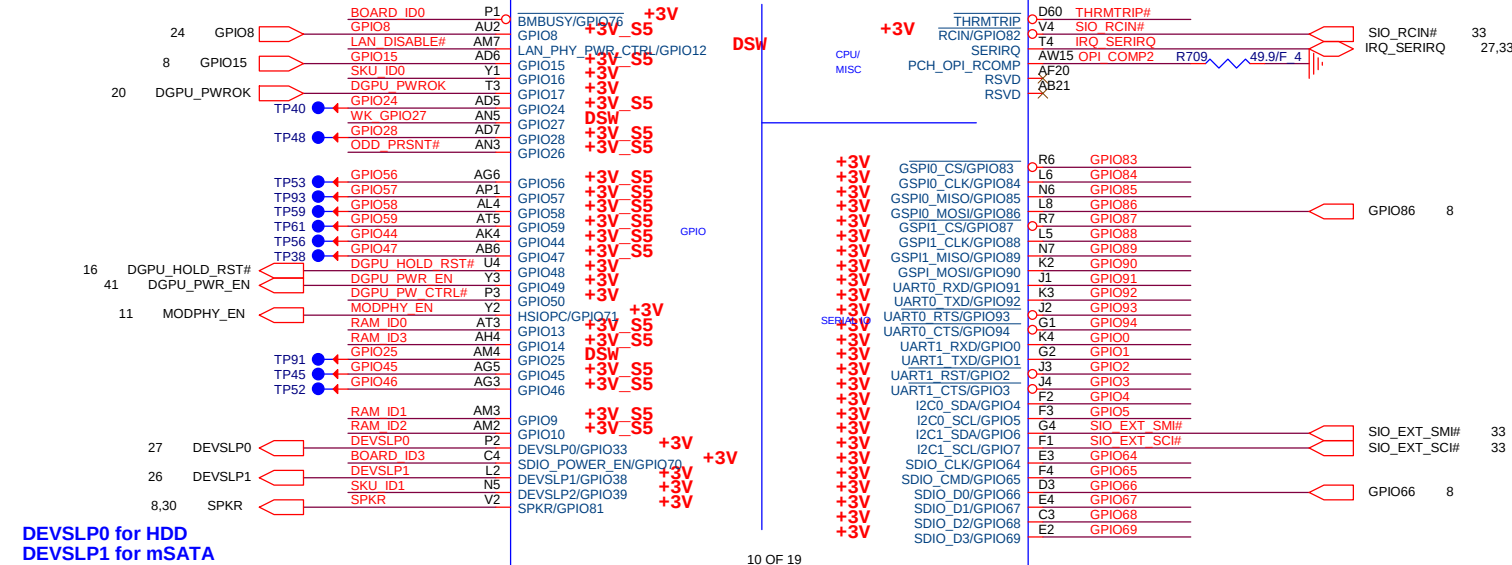
09



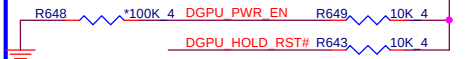
Haswell ULT PCH (GPIO,CPU/MISC,NCTF)

10

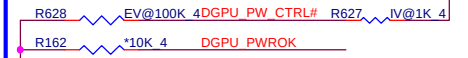
	High	Low
GPIO8	No touch panel	Touch panel



IRQ_SERIRQ	R159	10K 4
DEVSLP0	R169	*10K 4
DEVSLP1	R611	*10K 4
SIO_RCIN#	R187	*10K 4
SIO_EXT_SM#	R135	*10K 4
SIO_EXT_SCI#	R131	*10K 4
GPIO83	R206	*10K 4
GPIO84	R150	*10K 4
GPIO85	R207	*10K 4
GPIO87	R152	*10K 4
GPIO88	R208	*10K 4
GPIO89	R205	*10K 4
GPIO90	R597	*10K 4
GPIO91	R594	*10K 4
GPIO92	R209	*10K 4
GPIO93	R590	*10K 4
GPIO94	R588	*10K 4
GPIO1	R210	*10K 4
GPIO2	R595	*10K 4
GPIO3	R592	*10K 4
GPIO4	R585	*10K 4
GPIO5	R586	*10K 4
GPIO64	R584	*10K 4
GPIO65	R134	*10K 4
GPIO67	R130	*10K 4
GPIO68	R128	*10K 4
GPIO69	R581	*10K 4



high	UMA Only
low	GPU power is control by PCH GPIO (Discrete, SG or Optimize)

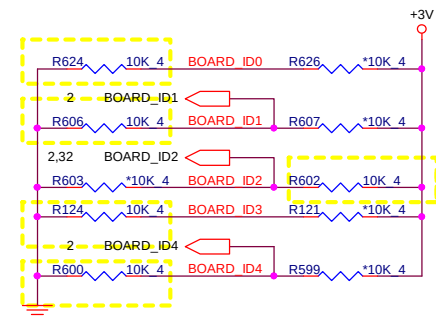


LAN_DISABLE#	R260	10K 4
ODD_PRSTNT#	R679	10K 4
GPIO8	R250	*10K 4



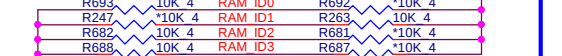
GPIO27 : If not used then use 8.2-k Ω to 10-k Ω pull-down to GND.

Board ID



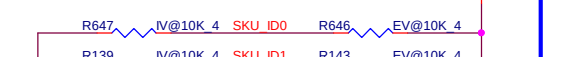
	Low	High
BOARD_ID0	DDR3	GDDR5
BOARD_ID1	Enable on board memory	Disable on board memory
BOARD_ID2	Pin8 of SYNAPTICS and ELAN are NC pin. BIOS maybe will use EEPROM detection. Default is pull high.	
BOARD_ID3	Reserved (Default)	Reserved
BOARD_ID4	Reserved (Default)	Reserved

RAM ID



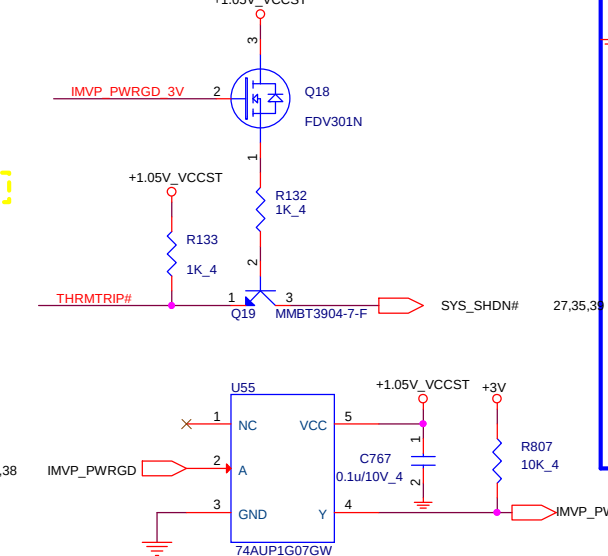
Vender	RAM_ID	Q PN	Mfr. PN	Freq.
Hynix	0000	AKD5J6ETW04	H5TC4G63AFR-PRBA	1600MHZ
Elpida	0001	AKD5J6ST400	EDJ4216EBB6-DJ-F	1333MHZ
Elpida	0010	AKD5J6ST404	EDJ4216EFB6-GN-F	1600MHZ

SKU ID



	SKU_ID1	SKU_ID0	VGA H/W Signal	Setup Menu	
UMA Only	0	0	UMA	Hidden	UMA boot
dGPU Only	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	1	0	UMA+GPU	dGPU/SG	UMA boot
Optimize (Muxless)	1	1	UMA	UMA/SG	UMA boot

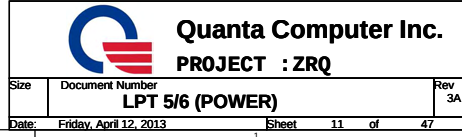
CPU thermal trip



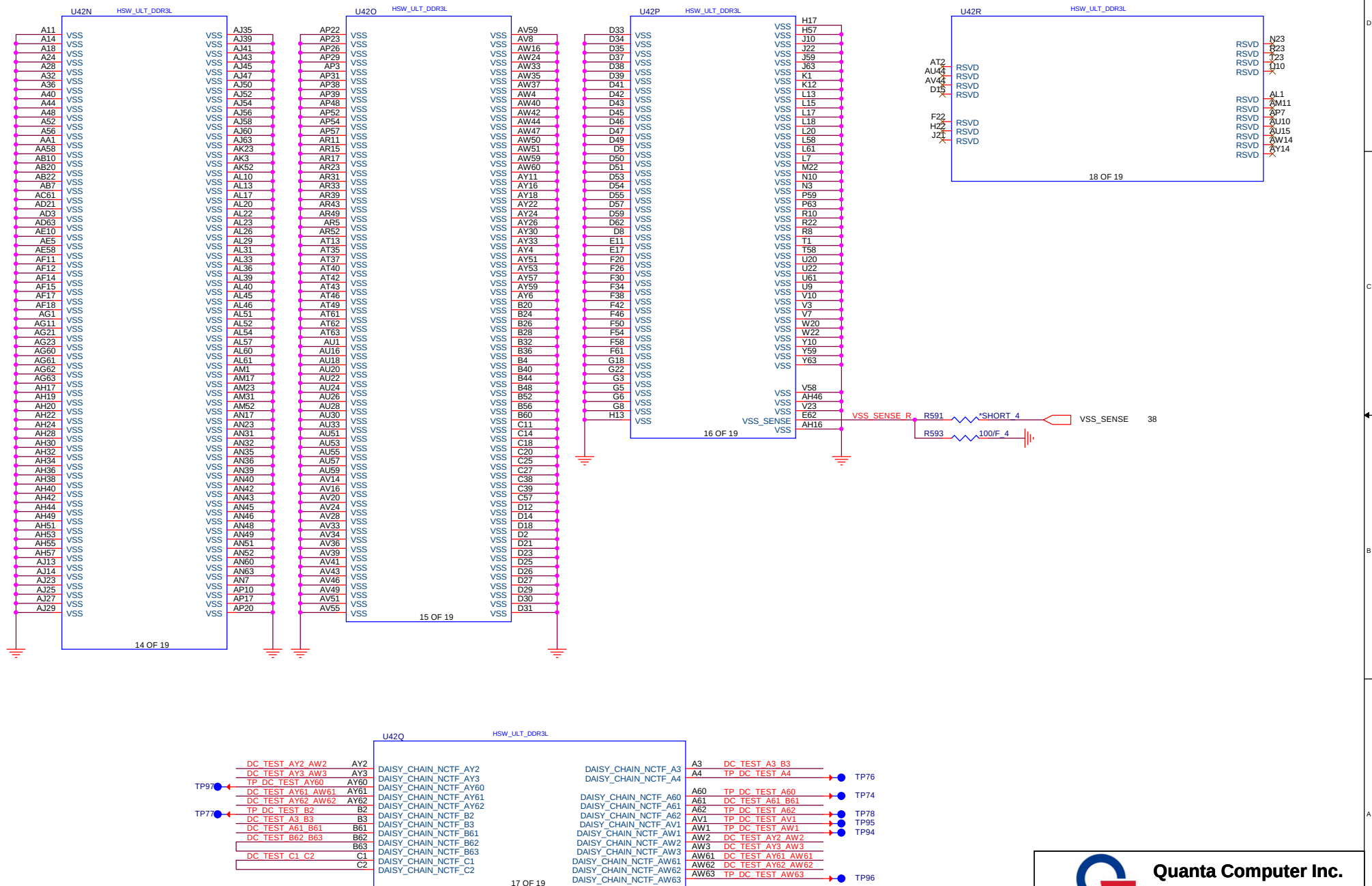
Quanta Computer Inc.
PROJECT : ZRQ

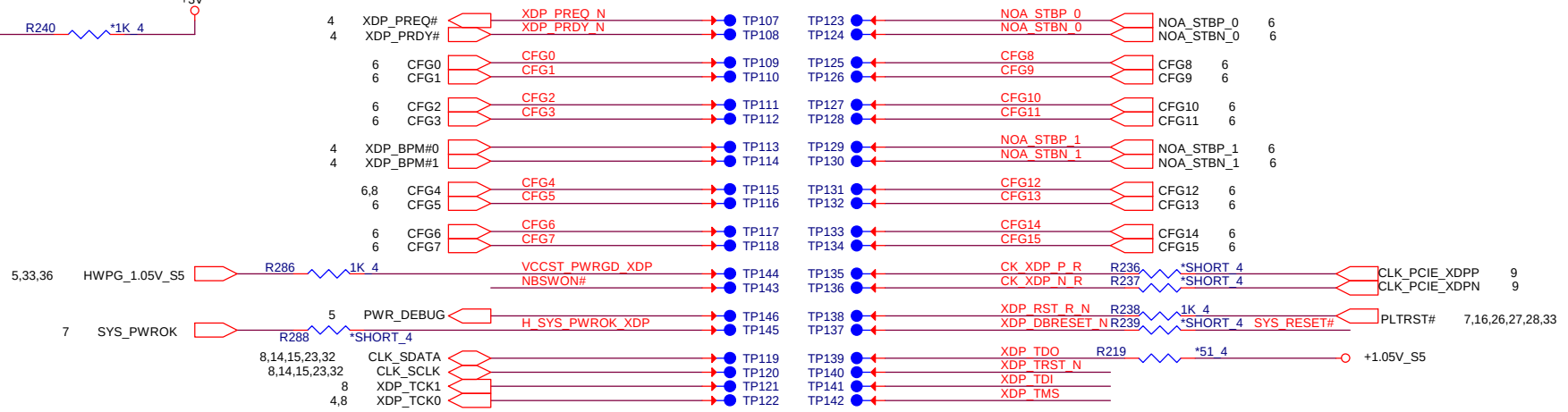
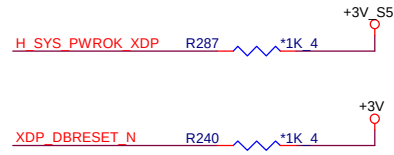
[illegible]

PCH HDA Power

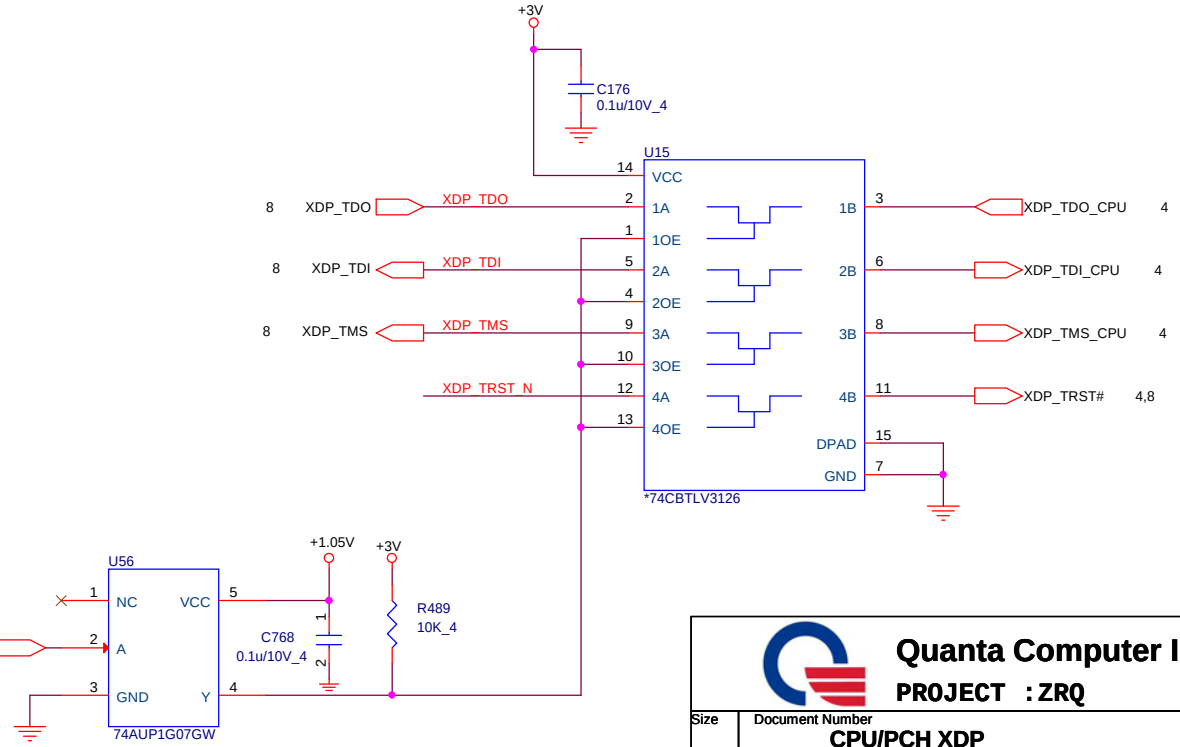
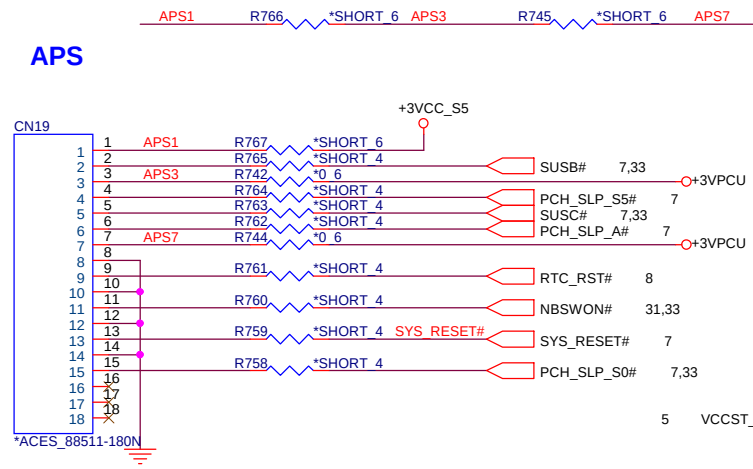


Haswell ULT (GND)





APS





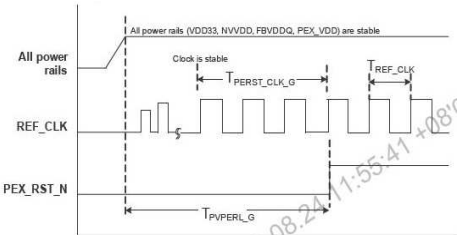
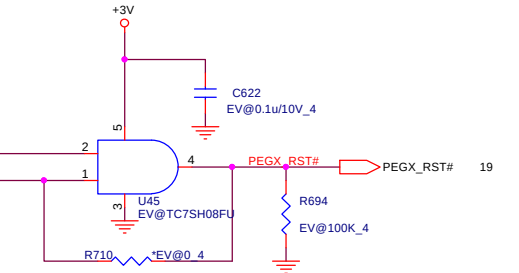
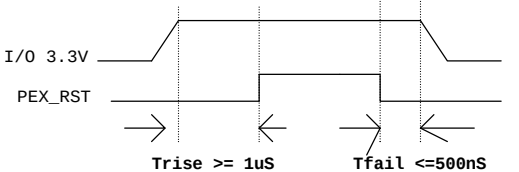


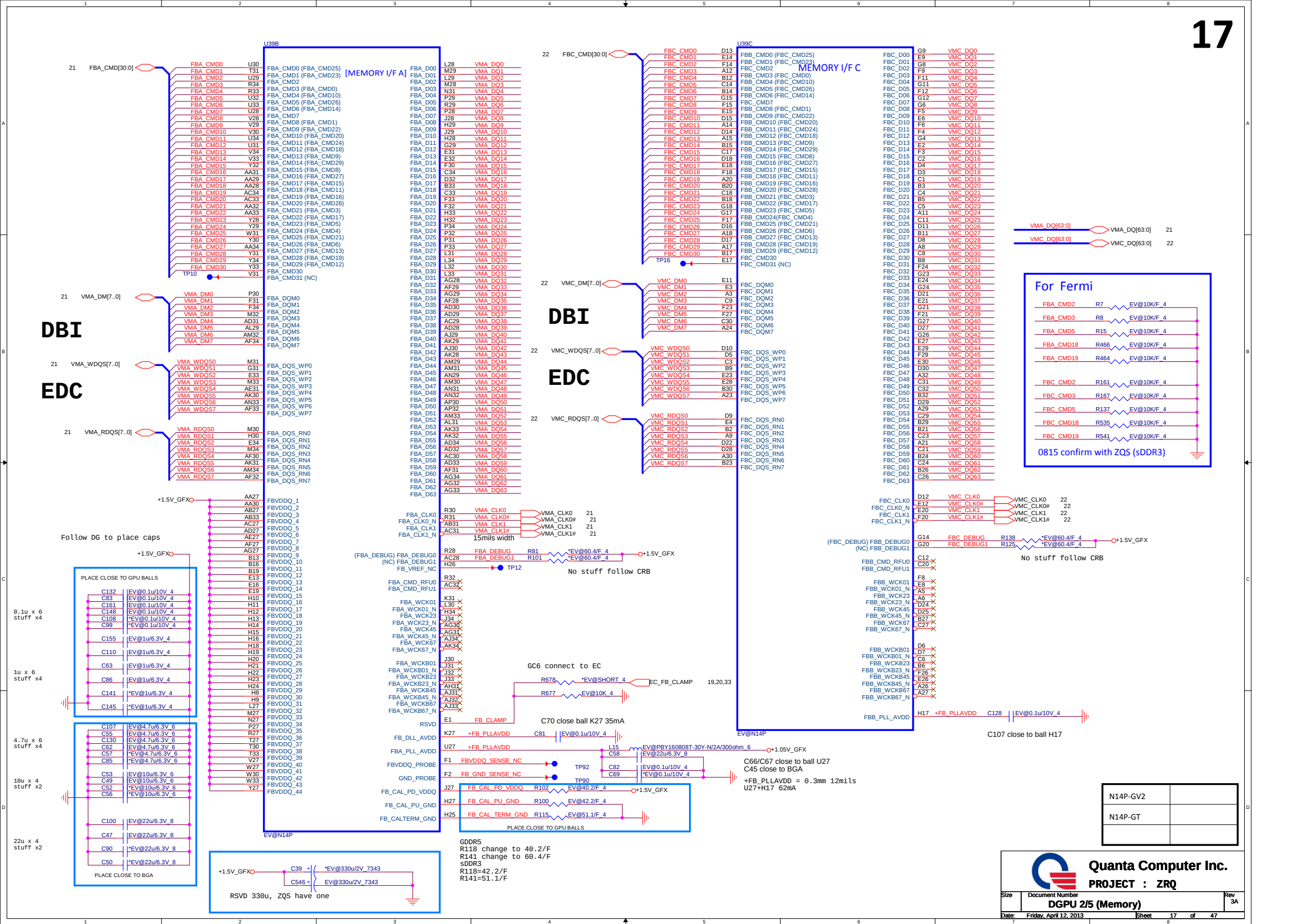
Table 3-8. N11x Reset Requirements for PCI Express 2.0

Constraint Parameter	Requirement	Notes
T_{FVPERL_G}	$T_{FVPERL_G} \geq 100$	
$T_{PERST_CLK_G}$	$T_{PERST_CLK_G} \geq 1T_{REF_CLK}$	

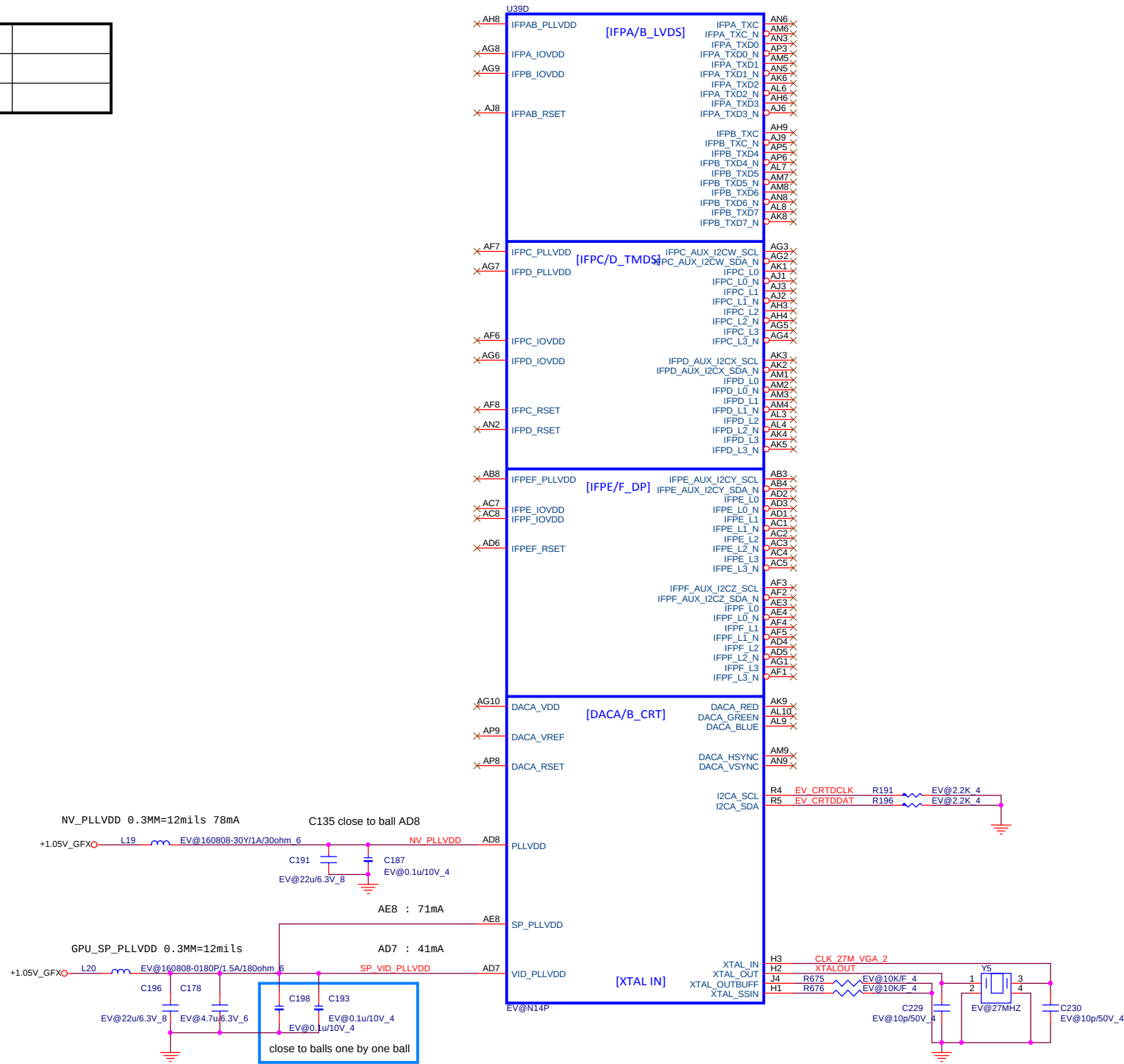


PEX_RST timing





N14P-GV2	
N14P-GT	



N14P-GV2	
N14P-GT	

Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

STRAP3
Optimus ---> 4.99K PD
Discrete only ---> 15K PD

Resistor P/N
4.99K ---> CS24992FB26
10K ---> CS31002FB26
15K ---> CS31502FB24
20K ---> CS32002FB29
24.9K ---> CS32492FB16
30.1K ---> CS33012FB18
34.8K ---> CS33482FB22
45.3K ---> CS34532FB18

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	FB 1	FB 0	SMB_ALT_ADDR	VGA_DEVICE	1000
ROM_SCLK	PCI_DEVICE[4]	SUB_VENDOR	PCI_DEVICE[5]	PEX_PL_LN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0000
STRAP2	PCI_DEVICE[3]	PCI_DEVICE[2]	PCI_DEVICE[1]	PCI_DEVICE[0]	0100
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33	0111

	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N14P_GV	L 10K	H 4.99K	H 4.99K	H 45.3K	L 45.3K	L 15K	L 4.99K	L 45.3K
N14P_GE	L 10K	L 10K	L 10K	H 10K	H 10K	L 10K	L 10K	L 10K
N14P_GT	L 10K	H 4.99K	L 15K	H 45.3K	L 4.99K	L 24.9K	L 4.99K	L 45.3K

A.ROM_SI - MEMORY STRAP
B.ROM_SO - 5K pull high

D.STRAP 0 - 45k pull high
E.STRAP 1 - 5K pull down
F.STRAP 3 - 5k pull down

C1.For N14P-GT sku
N14P-GT device ID=0x0FE4
1.ROM_SCLK = 15K pull down
2.STRAP2 = 25K pull down
3.STRAP4 = 45K pull down

C.For N14P-GV2 sku
N14P-GV2 QS device ID=0x1292
1.ROM_SCLK = 5K pull high
2.STRAP2 = 15k pull down
3.STRAP4 = 45 pull down
//For N14P-GV2 QS

N14P-GV2 ES device ID=0x12AD
1.ROM_SCLK = 15K pull down
2.STRAP2 = 30k pull high
3.STRAP4 = 10K pull down
//For N14P-GV2 ES

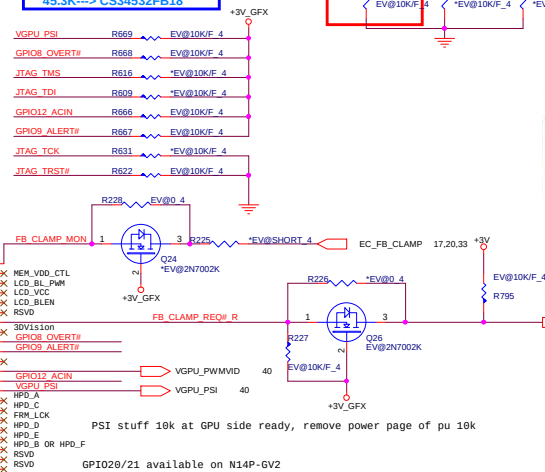
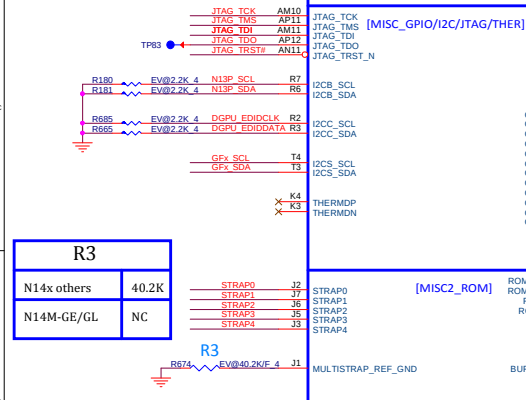
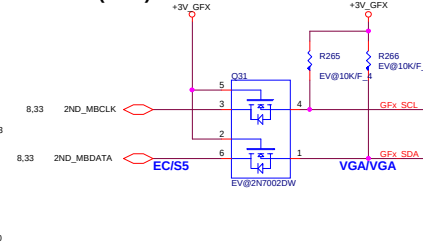


Table 9. N14P-GV/GT/G5/LP/GE GDDR5 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed WCK (MHz)	Memory Date Code Minimum	Status
128Mx16 GDDR5	Hynix	0x4	1.5 V/ 1.5 V	H5GQ2H24AFR-T2C	2500	N/A	Production Candidate
		0x6	1.35V/ 1.35V	H5GQ2H24AFR-T2C	2000	N/A	Production Candidate
	Samsung	0x5	1.5 V/ 1.5 V	K4G020325FD-FC04	2500	1219	Production Candidate
		0x7	1.35V/ 1.35V	K4G020325FD-FC04	2000	1219	Production Candidate

Vendor	P/N	Mfr. P/N	ROM_SI
Hynix	AKG5MUTW13	H5GQ2H24AFR-T2C	0100
Samsung		K4G020325FD-FC04	0101

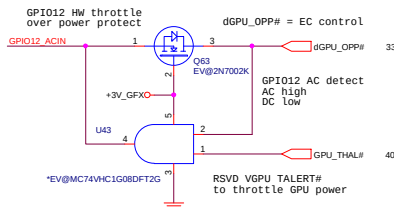
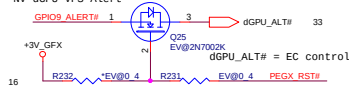
SMBus(VGA)



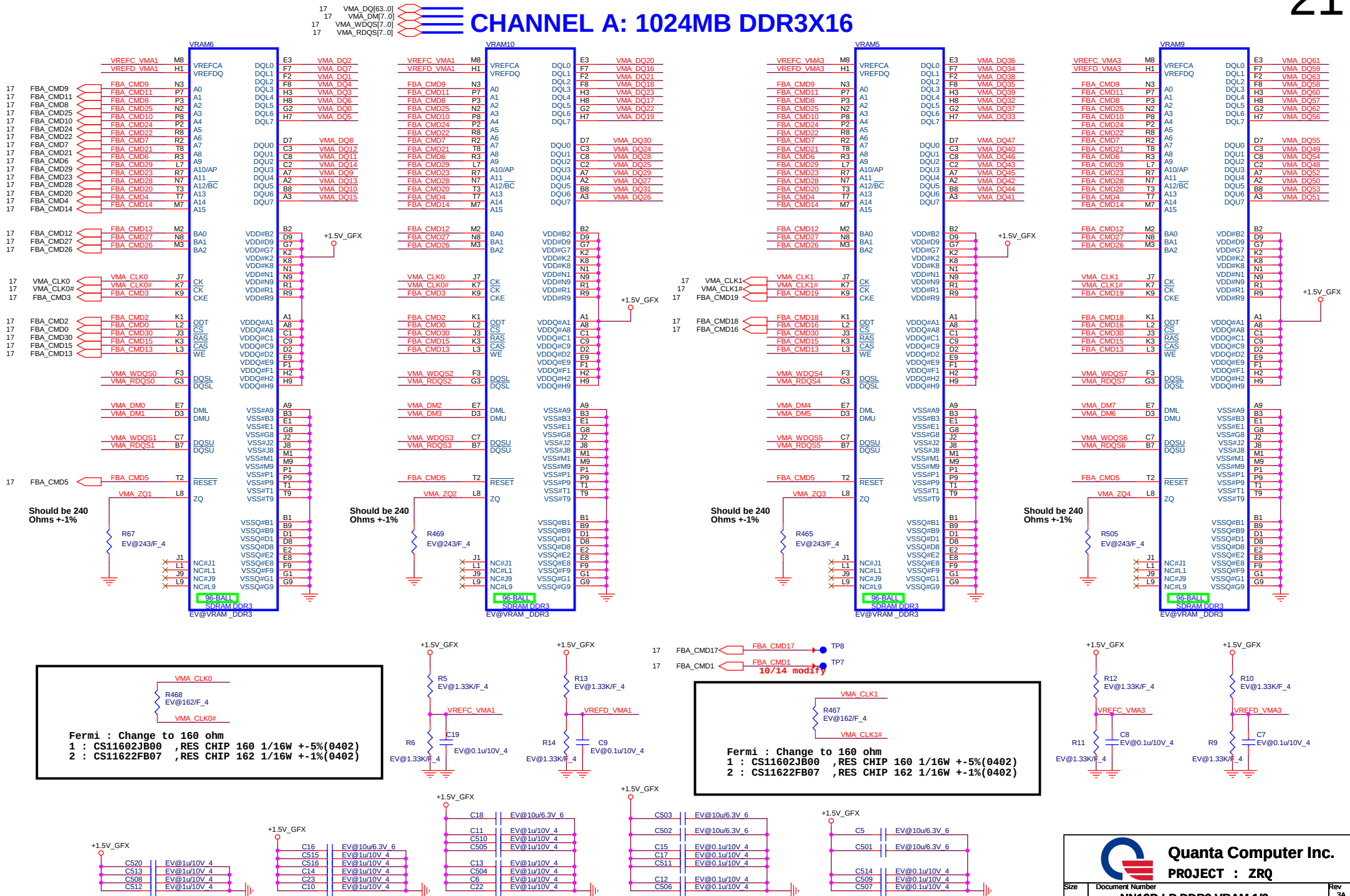
GPI08 VGA throttle# -> inform EC
over temperature protect

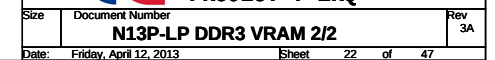


GPI09 for ADPS circuit to inform EC
NV dGPU VPS Alert

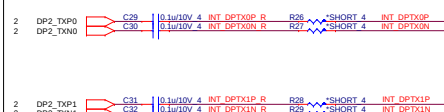


CHANNEL A: 1024MB DDR3X16

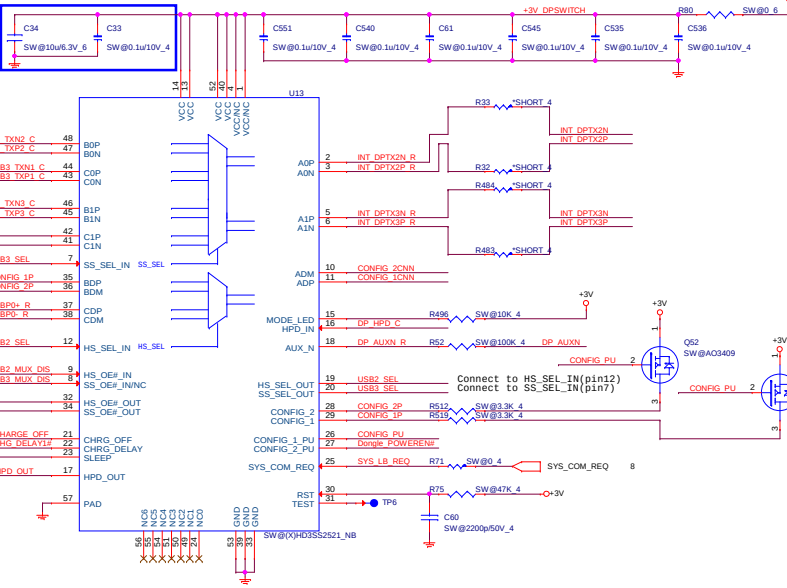




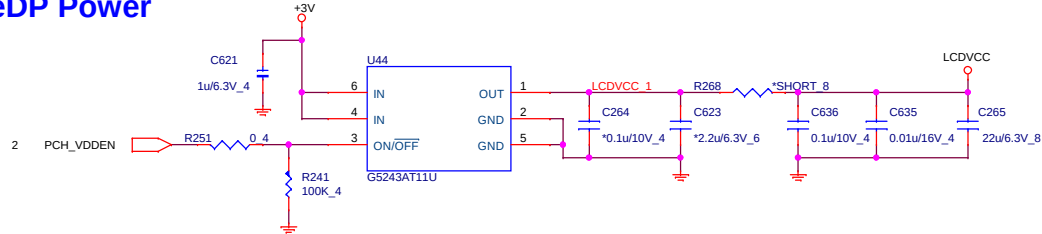
Mini DP ML (DPP)



Layout Notes:
Place near Pin13 and Pin14



eDP Power



eDP

MP confirm 2 or 4 Lane

eDP

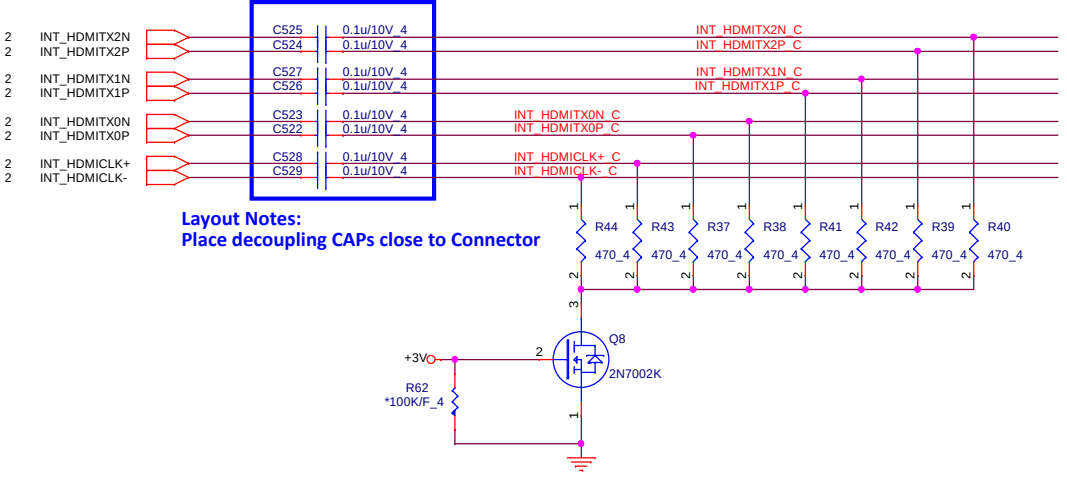
CCD

Touch Panel

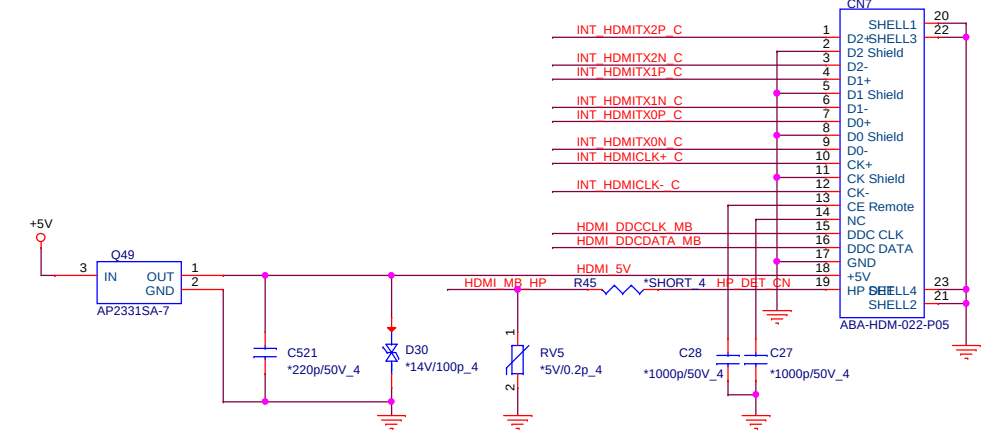
Touch Panel interrupt



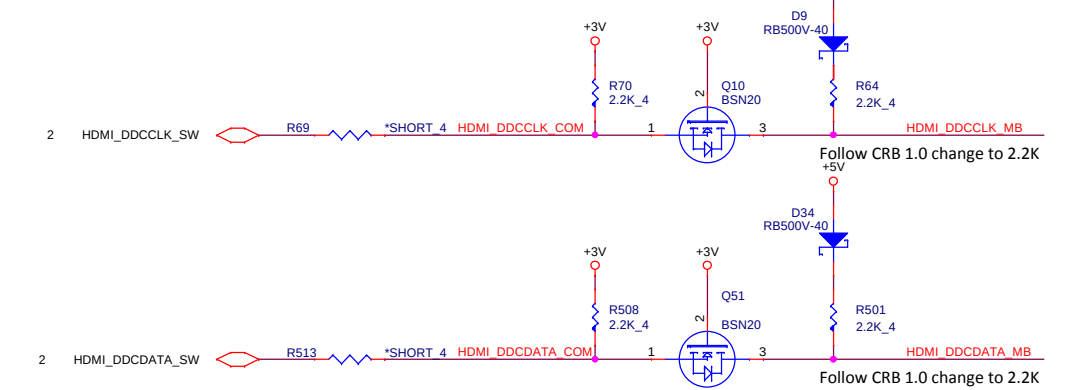
HDMI Cost Reduced level shift (HDM)



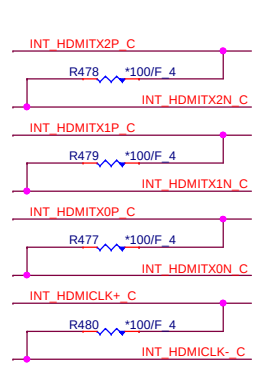
HDMI connector (HDM)



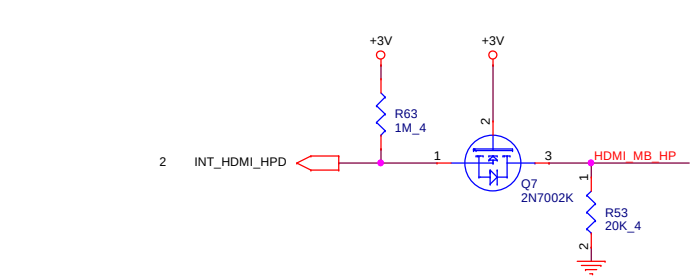
HDMI DDC (HDM)



EMI (EMC)



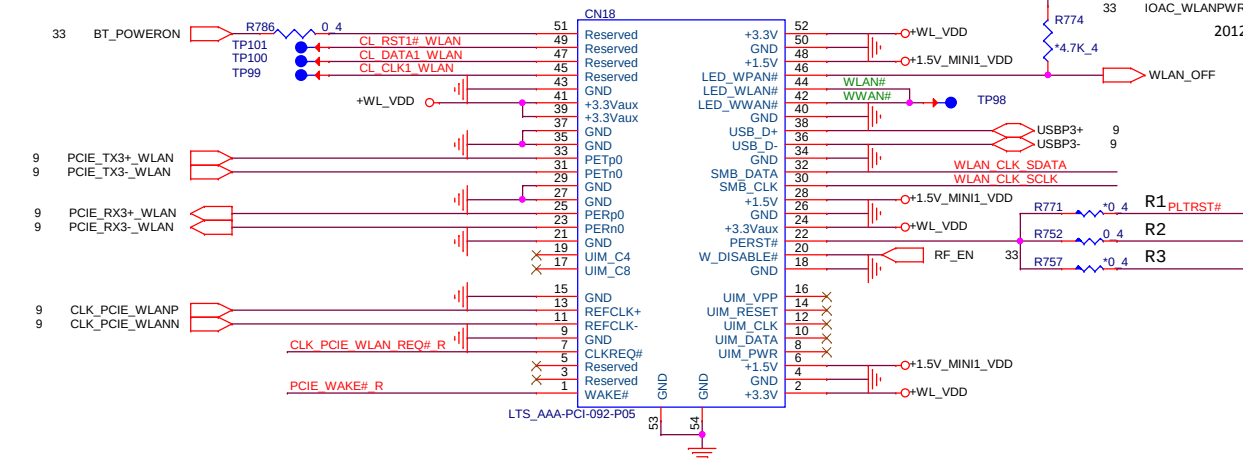
HDMI-detect (HDM)



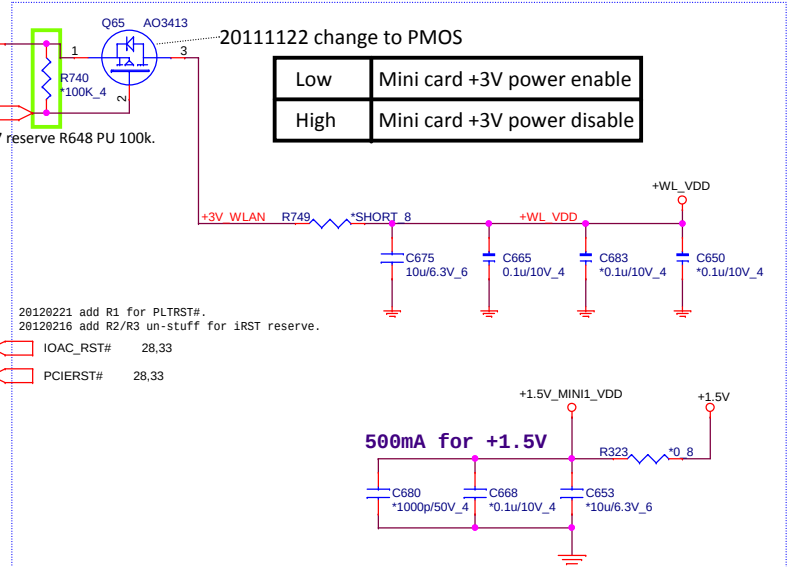
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux: 330mA
+1.5V: 500mA

Check LED signal. (active high or low)
H=5.2mm



2011017 : stuff Q81 to enable wake function on WLAN for IOAC
check IOAC power rail can reduce Q81

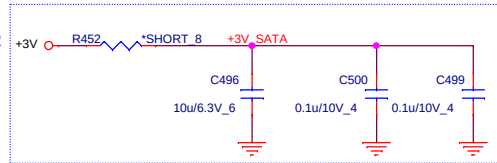


LAYOUT NOTE:
CLOSE TO CONNECTOR

mSATA(MNC)

LAYOUT NOTE:
CLOSE TO CONNECTOR

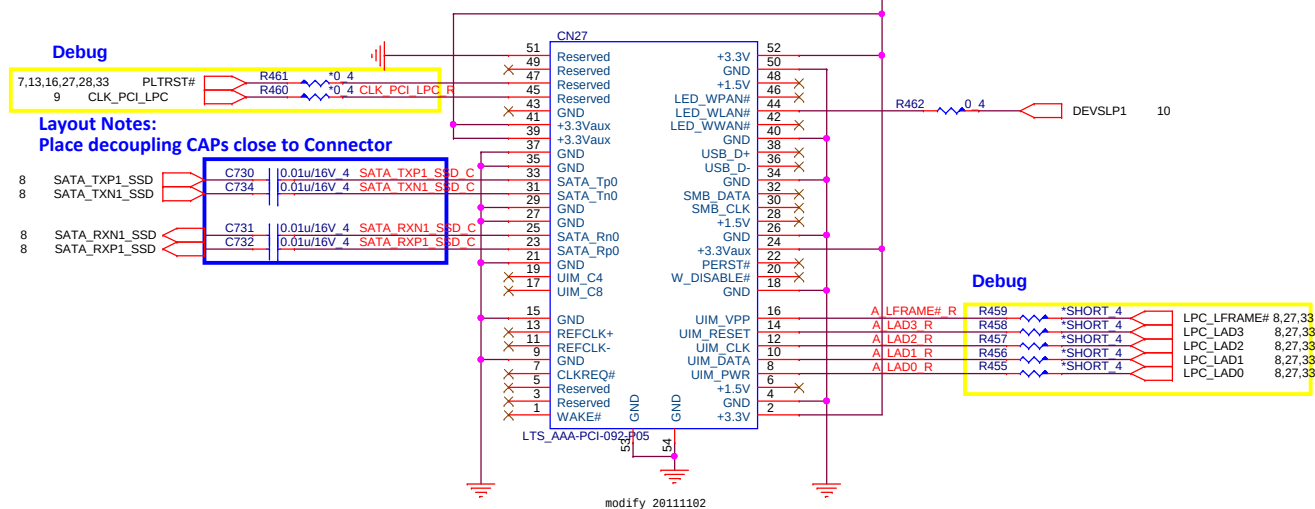
rating = 1000mA @ 128G



H=4.95mm

Debug

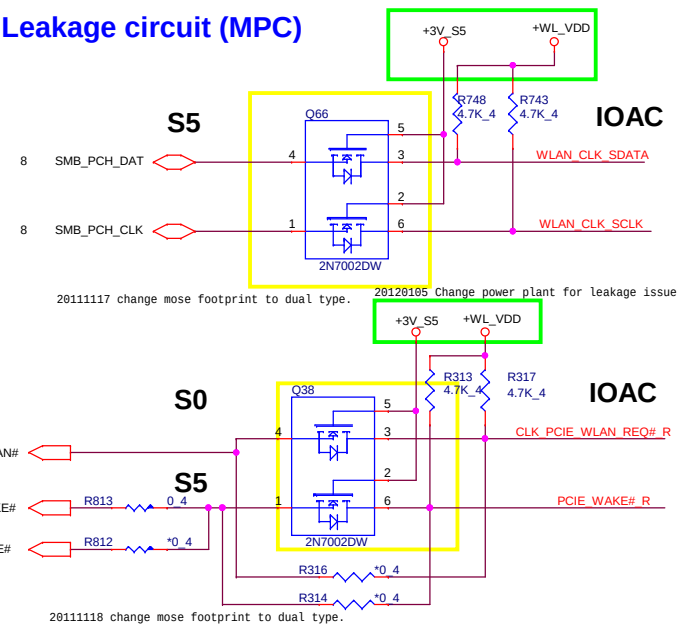
Layout Notes:
Place decoupling CAPs close to Connector



modify 20111102

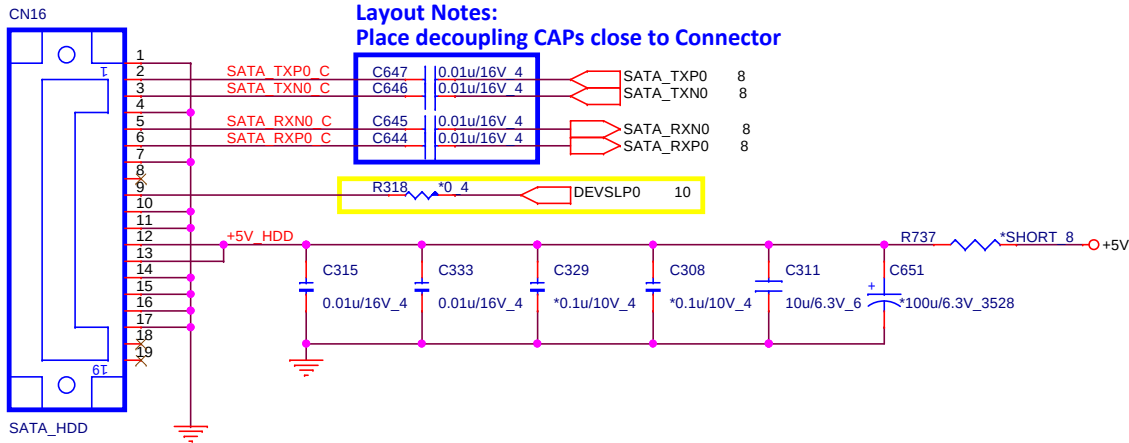
Leakage circuit (MPC)

20120185 change power plant for Leakage issue.



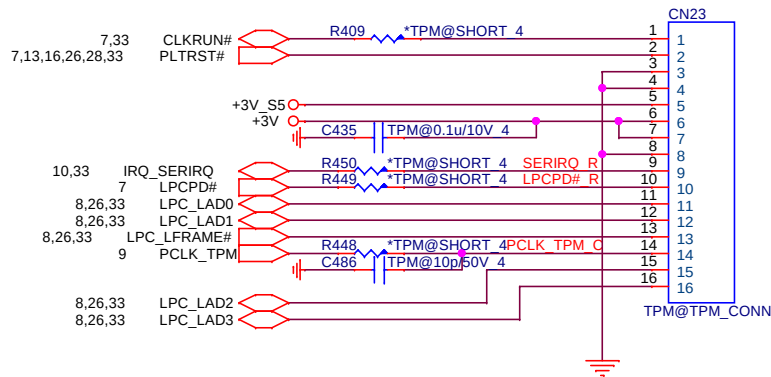
20111118 change mose footprint to dual type.

MAIN SATA HDD (HDD)

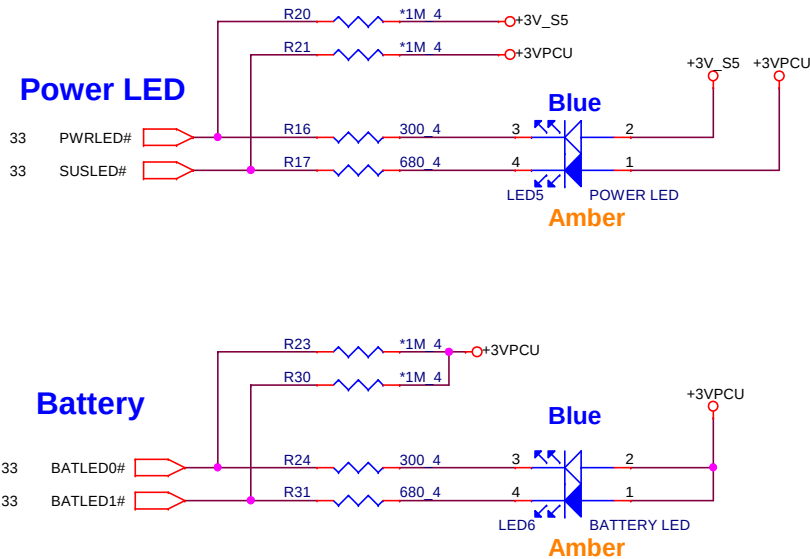


TPM (TPM)

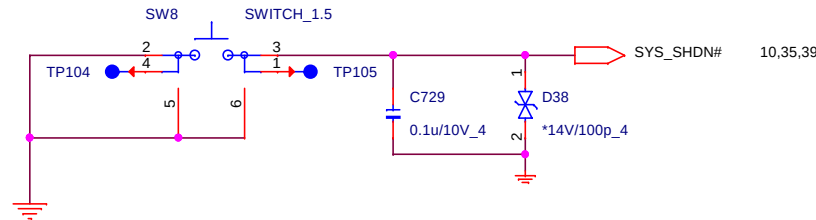
27



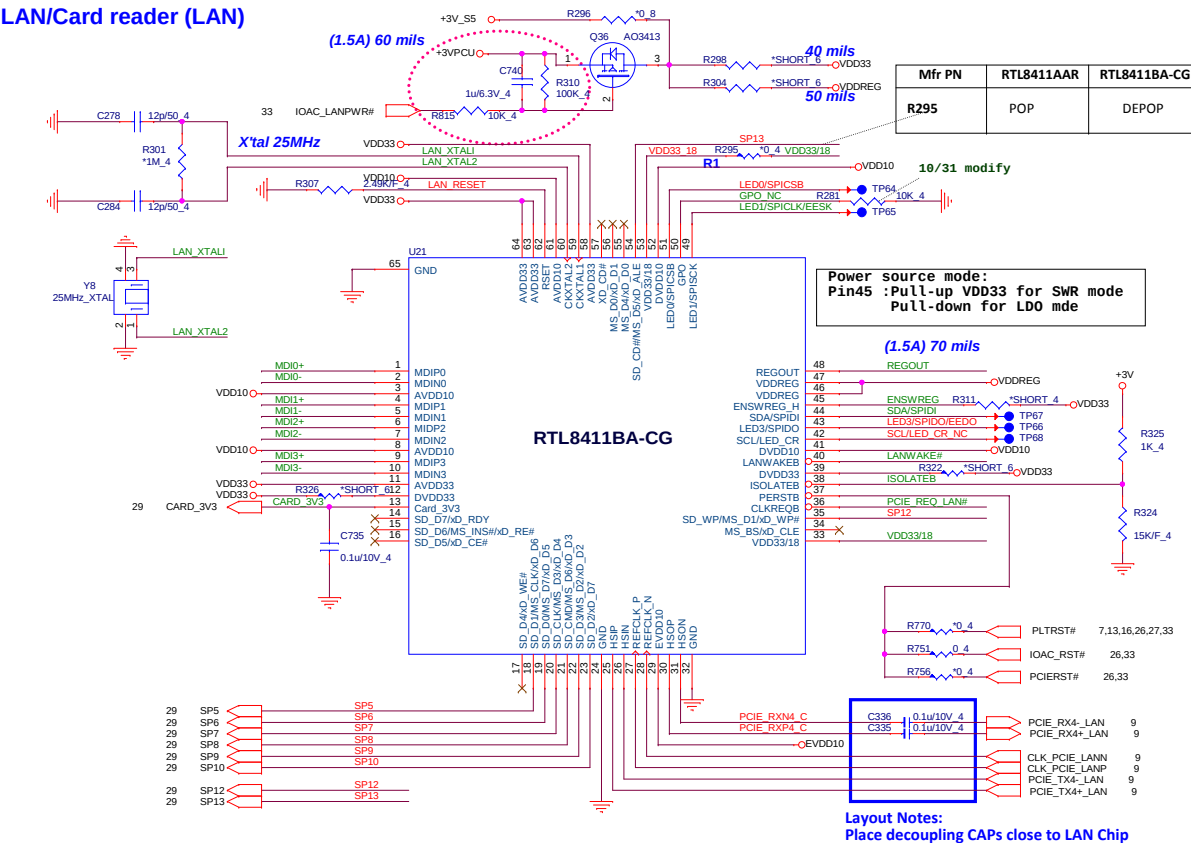
LED(UIF)



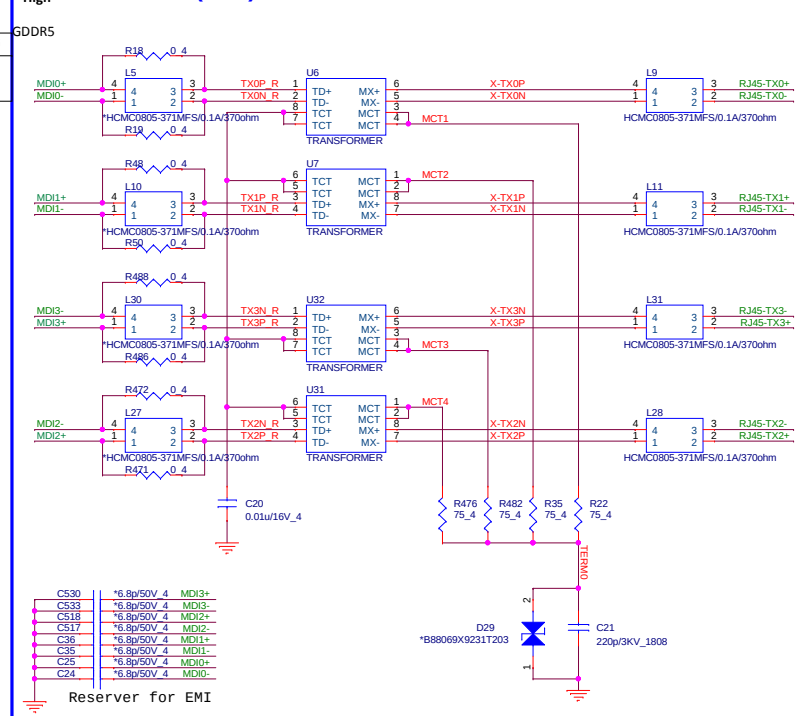
3/5VPCU reset switch (CLG)



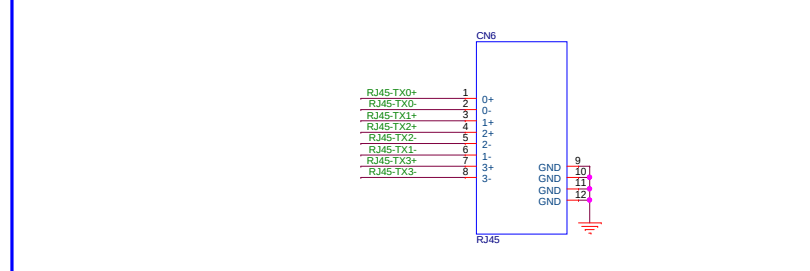
LAN/Card reader (LAN)



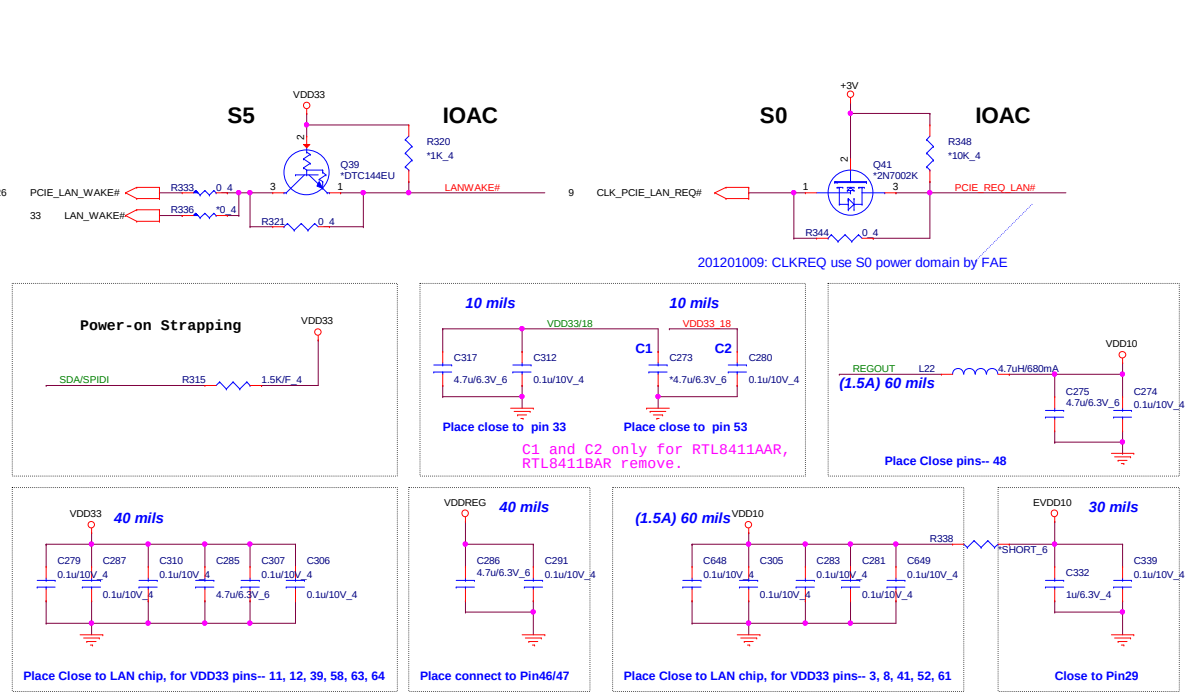
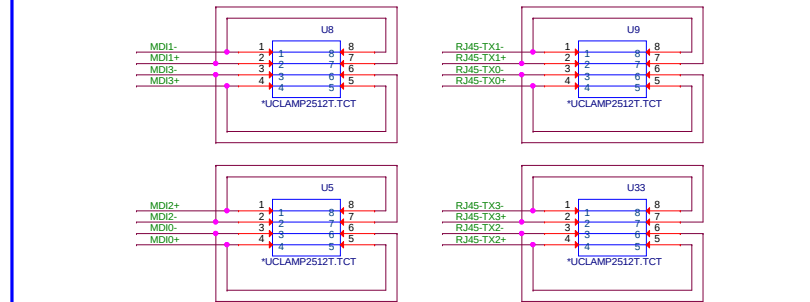
High Transformer (LAN)



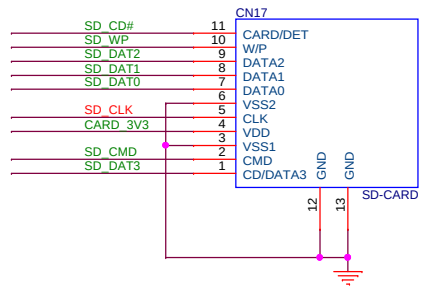
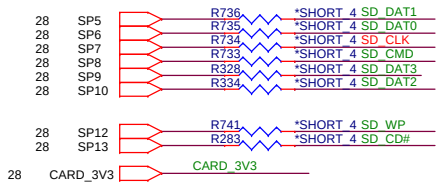
RJ45 CONNECTOR (LAN)



SURGE (LAN)



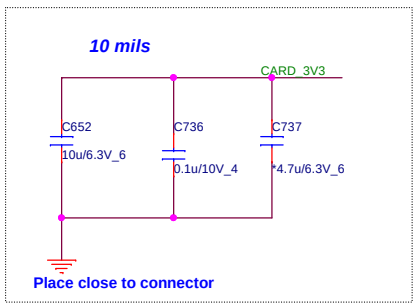
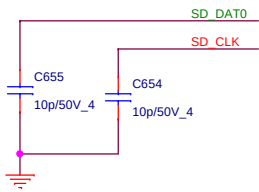
SD/MMC CARD READER CONNECTOR (MMC)



EMI

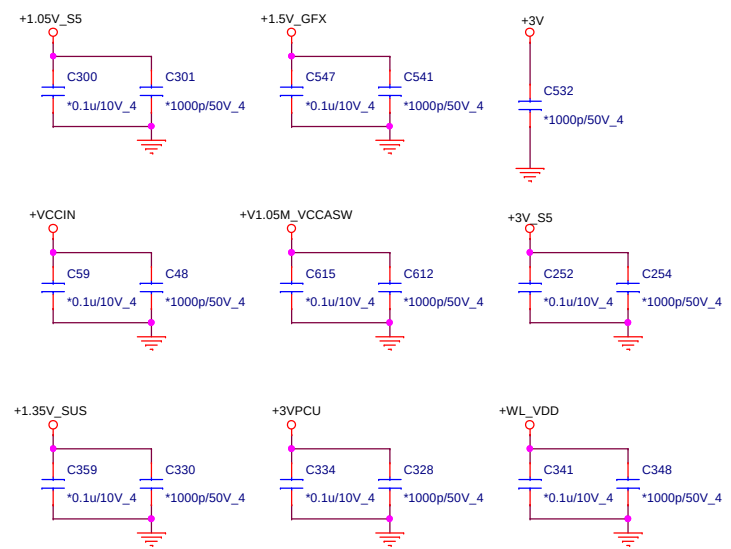
Share Pin

SP1	SD D7	xD RDY
SP2	SD D6	MS INS#
SP3	SD D5	xD CE#
SP4	SD D4	xD WE#
SP5	SD D1	MS CLK
SP6	SD D0	xD D5
SP7	SD CLK	MS D3
SP8	SD CMD	MS D6
SP9	SD D3	MS D2
SP10	SD D2	xD D7
SP11	MS BS	xD CLE
SP12	SD WP	MS D1
SP13	SD CD#	MS D5
SP14	MS D4	xD D9
SP15	MS D0	xD D1
SP16		xD CD#

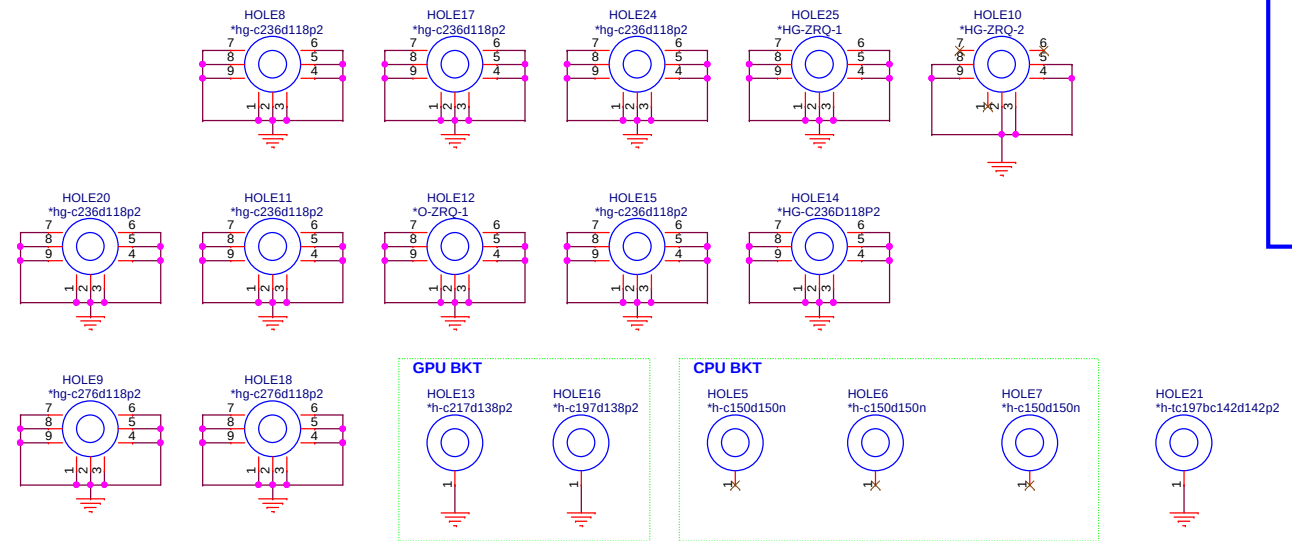


Stitching cap (EMC)

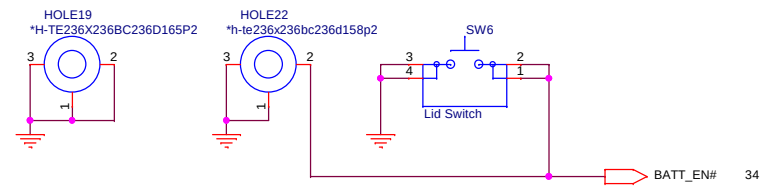
29



HOLE(OTH)



BATT Enable short pad



PAD5
*spad-e858x1268

Quanta Computer Inc.
PROJECT : ZRQ

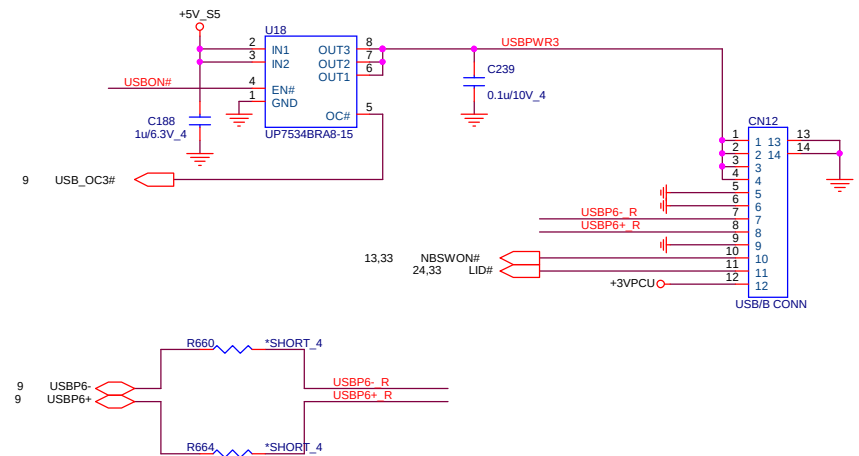
Size	Document Number	Rev
	CARD READER CONNECTOR	3A

Date: Friday, April 12, 2013 Sheet 29 of 47

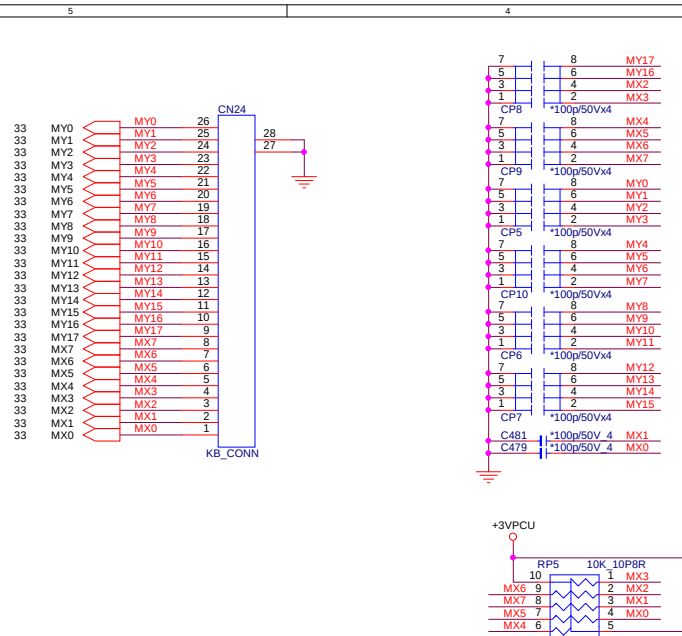
Active High:
1st: AL007534001 (Promate)
2nd: AL000547006 (GMT)
3rd: AL002511002 (DDS)



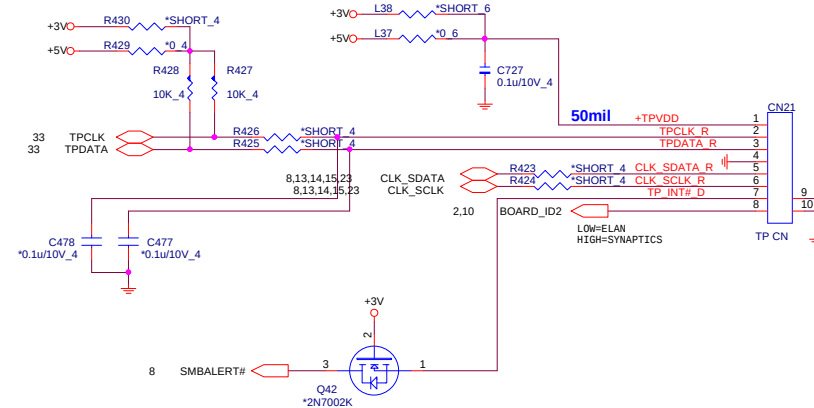
CB	SELCDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	SD charging with SDP only
1	1	SD charging with CDP or SDP only (depending on external device)



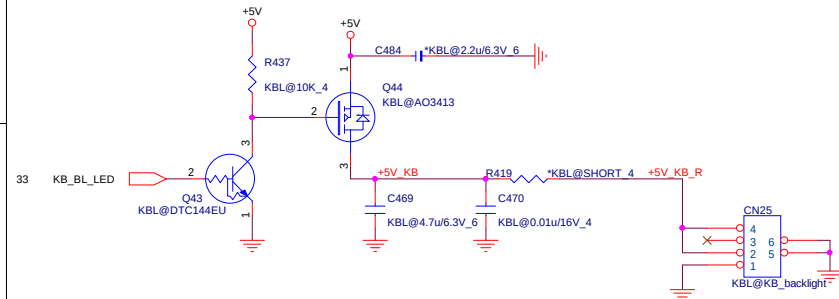
K/B (KBC)



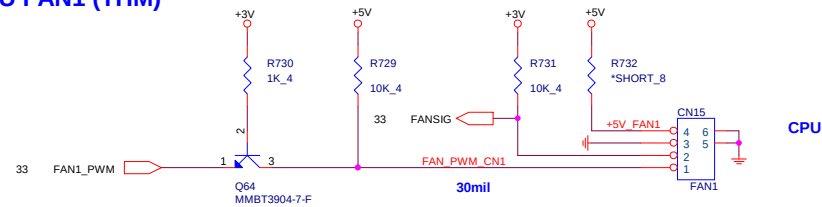
TOUCHPAD BOARD CONN (TPD)



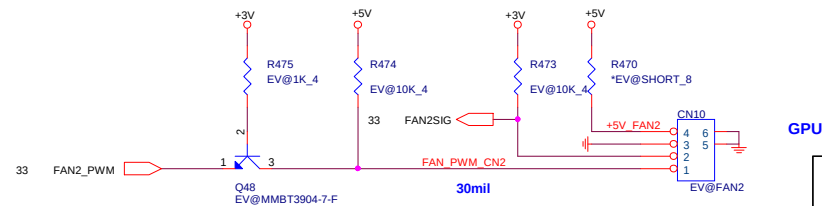
KB_BL LED (KBC)



CPU FAN1 (THM)

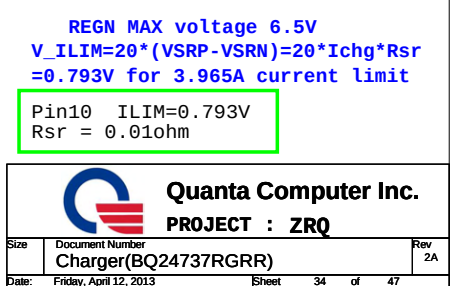


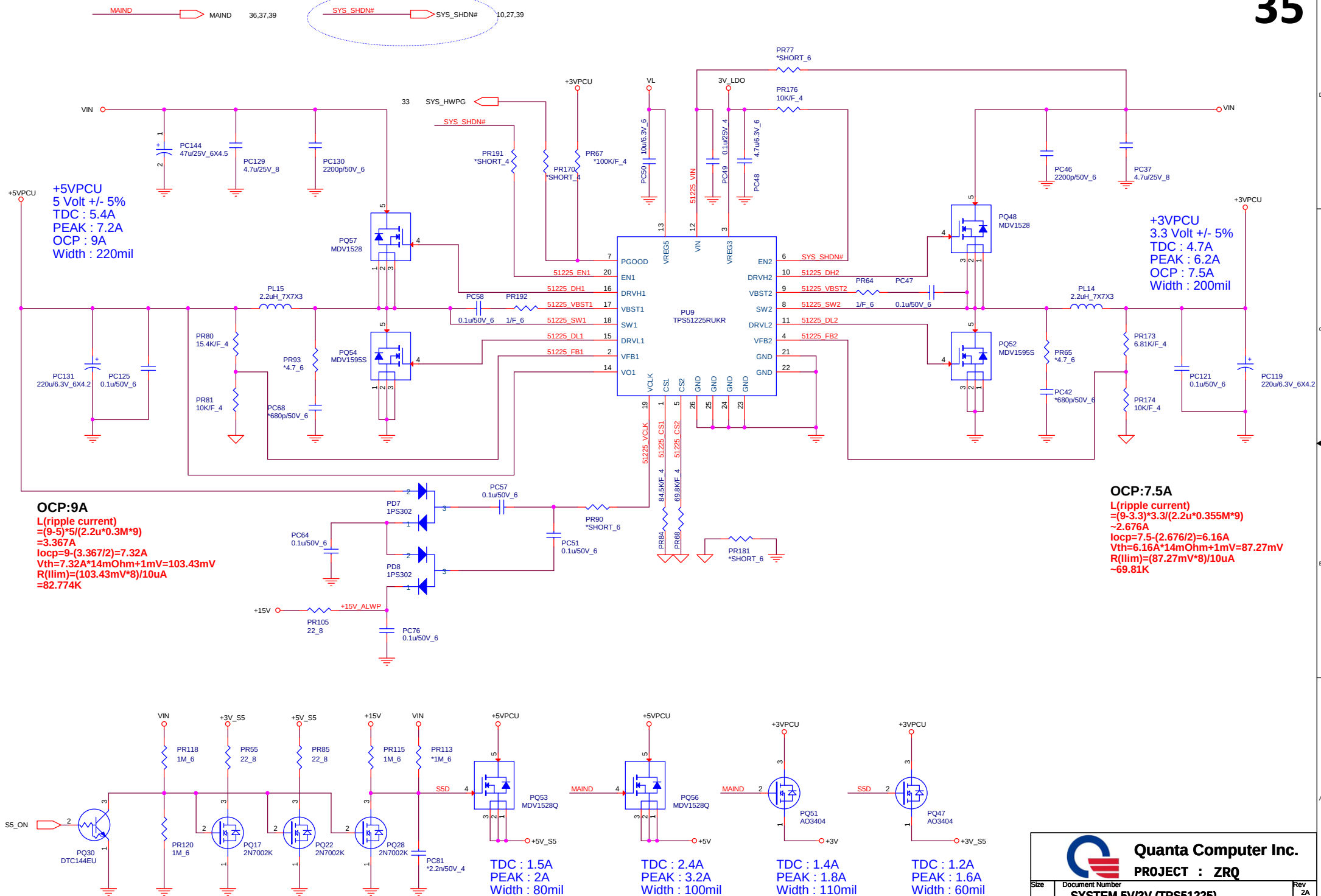
CPU FAN2 (THM)



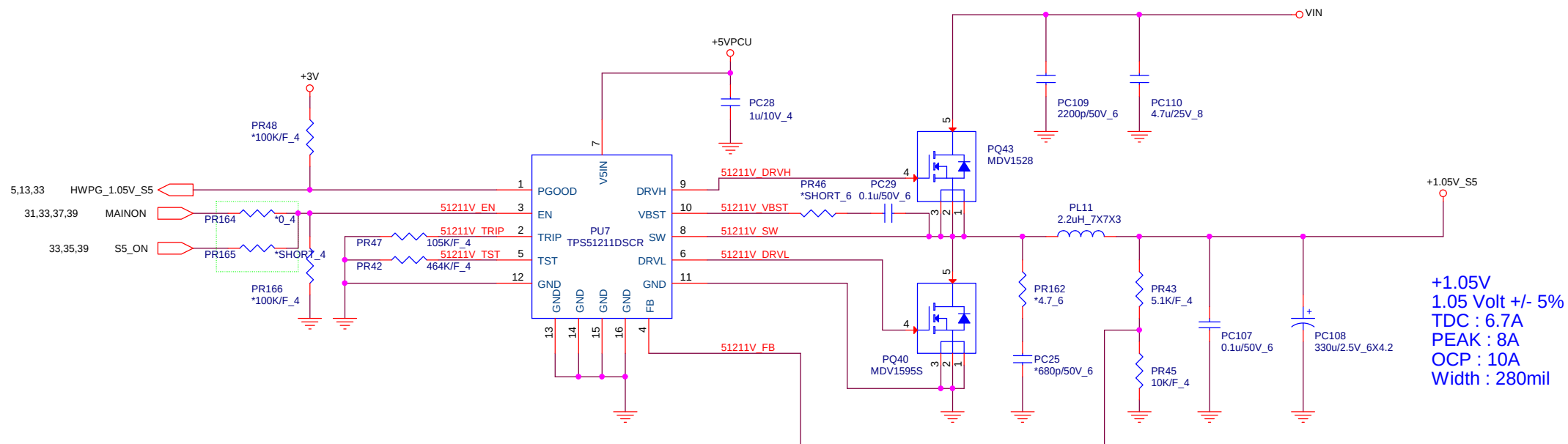
Quanta Computer Inc.
PROJECT : ZRQ

Size	Document Number	Rev
	KB/TP/FAN	3A
Date:	Friday, April 12, 2013	Sheet 32 of 47

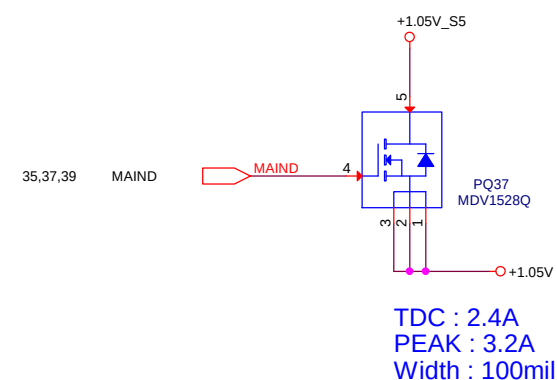




Quanta Computer Inc.
PROJECT : ZRQ



OCP=10A
 L ripple current
 $= (19-1.05) \cdot 1.05 / (2.2 \mu \cdot 290k \cdot 19)$
 $= 1.555A$
 $V_{trip} = 10 - (1.555/2) \cdot 14m\Omega$
 $= 0.129V$
 $R_{limit} = 0.129 / 10\mu A \cdot 8 = 103.293K\Omega$

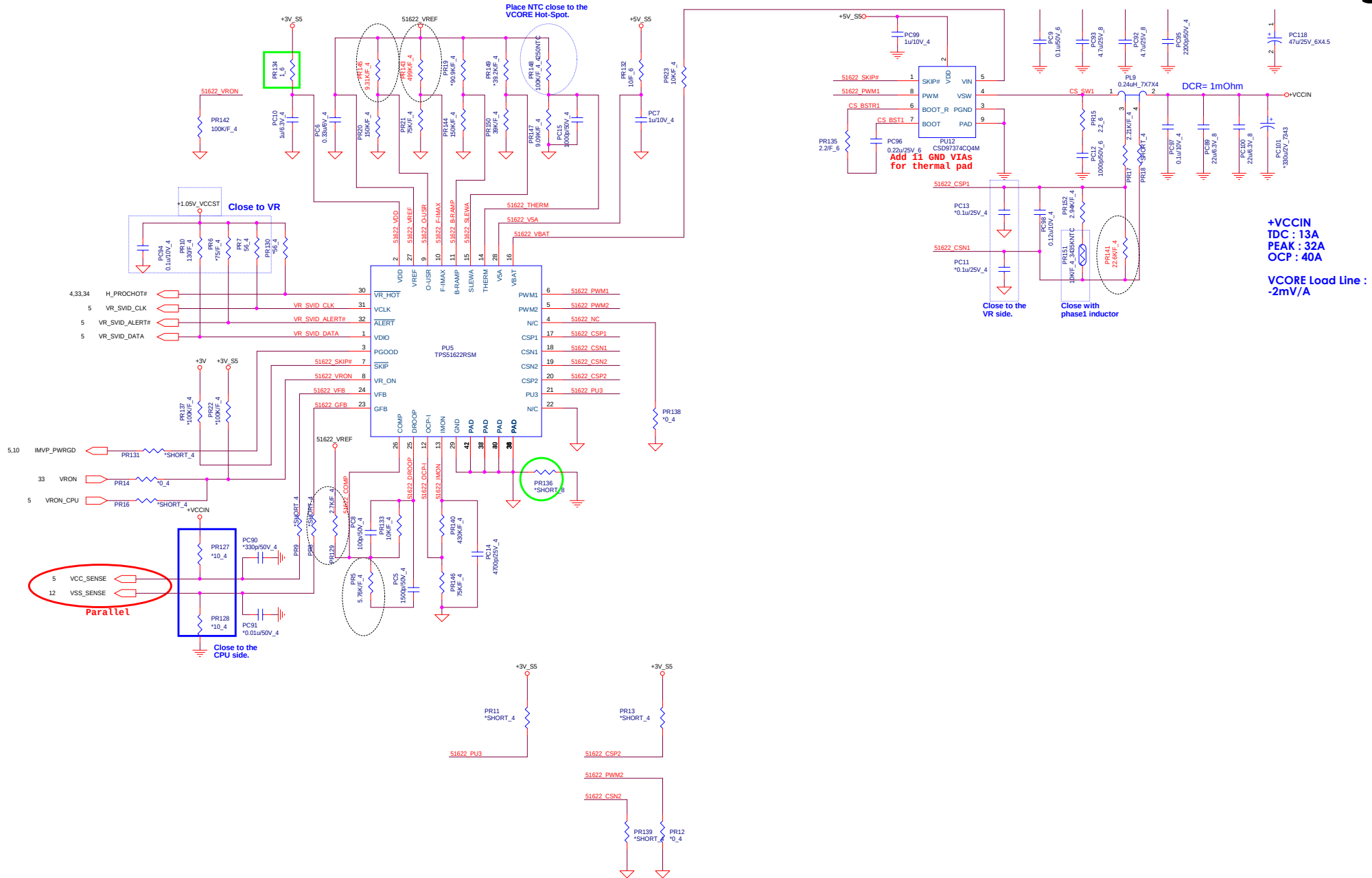


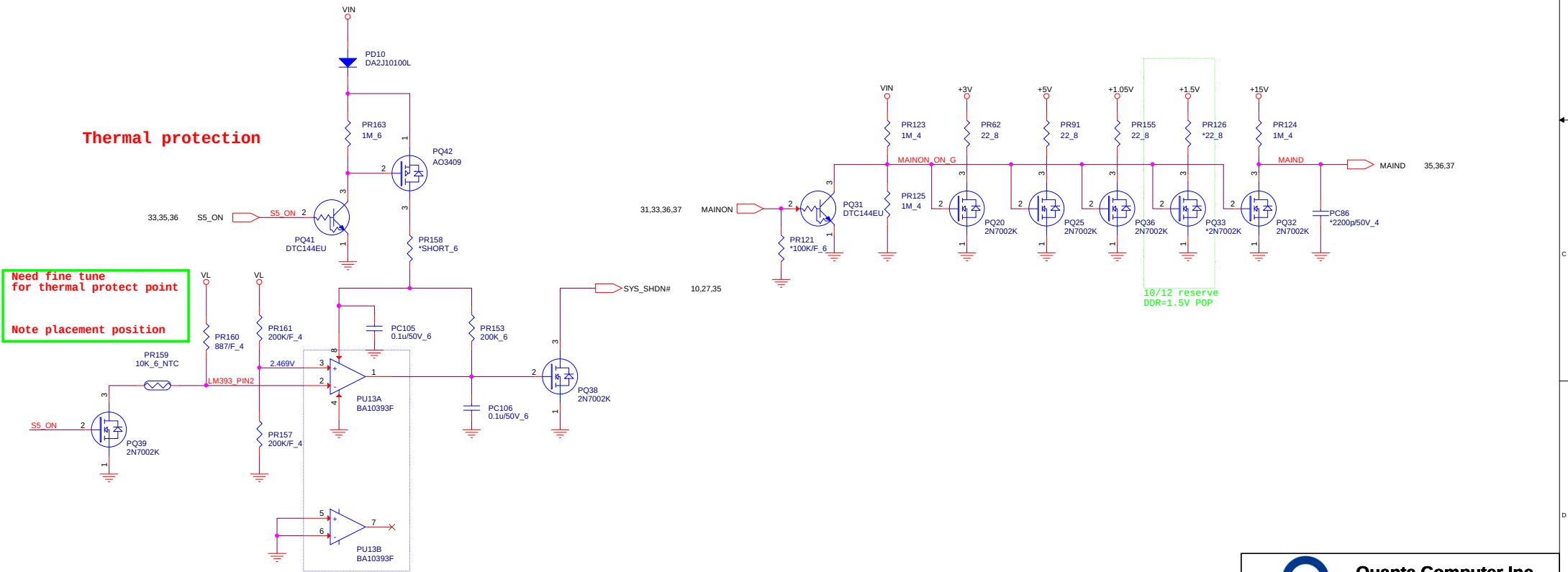
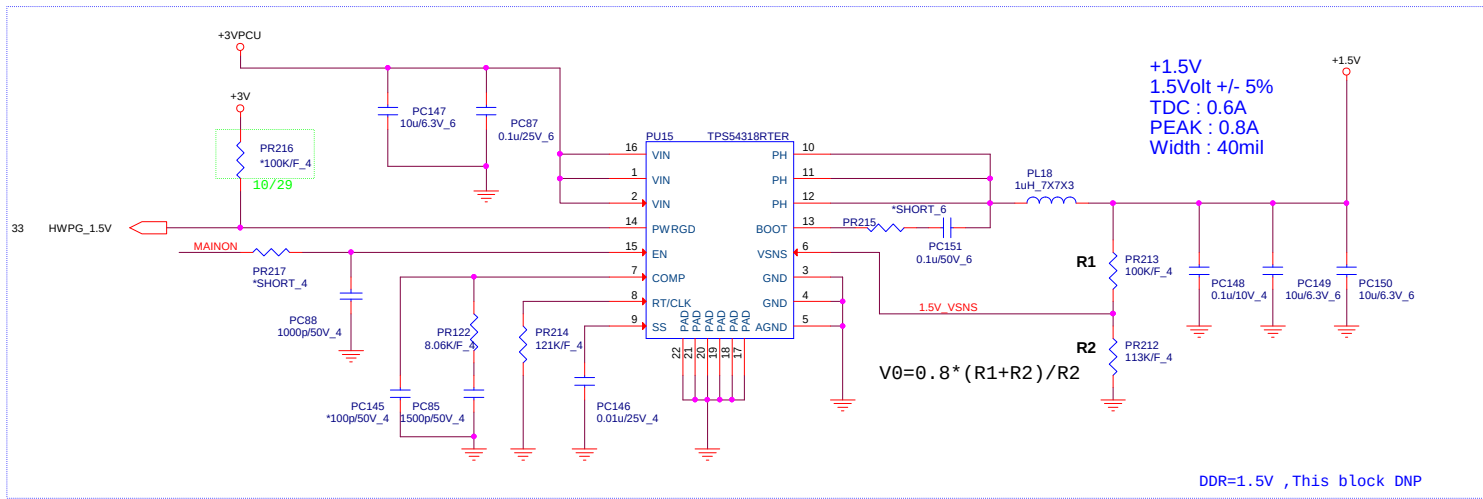
Quanta Computer Inc.
PROJECT : ZRQ

Size	Document Number	Rev
	+1.05V(TPS51211)	2A

Date: Friday, April 12, 2013 Sheet 36 of 47



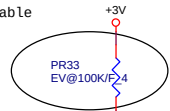




For EC control thermal protection (output 3.3V)

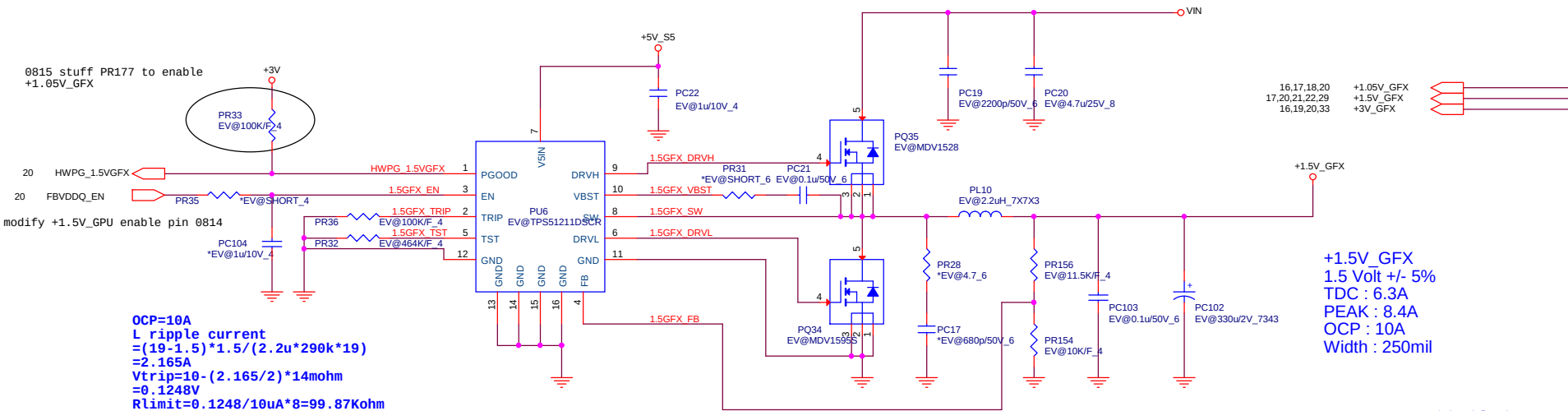


0815 stuff PR177 to enable
+1.05V_GFX



modify +1.5V_GPU enable pin 0814

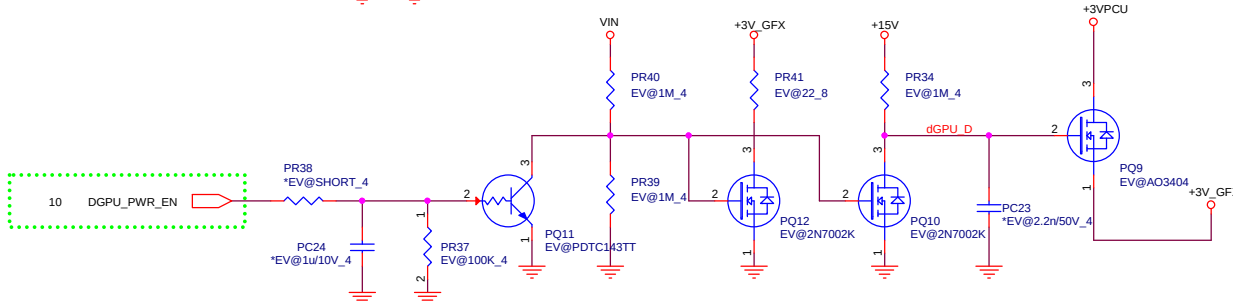
OCP=10A
L ripple current
 $= (19-1.5) * 1.5 / (2 * 290k * 19)$
 $= 2.165A$
 $V_{trip} = 10 - (2.165/2) * 14mohm$
 $= 0.1248V$
 $R_{limit} = 0.1248 / 10uA * 8 = 99.87Kohm$



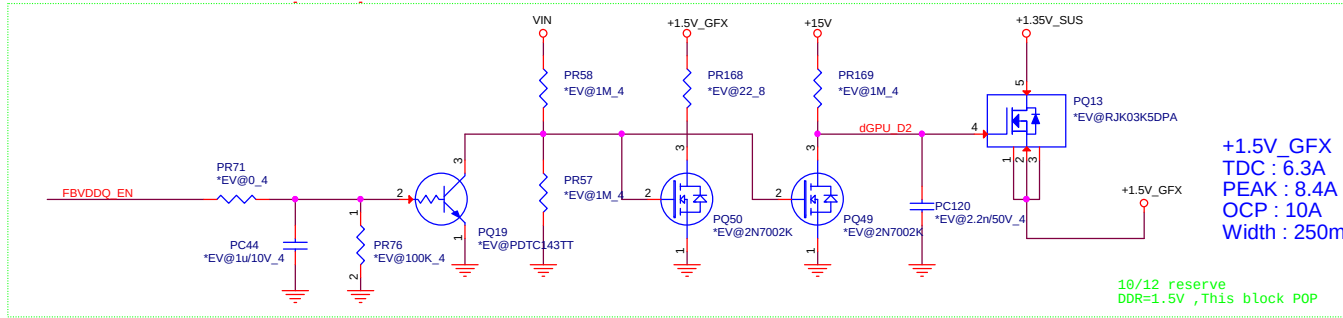
modify +1.05V_GFX enable pin 0814



+1.05V_GFX
TDC : 2.3A
PEAK : 3A
Width : 100mil

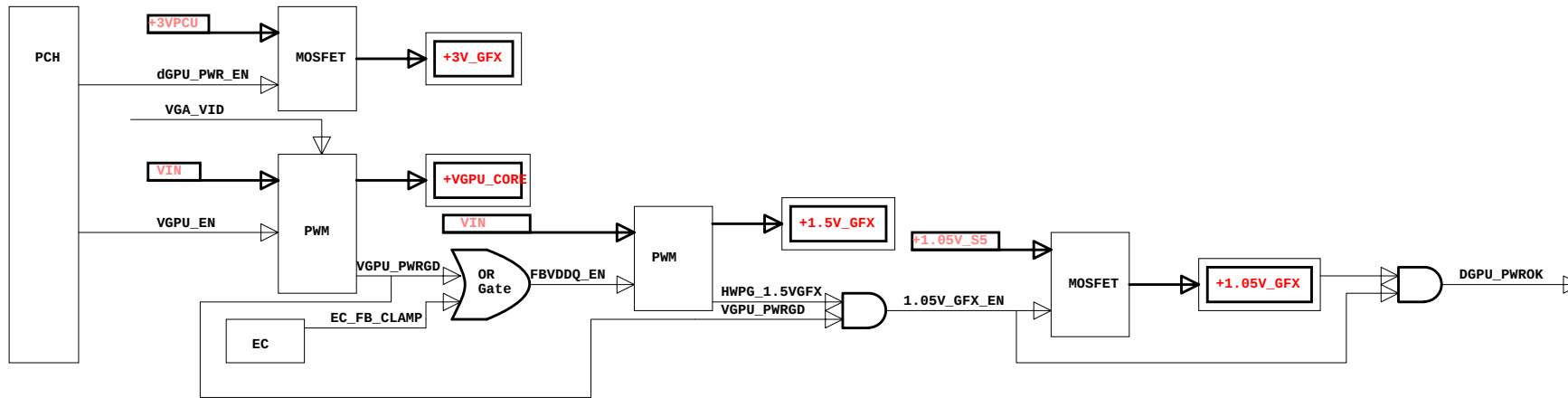


+3V_GFX
TDC : 0.76A
PEAK : 1A
Width : 40mil

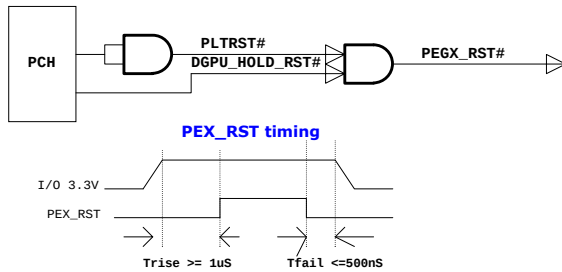


+1.5V_GFX
TDC : 6.3A
PEAK : 8.4A
OCP : 10A
Width : 250mil

VGA power up sequence



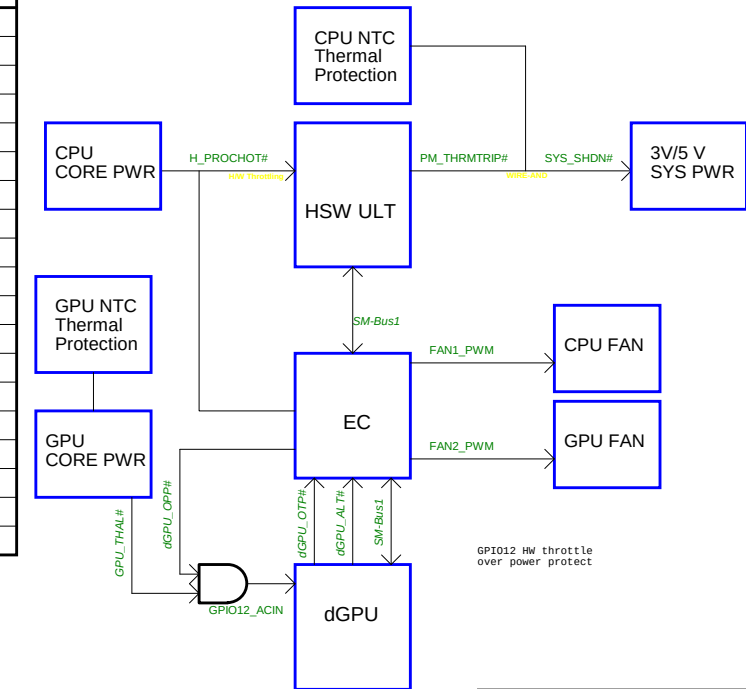
VGA Reset



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+3V_RTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	USB CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/SPK/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.35VSUS	+1.35V	CPU/SODIMM/MD POWER	SUSON	S0-S3
+DDR_VTT_RUN	+0.675V	SODIMM/MD Termination POWER	MAINON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE VCCST POWER	MAINON	S0
+VCCIN	variation	CPU CORE POWER	VRON	S0
+VGPU_CORE	variation	External GPU POWER	VGPU_EN	S0
+3V_GFX	+3.3V	External GPU POWER	dGPU_PWR_EN	S0
+1.5V_GFX	+1.5V	External GPU POWER	FBVDDQ_EN	S0
+1.05V_GFX	+1.05V	External GPU POWER	1.05V_GFX_EN	S0

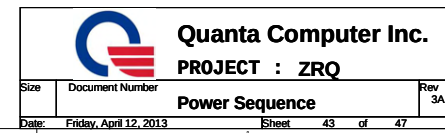
Thermal Follow Chart

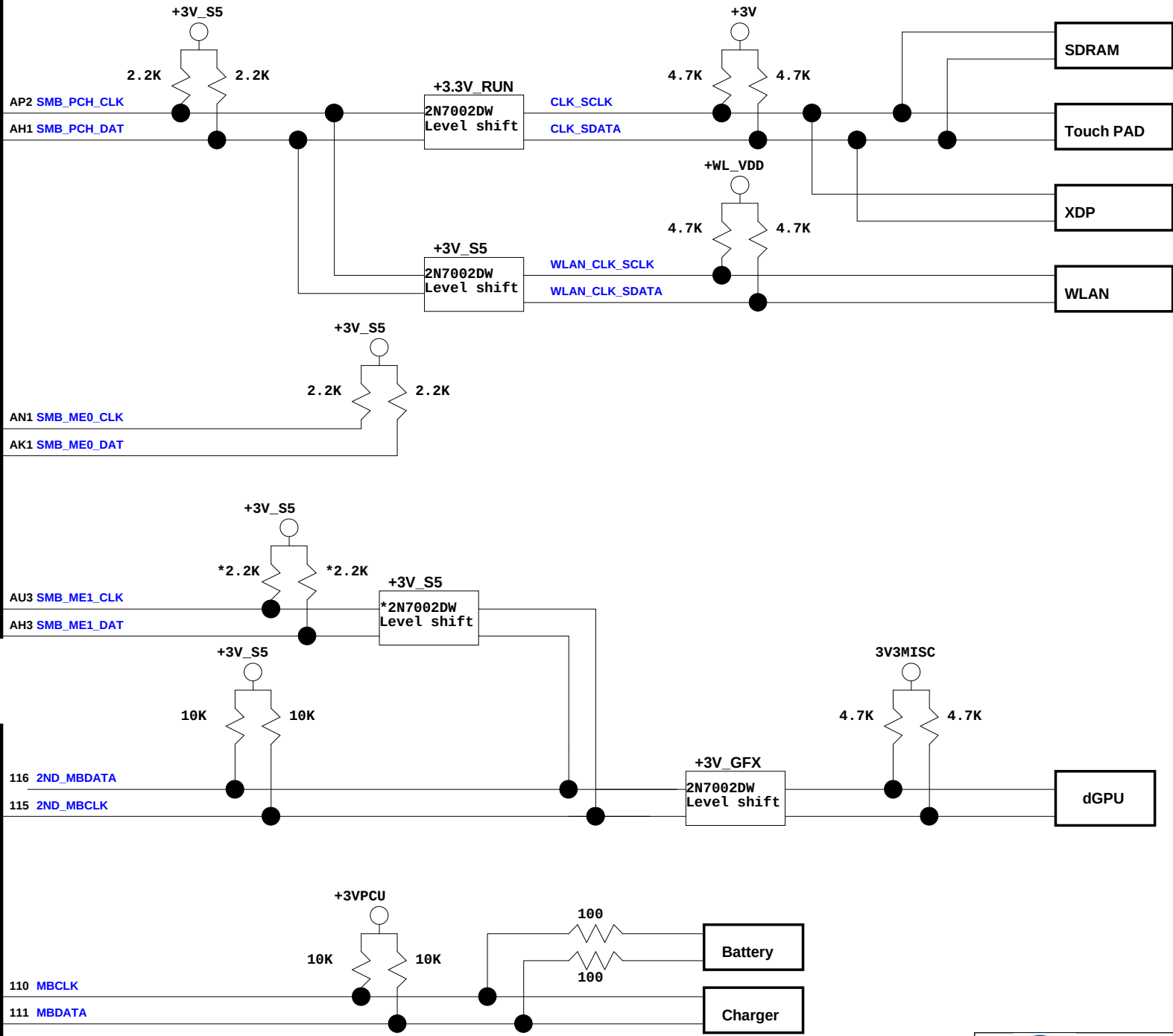
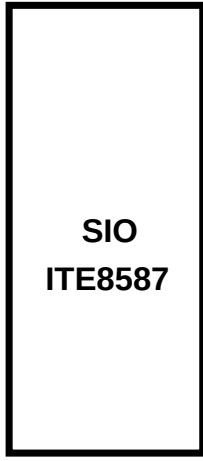
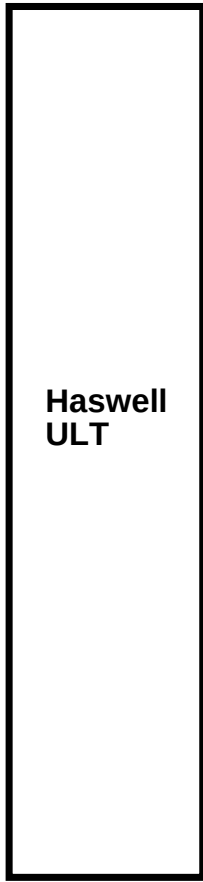


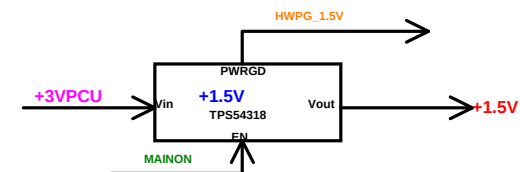
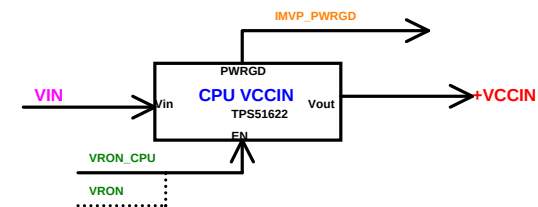
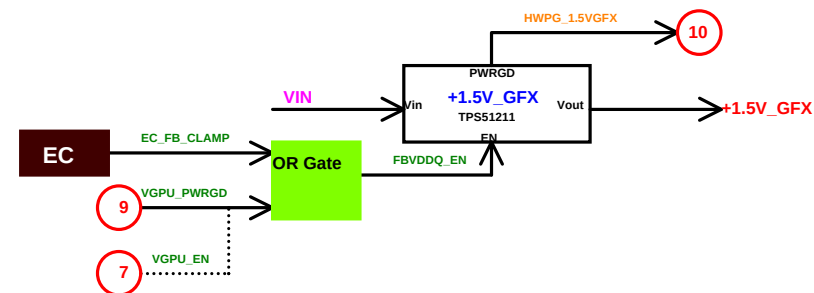
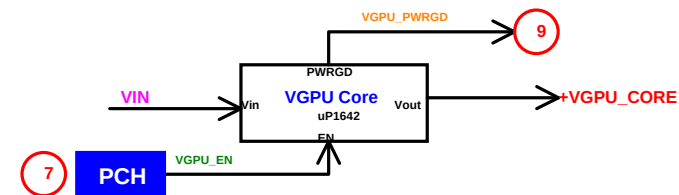
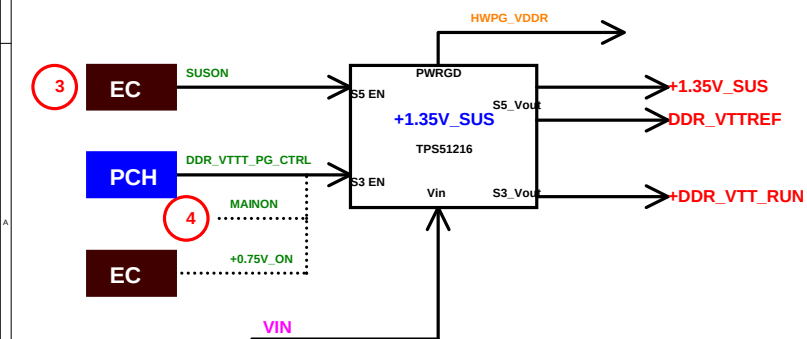
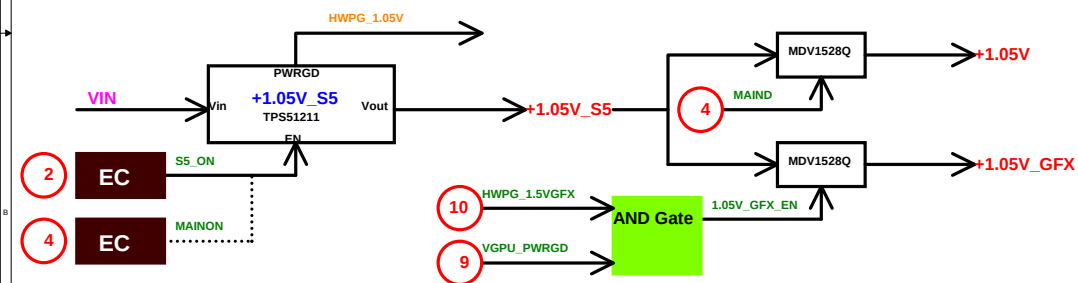
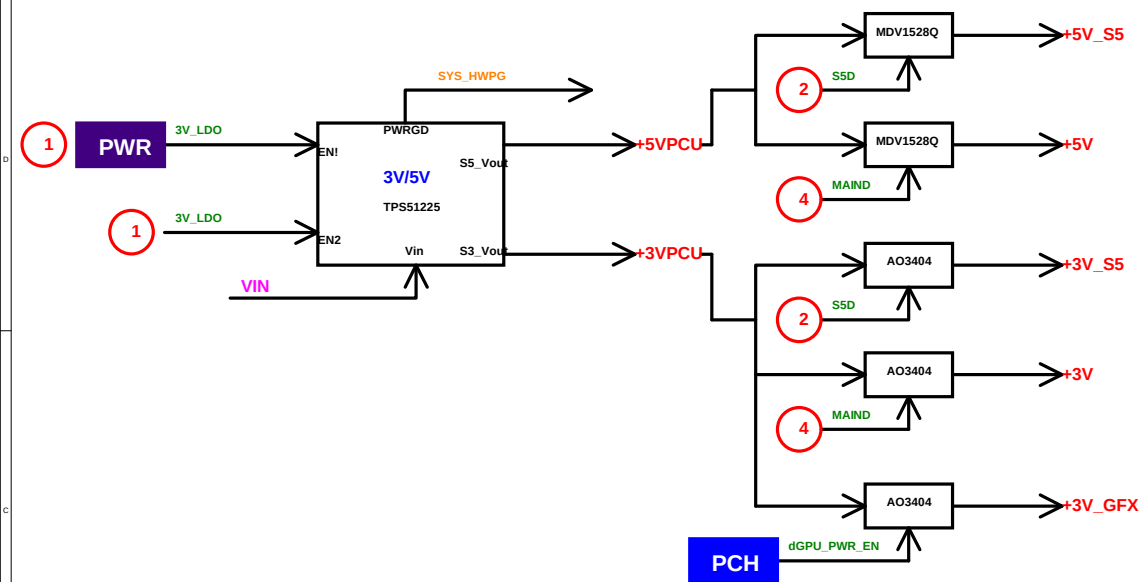
dGPU_OPP# EC notify HW throttle over power protect
dGPU_ALT# for ADPS circuit to inform EC NV dGPU VPS Alert
dGPU_OTP# VGA thrmtrip# => inform EC over temperature protect

Support Deep Sx

depend on A measure
result to implement
for B test







Model	Version	CHANGE LIST			
ZRQ	1A				
2A		1	Add R886 Pull down for EDP_JPD(Intel check list)(Page 62)		
		2	Add RB11 and reserve RB09 for Codes Vendor request.(Page 30)		
		3	Change R345 footprint from 0402 to 0603.(Page 14)		
		4	Change U10 to correct PN AL007534001.(Page 31)		
		5	Improve IMVP_PWBGD voltage to low , to del R86_Q9 , R51_Q50 ,R495 and add U55 , C767 , RB07. (Page 18)		
		6	Change CN2 to 12 PIN connect, DFFC12FR034 (Page 31)		
		7	Change SW6 from DHP00BTEPV00 to DHPATE2CK03.(Page 29)		
		8	Move Hall sensor funtion to USB0.B.(Page 24)		
		9	Add R828 100K PD for MAINON, Upgrade U27 from AJ0854870F02 to AJ0854870F03. (Page33)		
		10	Collect nemeame +V1.85S_VCCPCPU to +V3.3S_VCCSDIO. (Page11)		
		11	Q7 change from PMF780SN to BAW70020002. (Page25)		
		12	Correct U41 footprint to s00p5-p-a-tchb1a-b. (Page23)		
		13	Change LE5D5.LED6 P/N from BEB00024ZA0 to BEB0002EZA0. (Page27)		
		14	Del Q5 ,Q47,R51,R25 , add U56,C768. (Page13)		
		15	DEL PL5,PL6,PL7,PL8. (Page34_Power)		
		16	Change PR145 from CS28872FB08 to CS29312FB13. (Page38_Power)		
		17	Change PR143 from CS45362FB00 to CS44992FB11. (Page38_Power)		
		18	Change PR129 from CS22672FB12 to CS22702FB14. (Page38_Power)		
		19	Change PR5 from CS1002FB26 to CS25762FB01. (Page38_Power)		
		20	Change PR141 from CS32432FB19 to CS32262FB15. (Page38_Power)		
		21	Change PC123 from CC64704MZ10 to CH6104KEA00. (Page40_Power)		
		22	Add PC152,PC153,PC154 to CH6104KEA00. (Page40_Power)		
		23	Change PL12,PL13 from CV+24P0MZ00 to CV+36T0MZ01 10X10 size. (Page40_Power)		
		24	SWAP USB0 and USB1. (Page09)		
		25	Change CN27 to DFHS2FR044 ,same as CN18 (Page 26)		
		26	add CN12 PIN4 for USBPWR3. (Page 31)		
		27	CN9 change footprint to dp-adis0022-p001a-20p-smt. (Page 23)		
		28	Dpop R728 and Pop R727 to save Deep S3 can't wakep issue. (Page 10)		
		29	Del C429. (Page20)		
		30	Add R826(VRON) ,R827(SON) 100K to Gnd. (Page33)		
		31	Change CN9 PN to DFTD20FR001. (Page23)		
		32	Add C735 ,0.1u for Vendor request. (Page28)		
		33	Add C736 ,0.1u and reserve C727 ,4.7u for Vendor request. (Page28)		
		34	Change R348 Pu ligns to +3V. (Page20)		
		35	TEMP_MBAT from battery connect pin 5 to pin 6 (BATT_EN0). (Page34)		
		36	Change R354(PCH_PWROK) from 10 k to 100K. (Page07)		
		37	Reverse RB00 ,RB10 ,0 Ohm. (Page30)		
		38	Change JP18 Packing and PN same as JP19. (Page37)		
		39	Add RB35 for Vendor request. (Page23)		
		40	Change R491 from 1M to 5.1M. (Page23)		
		41	Change R491 from 12i to 120ohm(Intel Check list). (Page04)		
		42	Change SUSL_EDP power from +3V_55 to +3V_PCV. (Page27)		
		43	Change CN13 to DFHS00F0A47 10-4, also to PE request. Footprint is "gs12401-1011-40p-e-ub-smt. (Page24)		
		44	VCP1_PSI Pull high from +3V to +3V_55. (Page40)		
		45	B-SMT USE RTL841BA-CC need Dpop R295 and change U21 PN to AL008411004. (Page28)		
		46	C596,C591 change from 18P to 12PV0. (Page09)		
		47	C278,C284 change from 27P to 12PV0. (Page08)		
		48	Dpop R147,R106,R04,R534 and Pop R01,R05,R146,R533 to support Qual Mode. (Page10)		
		49	Pop P01044. (Page40_Power) 内部行文		
		50	Change PU8 from AL001642000 to AL001642001. (Page40_Power) 内部行文		
		51	PC6 EOD Part change to CH4331K9006. (Page38_Power)		
		52	PC5,PC85 EOD Part change to CH21506KB14. (Page38_39_Power)		
		53	Change U27 from AJ083870F03 to AJ083870F04. (Page33) 内部行文		
		54	Add level Shift funtion. (Page25)		
		55	Dpop PR75. (Page40_Power) 内部行文		
		56	Change PC15 to 1000p_50V(CHE1006J010). (Page38_Power) 内部行文		
		57	Dpop PR75. (Page40_Power) 内部行文		
3A		1	Dpop R226, Pop Q26(BAW70020002) ,R795 (CS31002FB20) for CG6 funtion.(Page19)		
		2	Swap Pin 25 and Pin 32.(Page33)		
		3	Del D31,C519 , and Add Q69,C738,CR22,CR23,CR24 for SDA request.(Page23)		
		4	Add Test Pad on SW5_SWB for SMT request.(Page27,33)		
		5	Add C317 ,4.7u for Vendor request.(Page20)		
		6	SWAP CLKOUT_PCIE. (Page09)		
		7	Pop R477, R478 ,R479, R480 _000hm(CS11002FB22)for HDMI EMI Issue.(Page25)		
		8	Pop C655,C654 _10p(CB01006JB00) for SD CLK EMI Issue. (Page29)		
		9	Pop Bltch C399 _22p(CB0206JB00) for EMI issue. (Page30)		
		10	DelPop PR117. (Page34)		
		11	C285 change from 0402 to 0603 size. (Page20)		
		12	Del CNS,C272,C253 footprint. (Page13)		
		13	Dpop R336 ,Pop R533 for Lan can't link to exlurer. (Page20)		
		14	Dpop R340. (Page20)		
		15	Reserve RB12 for PCH_LAN_WAKE#.(Page26)		
		16	Add RB15,C740 and pop R310 for softstart of Lan VCC.(Page20)		
		17	R600 connect to CLK_PCIE_REQ49. (Page09)		
		18	Dpop SW7. (Page23)		
		19	Del JP Resistor 0.001F_3720 (CS+0010F100) : JP5 ,JP6 ,JP10 ,JP11 ,JP12 ,JP13 ,JP14 ,JP15 ,JP17 ,JP18 ,JP19 ,JP20 ,JP21 ,JP16.		
		20	Del 0_4 (CS00002JB30) to SHORT PAD_4 : PR0,PR0,PR11,PR13,PR16,PR18,PR30,PR33,PR36,PR44,PR61,PR66,PR83,PR106,PR131,PR139,PR165,PR170,PR178,PR180,PR185,PR191,PR193,PR194,PR196,PR200,PR204,PR205,PR209,PR211,PR217,PR106		
		21	Del 0_6 (CS00003J951) to SHORT PAD_6 : PR31,PR46,PR54,PR77,PR90,PR181,PR201,PR203,PR215,PR158		
		22	Del 0_8 (CS00004JA00) to SHORT PAD_8 : PR136		
		23	Add RB13 ,0 OHM.(Page26)		
		24	Change C740 from 0603 to 0402 size.(Page20)		
		25	Dpop Q29 , R276,Pop R321 and change R320 to 1K to meet Lmwake signal spec.(Page20)		
		26	Pop R531,R531,R531,20; and Pop R54,R47,R49,R55,R490,R407,R408,R401.(Page20)		
		27	Del JP7 ,JP8 ,JP9 (CS+001AGM13).(Page05)		
		28	Change to 0402 shortpad:R45,R69,R177,R215,R236,R237,R239,R274,R277,R283,R288,R311,R320,R334,R353,R440,R409,R419,R423,R424,R425,R426,R430,R432,R434,R448,R449,R450, R513,R570,R573,R587,R591,R596,R625,R641,R652,R653,R678,R695,R712,R719,R722,R733,R734,R735,R766,R741,R758,R759,R760,R761,R762,R763,R764,R765,		
		29	Change to 0603 shortpad:R107,R111,R150,R194,R197,R212,R229,R233,R234,R252,R260,R290,R303,R304,R330,R350,R351,R352,R356,R358,R441,1,415,R418,R422,R431,R433,R440,R441, R442,R443,R444,R445,R446,R447,R450,R475,R766,R767		
		30	Change to 0805 shortpad:R165,R174,R179,R190,R217,R268,R270,R452,R470,R559,R560,R732,R737,R749		
		31	Change R400,R420 from 47 ohm to 50 ohm.(Page30)		
		32	Change R411, R422 from shortpad to 0603 footprint.(Page30)		

Model	Version	CHANGE LIST				
ZRQ	3B	1R276 change fro m 10Ks to 1K , Ddpop R328. (PCIE_LAN_WAKE#), 内部行文 2Change C24 KB Conn P8 to DFF C26FR063. (Page 32), 内部行文 3Change U27 E.C to E version A10B5670F05. (Page 33), 内部行文 4Fine tune Amp Gain =>R422,R411 change from 0 ohm to 1k , and psp R421,R410 to 1.62K. (Page 30) 5Change TEMP_MBAT from Pin 6 to Pin 5 of P.J1. (Page 34) 6Ddpop Q24 , and Add R228 to solve level abnormal issue for CG6. (Page 19) 7Add RE16 and net "LB_PWR_CNN_Q" to stuff Q69 always for safety issue. (Page 19) 8Reserve R855,R859 and add R854,R857. (Page 23) 9For WHQL Change USB Port1 and Port4 10Add new on Board RAM HYNIX H5TC4G63AFR-PRBA RAM 1D:0000 11Del L35,L36,L6,L7,L8,L29,L12,L13,L32,L16,L34				
	3C	1Change to 0402 shortpad: R725,R724,R711,R716,R26,R27,R28,R29,R32,R33,R483,R484,R493,R492,R56,R57,R58,R59,R96,R89,R669,R664,R702,R638,R639,R651,R225,R346,R355,R770,R705,R790,R73 , R455,R456,R457,R458,R459,R343,R406,R596 2For HDMI 7-2 issue change R37,R38,R39,R40,R41,R42,R43,R44 To 470 ohm and remove R478,R479,R477,R480 (Page 25) 3For T1 HD3S2521 issue R77,R79,R592,R503 need mount 10K, change R528 from 100 ohm to 0 ohm and remove R854,R857 , add R855,R859. (Page 23) 4Change to 0603 shortpad: R373,R337,R382,R297,R235,R326,R322,L30,R385,R220,R254,R359				
	3F	1.Add C245 for intel request for G3 can't boot issue				
DOC NO.	PROJECT MODEL	ZRQ	APPROVED BY:		DATE:	
	PART NUMBER:		DRAWING BY:		REVISION:	
			Quanta Computer Inc. PROJECT : ZRQ Change list-2			