C743

ZRJ BLOCK DIAGRAM

01

GPU CORE PWR RT8204 P45	CHARGER ISL88731 P53
GPU IO PWR UP6111AQDD P46	3/5V SYS PWR RT8206 P52
Discharger/+3V_M P54	CPU CORE PWR ISL95831 P43~P44
+1.8V UP61111AQDD P51	CPU +1.05V_VTT UP61111AQDD P47
CPU iGPU_CORE RT8204 P45	PCH +1.05V UP61111AQDD P49
+0.85V ISL62871 P48	DDR3 PWR RT8207A P50

intel <MCH Processor>
SandyBridge QC /DC 35W
rPGA 988 (37.5mm X 37.5mm)
PCI-E X16
DDR SYSTEM MEMORY
FDI CLK DMI
P4~P7

DDR III - SODIMM 0
DDR III - SODIMM 1
P14, 15
Dual Channel DDR III 1066/1333 MHz

PCIE X16 5GT/s

X'TAL 27.0MHz
nVIDIA GPU
N12GS & N12GV Fermi
Package GB2-128
Optimus (Muxless)
P16~P22

Channel A
Channel B
VRAM GDDR3
64(or 128)Mb x16 x8 pcs
P14, 15

EXT_HDMI
EXT_CRT
EXT_LVDS

CRT P24
LVDS P24
USB-8
HDMI P24

FDI interface 2.7GT/s
X4 DMI interface 5GT/s

HDD (SATA) P25 — SATA0
ODD (SATA) P25 — SATA5

intel <PCH>
CougarPoint 0.7
mBGA 989 (25mm X 25mm)
FDI CLK DMI
SATA Gen3
SATA Gen2
iGFX Interfaces
USB
HDA
PCI-E
RTC P9
SPI
LPC
P8~P13

INT_CRT
INT_LVDS
INT_HDMI

USB 2.0 * 3 USB0,1,2 P27
Bluetooth USB9 P27
CCD USB6 P24
USB 2.0

Azalia

X'TAL 32.768KHz

PCI-Express Gen2 5GT/s

X'TAL 25MHz X'TAL 25MHz

PCIE6 — Giga LAN Arthohorus AR8151 P26
PCIE1 — Mini Card WiFi +BT (Half) USB3 P28
PCIE2 — Mini Card 3G USB4 P28
CardReader Realtek RTS5209 USB5 P23

USB3
USB4

Transformer P26
RJ45 P26
SIM Card Conn DB P28

Audio CODEC CONEXANT CX20584-21Z P30
Dual SPI ROM 4MB x1 (Basic ME+Braidwood) P9
WPCE791/FLASH NPCE971 P31

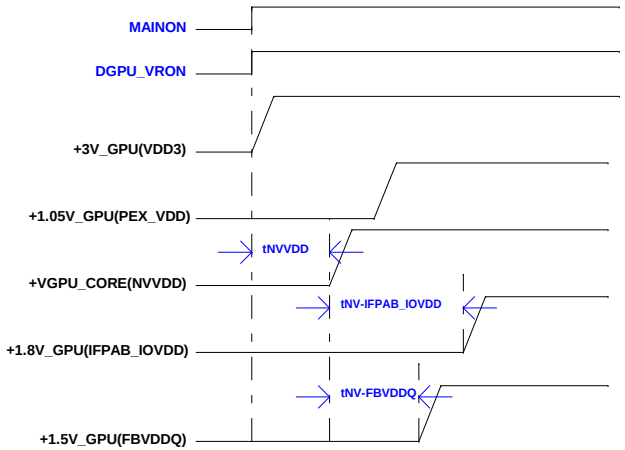
HP Jack P30
MIC Jack P30
SPK P30
DMIC P24
SPI ROM P31
Touch Pad P29
Keyboard P29
Light Sensor P33
Button on mechanical key P31
Fan Driver (PWM Type) P42

Note:
HM65 not support USB 6 & 7
HM65 not support SATA 2 & 3

Quanta Computer Inc.
PROJECT : ZRJ

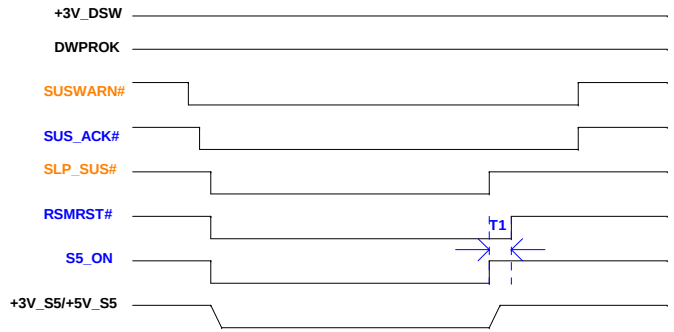
Size	Document Number	Rev
	Block Diagram	1A
Date: Thursday, December 23, 2010	Sheet 1 of 41	

N12P-GE Power Up Sequence



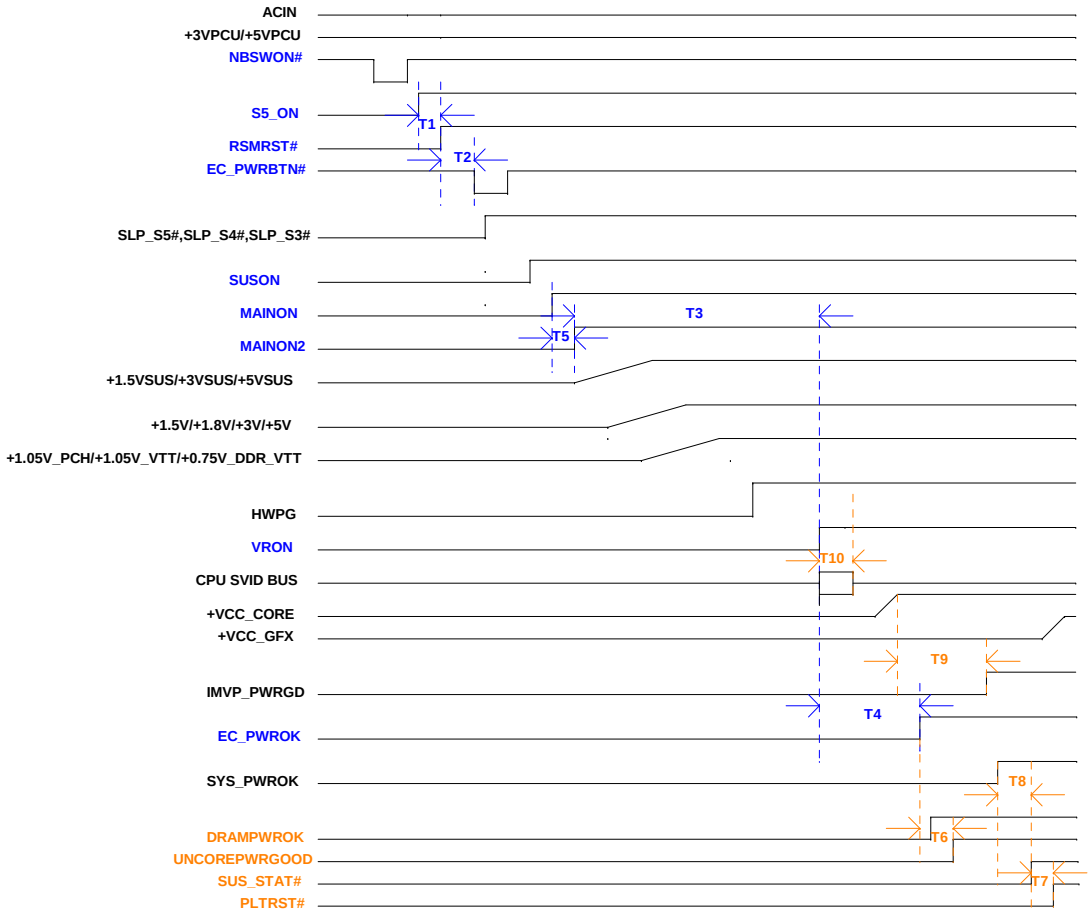
N12P-GE Power up Sequence
tNVVDD>0
tNV-IFPAB_IOVDD>0
tNV-FBVDDQ>0

Deep S4/S5 off-on Sequence

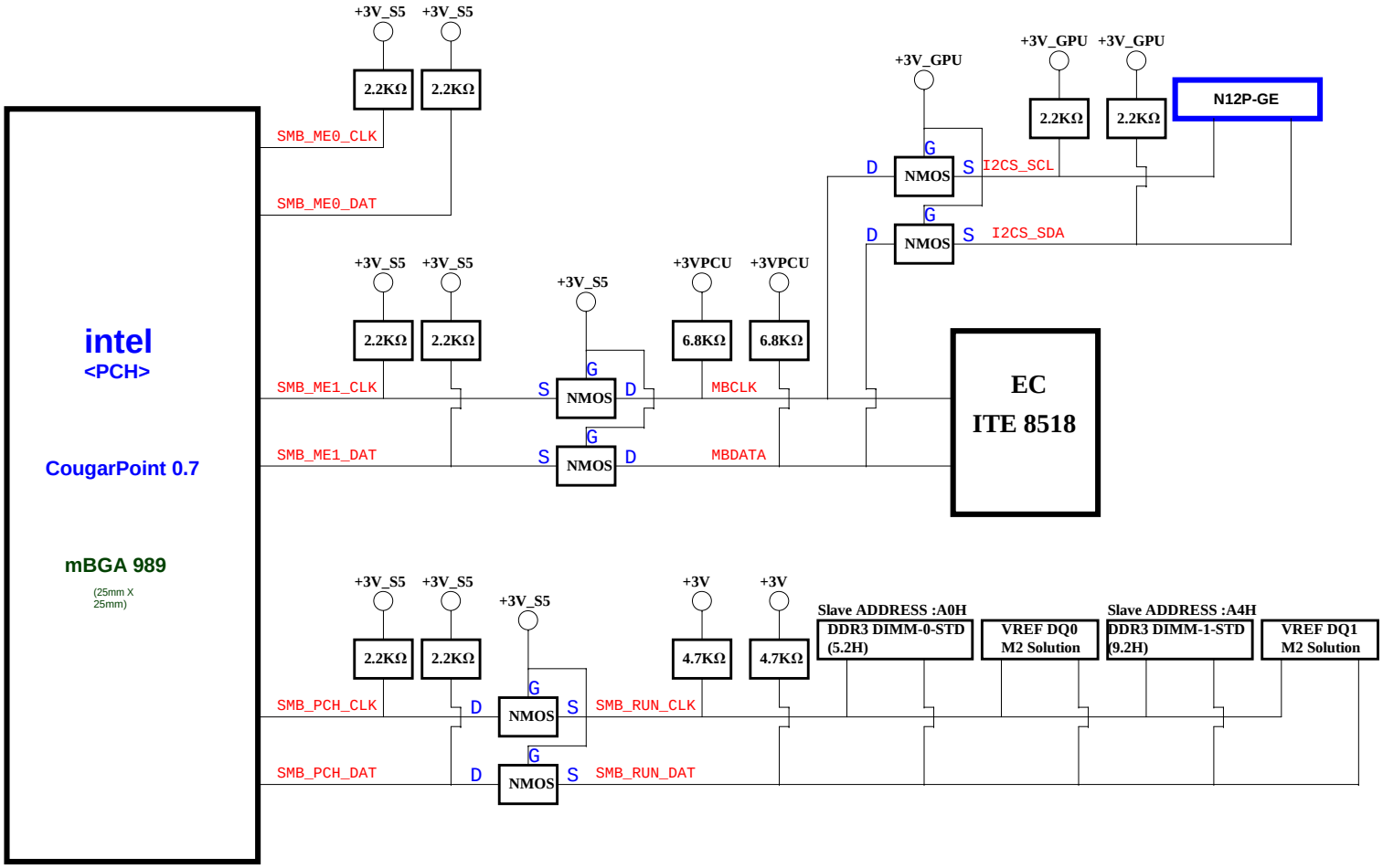


Deep S4/S5 Sequence
T1: S5_ON TO RSMRST# = 30ms (spec:mini 10ms)

MS15-UMA Power-ON Sequence



System Power Sequence
T1: S5_ON TO RSMRST# = 30ms (spec:mini 10ms)
T2: RSMRST# TO EC_PWRBTN# = 110ms (spec:mini 100ms)
T3: MAINON2 TO VRON = 110ms (spec:mini 99ms)
T4: VRON TO EC_PWROK = 10ms (HWPG NEED TO BE HIGH at that time)
T5: MAINON to MAINON2 =500us
T6: EC_PWROK to UNCOREPWRGOOD =2ms(Min)
T7: SUS_STAT# to PLTRST# =60us(Min)
T8: SYS_PWROK to SUS_STAT# =1ms(Min)
T9: +VCC_CORE to IMVP_PWRGD =5ms(Max)
T10: VRON to accept SVID command. =5ms(Max)



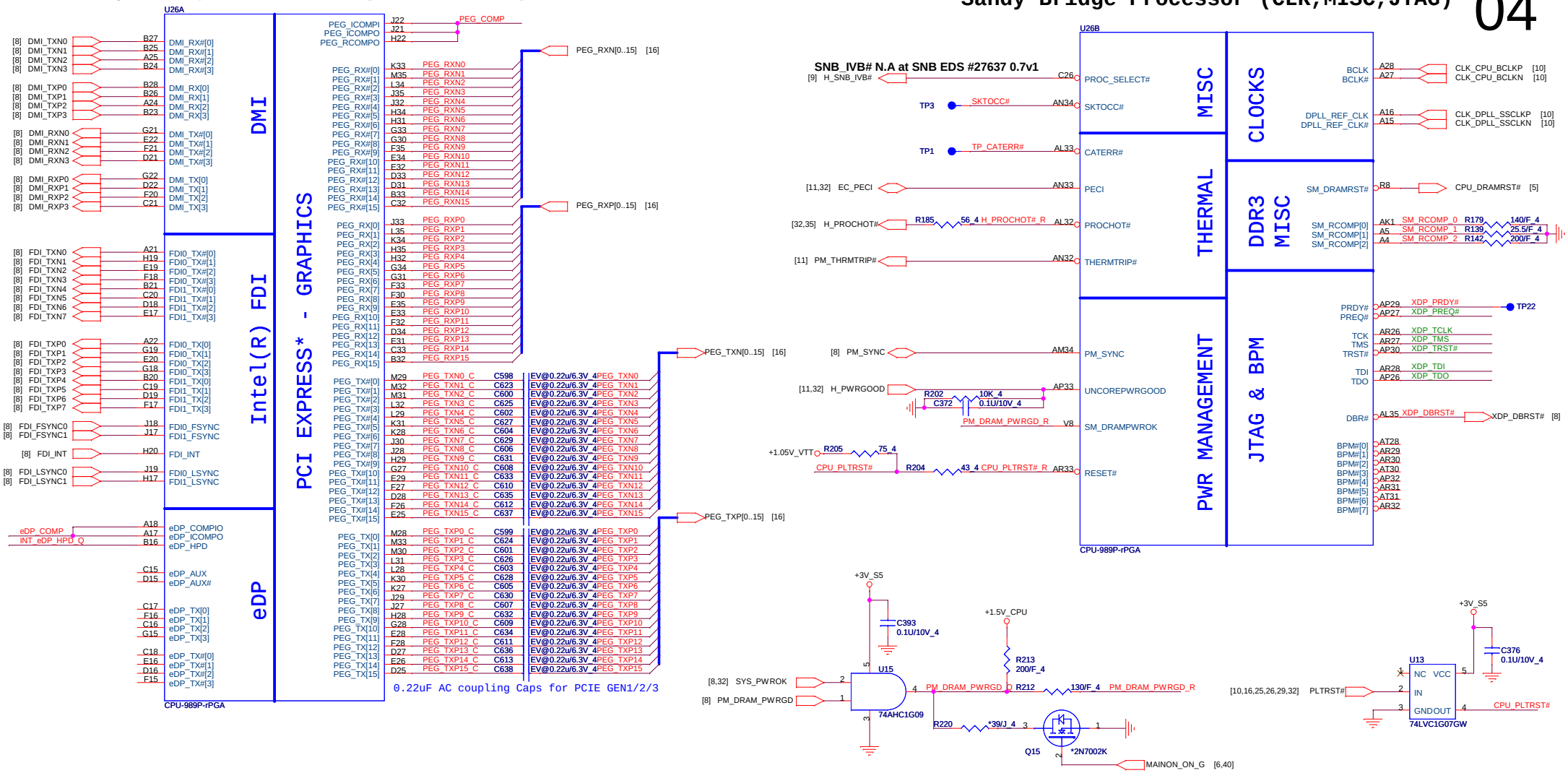
Quanta Computer Inc.
PROJECT : ZRJ

Size	Document Number	Rev
	SMBus Address	1A
Date: Monday, December 13, 2010	Sheet 3 of 41	

Sandy Bridge Processor (DMI,PEG,FDI)

Sandy Bridge Processor (CLK,MISC,JTAG)

04



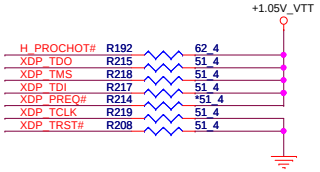
DP & PEG Compensation

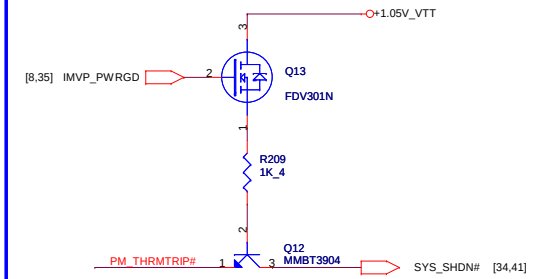
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms

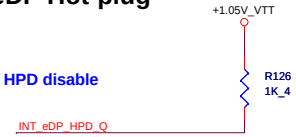
PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up(CPU)





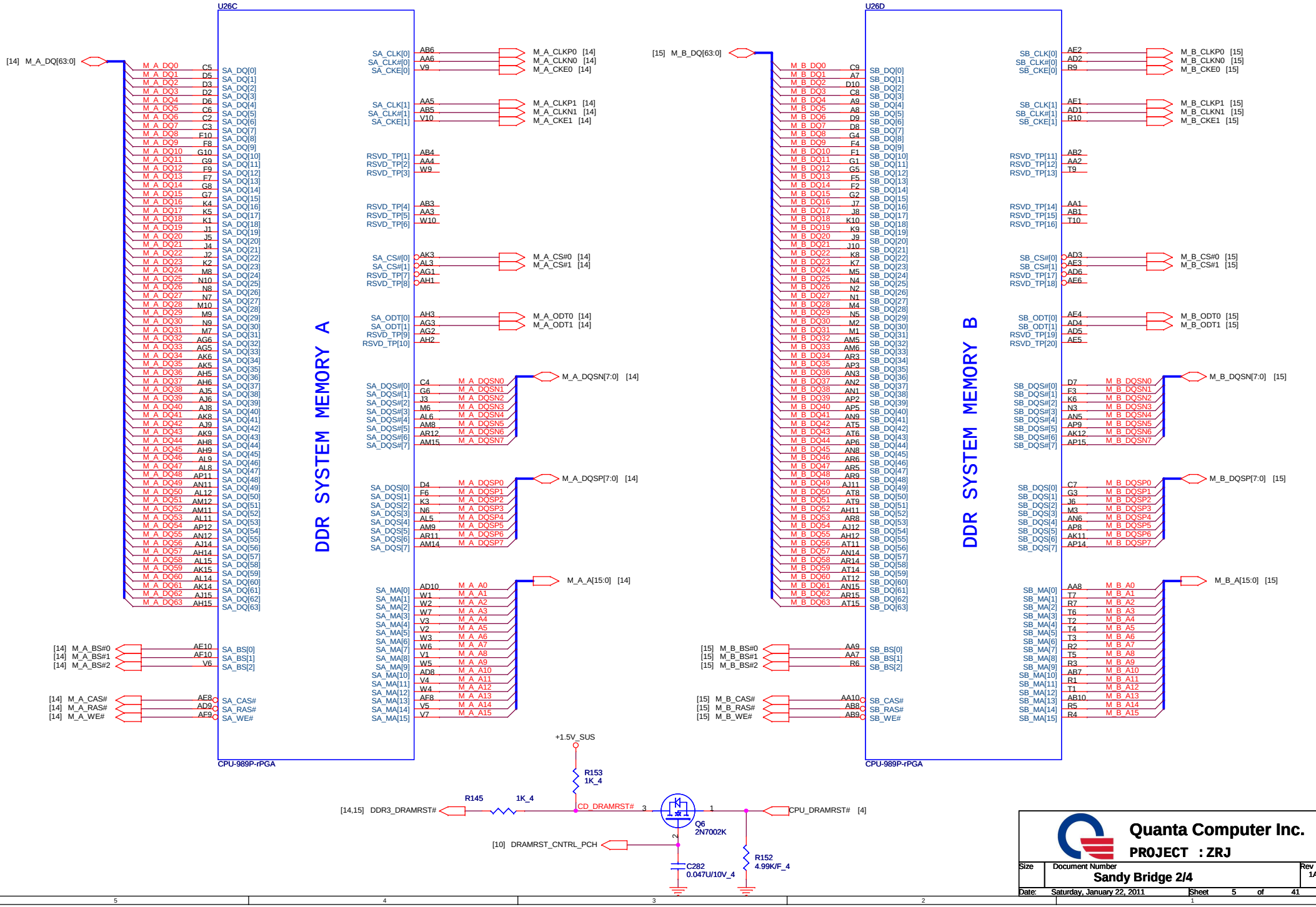
eDP Hot-plug



Quanta Computer Inc.
PROJECT : ZRJ

Size	Document Number	Rev
	Sandy Bridge 1/4	1A
Date: Saturday, January 22, 2011	Sheet 4 of 41	

Sandy Bridge Processor (DDR3)



Quanta Computer Inc.

PROJECT : ZRJ

Size	Document Number	Rev
	Sandy Bridge 2/4	1A
Date: Saturday, January 22, 2011	Sheet 5 of 41	

Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

06

CPU Core Power

SNB 45W:52A

Spec

470uF/4mohm x 4

22uF x 16

10uF x 10

CPU VTT

SNB 45W:8.5A

Spec

330uF/6mohm x 2

22uF x 12

22uF x 7 (Non-stuff)

CPU VGT

SNB 45W:21.5A

Spec

470uF/4mohm x 2

22uF x 12

CPU VCCPL

SNB 45W:1.5A

Spec

330uF/7mohm x 1

10uF x 1

1uF x 2

CPU MCH

SNB 45W: 5A

Spec

330uF/6mohm x 1

10uF x 6

Real

10uF x 6

CPU SA

SNB 45W: 6A

Spec

330uF/7mohm x 1

10uF x 3

U26F

CPU-989P-rPGA

POWER

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

U26G

POWER

GRAPHICS

SENSE LINES

VREF

DDR3 -1.5V RAILS

SA RAIL

1.8V RAIL

MISC

CPU-989P-rPGA

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK

SVID DATA

SVID ALERT

Place PU resistor close to CPU

Place PU resistor close to CPU

4.5A

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

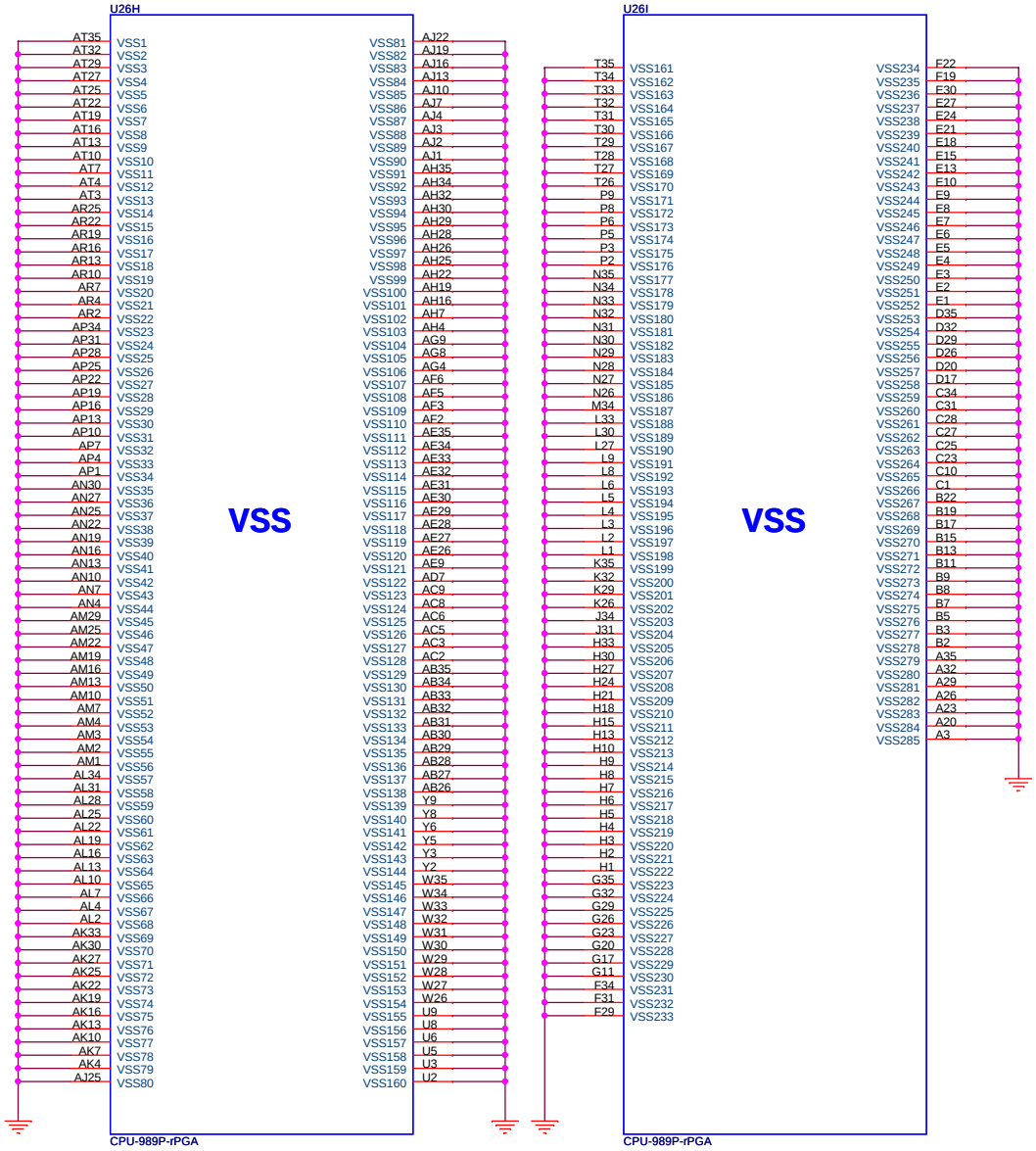
Quanta Computer Inc.

PROJECT : ZRJ

Size: | Document Number: Sandy Bridge 3/4 | Rev: 1A

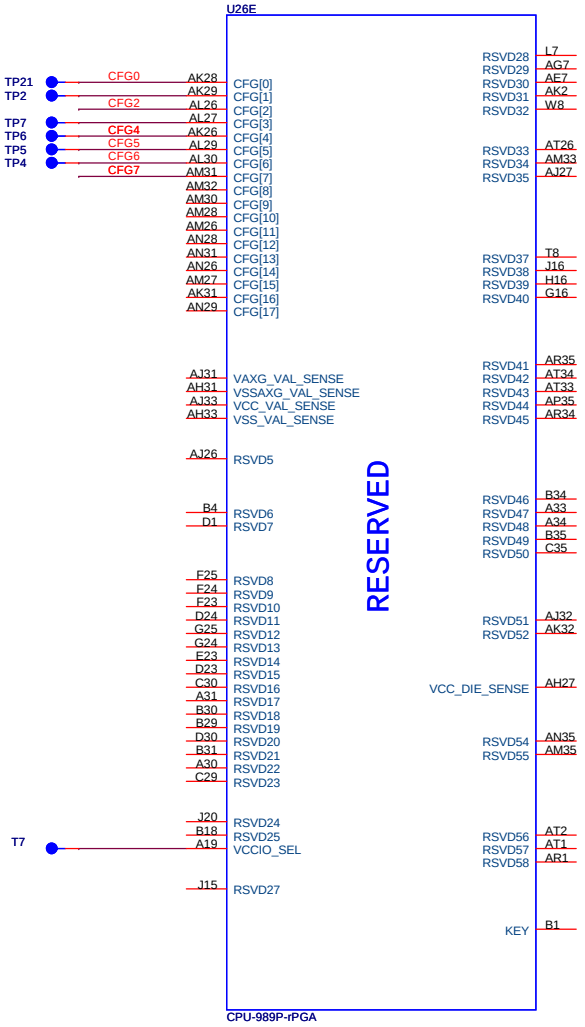
Date: Saturday, January 22, 2011 | Sheet 6 of 41

Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)

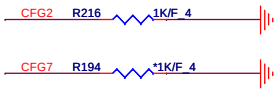
07



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



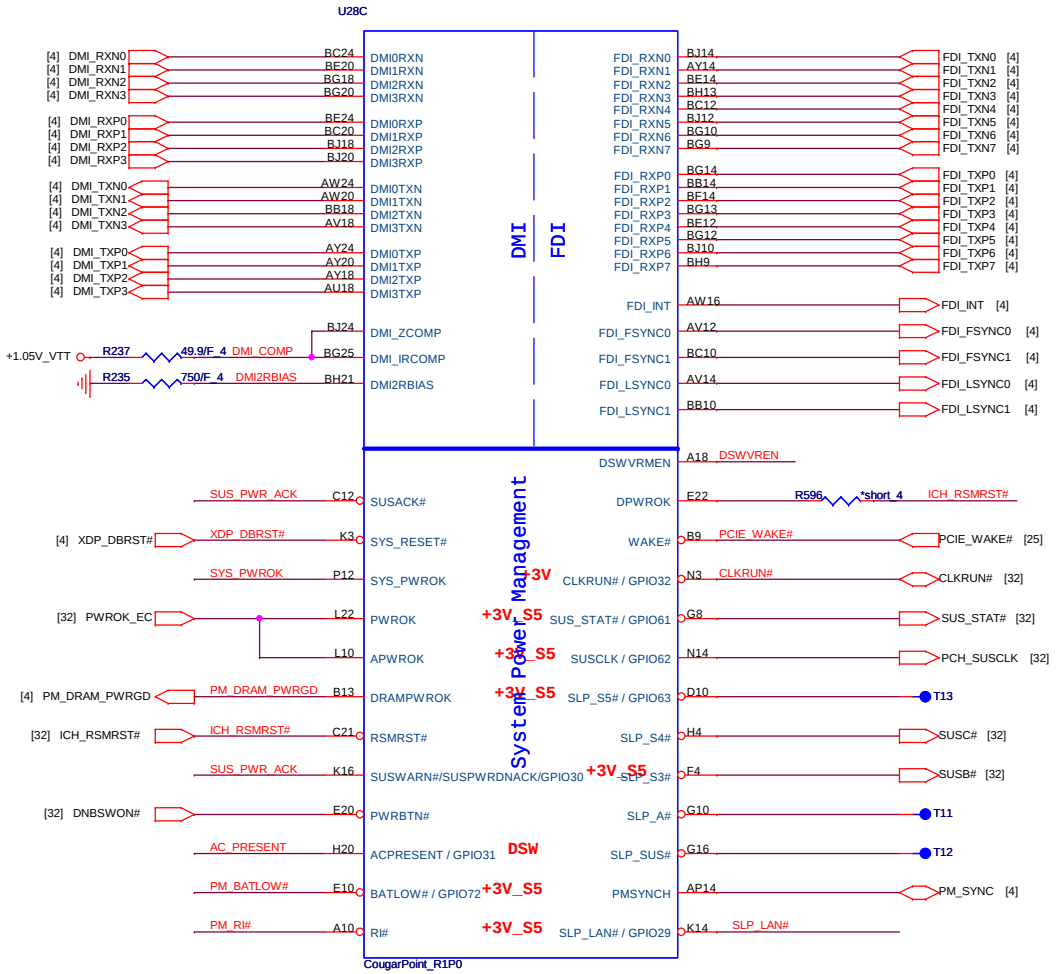
CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

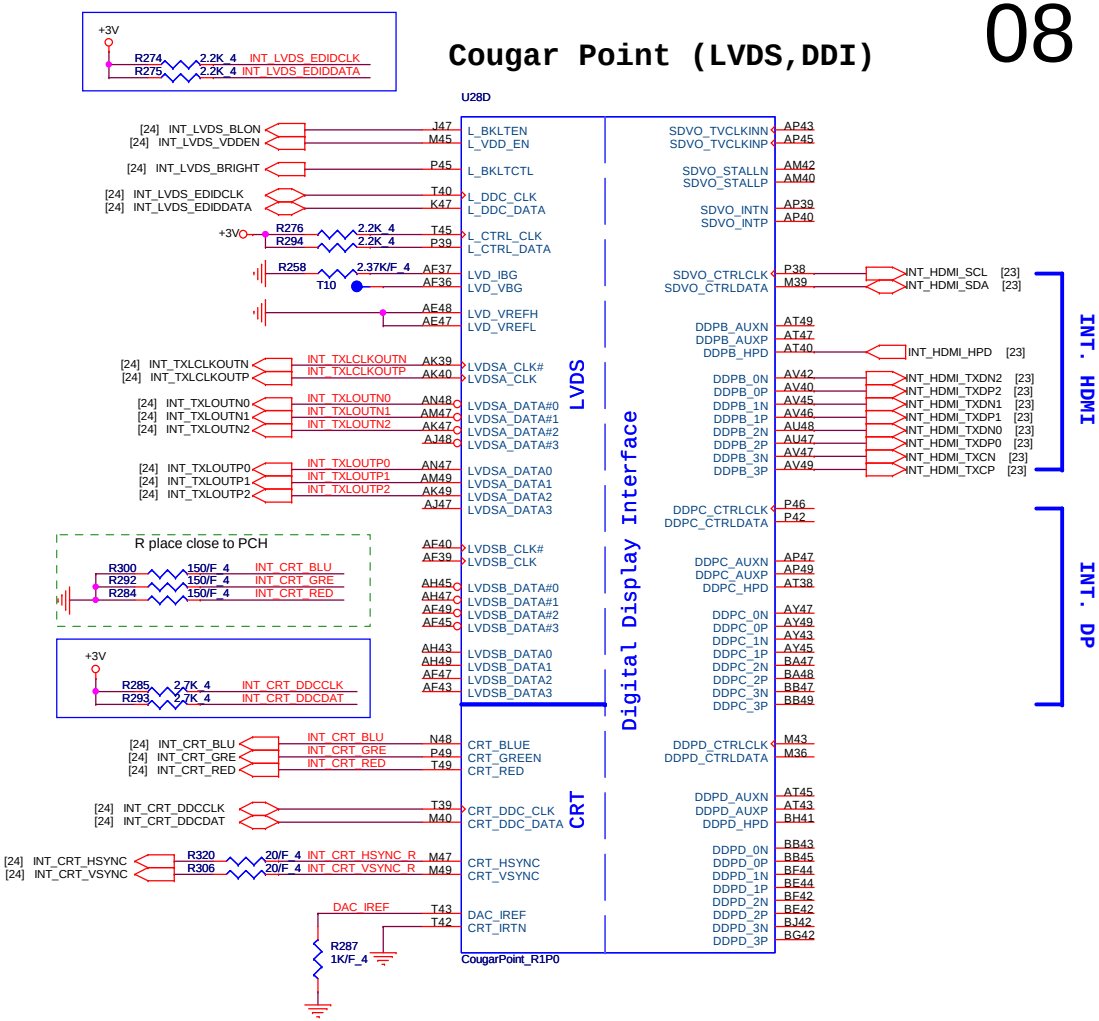
Quanta Computer Inc.
PROJECT : ZRJ

Size	Document Number	Rev
	Sandy Bridge 4/4	1A
Date: Monday, December 20, 2010	Sheet 7 of 41	

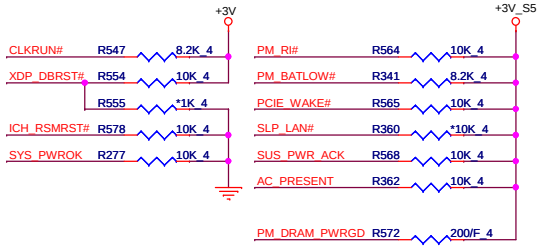
Cougar Point (DMI,FDI,PM)



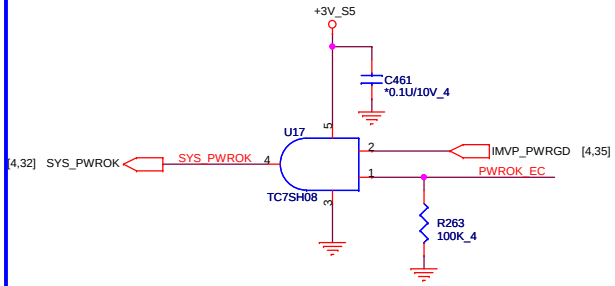
Cougar Point (LVDS,DDI)

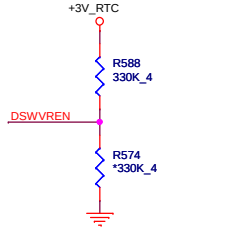


PCH Pull-high/low(CLG)



System PWR_OK(CLG)



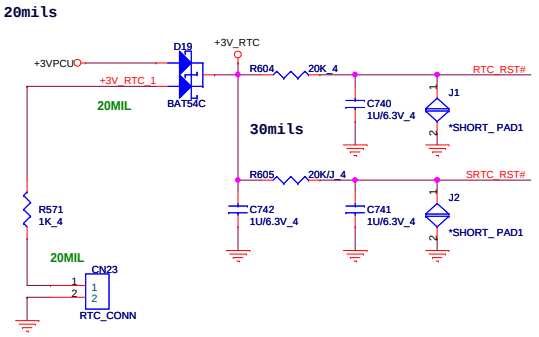


On Die DSW VR Enable
High = Enable (Default)
Low = Disable

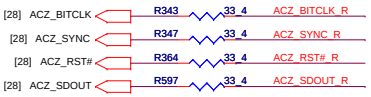
Quanta Computer Inc.
PROJECT : ZRJ

Size	Document Number	Rev
	Cougar Point 1/6	1A
Date: Saturday, January 22, 2011	Sheet 8 of 41	

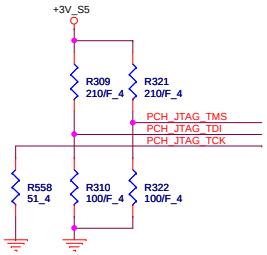
RTC Circuitry(RTC)



HDA Bus(CLG)

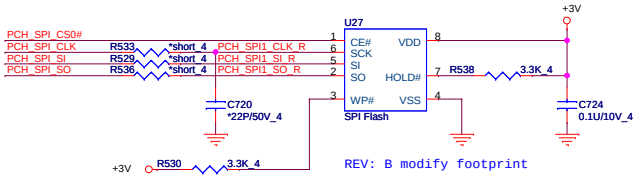


PCH JTAG Debug (CLG)



PCH Dual SPI (CLG)

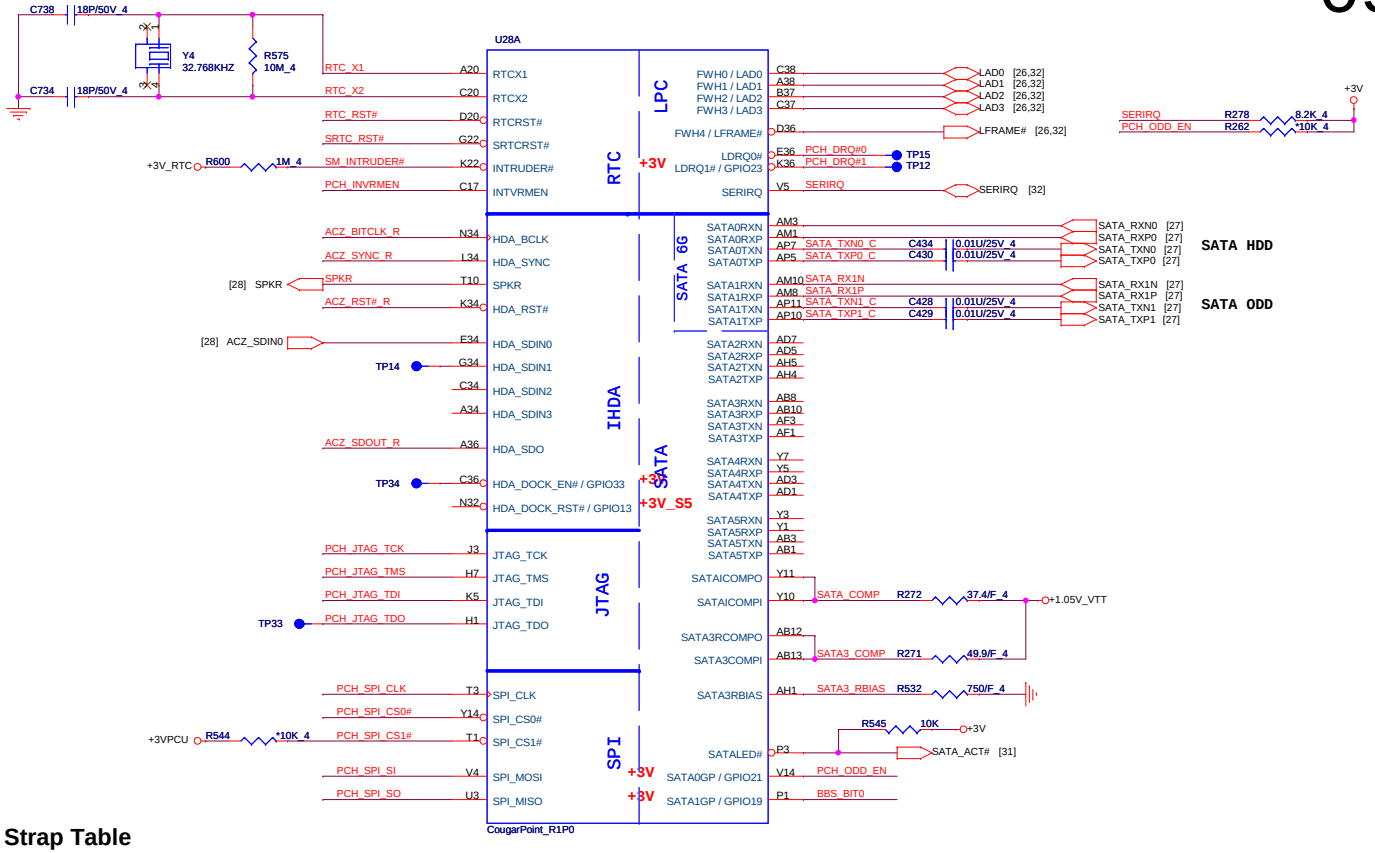
MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00



PCH2(CLG)

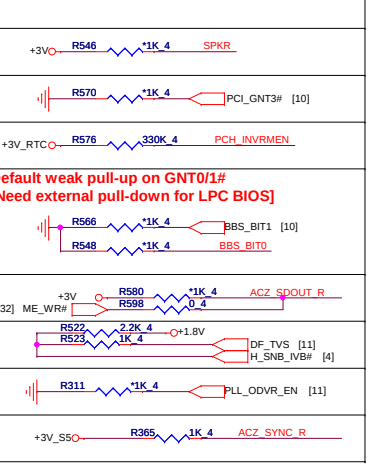
Cougar Point (HDA,JTAG,SATA)

09



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI *; 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)

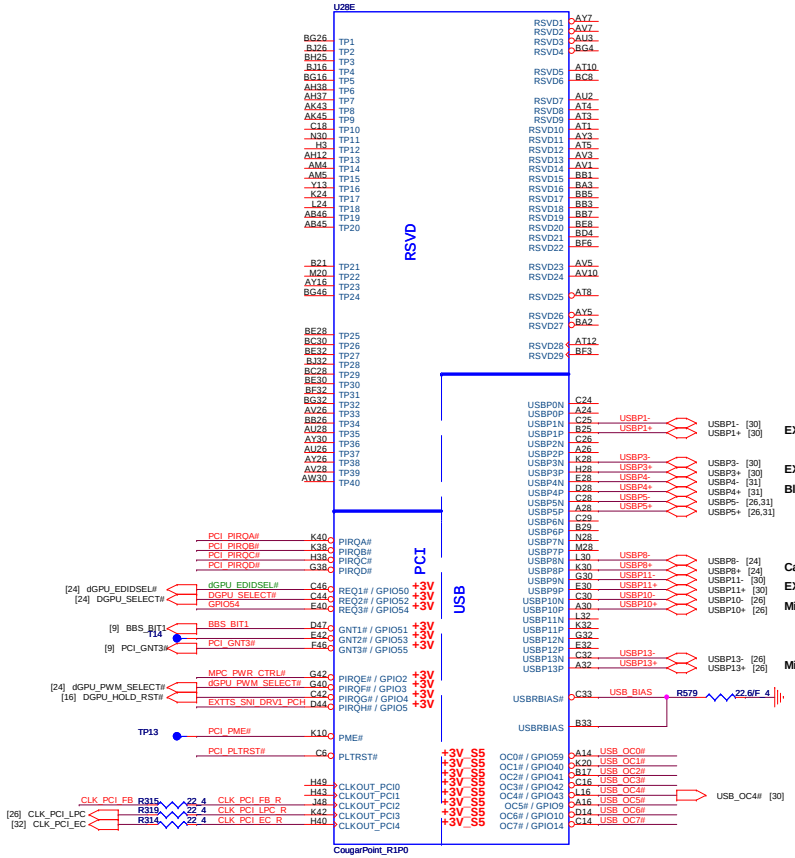


Quanta Computer Inc.
PROJECT : ZRJ

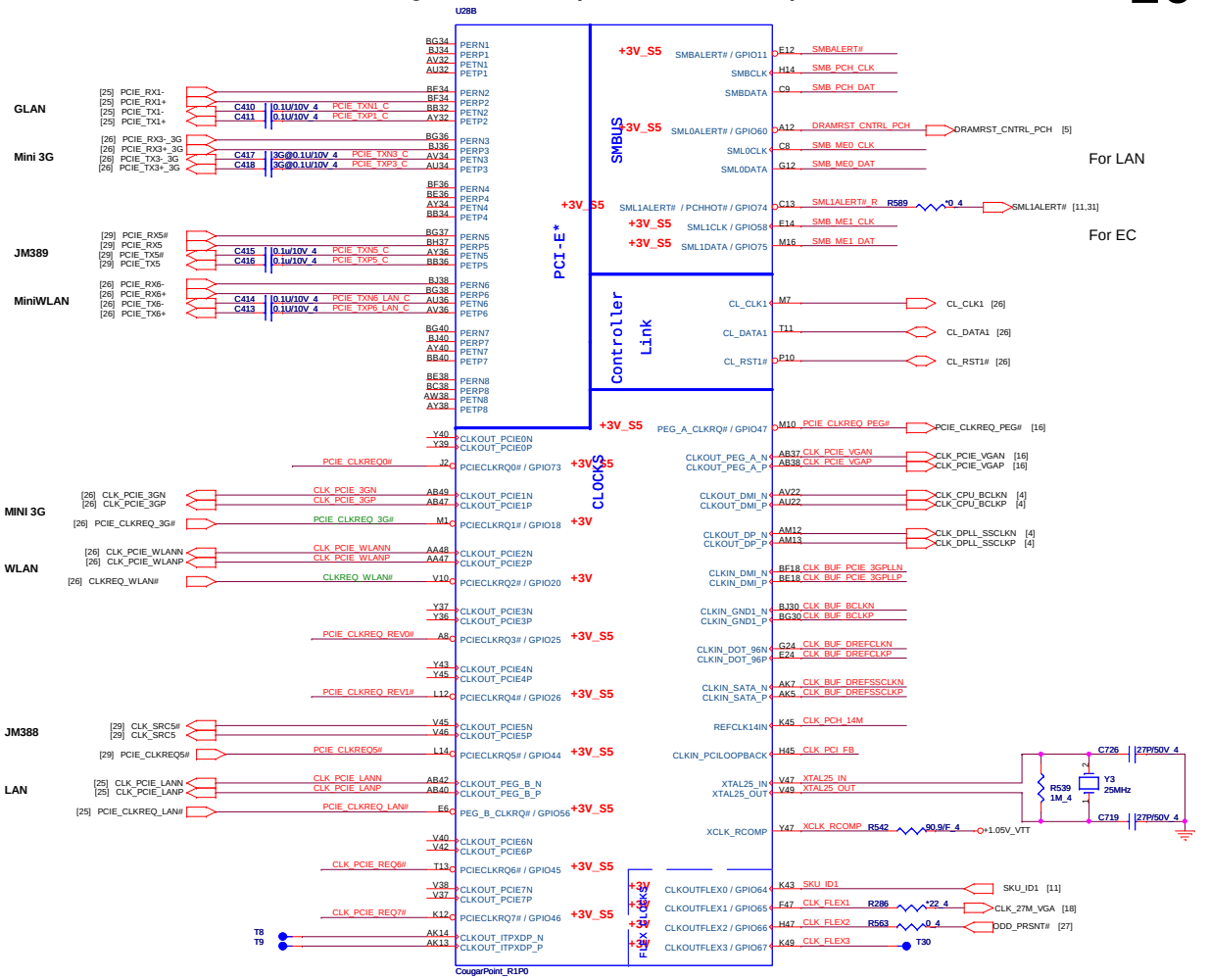
Size	Document Number	Rev
	Cougar Point 2/6	1A

Date: Saturday, January 22, 2011 Sheet 9 of 41

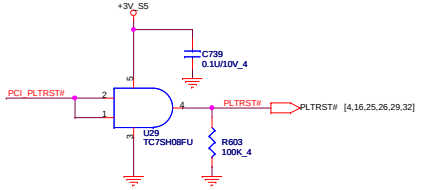
Cougar Point-M (PCI,USB,NVRAM)



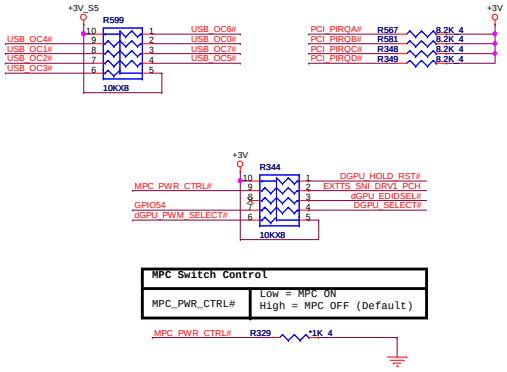
Cougar Point-M (PCI-E,SMBUS,CLK)



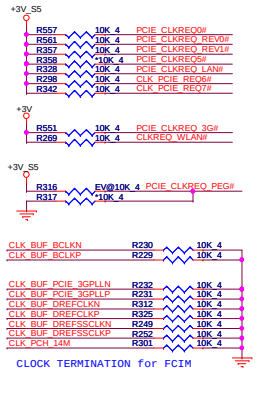
PLTRST#(CLG)



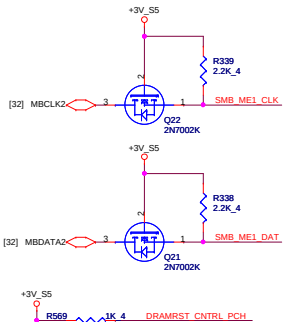
PCI/USBOC# Pull-up(CLG)



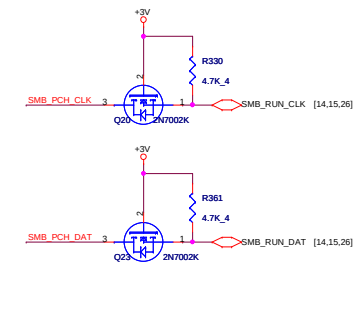
CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)



SMBus(PCH)



Cougar Point (GPIO,VSS_NCTF,RSVD)

U28F

GPIO

S_GPIO	R283 100_4	T7	BMBUSY# / GPIO0	+3V	+3V	TACH4 / GPIO68	C40 DGPU_PRSNT#
[32] EC_EXT_SMI#	EC_EXT_SMI#	A42	TACH1 / GPIO1	+3V	+3V	TACH5 / GPIO69	B41 R583 1.5K/F_4
	BOARD_ID1	H36	TACH2 / GPIO6	+3V	+3V	TACH6 / GPIO70	C41 R593 1.5K/F_4 +3V
[32] EC_EXT_SCI#	EC_EXT_SCI#	E38	TACH3 / GPIO7	+3V	+3V	TACH7 / GPIO71	A40 R592 1.5K/F_4
TP16		C10	GPIO8	+3V_S5			
	SMIB#	C4	LAN_PHY_PWR_CTRL / GPIO12		+3V_S5		
	PCH_GPIO15	G2	GPIO15	+3V_S5			
check VR_ON GPIO	SKU_ID0	U2	SATA4GP / GPIO16	+3V			
[16,32] dGPU_PWROK	dGPU_PWROK	D40	TACH0 / GPIO17	+3V			
	BIOS_REC	T5	SCLOCK / GPIO22	+3V			
	CR_WAKER#	E8	GPIO24 / MEM_LED	+3V_S5			
	GPIO27	E16	GPIO27	DSW			
[9] PLL_ODVR_EN	R308 *short_4 PLL_ODVR_EN_R	P8	GPIO28	+3V_S5			
Need Check	STP_PCI#	K1	STP_PCI# / GPIO34	+3V			
[32,38,40] dGPU_VRON		K4	GPIO35	+3V			
[40] DGPU_PWR_EN	DGPU_PWR_EN R280 0_4 DMI_OVRVLTG	V8	SATA2GP / GPIO36	+3V			
	FDI_OVRVLTG	M5	SATA3GP / GPIO37	+3V			
	MFG_MODE	N2	SLOAD / GPIO38	+3V			
	BOARD_ID0	M3	SDATAOUT0 / GPIO39	+3V			
	TEST_SET_UP	V13	SDATAOUT1 / GPIO48	+3V			
[10,31] SML1ALERT#	R534 0_4 CRIT_TEMP_REP#	V3	SATA5GP / GPIO49	+3V			
	SV_DET	D6	GPIO57	+3V_S5			

CPU/MISC

A20GATE	P4	EC_A20GATE [32]	
PECI	AU16	R188 *0_4	EC_PECI [4,32]
RCIN#	P5	EC_RCIN	EC_RCIN# [32]
PROCPWRGD	AY11		H_PWRGOOD [4,32]
THRMTRIP#	AY10	PCH_THRMTRIP# R245 390_4	PM_THRMTRIP# [4]
INIT3_3V#	T14		
DF_TVS	AY1		DF_TVS [9]
TS_VSS1	AH8		
TS_VSS2	AK11		
TS_VSS3	AH10		
TS_VSS4	AK10		
NC_1	P37		

NCTF

A4	VSS_NCTF_1	VSS_NCTF_15	BG2
A44	VSS_NCTF_2	VSS_NCTF_16	BG48
A45	VSS_NCTF_3	VSS_NCTF_17	BH3
A46	VSS_NCTF_4	VSS_NCTF_18	BH47
A5	VSS_NCTF_5	VSS_NCTF_19	BJ4
A6	VSS_NCTF_6	VSS_NCTF_20	BJ44
B3	VSS_NCTF_7	VSS_NCTF_21	BJ45
B47	VSS_NCTF_8	VSS_NCTF_22	BJ46
BD1	VSS_NCTF_9	VSS_NCTF_23	BJ5
BD49	VSS_NCTF_10	VSS_NCTF_24	BJ6
BE1	VSS_NCTF_11	VSS_NCTF_25	C2
BE49	VSS_NCTF_12	VSS_NCTF_26	C48
BF1	VSS_NCTF_13	VSS_NCTF_27	D1
BF49	VSS_NCTF_14	VSS_NCTF_28	D49
		VSS_NCTF_29	E1
		VSS_NCTF_30	E49
		VSS_NCTF_31	F1
		VSS_NCTF_32	F49

CougarPoint_R1P0

	DGPU_PRSNT# (GPIO68)	SKU_ID1 (GPIO64)	SKU_ID0 (GPIO16)	VGA H/W Signal	Setup Menu	
UMA Only	1	0	0	UMA	Hidden	UMA boot
Discrete Only	0 or 1	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	0	1	0	UMA+GPU	DIS/SG	UMA boot
Optimize (Muxless)	0	1	1	UMA	UMA/SG	UMA boot

0 = GPU power is control by PCH GPIO (Discrete, SG or Optimize)
1 = GPU power is control by H/W (pure Discrete SKU)

+3V
R591 IV@10K_4 DGPU_PRSNT#
R582 EV@100K_4

+3V
R594 EV@10K_4 SKU_ID1 [10]
R585 IV@10K_4

+3V
R543 *10K_4 SKU_ID0
R541 10K_4

+3V
R553 10K_4 BOARD_ID0 R552 *10K_4
R590 10K_4 BOARD_ID1 R601 *10K_4

+3V_S5
R327 *10K_4 SV_DET R331 100K_4

SV_SET_UP
High = Strong (Default)

+3V
TEST_SET_UP R265 10K_4
R270 *0_4

+3V_S5
PCH_GPIO15 R559 1K_4

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

SGPIO

+3V
S_GPIO R289 1K/F_4
R282 *0_4

MFG-TEST

+3V
MFG_MODE R549 10K_4
R550 *0_4

GPIO Pull-up/Pull-down(CLG)

+3V_S5
CR_WAKER# R332 10K_4
SMIB# R560 10K_4
PLL_ODVR_EN R296 *10K_4

+3V
EC_EXT_SMI# R584 10K_4
EC_EXT_SCI# R351 10K_4
STP_PCI# R556 *10K_4
EC_A20GATE R299 10K_4
EC_RCIN# R297 10K_4
CRIT_TEMP_REP# R535 10K_4

GPIO27 R353 *10K_4
dGPU_PWROK R354 *10K_4

+3V
FDI_OVRVLTG R318 *10K/F_4

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

+3V
DMI_OVRVLTG R279 *200K/F_4

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

+3V
BIOS_REC R290 10K_4
R291 *0_4

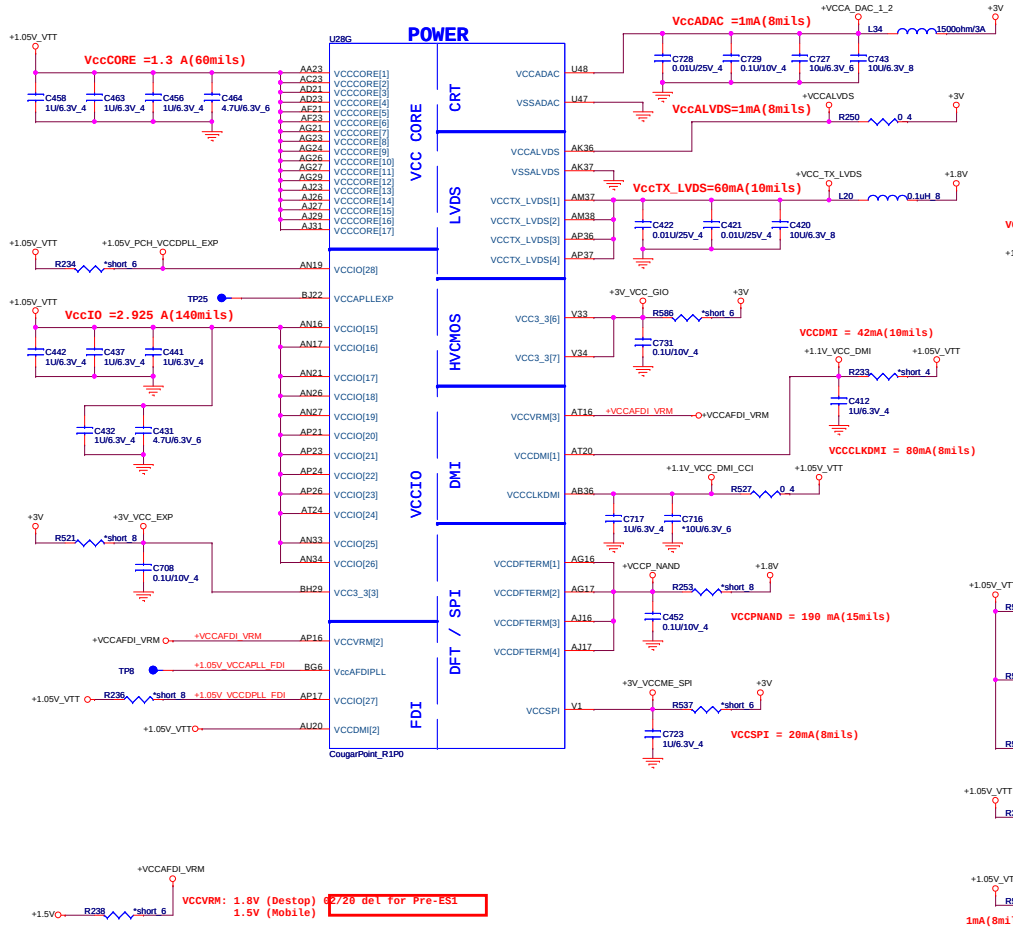
BIOS RECOVERY	High = Disable (Default) Low = Enable

Quanta Computer Inc.
PROJECT : ZRJ

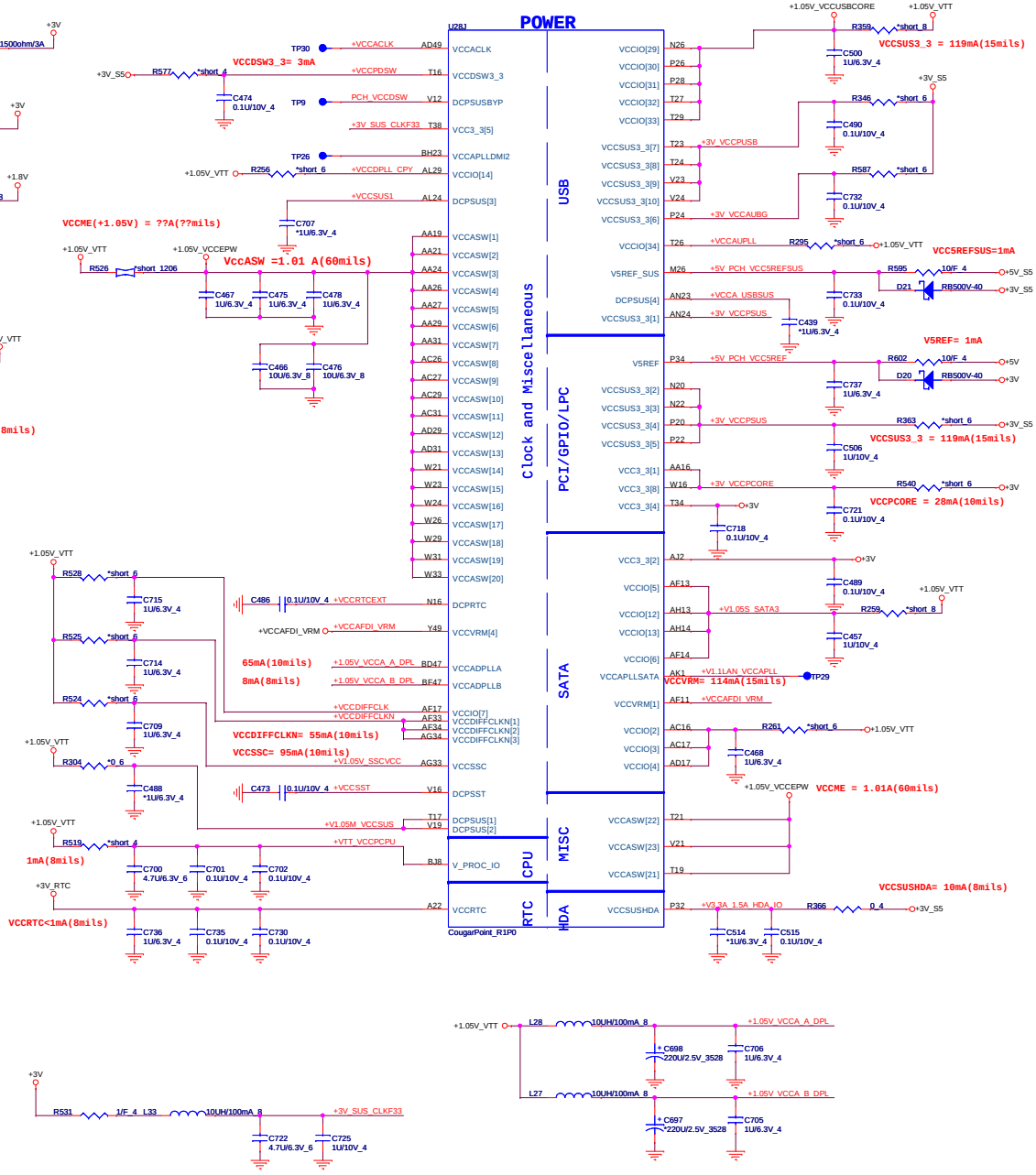
Size	Document Number	Rev
	Cougar Point 4/6	1A

Date: Saturday, January 22, 2011 Sheet 11 of 41

COUGAR POINT (POWER)



Cougar Point-M (POWER)



Quanta Computer Inc.

PROJECT : ZRJ

Size	Document Number	Rev
	Cougar Point 5/6	1A

Date: Saturday, January 22, 2011 Sheet 12 of 41

PCH6(CLG)

IBEX PEAK-M (GND)

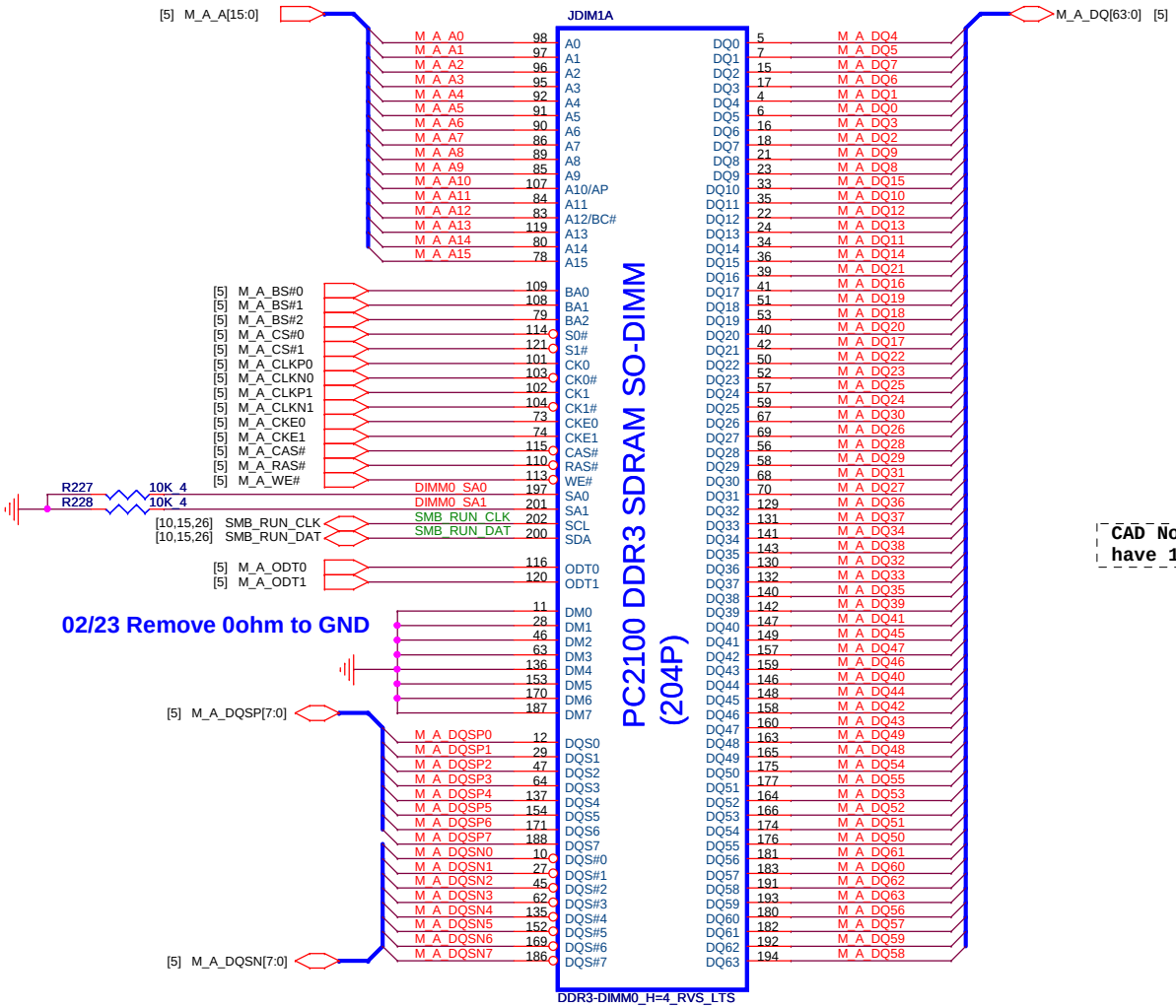
13

Quanta Computer Inc.

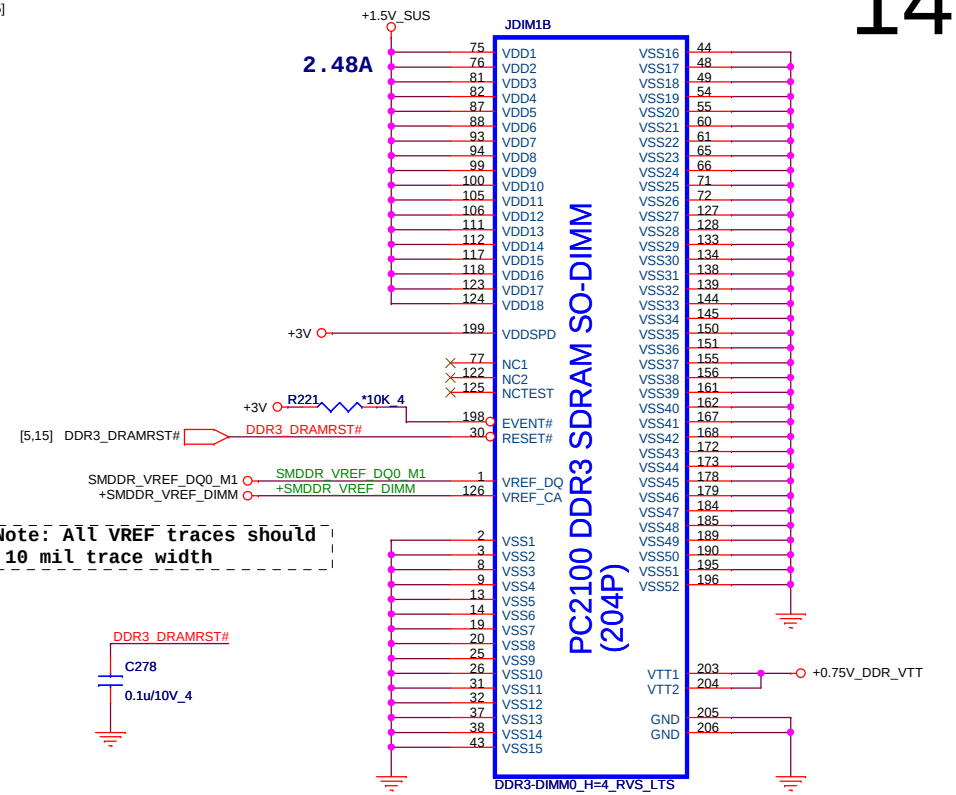
PROJECT : ZRJ

Size	Document Number	Rev
	Cougar Point 6/6	1A
Date: Monday, December 13, 2010	Sheet 13 of 41	

DDR_STD(DDR)

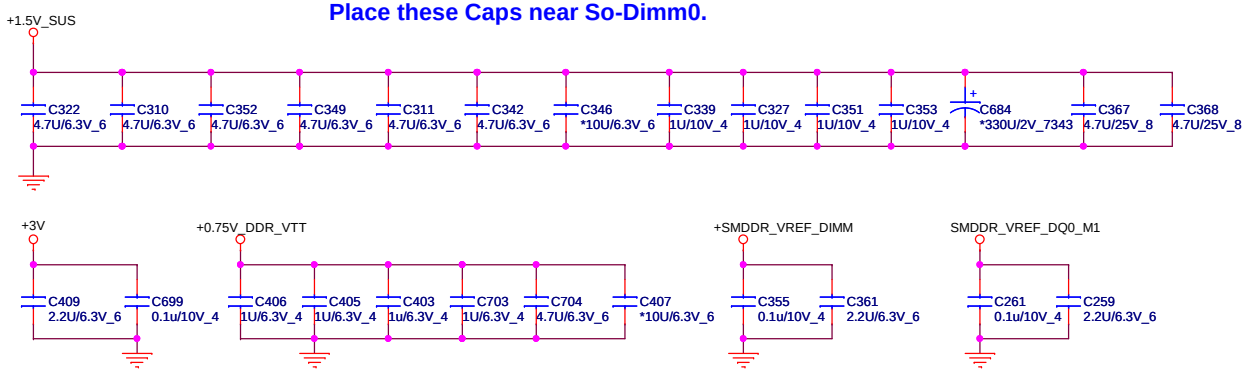


02/23 Remove 0ohm to GND

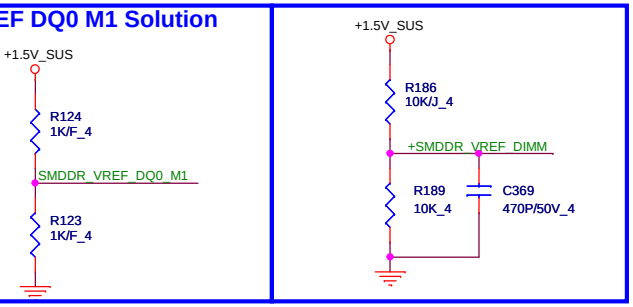


CAD Note: All VREF traces should have 10 mil trace width

Place these Caps near So-Dimm0.

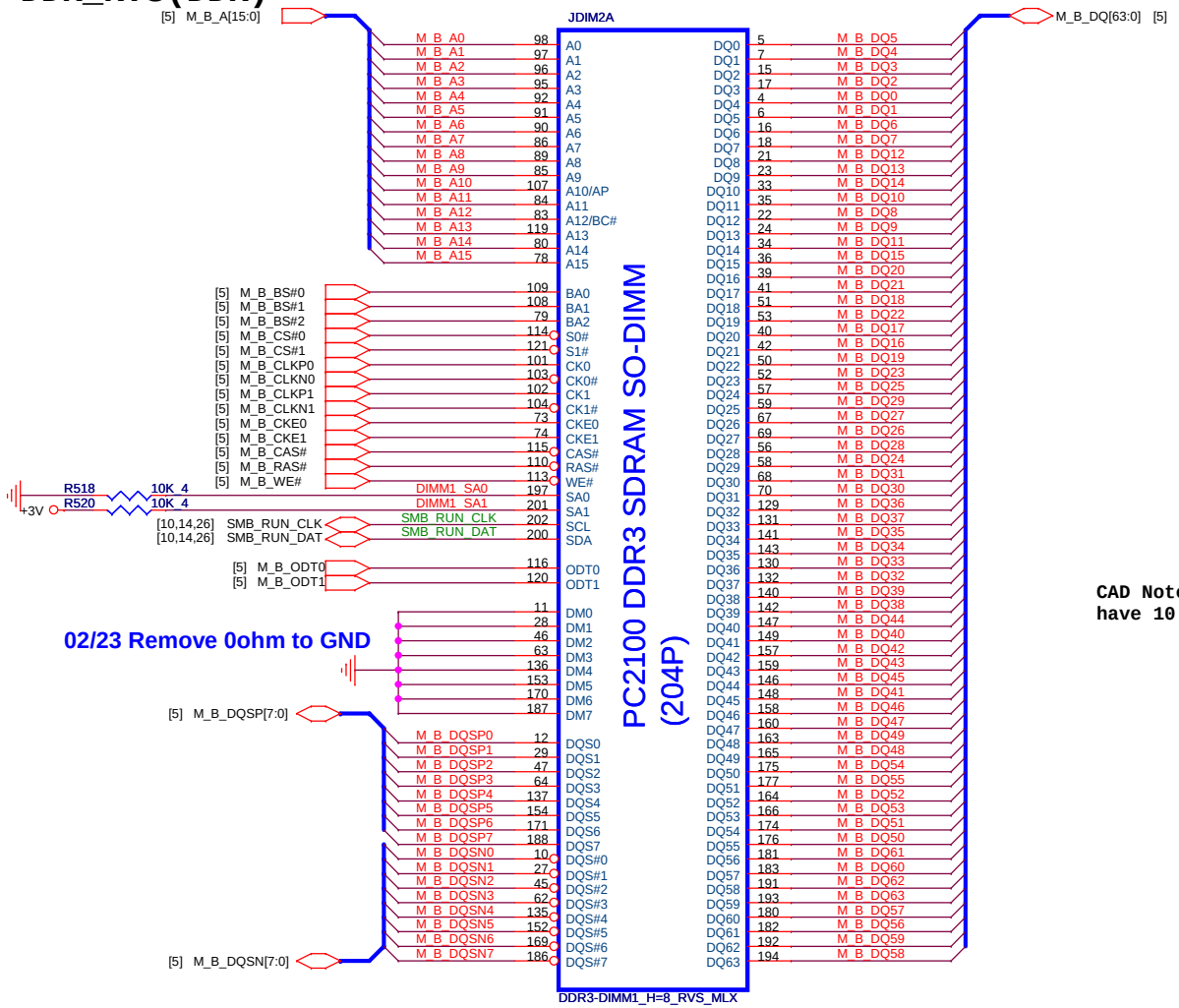


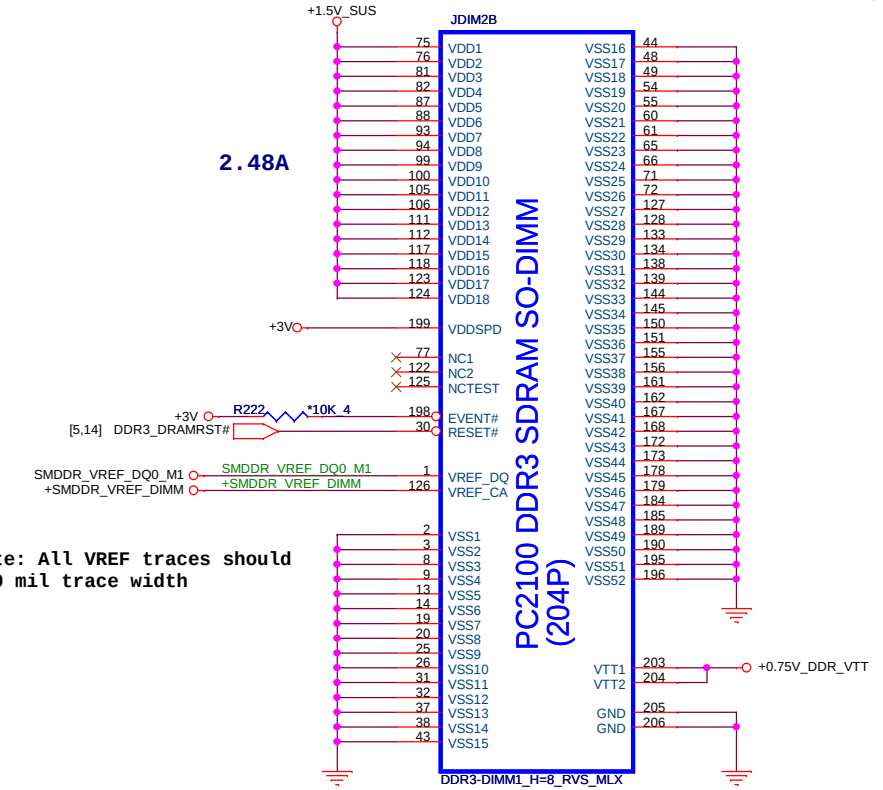
VREF DQ0 M1 Solution



Quanta Computer Inc.		
PROJECT : ZRJ		
Size	Document Number: DDRIII SO-DIMM-0	Rev: 1A
Date: Saturday, January 22, 2011	Sheet 14 of 41	

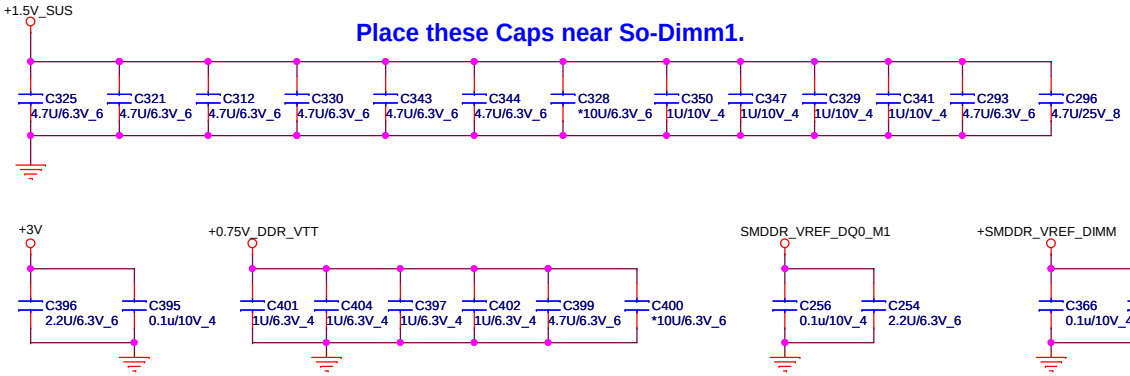
DDR_RVS(DDR)





CAD Note: All VREF traces should have 10 mil trace width

Place these Caps near So-Dimm1.



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080

Standard 8H type:DDR-C-2013310-204p-1

Quanta Computer Inc.
PROJECT :ZRJ

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A

Date: Saturday, January 22, 2011 Sheet 15 of 41

PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

2200mA

PLACE NEAR BALLS

PLACE NEAR BGA

285 mA

120mA

120-ohm / ESR=0.18

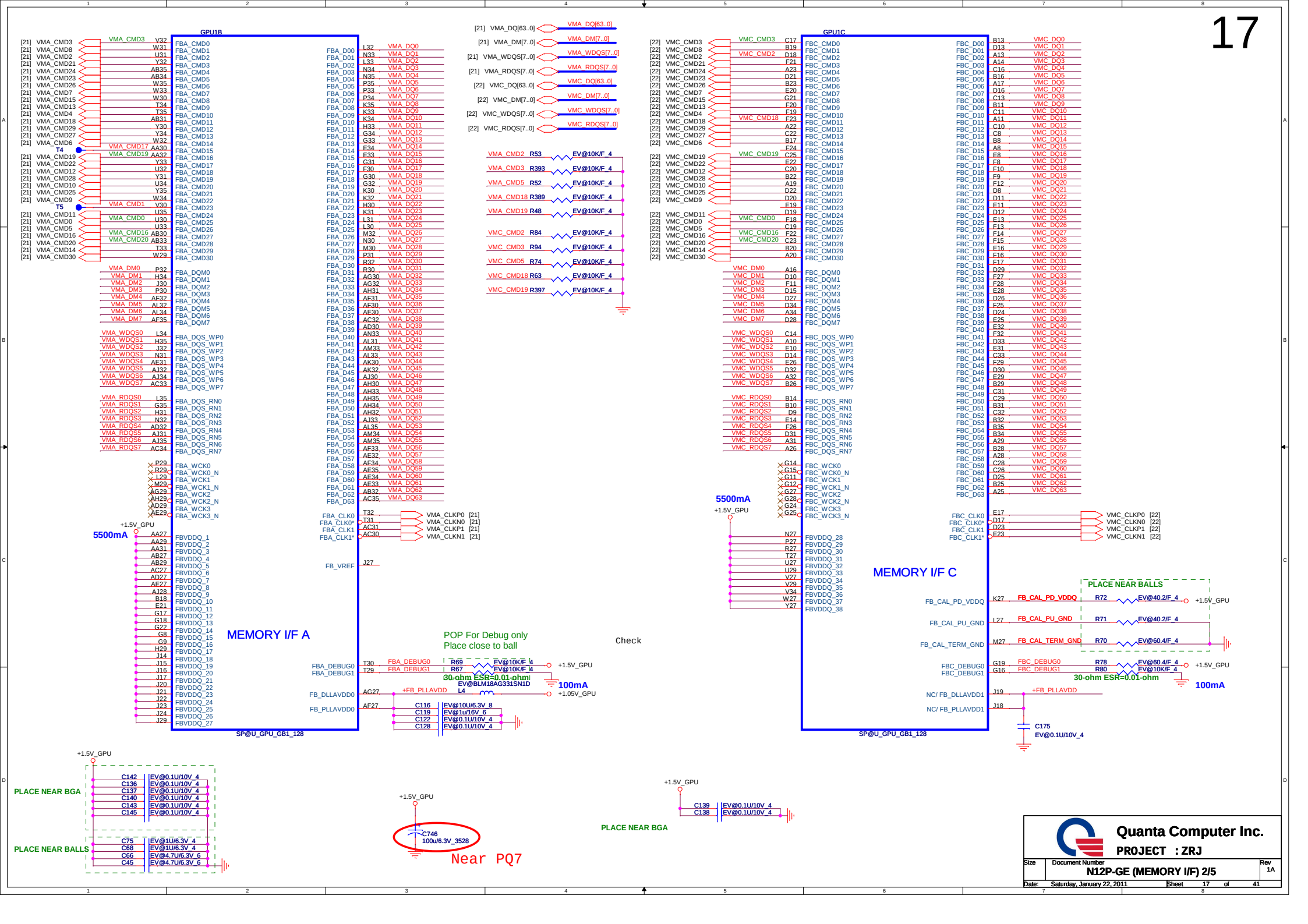
PCI EXPRESS

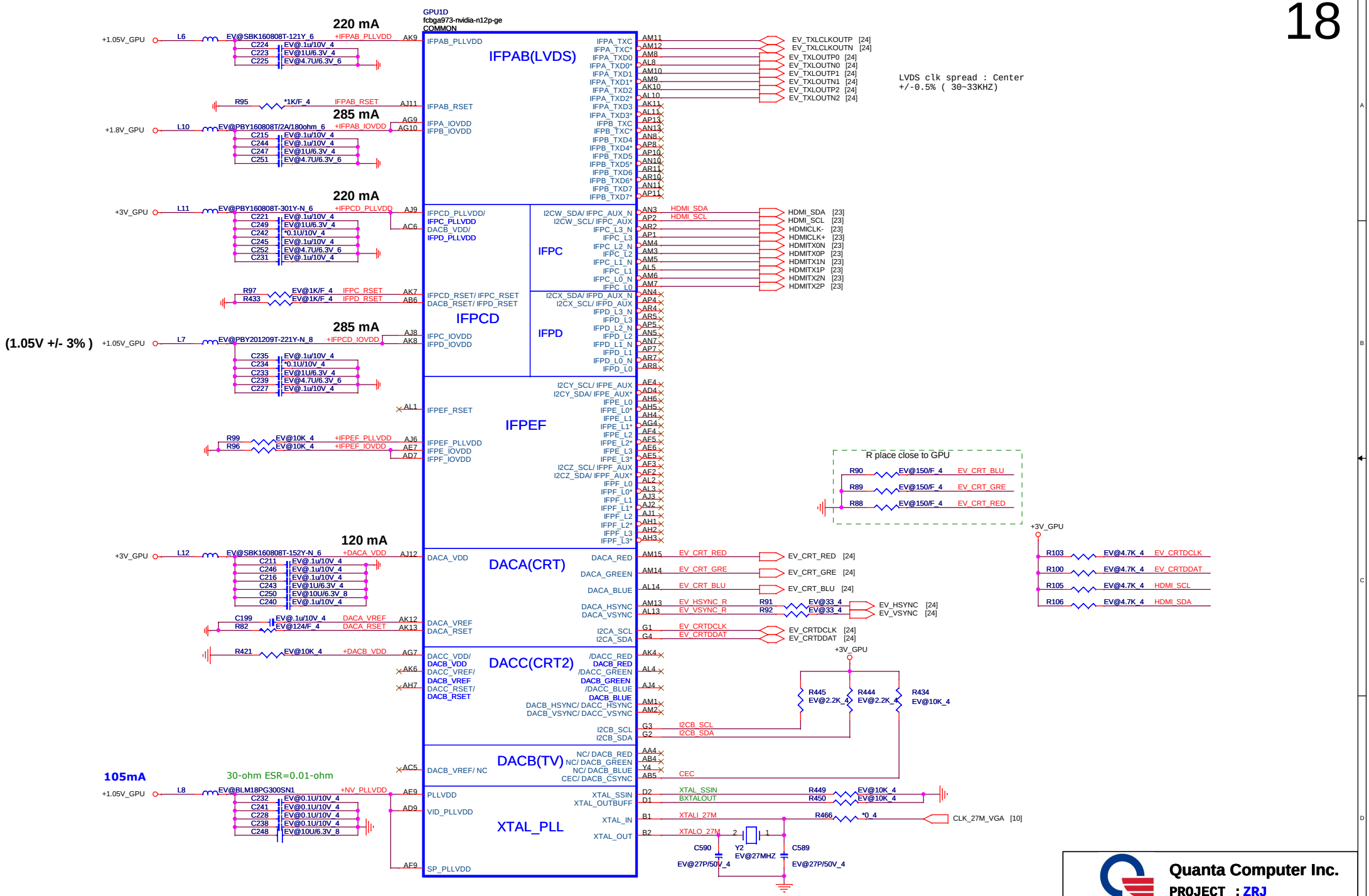
SP@U_GPU_GB1_128

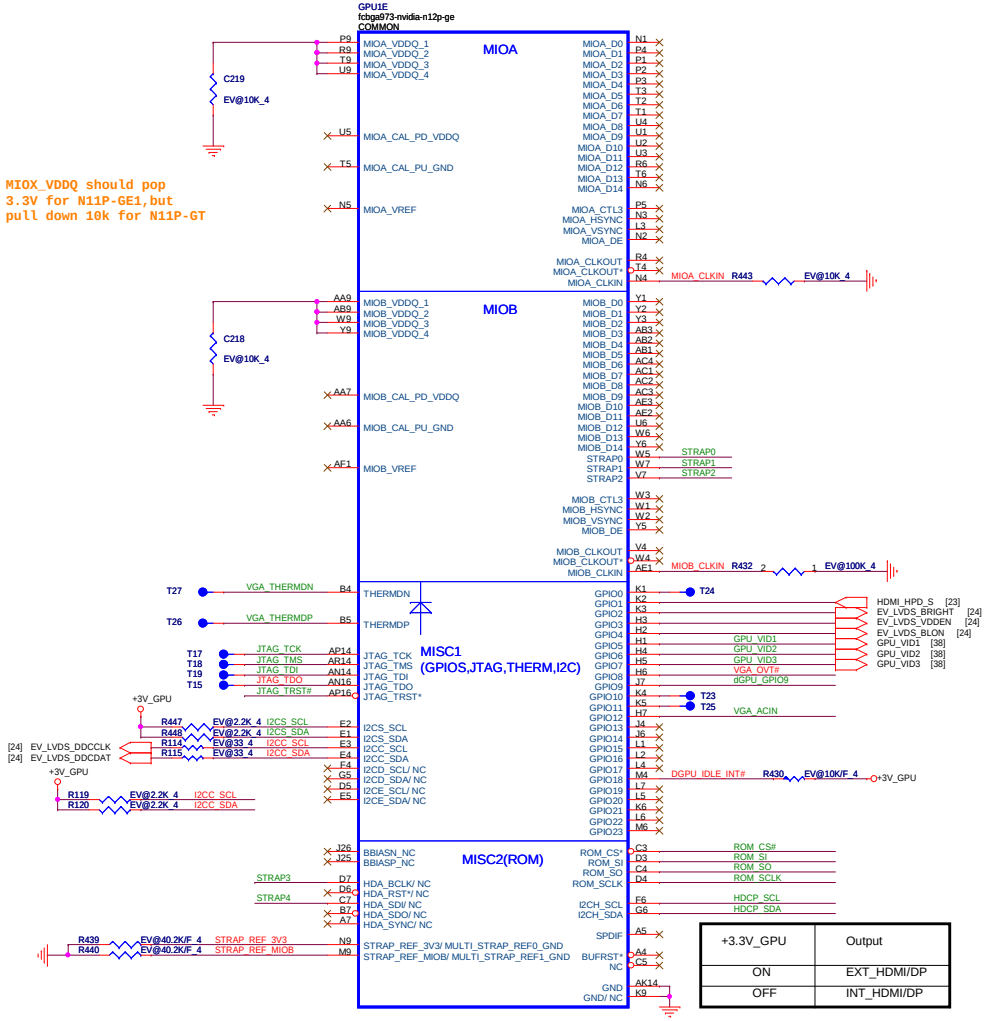
GPU RST#

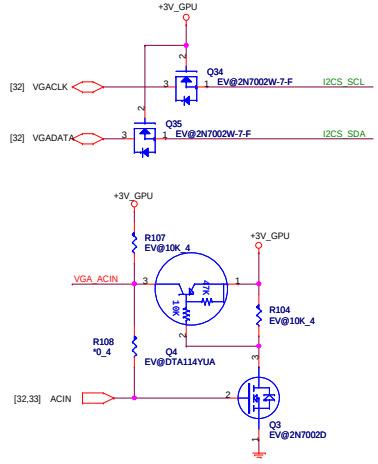
GPU all PWROK

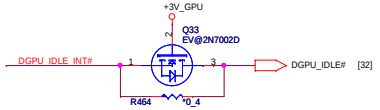
Quanta Computer Inc.
PROJECT : ZRJ
Size | Document Number: N12P-GE (PCIE I/F) 1/5 | Rev: 1A
Date: Saturday, January 22, 2011 | Sheet 16 of 41

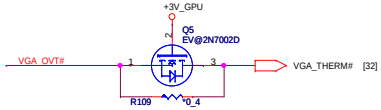

GPU1B
GPU1C
MEMORY I/F A
MEMORY I/F C
SP@U_GPU_GB1_128
5500mA
+1.5V_GPU
POP For Debug only
Place close to ball
30-ohm ESR=0.01-ohm
EV@BLM18AG331SN1D
100mA
+1.05V_GPU
Check
PLACE NEAR BGA
PLACE NEAR BALLS
Near PQ7
Quanta Computer Inc.
PROJECT : ZRJ
N12P-GE (MEMORY I/F) 2/5
Size
Document Number
Rev
1A
Date: Saturday, January 22, 2011
Sheet 17 of 41


GPU1D
fcbga973-nvidia-n12p-ge
COMMON
IFPAB(LVDS)
IFPCD
IFPC
IFPD
IFPEF
DACA(CRT)
DACC(CRT2)
DACB(TV)
XTAL_PLL
220 mA
285 mA
220 mA
285 mA
120 mA
105mA
(1.05V +/- 3%)
30-ohm ESR=0.01-ohm
LVDS clk spread : Center
+/-0.5% (30~33KHZ)
R place close to GPU
Quanta Computer Inc.
PROJECT : ZRJ
N12P-GE (DISPLAY) 3/5
Saturday, January 22, 2011









	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	N12P-GS	N12P-GV
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001	1001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	1010	1000
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	xxxx	xxxx
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0100	0000
STRAP3	SOR_EXPOSED[3]	SOR_EXPOSED[2]	SOR_EXPOSED[1]	SOR_EXPOSED[0]	TBD	xxxx
STRAP4	Reserve	Reserve	PCI_MAX_SPEED	DP_PLL_VDD3	TBD	0001

	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

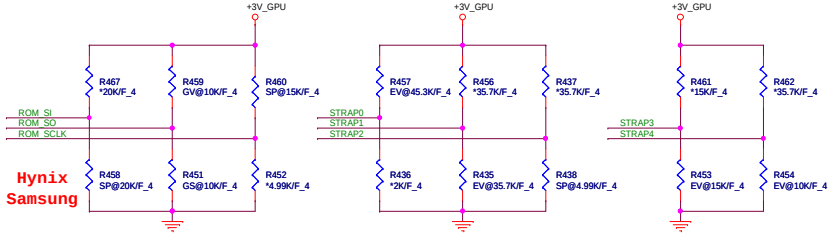
VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN
★ 0x3(0011)	900MHz 512MB(64M*16) Samsung	AKD5LGHT500		K4W1G1646E-HC11
0x2(0010)	900MHz 512MB(64M*16) Hynix	AKD5LZWTW01	AKD5LZWTW00	H5TQ1G63BFR-11C
0x6(0110)	800MHz 1GB(128M*16) Hynix	AKD5MGGTW00	AKD5MGGTW01	H5TQ2G63BFR-12C
0x7(0111)	800MHz 1GB(128M*16) Samsung	AKD5MGGT501	AKD5MGGT502	K4W2G1646B-HC12

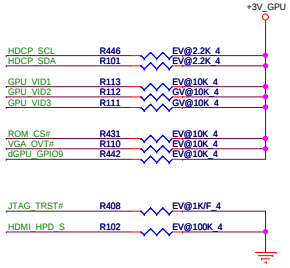
```
4.99K/F_4 ==> CS24992FB26
10K/F_4 ==> CS31002FB26
15K/F_4 ==> CS31502FB24
20K/F_4 ==> CS32002FB29
30.1K/F_4 ==> CS33012FB18
35.7K/F_4 ==> CS33572FB13
45.3K/F_4 ==> CS34532FB18
```

	Register value
ROM_SO	N12P-GS 10k pull down; N12P-GV 10K pull up.
ROM_SCLK	N12P-GS need 15K pull up; N12P-GV need 5K pull up
ROM_SI	1G: Hynix =15K pull down ,Samsung =20k pull down 2G: Hynix =35K pull down ,Samsung =45k pull down
STRAP0	N12P-GS and N12P-GV both 45K pull high
STRAP1	N12P-GS and N12P-GV both 35k pull down
STRAP2	N12P-GS need 25K pull down; N12P-GV need 5K pull down
STRAP3	STRAP3 need 15K pull down by R3513.
STRAP4	STRAP4 need 10K pull down by R3519.

ROM_SI Strap Bit for RAM Mapping

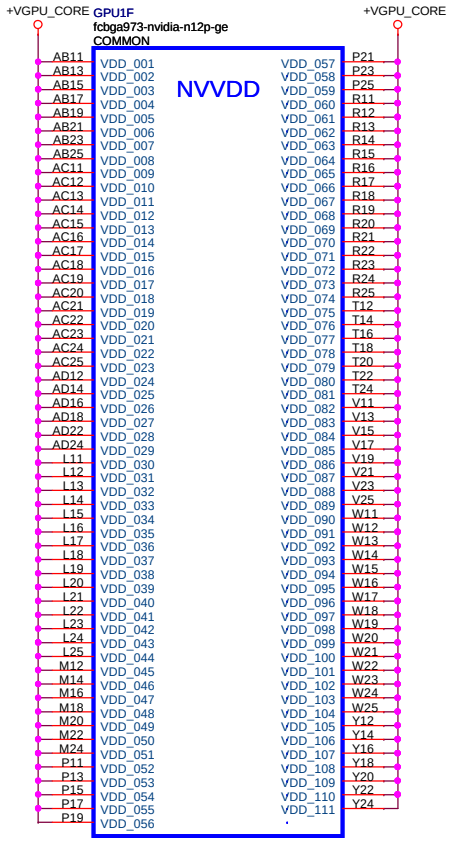


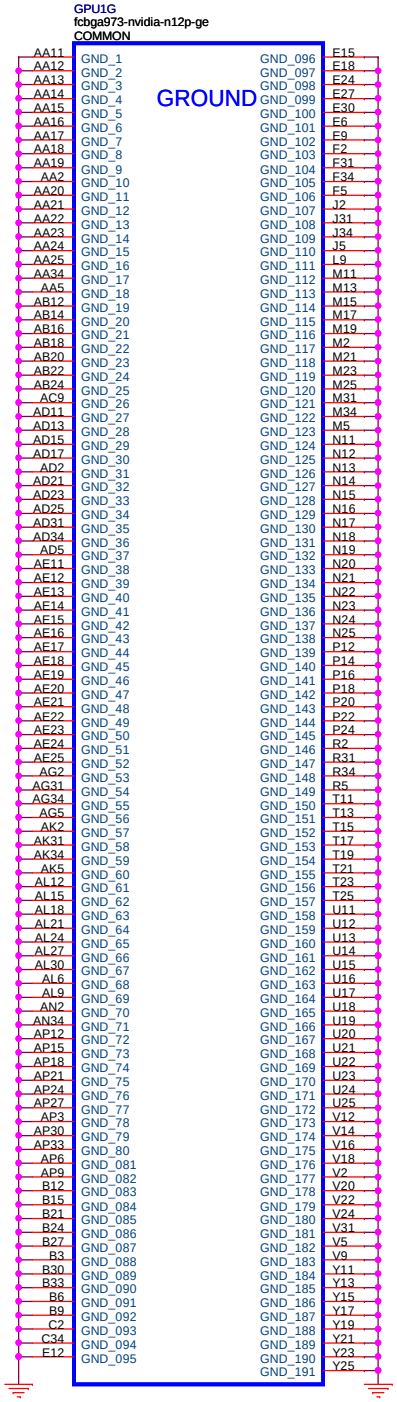
N11P-GE1 DevID is 0x0DFE, so pull up
ROM_SCLK with 15Kohm and STRAP2
pull up 35Kohm

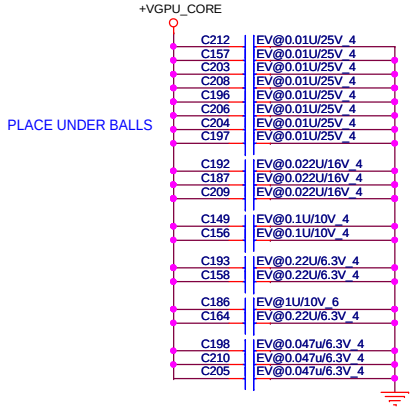


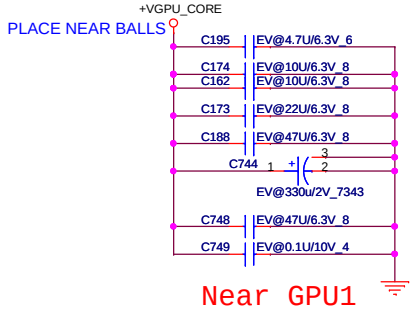
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	N/A	
3	OUT	N/A	
4	OUT	N/A	
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL









Quanta Computer Inc.		
PROJECT : ZRJ		
Size	Document Number: N12P-GE(POWER&THM)5/5	Rev: 1A
Date: Saturday, January 22, 2011	Sheet 20 of 41	

CHANNEL A: 512MB/1024MB DDR3

[17] VMA_DQ[63..0]
[17] VMA_DM[7..0]
[17] VMA_WDQS[7..0]
[17] VMA_RDQS[7..0]

VRAM2 / VRAM6 / VRAM1 / VRAM5

96-BALL SDRAM DDR3
SP@K4W1G1646E-HC11

Should be 240 Ohms +-1%

R62 EV@240/F_4
R392 EV@240/F_4
R49 EV@240/F_4
R394 EV@240/F_4

+1.5V_GPU

R390 EV@1.33K/F_4
R391 EV@1.33K/F_4
C537 EV@0.01U/25V_4
R55 EV@1.33K/F_4
R54 EV@1.33K/F_4
C59 EV@0.01U/25V_4
C565 *10U/6.3V_6
R51 EV@1.33K/F_4
R50 EV@1.33K/F_4
C53 EV@0.01U/25V_4
R387 EV@1.33K/F_4
R388 EV@1.33K/F_4
C530 EV@0.01U/25V_4

VREFC_VMA1
VREFD_VMA1
VREFC_VMA3
VREFD_VMA3

Placement has to be close to VRAM

R57 EV@162/F_4
R56 EV@162/F_4

VMA_CLKP0
VMA_CLKN0
VMA_CLKP1
VMA_CLKN1

C536 C548 C535 C547 C527 C528 C529 C52 EV@1U/6.3V_4
C531 C532 C533 C534 EV@0.1U/10V_4
C80 C71 C79 C97 C549 C98 C54 EV@1U/6.3V_4
C55 C49 C50 C51 EV@0.1U/10V_4
C550 C552 C551 C553 C554 C541 C540 EV@1U/6.3V_4
C539 C538 C542 C543 EV@0.1U/10V_4
C101 C100 C99 C102 C47 C48 C56 EV@1U/6.3V_4
C61 C60 C58 C57 EV@0.1U/10V_4

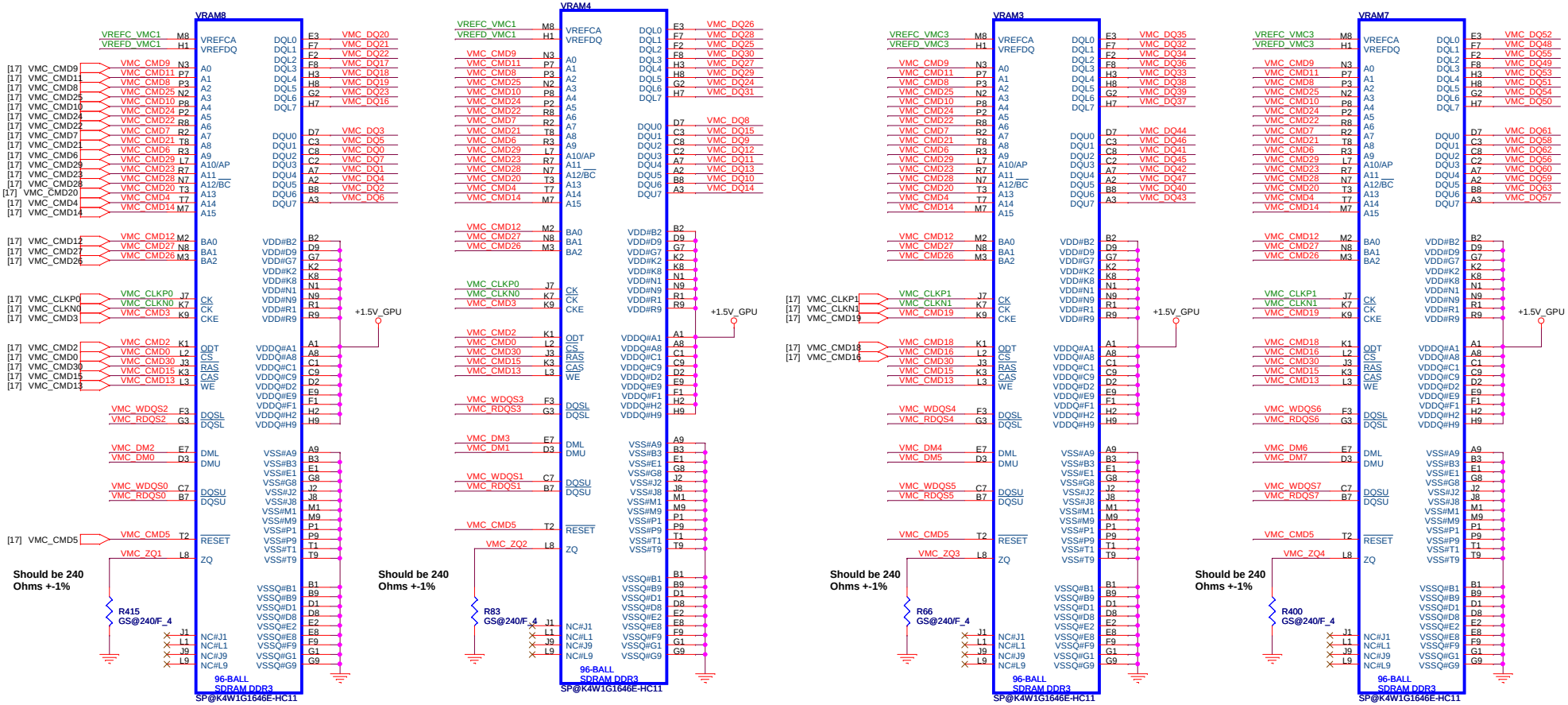
Quanta Computer Inc.
PROJECT : ZRJ

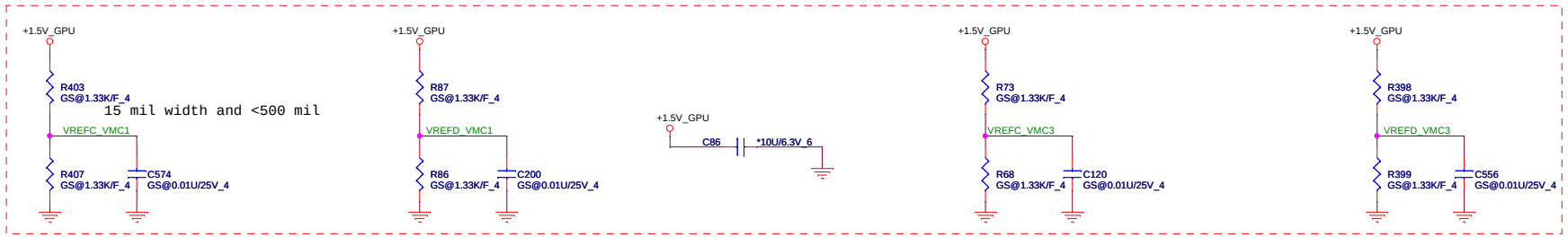
Size	Document Number	Rev
	N12P-GE VRAM-1	1A

Date: Saturday, January 22, 2011 Sheet 21 of 41

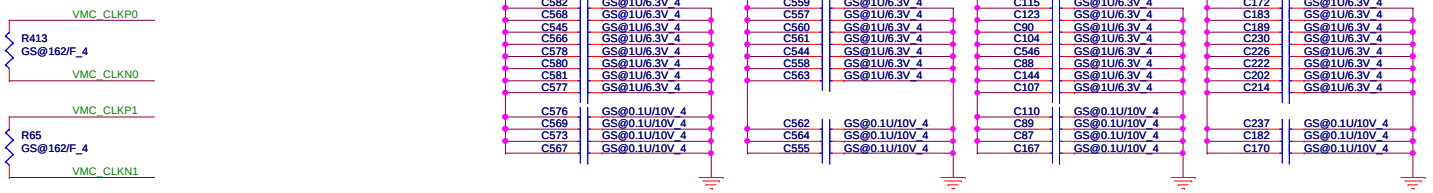
CHANNEL B: 512MB/1024MB DDR3

[17] VMC_DQ[63..0]
[17] VMC_DM[7..0]
[17] VMC_WDQS[7..0]
[17] VMC_RDQS[7..0]





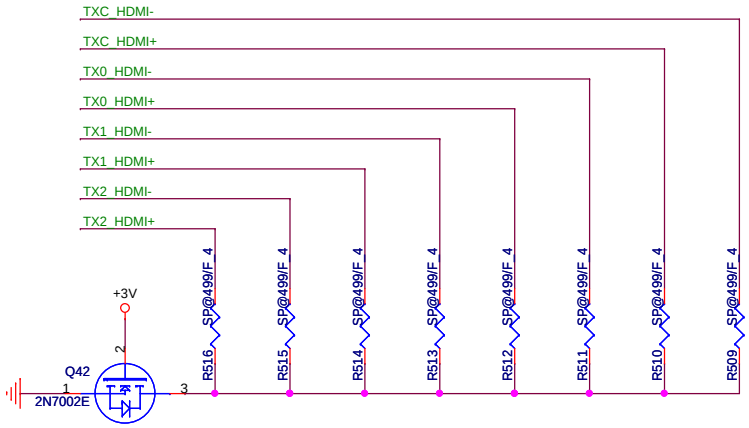
Placement has to be close to VRAM



Quanta Computer Inc.
PROJECT : ZRJ

Size	Document Number	Rev
	N12P-GE VRAM-2	1A

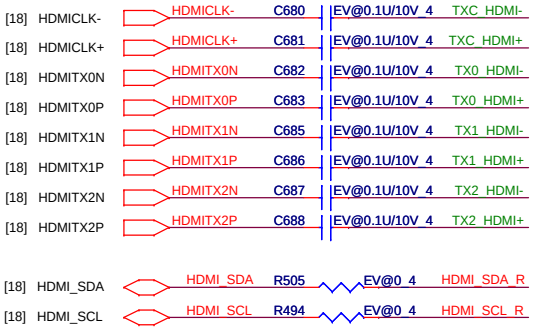
Date: Saturday, January 22, 2011 Sheet 22 of 41



	EV@	IV@
SP@	500 ohm	680 ohm

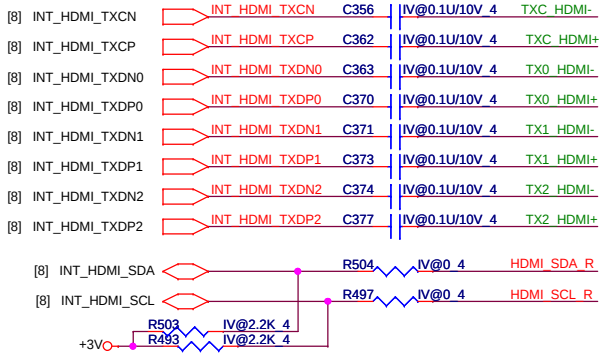
PLACE PULL DOWN RESISTORS CLOSE TO DIFFERENTIAL PAIRS CONNECTED TO SOLID GROUND FLOOD WHICH IS CONTROLLED BY THE FET
AVOID STUBS TO ALL DIFFERENTIAL TRACES

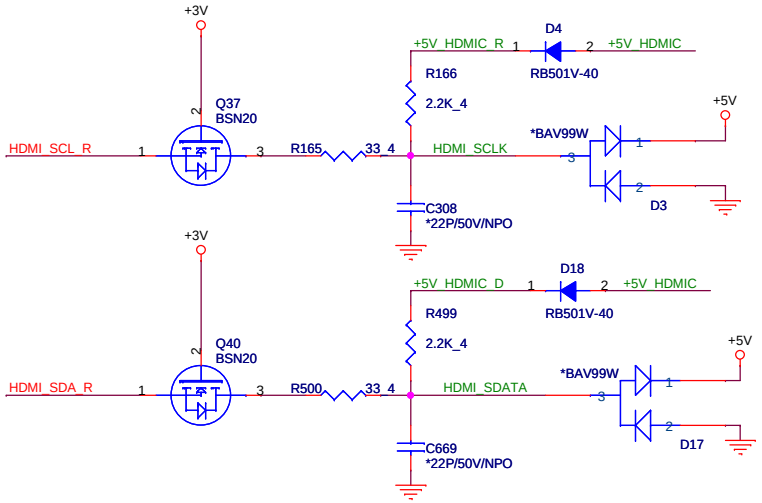
EXT-HDMI



INT-HDMI

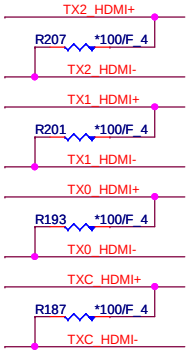
PLACE AC CAP CLOSE TO CONNECTOR



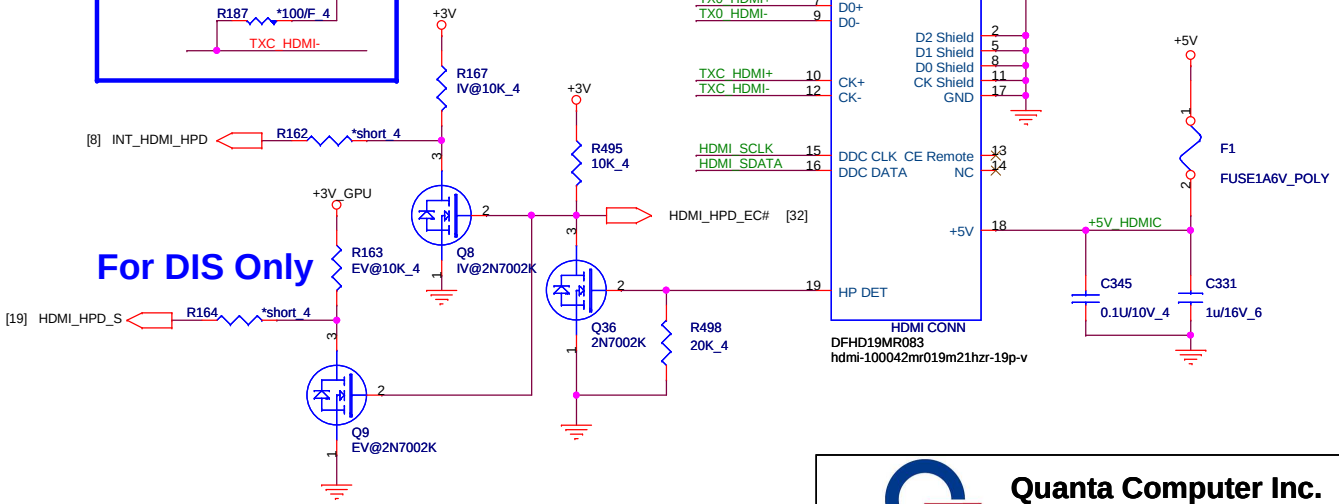


For UMA / Optimus HDMI function

EMI



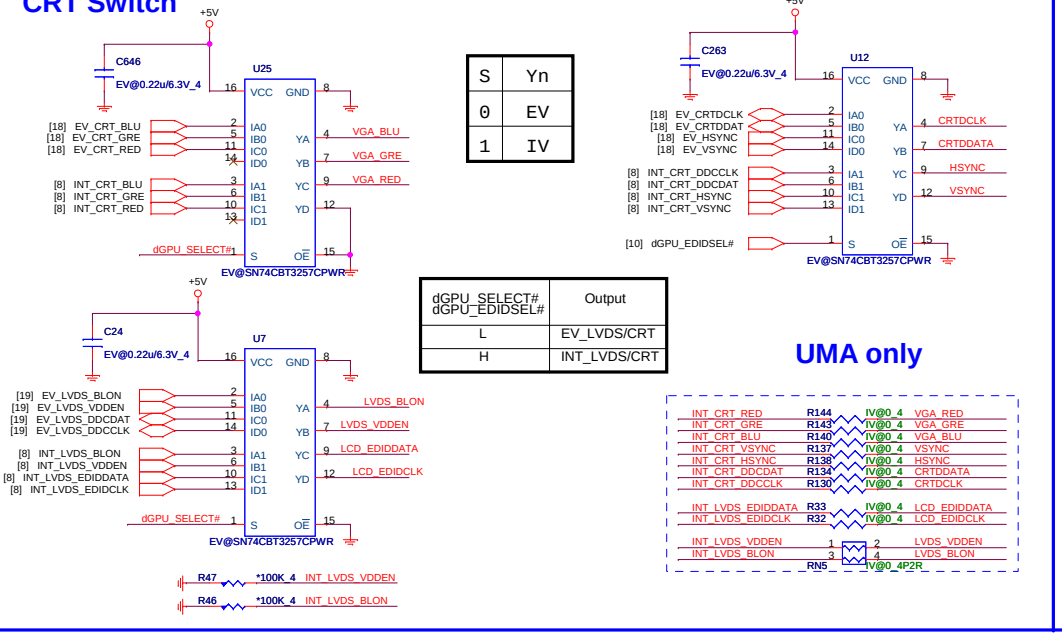
HDMI CONN



Quanta Computer Inc.
PROJECT : ZRJ

Size	Document Number	Rev
	CRT CONN/HDMI	1A
Date: Saturday, January 22, 2011	Sheet 23 of 41	

CRT Switch

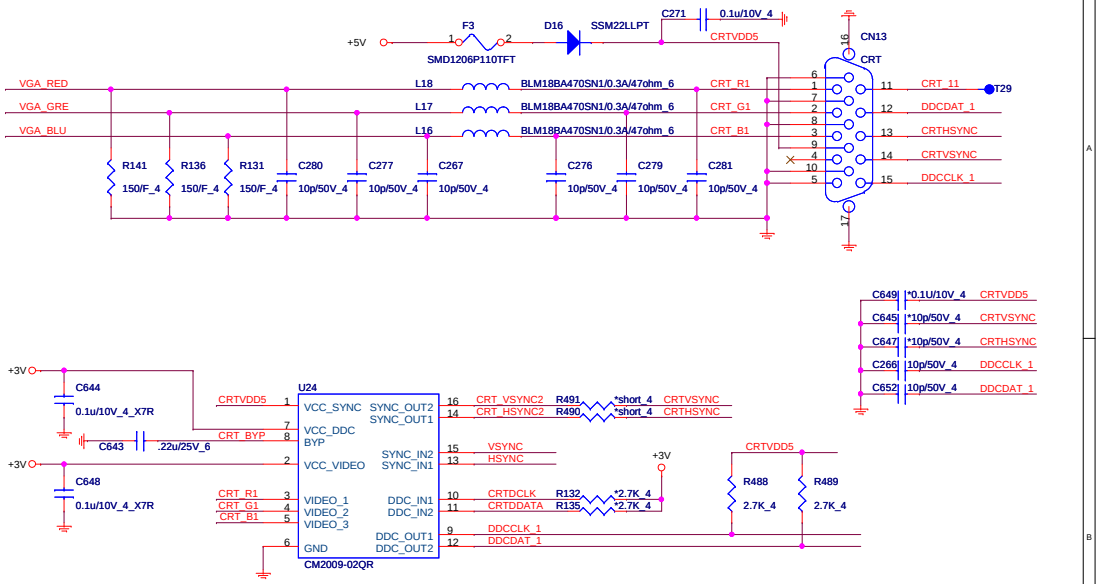


S	Yn
0	EV
1	IV

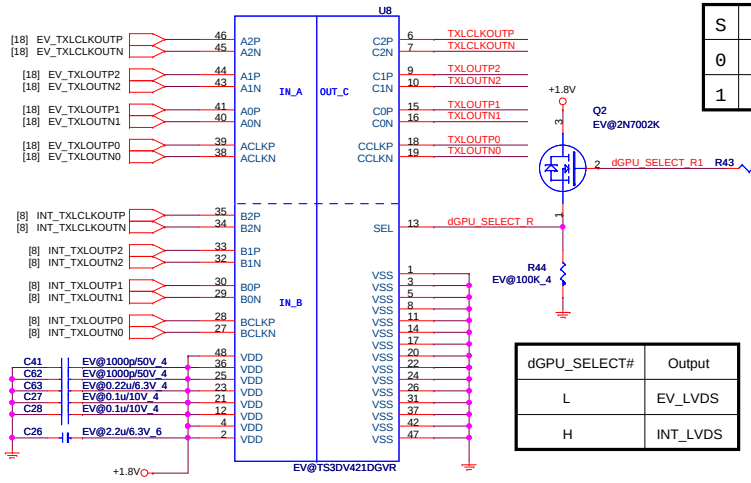
dGPU_SELECT# dGPU_EDIDSEL#	Output
L	EV_LVDS/CRT
H	INT_LVDS/CRT

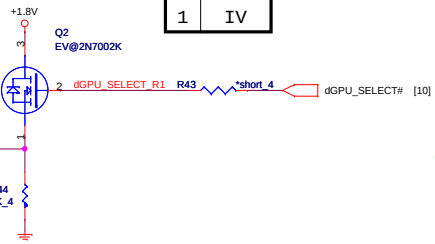
UMA only

CRT



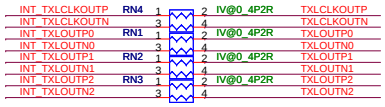
LVDS Switch





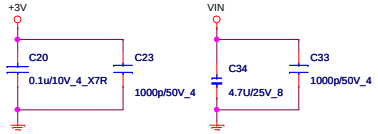
dGPU_SELECT#	Output
L	EV_LVDS
H	INT_LVDS

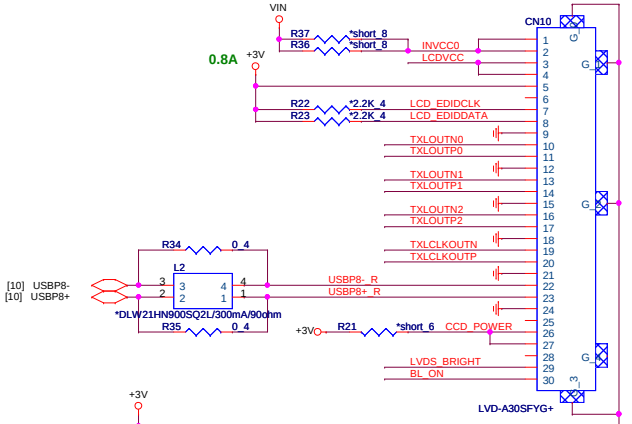
UMA only

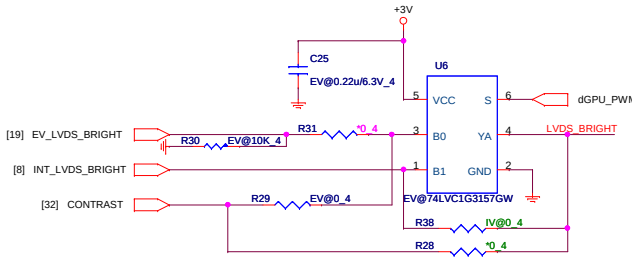


LVDS

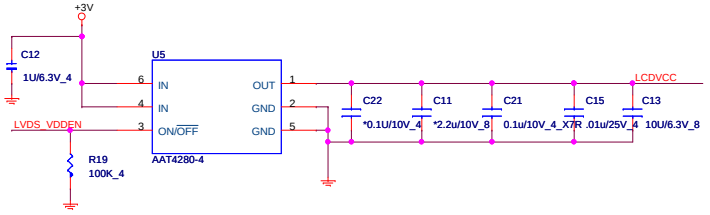
S	Yn
0	EV
1	IV



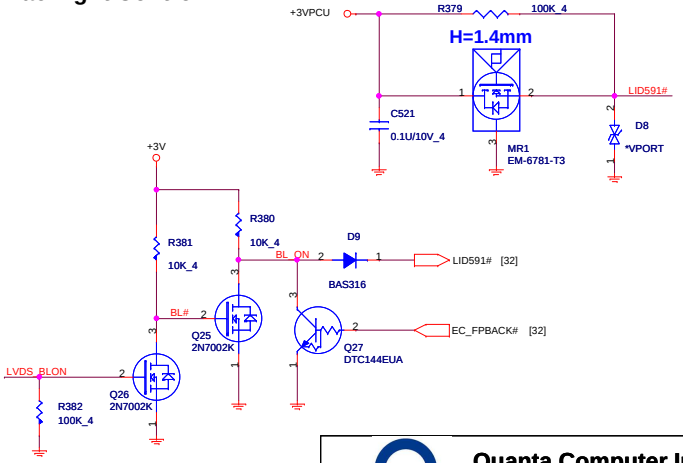




LCD Power



Backlight Control



Quanta Computer Inc.

PROJECT : ZRJ

Size	Document Number	Rev
	CRT/LVDS/CCD/HALL	1A

Date: Saturday, January 22, 2011 Sheet 24 of 41

LAN (LAN)
Arthorus AR8151

close Pin1

+3V_S5 — R61 *short_8 — +3V_LAN

C81 4.7U/25V_8 | C91 *10U/6.3V_8 | C67 1u/6.3V_4 | C72 0.1u/10V_4 | C78 1000p/50V_4

U9 — AR8151 (5X5mm, 40-Pin QFN)

1	VDD33	AVDDH	22	AVDDH_REG	C42 0.1u/10V_4
2	PERSTn	CLKREQn/LED2	23	LED2	T1
3	WAKEn	DVDDL	24	DVDDL_REG	C44 0.1u/10V_4
4	CLKREQn	SMCLK	25		T3
5	VDDCT	SMDATA	26		T2
6	AVDDL_REG	TESTMODE	27		
7	XTLO	TEST_RST	28		
8	XTLI	TX_N	29	PCIE_RXN1_C	C69 0.1u/10V_4 — PCIE_RX1- [10]
9	AVDDH_REG	TX_P	30	PCIE_RXP1_C	C70 0.1u/10V_4 — PCIE_RX1+ [10]
10	RBIAS	AVDDL	31	AVDDL_REG	C76 0.1u/10V_4
11	TRXP0	REFCLK_N	32		CLK_PCIE_LANN [10]
12	TRXN0	REFCLK_P	33		CLK_PCIE_LANP [10]
13	NC/AVDDL	AVDDL	34	AVDDL_REG	C77 0.1u/10V_4
14	TRXP1	RX_P	35		PCIE_TX1+ [10]
15	TRXN1	RX_N	36		PCIE_TX1- [10]
16	NC/AVDDH	DVDDL_REG	37	DVDDL_REG	C73 1u/6.3V_4
17	NC/TRXP2	LED0	38	LAN_ACTLED#	C74 0.1u/10V_4
18	NC/TRXN2	LED1	39	LAN_LINKLED#	
19	NC/AVDDL	LX	40	LX	L3 4.7uH/1A_2X2 — +VDDCT
20	NC/TRXP3	GND	41		C92 4.7U/25V_8, C83 0.1u/10V_4, C84 1000p/50V_4
21	NC/TRXN3				

[4,10,16,26,29,32] PLTRST# — PLTRST#
[8] PCIE_WAKE# — PCIE_WAKE#
[10] PCIE_CLKREQ_LAN# — CLKREQn
C65 0.1u/10V_4 +VDDCT — VDDCT
C64 1u/6.3V_4, C46 0.1u/10V_4 — AVDDL_REG
XTLO, XTLI
C38 1u/6.3V_4, C39 0.1u/10V_4 — AVDDH_REG
R45 2.37K/F_4 — RBIAS
TX0P R4 1/F_4 TX0P_C
TX0N R5 1/F_4 TX0N_C
C37 0.1u/10V_4 AVDDL_REG
TX1P R10 1/F_4 TX1P_C
TX1N R12 1/F_4 TX1N_C
C36 0.1u/10V_4 AVDDH_REG
TX2P R13 1/F_4 TX2P_C
TX2N R14 1/F_4 TX2N_C
C35 0.1u/10V_4 AVDDL_REG
TX3P R15 1/F_4 TX3P_C
TX3N R16 1/F_4 TX3N_C

C43 33p/50V_4 — XTLO
1.2H — Y1 25MHz
C40 33p/50V_4 — XTLI

TRANSFORMER(LAN)

TX0P_C R27 49.9/F_4 — LAN_N1 — C19 0.1U/10V_4, C18 *1000p/50V_4
TX0N_C R26 49.9/F_4
TX1P_C R41 49.9/F_4 — LAN_N2 — C32 0.1U/10V_4, C31 *1000p/50V_4
TX1N_C R40 49.9/F_4
TX2P_C R25 49.9/F_4 — LAN_N3 — C17 0.1U/10V_4, C16 *1000p/50V_4
TX2N_C R24 49.9/F_4
TX3P_C R39 49.9/F_4 — LAN_N4 — C30 0.1U/10V_4, C29 *1000p/50V_4
TX3N_C R42 49.9/F_4

Close Transformer U2

AVDD_CEN — BLM11A601S L1 — +VDDCT
C9 1U/10V_4

C7 0.1u/10V_4, C8 *1000p/50V_4 — TX0P, TX0N
C10 0.1u/10V_4, C3 *1000p/50V_4 — TX1P, TX1N
C4 0.1u/10V_4, C6 *1000p/50V_4 — TX2P, TX2N
C5 0.1u/10V_4, C1 *1000p/50V_4 — TX3P, TX3N

U20 — TRANSFORMER

1	TCT1	MCT1	24	
2	TD1+	MX1+	23	X-TX0P
3	TD1-	MX1-	22	X-TX0N
4	TCT2	MCT2	21	
5	TD2+	MX2+	20	X-TX1P
6	TD2-	MX2-	19	X-TX1N
7	TCT3	MCT3	18	
8	TD3+	MX3+	17	X-TX2P
9	TD3-	MX3-	16	X-TX2N
10	TCT4	MCT4	15	
11	TD4+	MX4+	14	X-TX3P
12	TD4-	MX4-	13	X-TX3N

Delta LFE9276D-R (DB0ZY8LAN00)

R1 75/F_8, R2 75/F_8, R11 75/F_8, R383 75/F_8
D2 *B88069X9231T203
C522 1500p/3KV_18
LANGND

U2 *UCLAMP2512T.TCT — TX1N_C, TX1P_C, TX0N_C, TX0P_C
U3 *UCLAMP2512T.TCT — TX3N_C, TX3P_C, TX2N_C, TX2P_C

U1 *SRV05-4.TCT — X-TX0N, X-TX0P
U4 *SRV05-4.TCT — X-TX2N, X-TX2P

RJ45(LAN)

LAN_ACTLED# — R59 220_8 — LAN_ACT_LED_PWR
R58 5.1K_4
+3V_LAN — R60 220_8 — LAN_LNK_LED_PWR
LAN_LINKLED#

CN9 — RJ45
YELLOW_P, YELLOW_N
X-TX3N, X-TX3P, X-TX1N, X-TX2N, X-TX2P, X-TX1P, X-TX0N, X-TX0P
GREEN_P, GREEN_N
GND2, GND1 — LANGND

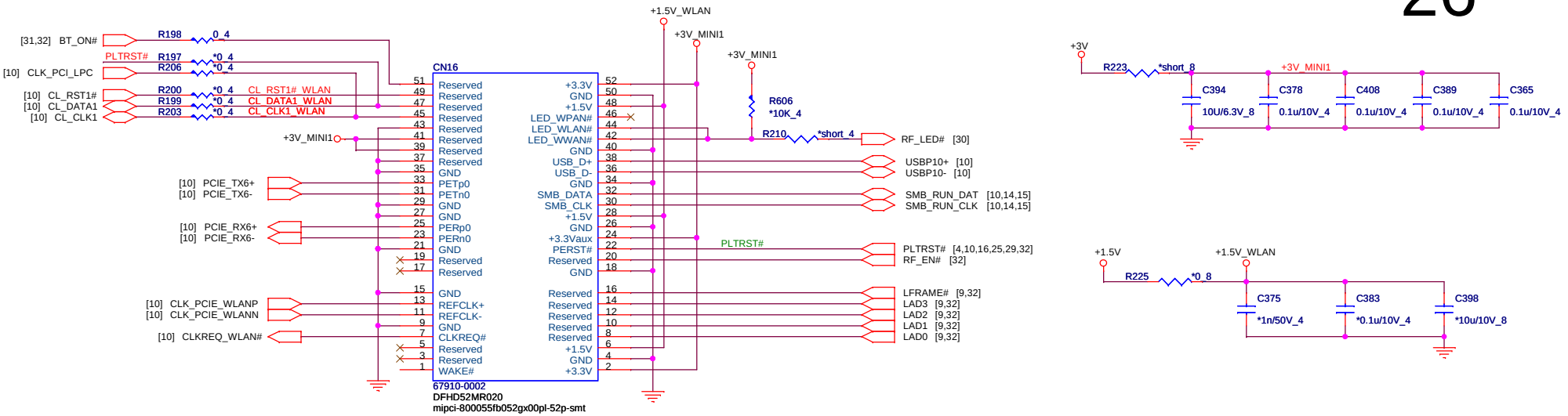
LAN_ACTLED#, LAN_LINKLED#
C85 *0.1u//50V_8, C96 *0.1u//50V_8
C2 0.1u//50V_8, C14 0.1u//50V_8 — LANGND

Quanta Computer Inc.
PROJECT : ZRJ

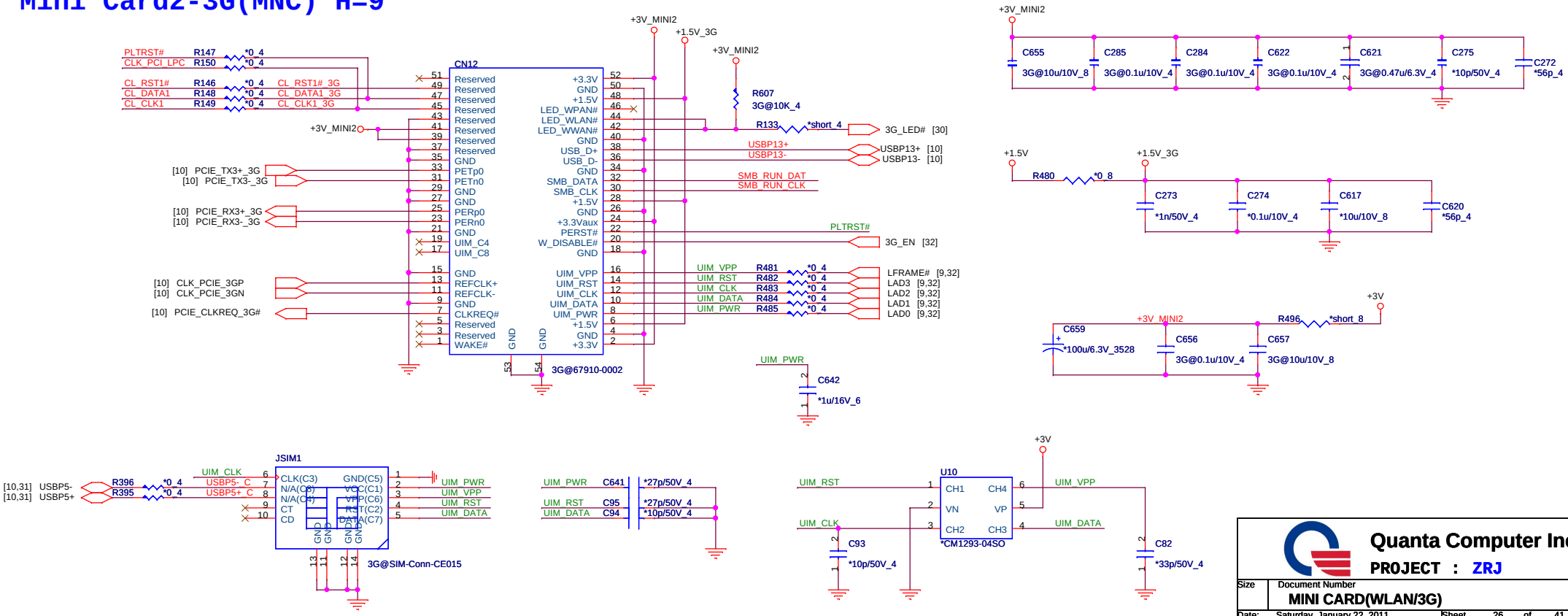
Size	Document Number	Rev
	LAN (AR8151)	1A

Date: Saturday, January 22, 2011 — Sheet 25 of 41

MINI CARD (WLAN) H=7

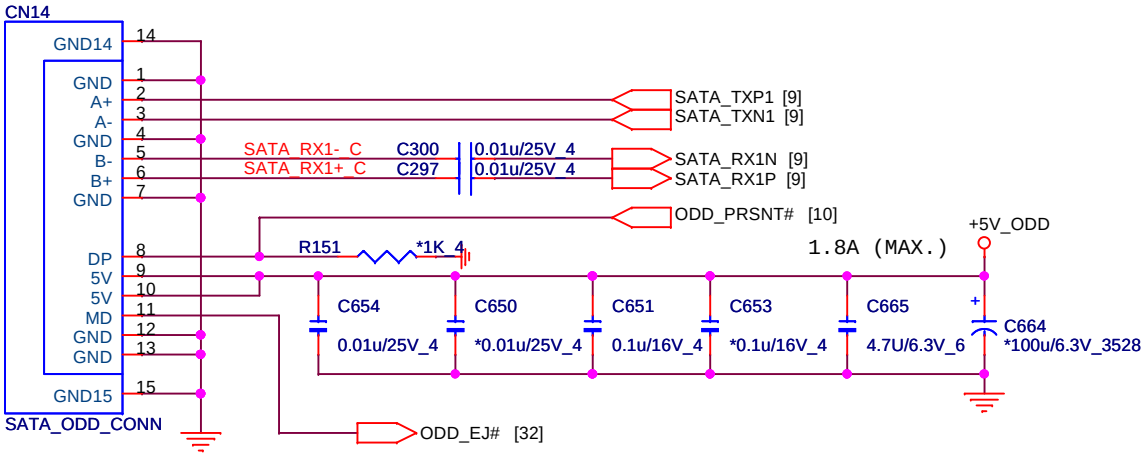


Mini Card2-3G(MNC) H=9

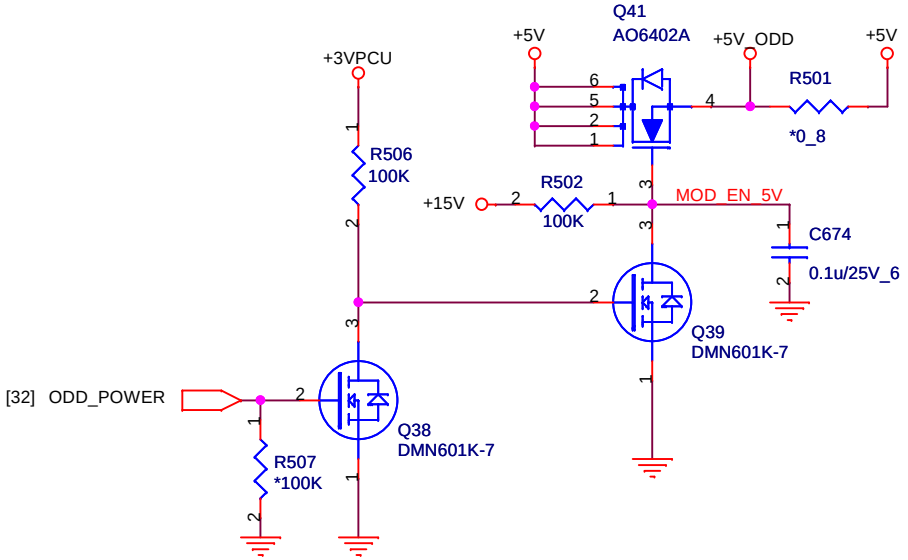


Quanta Computer Inc.	
PROJECT : ZRJ	
Size	Document Number: MINI CARD(WLAN/3G) — Rev: 1A
Date: Saturday, January 22, 2011	Sheet 26 of 41

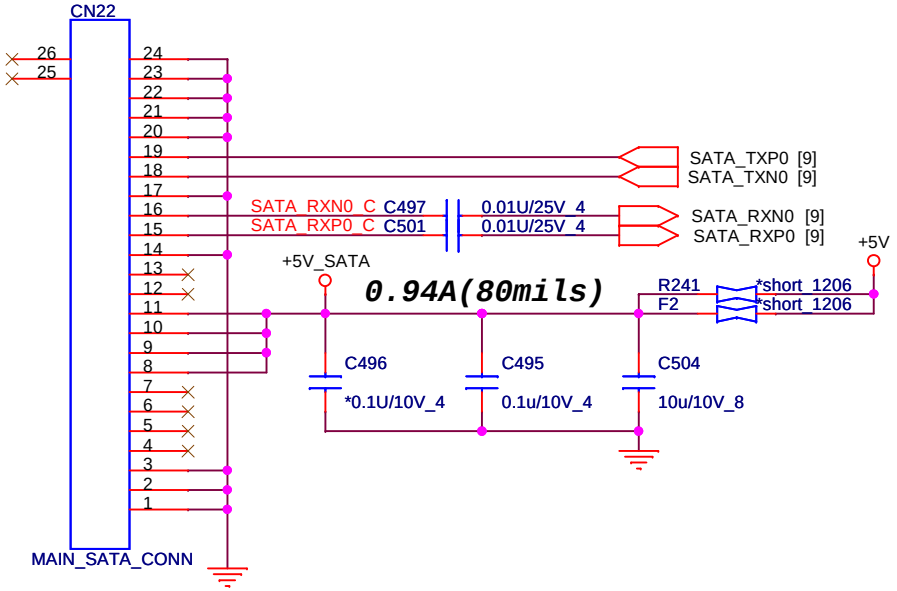
ODD (SATA)

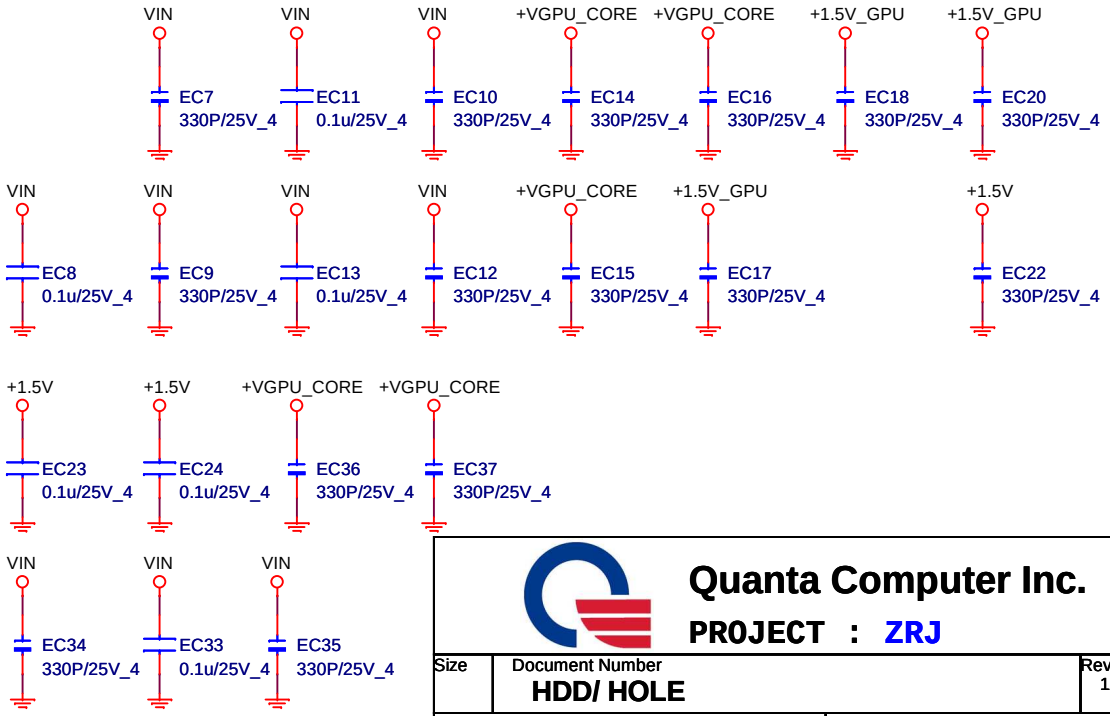


ODD Power (SATA)



2.5" SATA HDD



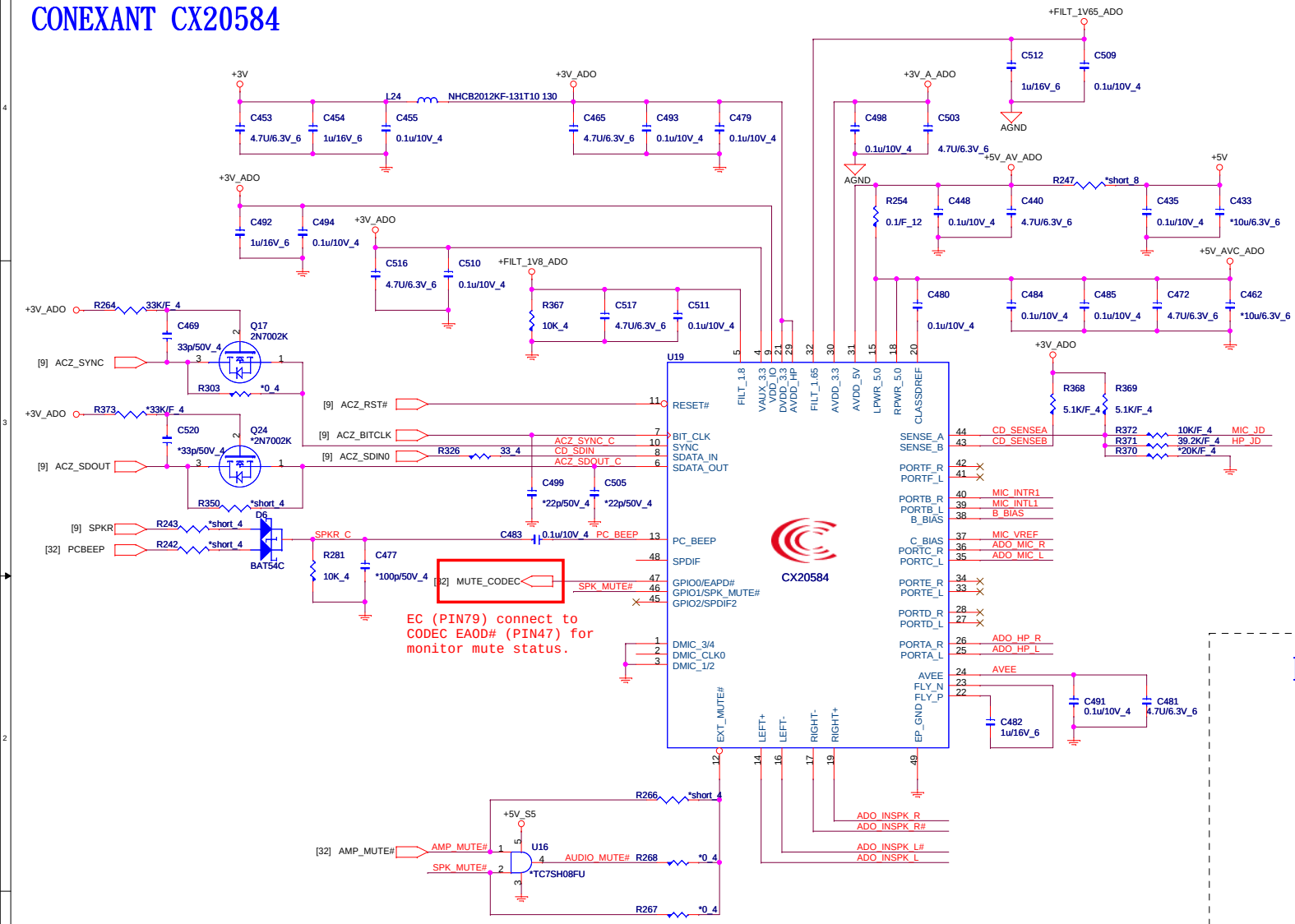


Quanta Computer Inc.

PROJECT : ZRJ

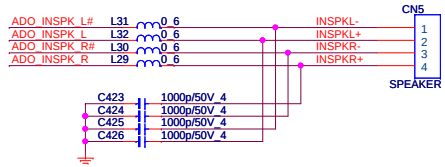
Size	Document Number	Rev
	HDD/ HOLE	1A
Date: Saturday, January 22, 2011	Sheet 27 of 41	

CODEC (ADO)
CONEXANT CX20584

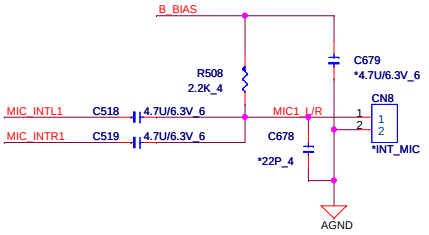


EC (PIN79) connect to CODEC EAOD# (PIN47) for monitor mute status.

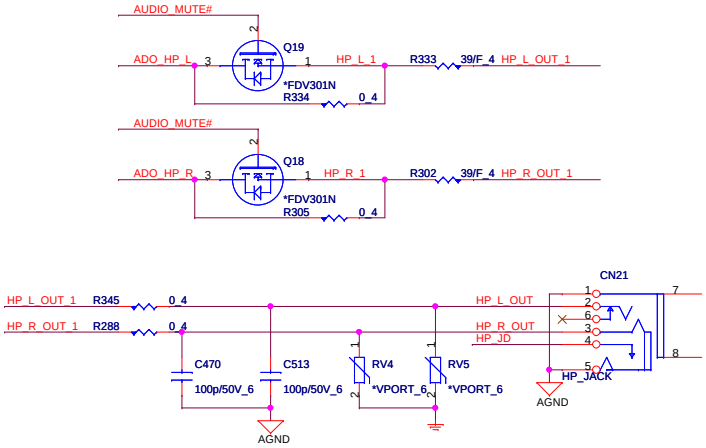
Speaker



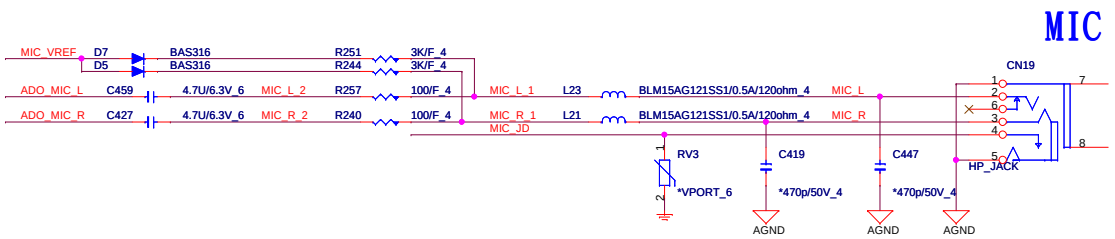
INT MIC



HP/SPDIF



MIC



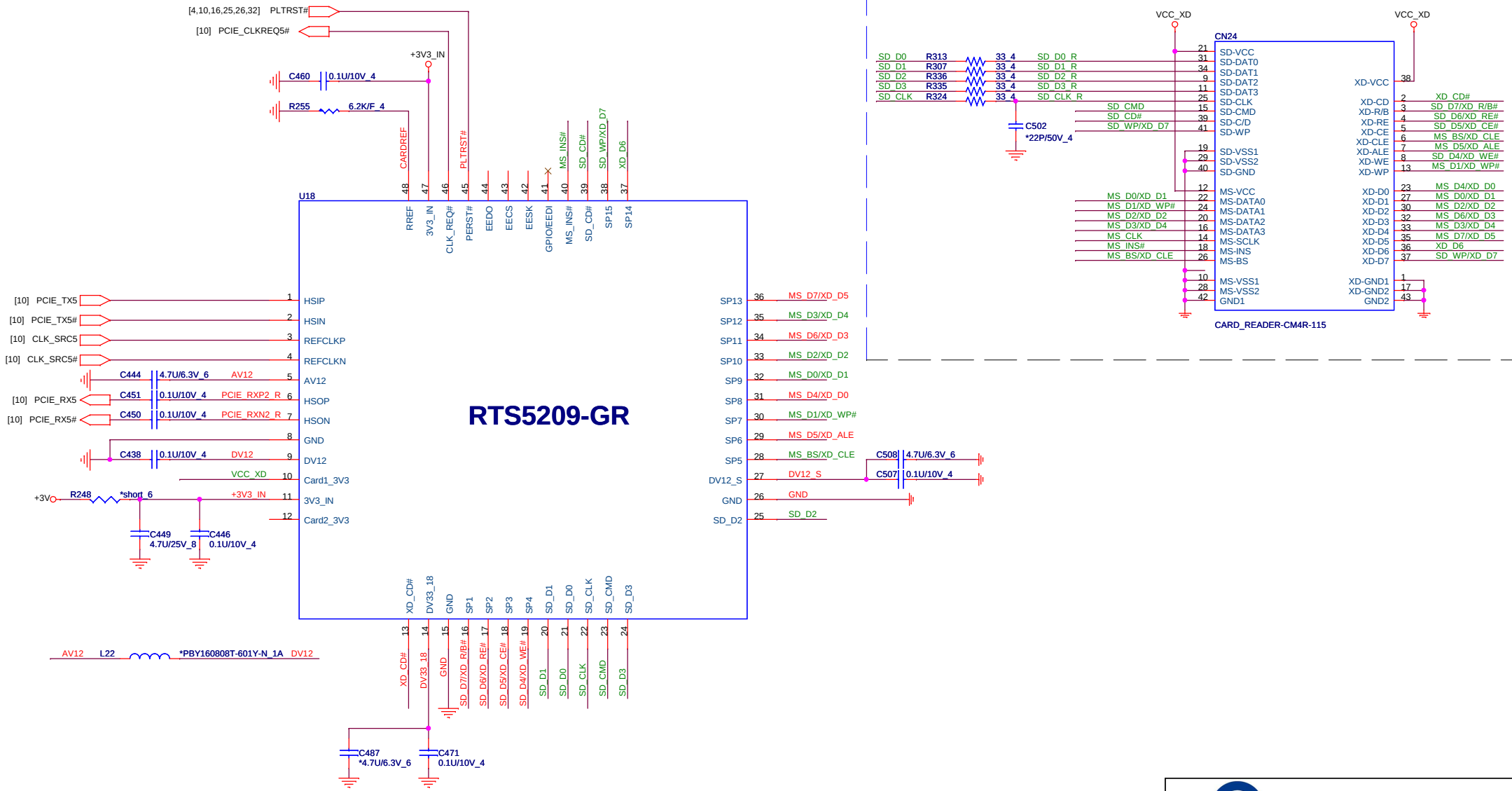
Quanta Computer Inc.		
PROJECT : ZRJ		
Size	Document Number: CODEC CX20584	Rev: 1A
Date: Saturday, January 22, 2011	Sheet 28 of 41	

Card reader controller

<MMC>

5 IN 1 Card reader CONN

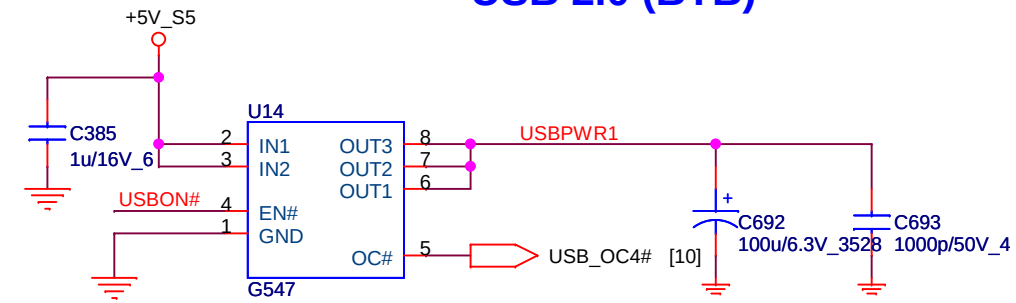
<MMC>

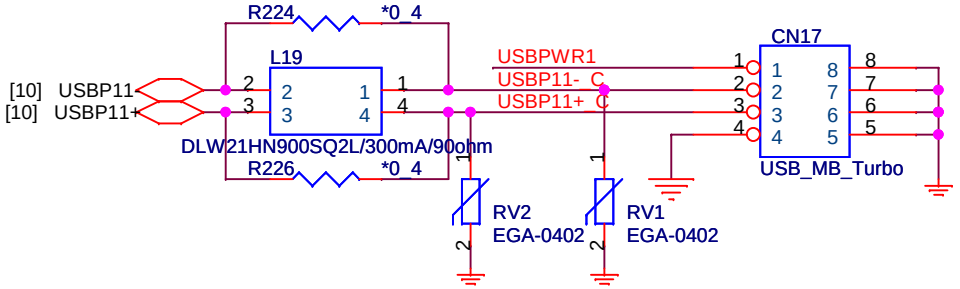


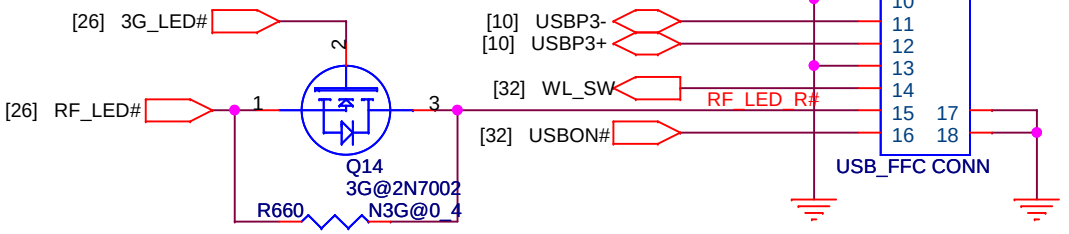
Quanta Computer Inc.		
PROJECT : ZRJ		
Size	Document Number	Rev
	RTS5209 (Card Reader)	3G
Date: Saturday, January 22, 2011	Sheet 29 of 41	

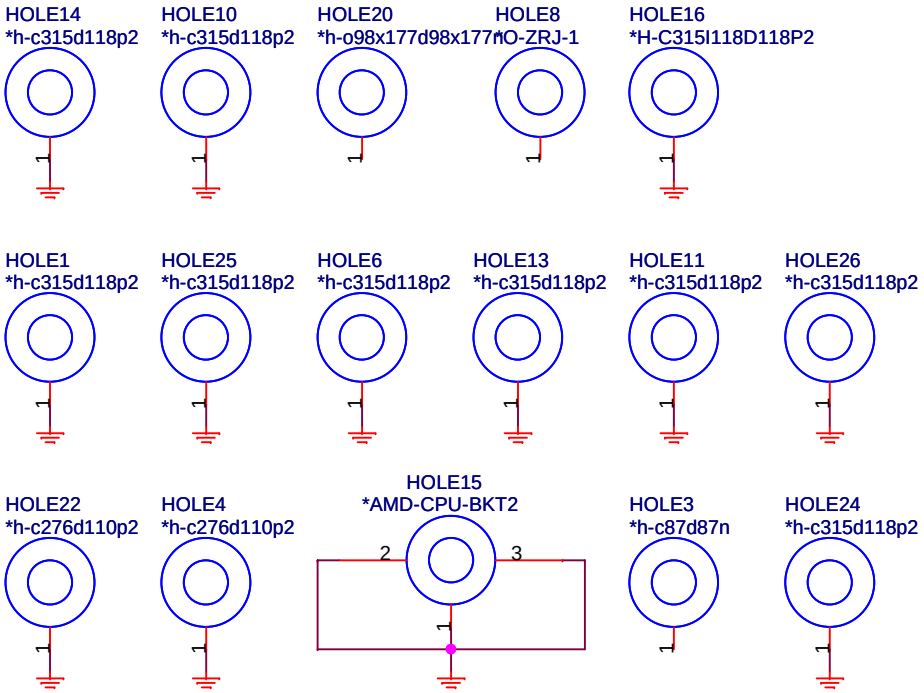
USB 2.0 (BTB)

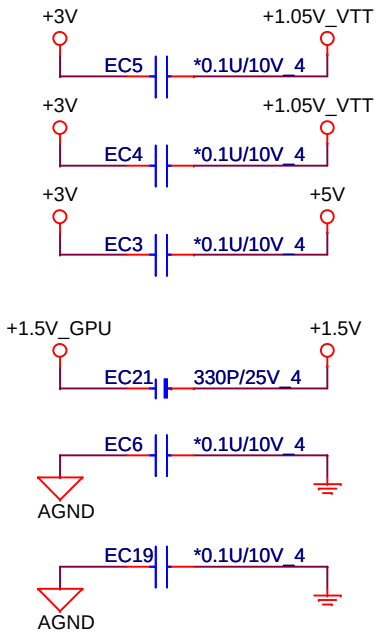
30

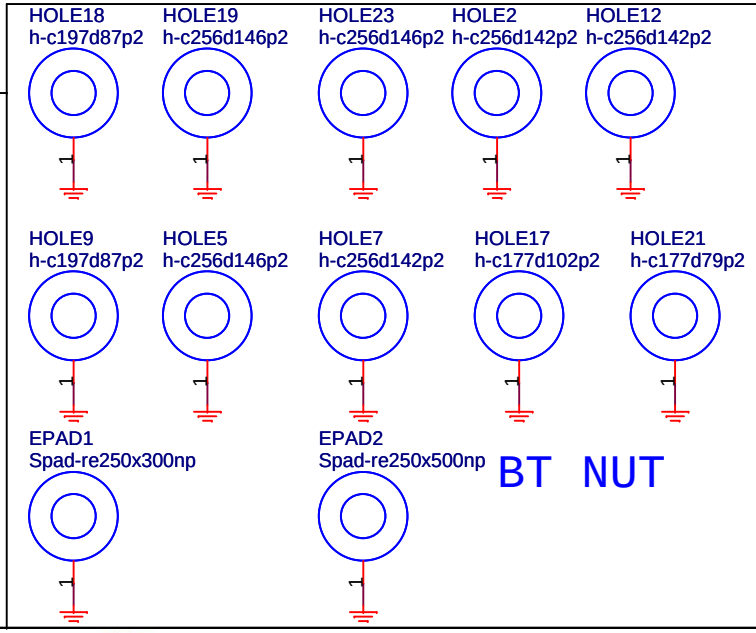










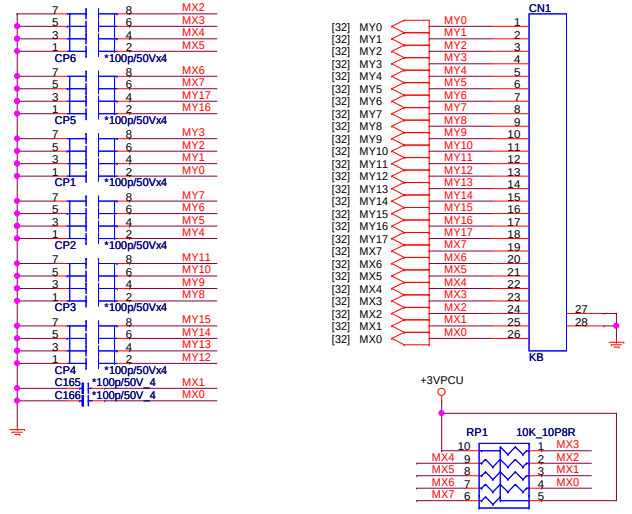


Quanta Computer Inc.

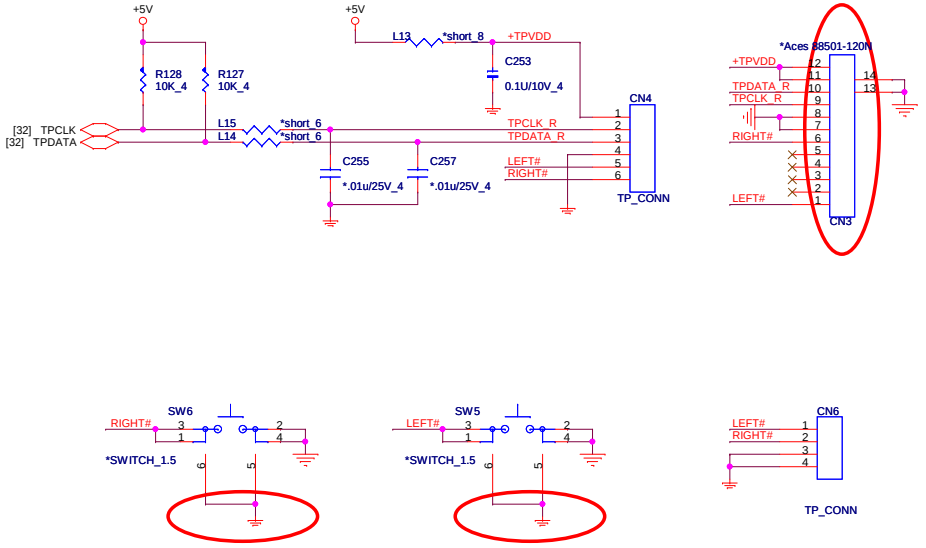
PROJECT : ZRJ

Size	Document Number	Rev
	USB2.0 Board (Dual Way)	1A
Date: Monday, January 24, 2011	Sheet 30 of 41	

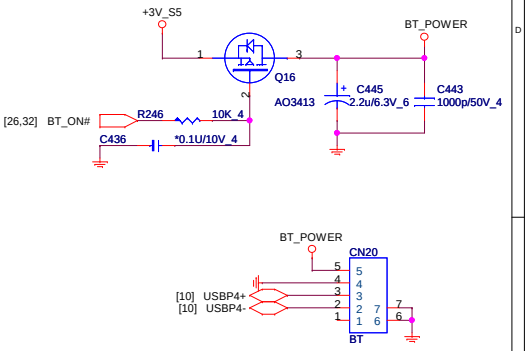
Keyboard (KBC)



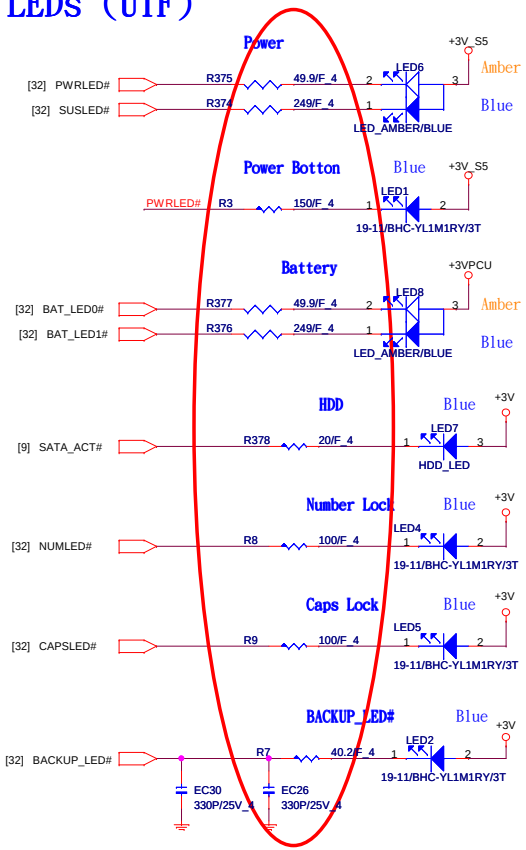
TouchPad (TPD)

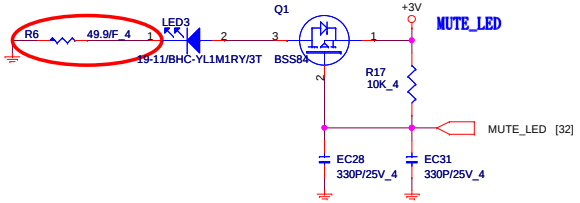


Bluetooth (BTM)

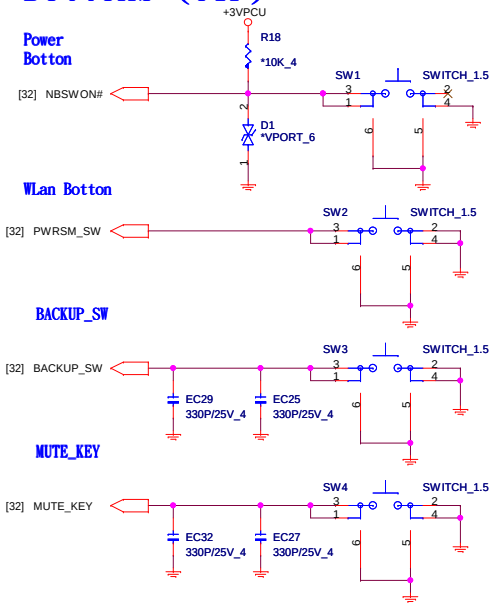


LEDs (UIF)

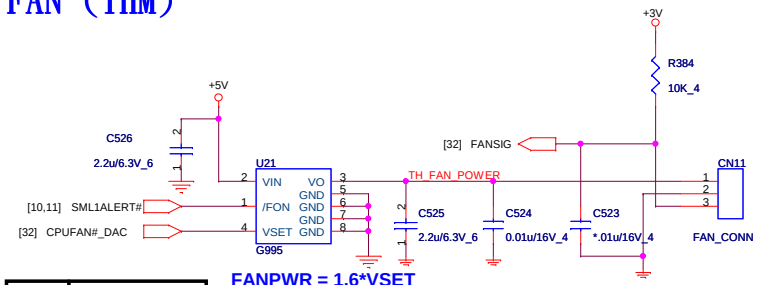




Bottons (UIF)

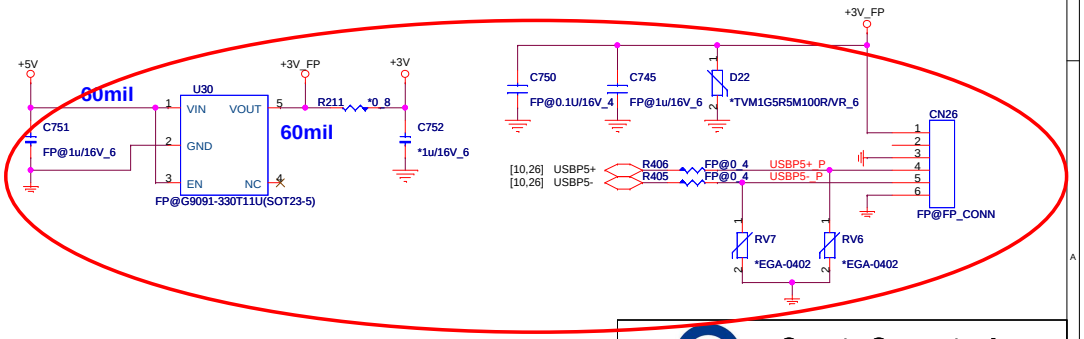


FAN (THM)



ACS	DFWF03MS091
SCY	DFWF03MS000

Finger-Printer CONN.

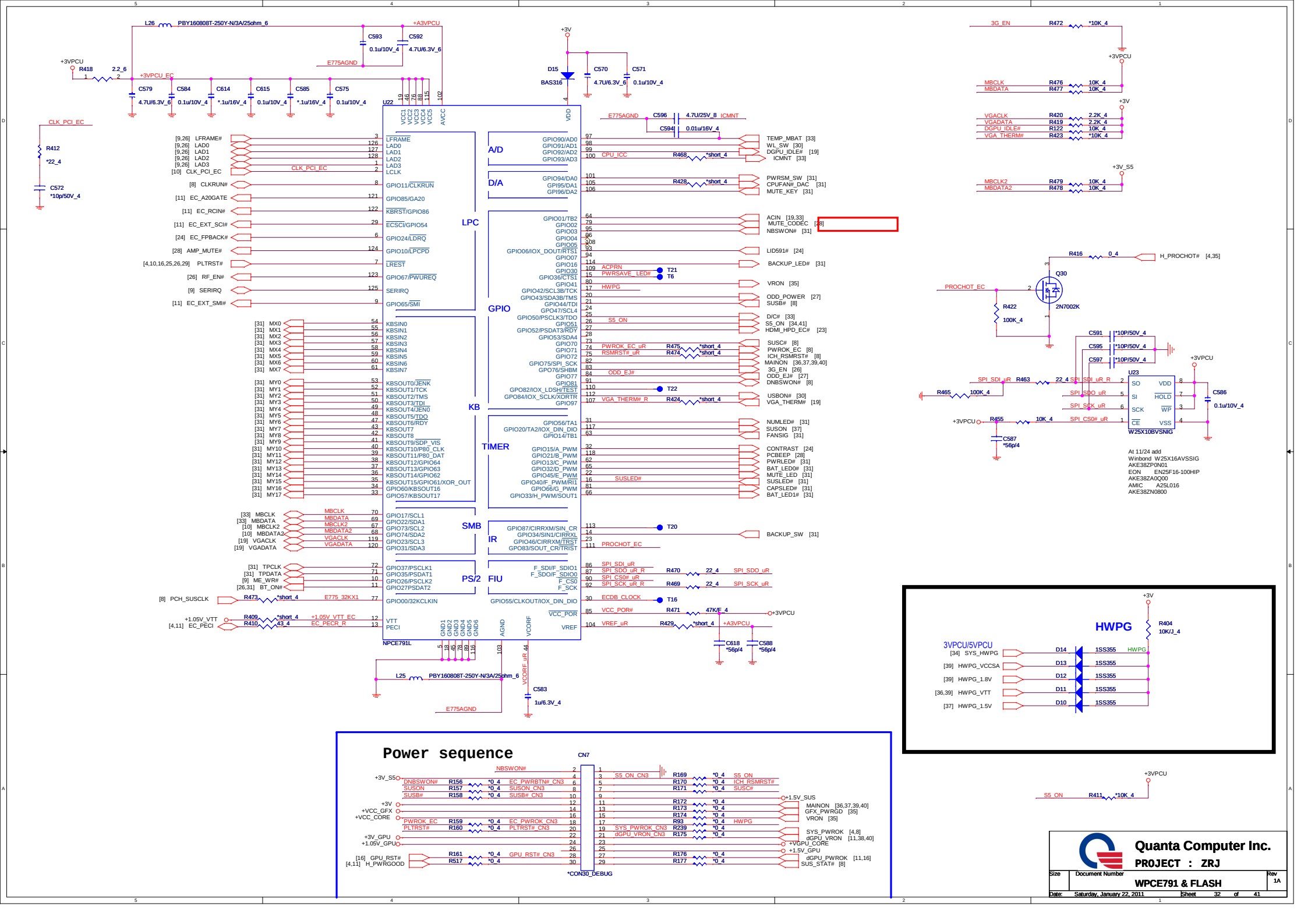


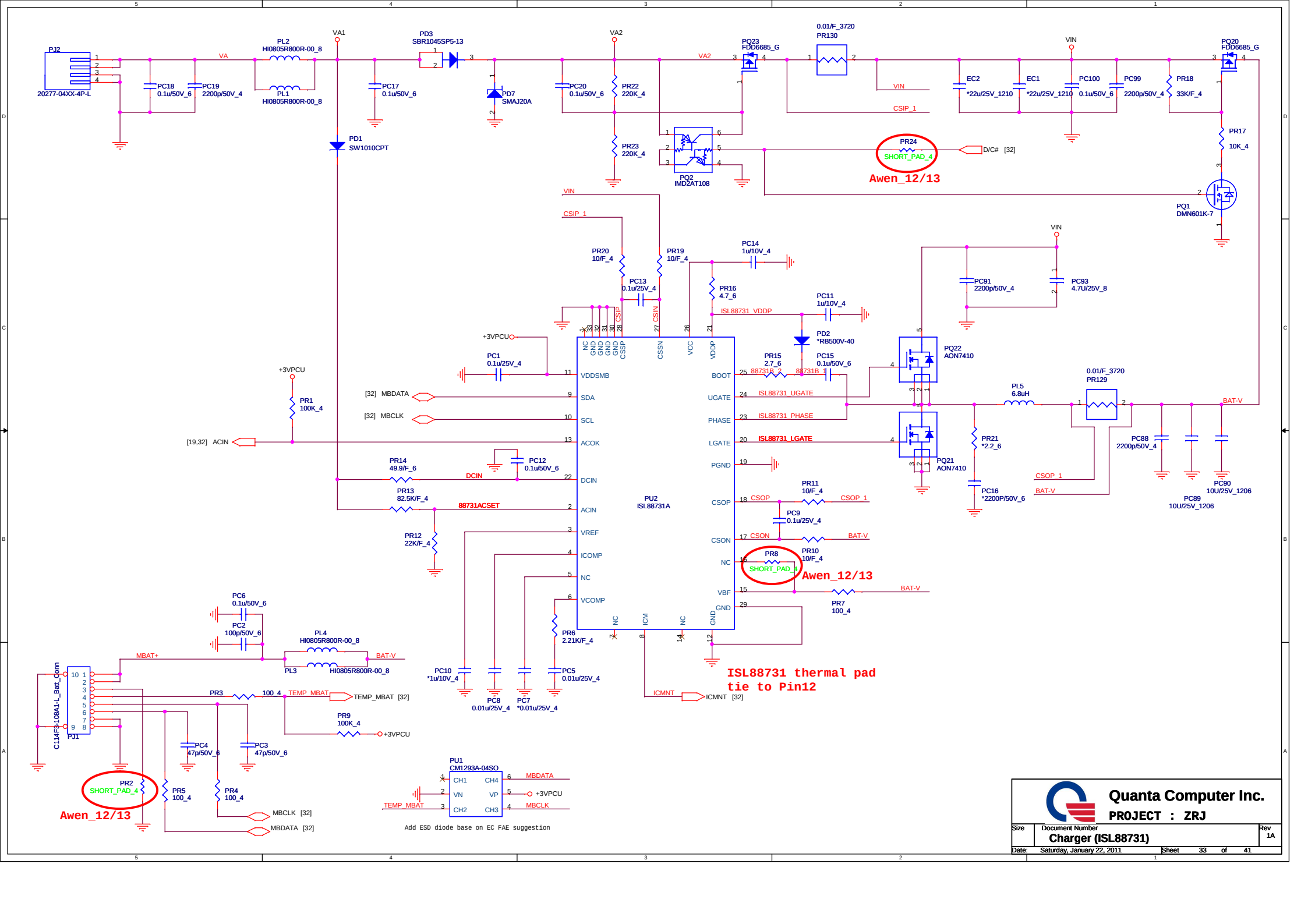
Quanta Computer Inc.

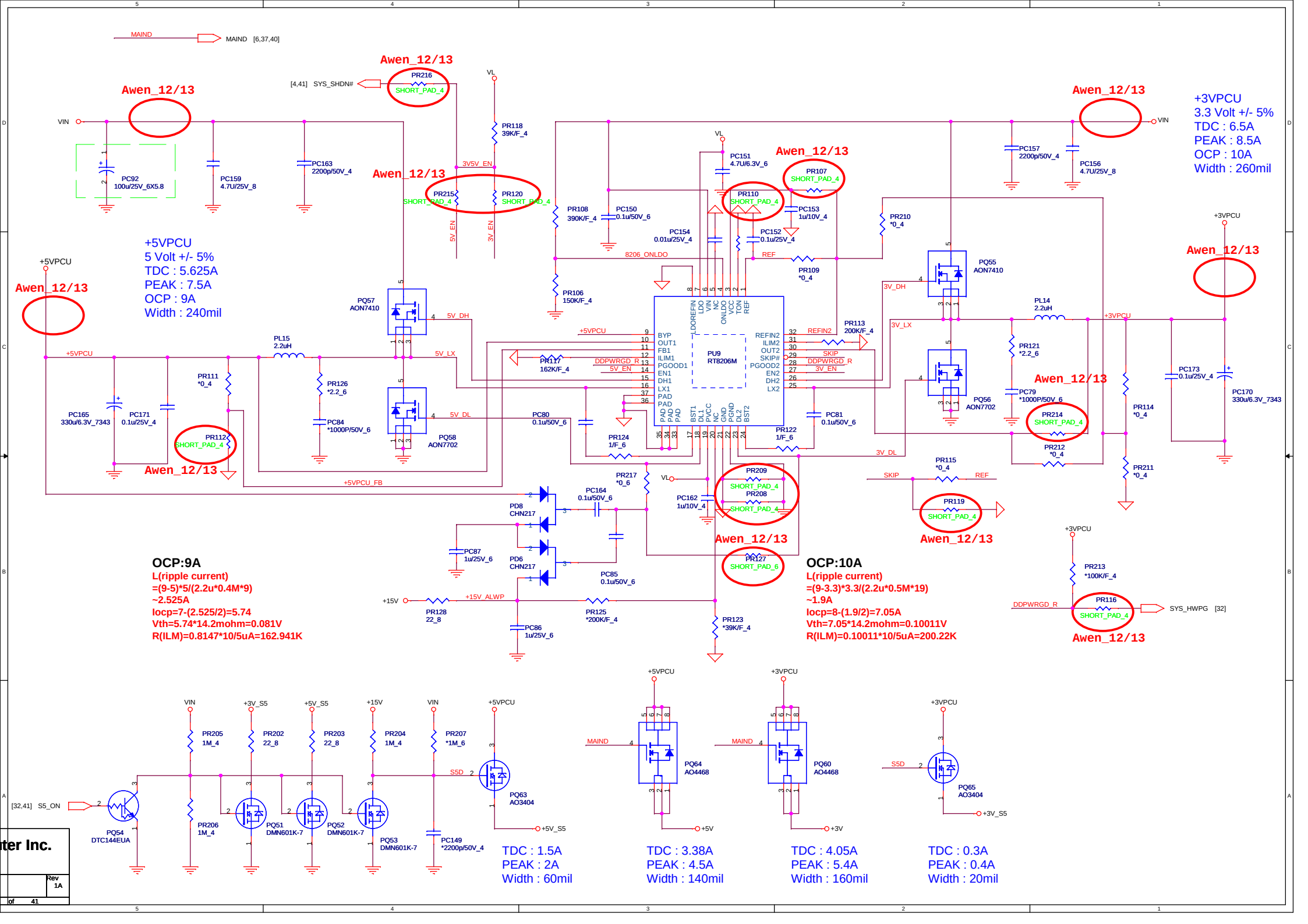
PROJECT : ZRJ

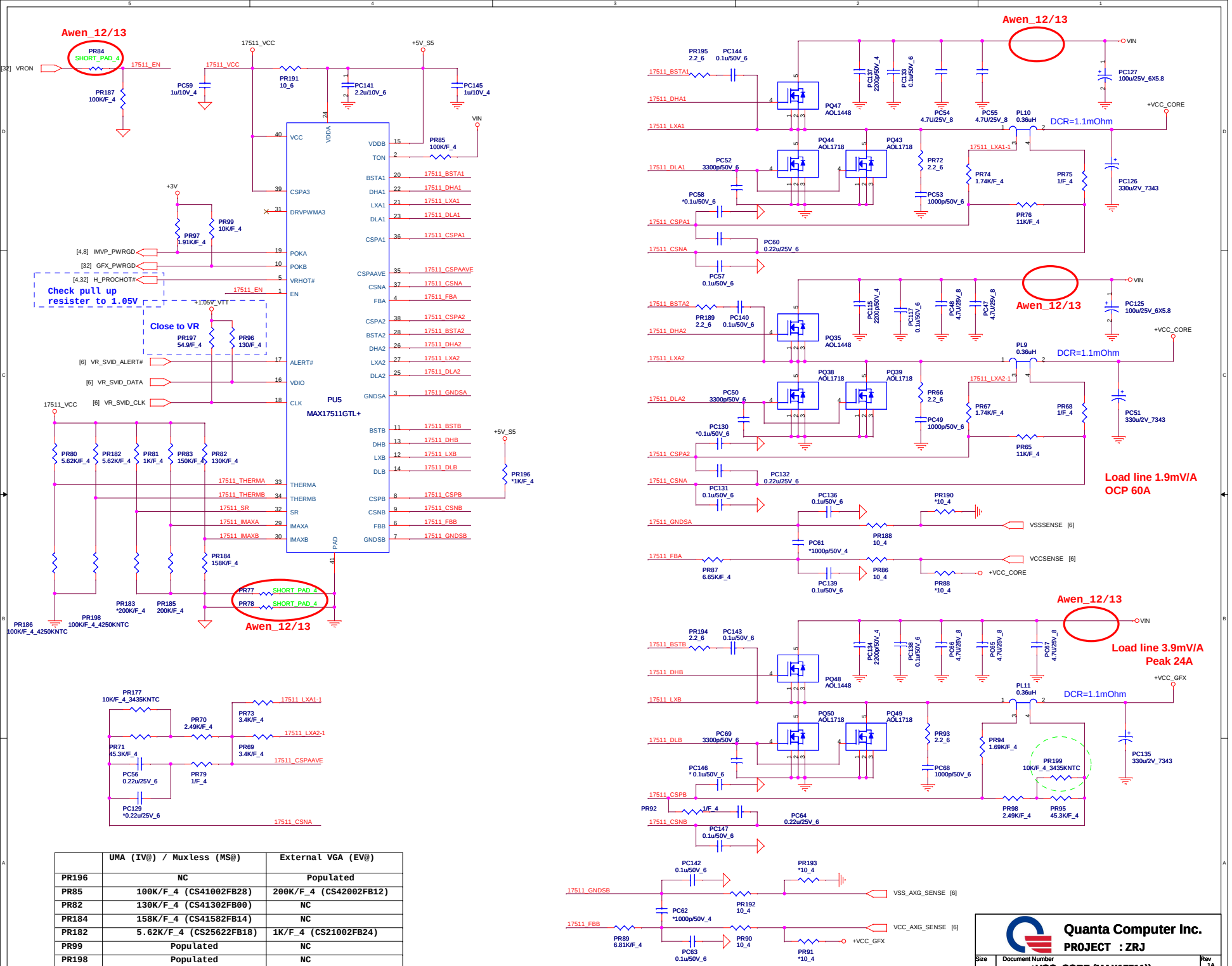
Size	Document Number	Rev
	KB/TP/BT/FAN/USB/LED/Bottom	1A

Date: Saturday, January 22, 2011 Sheet 31 of 41


L26 PBY160808T-250Y-N/3A/25ohm_6
+A3VPCU
C593 0.1u/10V_4
C592 4.7U/6.3V_6
E775AGND
+3VPCU
R418 2.2_6
+3VPCU_EC
C579 4.7U/6.3V_6
C584 0.1u/10V_4
C614 *.1u/16V_4
C615 0.1u/10V_4
C585 *.1u/16V_4
C575 0.1u/10V_4
U22
VCC1 VCC2 VCC3 VCC4 VCC5 AVCC
VDD
CLK_PCI_EC
R412 *22_4
C572 *10p/50V_4
[9,26] LFRAME#
[9,26] LAD0
[9,26] LAD1
[9,26] LAD2
[9,26] LAD3
[10] CLK_PCI_EC
[8] CLKRUN#
[11] EC_A20GATE
[11] EC_RCIN#
[11] EC_EXT_SCI#
[24] EC_FPBACK#
[28] AMP_MUTE#
[4,10,16,25,26,29] PLTRST#
[26] RF_EN#
[9] SERIRQ
[11] EC_EXT_SMI#
LPC
A/D
D/A
GPIO
KB
TIMER
SMB
PS/2
IR
FIU
[31] MX0
[31] MX1
[31] MX2
[31] MX3
[31] MX4
[31] MX5
[31] MX6
[31] MX7
[31] MY0
[31] MY1
[31] MY2
[31] MY3
[31] MY4
[31] MY5
[31] MY6
[31] MY7
[31] MY8
[31] MY9
[31] MY10
[31] MY11
[31] MY12
[31] MY13
[31] MY14
[31] MY15
[31] MY16
[31] MY17
[33] MBCLK
[33] MBDATA
[10] MBCLK2
[10] MBDATA2
[19] VGACLK
[19] VGADATA
[31] TPCLK
[31] TPDATA
[9] ME_WR#
[26,31] BT_ON#
[8] PCH_SUSCLK
R473 *short_4
E775_32KX1
+1.05V_VTT
[4,11] EC_PECI
R409 *short_4
R410 43_4
+1.05V_VTT_EC
EC_PECR_R
NPCE791L
GND1 GND2 GND3 GND4 GND5 GND6 AGND VCORF
L25 PBY160808T-250Y-N/3A/25ohm_6
VCORF_uR_44
C583 1u/6.3V_4
E775AGND
+3V
D15 BAS316
C570 4.7U/6.3V_6
C571 0.1u/10V_4
E775AGND
C596 4.7U/25V_8 ICMNT
C594 0.01u/16V_4
TEMP_MBAT [33]
WL_SW [30]
DGPU_IDLE# [19]
ICMNT [33]
CPU_ICC
R468 *short_4
PWRSM_SW [31]
CPUFAN#_DAC [31]
MUTE_KEY [31]
ACIN [19,33]
MUTE_CODEC [28]
NBSWON# [31]
LID591# [24]
BACKUP_LED# [31]
ACPRN
PWRSAVE_LED#
T21
T6
VRON [35]
ODD_POWER [27]
SUSB# [8]
S5_ON
D/C# [33]
S5_ON [34,41]
HDMI_HPD_EC# [23]
SUSC# [8]
PWROK_EC_uR
RSMRST#_uR
R475 *short_4
R474 *short_4
PWROK_EC [8]
ICH_RSMRST# [8]
MAINON [36,37,39,40]
3G_EN [26]
ODD_EJ# [27]
DNBSWON# [8]
ODD_EJ#
T22
USBON# [30]
VGA_THERM# [19]
VGA_THERM#_R
R424 *short_4
NUMLED# [31]
SUSON [37]
FANSIG [31]
CONTRAST [24]
PCBEEP [28]
PWRLED# [31]
BAT_LED0# [31]
MUTE_LED [31]
SUSLED# [31]
CAPSLED# [31]
BAT_LED1# [31]
SUSLED#
T20
BACKUP_SW [31]
PROCHOT_EC
SPI_SDI_uR
SPI_SDO_uR
SPI_CS0#_uR
SPI_SCK_uR
R470 22_4
R469 22_4
ECDB_CLOCK
T16
VCC_POR#
R471 47K/F_4
VREF_uR
R429 *short_4
+A3VPCU
C618 *56p/4
C588 *56p/4
3G_EN
R472 *10K_4
MBCLK
MBDATA
R476 10K_4
R477 10K_4
VGACLK
VGADATA
DGPU_IDLE#
VGA_THERM#
R420 2.2K_4
R419 2.2K_4
R122 10K_4
R423 *10K_4
+3V_S5
MBCLK2
MBDATA2
R479 10K_4
R478 10K_4
R416 0_4
H_PROCHOT# [4,35]
PROCHOT_EC
Q30
2N7002K
R422 100K_4
C591 *10P/50V_4
C595 *10P/50V_4
C597 *10P/50V_4
R465 100K_4
SPI_SDI_uR
R463 22_4
SPI_SDO_uR
SPI_SCK_uR
SPI_CS0#_uR
R455 10K_4
C587 *56p/4
U23
SO SI SCK CE VDD HOLD WP VSS
W25X10BVSNIG
C586 0.1u/10V_4
At 11/24 add
Winbond W25X16AVSSIG
AKE38ZP0N01
EON EN25F16-100HIP
AKE38ZA0Q00
AMIC A25L016
AKE38ZN0800
HWPG
3VPCU/5VPCU
[34] SYS_HWPG
[39] HWPG_VCCSA
[39] HWPG_1.8V
[36,39] HWPG_VTT
[37] HWPG_1.5V
D14 D13 D12 D11 D10
1SS355
R404 10K/J_4
Power sequence
CN7
NBSWON#
+3V_S5
DNBSWON# R156 *0_4 EC_PWRBTN#_CN3
SUSON R157 *0_4 SUSON_CN3
SUSB# R158 *0_4 SUSB#_CN3
+3V
+VCC_GFX
+VCC_CORE
PWROK_EC R159 *0_4 EC_PWROK_CN3
PLTRST# R160 *0_4 PLTRST#_CN3
+3V_GPU
+1.05V_GPU
[16] GPU_RST#
[4,11] H_PWRGOOD
R161 *0_4 GPU_RST#_CN3
R517 *0_4
S5_ON_CN3
R169 *0_4 S5_ON
R170 *0_4 ICH_RSMRST#
R171 *0_4 SUSC#
+1.5V_SUS
R172 *0_4
R173 *0_4
R174 *0_4
R93 *0_4 HWPG
SYS_PWROK_CN3
R239 *0_4
dGPU_VRON_CN3
R175 *0_4
+VGPU_CORE
+1.5V_GPU
R176 *0_4
R177 *0_4
MAINON [36,37,39,40]
GFX_PWRGD [35]
VRON [35]
SYS_PWROK [4,8]
dGPU_VRON [11,38,40]
dGPU_PWROK [11,16]
SUS_STAT# [8]
*CON30_DEBUG
S5_ON
R411 *10K_4
Quanta Computer Inc.
PROJECT : ZRJ
Size
Document Number
WPCE791 & FLASH
Rev 1A
Date: Saturday, January 22, 2011
Sheet 32 of 41

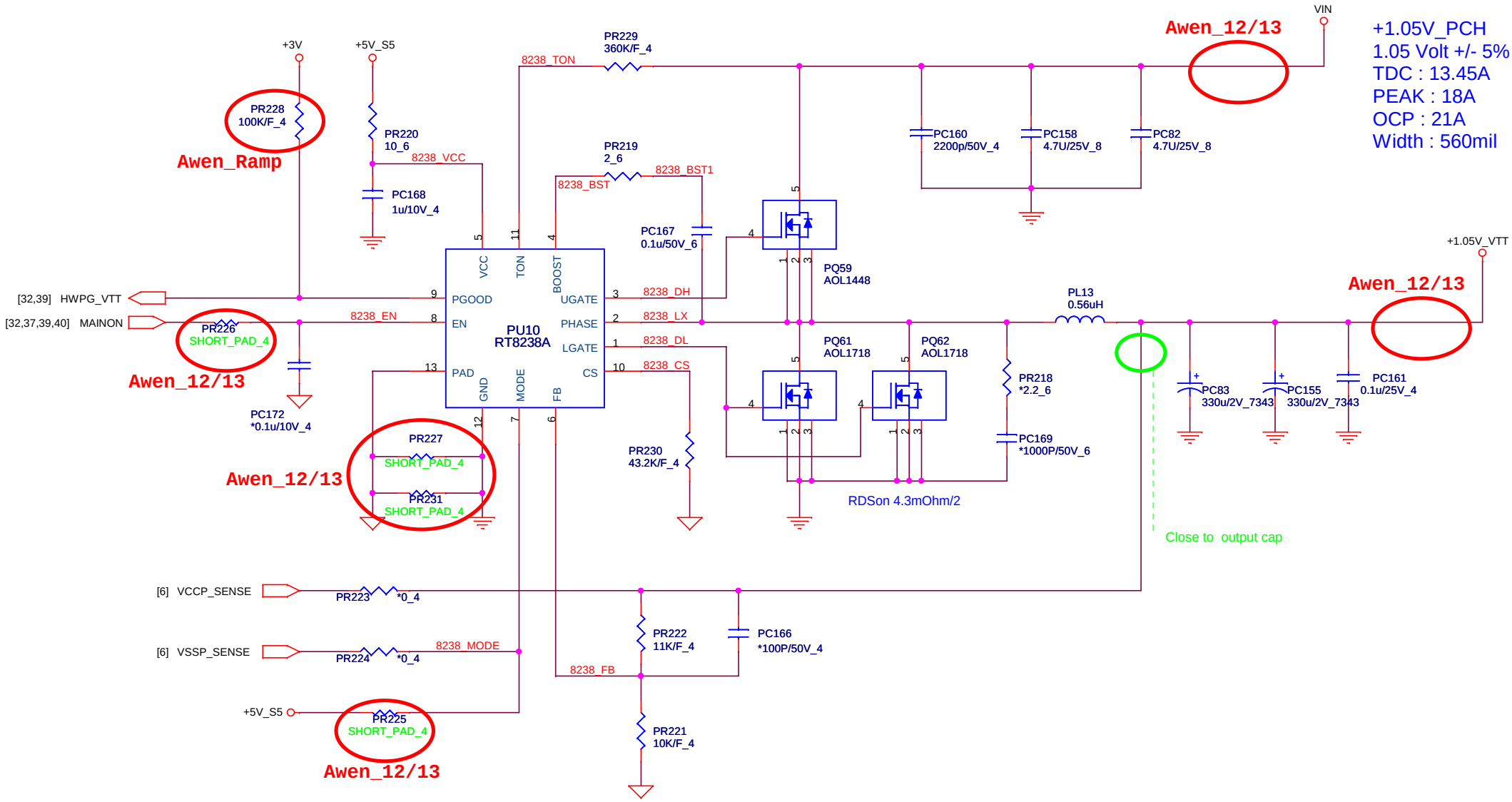

PJ2
20277-04XX-4P-L
PC18 0.1u/50V_6
PC19 2200p/50V_4
PL2 HI0805R800R-00_8
PL1 HI0805R800R-00_8
VA1
PC17 0.1u/50V_6
PD3 SBR1045SP5-13
PD7 SMAJ20A
PD1 SW1010CPT
VA2
PC20 0.1u/50V_6
PR22 220K_4
PR23 220K_4
PQ2 IMD2AT108
PQ23 FDD6685_G
0.01/F_3720 PR130
VIN
CSIP_1
PR24 SHORT_PAD_4
D/C# [32]
Awen_12/13
EC2 *22u/25V_1210
EC1 *22u/25V_1210
PC100 0.1u/50V_6
PC99 2200p/50V_4
PR18 33K/F_4
PQ20 FDD6685_G
PR17 10K_4
PQ1 DMN601K-7
PR20 10/F_4
PR19 10/F_4
PC13 0.1u/25V_4
PR16 4.7_6
PC14 1u/10V_4
PC11 1u/10V_4
ISL88731_VDDP
PD2 *RB500V-40
PC91 2200p/50V_4
PC93 4.7U/25V_8
+3VPCU
PC1 0.1u/25V_4
PR1 100K_4
[19,32] ACIN
[32] MBDATA
[32] MBCLK
PR14 49.9/F_6
DCIN
PC12 0.1u/50V_6
PR13 82.5K/F_4
88731ACSET
PR12 22K/F_4
PU2 ISL88731A
NC GND GND GND GND CSSP CSSN VCC VDDP
VDDSMB SDA SCL ACOK DCIN ACIN VREF ICOMP NC VCOMP
BOOT UGATE PHASE LGATE PGND CSOP CSON NC VBF GND
PR15 2.7_6
PC15 0.1u/50V_6
88731B_2
88731B_1
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
PQ22 AON7410
PQ21 AON7410
PL5 6.8uH
0.01/F_3720 PR129
BAT-V
PR21 *2.2_6
PC16 *2200P/50V_6
PC88 2200p/50V_4
PC90 10U/25V_1206
PC89 10U/25V_1206
CSOP_1
PR11 10/F_4
PC9 0.1u/25V_4
CSON
PR8 SHORT_PAD_4
PR10 10/F_4
Awen_12/13
PR7 100_4
PR6 2.21K/F_4
PC10 *1u/10V_4
PC8 0.01u/25V_4
PC7 *0.01u/25V_4
PC5 0.01u/25V_4
ICMNT
ICMNT [32]
ISL88731 thermal pad tie to Pin12
PC6 0.1u/50V_6
PC2 100p/50V_6
PL4 HI0805R800R-00_8
PL3 HI0805R800R-00_8
MBAT+
BAT-V
PJ1 C114F3-108A1-L_Batt_Conn
PR3 100_4
TEMP_MBAT
TEMP_MBAT [32]
PR9 100_4
PC4 47p/50V_6
PC3 47p/50V_6
PR2 SHORT_PAD_4
PR5 100_4
PR4 100_4
Awen_12/13
MBCLK [32]
MBDATA [32]
PU1 CM1293A-04SO
CH1 CH4 VN VP CH2 CH3
MBDATA
+3VPCU
MBCLK
TEMP_MBAT
Add ESD diode base on EC FAE suggestion
Quanta Computer Inc.
PROJECT : ZRJ
Size
Document Number
Charger (ISL88731)
Rev 1A
Date: Saturday, January 22, 2011
Sheet 33 of 41


MAIND
MAIND [6,37,40]
Awen_12/13
[4,41] SYS_SHDN#
PR216
SHORT_PAD_4
VL
VIN
PC92
100u/25V_6X5.8
PC159
4.7U/25V_8
PC163
2200p/50V_4
PR118
39K/F_4
3V5V_EN
PR215
SHORT_PAD_4
PR120
SHORT_PAD_4
5V_EN
3V_EN
+3VPCU
3.3 Volt +/- 5%
TDC : 6.5A
PEAK : 8.5A
OCP : 10A
Width : 260mil
PC157
2200p/50V_4
PC156
4.7U/25V_8
+5VPCU
5 Volt +/- 5%
TDC : 5.625A
PEAK : 7.5A
OCP : 9A
Width : 240mil
PR108
390K/F_4
PC150
0.1u/50V_6
PC151
4.7U/6.3V_6
PR107
SHORT_PAD_4
PR110
SHORT_PAD_4
PC153
1u/10V_4
PC154
0.01u/25V_4
PC152
0.1u/25V_4
8206_ONLDO
REF
PR109
*0_4
PR210
*0_4
PR106
150K/F_4
PQ55
AON7410
3V_DH
PQ57
AON7410
5V_DH
PL14
2.2uH
3V_LX
PL15
2.2uH
PR113
200K/F_4
REFIN2
PR117
162K/F_4
DDPWRGD_R
5V_EN
SKIP
3V_EN
PU9
RT8206M
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
LDOREFIN
LDO
VIN
NC
ONLDO
VCC
TON
REF
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
BST1
DVCC
NC
GND
PGND
DL2
BST2
PR111
*0_4
PR126
*2.2_6
PC84
*1000P/50V_6
PC165
330u/6.3V_7343
PC171
0.1u/25V_4
PR112
SHORT_PAD_4
PQ58
AON7702
5V_DL
PC80
0.1u/50V_6
PC81
0.1u/50V_6
PR124
1/F_6
PR122
1/F_6
PQ56
AON7702
PC79
*1000P/50V_6
PR214
SHORT_PAD_4
PR212
*0_4
PR114
*0_4
PR211
*0_4
PC173
0.1u/25V_4
PC170
330u/6.3V_7343
PR121
*2.2_6
+5VPCU_FB
PR217
*0_6
PC164
0.1u/50V_6
PD8
CHN217
PD6
CHN217
PC87
1u/25V_6
PC85
0.1u/50V_6
PC162
1u/10V_4
PR209
SHORT_PAD_4
PR208
SHORT_PAD_4
PR127
SHORT_PAD_6
PR115
*0_4
PR119
SHORT_PAD_4
+15V
+15V_ALWP
PR128
22_8
PC86
1u/25V_6
PR125
*200K/F_4
PR123
*39K/F_4
PR213
*100K/F_4
PR116
SHORT_PAD_4
SYS_HWPG [32]
OCP:9A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
~2.525A
Iocp=7-(2.525/2)=5.74
Vth=5.74*14.2mohm=0.081V
R(ILM)=0.8147*10/5uA=162.941K
OCP:10A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*19)
~1.9A
Iocp=8-(1.9/2)=7.05A
Vth=7.05*14.2mohm=0.10011V
R(ILM)=0.10011*10/5uA=200.22K
[32,41] S5_ON
PR205
1M_4
PR202
22_8
PR203
22_8
PR204
1M_4
PR207
*1M_6
S5D
PQ54
DTC144EUA
PR206
1M_4
PQ51
DMN601K-7
PQ52
DMN601K-7
PQ53
DMN601K-7
PC149
*2200p/50V_4
PQ63
AO3404
+5V_S5
PQ64
AO4468
+5V
PQ60
AO4468
+3V
PQ65
AO3404
+3V_S5
TDC : 1.5A
PEAK : 2A
Width : 60mil
TDC : 3.38A
PEAK : 4.5A
Width : 140mil
TDC : 4.05A
PEAK : 5.4A
Width : 160mil
TDC : 0.3A
PEAK : 0.4A
Width : 20mil
ter Inc.
Rev
1A
of 41



	UMA (IV@) / Muxless (MS@)	External VGA (EV@)
PR196	NC	Populated
PR85	100K/F_4 (CS41002FB28)	200K/F_4 (CS42002FB12)
PR82	130K/F_4 (CS41302FB00)	NC
PR184	158K/F_4 (CS41582FB14)	NC
PR182	5.62K/F_4 (CS25622FB18)	1K/F_4 (CS21002FB24)
PR99	Populated	NC
PR198	Populated	NC

Quanta Computer Inc.
PROJECT : ZRJ
Size | Document Number: +VCC_CORE (MAX17511)) | Rev: 1A
Date: Saturday, January 22, 2011 | Sheet 35 of 41


+1.05V_PCH
1.05 Volt +/- 5%
TDC : 13.45A
PEAK : 18A
OCP : 21A
Width : 560mil
VIN
+3V
+5V_S5
+1.05V_VTT
PR228 100K/F_4
PR220 10_6
PR229 360K/F_4
PR219 2_6
PC168 1u/10V_4
PC167 0.1u/50V_6
PC160 2200p/50V_4
PC158 4.7U/25V_8
PC82 4.7U/25V_8
PU10 RT8238A
VCC
TON
BOOST
PGOOD
UGATE
EN
PHASE
LGATE
PAD
GND
MODE
FB
CS
8238_TON
8238_VCC
8238_BST
8238_BST1
8238_DH
8238_LX
8238_DL
8238_CS
8238_EN
8238_MODE
8238_FB
[32,39] HWPG_VTT
[32,37,39,40] MAINON
PR226 SHORT_PAD_4
PC172 *0.1u/10V_4
PR227 SHORT_PAD_4
PR231 SHORT_PAD_4
PR230 43.2K/F_4
PQ59 AOL1448
PQ61 AOL1718
PQ62 AOL1718
PL13 0.56uH
PR218 *2.2_6
PC169 *1000P/50V_6
PC83 330u/2V_7343
PC155 330u/2V_7343
PC161 0.1u/25V_4
RDSon 4.3mOhm/2
Close to output cap
[6] VCCP_SENSE
[6] VSSP_SENSE
PR223 *0_4
PR224 *0_4
PR222 11K/F_4
PC166 *100P/50V_4
PR221 10K/F_4
PR225 SHORT_PAD_4
Awen_Ramp
Awen_12/13
Awen_12/13
Awen_12/13
Awen_12/13
Awen_12/13
Current limit =10uA*Rth/RDSon
VOUT=(1+R1/R2)*0.5
Quanta Computer Inc.
PROJECT : ZRJ
Size
Document Number
+PCH&VTT (RT8238A)
Rev 1A
Date: Saturday, January 22, 2011
Sheet 36 of 41

[PWM]

+0.75V_DDR_VTT
0.75 Volt +/- 5%
TDC : 0.75A
PEAK : 1A
Width : 40mil

SMDDR_VREF
0.75 Volt +/- 5%
TDC : 0.375A
PEAK : 0.5A
Width : 10mil

+1.5V_SUS
1.5 Volt +/- 5%
TDC : 13.79A
PEAK : 18.4A
OCP : 20A
Width : 560mil

+1.5V
1.5 Volt +/- 5%
TDC : 0.38A
PEAK : 0.5A
Width : 25mil

RT8207L
PU6

Awen_12/13

Awen_Ramp

(For RT8207A 400KHZ) close to pc2008

Vout = (PR150/PR149) X 0.75 + 0.75

L(ripple current)
=(9-1.5)*1.5/(2.2u*400k*9)
~1.42A
Vtrip= (15-0.71)*4.3mohm=0.06145V
RILIM=Vtrip/10u=6.144K

	S3	S5	+1.5V_SUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZRJ

Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A

Date: Saturday, January 22, 2011 Sheet 37 of 41

NV VID Table for N12P-GV

GPU_VID1	GPU_VID2	GPU_VID3	+VGPU_CORE
0	0	0	1.025V
1	0	0	1
0	1	0	0.9V
1	1	1	0.85V(Boot)

N12P-GV resister change table

R1	32.4K	CS33242FB19
R2	19.1K	CS31912FB15
R3	487K	CS44872FB19
R4	86.6K	CS38662FB16
R5	267K	CS42672FB16

Awen_12/13

+VGPU_CORE
1 Volt +/- 5%
TDC : 24A
PEAK : 31.5A
OCP : 35.8A
Width : 1320mil

VIN

+5V_S5

+3V

+VGPU_CORE

PR40 EV@100K/F_4
PC36 EV@1u/10V_4
8117_VDDA
PR48 EV@22_6
PC30 EV@1u/10V_4
PD5 EV@RB500V-40
8117_BST1
PR54 EV@1/F_6
PC28 EV@0.01u/25V_4
PR44 EV@10K_4

PC111 EV@2200p/50V_4
PC110 EV@4.7u/25V_8
PC44 EV@4.7u/25V_8
PC45 EV@4.7u/25V_8

[40] VGA_PG
[11,32,40] dGPU_VRON
+3V_GPU
PR51 *0_4
PR49 *100K/F_4
PR47 EV@1_4

PU4
EV@OZ8117

VIN, VDDA, VDDP, PG, ON/SKIP, G0, G1, VSET2, VSET1, VREF, TSET, GNDA, BST, HDR, LX, LDR, GNDP, CSP, CSN, RSP, RSN

8117_EN
8117_VREF
8117_TEST
8117_BST
8117_DH
8117_LX
8117_DL
8117_CSP
8117_CSN
8117_RSP
8117_RSN

PC33 EV@0.1u/50V_6

PQ33 EV@AOL1448
PQ34 EV@AOL1448
PQ32 EV@AOL1718
PQ31 EV@AOL1718

PL7 EV@0.68uH_13X13X5

Close to Phase 1 Inductor

PR159 EV@2.2_6
PR158 EV@20K/F_4
PR161 EV@10K_6_NTC
PR160 EV@20K/F_4
PC109 EV@1000p/50V_6
PC38 EV@33n/25V_4
PR64 EV@51.1/F_6
PC39 EV@0.1u/25V_4
PC42 EV@330u/2V_7343
PC41 EV@470u/2V_7343
PC43 EV@330u/2V_7343

Awen_12/16
PR61 EV@1.2K/F_4
PC40 EV@1000p/50V_4
PC37 EV@22p/50V_4
PR62 10_4
PR63 EV@10/F_6
PR53 EV@10/F_6
PR52 10_4
Awen_12/18

R3
PR36 SP@365K/F_4
VREF=2.75V
R1
PR37 EV@32.4K/F_4
R2
PR38 SP@18.7K/F_4
PR32 EV@1_4
PR39 EV@200K/F_4
PC25 EV@1000p/50V_4
PC29 EV@0.1u/25V_4
PC34 EV@0.01u/50V_4
PC32 EV@0.01u/50V_4

PR30 SHORT_PAD_4
PR29 SHORT_PAD_4

R4
PR35 SP@100K/F_4
R5
PR34 SP@174K/F_4

[19] GPU_VID1
PQ5 EV@DMN601K-7
PR27 EV@10K_4
PC22 EV@0.01u/25V_4

[19] GPU_VID2
PQ4 EV@DMN601K-7
PR26 EV@10K_4
PC23 EV@0.01u/25V_4

[19] GPU_VID3
PQ9 EV@DMN601K-7
PR41 EV@10K_4
PC26 EV@0.01u/16V_4

PR31 EV@1M_4
PR43 EV@22_8
PR33 EV@1M_4
PQ10 EV@DTC144EUA
PQ8 EV@DMN601K-7

NV VID Table for N12P-GS

GPU_VID1	GPU_VID2	GPU_VID3	+VGPU_CORE
0	0	0	1.00V
1	0	0	0.975V(Boot)
0	1	0	0.9V
1	1	1	0.825V

Quanta Computer Inc.
PROJECT : ZRJ

Size	Document Number	Rev
	GPU CORE(OZ8117)	1A
Date: Saturday, January 22, 2011	Sheet 38 of 41	

VID0	VID1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

VCCSA
0.9 Volt +/- 5%
TDC : 4.5A
PEAK : 6A
Width : 240mil

+3V
Awen_12/13
PC119 0.1u/25V_4
PC46 10u/10V_8
PC120 10u/10V_8
+5V_S5
PC124 2.2u/10V_6
PR170 SHORT_PAD_6
Awen_Ramp
Awen_12/13
PR172 *100K/F_4
PC123 1u/10V_4
51461_FILT
[32] HWPG_VCCSA
[32,36] HWPG_VTT
Awen_12/13
PR174 SHORT_PAD_4
PC122 *0.1u/25V_4
51461_EN
[6] VCCSA_SEL
TPS51461 PU7
VIN VIN VIN PGND PGND PGND
V5DRV V5FILT PGOOD EN VID0 VID1 AGND
BST SW SW SW SW SW SW
51461_BST
51461_SW
PC121 0.1u/50V_6
PL8 1uH_7X7X3
VCCSA
Awen_12/13
PC113 330u/2V_7343
PC118 0.1u/25V_4
PR166 100_4
Awen_12/13
PR162 SHORT_PAD_4
PR163 SHORT_PAD_4
PR173 1K_4
MODE GND VREF COMP SLEW VOUT
51461_MODE 51461_VREF 51461_SLEW
PR164 4.99K/F_4
PR167 *0_4
PC114 0.22u/25V_6
PC112 3.3n/50V_4
PC116 0.01u/25V_4
51461_VOUT
PR165 SHORT_PAD_4
VCCSA_SENSE [6]
Awen_12/13

VCCSA_SEL	VCCSA
1	0.8V
0	0.9V

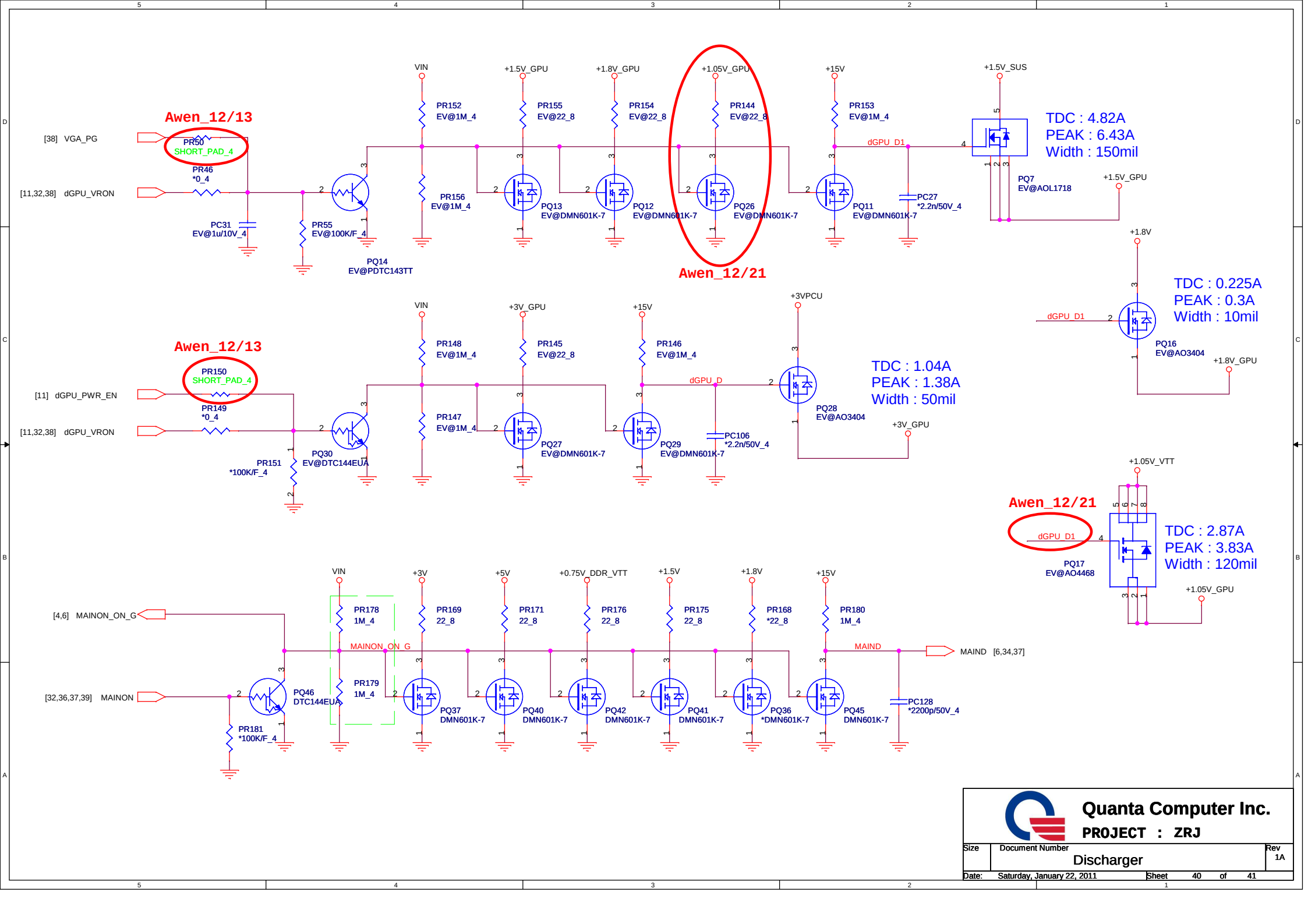
default 0.9V

+1.8V
1.8 Volt +/- 5%
TDC : 1.54A
PEAK : 2.05A
Width : 70mil

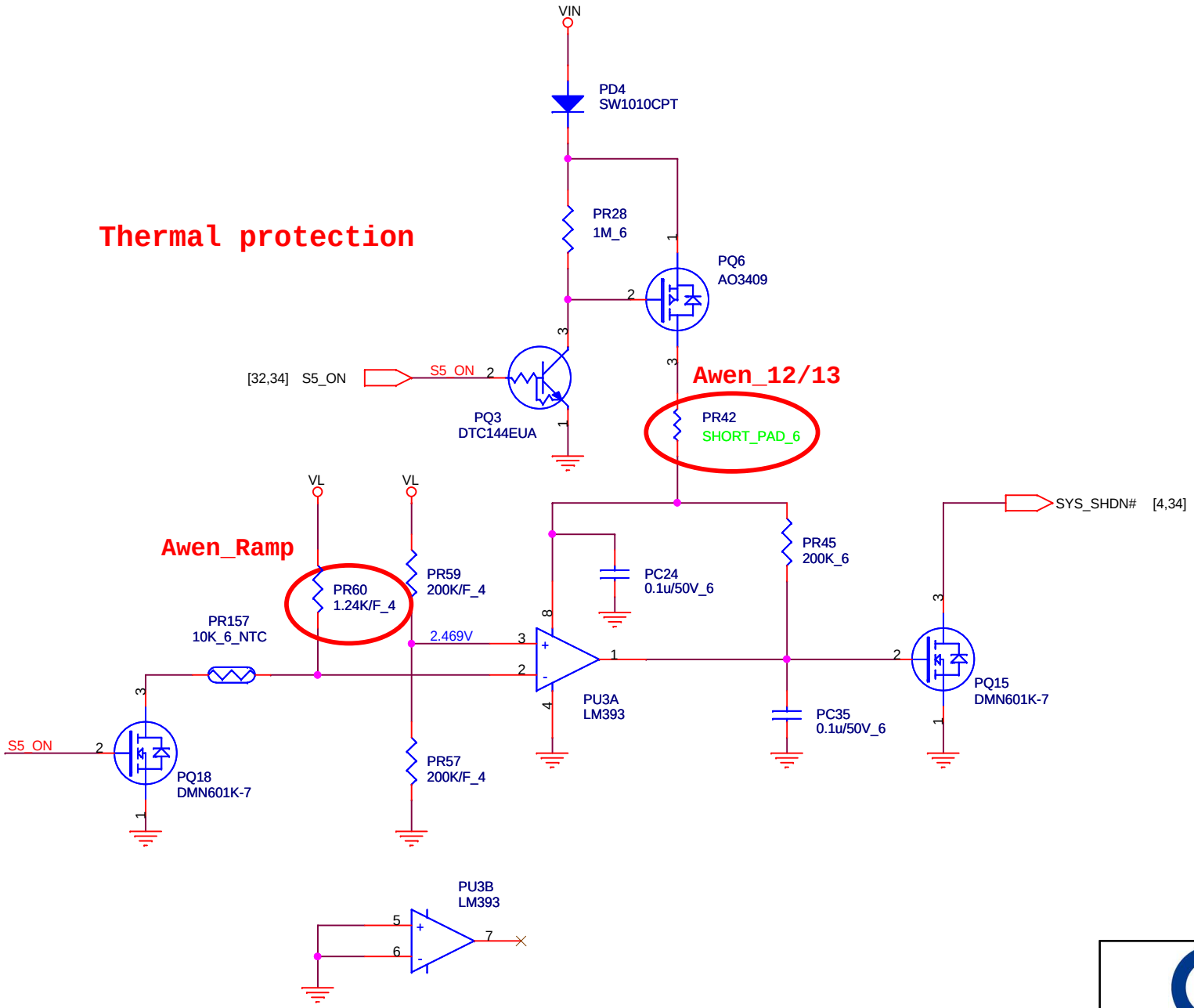
+3VPCU
Awen_12/13
PC76 10u/10V_8
PC148 0.1u/10V_4
PU8 HPA0835RTER
VIN VIN VIN EN VSNS COMP RT/CLK SS
PH PH PH BOOT PWRGD GND GND AGND
835_PH
Awen_12/13
PR104 SHORT_PAD_6
PC74 0.1u/50V_6
PL12 1uH_7X7X3
+1.8V
Awen_12/13
MAINON
PR201 SHORT_PAD_4
835_EN
54418-1.8_VFB
835_COMP
835_RTCLK
835_SS
PR105 *100K/F_4
PC78 1000p/50V_4
PR100 8.06K/F_4
PR103 182K/F_4
PC72 *100P/50V_4
PC75 0.01u/25V_4
PC71 2700p/50V_4
HWPG_1.8V [32]
PR200 *100K/F_4
+3V
Awen_Ramp
R1
R2
PR101 100K/F_4
PR102 78.7K/F_4
PC70 0.1u/10V_4
PC73 10u/10V_8
PC77 10u/10V_8
V0=0.8*(R1+R2)/R2
MAINON
MAINON [32,36,37,40]

Quanta Computer Inc.
PROJECT : ZRJ

Size	Document Number	Rev
	VCCSA(TPS51461)/+1.8V(HPA00835)	1A
Date: Saturday, January 22, 2011	Sheet 39 of 41	


Awen_12/13
[38] VGA_PG
PR50
SHORT_PAD_4
PR46
*0_4
[11,32,38] dGPU_VRON
PC31
EV@1u/10V_4
PR55
EV@100K/F_4
PQ14
EV@PDTC143TT
VIN
PR152
EV@1M_4
PR156
EV@1M_4
+1.5V_GPU
PR155
EV@22_8
PQ13
EV@DMN601K-7
+1.8V_GPU
PR154
EV@22_8
PQ12
EV@DMN601K-7
+1.05V_GPU
PR144
EV@22_8
PQ26
EV@DMN601K-7
Awen_12/21
+15V
PR153
EV@1M_4
PQ11
EV@DMN601K-7
dGPU_D1
PC27
*2.2n/50V_4
+1.5V_SUS
PQ7
EV@AOL1718
+1.5V_GPU
TDC : 4.82A
PEAK : 6.43A
Width : 150mil
Awen_12/13
[11] dGPU_PWR_EN
PR150
SHORT_PAD_4
PR149
*0_4
[11,32,38] dGPU_VRON
PR151
*100K/F_4
PQ30
EV@DTC144EUA
VIN
PR148
EV@1M_4
PR147
EV@1M_4
+3V_GPU
PR145
EV@22_8
PQ27
EV@DMN601K-7
+15V
PR146
EV@1M_4
dGPU_D
PQ29
EV@DMN601K-7
PC106
*2.2n/50V_4
+3VPCU
PQ28
EV@AO3404
+3V_GPU
TDC : 1.04A
PEAK : 1.38A
Width : 50mil
+1.8V
dGPU_D1
PQ16
EV@AO3404
+1.8V_GPU
TDC : 0.225A
PEAK : 0.3A
Width : 10mil
+1.05V_VTT
Awen_12/21
dGPU_D1
PQ17
EV@AO4468
+1.05V_GPU
TDC : 2.87A
PEAK : 3.83A
Width : 120mil
[4,6] MAINON_ON_G
[32,36,37,39] MAINON
PQ46
DTC144EUA
PR181
*100K/F_4
VIN
PR178
1M_4
PR179
1M_4
MAINON_ON_G
+3V
PR169
22_8
PQ37
DMN601K-7
+5V
PR171
22_8
PQ40
DMN601K-7
+0.75V_DDR_VTT
PR176
22_8
PQ42
DMN601K-7
+1.5V
PR175
22_8
PQ41
DMN601K-7
+1.8V
PR168
*22_8
PQ36
*DMN601K-7
+15V
PR180
1M_4
PQ45
DMN601K-7
MAIND
PC128
*2200p/50V_4
MAIND [6,34,37]
Quanta Computer Inc.
PROJECT : ZRJ
Size
Document Number
Discharger
Rev
1A
Date: Saturday, January 22, 2011
Sheet 40 of 41

Thermal protection



For EC control thermal protection (output 3.3V)

Quanta Computer Inc.		
PROJECT : ZRJ		
Size	Document Number: Thermal protect	Rev: 1A
Date: Saturday, January 22, 2011	Sheet 41 of 41	

Model	REV	CHANGE LIST
ZRJ MB	1A	FIRST RELEASED
	2A	Page 9 : U27 Change footprint Page 12 : R244 ,R260 & R526 Change to short pad. Page 12 : Add C743 Page 19 : Remove R116 ,R117 & R118 Page 19 : GPU1.K3 Change to EV_LVDS_BRIGHT & GPU1.H3 Change to EV_LVDS_VDDEN Page 23 : D4 & D18 Change footprint Page 26 : CN12.45 ,47 & 49 modify PIN name from *_WLN to *_3G Page 30 : CN17 Change footprint Page 31 : Led6 & Led8 change pin define. Page 31 : Led8 change form +3V_S5 to +3VPCU Page 32 : U23 Change footprint. Page 38 : PR47 PU Change to +3V_GPU Page All : Remove 0 ohm Location : R121 ,R406 ,R405 ,R20 & R273 Page All : Change from 0 ohm to short pad Location : R468 ,R428 ,R475 ,R474 ,R424 ,R429 ,R409 ,R178 ,R168 ,L13 ,R195 ,R236 ,R253 ,R259 ,R359 ,R521 ,R61 ,R223 ,R247 ,R210 ,R133 ,R395 ,R396 ,R496 ,R162 ,R164 ,R43 ,L14 ,L15 ,R234 ,R256 ,R261 ,R295 ,R346 ,R363 ,R524 ,R525 ,R528 ,R537 ,R540 ,R586 ,R587 ,R248 ,R596 ,R533 ,R529 ,R536 ,R233 ,R519 ,R490 ,R491 ,R350 ,R242 ,R243 ,R266 ,R345 & R288
	2B	Page 26 : Add R606 , R607 Page 27 : (1) F2 Change to short pad. (2) Add R241(Short pad) Page 28 : Add net : MUTE_LED in U19.47 Page 30 : (1) Add Q14 & R660 (2) Del. Q44 & R223 (3) Change CN18.5 connect to +3V(originally : USB_OC1) (4) Change CN18.6 connect to 3G_LED(originally : USB_OC0) Page 31 : (1) Add LDO (Location : U30) (2) Change CN26 (FP pin define) (3) Add R273 & R260 Page 32 : Del. T28
	3A	Page 31 : (1) C751 & C752 Change from 0805 to 0603 (2) Remove R385 & R386 Page 38 : (1) PC42 replace C747
	3C	

MODEL	ZRJ	
	FROM	To
	X	1A
	X	1A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B

DOC NO.	PROJECT MODEL :	ZRJ	APPROVED BY:		DATE:	2009/05/??
	PART NUMBER:		DRAWING BY:		REVISON:	1A