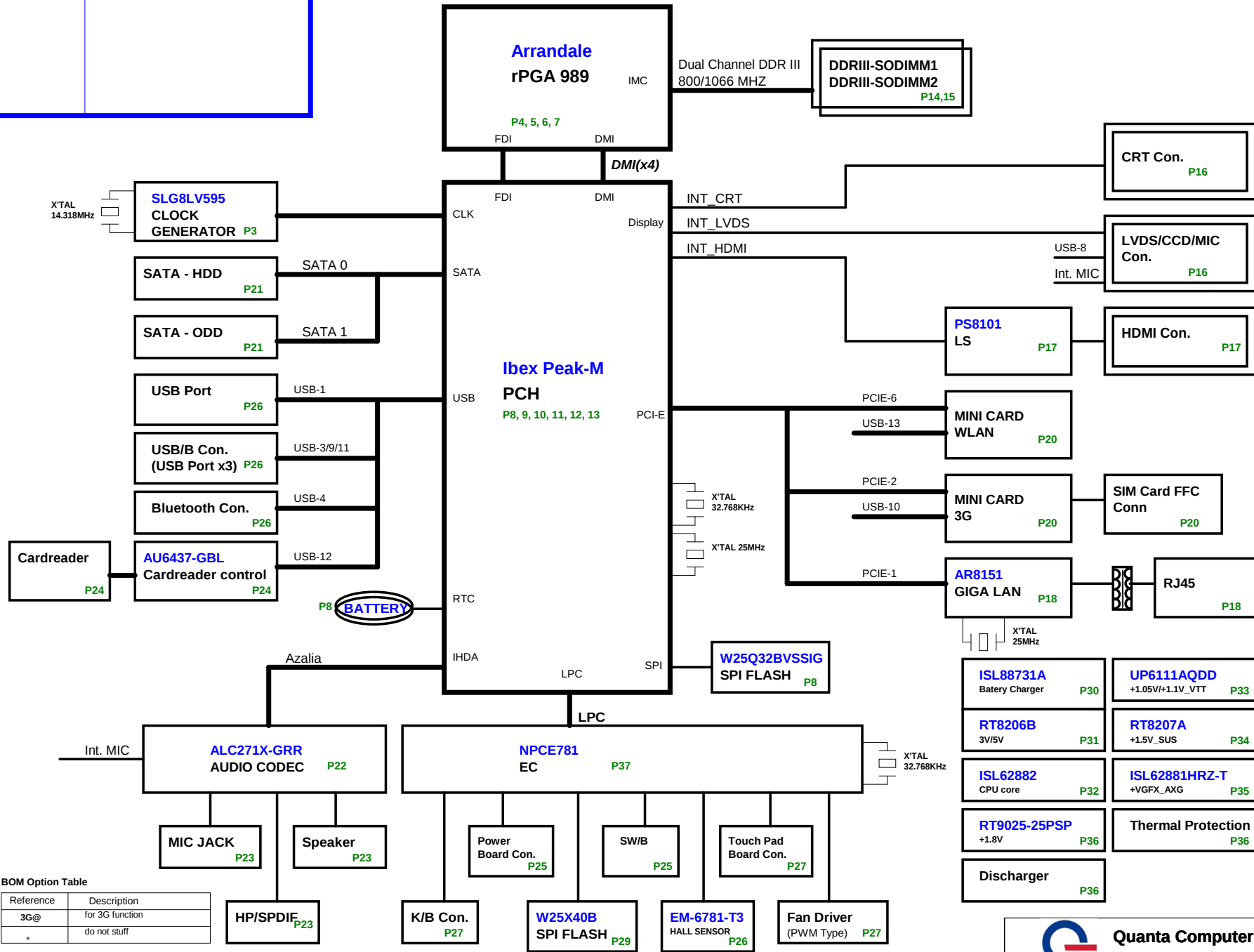


VER : 1A

ZR7U SYSTEM BLOCK DIAGRAM

BOM P/N	Description

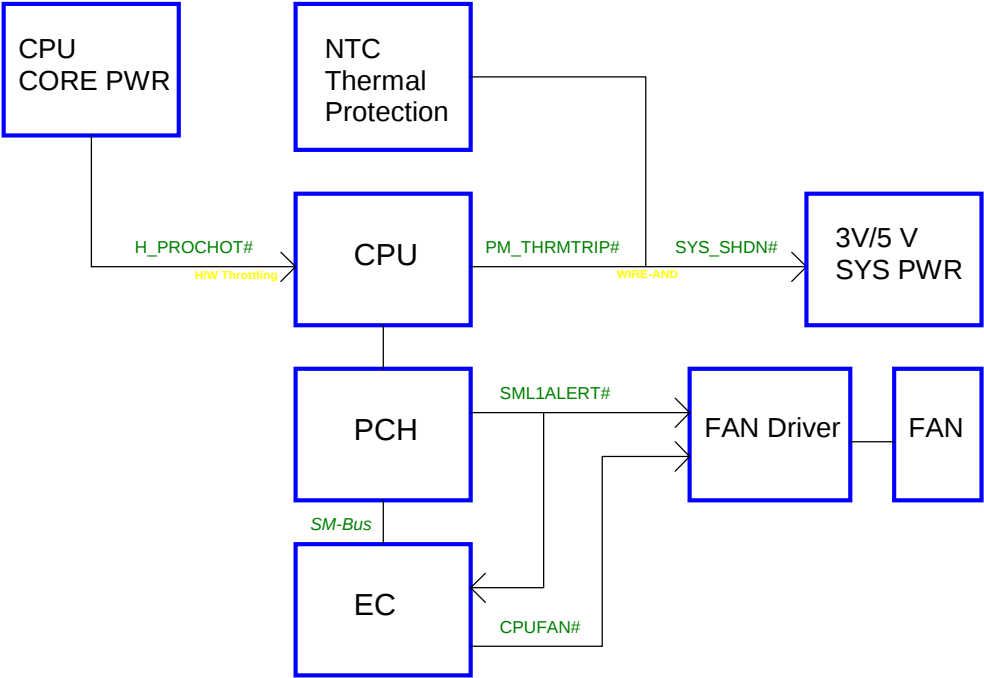


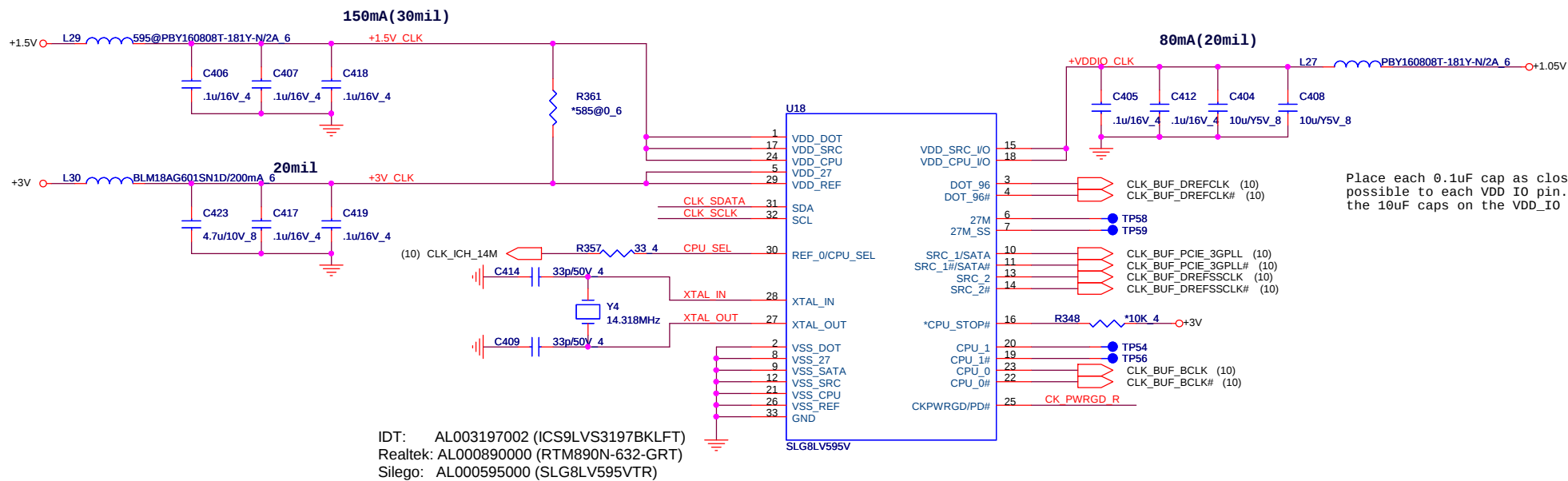
BOM Option Table

Reference	Description
3G@	for 3G function
*	do not stuff

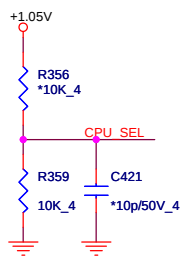
Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0



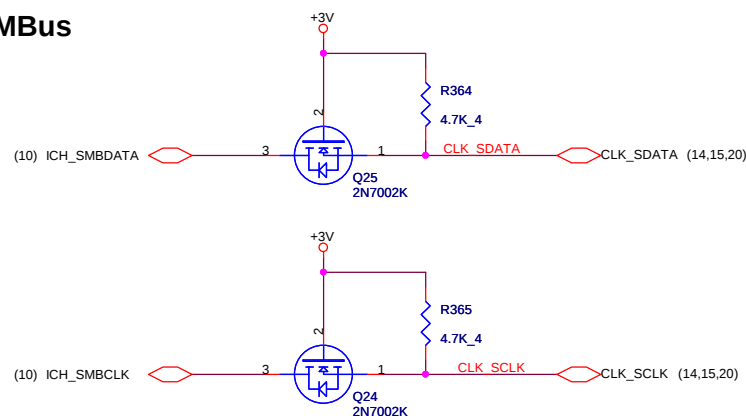


CPU_CLK select

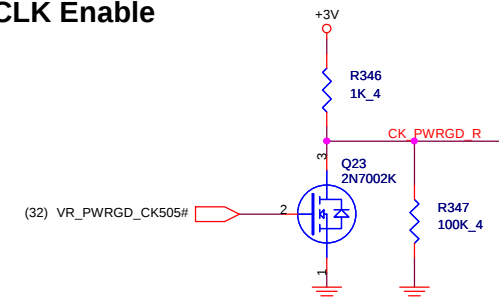


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



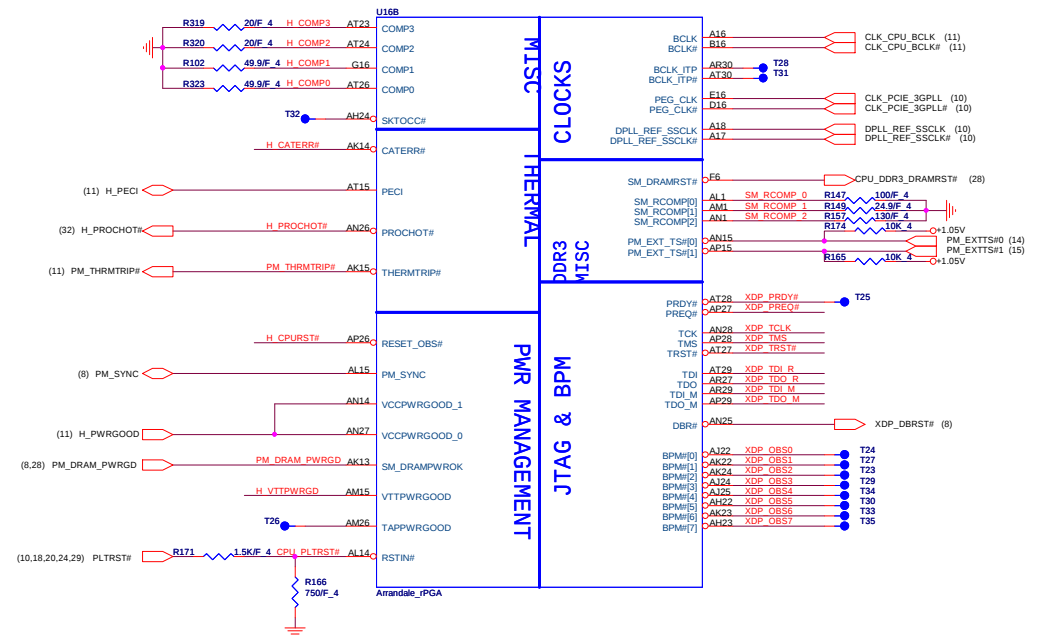
CLK Enable



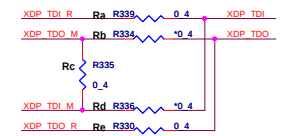
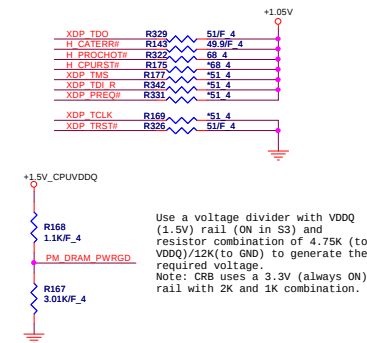
Quanta Computer Inc.
PROJECT : ZR7U

Size	Document Number	Rev
	Clock Generator	1A
Date:	Tuesday, April 20, 2010	Sheet 3 of 38

AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



JTAG MAPPING



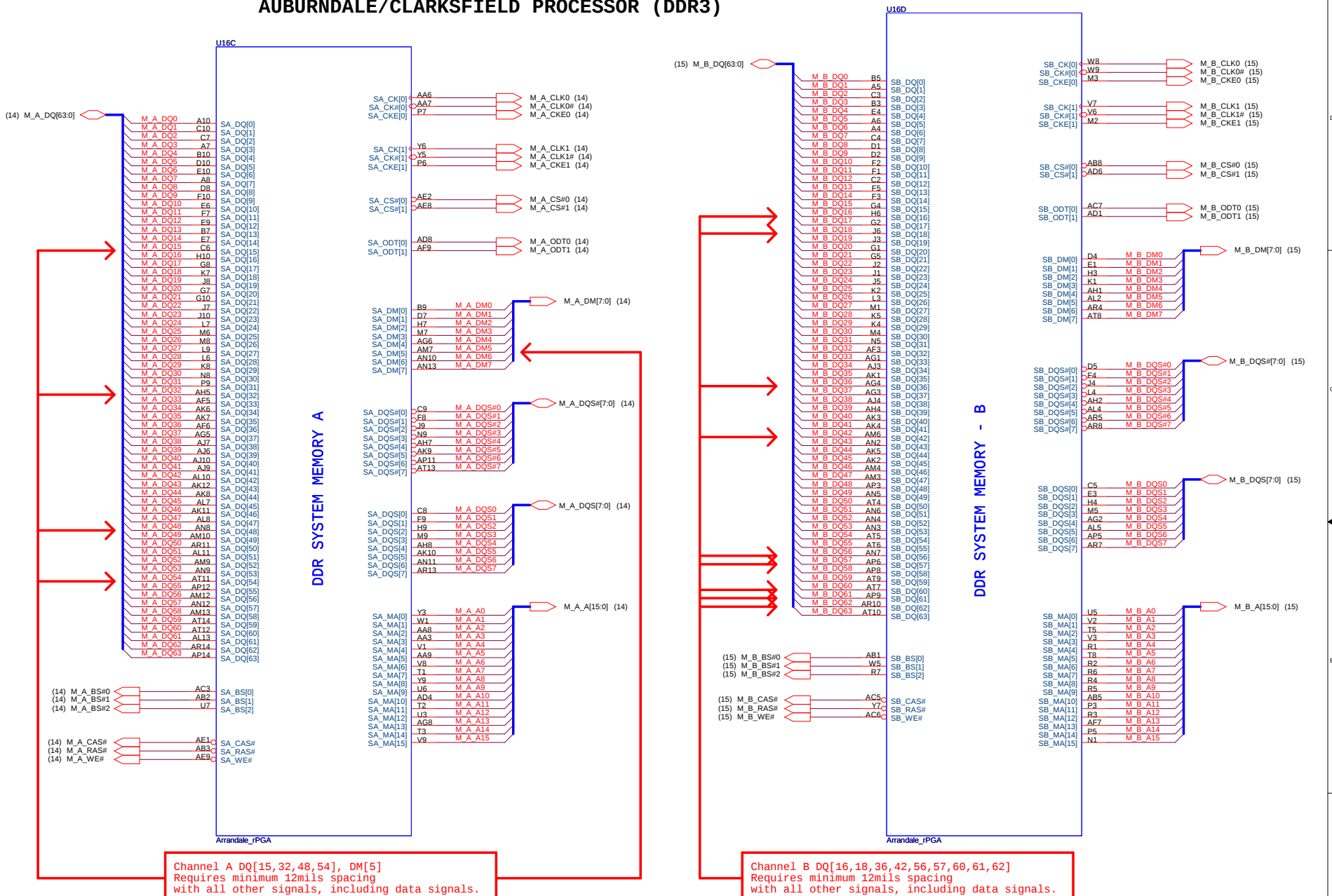
Scan Chain (Default)	STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only	STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only	STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc



Quanta Computer Inc.
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Size	Document Number AUBURNDA 1/4	Rev 1A
Date:	Tuesday, April 20, 2010	Sheet 4 of 38

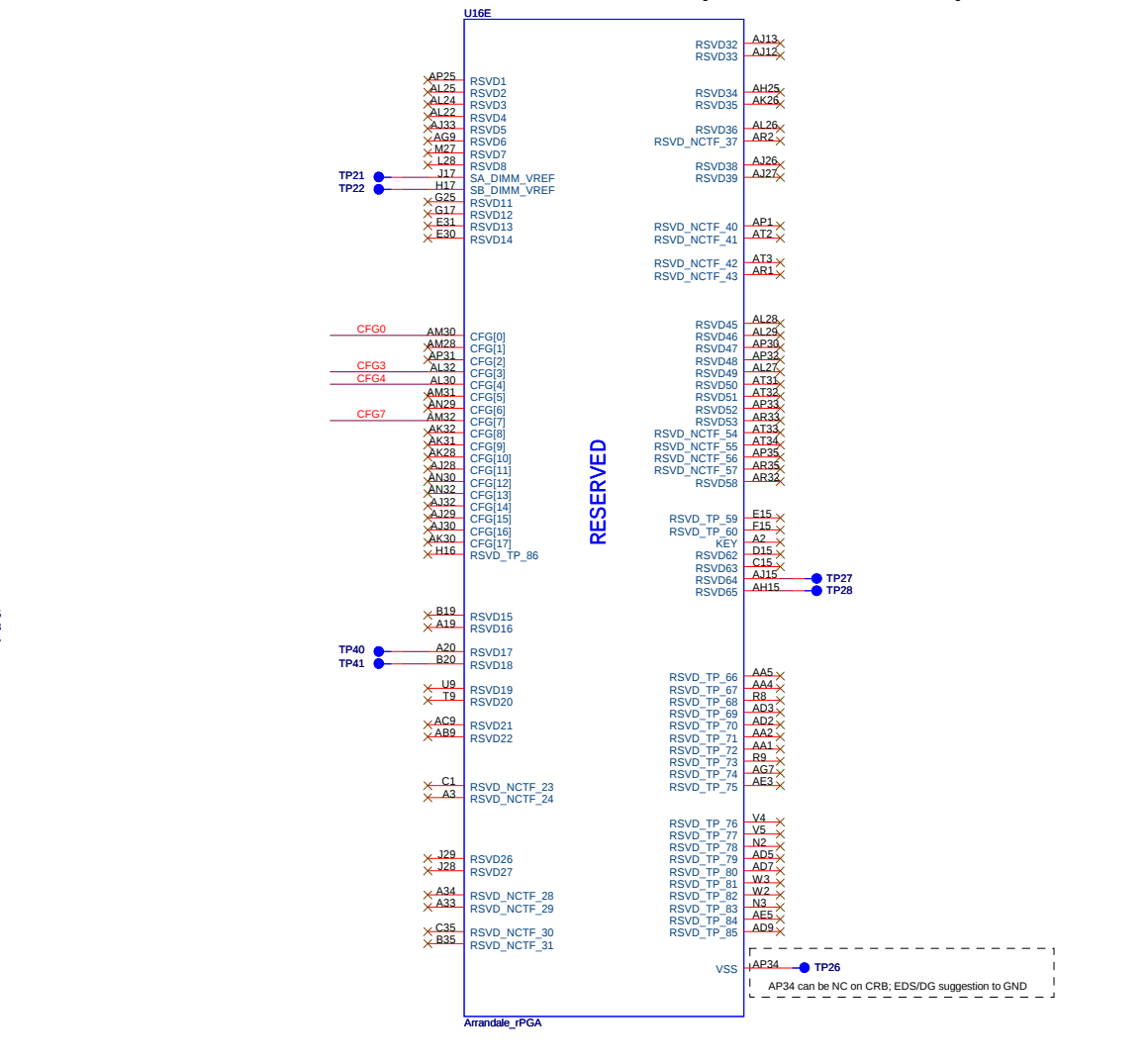
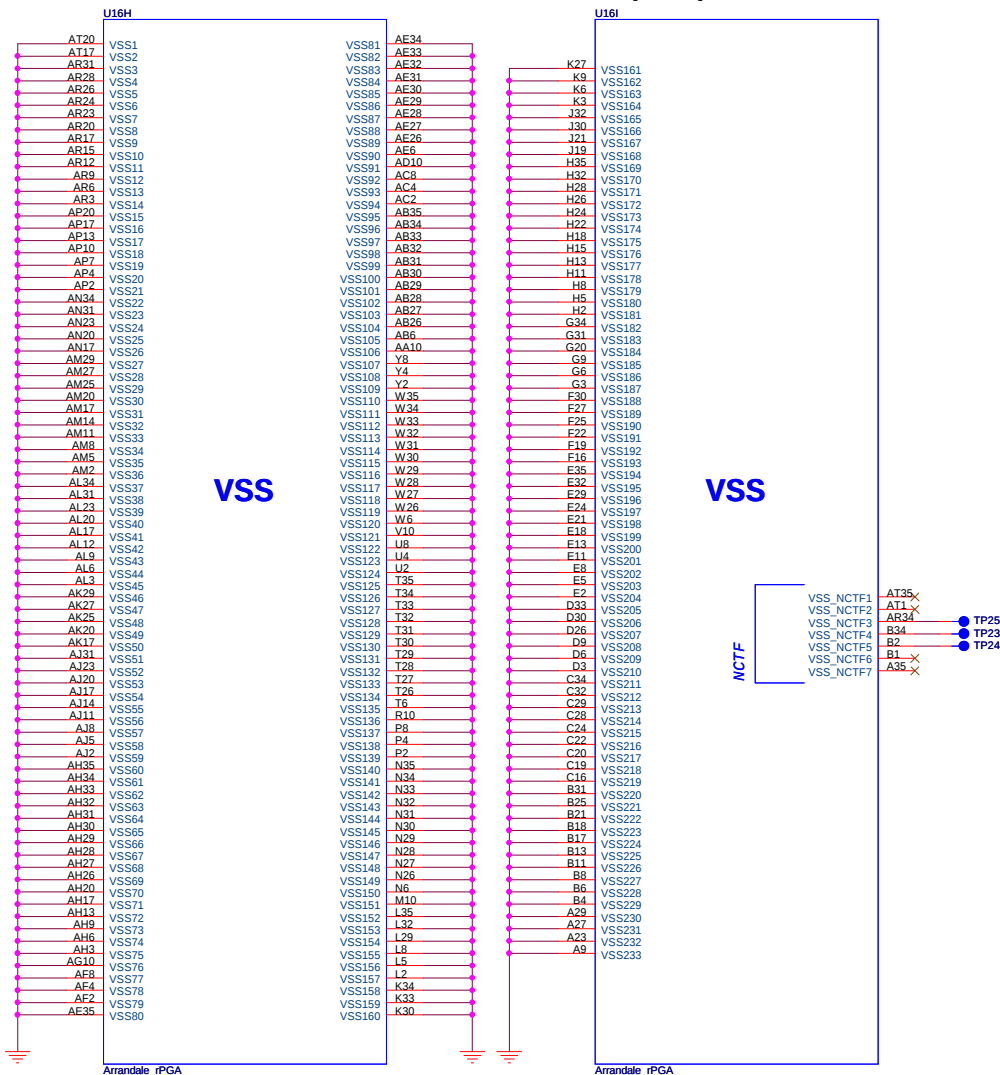
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Size	Document Number AUBURND 3/4 (PWR)	Rev 1A
Date	Tuesday, April 20, 2010	Sheet 6 of 38

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

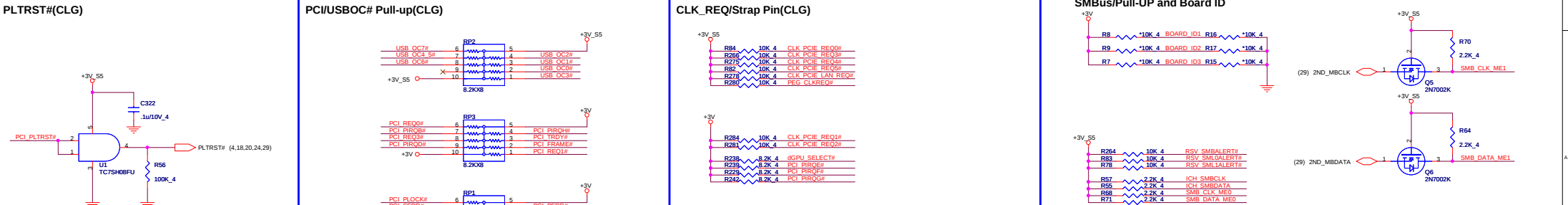
AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



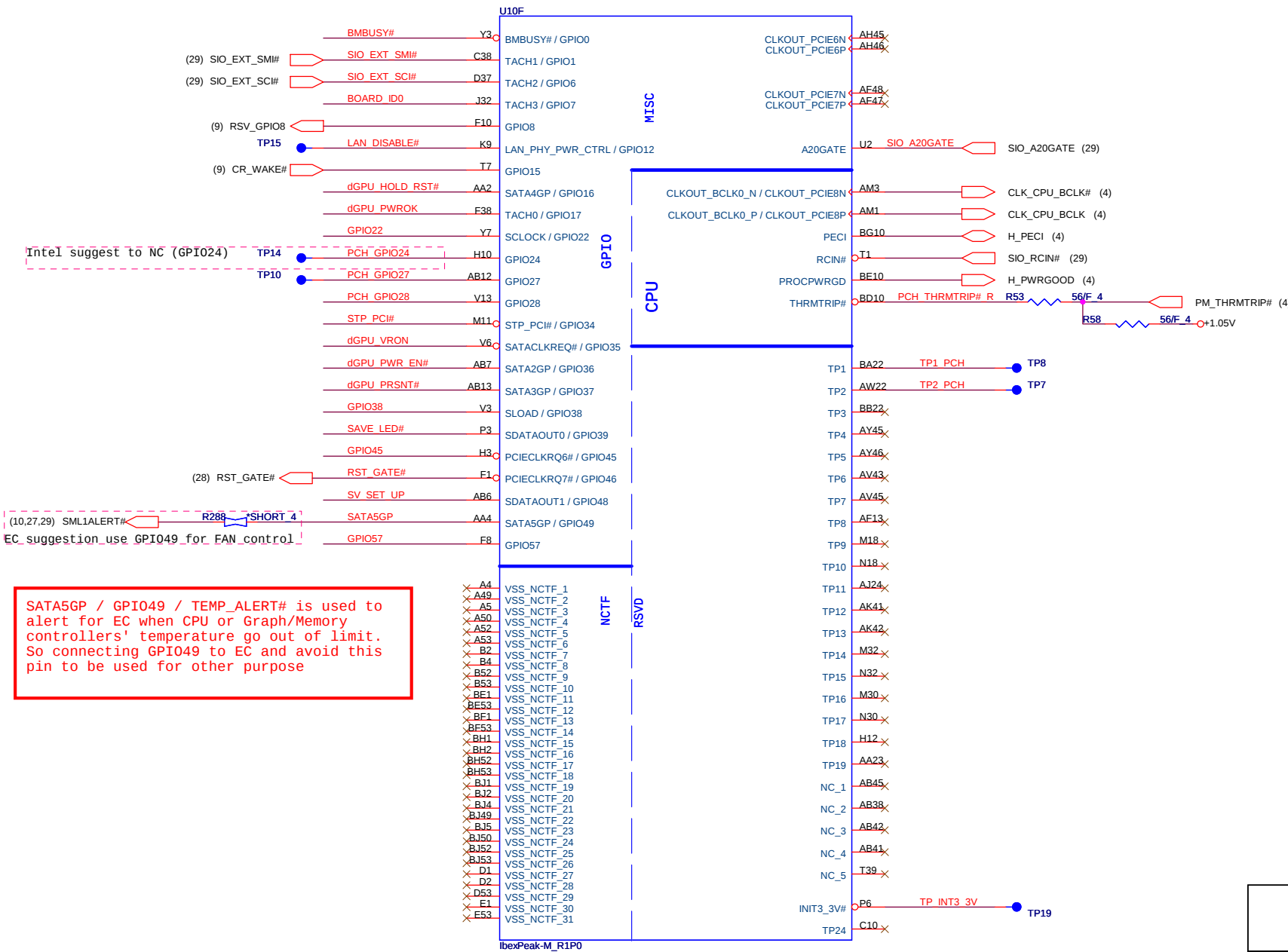
Processor Strapping

	1	0	DEFAULT	
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	No use	CFG0 R172 *3.01K/F 4
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	No use	CFG3 R156 *3.01K/F 4
CFG4 (Embedded Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port	No use	CFG4 R148 *3.01K/F 4
T A b e t p b p c				CFG7 R158 *3.01K/F 4

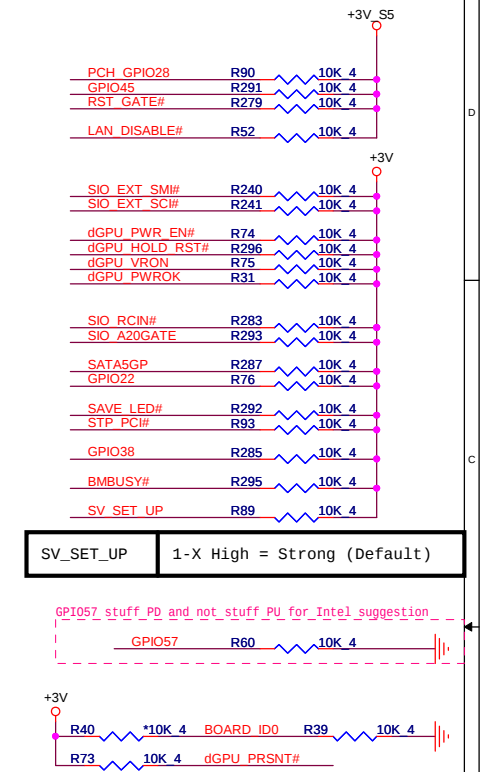
IBEX PEAK-M (PCI-E, SMBUS, CLK)



IBEX PEAK-M (GPIO, VSS_NCTF, RSVD)



GPIO Pull-up/Pull-down(CLG)



SV_SET_UP	1-X High = Strong (Default)
-----------	-----------------------------

GPIO57 stuff PD and not stuff PU for Intel suggestion

BOARD_ID0	High = JV41/JM41 Low = JM51
RSV_GPIO8	High = Disable Low = Enable



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Size	Document Number	Rev
	IBEX PEAK-M 4/6	1A
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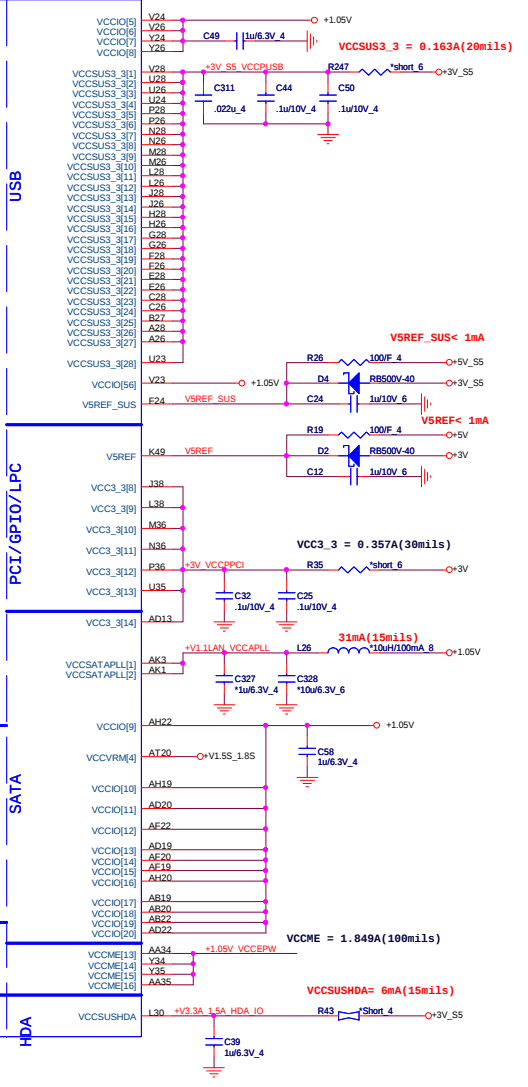
VCCCORE(+1.05V) = 1.432A(80mils)

VCCADA
VCCADA
VSSA_DA
VSSA_DA

VCCAL
VSSA_L



VCC[Q5] V24 +1.05V



37mA(15mils)

+1.05V

L25

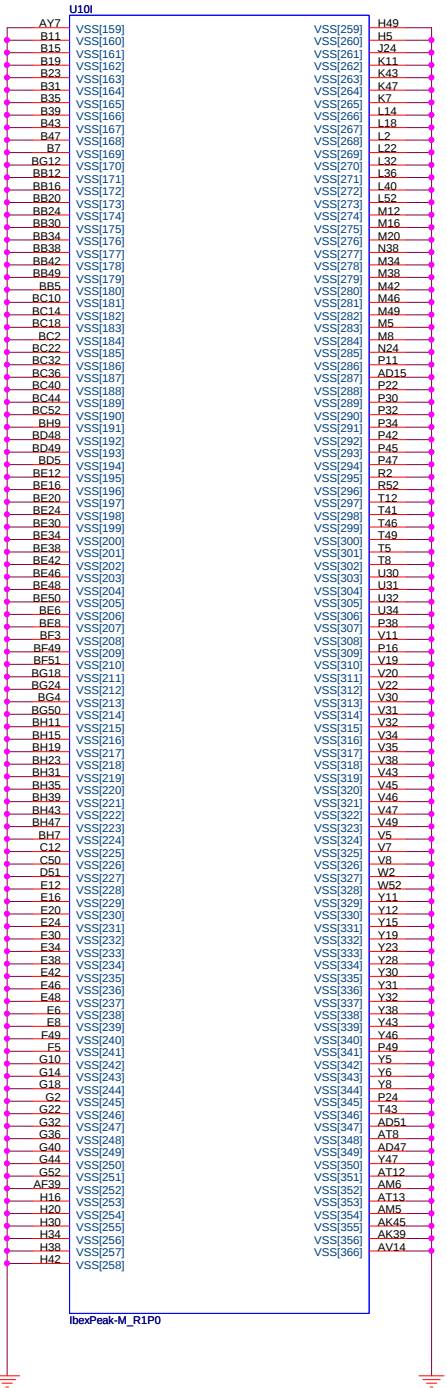
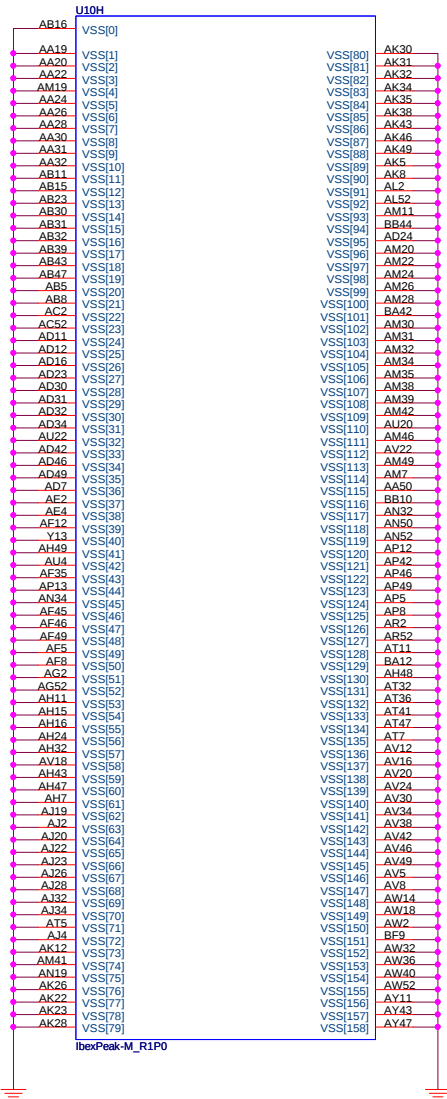
1uH/25mA 6

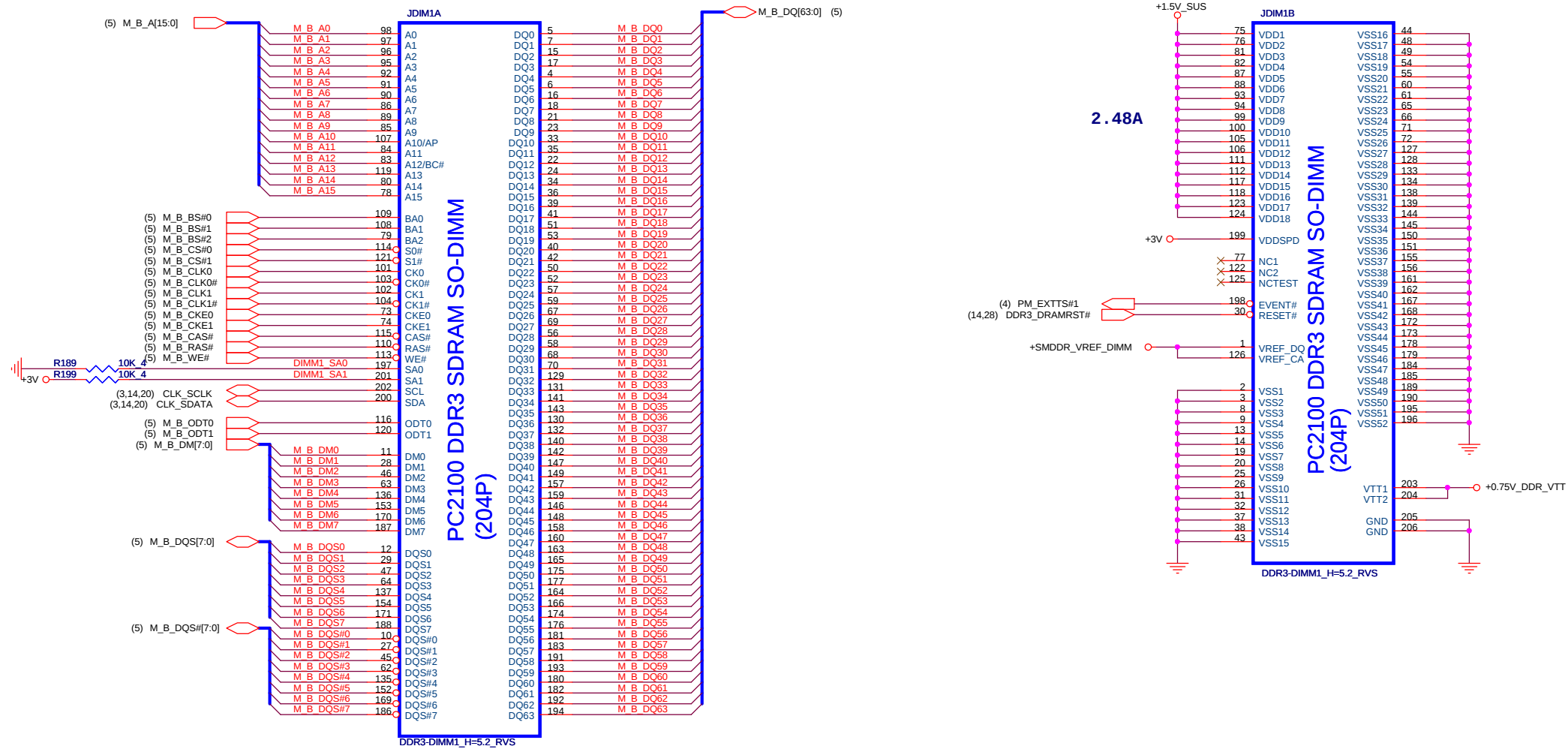
C316

10u/6.3V

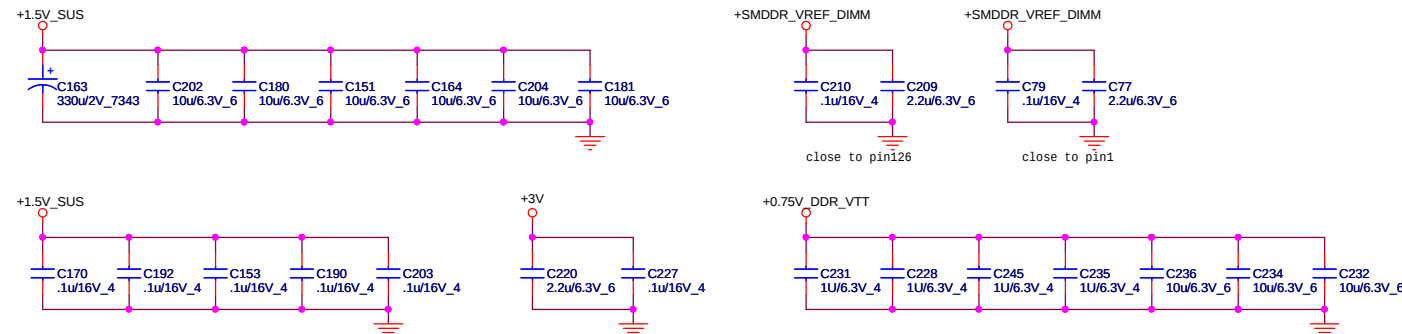
Internal weak pull-down
VCCVRM=>+1.8V (default)
external pull-up
VCCVRM=>+1.5V

IBEX PEAK-M (GND)

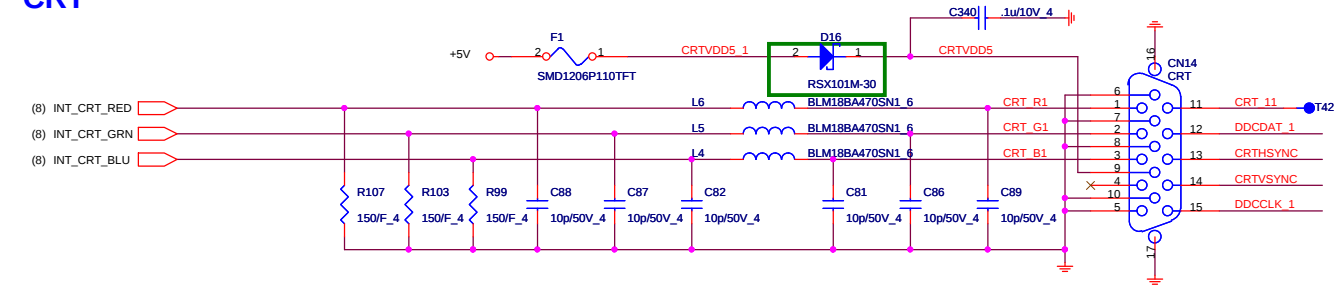




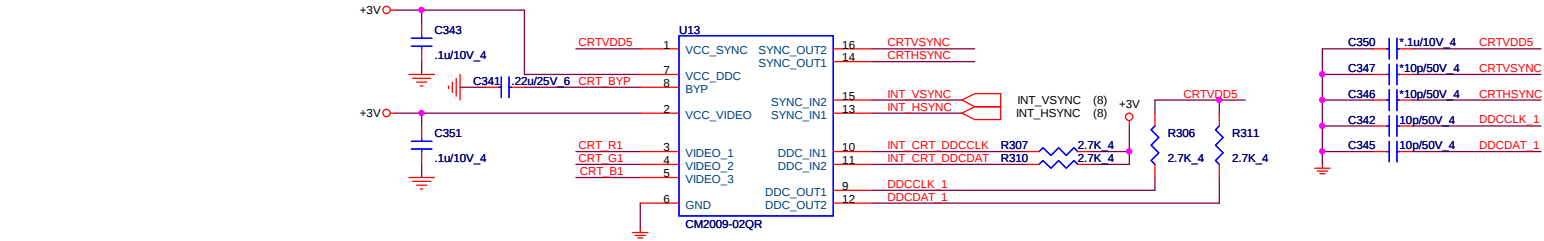
DIMM decoupling CAP (near So-Dimm1)



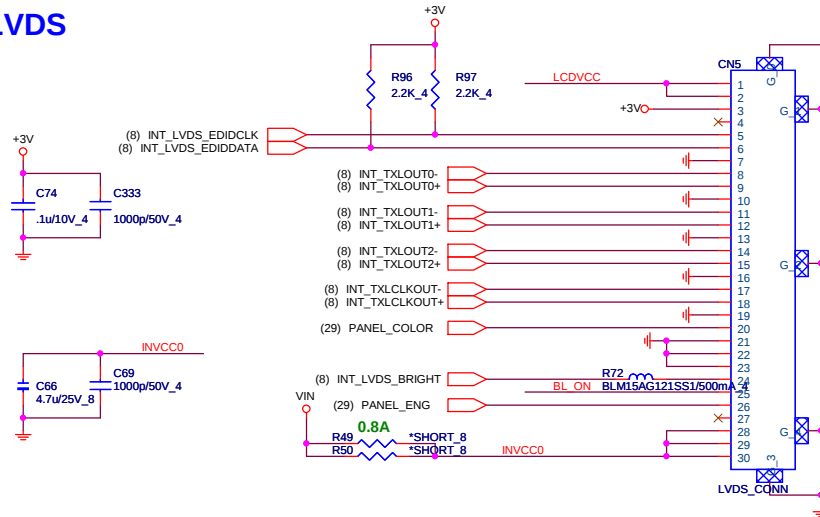
CRT



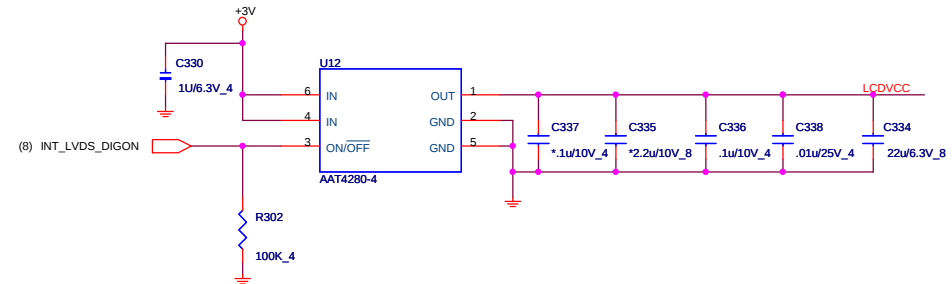
(8) INT_CRT_RED
(8) INT_CRT_GRN
(8) INT_CRT_BLU



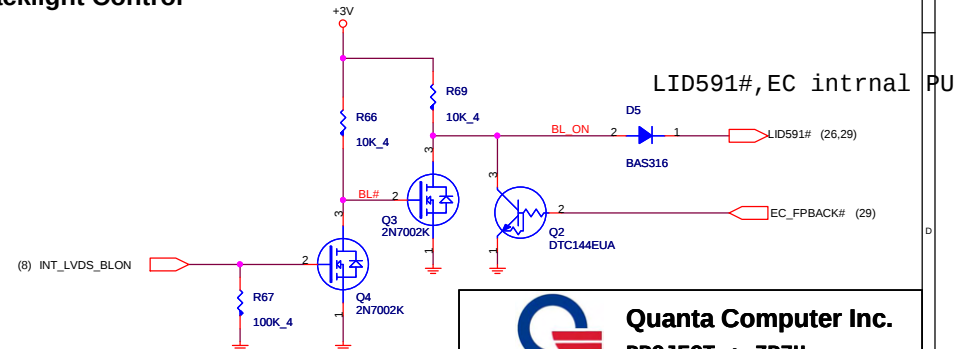
LVDS



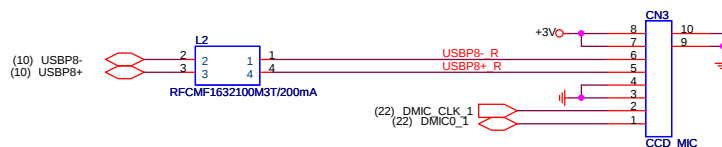
LCD Power



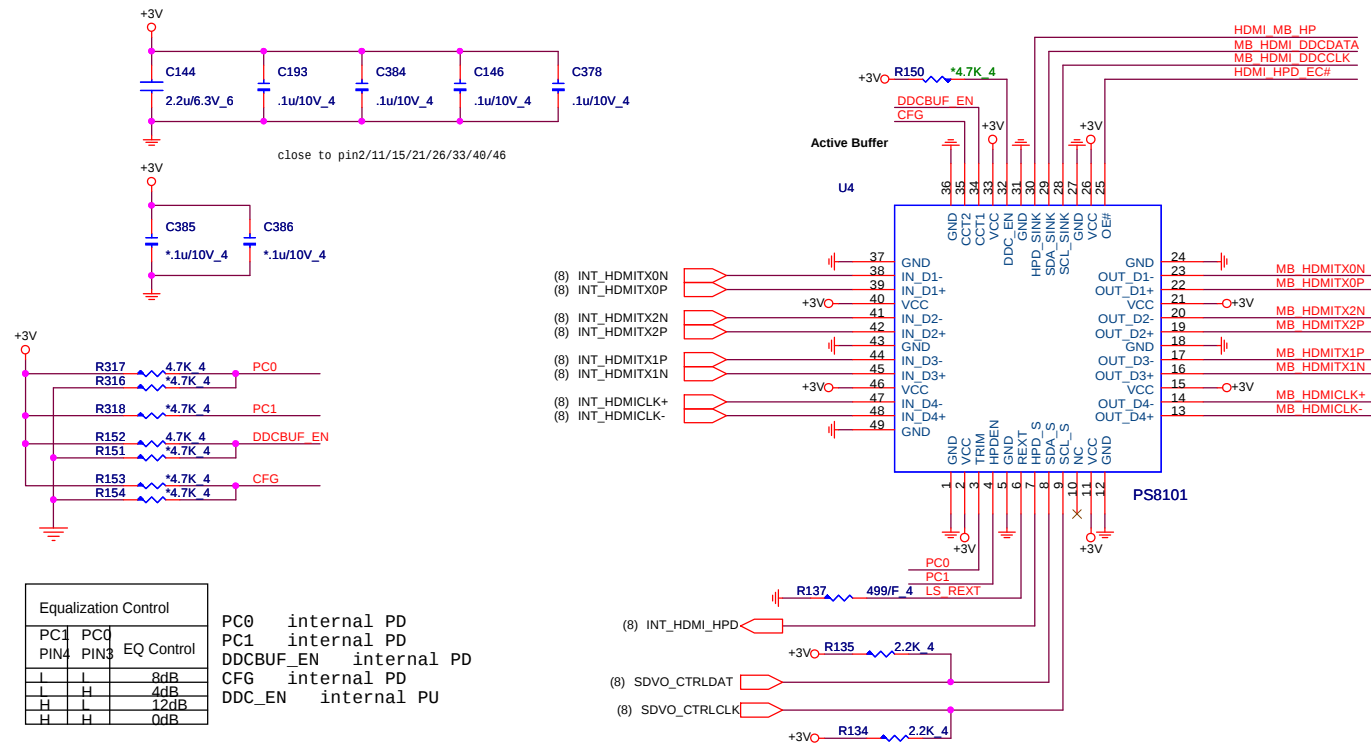
Backlight Control



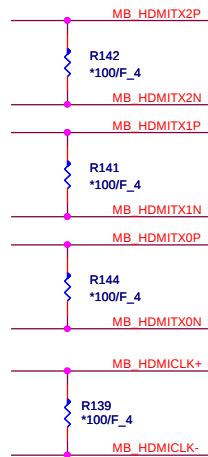
CCD and MIC



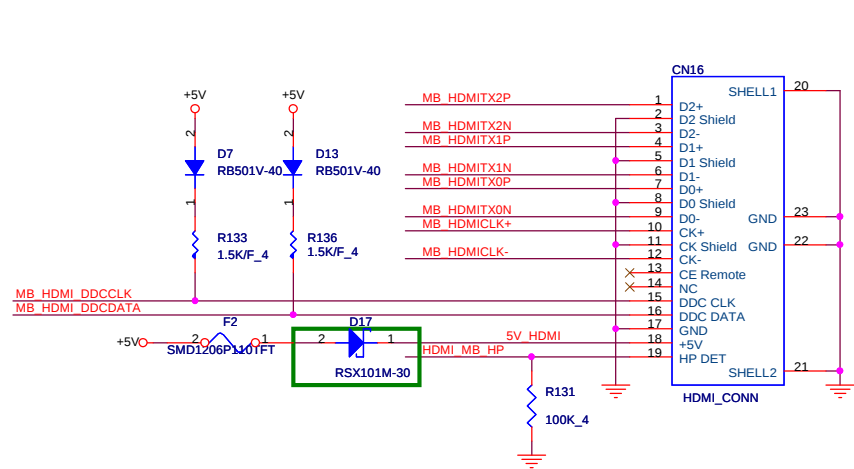
HDMI LEVEL SHIFTER



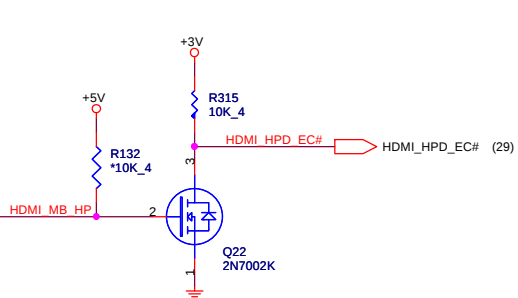
EMI



HDMI connector



HP-detect & OE# control





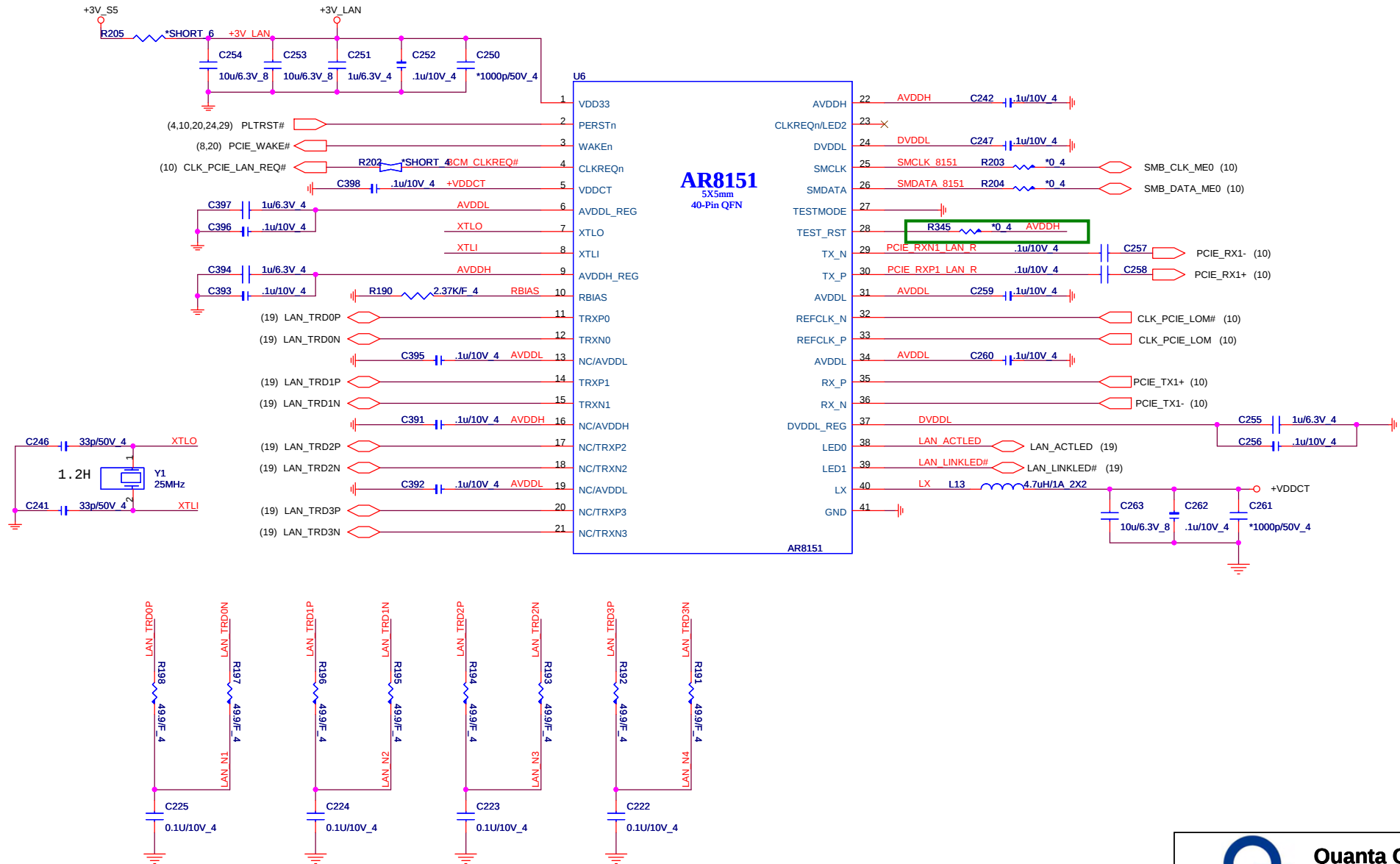
Quanta Computer Inc.

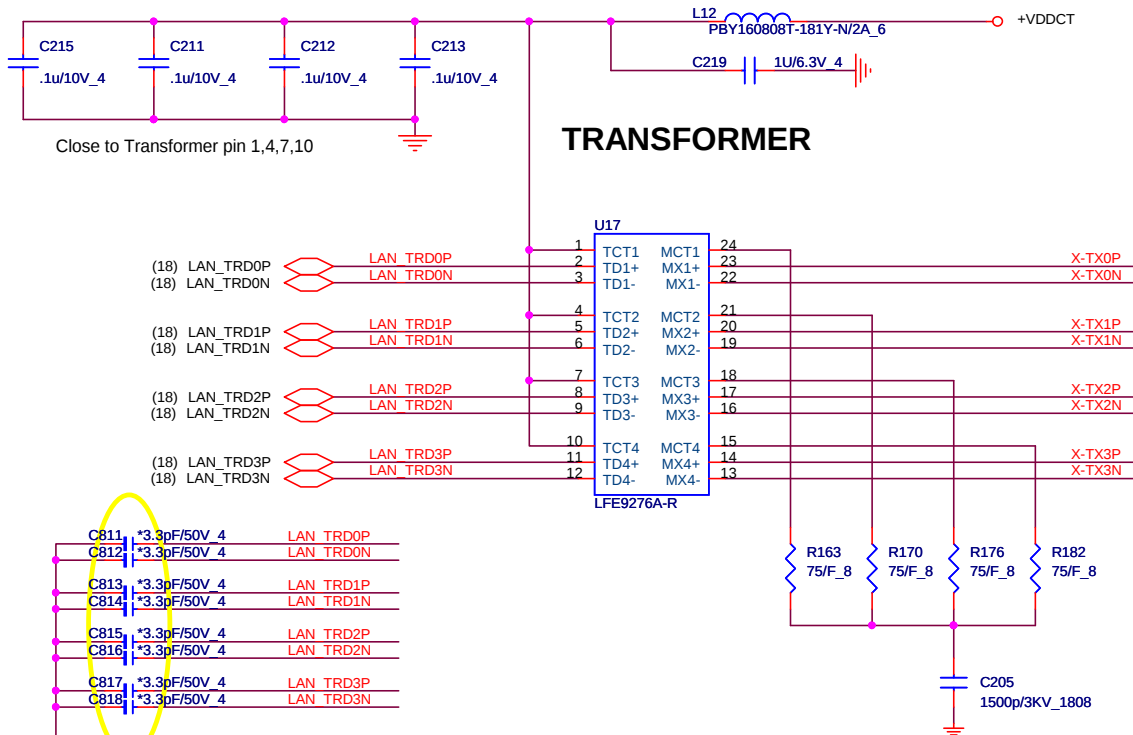
PROJECT : ZR7U

HDMI (PS8101)

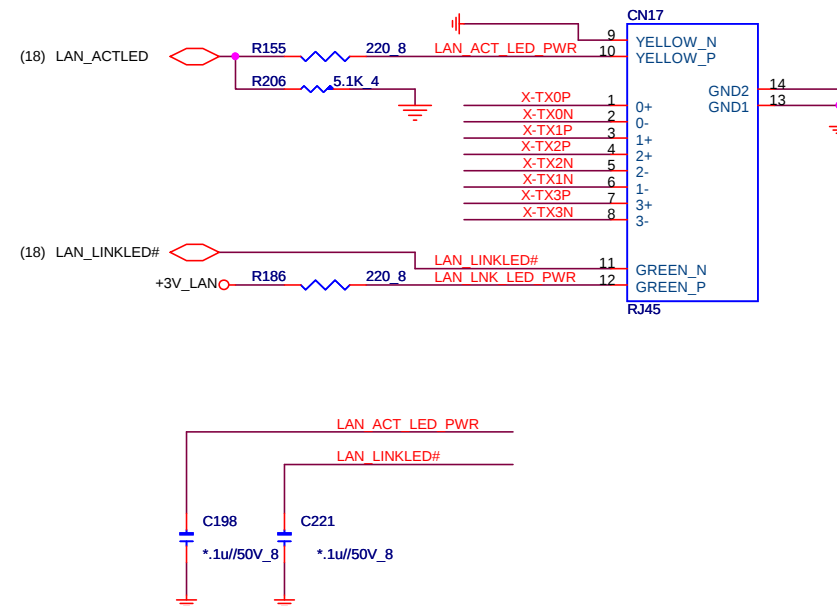
Size	Document Number	Rev
		1A
Date: Tuesday, April 20, 2010		
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Giga-LAN AR8151



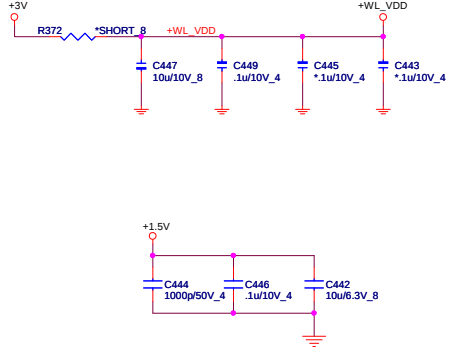
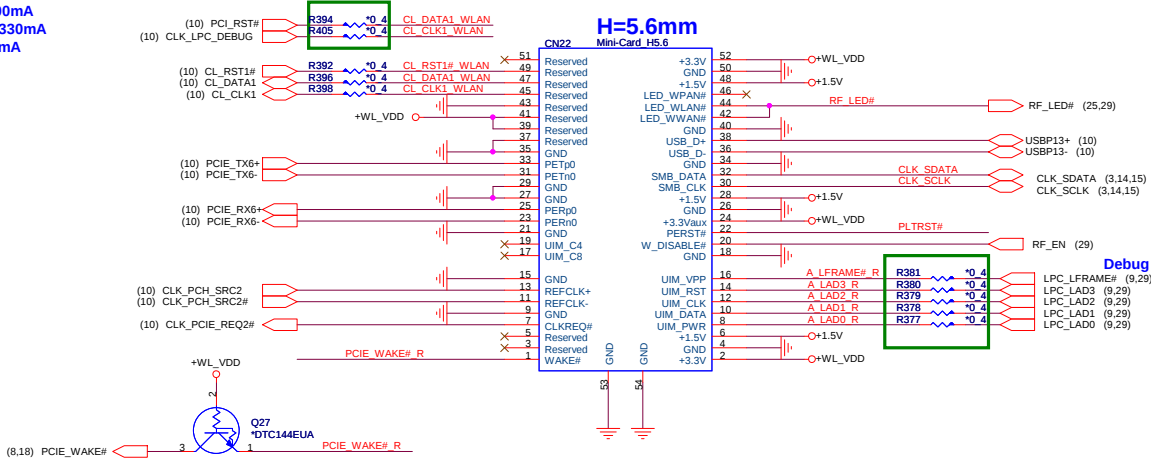


Delta LFE9276C-R (DB0ZR1LAN00)
FCE NS892407 (DB0LL1LAN00)
Bothhand GST5009B (DB0Z06LAN00)

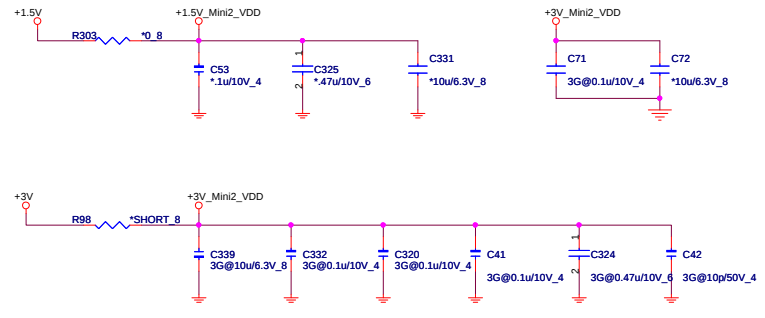
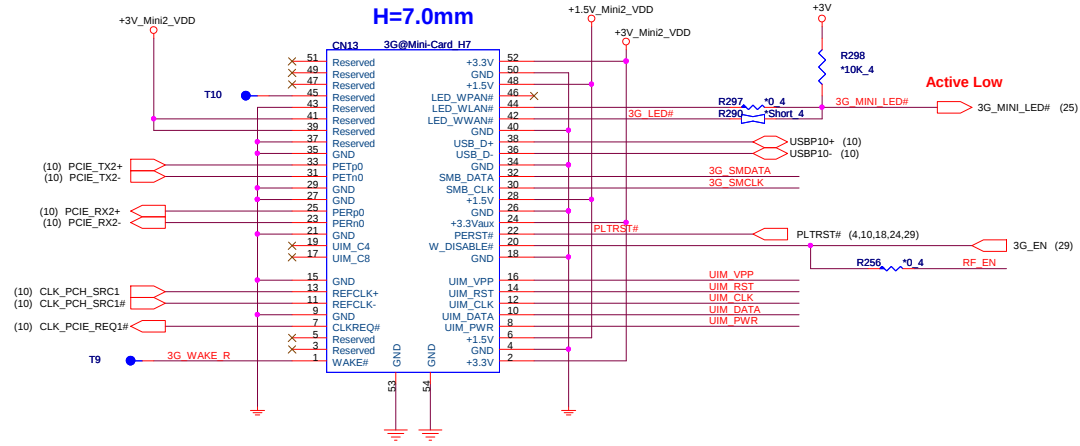


MINI-CARD WLAN(MPC)

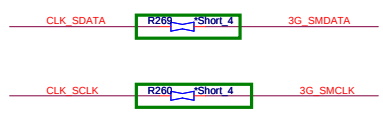
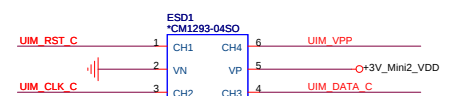
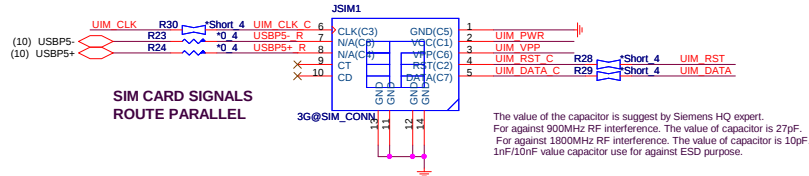
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA



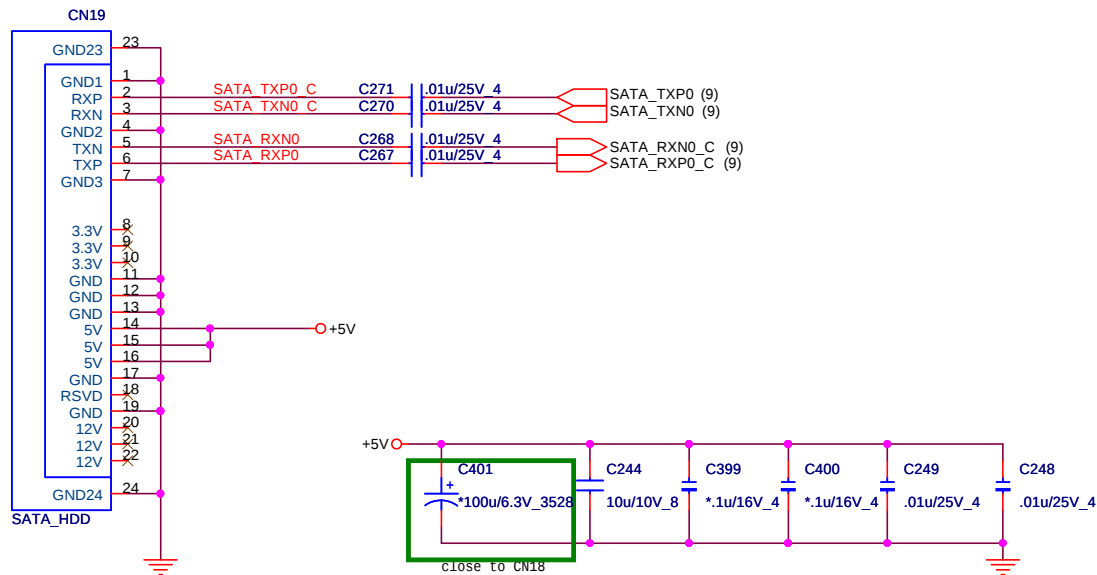
MINI-CARD 3G(MNC)



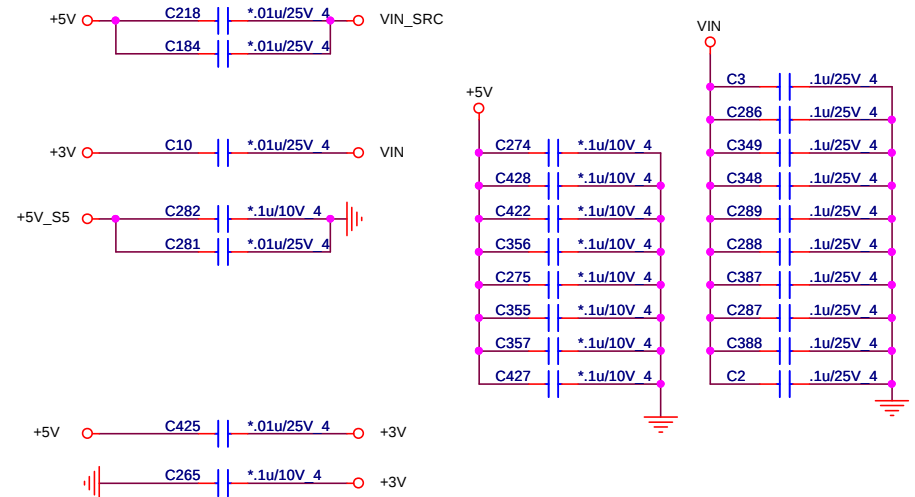
SIM CARD(RFM)



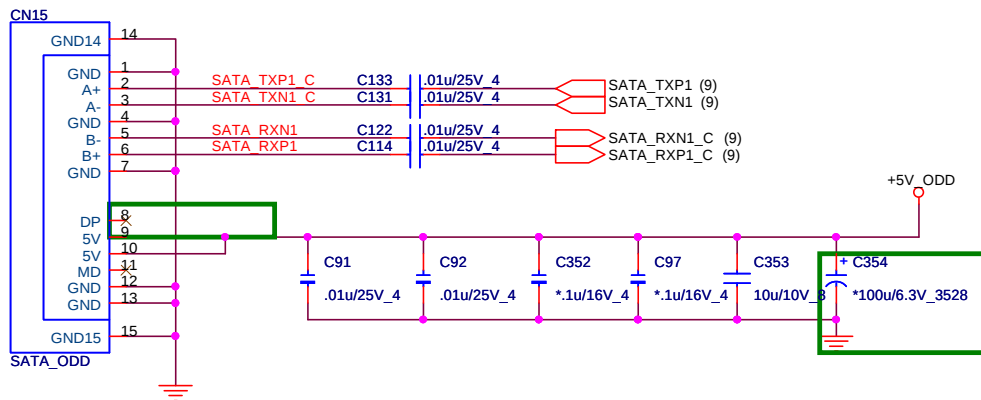
MAIN SATA HDD



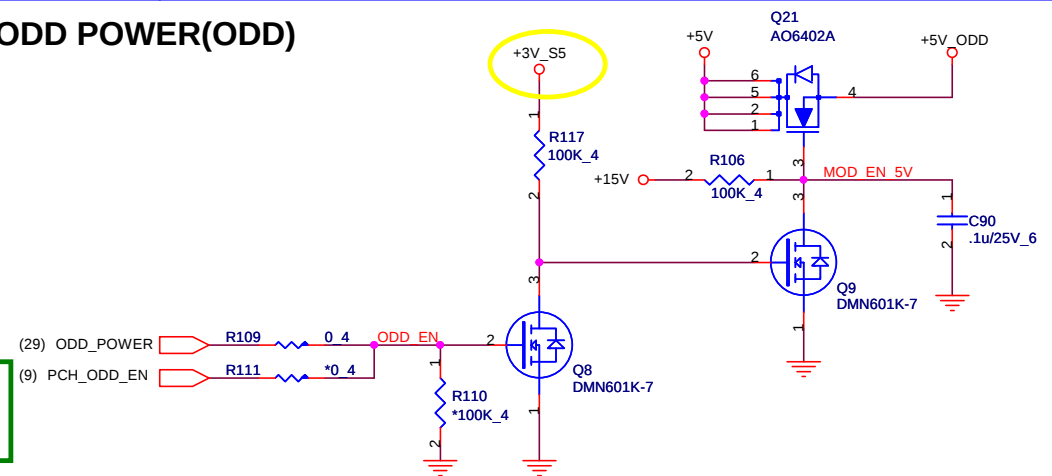
EE RETURN-PATH CAPACITORS



ODD (SATA)



ODD POWER(ODD)

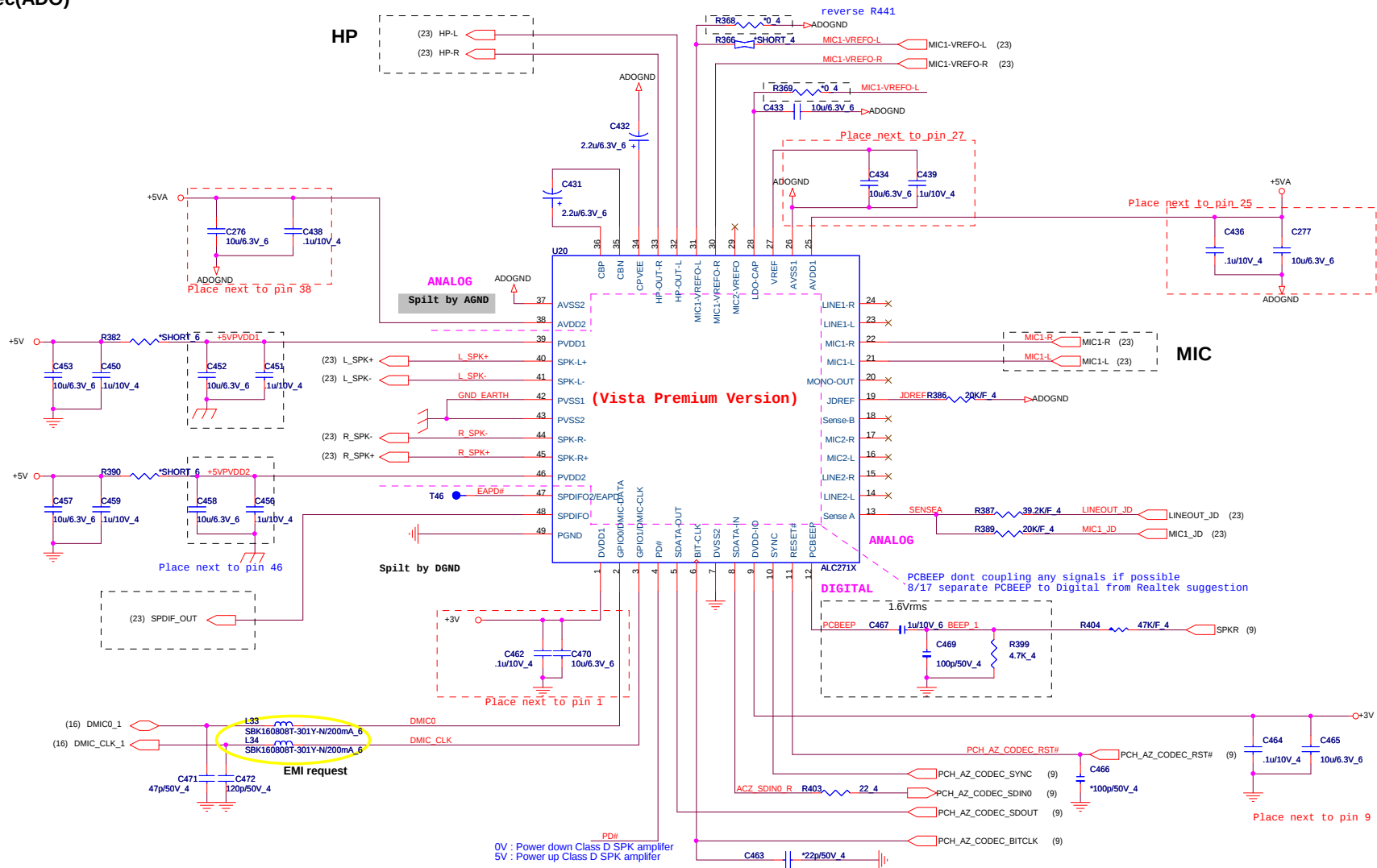


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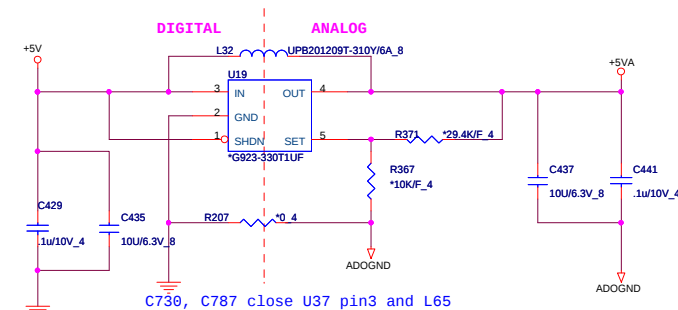
Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	1A

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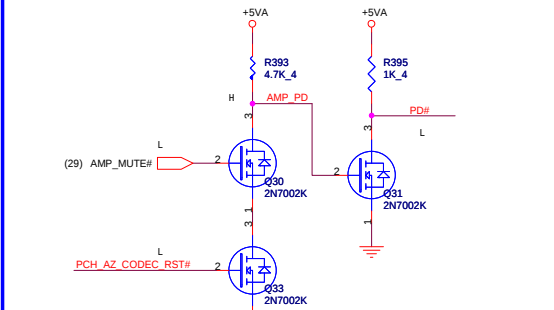
Codec(ADO)



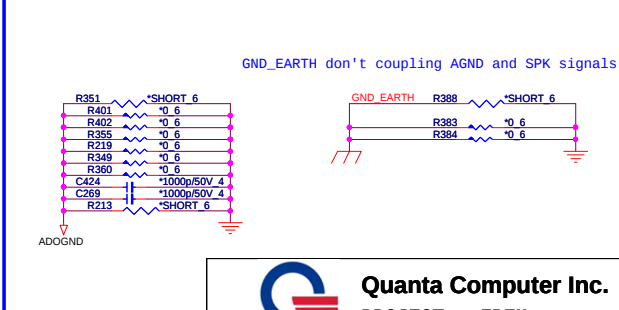
Power (ADO)



Mute(ADO)



Split-GND



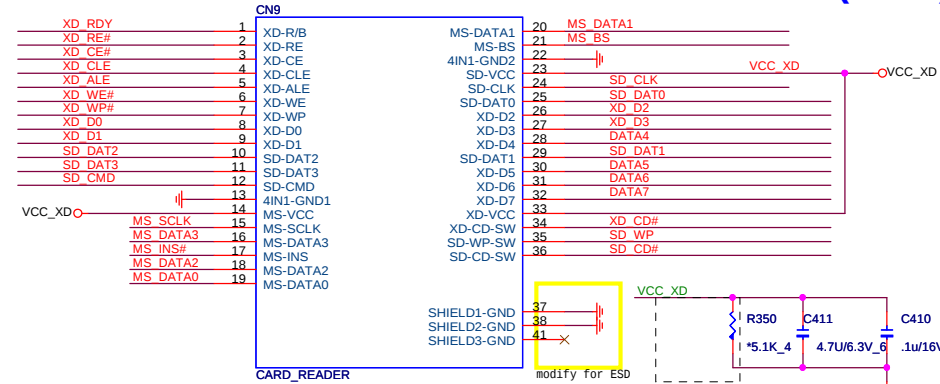
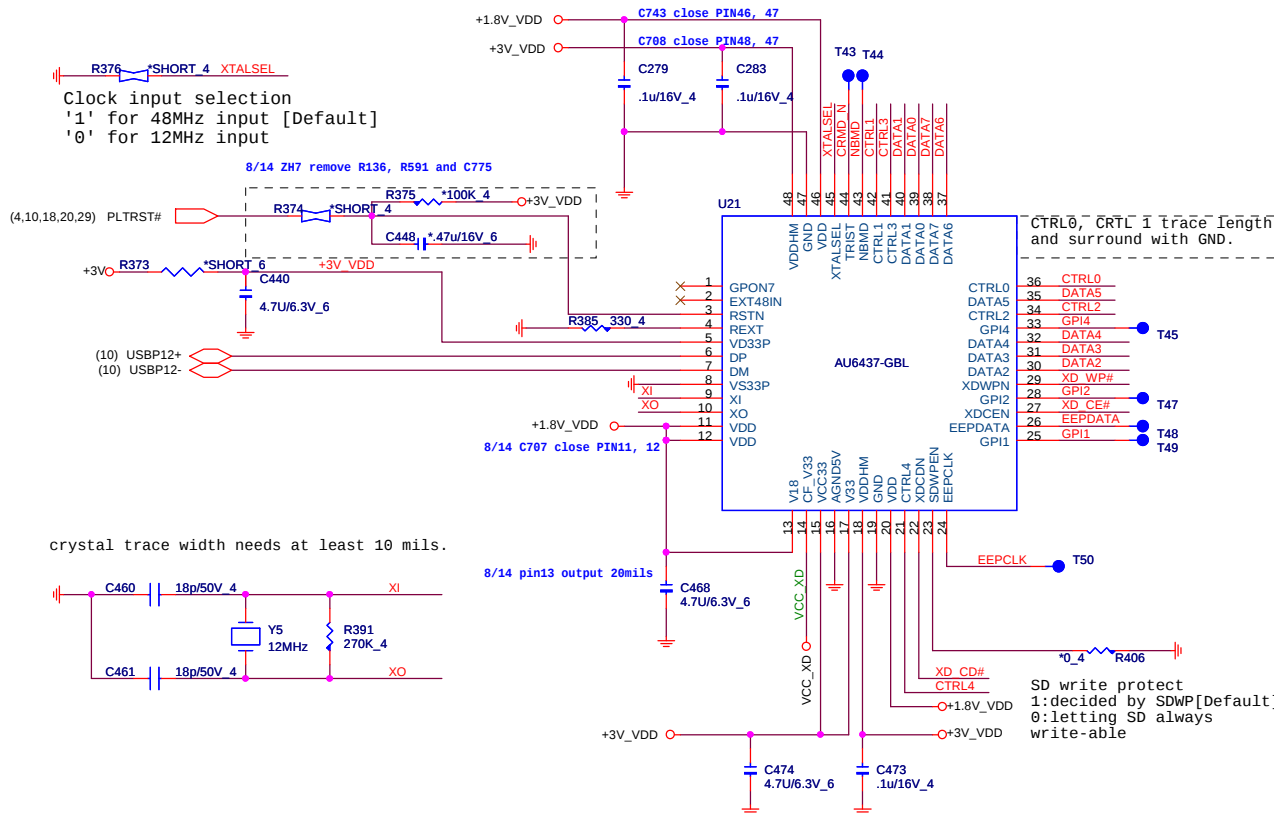
[illegible]

The schematic diagram illustrates the HP-1000 PCB layout, featuring several key components and their interconnections:

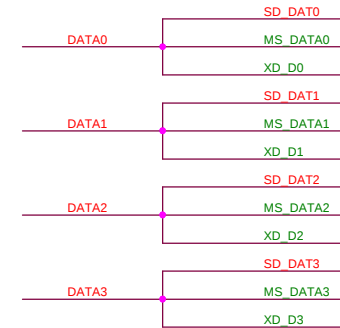
- Input/Output Connectors:**
 - HP-L and HP-R (22):** Input connectors for the HP-L and HP-R signals.
 - SPDIF_OUT (22):** Output connector for the SPDIF_OUT signal.
 - LINEOUT_JD (22):** Output connector for the LINEOUT_JD signal.
- Power and Grounding:**
 - +3V_SPD:** Power supply for the SPDIF_OUT signal.
 - +5VA:** Power supply for the HP-L and HP-R signals.
 - ADOGND:** Analog ground connection.
- Resistors and Capacitors:**
 - R209, R214:** Resistors connected to the HP-L and HP-R inputs.
 - R216, R208:** Resistors connected to the HP-L and HP-R inputs.
 - R210, R217:** Resistors connected to the HP-L and HP-R inputs.
 - C280:** Capacitor connected to the +3V_SPD supply.
 - C284, C273:** Capacitors connected to the +5VA supply.
- Transistors and Diodes:**
 - Q29 (ME2347):** Transistor connected to the +3V_SPD supply.
 - Q28 (2N7002K):** Transistor connected to the +5VA supply.
 - Q26 (2N7002K):** Transistor connected to the LINEOUT_JD output.
 - D18:** Diode connected to the +5VA supply.
- Other Components:**
 - BLM15AG121SS1/500mA 4:** Inductor components.
 - SPDIF_BLACK:** Signal line for the SPDIF_BLACK output.

CARD READER Controller

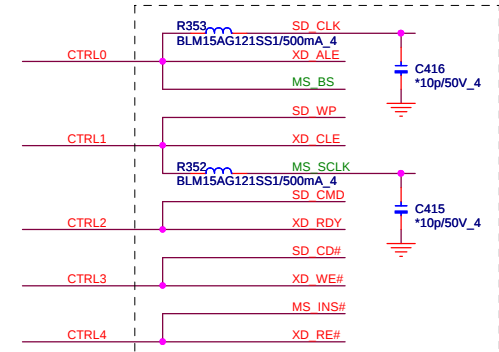
4 IN 1 CARD READER (MMC)



Close to CN14 pin 14 & pin23
4.7u CAP close to pin23



Close to connector

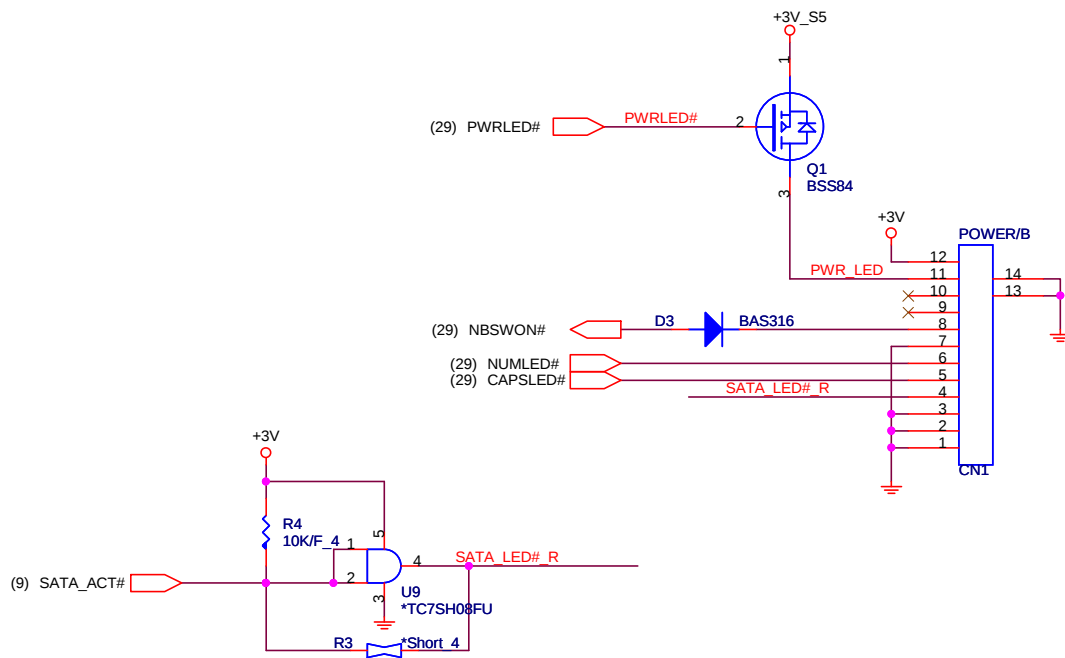


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PROJECT : ZR7U

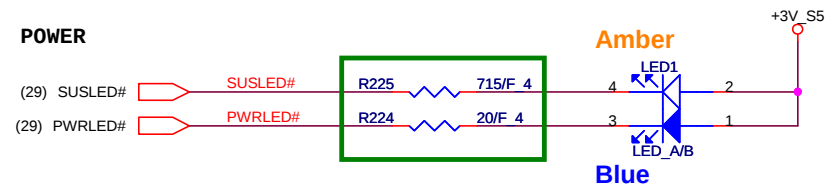
AU6433 CardReader

POWER BOARD CONN(UIF)

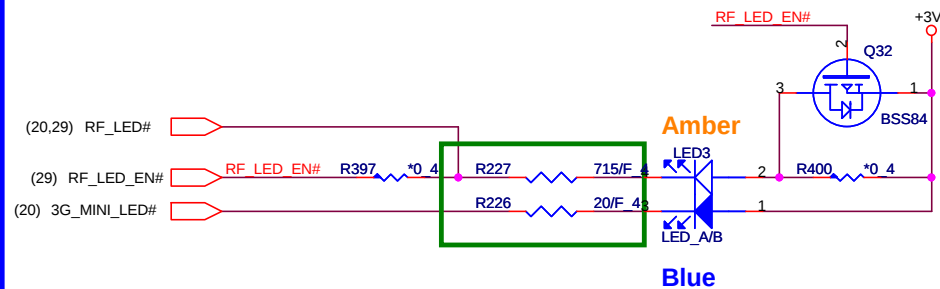
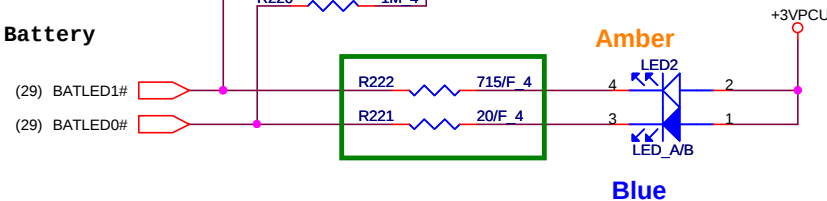


LED

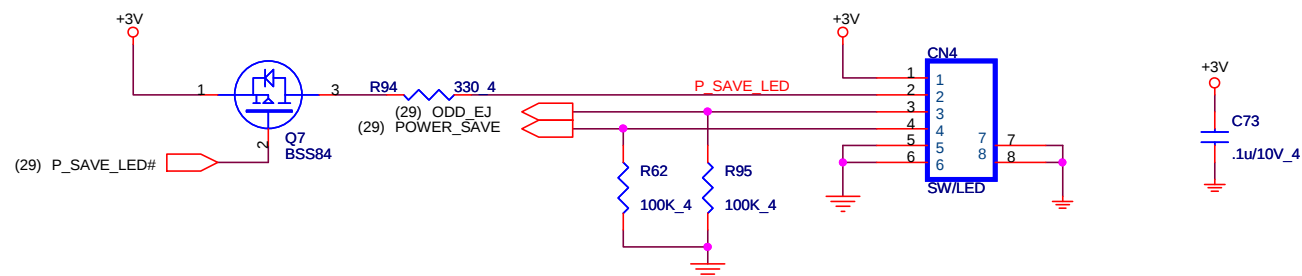
POWER



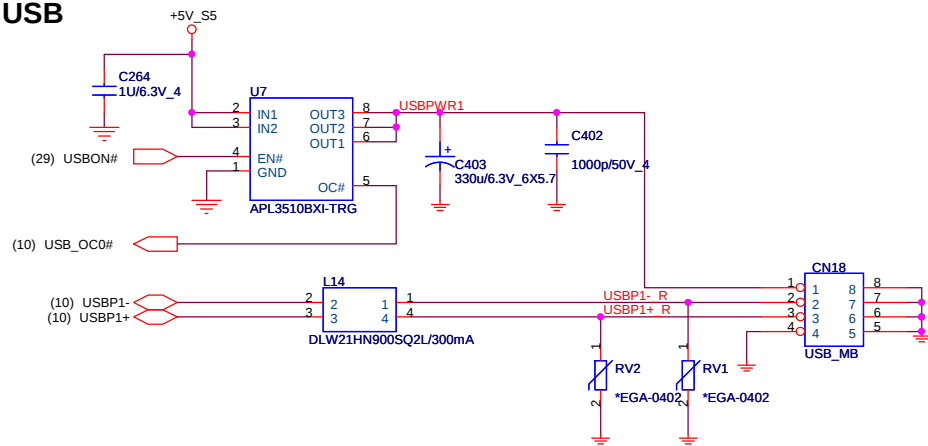
Battery



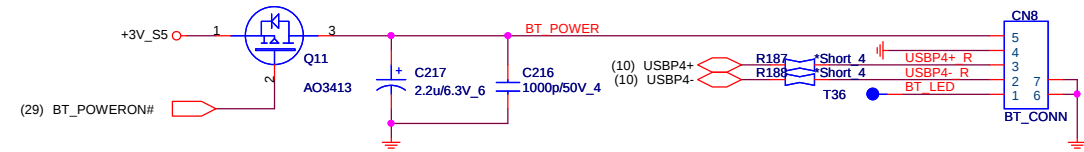
SW /B



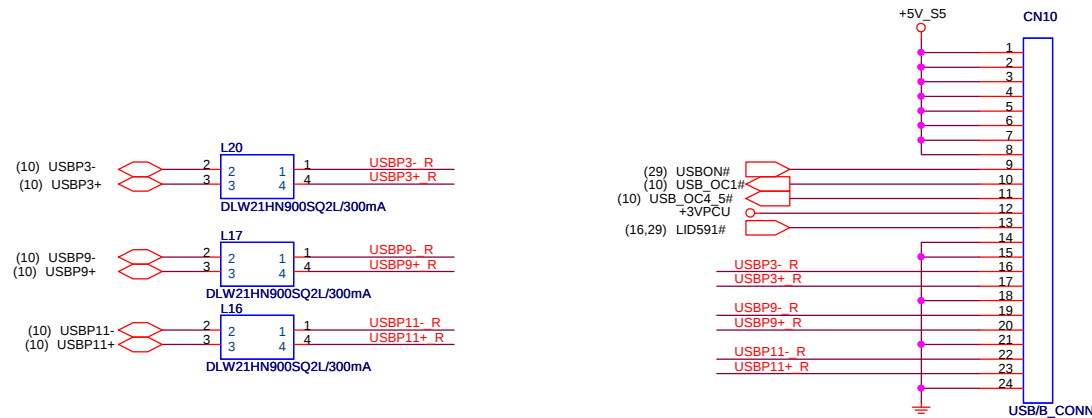
USB



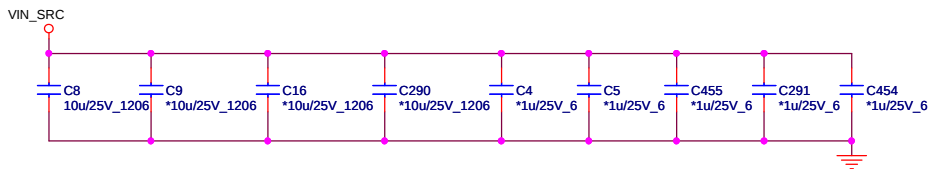
BLUETOOTH CONNECTOR



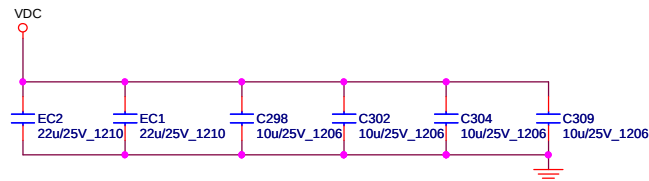
USB/B



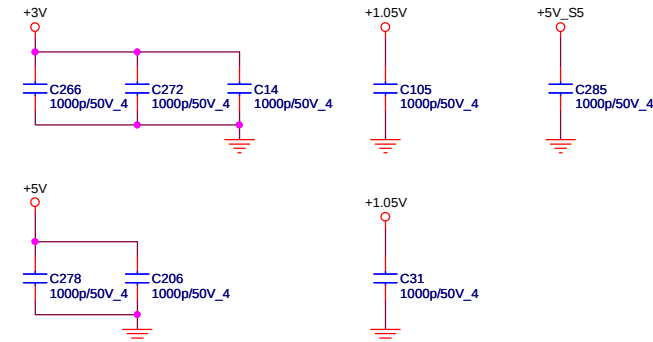
EMI decoupling



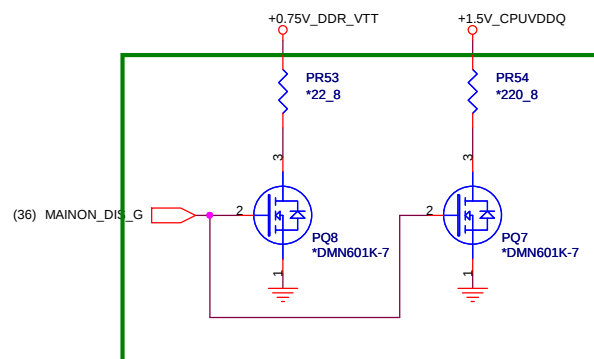
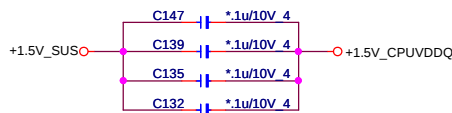
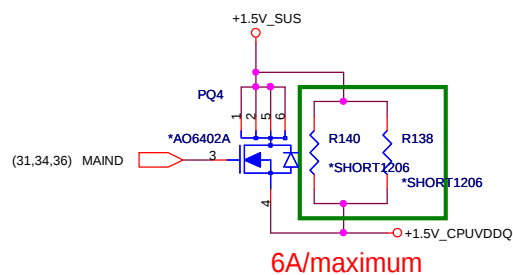
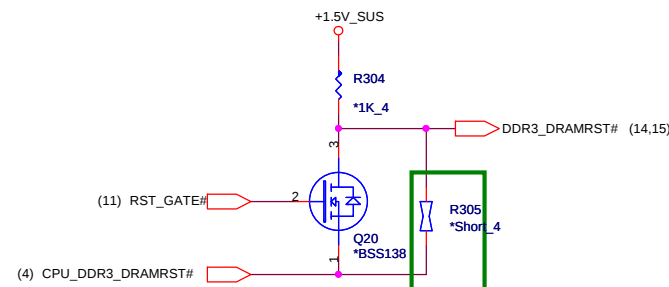
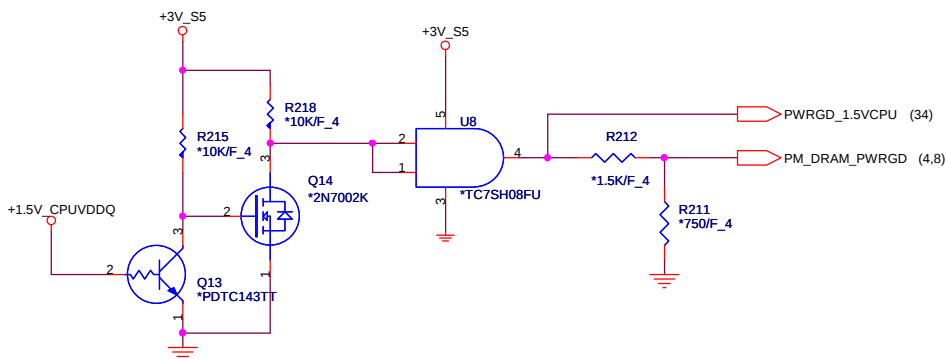
EMI ISN solution

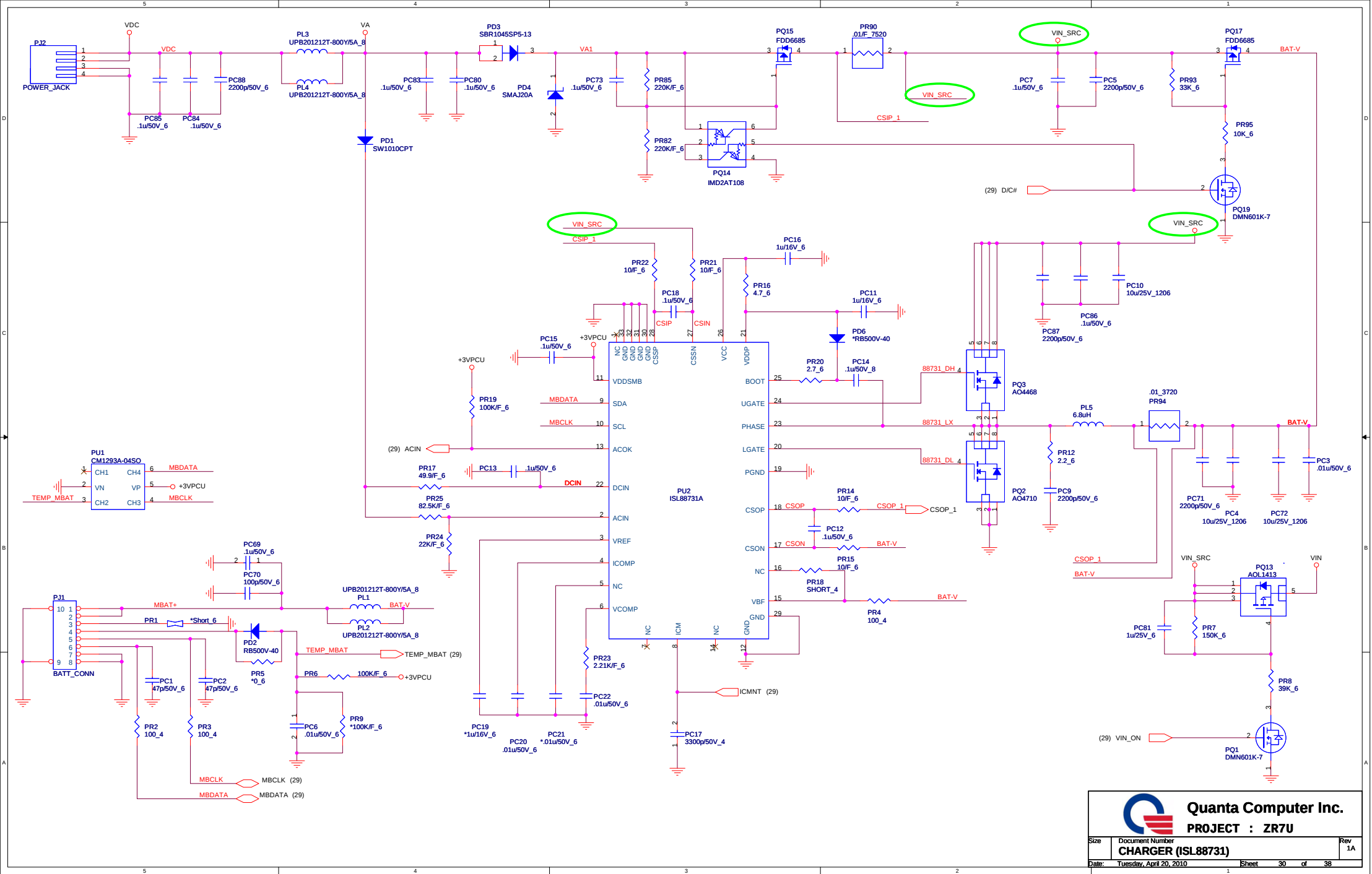


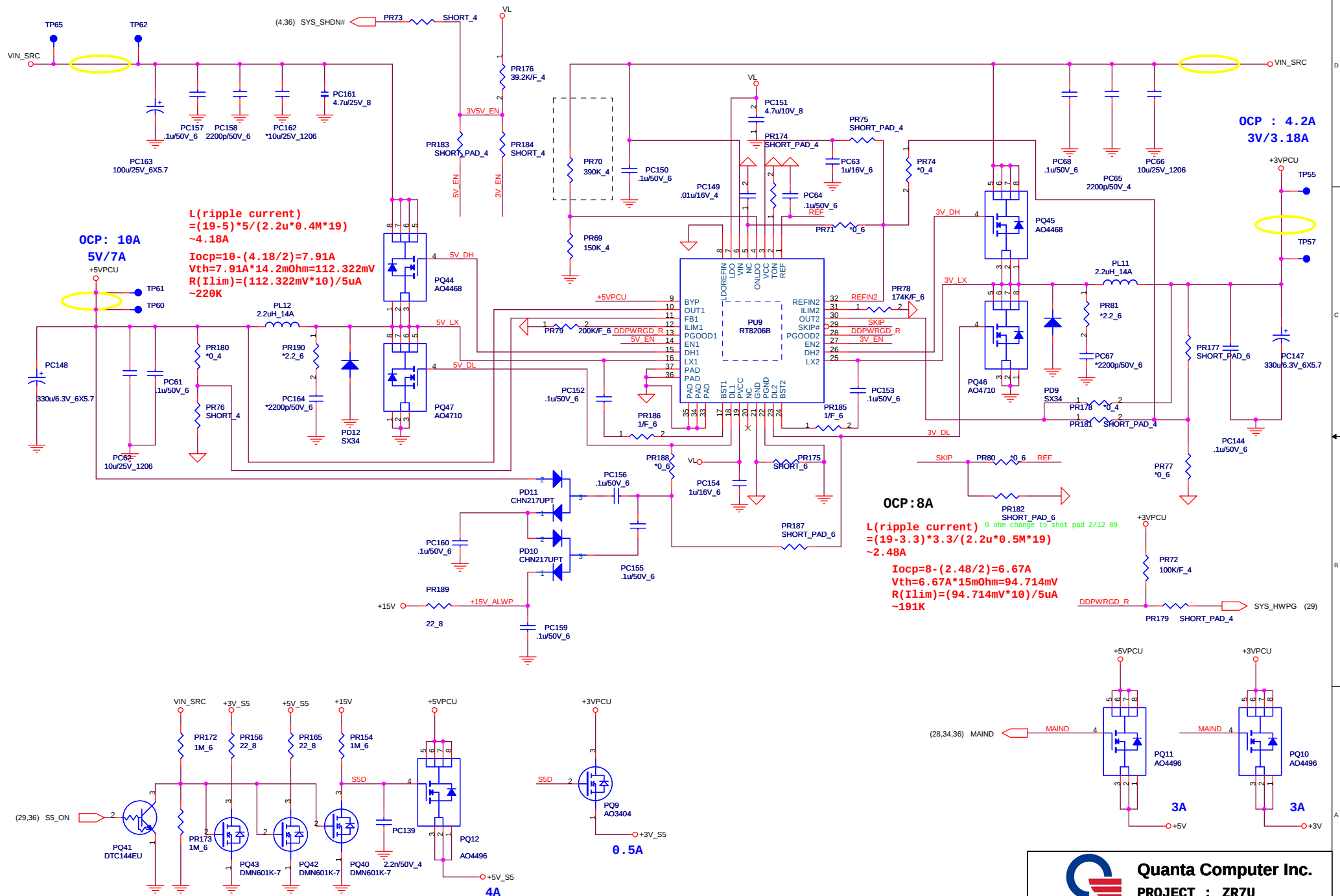
EMI decoupling

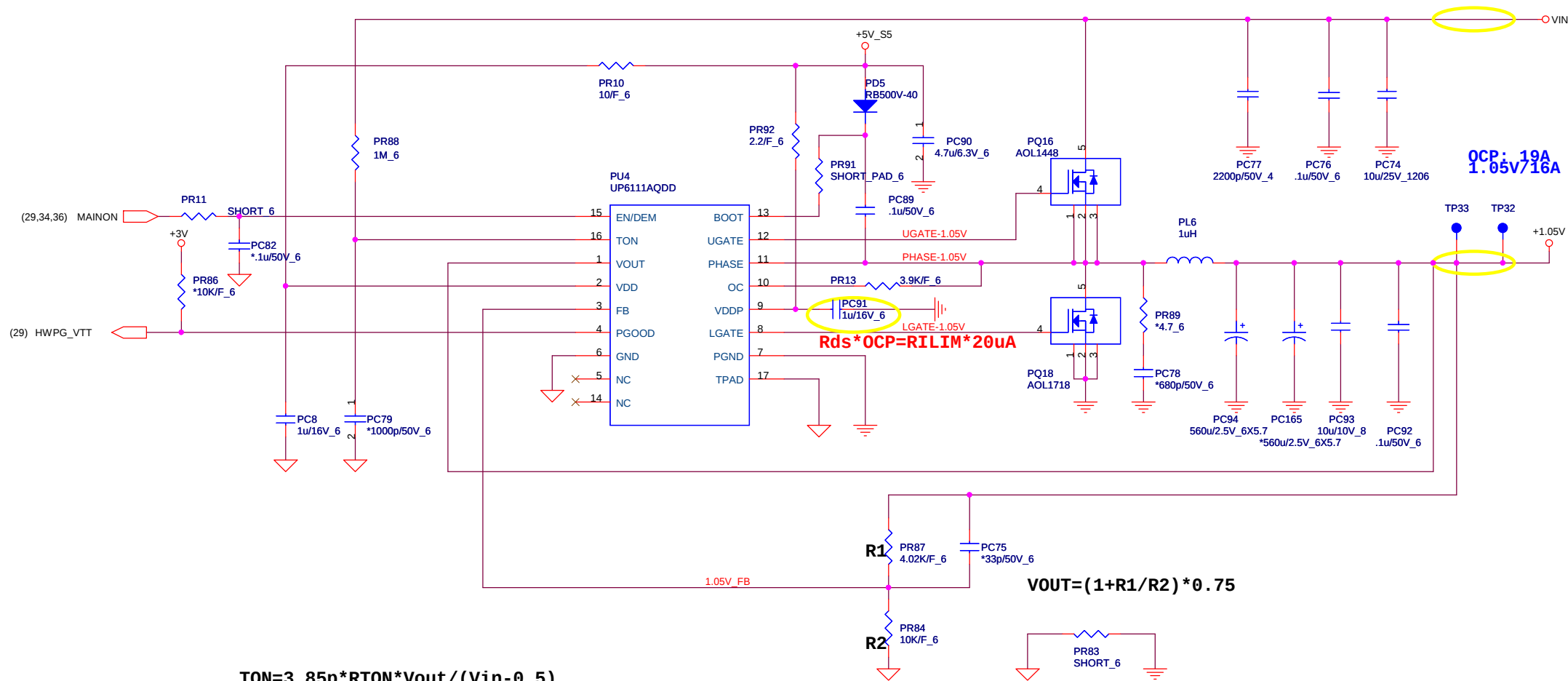


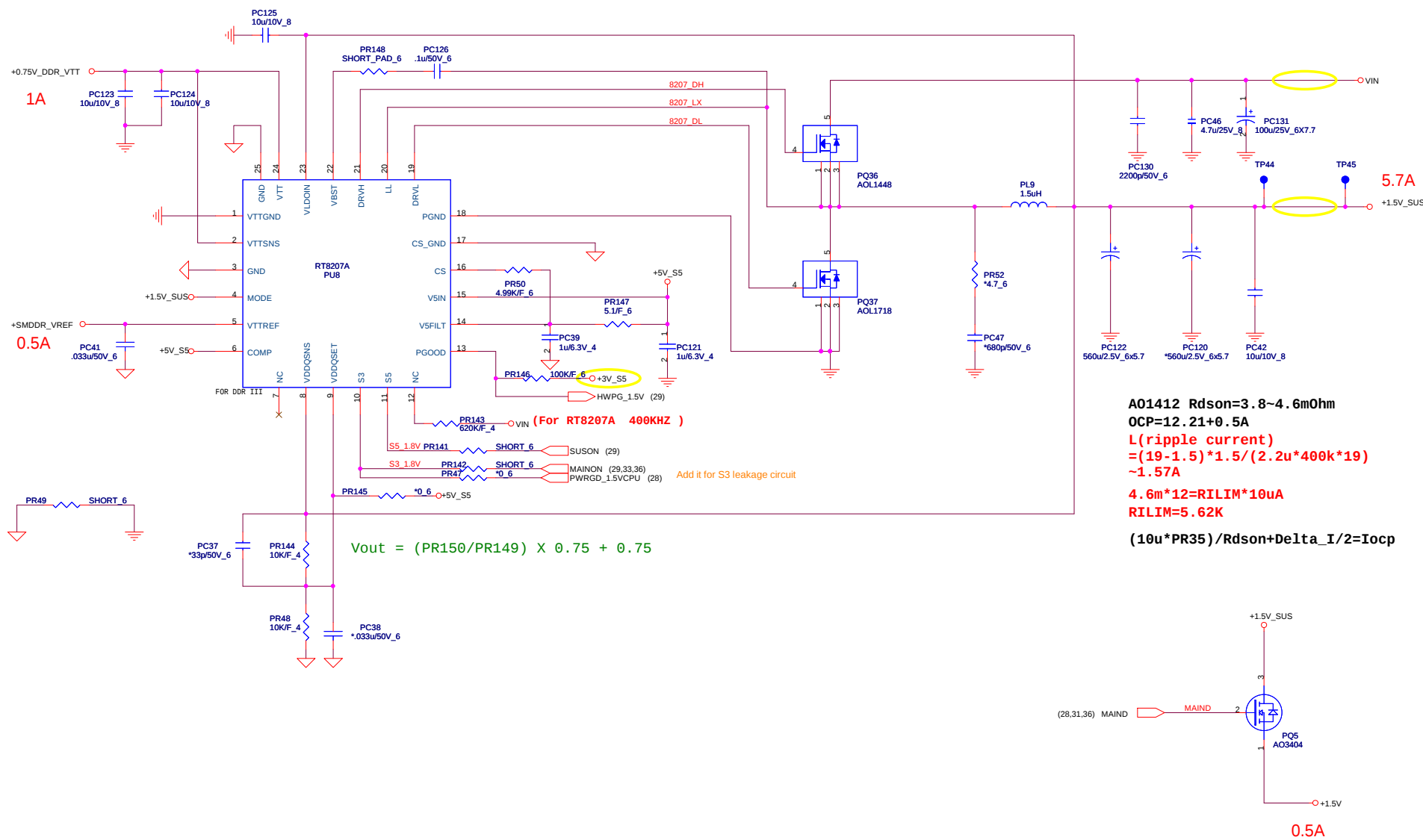
Intel S3 leakage circuit

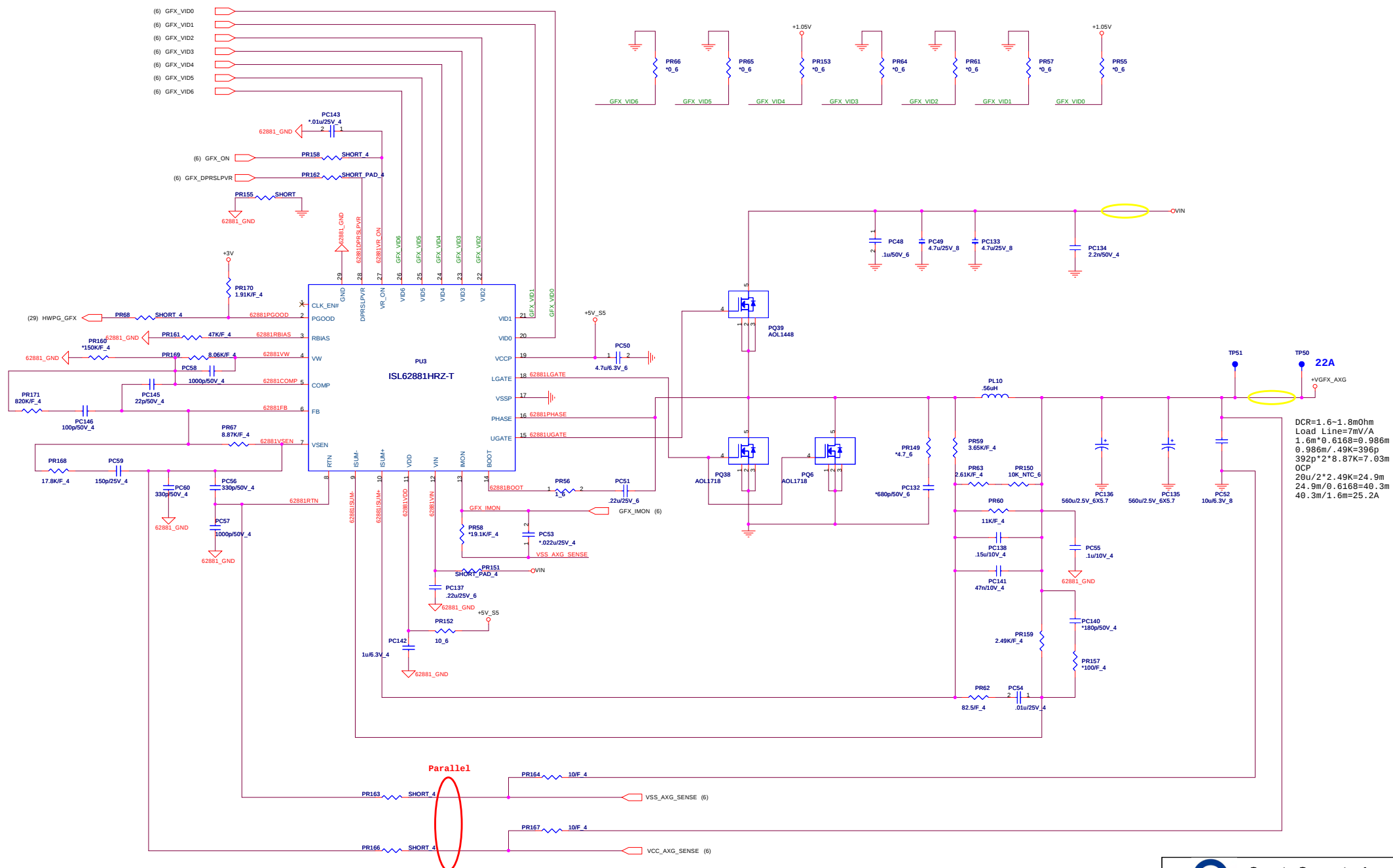


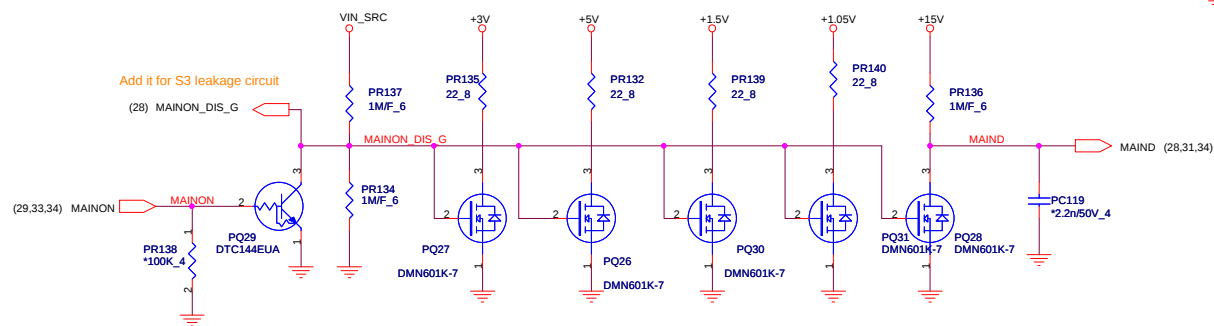
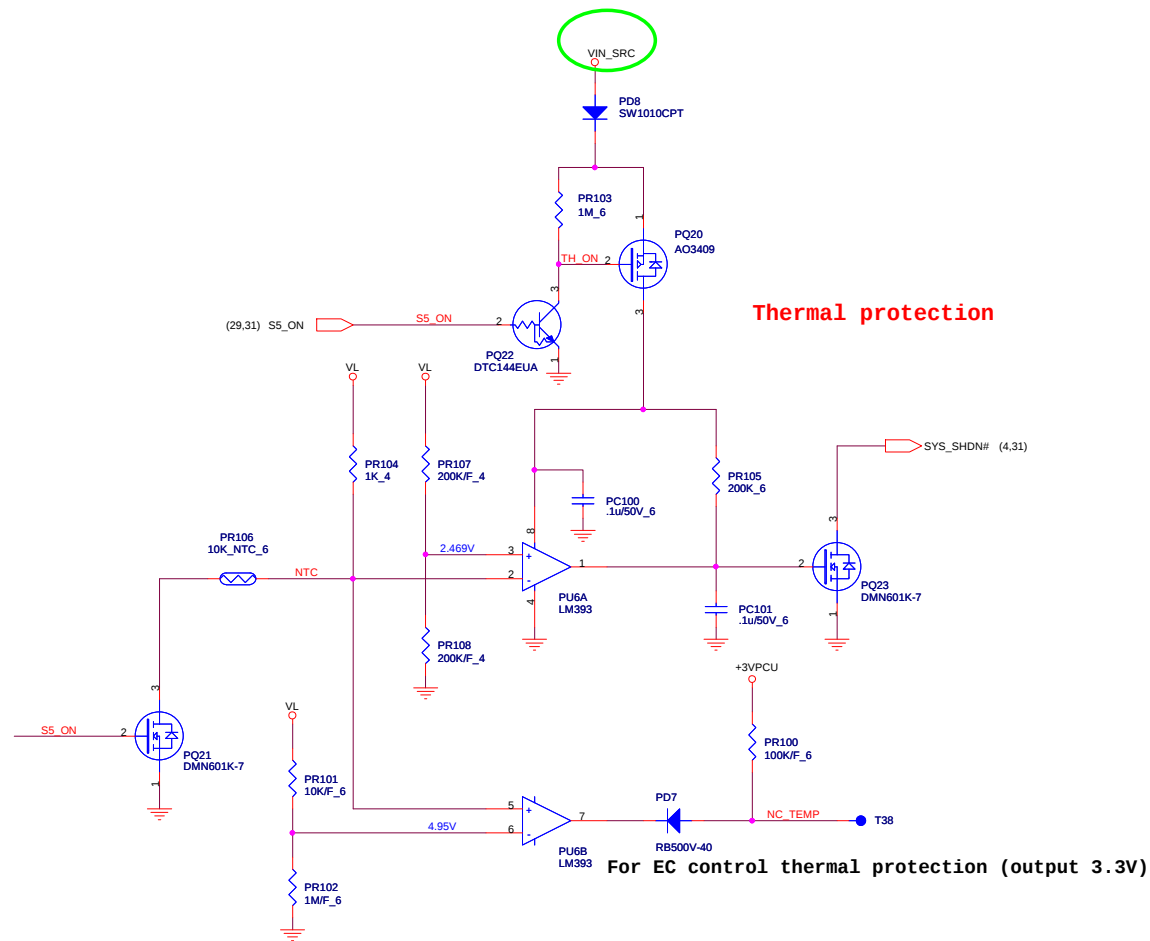
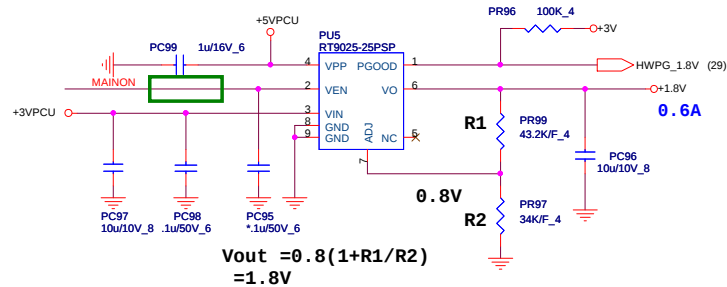


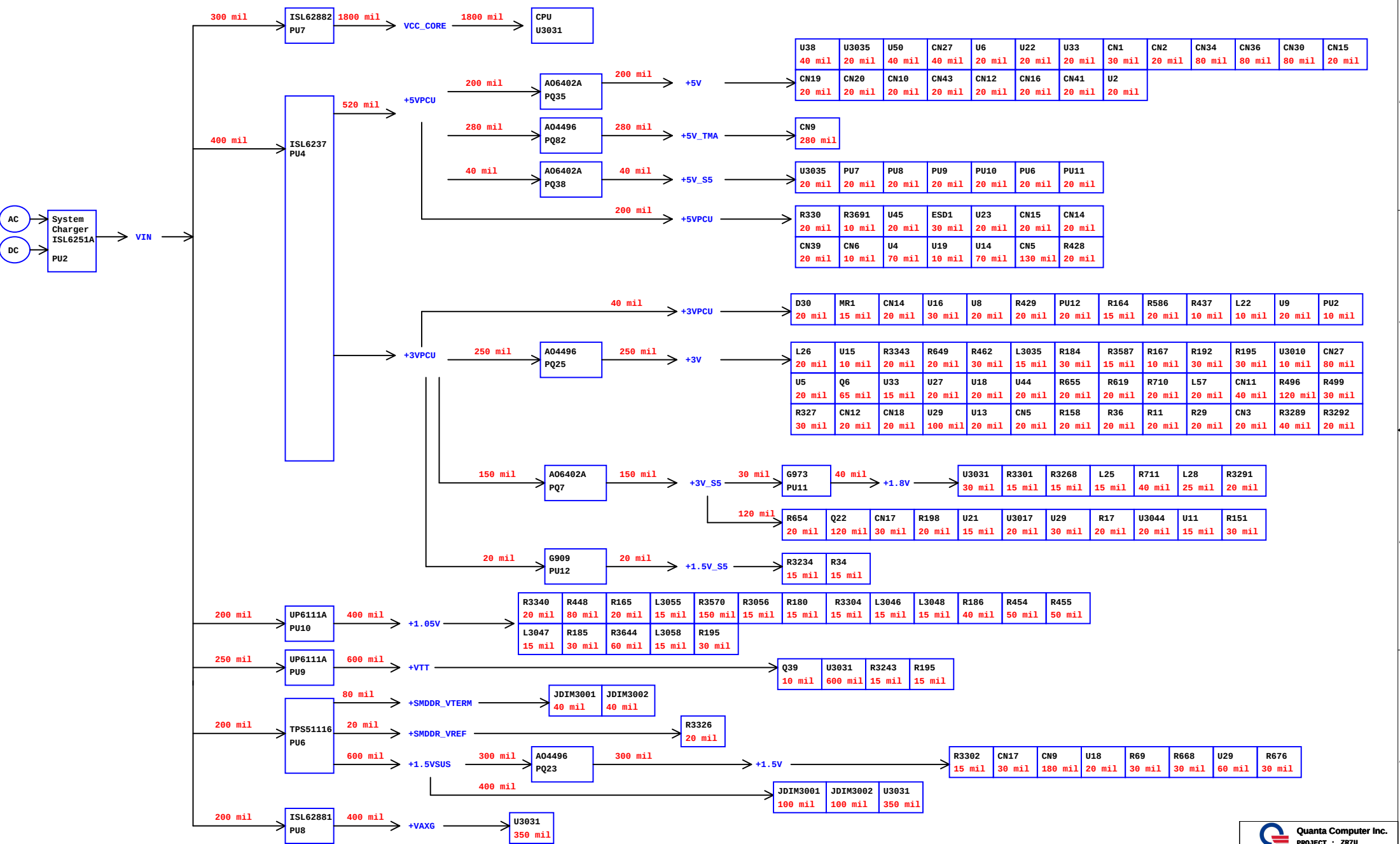












Model	REV	CHANGE LIST	MODEL	ZR7	
				FROM	To
ZR7U MB	1A	2/11 1. Del trace VREF_DQ_DIMM0/VREF_DQ_DIMM1, and R131,R127,R116,R129 2. Add two test point (TP35/TP36) 3. Remove D16, and connect to EC directly by Anda confirmed 2/12 1. Add Q44/Q45/R600 for AMP_PWR_DOWN function 2/22 1. Change C630/C516 to VIN_SRC 2. Change R489, R488 P/N to 5% 3. Change PL18 footprint by power engineer 4. Del R190,R217,R218 and Add JP1007 5. Change R7643, R7646 P/N to 4.7K 5% 6. Remove 0ohm and short PAD R482,R7575, R7576,R7562, R7565 2/23 1. Del C791,C794,T77,T79 for layout requirement 2. Swap USB_OC0#,USB_OC2# ,USB_OC6#,USB_OC4.5#for layout requirement 3. Change C763,C767 for cost down 4. Change Y7000 P/N and footprint for cost down 2/25 1. Stuff R166 for vender commend 2. Del R171,R203 for layout requirement 3. Add C781,C782,C785,C786,C787,C788,C791,C794 for EMI decoupling cap 3/02 1. Correct Function Code 2. Change C655,C702,C7790 P/N and Footprint 3/04 1. Change PC219,PC61,PC164,PC74,PC176,PC76,PC180,PC79,PC182 P/N and Footprint for Power design change 2. Layout reference rename			
		3/22 1. Del TP63,TP64,TP46,TP47,TP29,TP48,TP49,TP53,TP30,TP52,JP1,JP2,JP3,JP4,JP5JP6,JP7,JP8,JP9,JP10,JP11,JP12,JP13 for remove current test components_All 2. PR146, R117 link to +.3V_S5 for power sequence_P34 3. Unstuff SW1 on board power switch_P29 4. Change 0ohm to short pad R45,R48,R54,R247,R35,R87,R86,R257,R1,R2,R61,43,R11,R59,R290.R30,R28,R29,R98,R3,R107,R108_All 5. Change netname +1.1V_VTT to +1.05V_All 6. Unstuff R237,R230,R228,Q15 and change CN11 for change RTC Battery type_P9 3/24 1. Reserve PC165 for +1.05V ripple_P33 2. PQ16 AOL1718 change to AOL1448_P33 3. PR78 102K/F change to 174K/F_P31 4. Add C475 for Monitor test_P12 5. Del U15 120K EEPROM_P20 3/25 1. Reserve CB11,CB12,CB13,CB14,CB15,CB16,CB17,CB18 for EMI 1G Hz_P19 2. Del R38, R41_P16			
		4/1 1. Change C295,C296 value to 27pF and 33pF for X'tal vender commend_P10 2. Add C300,C305 for HDMI signal quality_P12 3. Add C471,C472 to 47pF and 220pF for EMI solution _P22 4. Del C390,C354,C401,C303,C140 for cost down _All			
		4/19 1. Change D16,D17 P/Nand fotprint for 5V power_P16,17 2. Remove R120 for don't need it _P21 3. Unstuff PQ7,PQ8,PR53,PR54 for leakage in S3 _P28 4. Remove 0 ohm: * Remove PR08_P36 * Short R260,R260_P20 * Remove R377/R378/R379/R380/R381/R394/R405_P20 * Short L7,L8,L9 * Short R125 5. Change R209,R214 For Audio test_P23			
		4/20 1. Remove Q16/Q18/R268/R271 for no used_P20 2. Change R221,R222,R224,R225,R226,R227 value to fine turn the brightness_P25 3. Change C472 to 120pF for Audio requirement_P22			