Hades_HBS 860M SV

Schematics Document

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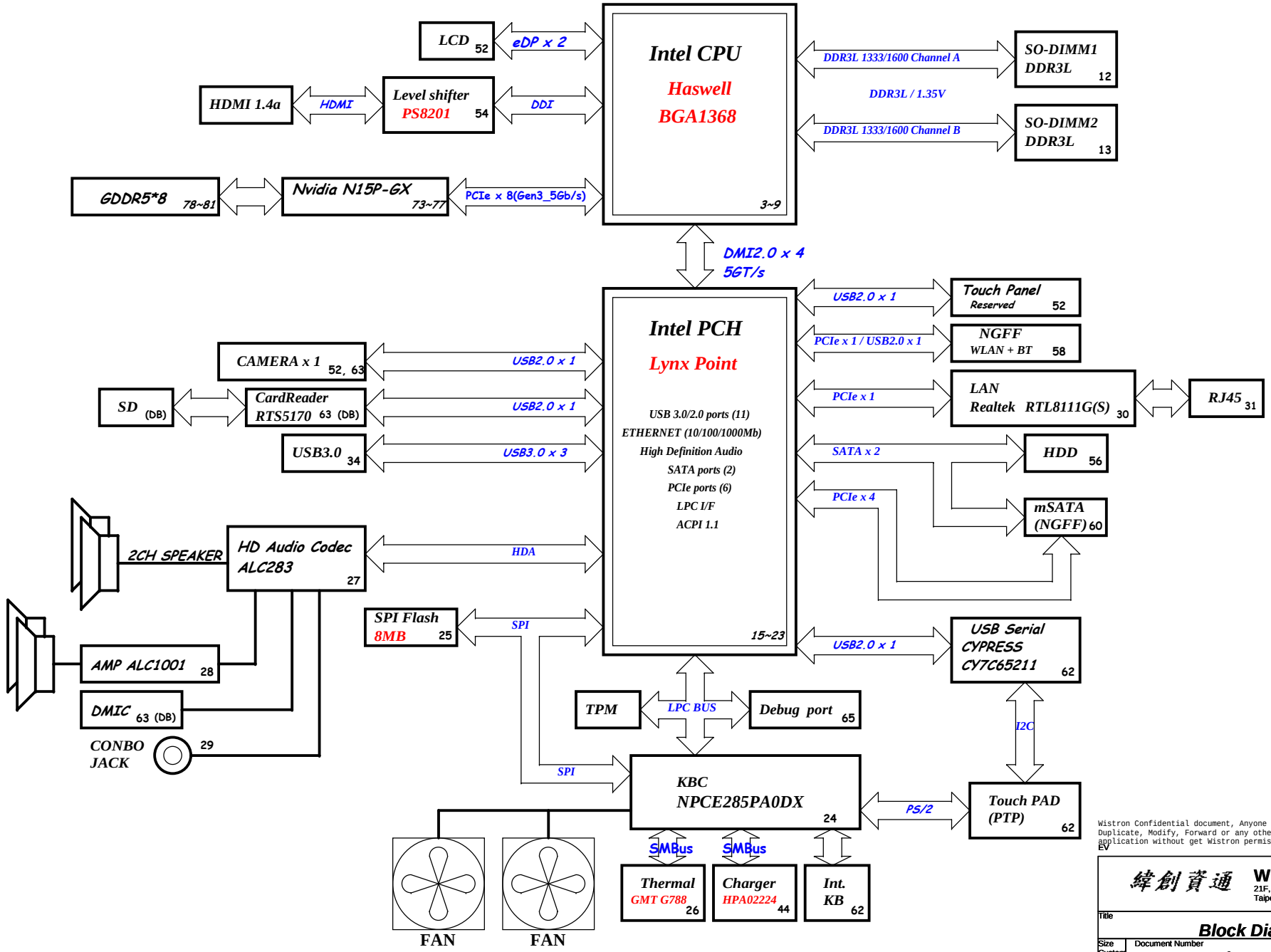
Title	Cover Page	
Size A3	Document Number Hades_HBS 860M	Rev SB
Date: Friday, April 11, 2014	Sheet 1 of 102	

Hades_HBS Board Block Diagram

Project code : 4PD02W010001
PCB P/N : 14206
Revision : SB



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Title: Block Diagram

Size	Document Number	Rev
Custom	Hades_HBS 860M	SB

Date: Friday, April 11, 2014 Sheet 2 of 102

SSID = CPU

Layout Note:
Max Length : 400 Mil
W/S (mil):12.0/15.0

R302 24D9R2F-L-GP
+VCOMP_OUT
PEG_RCOMPO 1

CPU1A 1 OF 12
HASWELL_BGA_E

Layout Note:
Max Length : 1000~8000 Mil
Max VIA : 3

Signal	Pin	Signal	Pin
17 DMI_TX_CPU_N0	DMI_TX_CPU_N0	DMI_RXN0	AB2
17 DMI_TX_CPU_N1	DMI_TX_CPU_N1	DMI_RXN1	AB3
17 DMI_TX_CPU_N2	DMI_TX_CPU_N2	DMI_RXN2	AC3
17 DMI_TX_CPU_N3	DMI_TX_CPU_N3	DMI_RXN3	AC1
17 DMI_TX_CPU_P0	DMI_TX_CPU_P0	DMI_RXP0	AB1
17 DMI_TX_CPU_P1	DMI_TX_CPU_P1	DMI_RXP1	AB4
17 DMI_TX_CPU_P2	DMI_TX_CPU_P2	DMI_RXP2	AC4
17 DMI_TX_CPU_P3	DMI_TX_CPU_P3	DMI_RXP3	AC2
17 DMI_RX_CPU_N0	DMI_RX_CPU_N0	DMI_TXN0	AF2
17 DMI_RX_CPU_N1	DMI_RX_CPU_N1	DMI_TXN1	AF4
17 DMI_RX_CPU_N2	DMI_RX_CPU_N2	DMI_TXN2	AG4
17 DMI_RX_CPU_N3	DMI_RX_CPU_N3	DMI_TXN3	AG2
17 DMI_RX_CPU_P0	DMI_RX_CPU_P0	DMI_TXP0	AF1
17 DMI_RX_CPU_P1	DMI_RX_CPU_P1	DMI_TXP1	AF3
17 DMI_RX_CPU_P2	DMI_RX_CPU_P2	DMI_TXP2	AG3
17 DMI_RX_CPU_P3	DMI_RX_CPU_P3	DMI_TXP3	AG1
17 FDI_CSYNC_CPU		FDI_CSYNC	F11
17 FDI_INT_CPU		DISP_INT	F12

DMI

FDI

PEG

Signal	Pin	Signal	Pin	Signal	Pin
PEG_RCOMP	AH6	PEG_RXN0	C10	PEG_RX_CPU_N15	73
PEG_RXN1	B10	PEG_RXN2	E9	PEG_RX_CPU_N14	73
PEG_RXN3	D9	PEG_RXN4	B9	PEG_RX_CPU_N13	73
PEG_RXN5	L5	PEG_RXN6	L2	PEG_RX_CPU_N12	73
PEG_RXN7	M4	PEG_RXN8	L4	PEG_RX_CPU_N11	73
PEG_RXN9	M2	PEG_RXN10	V5	PEG_RX_CPU_N10	73
PEG_RXN11	V4	PEG_RXN12	V1	PEG_RX_CPU_N9	73
PEG_RXN13	Y3	PEG_RXN14	Y2	PEG_RX_CPU_N8	73
PEG_RXN15	F10	PEG_RXP0	D10	PEG_RX_CPU_N7	73
PEG_RXP1	A10	PEG_RXP2	F9	PEG_RX_CPU_N6	73
PEG_RXP3	C9	PEG_RXP4	A9	PEG_RX_CPU_N5	73
PEG_RXP5	M5	PEG_RXP6	L1	PEG_RX_CPU_N4	73
PEG_RXP7	M3	PEG_RXP8	L3	PEG_RX_CPU_N3	73
PEG_RXP9	M1	PEG_RXP10	Y5	PEG_RX_CPU_N2	73
PEG_RXP11	V3	PEG_RXP12	V2	PEG_RX_CPU_N1	73
PEG_RXP13	Y4	PEG_RXP14	Y1	PEG_RX_CPU_N0	73
PEG_RXP15	B6	PEG_TXN0	C5	PEG_RX_CPU_P15	73
PEG_TXN1	E6	PEG_TXN2	D4	PEG_RX_CPU_P14	73
PEG_TXN3	G4	PEG_TXN4	E3	PEG_RX_CPU_P13	73
PEG_TXN5	J5	PEG_TXN6	G3	PEG_RX_CPU_P12	73
PEG_TXN7	J3	PEG_TXN8	J2	PEG_RX_CPU_P11	73
PEG_TXN9	T6	PEG_TXN10	R6	PEG_RX_CPU_P10	73
PEG_TXN11	R2	PEG_TXN12	R4	PEG_RX_CPU_P9	73
PEG_TXN13	T4	PEG_TXN14	T1	PEG_RX_CPU_P8	73
PEG_TXN15	C6	PEG_TXP0	B5	PEG_RX_CPU_P7	73
PEG_TXP1	D6	PEG_TXP2	E4	PEG_RX_CPU_P6	73
PEG_TXP3	G5	PEG_TXP4	E2	PEG_RX_CPU_P5	73
PEG_TXP5	J6	PEG_TXP6	G2	PEG_RX_CPU_P4	73
PEG_TXP7	J4	PEG_TXP8	J1	PEG_RX_CPU_P3	73
PEG_TXP9	T5	PEG_TXP10	R5	PEG_RX_CPU_P2	73
PEG_TXP11	R1	PEG_TXP12	R3	PEG_RX_CPU_P1	73
PEG_TXP13	T3	PEG_TXP14	T2	PEG_RX_CPU_P0	73
PEG_TXP15					

Signal	Pin	Capacitor	Part	Signal	Pin
PEG_TX_CPU_N15	B6	C310	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_N15	73
PEG_TX_CPU_N14	C5	C309	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_N14	73
PEG_TX_CPU_N13	E6	C320	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_N13	73
PEG_TX_CPU_N12	D4	C316	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_N12	73
PEG_TX_CPU_N11	G4	C318	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_N11	73
PEG_TX_CPU_N10	E3	C317	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_N10	73
PEG_TX_CPU_N9	J5	C321	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_N9	73
PEG_TX_CPU_N8	G3	C322	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_N8	73
PEG_TX_CPU_N7	J3	C307	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_N7	73
PEG_TX_CPU_N6	J2	C308	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_N6	73
PEG_TX_CPU_N5	T6	C314	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_N5	73
PEG_TX_CPU_N4	R6	C315	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_N4	73
PEG_TX_CPU_N3	R2	C311	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_N3	73
PEG_TX_CPU_N2	R4	C312	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_N2	73
PEG_TX_CPU_N1	T4	C313	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_N1	73
PEG_TX_CPU_N0	T1	C319	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_N0	73
PEG_TX_CPU_P15	C6	C324	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_P15	73
PEG_TX_CPU_P14	B5	C337	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_P14	73
PEG_TX_CPU_P13	D6	C338	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_P13	73
PEG_TX_CPU_P12	E4	C335	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_P12	73
PEG_TX_CPU_P11	G5	C333	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_P11	73
PEG_TX_CPU_P10	E2	C336	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_P10	73
PEG_TX_CPU_P9	J6	C339	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_P9	73
PEG_TX_CPU_P8	G2	C334	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_P8	73
PEG_TX_CPU_P7	J4	C323	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_P7	73
PEG_TX_CPU_P6	J1	C329	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_P6	73
PEG_TX_CPU_P5	T5	C330	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_P5	73
PEG_TX_CPU_P4	R5	C326	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_P4	73
PEG_TX_CPU_P3	R1	C327	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_P3	73
PEG_TX_CPU_P2	R3	C328	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_P2	73
PEG_TX_CPU_P1	T3	C331	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_P1	73
PEG_TX_CPU_P0	T2	C332	SCD22U10V2KX-L1-GP Muxless	PEG_TX_CON_P0	73

HASWELL-5-GP-NF
71.HASWE.D0U

x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Pro-cessor	Physical Lanes 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
x16	Off	Off	Reverse	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

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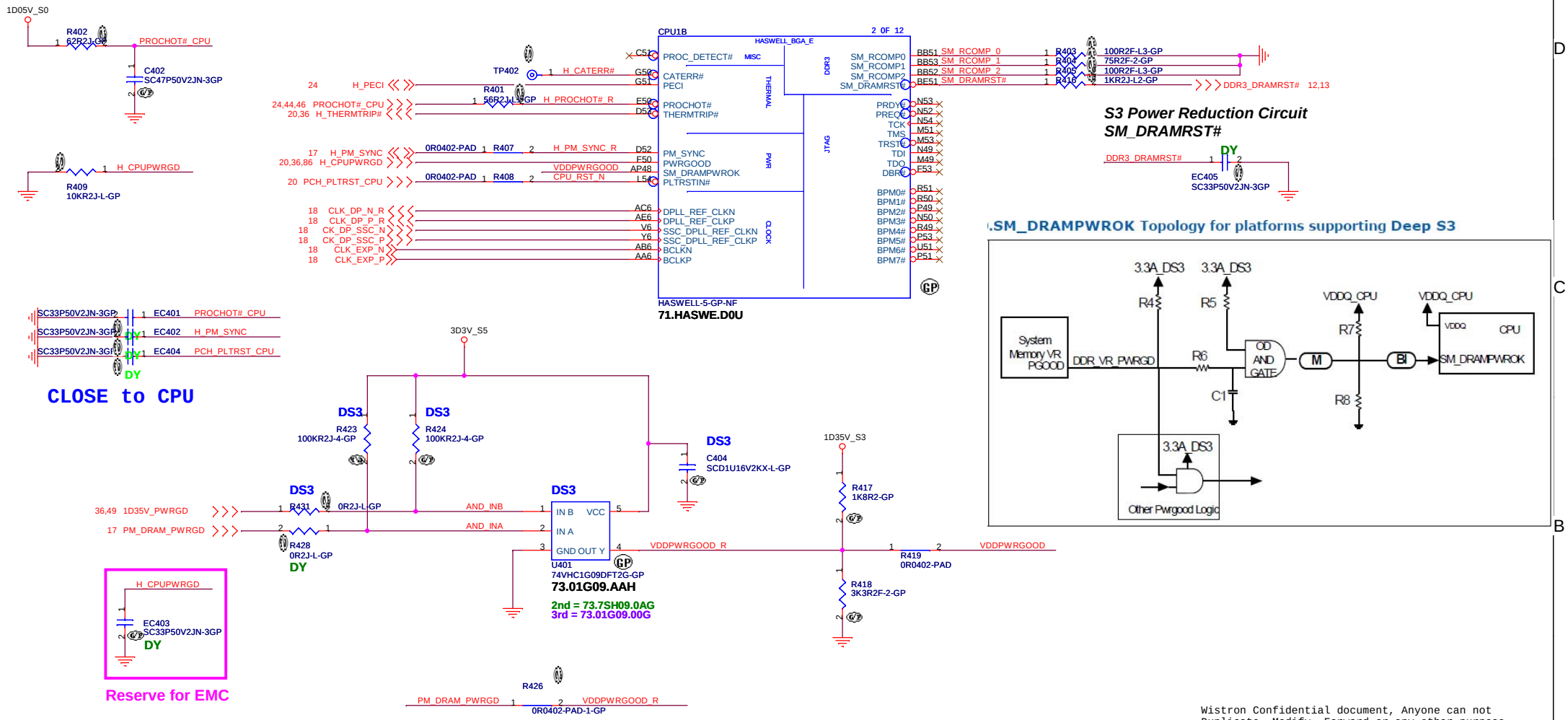
Title: **CPU (PCIE/DMI/FDI)**

Size: Custom | Document Number: Hades_HBS 860M | Rev: SB

Date: Friday, April 11, 2014 | Sheet 3 of 102

SSID = CPU



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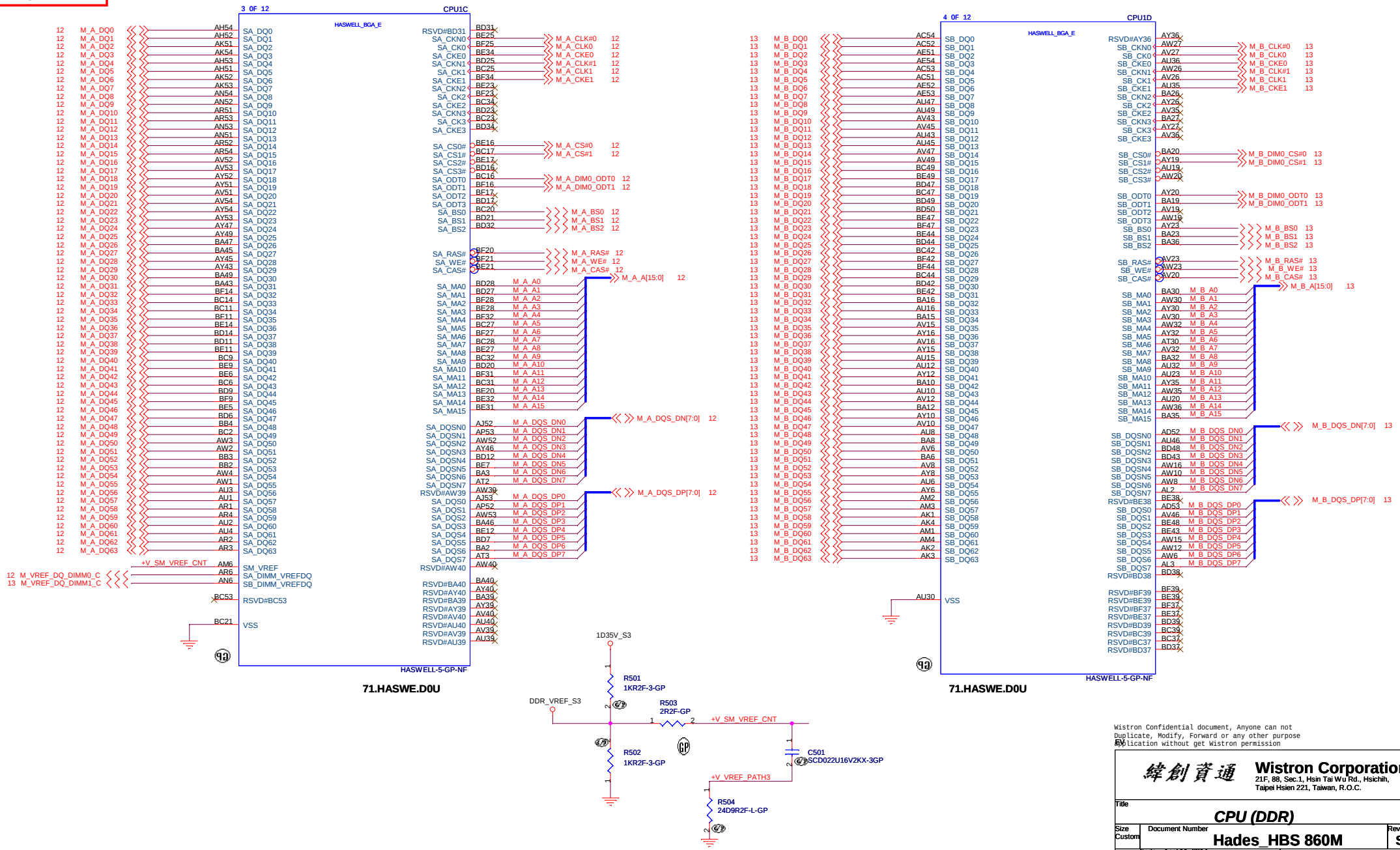
Title: CPU (THERMAL/CLOCK/PM)

Size: Custom | Document Number: Hades_HBS 860M | Rev: SB

Date: Wednesday, May 28, 2014 | Sheet 4 of 102

SSID = CPU



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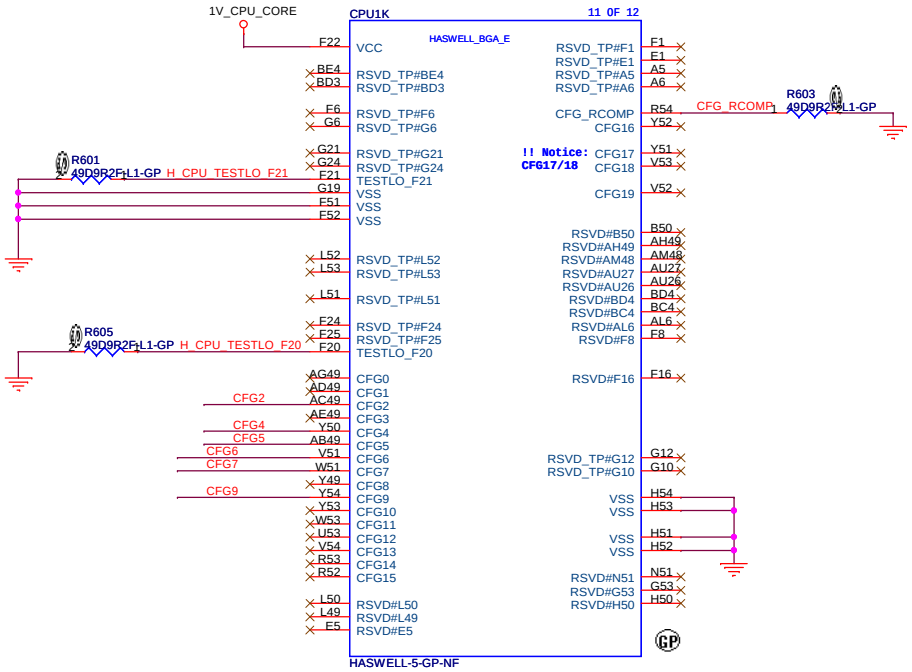
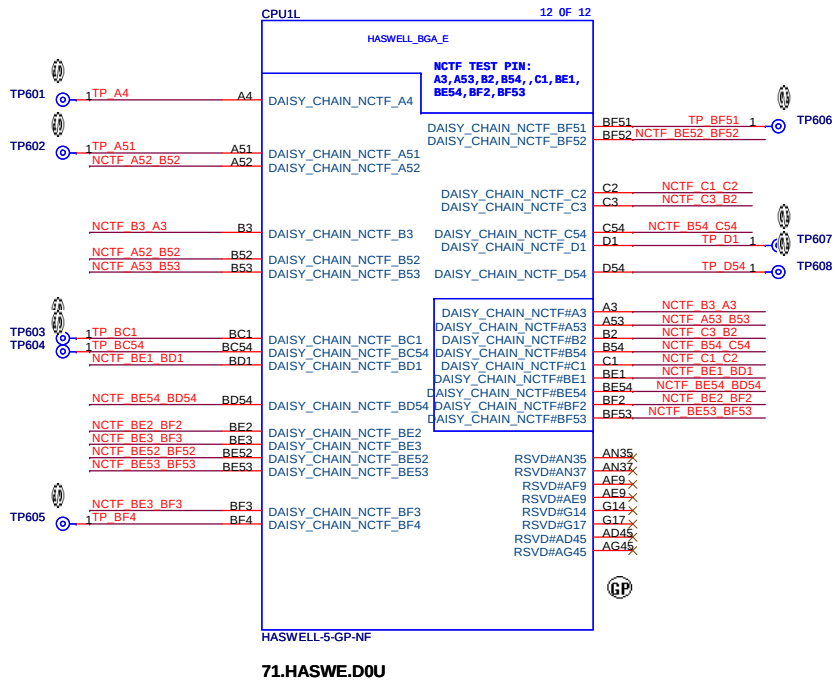
Title: **CPU (DDR)**

Size	Document Number	Rev
Custom	Hades_HBS 860M	SB

Date: Friday, April 11, 2014 Sheet 5 of 102

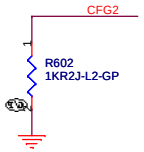
SSID = CPU

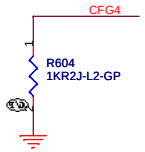




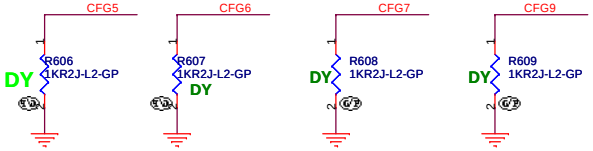
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

eDP Enable	
CFG4	1:Disable 0:Enable





PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



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Title: CPU (CFG)

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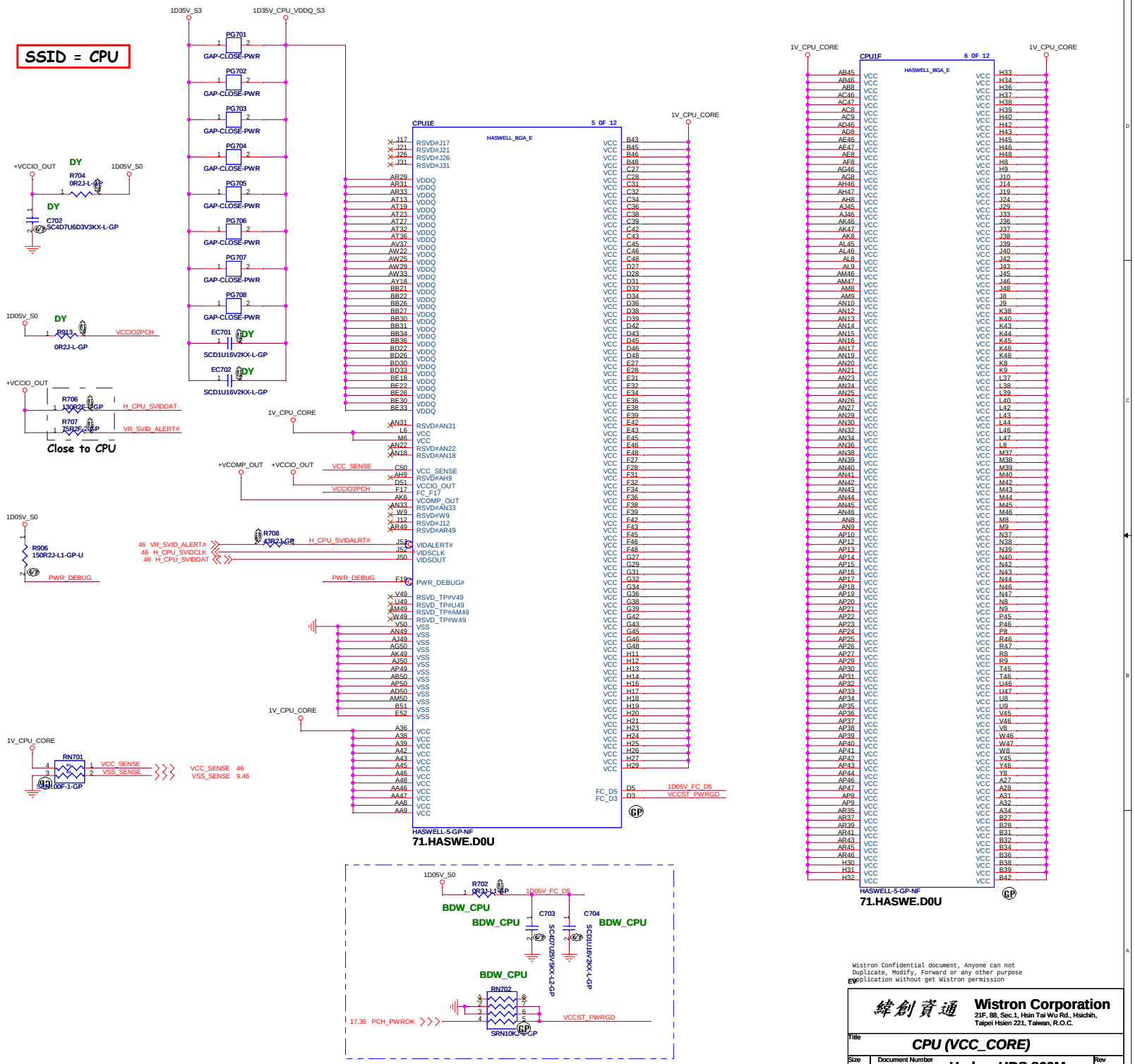
Date: Friday, April 11, 2014 | Sheet 6 of 102



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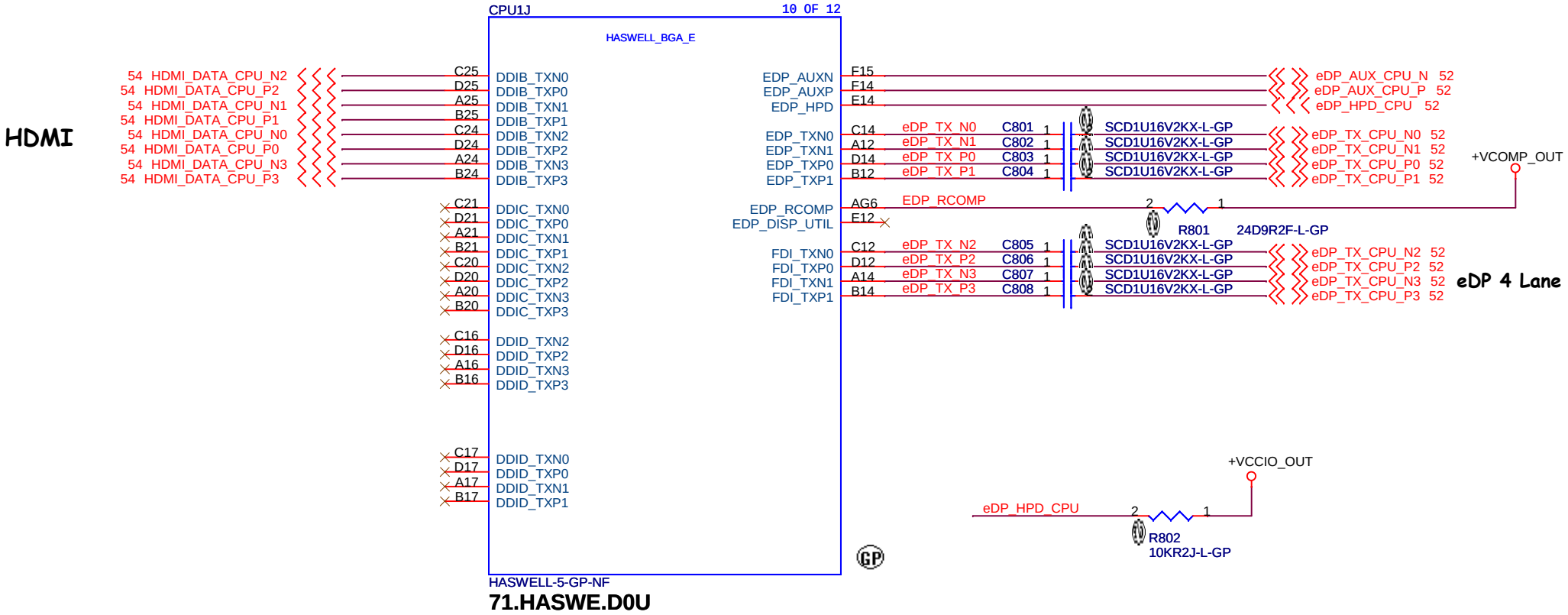
Title	CPU (VCC_CORE)	
Size: Custom	Document Number: Hades_HBS 860M	Rev: SB
Date: Monday, May 26, 2014	Sheet 7 of 102	

SSID = CPU



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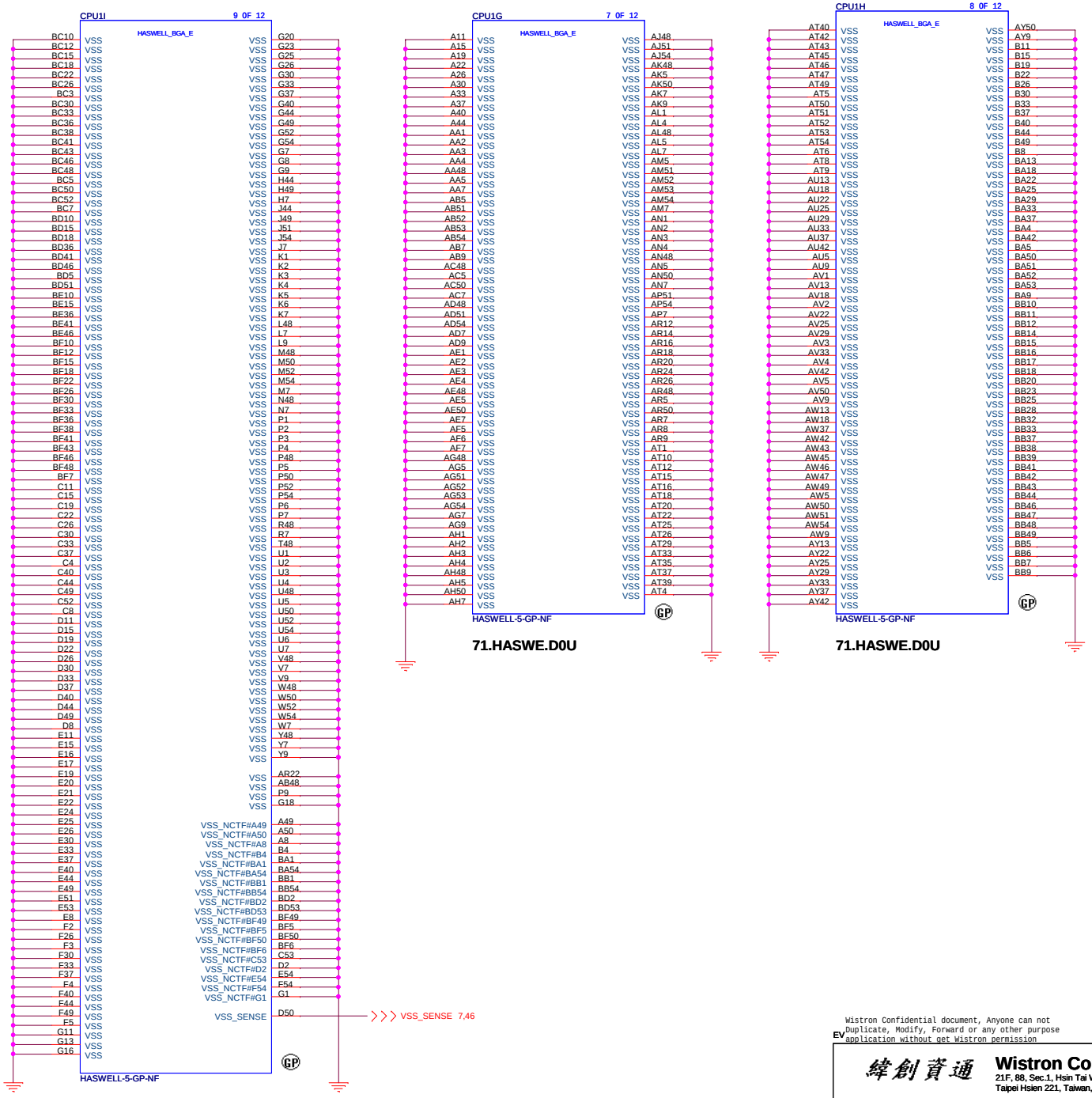
Title	CPU (DDI/EDP)	
Size A4	Document Number Hades_HBS 860M	Rev SB
Date: Friday, April 11, 2014	Sheet 8 of 102	

SSID = CPU



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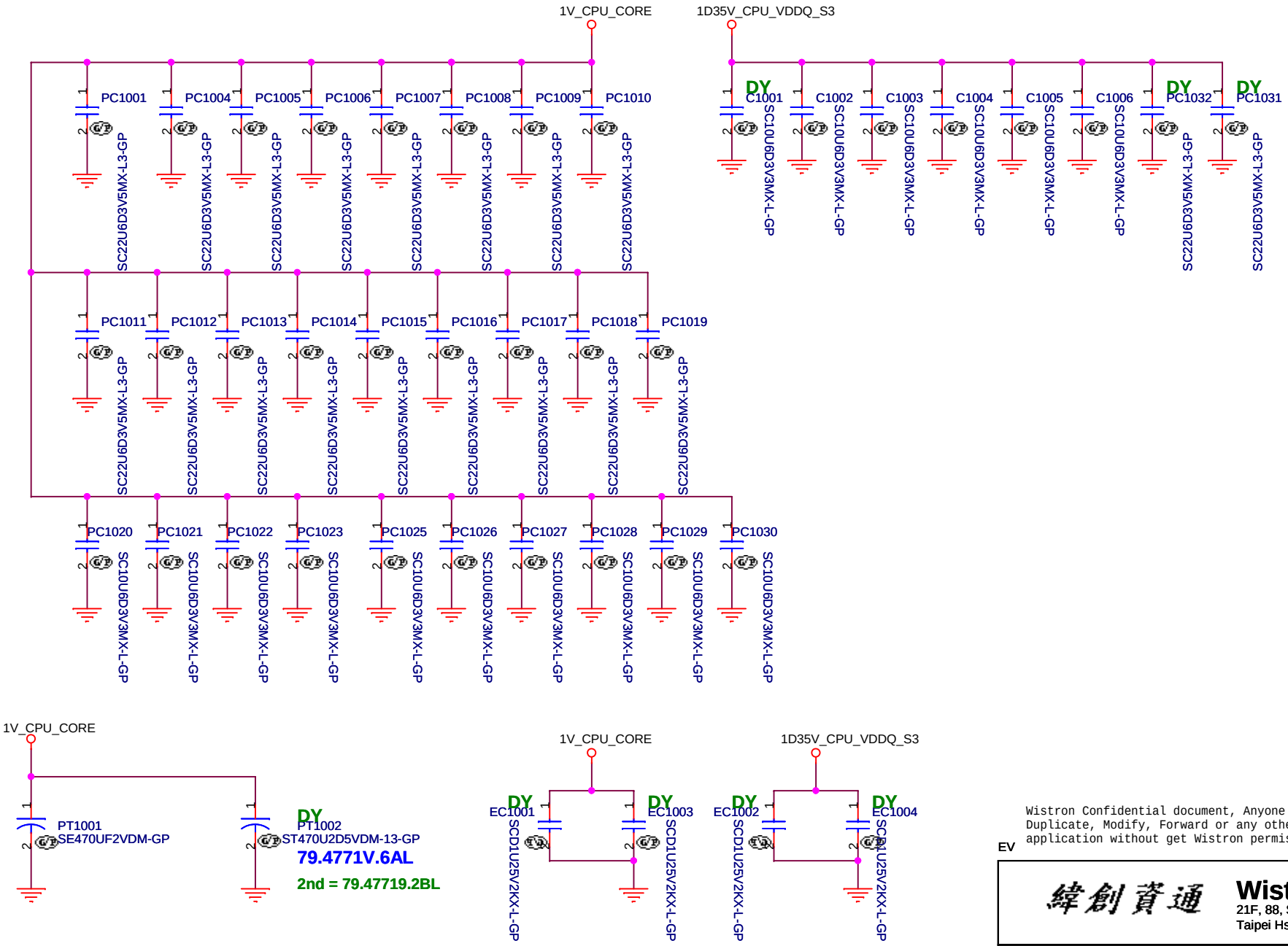
Title: **CPU (VSS)**

Size: Custom | Document Number: **Hades_HBS 860M** | Rev: **SB**

Date: Friday, April 11, 2014 | Sheet 9 of 102



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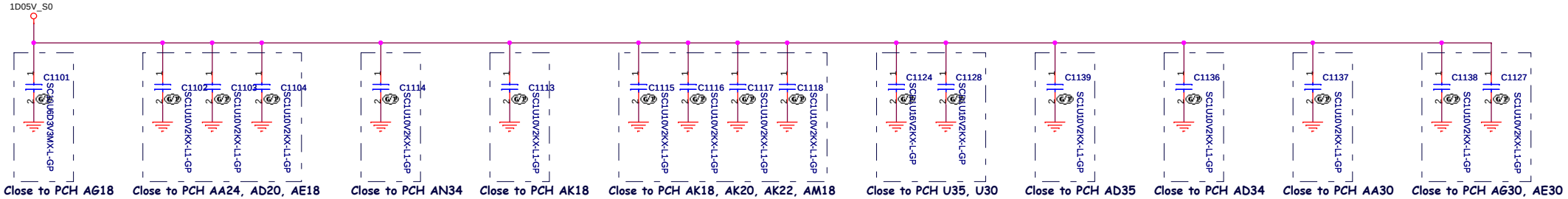
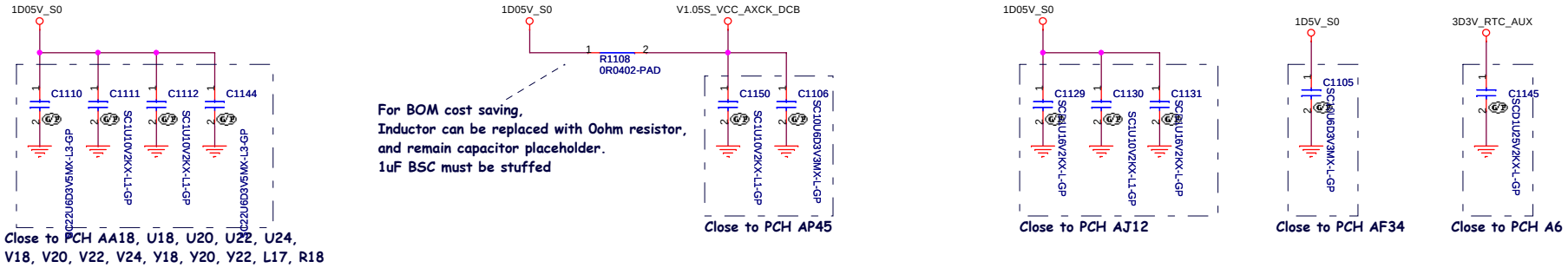
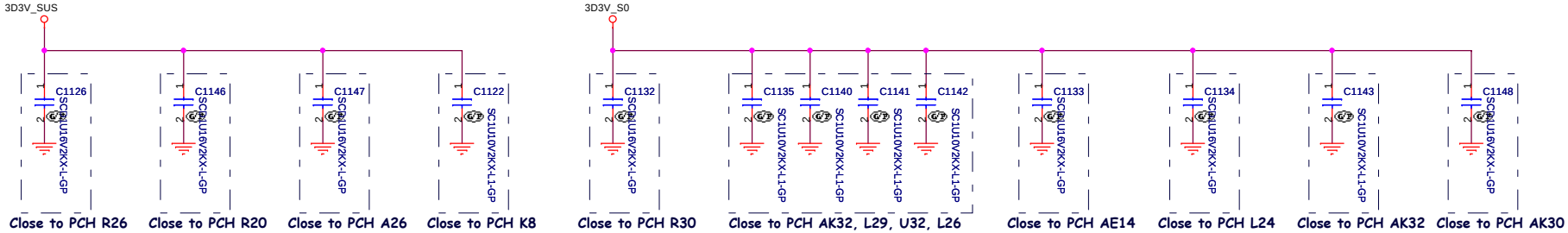
Title: **CPU (Power CAP1)**

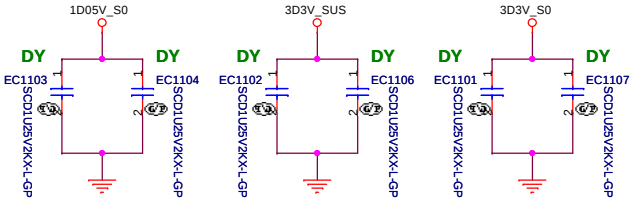
Size	Document Number	Rev
A4	Hades HBS 860M	SB

Date: Friday, April 11, 2014 Sheet 10 of 102









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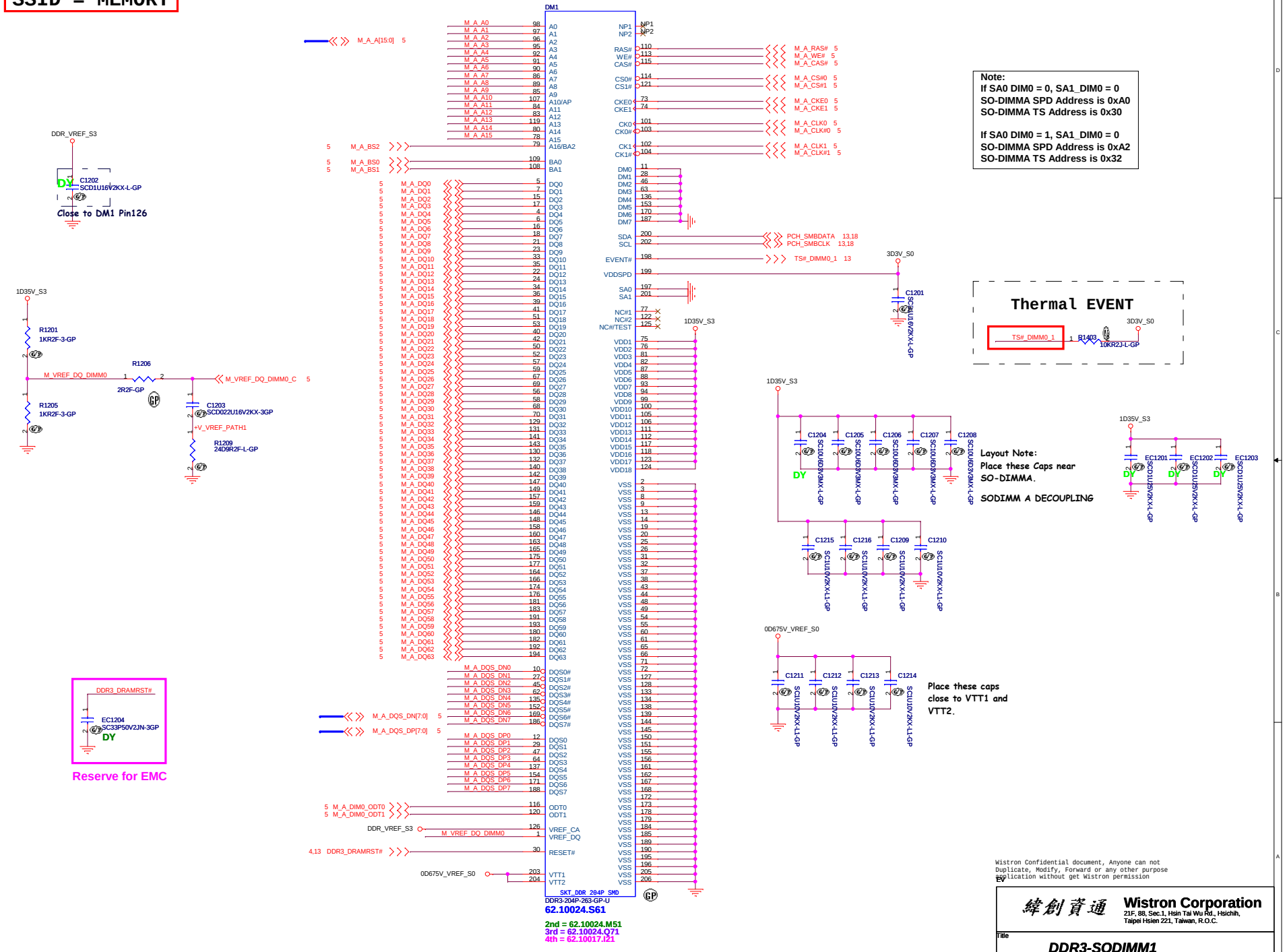
Title: ***CPU (Power CAP2)***

Size	Document Number	Rev
A3	**Hades HBS 860M**	**SB**

Date: Wednesday, May 28, 2014 Sheet 11 of 102

SSID = MEMORY



Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT

TS#_DIMM0_1 — R1403 10KR2J-L-GP — 3D3V_S0

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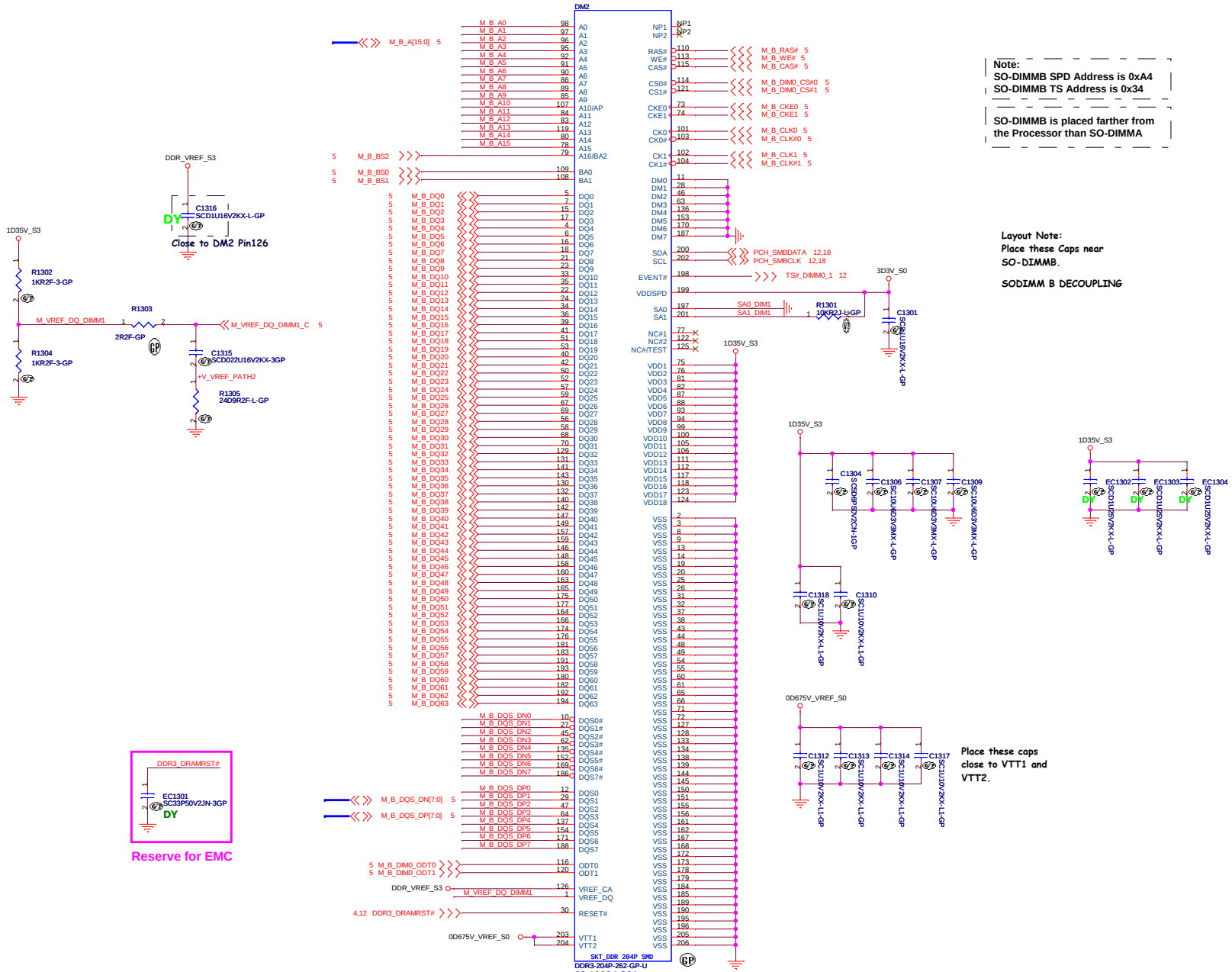
Title: DDR3-SODIMM1

Size	Document Number	Rev
Custom	Hades_HBS 860M	SB

Date: Friday, April 11, 2014 Sheet 12 of 102

SSID = MEMORY



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

Layout Note:
Place these Caps near SO-DIMMB.

SODIMM B DECOUPLING

Place these caps close to VTT1 and VTT2.

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Title: DDR3-SODIMM2

Size	Document Number	Rev
Custom	Hades_HBS 860M	SB

Date: Friday, April 11, 2014 Sheet 13 of 102

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Title
(Reserved)_SODIMM _SODIMM4

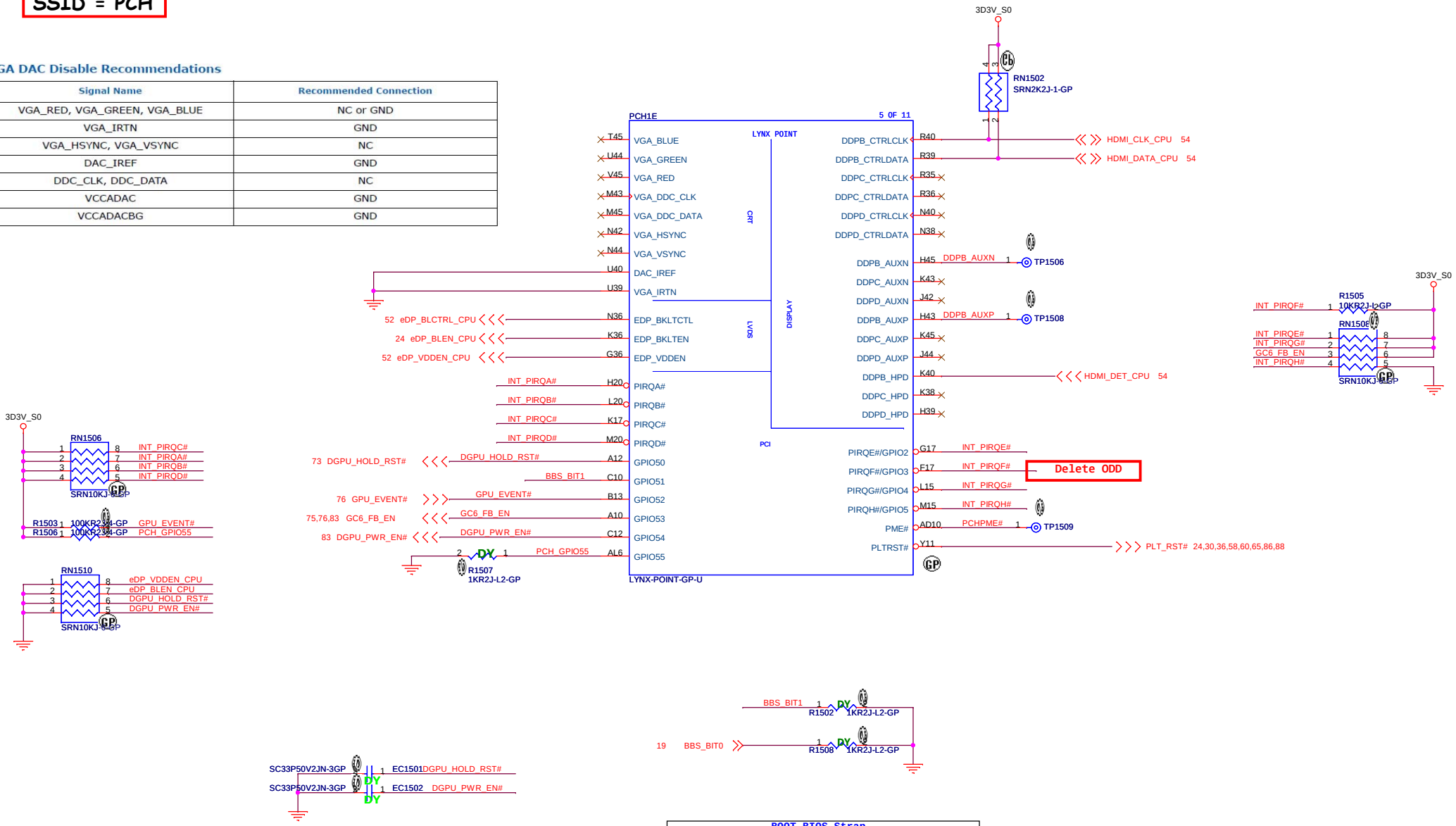
Size	Document Number	Rev
Custom	Hades_HBS 860M	SB

Date: Friday, April 11, 2014 Sheet 14 of 102

SSID = PCH

VGA DAC Disable Recommendations

Signal Name	Recommended Connection
VGA_RED, VGA_GREEN, VGA_BLUE	NC or GND
VGA_IRTN	GND
VGA_HSYNC, VGA_VSYNC	NC
DAC_IREF	GND
DDC_CLK, DDC_DATA	NC
VCCADAC	GND
VCCADACBG	GND



BOOT BIOS Strap		
GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

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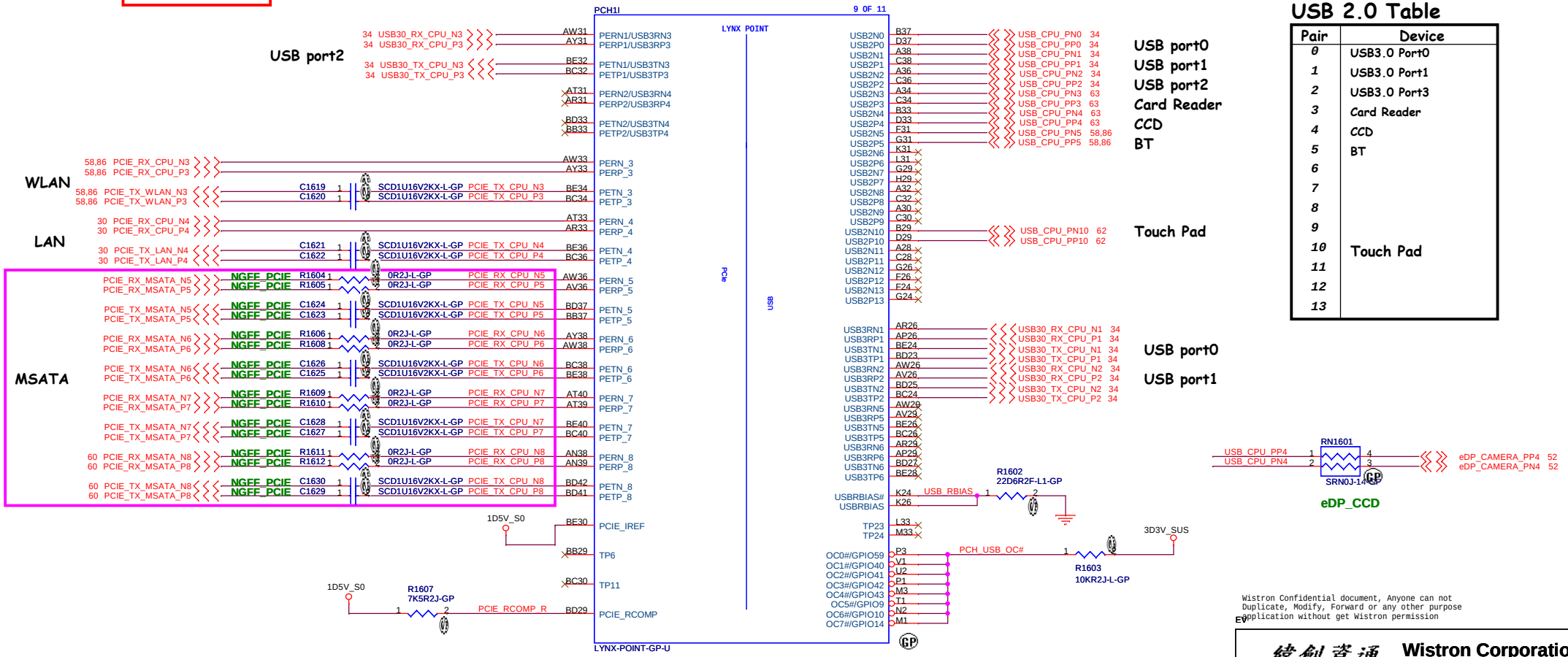
Title: CPU(EDP SIDEBAND/GPIO/DDI)

Size: A3 | Document Number: Hades_HBS 860M | Rev: SB

Date: Friday, April 11, 2014 | Sheet 15 of 102

SSID = PCH



USB 2.0 Table

Pair	Device
0	USB3.0 Port0
1	USB3.0 Port1
2	USB3.0 Port3
3	Card Reader
4	CCD
5	BT
6	
7	
8	
9	
10	Touch Pad
11	
12	
13	

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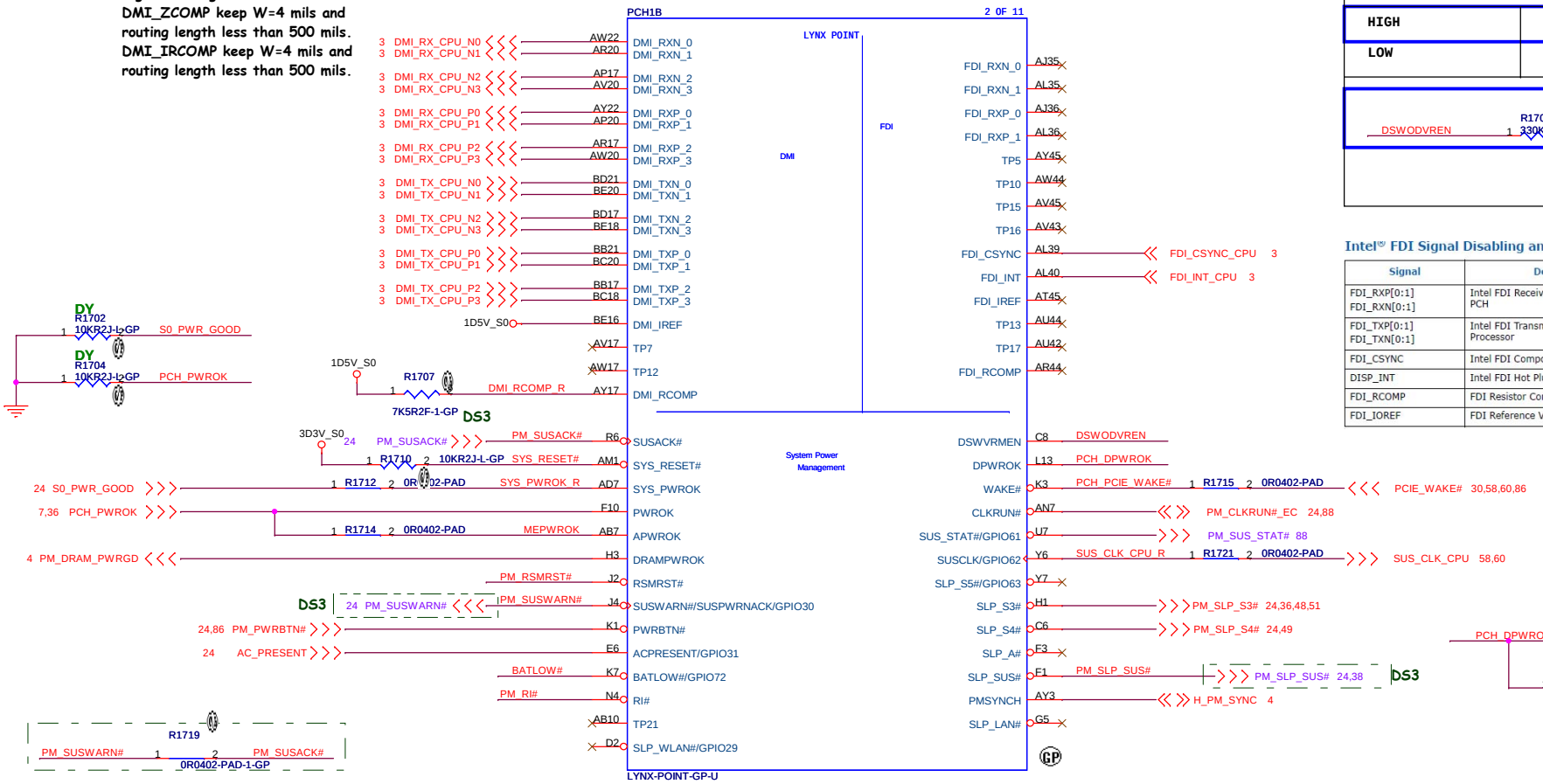
Title: CPU (PCI/USB)

Size: Custom | Document Number: Hades_HBS 860M | Rev: SB

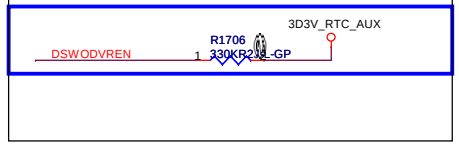
Date: Friday, May 23, 2014 | Sheet 16 of 102

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled



Intel® FDI Signal Disabling and Termination Guidelines

Signal	Description	Disable Guidelines
FDI_RXP[0:1] FDI_RXN[0:1]	Intel FDI Receive Differential Pair on PCH	Float
FDI_TXP[0:1] FDI_TXN[0:1]	Intel FDI Transmit Differential Pair on Processor	Float
FDI_CSYNC	Intel FDI Composite Sync	Connect to Processor and PCH
DISP_INT	Intel FDI Hot Plug Interrupt	Connect to Processor and PCH
FDI_RCOMP	FDI Resistor Compensation	Float
FDI_IOREF	FDI Reference Voltage	Float

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Title: CPU (DMI/FDI/PM)

Size: A3 | Document Number: Hades_HBS 860M | Rev: SB

Date: Wednesday, May 28, 2014 | Sheet 17 of 102

SSID = PCH

3D3V_SUS

RN1802 SRN10KJ-6-GP
1 EC_SW# 8
2 LAN_CLKREQ_CPU# 7
3 PCIE_CLKRQ0# 6
4 PEG_CLKREQ_CPU# 5

RN1805 SRN10KJ-6-GP
1 PCH_GPIO57 8 — PCH_GPIO57 20
2 PCIE_CLKRQ7# 7
3 PCIE_CLKRQ5# 6
4 MSATA_CLKREQ_CPU# 5

3D3V_S0

RN1807 SRN10KJ-6-GP
1 PCIE_CLKRQ1# 4
2 WLAN_CLKREQ_CPU# 3

PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only

PCH1C — LYNX POINT — 3 OF 11

Signal	Pin	Net
CLKOUT_PCIE_N_0	Y43	
CLKOUT_PCIE_P_0	Y45	
PCIECLKRQ0#/GPIO73	AB1	PCIE_CLKRQ0#
CLKOUT_PCIE_N_1	AA44	
CLKOUT_PCIE_P_1	AA42	
PCIECLKRQ1#/GPIO18	AF1	PCIE_CLKRQ1#
CLKOUT_PCIE_N_2	AB43	58,86 WLAN_CLK_CPU#
CLKOUT_PCIE_P_2	AB45	58,86 WLAN_CLK_CPU
PCIECLKRQ2#/GPIO20/SMI#	AF3	WLAN_CLKREQ_CPU# — 58,86 WLAN_CLKREQ_CPU#
CLKOUT_PCIE_N_3	AD43	30 LAN_CLK_CPU#
CLKOUT_PCIE_P_3	AD45	30 LAN_CLK_CPU
PCIECLKRQ3#/GPIO25	T3	LAN_CLKREQ_CPU# — 30 LAN_CLKREQ_CPU#
CLKOUT_PCIE_N_4	AF43	MSATA_CLK_CPU#
CLKOUT_PCIE_P_4	AF45	MSATA_CLK_CPU
PCIECLKRQ4#/GPIO26	V3	MSATA_CLKREQ_CPU# — MSATA_CLKREQ_CPU#
CLKOUT_PCIE_N_5	AE44	
CLKOUT_PCIE_P_5	AE42	
PCIECLKRQ5#/GPIO44	AA2	PCIE_CLKRQ5#
CLKOUT_PCIE_N_6	AB40	
CLKOUT_PCIE_P_6	AB39	
PCIECLKRQ6#/GPIO45	AE4	PCIE_CLKRQ6# — 20 PCIE_CLKRQ6#
CLKOUT_PCIE_N_7	AJ44	
CLKOUT_PCIE_P_7	AJ42	
PCIECLKRQ7#/GPIO46	Y3	PCIE_CLKRQ7#
CLKOUT_ITPXDP_N	AH43	
CLKOUT_ITPXDP_P	AH45	
CLKOUT_33MHZ0	D44	TP1813 — CLK_33MHZ0
CLKOUT_33MHZ1	E44	88 CLK_PCI_TPM — R1805 22R2J-L1-GP — CLK_PCI_TPM_R
CLKOUT_33MHZ2	B42	CLK_PCI_FB — R1801 22R2J-L1-GP — CLK_PCI_FB_R
CLKOUT_33MHZ3	F41	65 CLK_PCI_LPC — R1808 22R2J-L1-GP — CLK_PCI_LPC_R
CLKOUT_33MHZ4	A40	24 CLK_PCI_KBC — R1809 22R2J-L1-GP — CLK_PCI_KBC_R

CLOCK SIGNAL

Signal	Pin	Net
CLKOUT_PEG_A_N	AB35	PEG_CLK_CPU# 73
CLKOUT_PEG_A_P	AB36	PEG_CLK_CPU 73
PEGA_CLKRQ#/GPIO47	AF6	PEG_CLKREQ_CPU# — PEG_CLKREQ_CPU# 73
CLKOUT_PEG_B_N	Y39	
CLKOUT_PEG_B_P	Y38	
PEGB_CLKRQ#/GPIO56	U4	RTC_DET# — RTC_DET# 25
CLKOUT_DMI_N	AF39	CLK_EXP_N 4
CLKOUT_DMI_P	AF40	CLK_EXP_P 4
CLKOUT_DP_N	AJ40	CK_DP_SSC_N 4
CLKOUT_DP_P	AJ39	CK_DP_SSC_P 4
CLKOUT_DPNS_N	AF35	CLK_DP_N_R 4
CLKOUT_DPNS_P	AF36	CLK_DP_P_R 4
CLKIN_DMI_N	AY24	CLK_BUF_EXP_N
CLKIN_DMI_P	AW24	CLK_BUF_EXP_P
CLKIN_GND_N	AR24	CLK_BUF_CPYCLK_N
CLKIN_GND_P	AT24	CLK_BUF_CPYCLK_P
CLKIN_DOT96N	H33	CLK_BUF_DOT96_N
CLKIN_DOT96P	G33	CLK_BUF_DOT96_P
CLKIN_SATA_N	BE6	CLK_BUF_CKSSCD_N
CLKIN_SATA_P	BC6	CLK_BUF_CKSSCD_P
REFCLK14IN	F45	CLK_BUF_REF14
CLKIN_33MHZLOOPBACK	D17	CLK_PCI_FB
XTAL25_OUT	AL44	XTAL25_IN
XTAL25_IN	AM43	XTAL25_OUT
CLKOUTFLEX0/GPIO64	C40	
CLKOUTFLEX1/GPIO65	F38	
CLKOUTFLEX2/GPIO66	F36	
CLKOUTFLEX3/GPIO67	F39	DGPU_TYPE1 20
ICLK_IREF	AM45	1D5V_S0
TP18	AD38	
TP19	AD39	
DIFFCLK_BIASREF	AN44	DIFFCLK_R — R1810 7K5R2F-1-GP — 1D5V_S0

LYNX-POINT-GP-U

RN1806 SRN10KJ-5-GP

GPU PEG BUS

RN1803 SRN10KJ-6-GP
CLK_BUF_REF14 1 — 8
CLK_BUF_DOT96_N 2 — 7
CLK_BUF_DOT96_P 3 — 6
4 — 5

Need very close to PCH

RN1804 SRN10KJ-6-GP
CLK_BUF_CKSSCD_P 1 — 8
CLK_BUF_CKSSCD_N 2 — 7
CLK_BUF_EXP_P 3 — 6
CLK_BUF_EXP_N 4 — 5

3D3V_S5

RTC_DET# 1 — R1804 10KR2J-L-GP

XTAL25_IN — C1801 SC15P50V2JN-L-GP
R1806 1MR2F-GP
X1801 XTAL-25MHZ-102-GP
82.30020.851
2nd = 82.30020.791
XTAL25_OUT — C1802 SC15P50V2JN-L-GP

3D3V_SUS

RN1809 SRN2K2J-1-GP
SMB_CLK 4 — 1
SMB_DATA 3 — 2

RN1810 SRN2K2J-1-GP
SML0_DATA 3 — 2
SML0_CLK 4 — 1

RN1811 SRN2K2J-1-GP
SML1_CLK 3 — 2
SML1_DATA 4 — 1

RN1813 SRN10KJ-5-GP
PCH_GPIO74 1 — 4
PCH_GPIO60 2 — 3

CLK_PCI_TPM — EC1801 SC33P50V2JN-3GP DY
CLK_PCI_LPC — EC1802 SC33P50V2JN-3GP DY
CLK_PCI_KBC — EC1803 SC33P50V2JN-3GP DY

Reserve for EMC

3D3V_S0

R1813 10KR2J-L-GP — INT_SERIRQ

PCH1D — LYNX POINT — 4 OF 11

LPC

Signal	Pin	Net
LAD_0	A20	24,65,88 LPC_AD_CPU_P0
LAD_1	C20	24,65,88 LPC_AD_CPU_P1
LAD_2	A18	24,65,88 LPC_AD_CPU_P2
LAD_3	C18	24,65,88 LPC_AD_CPU_P3
LFRAME#	B21	24,65,88 LPC_FRAME#_CPU
LDRQ0#	D21	
LDRQ1#/GPIO23	G20	
SERIRQ	AL11	INT_SERIRQ — 24,88 INT_SERIRQ

SPI

Signal	Pin	Net
SPI_CLK	AJ11	24,25 SPI_CLK_CPU
SPI_CS0#	AJ7	24,25 SPI_CS_CPU_N0
SPI_CS1#	AL7	
SPI_CS2#	AJ10	
SPI_MOSI	AH1	24,25 SPI_SI_CPU
SPI_MISO	AH3	24,25 SPI_SO_CPU
SPI_IO2	AJ4	25 SPI_WP_CPU
SPI_IO3	AJ2	25 SPI_HOLD_CPU

SMBus

Signal	Pin	Net
SMBALERT#/GPIO11	N7	EC_SW#
SMBCLK	R10	SMB_CLK
SMBDATA	U11	SMB_DATA
SML0ALERT#/GPIO60	N8	PCH_GPIO60
SML0CLK	U8	SML0_CLK
SML0DATA	R7	SML0_DATA
SML1ALERT#/PCHHOT#/GPIO74	H6	PCH_GPIO74
SML1CLK/GPIO58	K6	SML1_CLK 24,26,76
SML1DATA/GPIO75	N11	SML1_DATA 24,26,76

C-Link

Signal	Pin
CL_CLK	AF11
CL_DATA	AF10
CL_RST#	AF7

Thermal

Signal	Pin
TP1	BA45
TP2	BC45
TP3	BE44
TP4	BE43
TD_IREF	AY43

TS_IREF — R1818 8K2R2F-2-GP

LYNX-POINT-GP-U

3D3V_S0

RN1808 SRN2K2J-1-GP
1 — 4
2 — 3

Q1801 2N7002KDW-GP
84.2N702.A3F
2nd = 75.00601.07C

SMB_DATA — PCH_SMBDATA 12,13
SMB_CLK — PCH_SMBCLK 12,13

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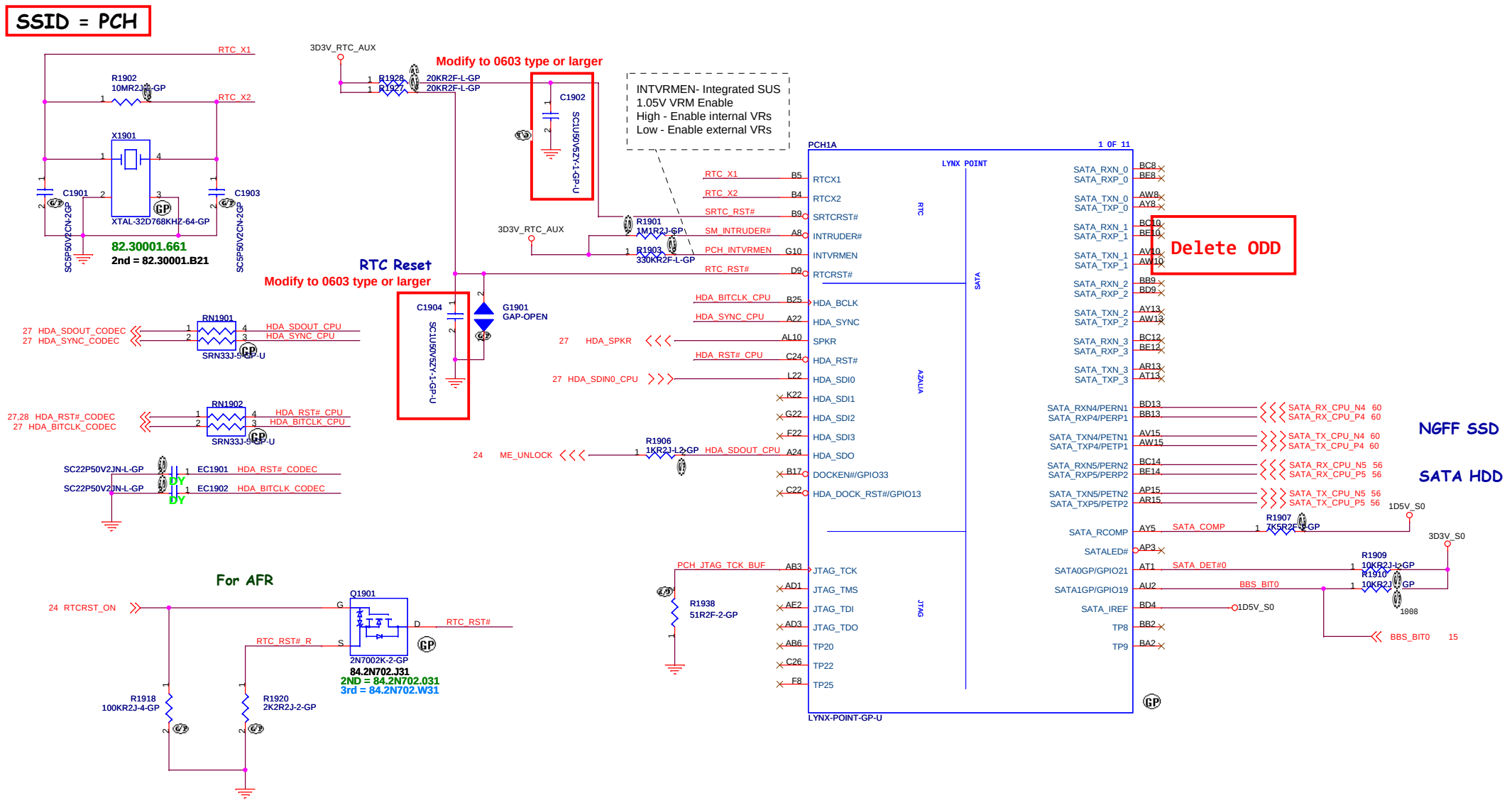
Title: CPU (PCI-E/SMBUS/CLOCK/CL)

Size	Document Number	Rev
Custom	Hades_HBS 860M	SB

Date: Friday, April 11, 2014 — Sheet 18 of 102



HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

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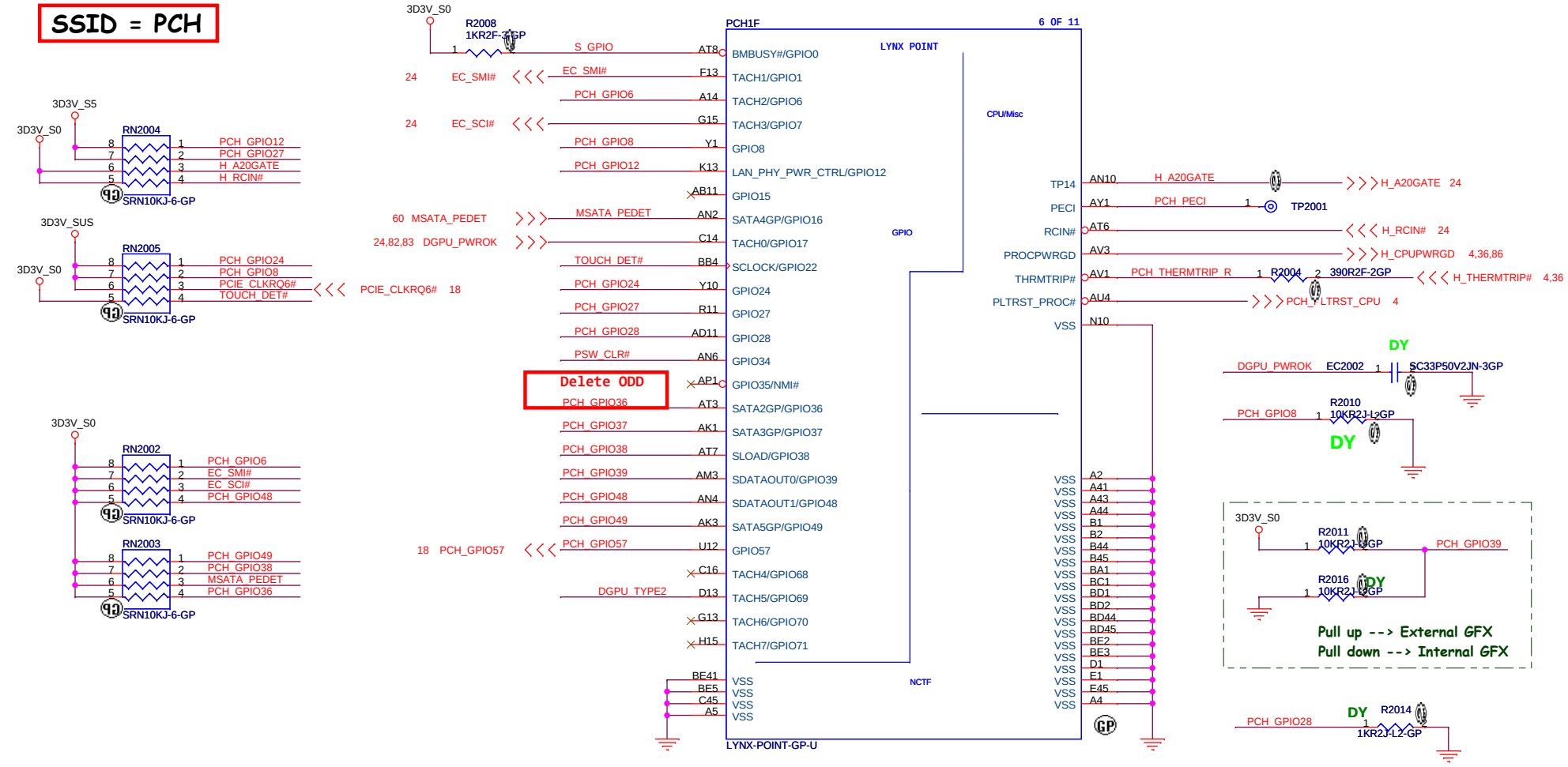
Title: **CPU (RTC/LPC/SATA/HDA)**

Size: Custom | Document Number: **Hades_HBS 860M** | Rev: **SB**

Date: Friday, April 11, 2014 | Sheet 19 of 102

SSID = PCH



PLL ON DIE VR ENABLE
ENABLED -- HIGH (R2013 UNSTUFFED) DEFAULT DISABLED -- LOW (R2013 STUFFED)

TLS Confidentiality
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality)

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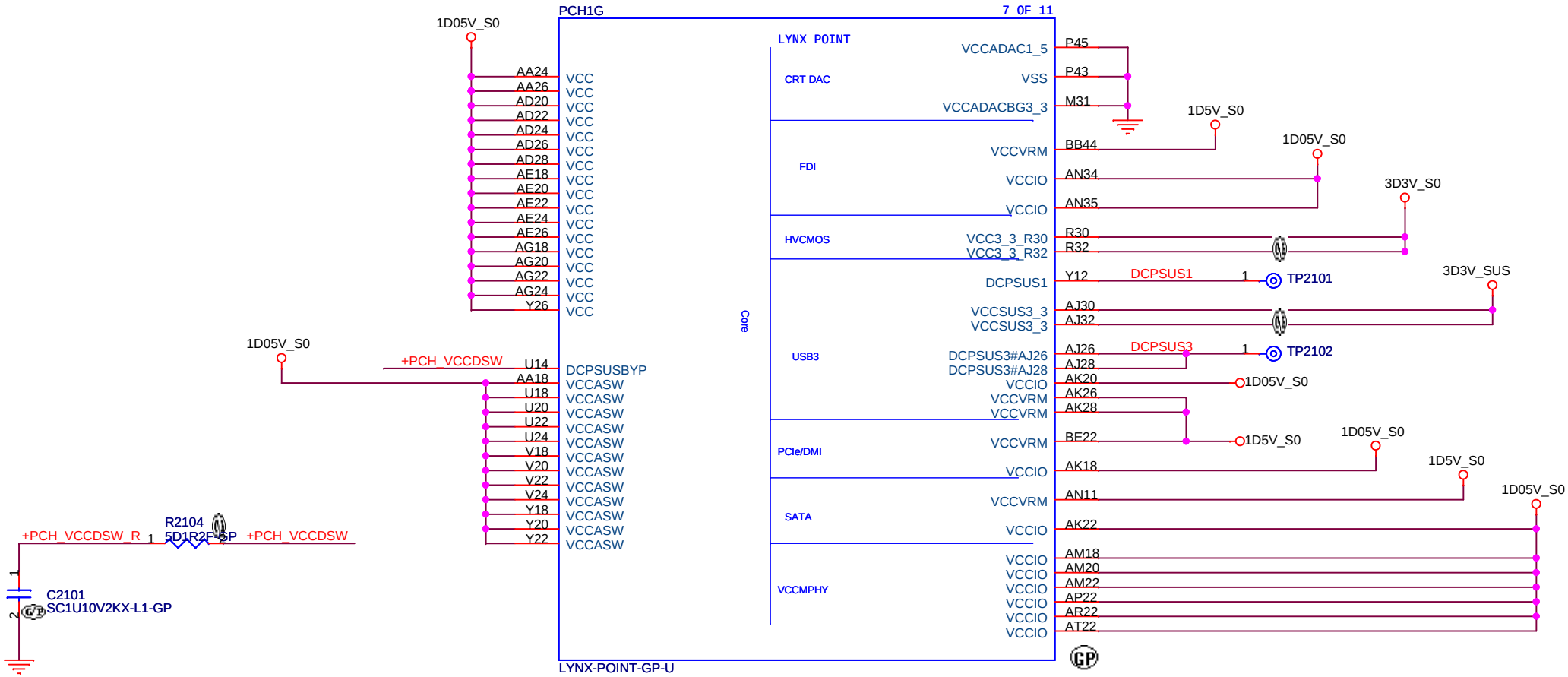
Title: CPU (GPIO/MISC)

Size: Custom | Document Number: Hades_HBS 860M | Rev: SB

Date: Thursday, May 29, 2014 | Sheet 20 of 102

SSID = PCH



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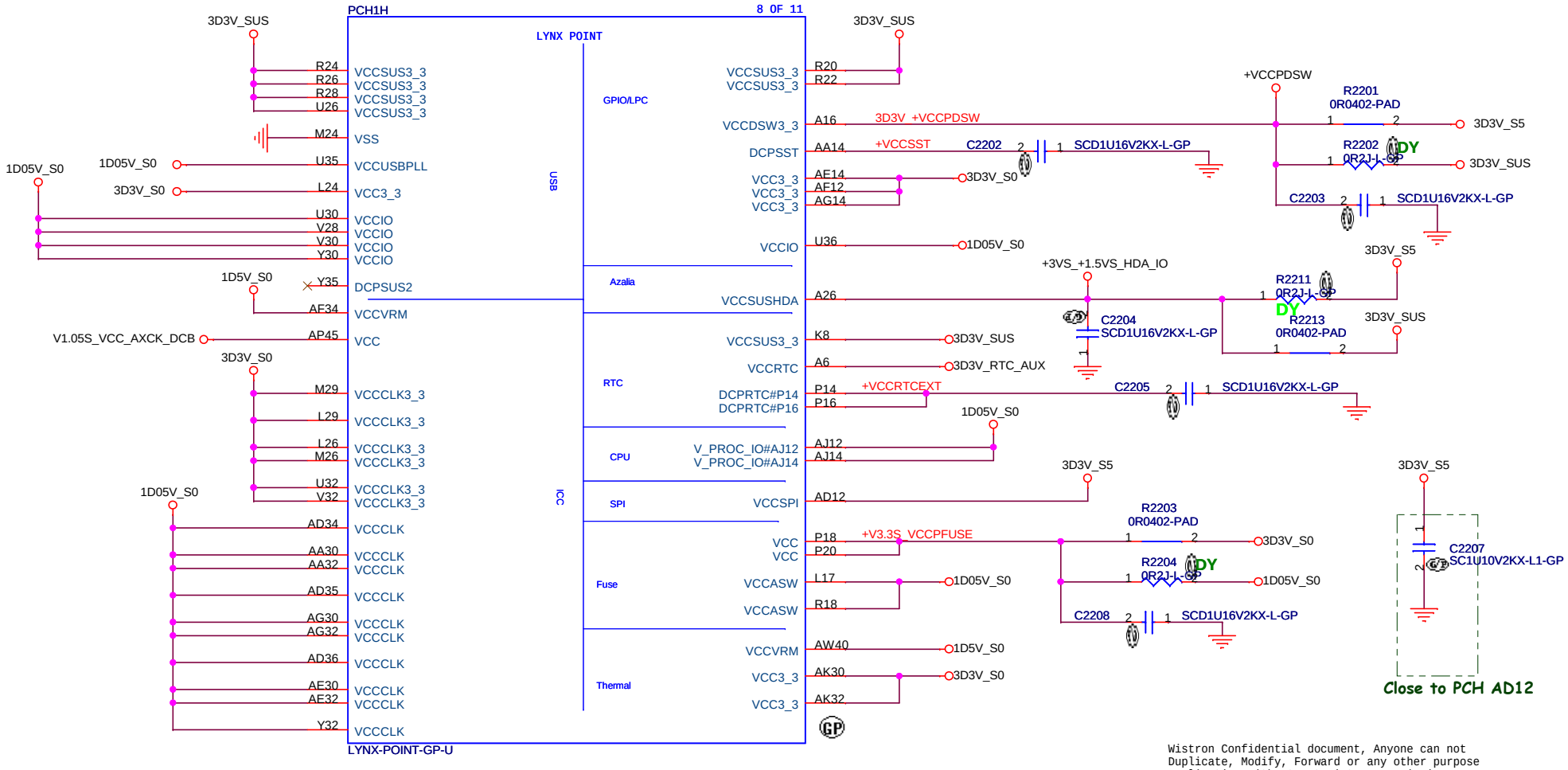
Title	CPU (POWER1)	
Size A4	Document Number Hades_HBS 860M	Rev SB
Date: Friday, April 11, 2014	Sheet 21 of 102	

SSID = PCH



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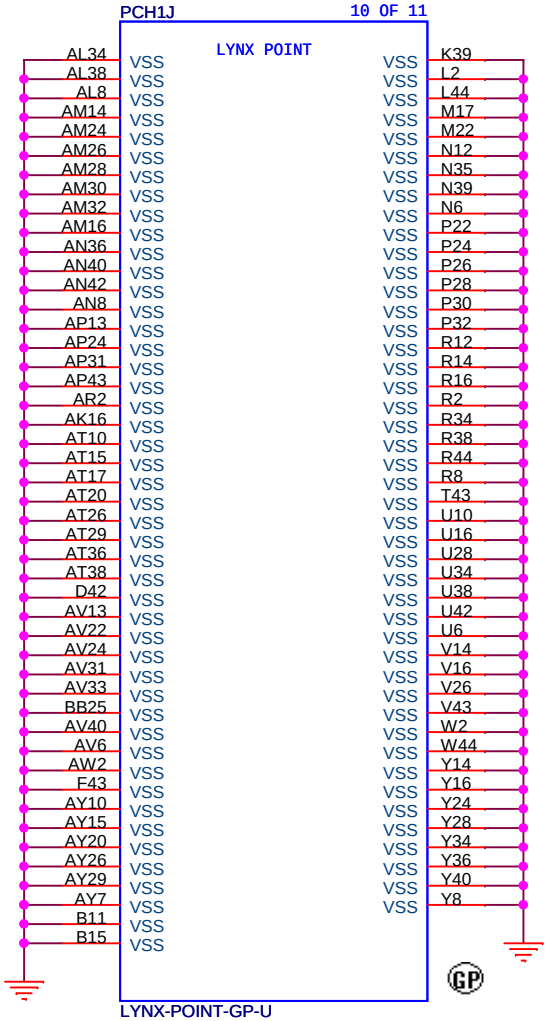
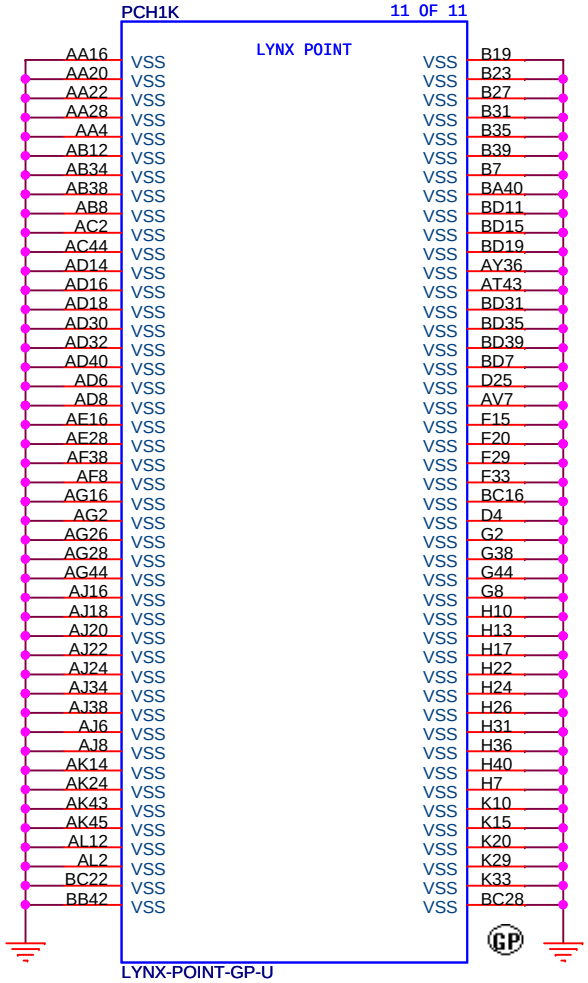
Title: CPU (RSVD)

Size: Custom | Document Number: Hades_HBS 860M | Rev: SB

Date: Wednesday, May 28, 2014 | Sheet 22 of 102

SSID = PCH





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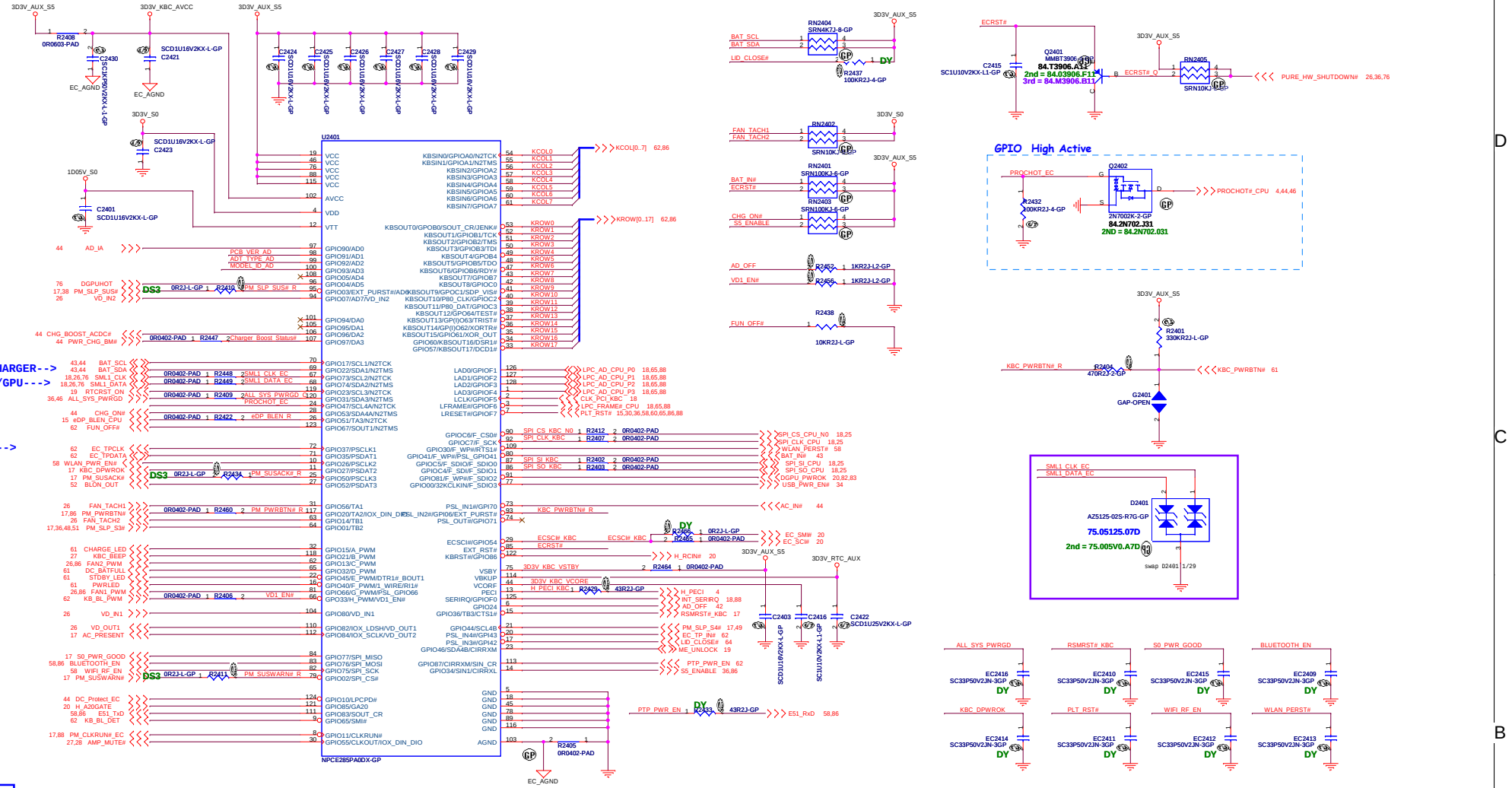
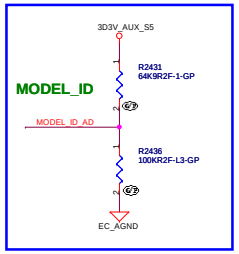
Title: *CPU (VSS)*

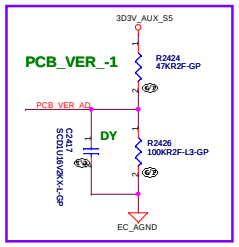
Size	Document Number	Rev
A4	Hades_HBS 860M	SB

Date: Friday, April 11, 2014 Sheet 23 of 102

SSID = KBC

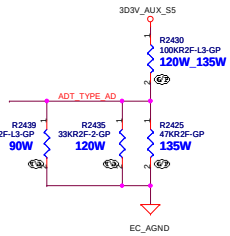






Model_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
VA30	100.0 K	10.0 K	3.000 V	3.0054	>= 2.875 V	
Hades UMA	100.0 K	20.0 K	2.750 V	2.7591	>= 2.616 V	< 2.875 V
Hades DIS 840	100.0 K	33.0 K	2.481 V	2.4935	>= 2.363 V	< 2.616 V
Hades DIS 850	100.0 K	47.0 K	2.245 V	2.2592	>= 2.123 V	< 2.363 V
Hades DIS 860	100.0 K	64.9 K	2.001 V	2.0169	>= 1.934 V	< 2.123 V
Poseidon DIS 840	100.0 K	76.8 K	1.867 V	1.8827	>= 1.758 V	< 1.934 V
Poseidon DIS 860	100.0 K	100.0 K	1.650 V	1.6665	>= 1.504 V	< 1.758 V
Poseidon DIS 850	100.0 K	143.0 K	1.358 V	1.3740	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	>= 0.524 V	< 1.126 V

PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
SA	100.0 K	10.0 K	3.000 V	3.0054	>= 2.875 V	
SB	100.0 K	20.0 K	2.750 V	2.7591	>= 2.616 V	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.4935	>= 2.363 V	< 2.616 V
-1	100.0 K	47.0 K	2.245 V	2.2592	>= 2.123 V	< 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169	>= 1.934 V	< 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.8827	>= 1.758 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.6665	>= 1.504 V	< 1.758 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.3740	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	>= 0.524 V	< 1.126 V



ADT_TYPE_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
65W	N/A	100.0 K	3.300 V		>= 3.000 V	
90W	100.0 K	N/A	0.000 V			< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.3055	>= 0.150 V	< 0.425 V
45W	20.0 K	100.0 K	0.550 V	0.5592	>= 0.425 V	< 0.684 V
120W	33.0 K	100.0 K	0.819 V	0.8312	>= 0.684 V	< 0.937 V
135W	47.0 K	100.0 K	1.055 V	1.0695	>= 0.937 V	< 1.177 V
150W	64.9 K	100.0 K	1.299 V	1.3146	>= 1.177 V	< 1.366 V
Reserved	76.8 K	100.0 K	1.433 V	1.4497	>= 1.366 V	< 1.542 V
Reserved	100.0 K	100.0 K	1.650 V	1.6665	>= 1.542 V	< 1.842 V

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Title: KBC_NPCE285PA0DX

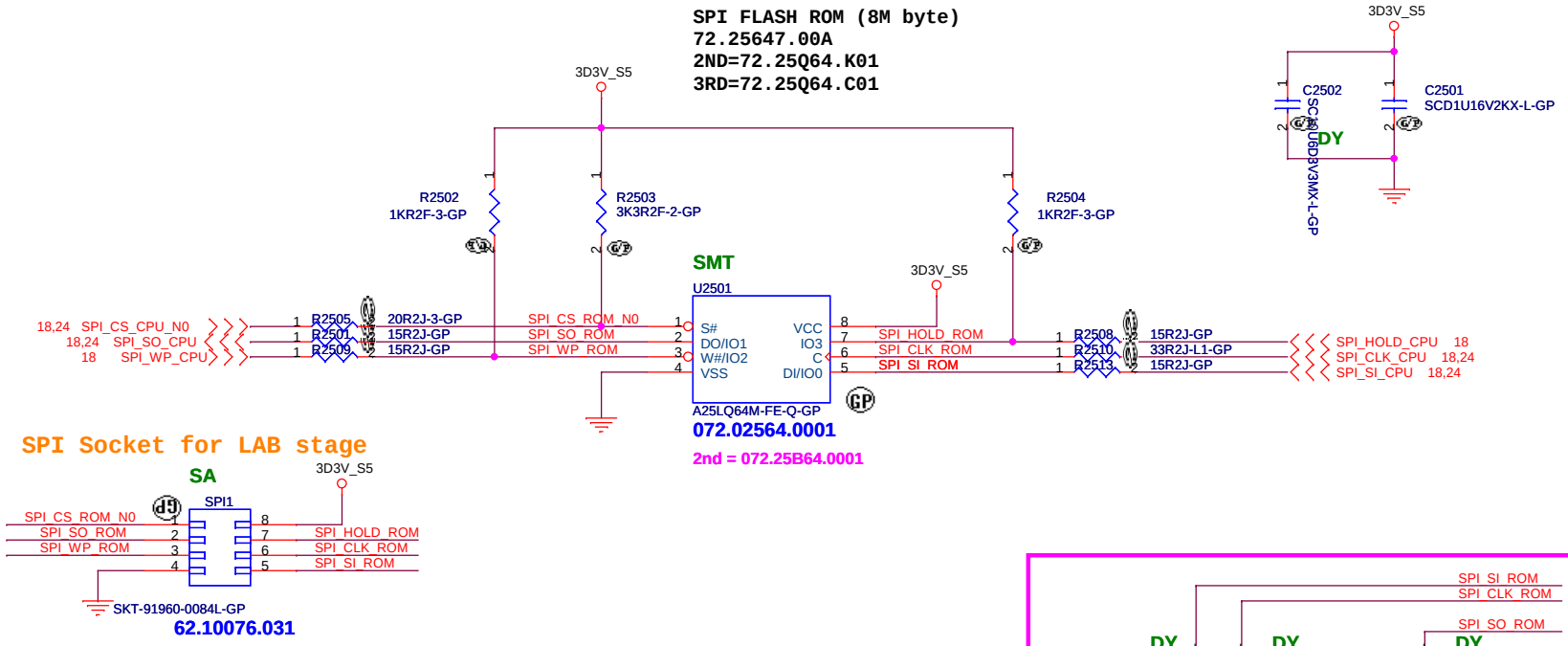
Size: A2 | Document Number: Hades_HBS 860M | Rev: SB

Date: Wednesday, May 28, 2014 | Sheet 24 of 102

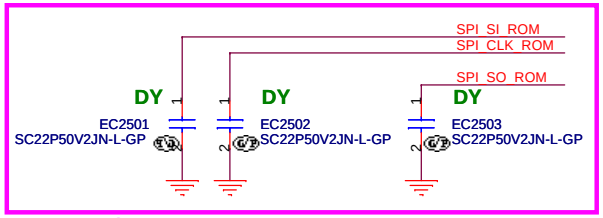
SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH

SPI ROM Equal length need to less than 500mil

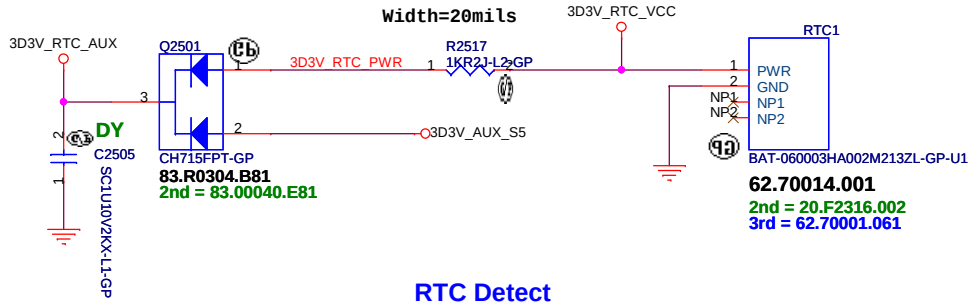


SPI Socket for LAB stage

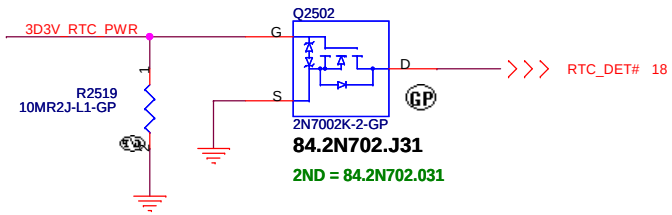


Reserve for EMC

SSID = RBAT



RTC Detect



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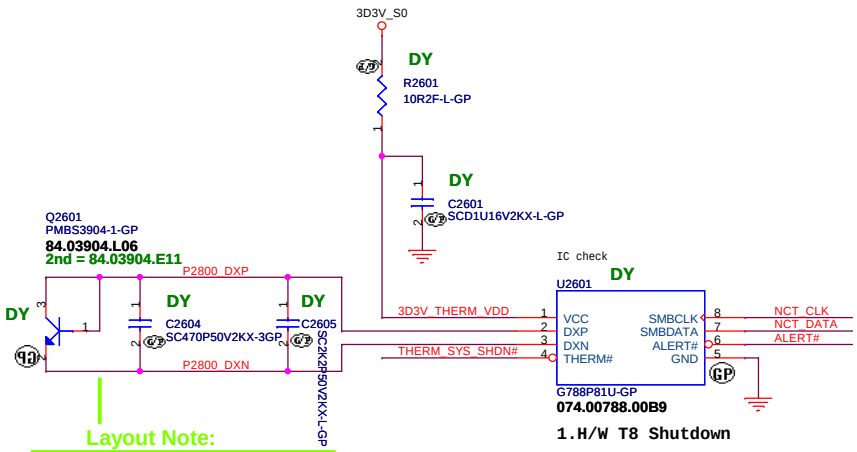
Title	Flash(KBC+PCH)/RTC	
Size Custom	Document Number Hades_HBS 860M	Rev SB
Date: Friday, April 11, 2014	Sheet 25 of 102	

SSID = Thermal

Thermal sensor GMT G788



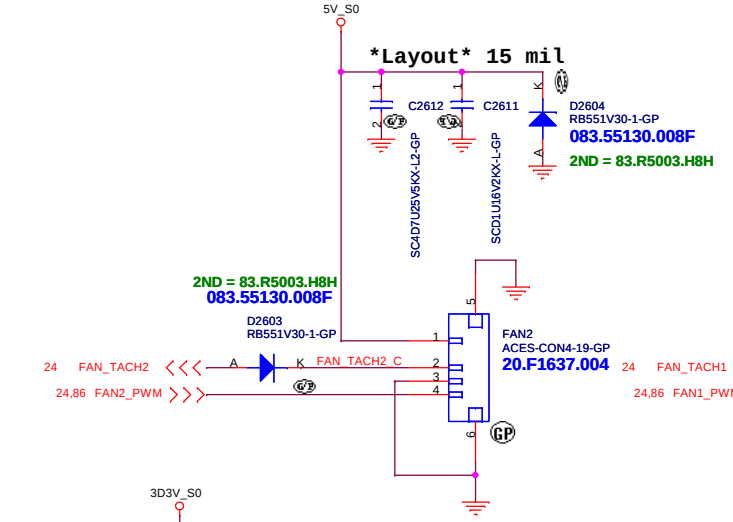
1.H/W T8 Shutdown

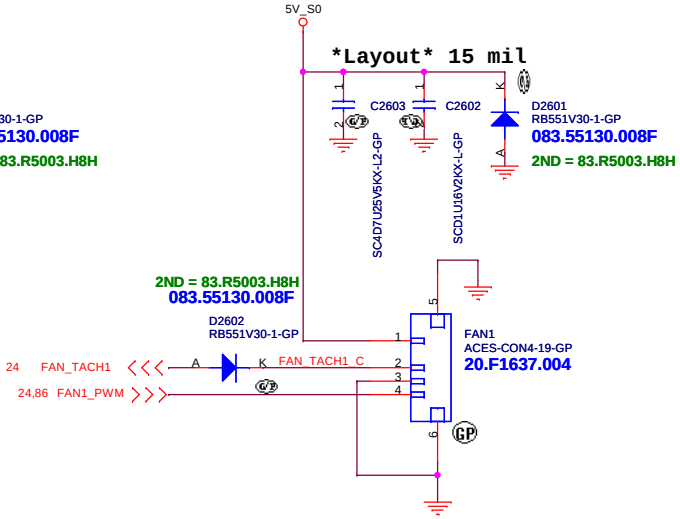
T8=85 degree

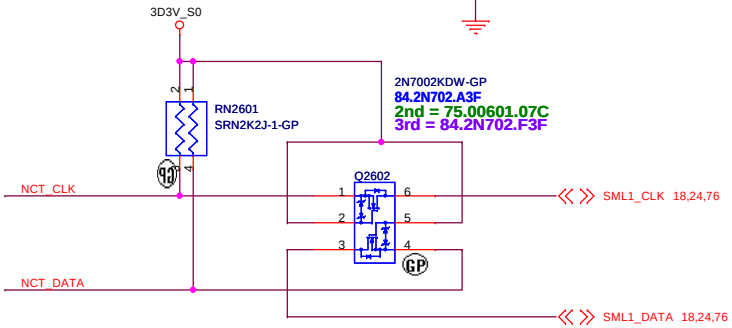
Layout Note:

Layout notice :
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

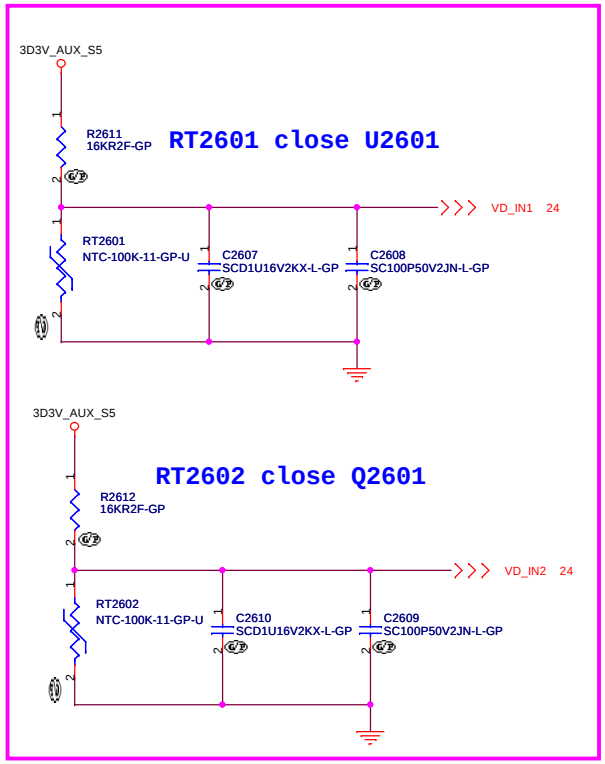
2.System Sensor, Put on palm rest

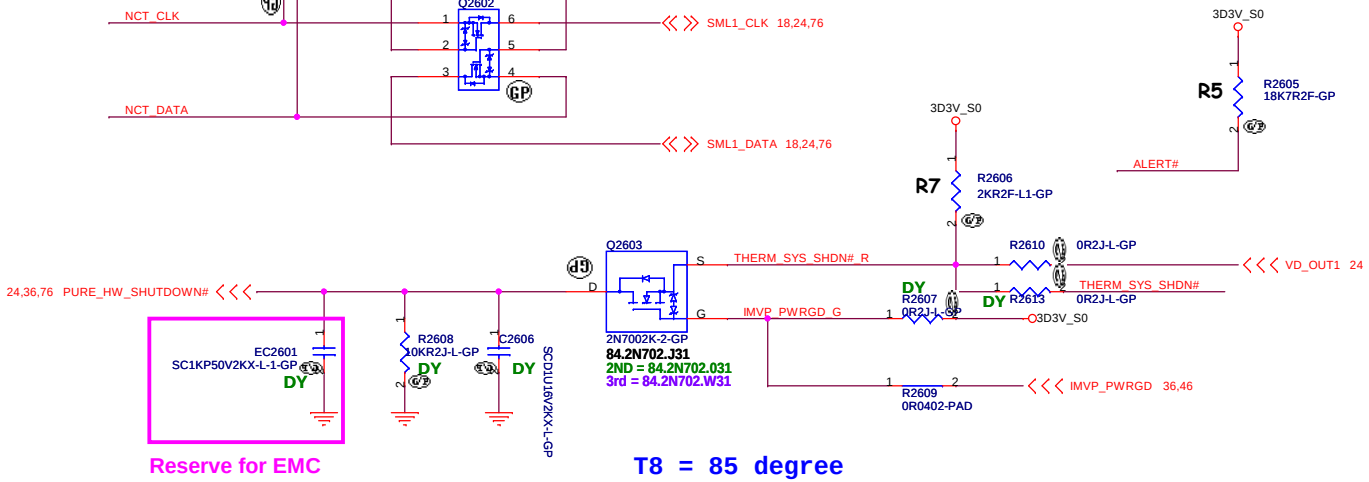






FAN_TACH1_C
FAN_TACH2_C
FAN_TACH1_C 86
FAN_TACH2_C 86





Reserve for EMC

T8 = 85 degree

ALERT# /T_CRIT# Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point

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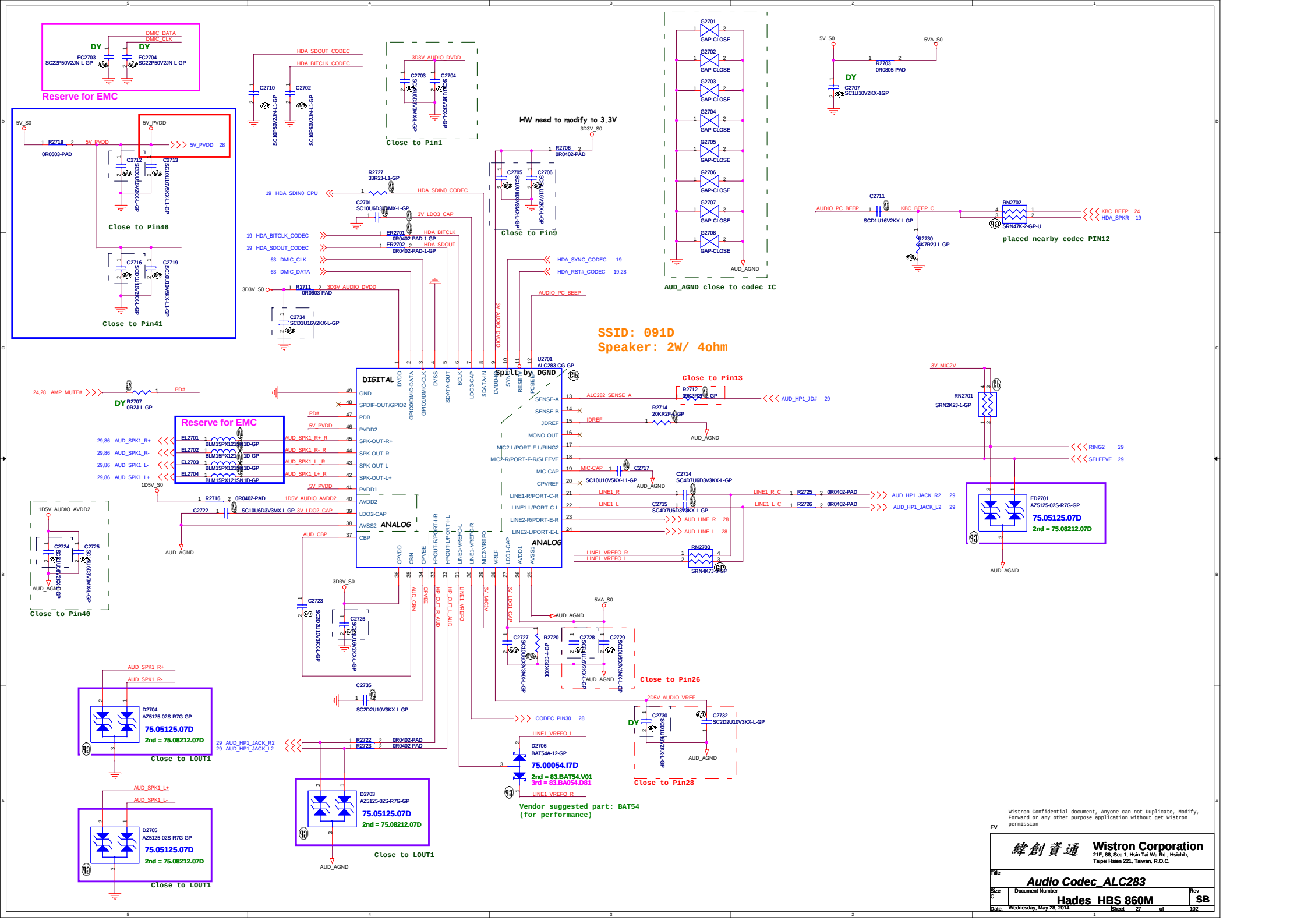
Title: *Thermal 7718/Fan Controllor P2793*

Size: A3 | Document Number: Hades HBS 860M | Rev: SB

Date: Wednesday, May 28, 2014 | Sheet 26 of 102



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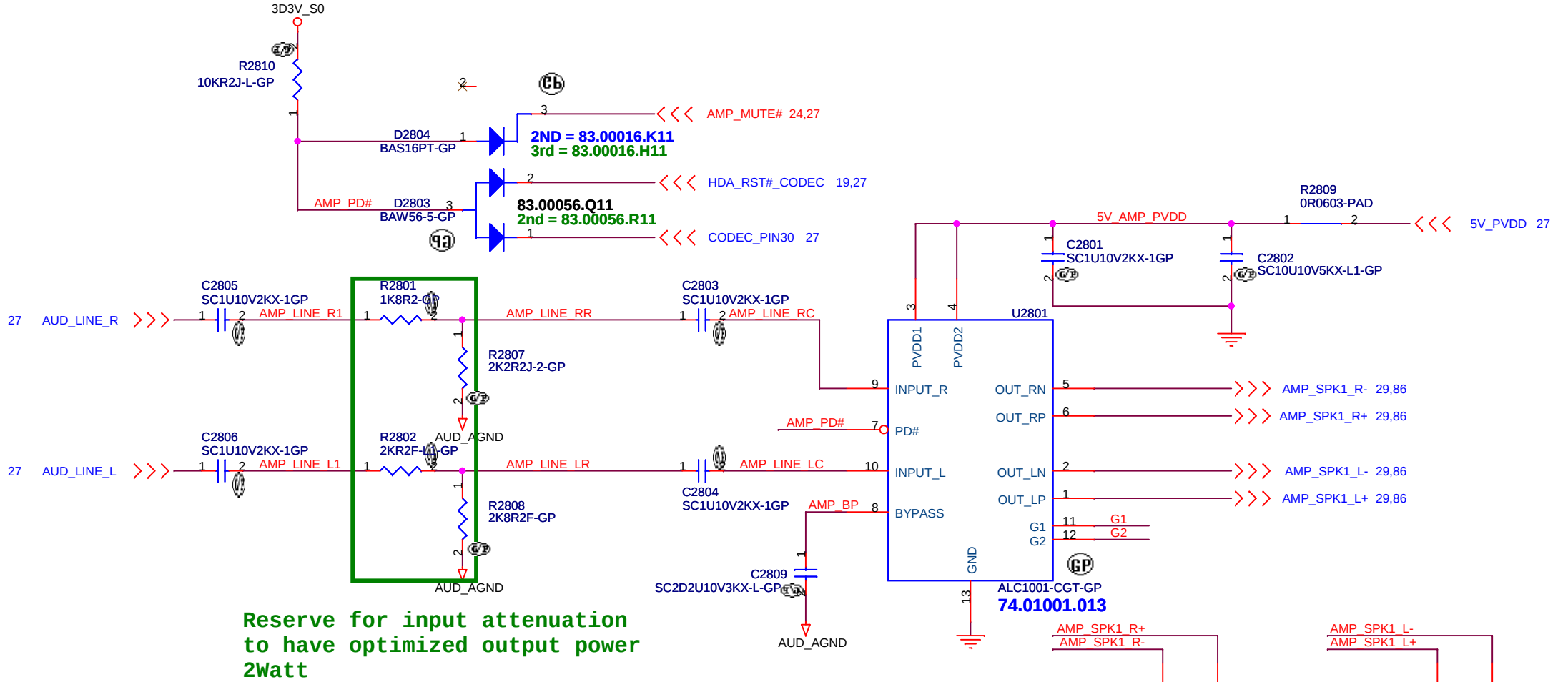
Title: ***Audio Codec_ALC283***

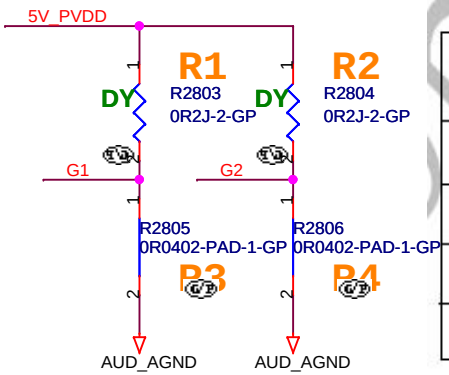
Size: C | Document Number: **Hades_HBS 860M** | Rev: **SB**

Date: Wednesday, May 28, 2014 | Sheet 27 of 102



Reserve for input attenuation
to have optimized output power
2Watt

2W 4ohm



Output Gain Table

R1	R2	R3	R4	Gain(Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB

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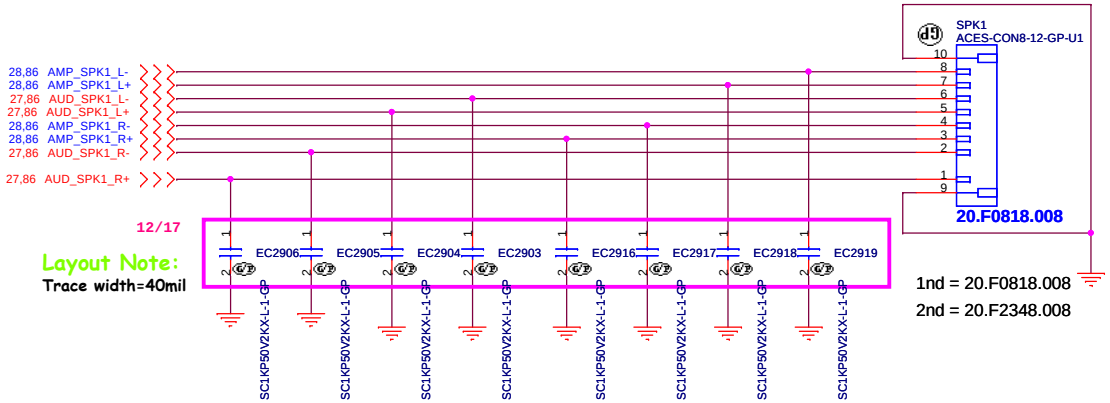
Title: **Audio AMP_ALC1001**

Size: A4 | Document Number: **Hades_HBS 860M** | Rev: **SB**

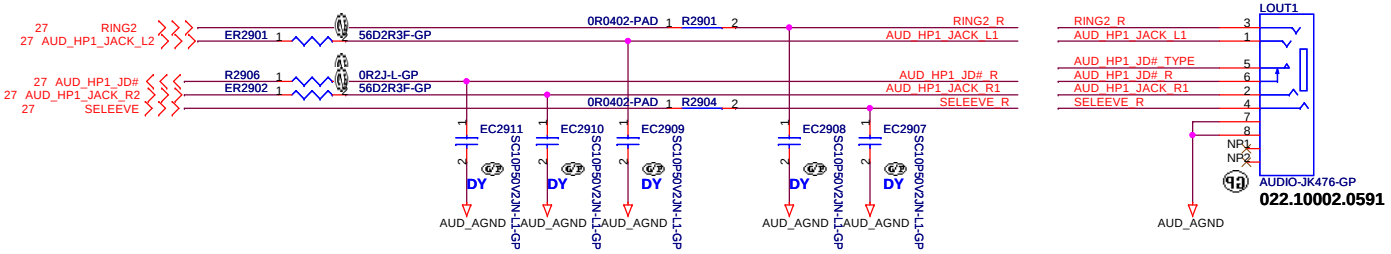
Date: Wednesday, May 28, 2014 | Sheet 28 of 102

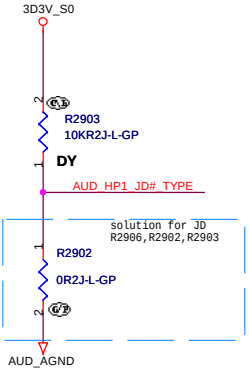
SSID = AUDIO

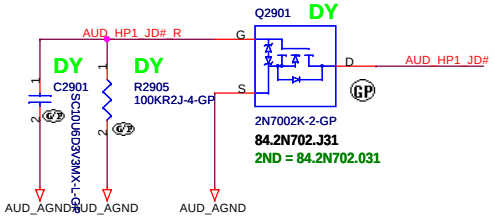
Speaker



Combo Jack







86 SELEEVE_R
86 AUD_HP1_JACK_L1
86 AUD_HP1_JD#_TYPE
86 AUD_HP1_JD#_R
86 AUD_HP1_JACK_R1
86 RING2_R

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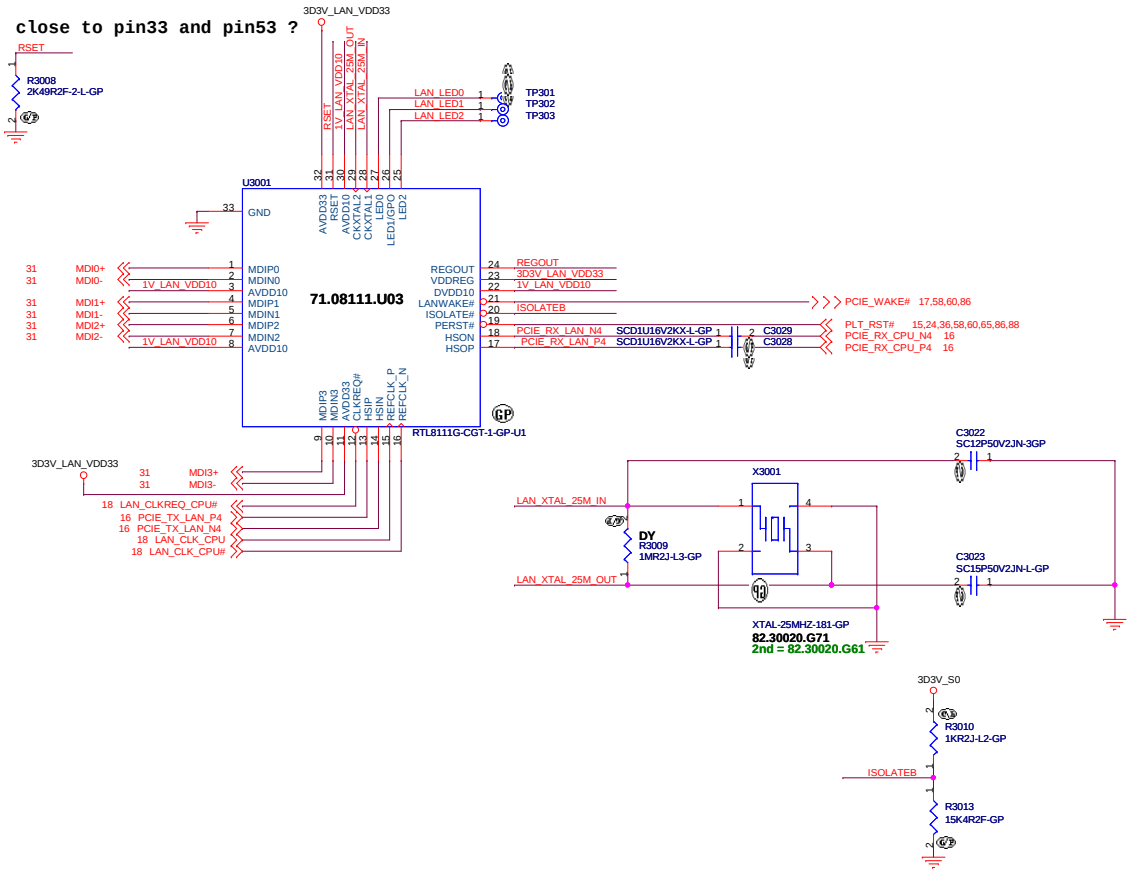
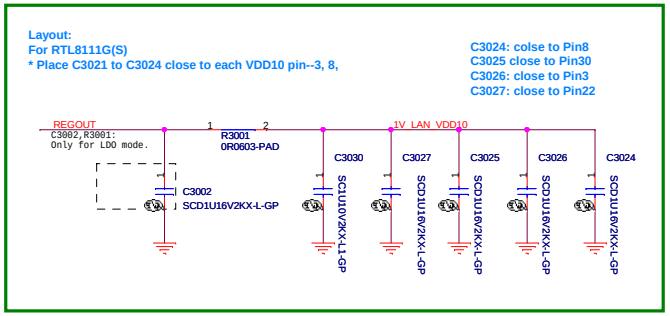
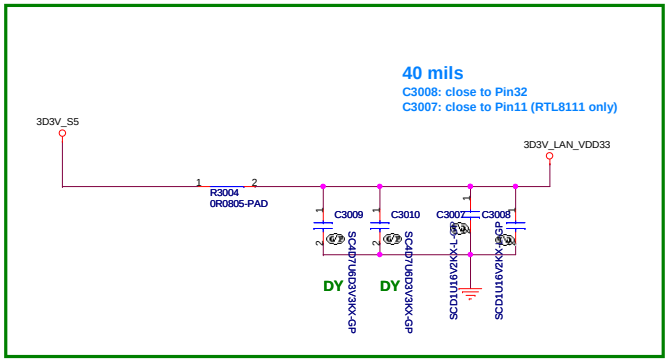
Title: Audio Jack

Size: Custom | Document Number: Hades HBS 860M | Rev: SB

Date: Wednesday, May 28, 2014 | Sheet 29 of 102







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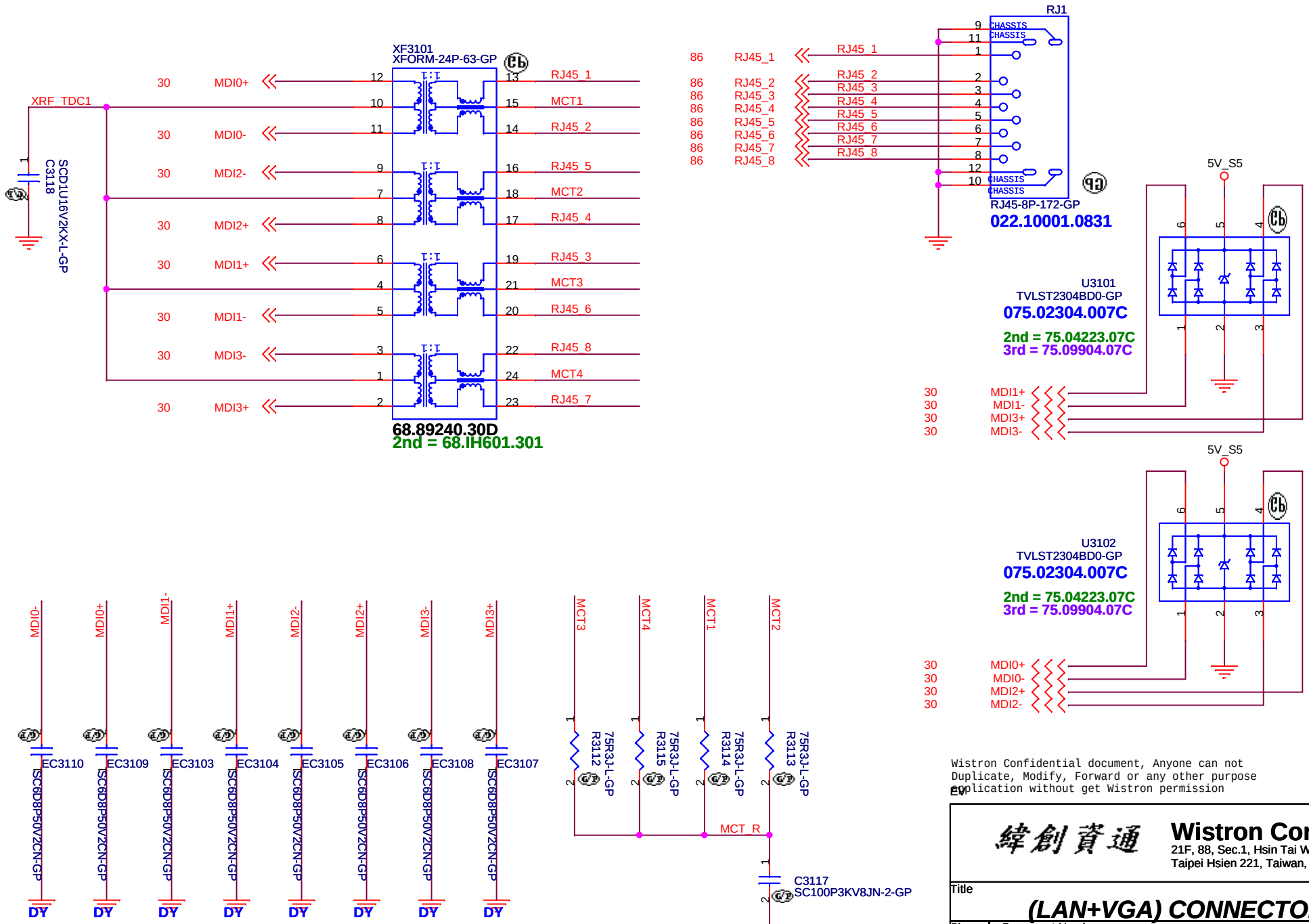
Title: ***LAN (RTL8111G(S))***

Size	Document Number	Rev
Custom	Hades_HBS 860M	SB

Date: Wednesday, May 28, 2014 Sheet 30 of 102

SSID = LAN



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Title: (LAN+VGA) CONNECTOR

Size: A4 | Document Number: Hades_HBS 860M | Rev: SB

Date: Wednesday, May 28, 2014 | Sheet 31 of 102

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Title

RTS5170(CARD READER)

Size	Document Number	Rev
A4	**Hades_HBS 860M**	**SB**

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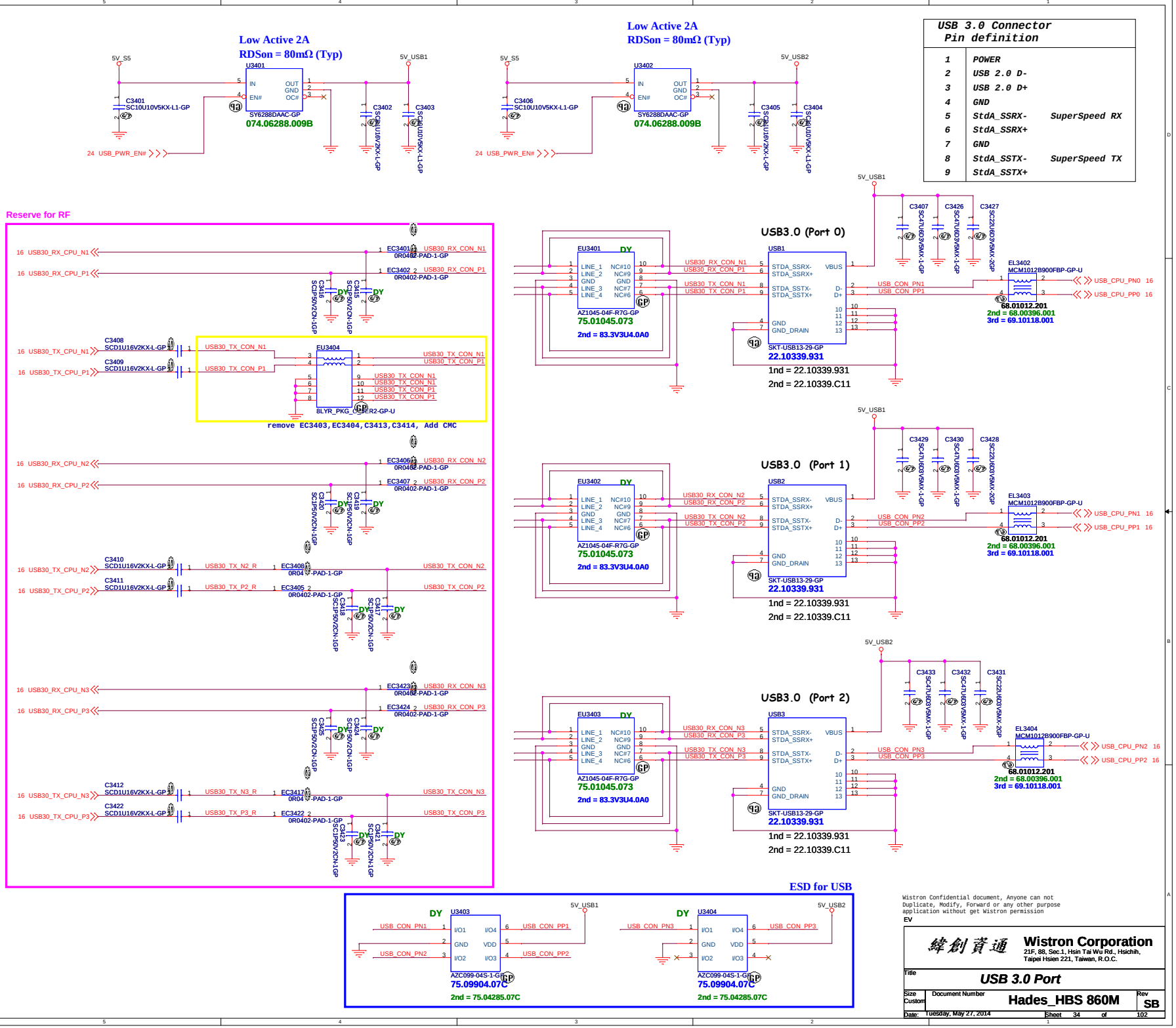
Title

Card Reader CONN (Reserved)

Size	Document Number	Rev
Custom	**Hades_HBS 860M**	**SB**

Date: Friday, April 11, 2014 Sheet 33 of 102



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Title: USB 3.0 Port

Size: Custom | Document Number: Hades_HBS 860M | Rev: SB

Date: Tuesday, May 27, 2014 | Sheet 34 of 102

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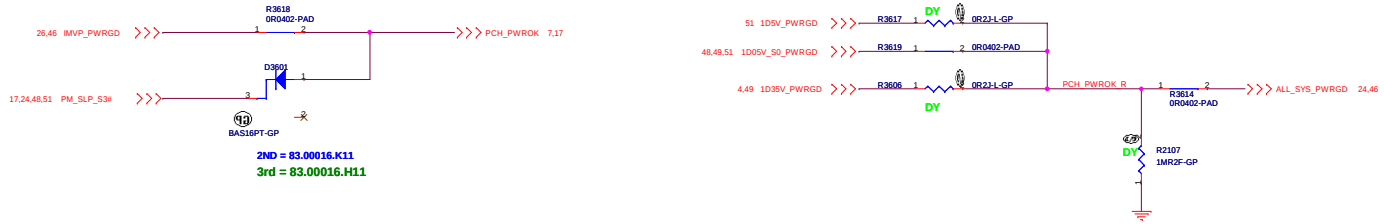
Title

USB CHARGER

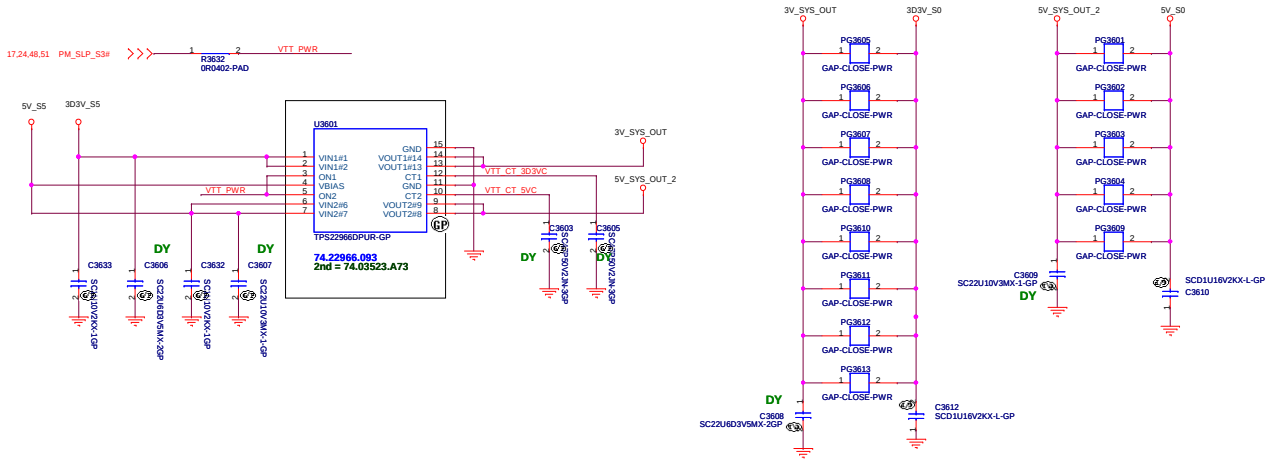
Size	Document Number	Rev
A4	**Hades HBS 860M**	**SB**

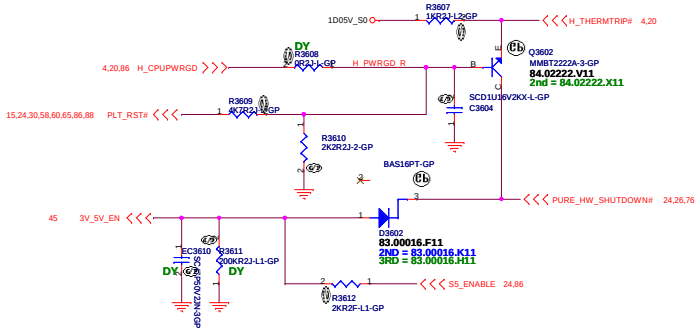
Date: Friday, April 11, 2014 Sheet 35 of 102

Power Sequence

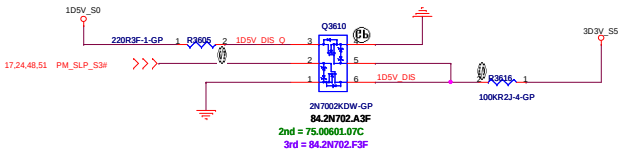


ANNIE Run Power





Discharge Circuit



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Title: Power Plane Enable & SEQUENCE

Size: A2 | Document Number: Hades_HBS 860M | Rev: SB

Date: Wednesday, May 28, 2014 | Sheet 36 of 102

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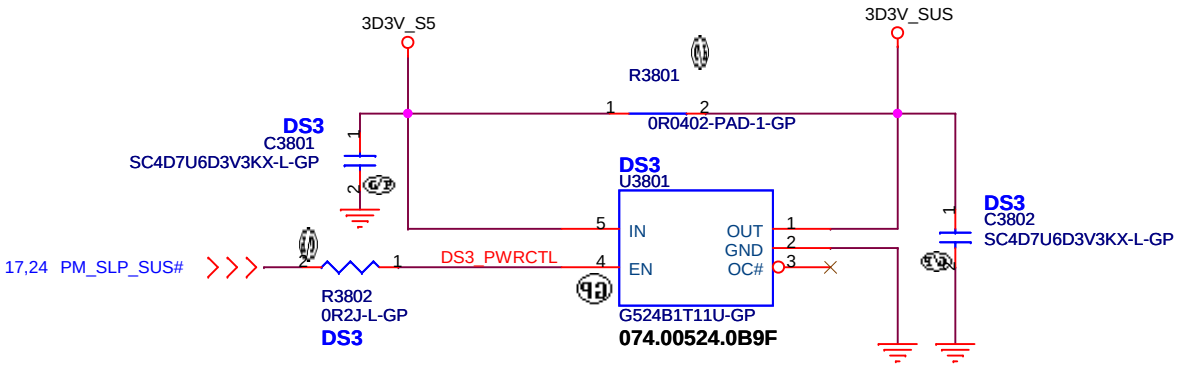
Title

ADAPTER OCP / S3 reduction

Size	Document Number	Rev
Custom	**Hades_HBS 860M**	**SB**

Date: Friday, April 11, 2014 Sheet 37 of 102



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Title: DS3

Size: A4 | Document Number: Hades HBS 860M | Rev: SB

Date: Thursday, May 22, 2014 | Sheet 38 of 102

Power Sequence

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Title: *1D05_M*

Size	Document Number	Rev
Custom	Hades_HBS 860M	SB

Date: Friday, April 11, 2014 Sheet 39 of 102

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Title

Connected Standby1

Size	Document Number	Rev
A	**Hades_HBS 860M**	**SB**

Date: Friday, April 11, 2014 Sheet 40 of 102

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Title

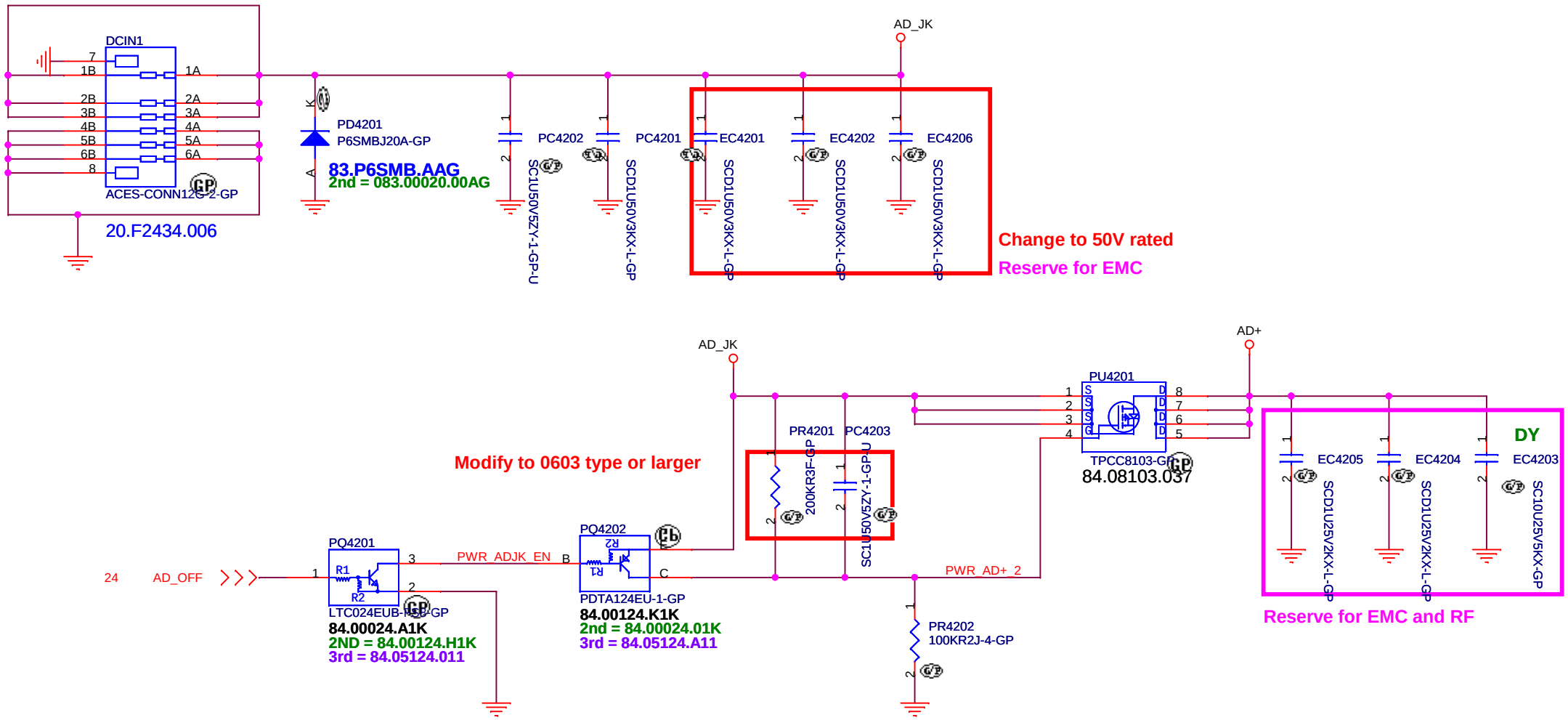
Connected Standby2

Size	Document Number	Rev
A	**Hades_HBS 860M**	**SB**

Date: Friday, April 11, 2014 Sheet 41 of 102

ANNIE solution

Adaptor in to generate DCBATOUT



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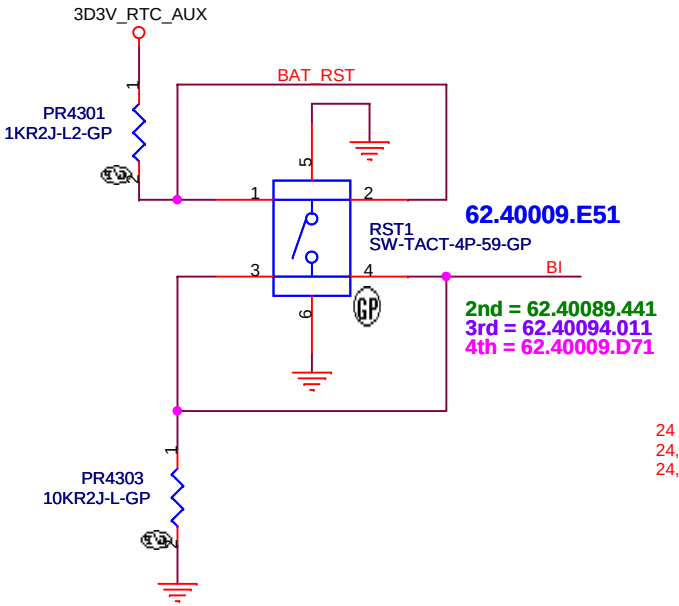
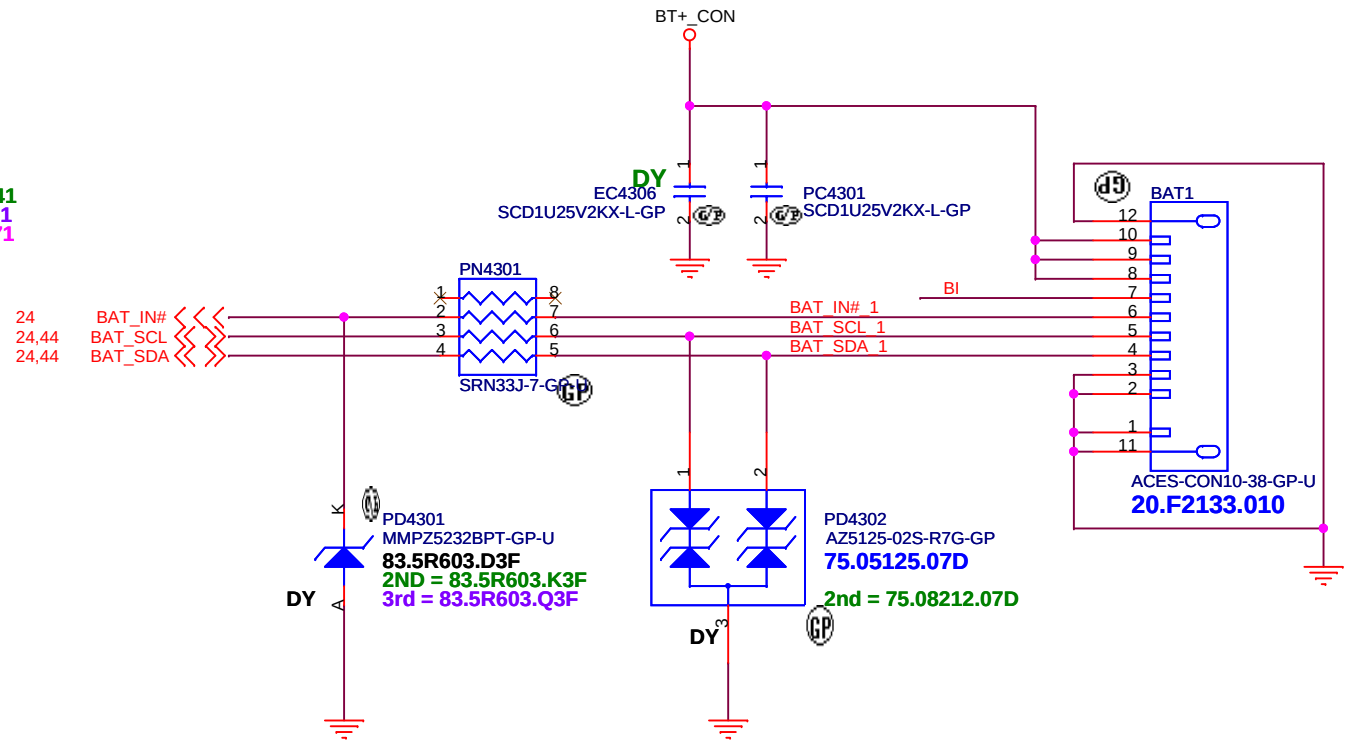
Title	DCIN JACK	
Size A4	Document Number Hades HBS 860M	Rev SB
Date: Thursday, May 15, 2014	Sheet 42 of 102	

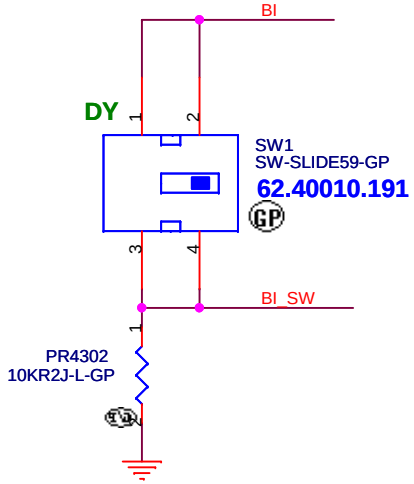
Battery Reset



Battery Connector



Battery Insert



86 BI
86 BAT_IN#_1
86 BAT_SCL_1
86 BAT_SDA_1

BI
BAT_IN# 1
BAT_SCL 1
BAT_SDA 1

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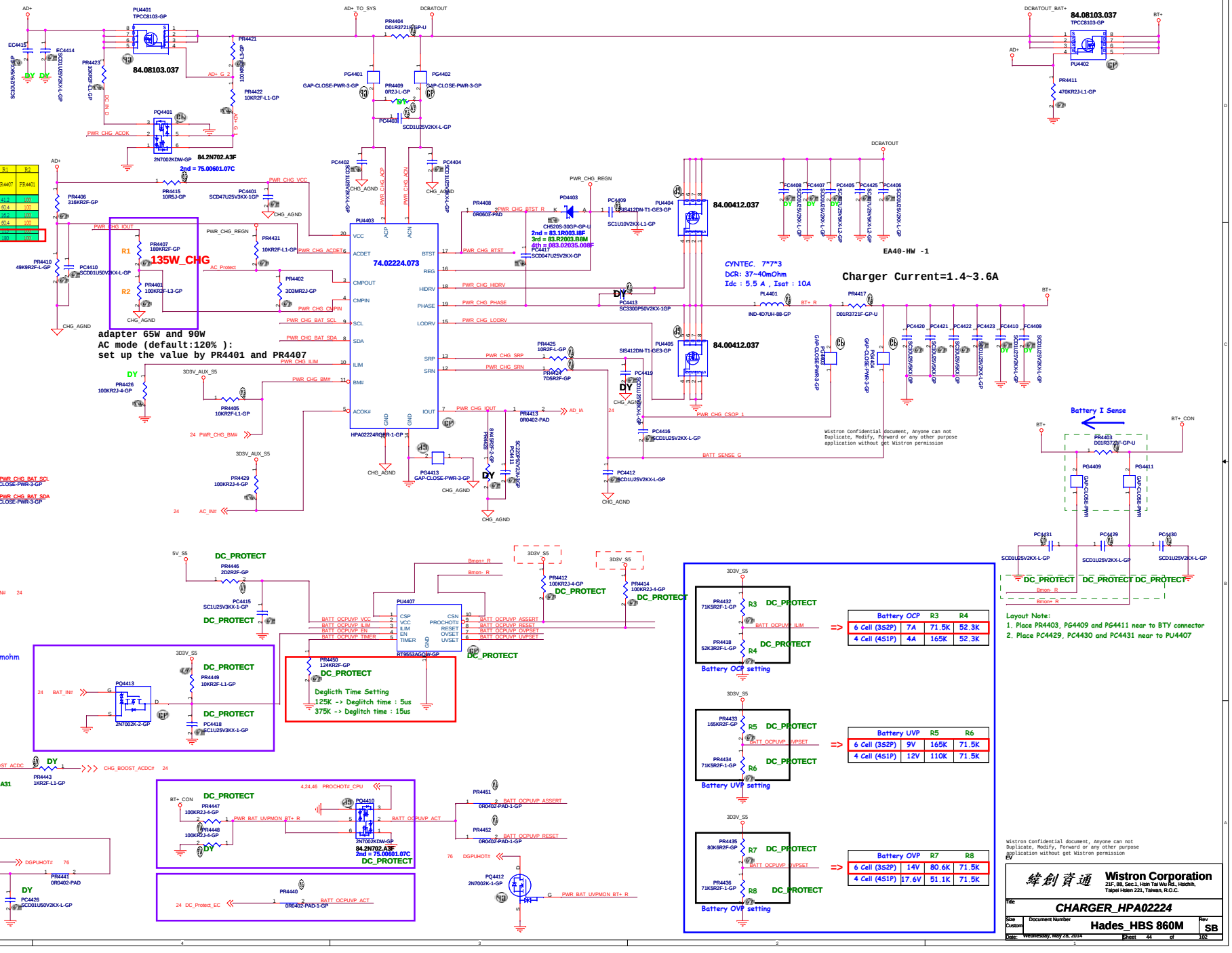
Title: BATT CONN

Size	Document Number	Rev
A4	Hades_HBS 860M	SB

Date: Friday, April 11, 2014 Sheet 43 of 102

SSID = Charger

	Stat	PM_SLP_A#	Adapter Current	AC_Protect present (85% x 120%)	AC_Protect Current	FR4404 Sense resistor	Current to Voltage	R1 PR4407	R2 PR4401
40W	AC + Battery	High	2.1	102%	2.142	20 mOhm	0.8568	41.2	100
45W	AC + Battery	High	2.37	102%	2.4174	20 mOhm	0.96696	60.4	100
65W	AC + Battery	High	3.42	102%	3.4884	10 mOhm	0.67768	124	100
90W	AC + Battery	High	4.74	102%	4.8348	10 mOhm	0.96696	60.4	100
120W	AC + Battery	High	6.32	102%	6.4464	10 mOhm	1.28928	41.2	100
135W	AC + Battery	High	7.1	102%	7.242	10 mOhm	1.4484	180	100



Battery OCP	R3	R4
6 Cell (3S2P)	7A	71.5K	52.3K
4 Cell (4S1P)	4A	165K	52.3K

Battery UVP	R5	R6
6 Cell (3S2P)	9V	165K	71.5K
4 Cell (4S1P)	12V	110K	71.5K

Battery OVP	R7	R8
6 Cell (3S2P)	14V	80.6K	71.5K
4 Cell (4S1P)	17.6V	51.1K	71.5K

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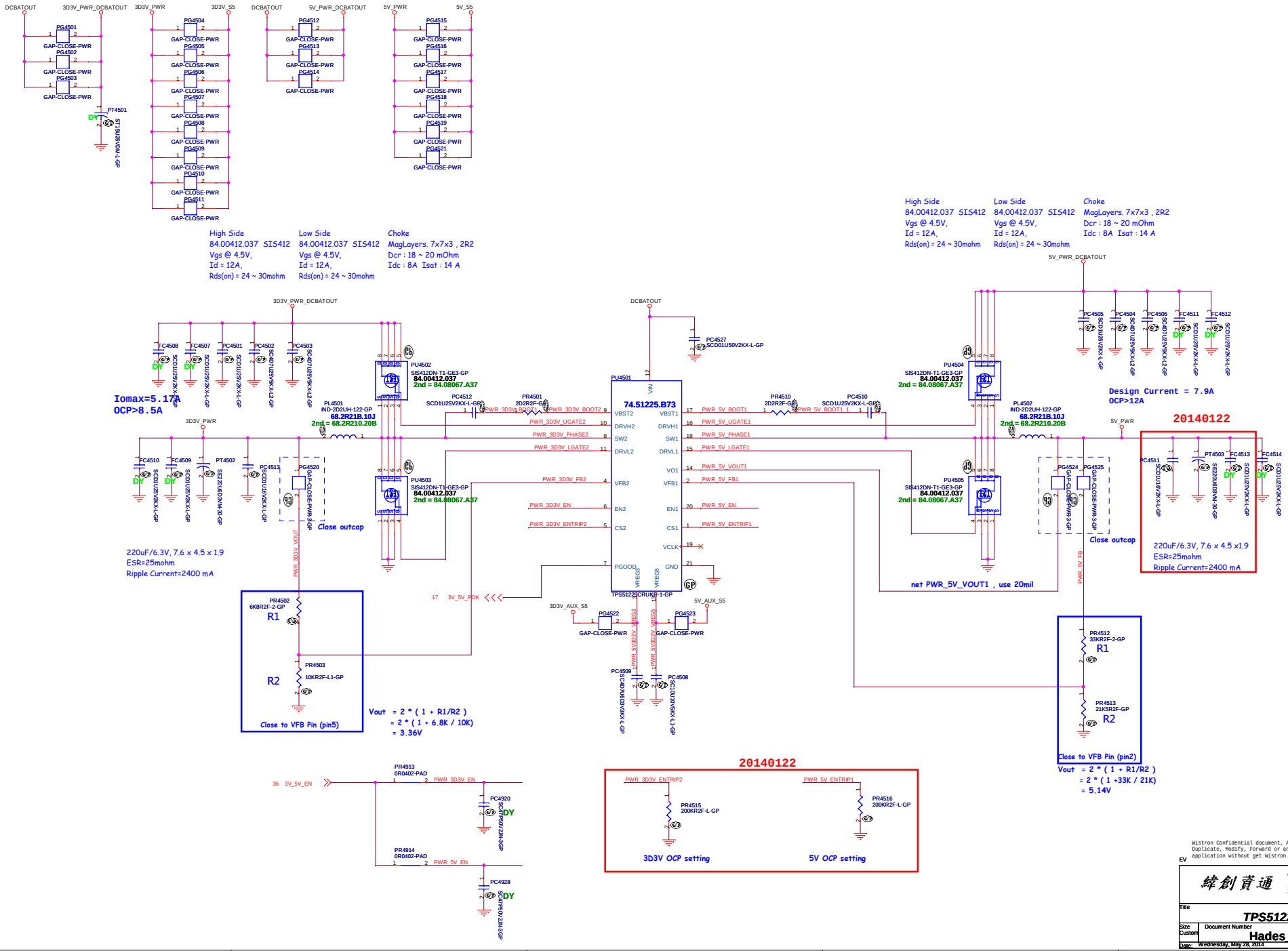
Title: CHARGER_HPA02224

Size: Custom | Document Number: Hades_HBS 860M | Rev: SB

Date: Wednesday, May 28, 2014 | Sheet 44 of 102

SSID = PWR.Plane.Regulator_3p3v5v



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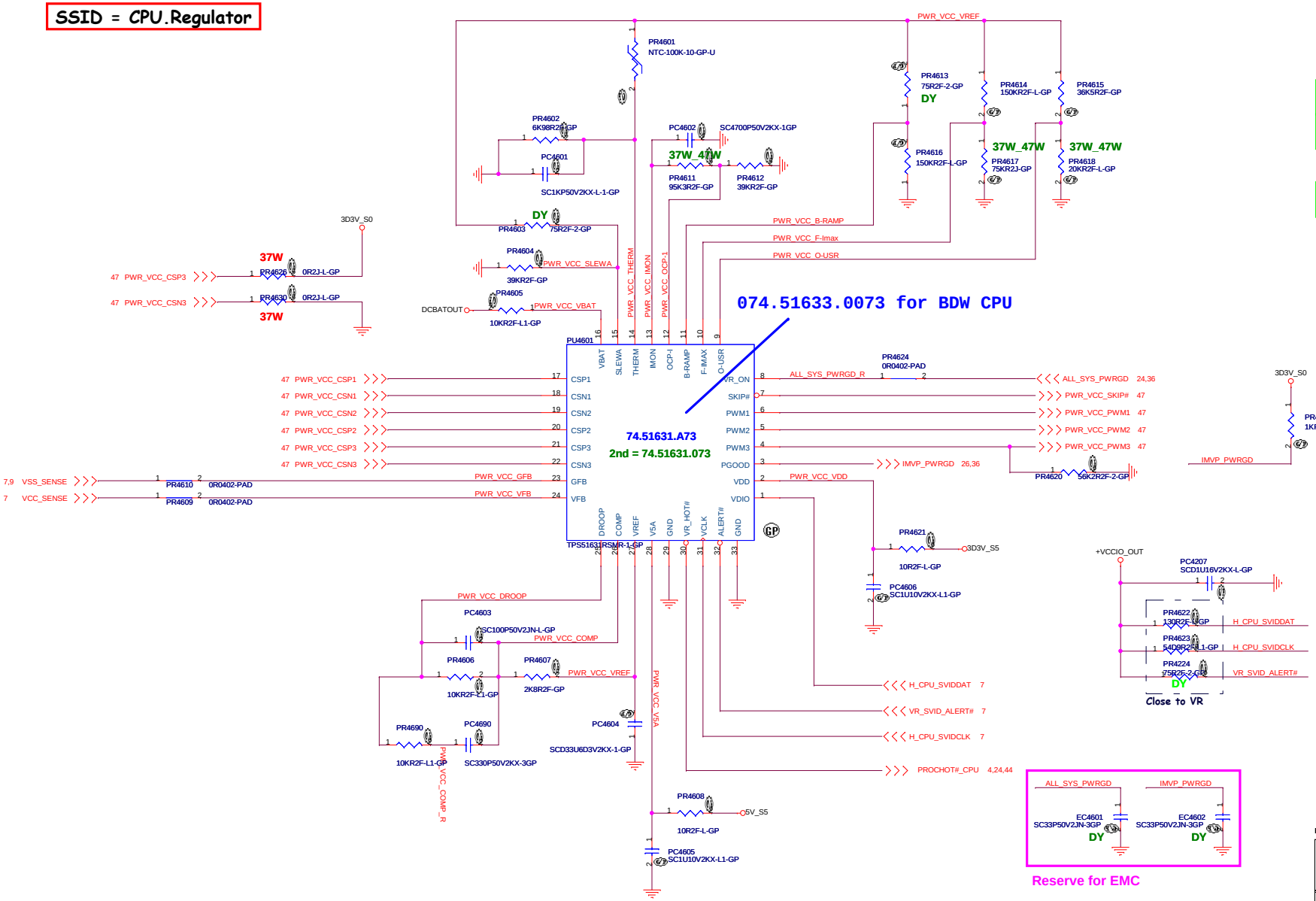
Title: TPS51225_5V/3D3V

Size: Custom | Document Number: Hades_HBS 860M | Rev: SB

Date: Wednesday, May 28, 2014 | Sheet 45 of 102

SSID = CPU.Regulator



	47W	37W
PC4602	4.7nF 78.47224.2FL	4.7nF 78.47224.2FL
PR4611	95.3k 64.95325.6DL	165k 64.16535.6DL
PR4614	150k 64.15035.6DL	274k 64.27435.6DL
PR4617	75k 63.75334.1DL	75k 63.75334.1DL
PR4615	36.5k 64.36525.6DL	64.9k 64.64925.6DL
PR4618	20k 64.20025.6DL	20k 64.20025.6DL
PR4626	DY	0R 63.R0034.L0L
PR4630	DY	0R 63.R0034.L0L
PR4602	6.98k 64.69815.6DL	6.98k 64.69815.6DL

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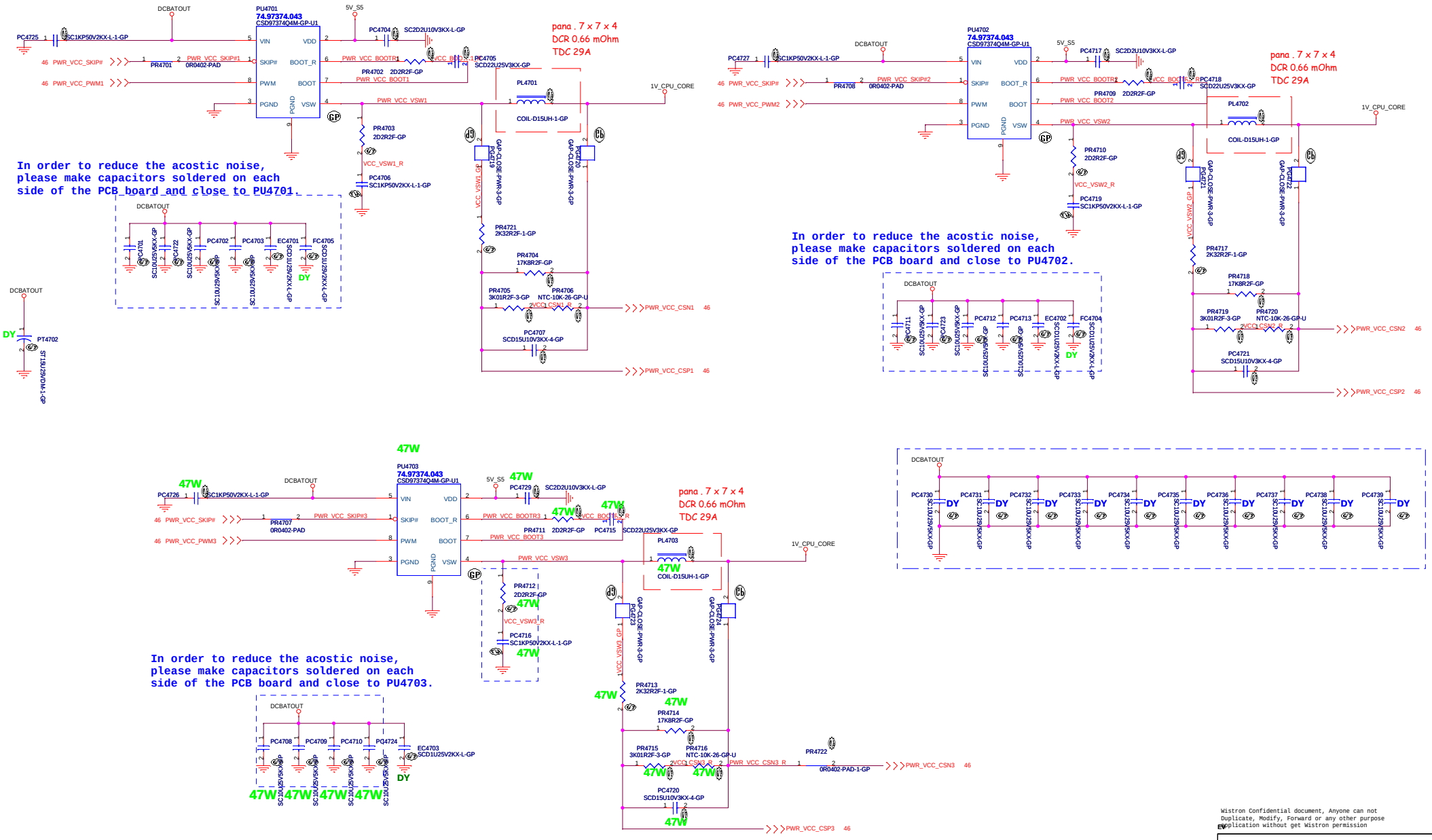
Title: TPS51624_CPUCORE(1/2)

Size: Custom | Document Number: Hades_HBS 860M | Rev: SB

Date: Thursday, May 29, 2014 | Sheet 46 of 102



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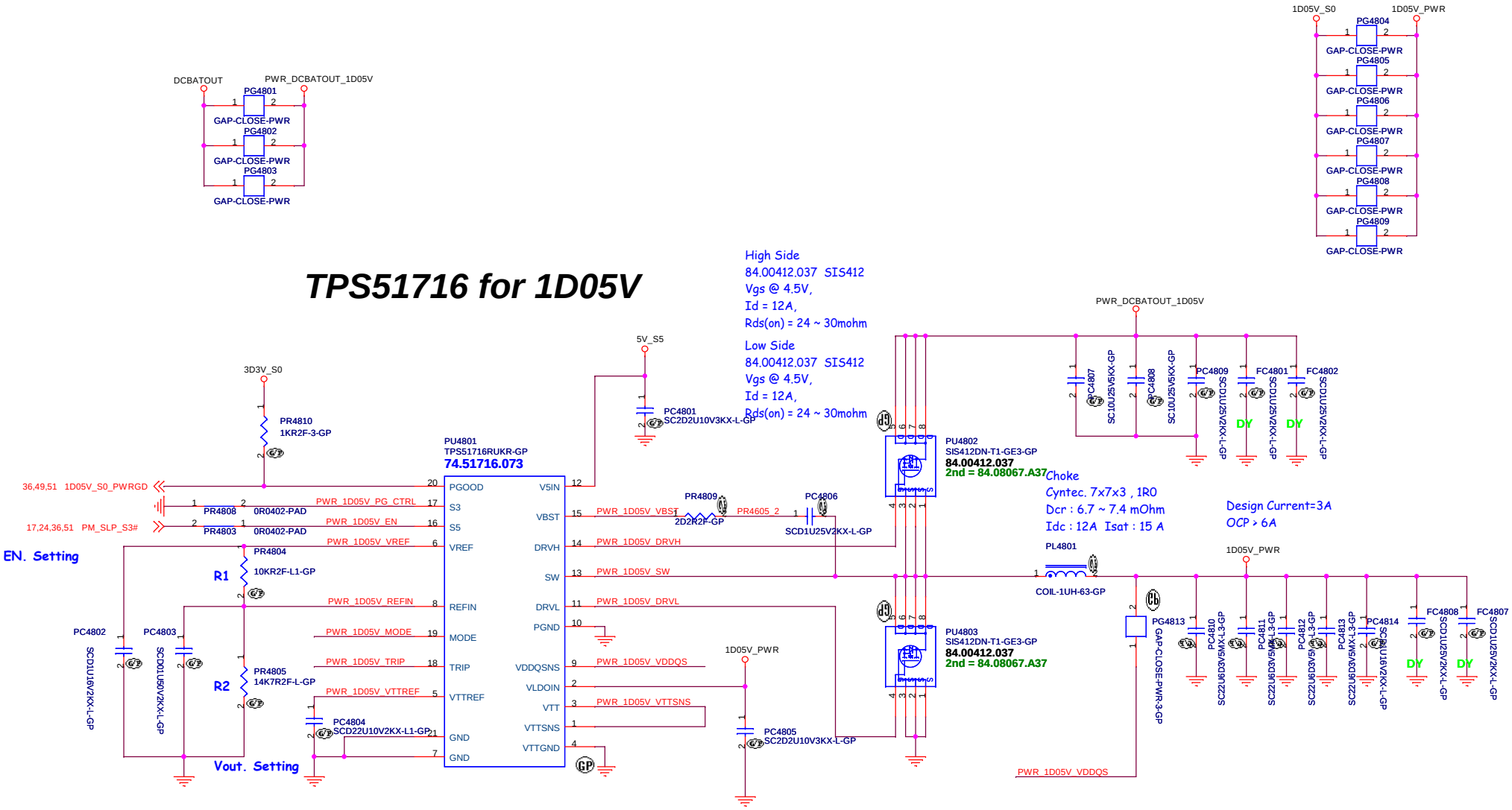
Title: CSD97374_CPUCORE(2/2)

Size: Custom | Document Number: Hades_HBS 860M | Rev: SB

Date: Wednesday, May 28, 2014 | Sheet 47 of 102



MODE

PR5006	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	
12k ohm	670kHz	Tracking Discharge
1k ohm	500kHz	

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

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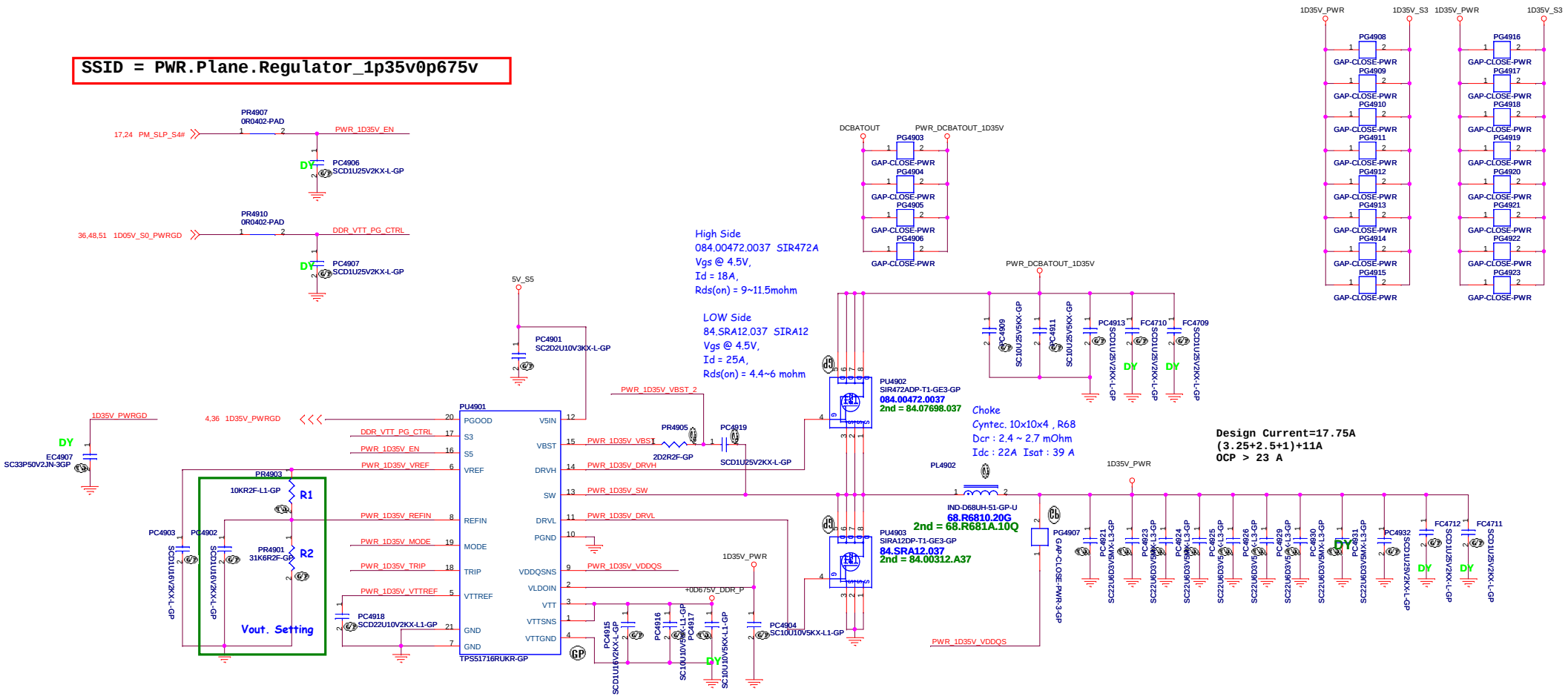
Title: DC to DC_1D05V (TPS51716)

Size: A3 | Document Number: Hades HBS 860M | Rev: SB

Date: Wednesday, May 28, 2014 | Sheet 48 of 102

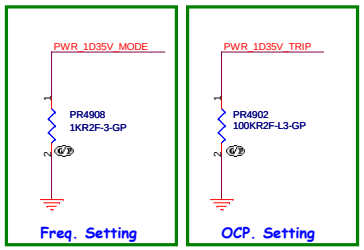
SSID = PWR.Plane.Regulator_1p35v0p675v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR4908	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	
12k ohm	670kHz	Tracking Discharge
1k ohm	500kHz	



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Title: TPS51716 (VDDQ_VTT)

Size: Custom | Document Number: Hades_HBS 860M | Rev: SB

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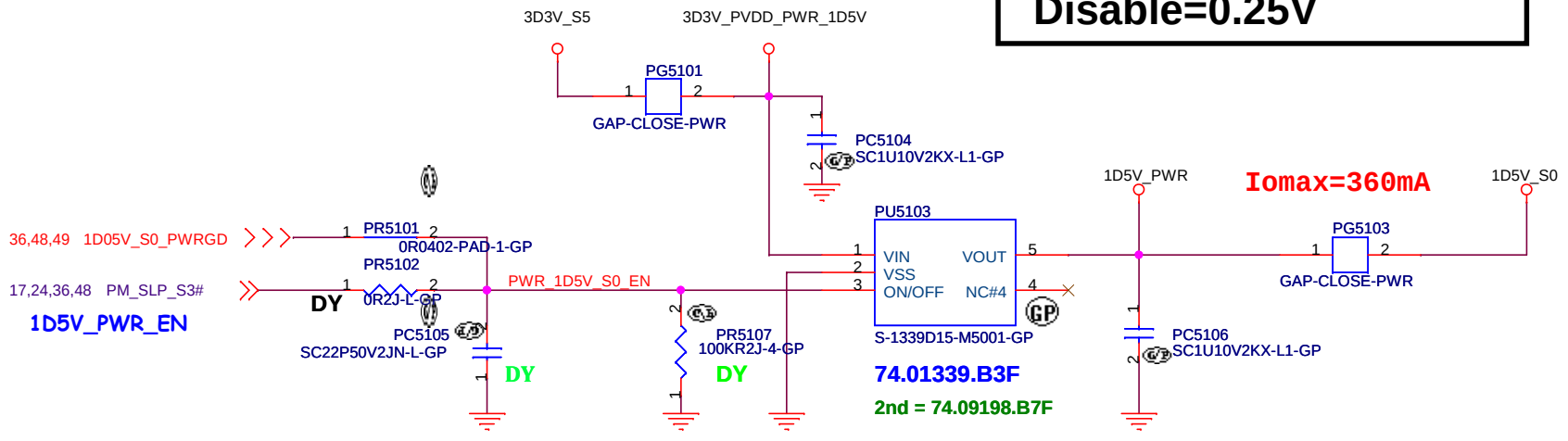
Title

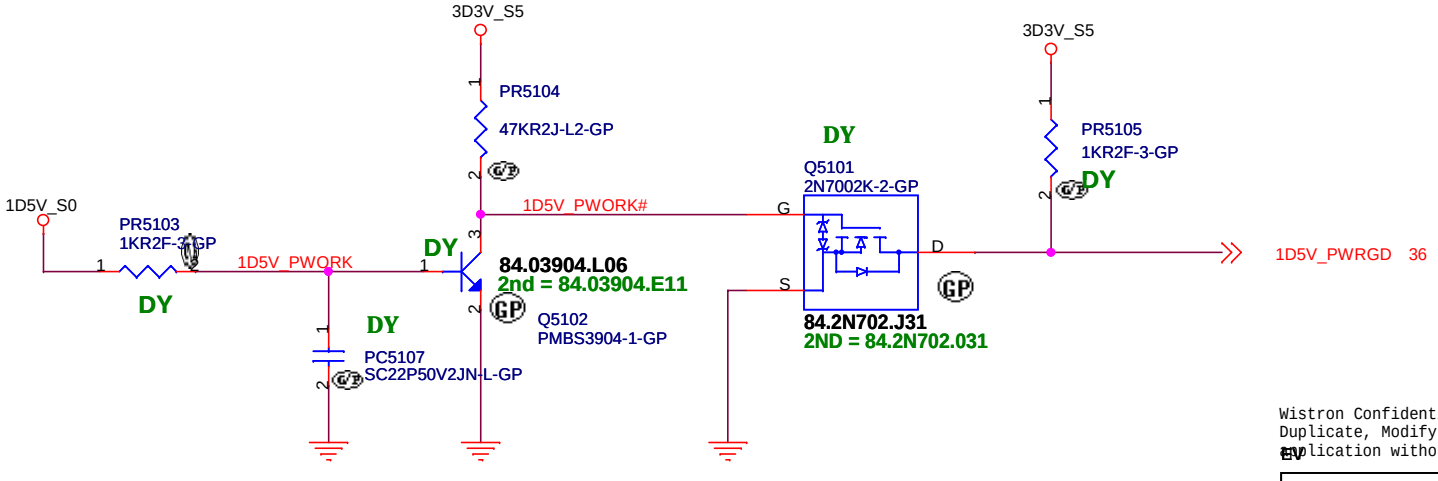
1D8V_S0 TLV62065

Size	Document Number	Rev
A4	**Hades_HBS 860M**	**SB**

Date: Friday, April 11, 2014 Sheet 50 of 102

S-1339D15 for 1D5V_S0
Enable=1.0V
Disable=0.25V





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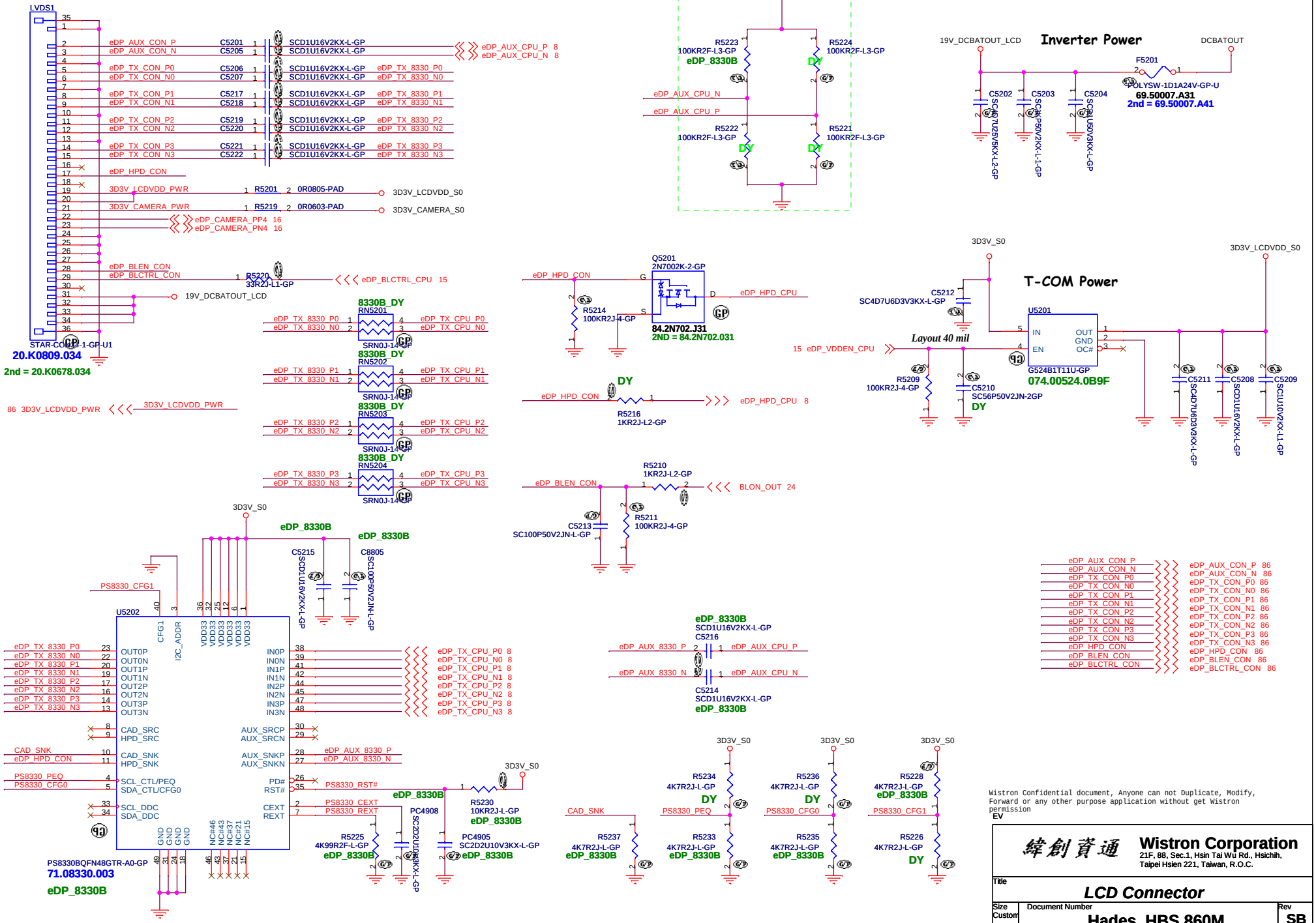
Title	***1D5V_S0 SYW232***	
Size: Custom	Document Number: **Hades_HBS 860M**	Rev: **SB**
Date: Wednesday, May 21, 2014	Sheet 51 of 102	

SSID = VIDEO



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Title: LCD Connector

Size: Custom | Document Number: Hades HBS 860M | Rev: SB

Date: Wednesday, May 28, 2014 | Sheet 52 of 102

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Title

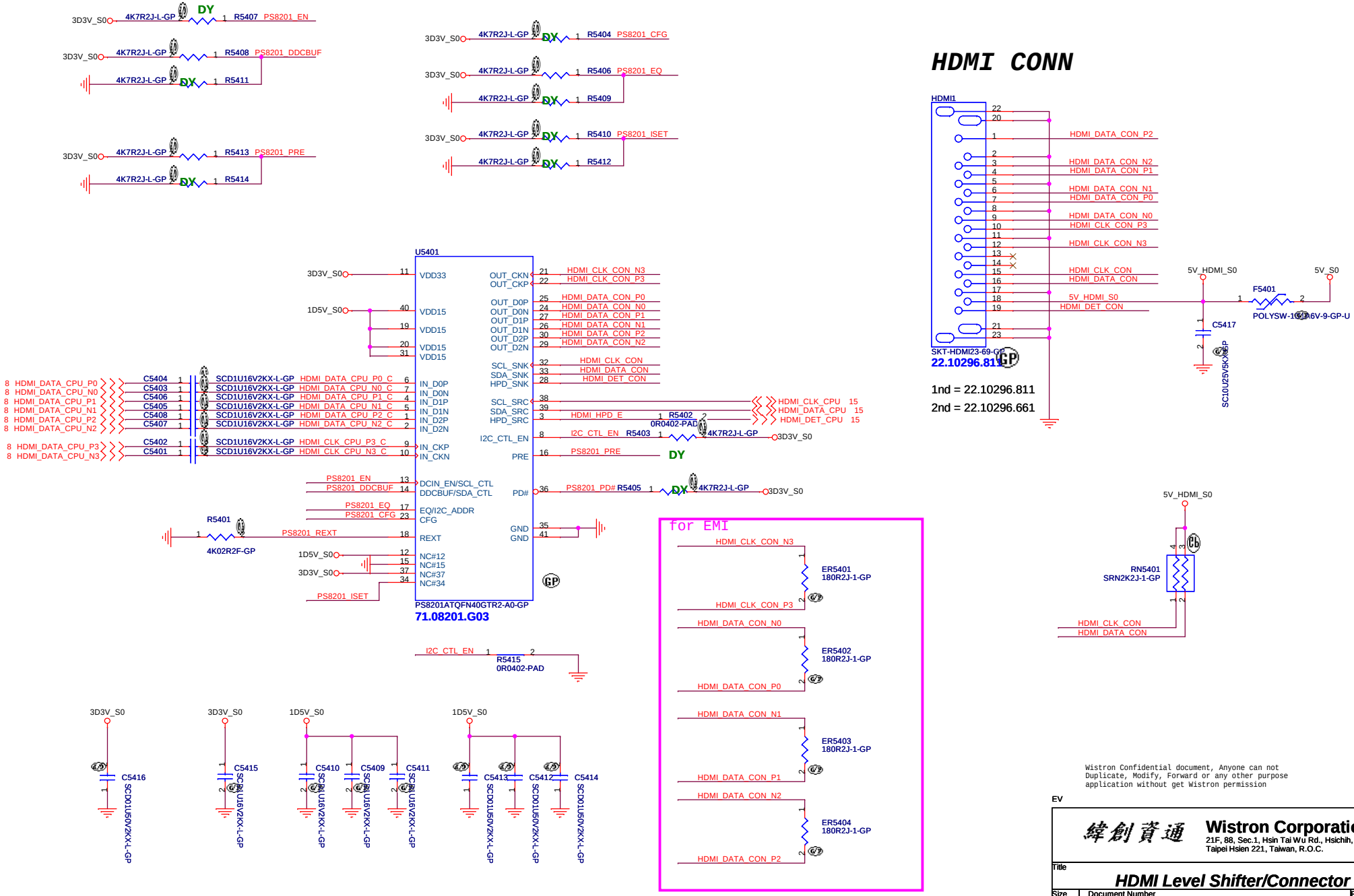
CRT Board Connector (Reserved)

Size	Document Number	Rev
A3	**Hades HBS 860M**	**SB**

Date: Friday, April 11, 2014 Sheet 53 of 102

SSID = VIDEO

HDMI Level Shifter & CONNECTOR



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Title

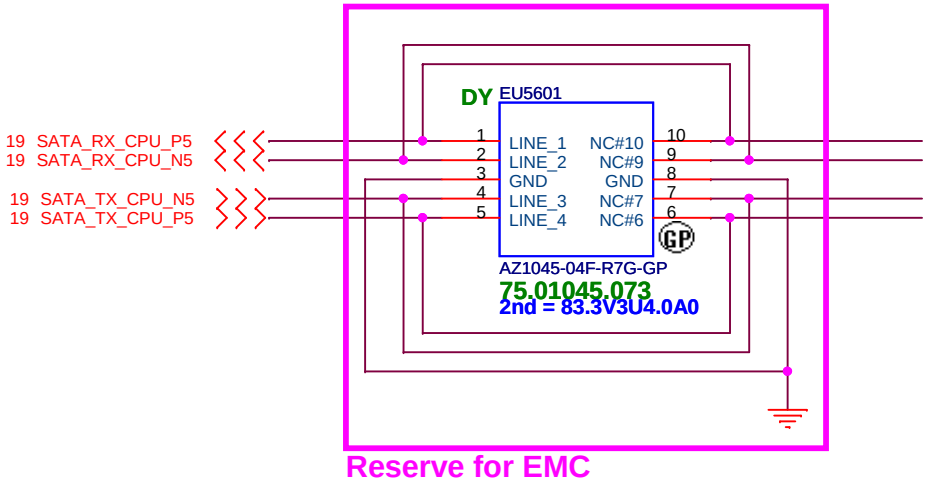
Display Port

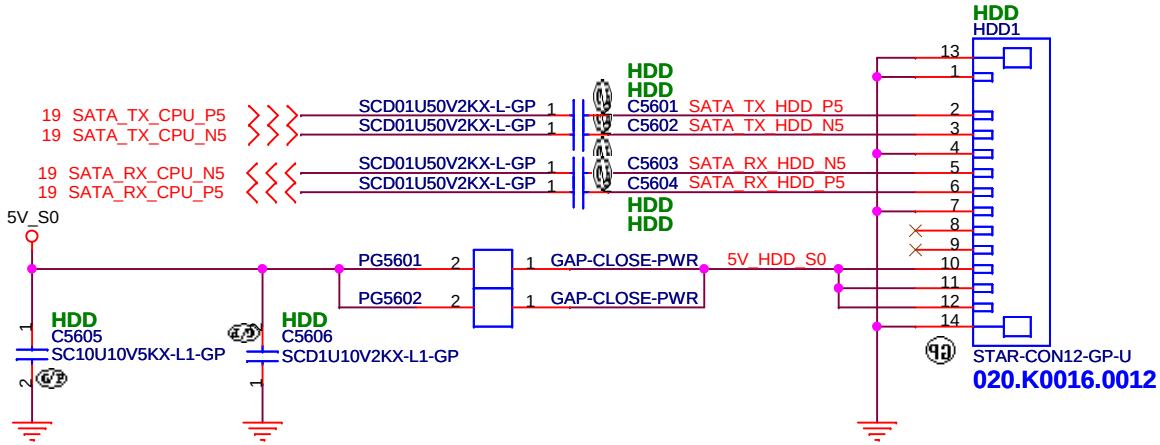
Size	Document Number	Rev
Custom	**Hades_HBS 860M**	**SB**

Date: Friday, April 11, 2014 Sheet 55 of 102

SSID = SATA

SATA HDD Connector





AC coupling caps near connector < 100 mils

SATA ODD Connector

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Title: HDD / ODD

Size: A4 | Document Number: Hades HBS 860M | Rev: SB

Date: Friday, April 11, 2014 | Sheet 56 of 102

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Title

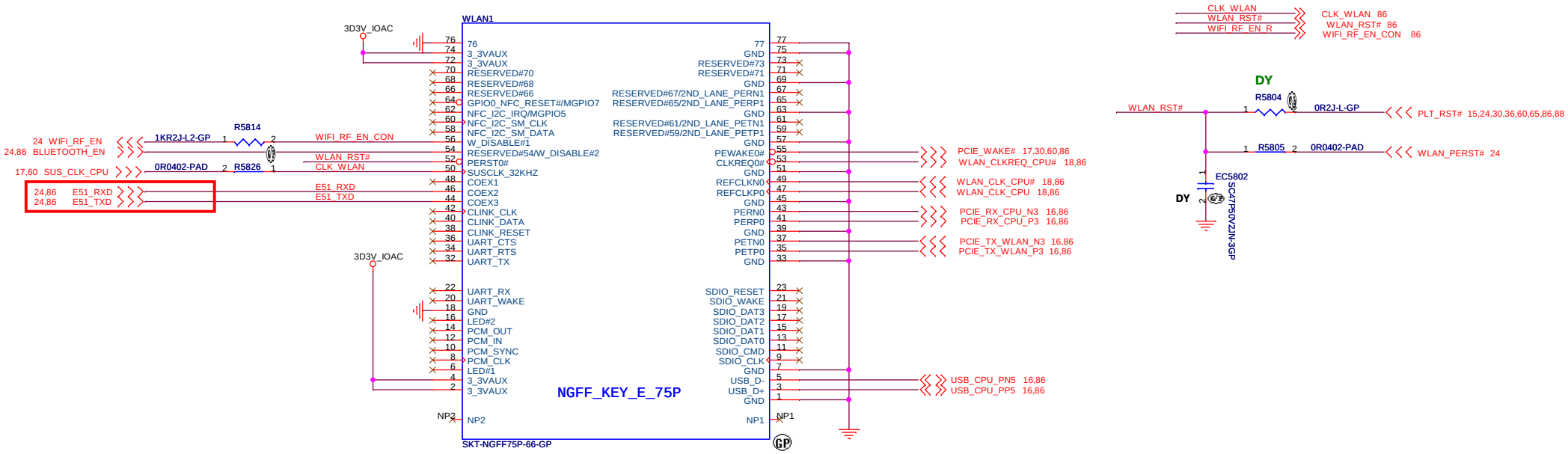
E-SATA

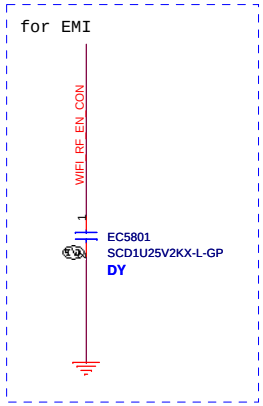
Size	Document Number	Rev
A4	**Hades HBS 860M**	**SB**

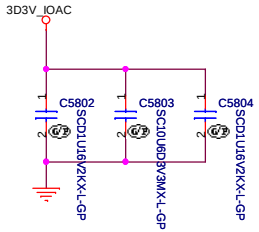
Date: Friday, April 11, 2014 Sheet 57 of 102

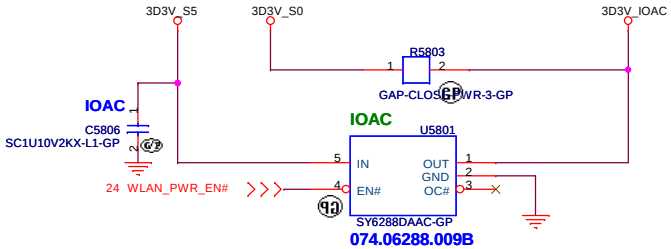
SSID = Wireless

NGFF Connector (802.11a/b/g/n)









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Title: MINICARD(WLAN)

Size: Custom | Document Number: Hades HBS 860M | Rev: SB

Date: Wednesday, May 28, 2014 | Sheet 58 of 102

SSID = Wireless

Mini Card Connector(mSATA)

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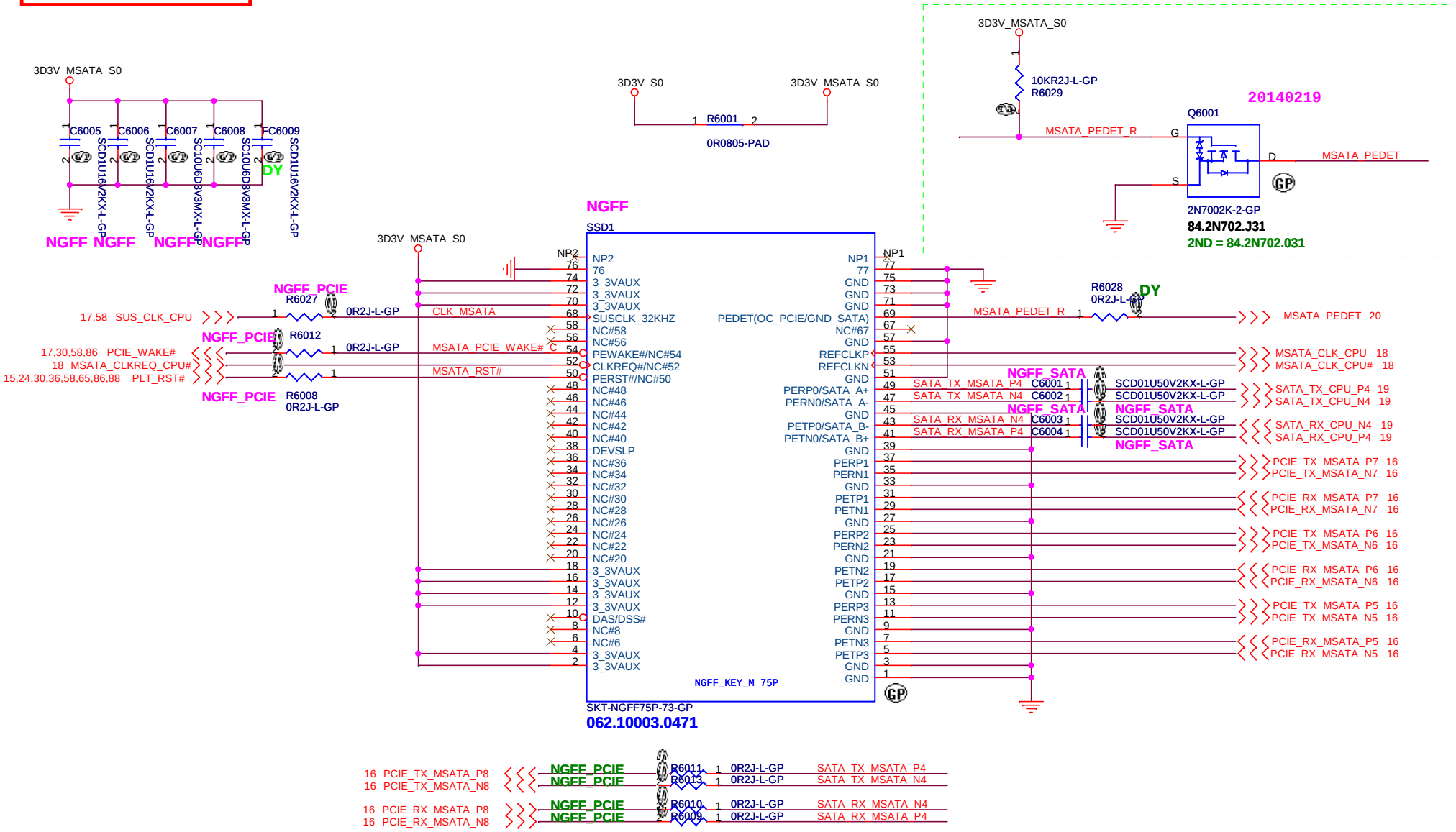
Title	WWAN CONN	
Size A4	Document Number Hades HBS 860M	Rev SB
Date: Friday, April 11, 2014	Sheet 59 of 102	

Mini Card Connector (NGFF m-SATA)

SSID = m-SATA



SATA/PCIe Gen 2 and Gen 3 Capacitor Values

Condition	PCIe Only	SATA Only	PCIe/SATA
PCH Tx	100 nF	10 nF	100 nF
PCH Rx	None	10 nF[2]	None[3]

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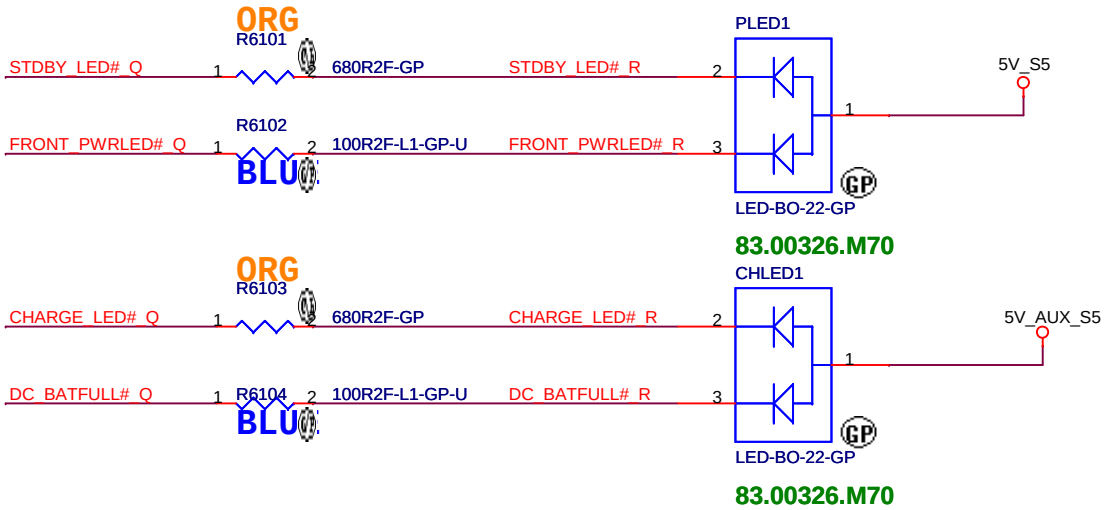
Title: NGFF m-SATA Connector

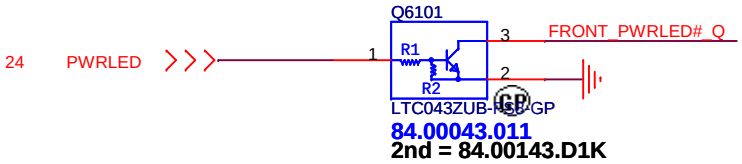
Size: Custom | Document Number: Hades_HBS 860M | Rev: SB

Date: Wednesday, May 28, 2014 | Sheet 60 of 102

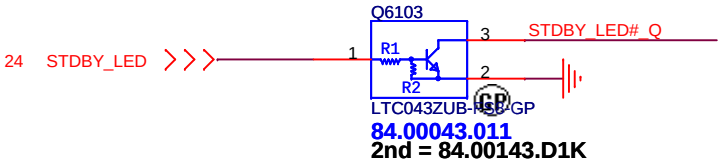
SSID = User.Interface



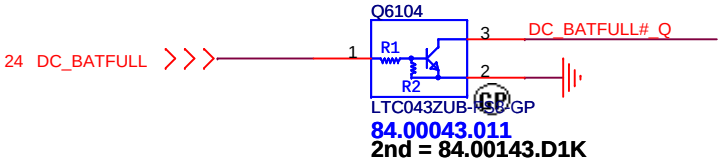
Power Button_LED



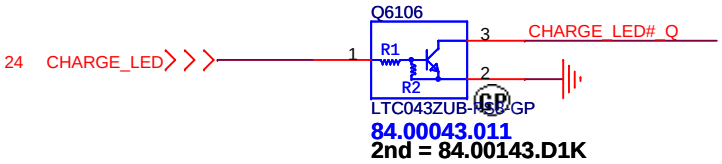
Power STDBY_LED



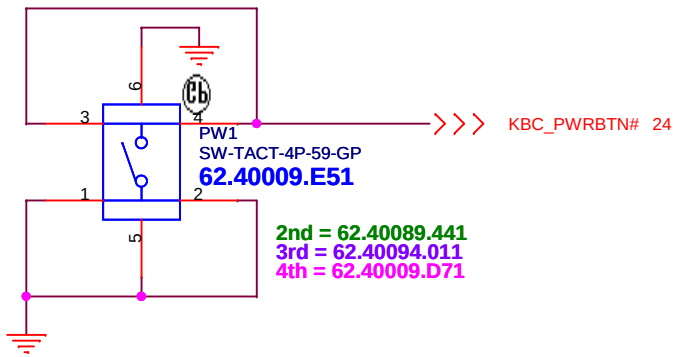
Battery LED2(DC_BATFULL)



Battery LED1(CHARGE)



Power Button



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Title: LED Bard/Power Button

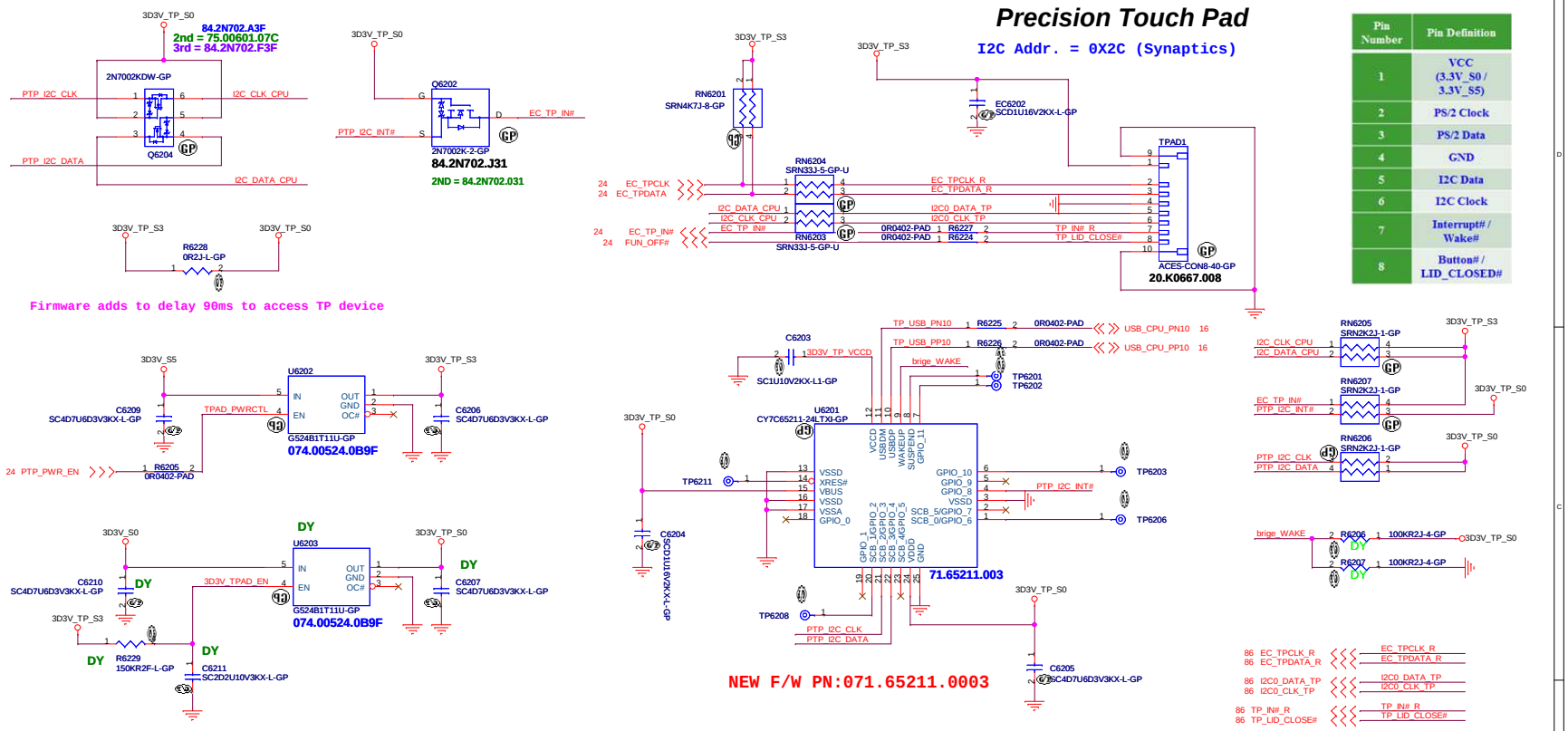
Size	Document Number	Rev
A4	Hades_HBS 860M	SB

Date: Monday, May 26, 2014 Sheet 61 of 102

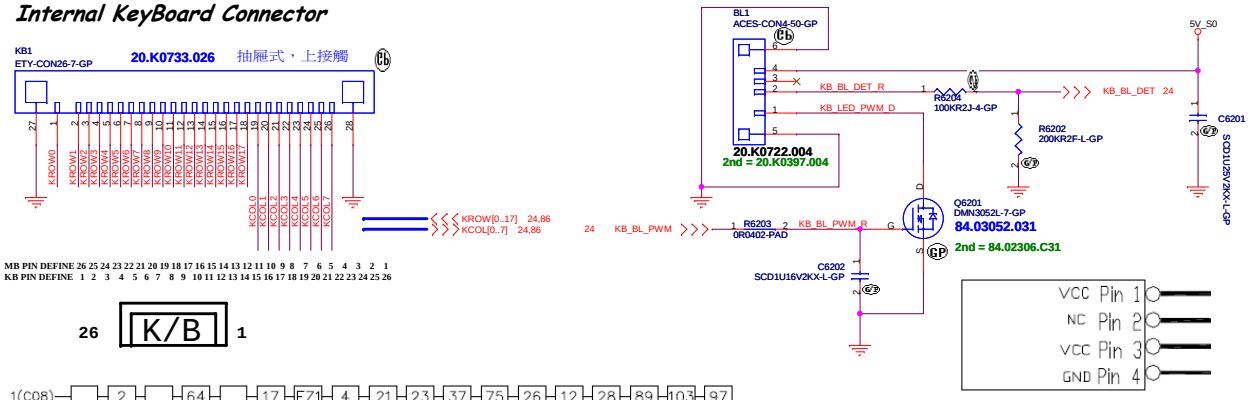
Precision Touch Pad

I2C Addr. = 0X2C (Synaptics)

Pin Number	Pin Definition
1	VCC (3.3V_S0 / 3.3V_S5)
2	PS/2 Clock
3	PS/2 Data
4	GND
5	I2C Data
6	I2C Clock
7	Interrupt# / Wake#
8	Button# / LID_CLOSED#



Internal KeyBoard Connector



MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

26 K/B 1

	R01	R02	R03	R04	R05	R06	R07	R08	R09	R10	R11	R12	R13	R14	R15	R16	R17	R18
1(C08)		2		64		17	EZ1	4	21	23	37	75	26	12	28	89	103	97
2(C07)		14				46	62	131	49	50	61	129	41	$	79	84	76	102
3(C06)		31				47	60	48	34	51	53	132	54	55	80	40	101	86
4(C05)		30	57			32	EZ3	33	35	36	52	130	€		83	29	85	104
5(C04)		16			127	18	EZ4	19	20	22	38	100	39	27	45	43	99	56
6(C03)		1		58		3	EZ6	5	6	8	24	91	25	11	13	15	92	98
7(C02)		112	44			113	EZ5	115	7	9	119	105	10	123	124	126	106	93
8(C01)	59	110				114	EZ2	116	117	118	120	96	121	122	90	81	95	108

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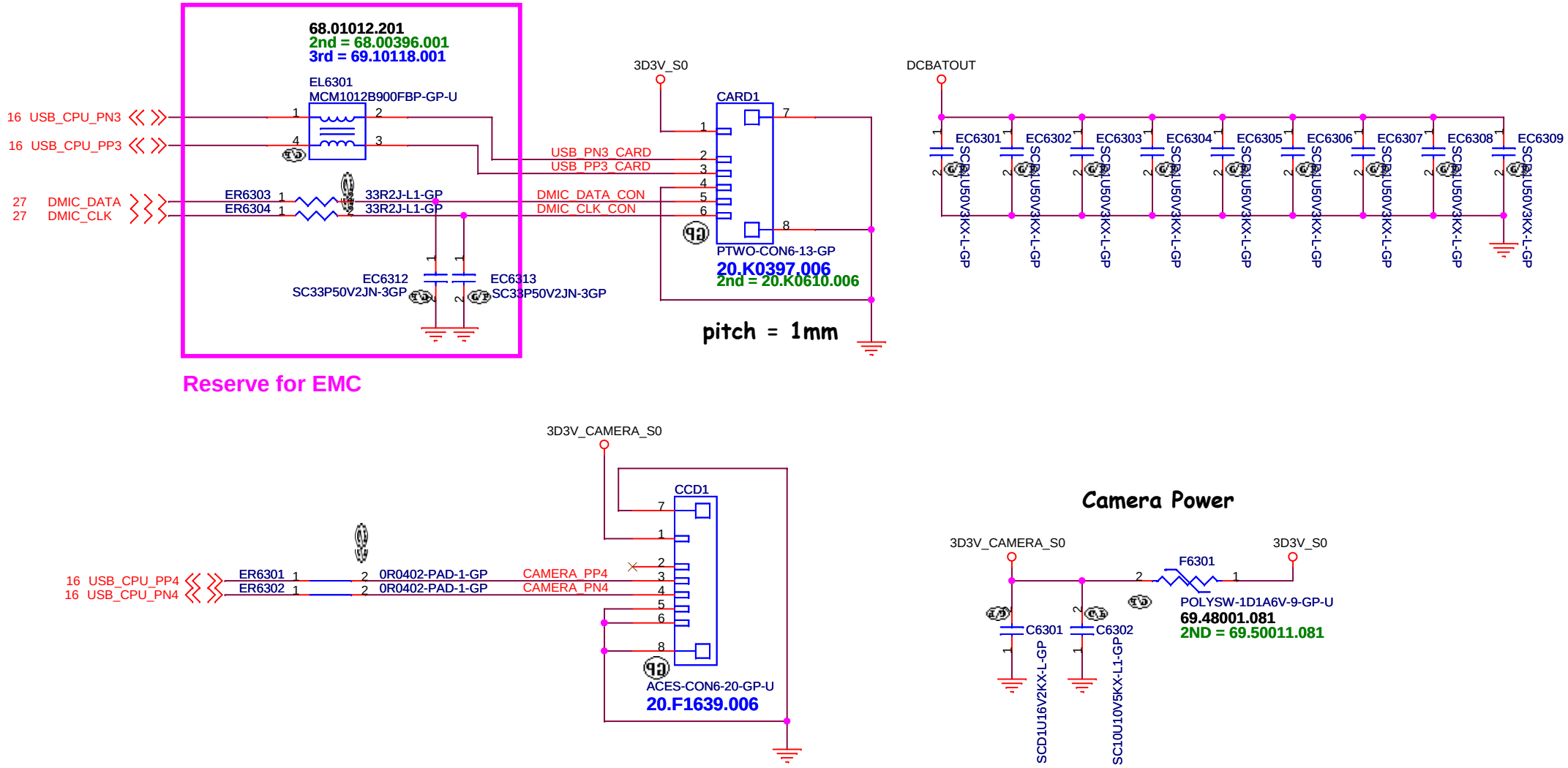
Title: Key Board/Touch Pad

Size: Custom | Document Number: Hades_HBS 860M | Rev: SB

Date: Wednesday, June 04, 2014 | Sheet 62 of 102



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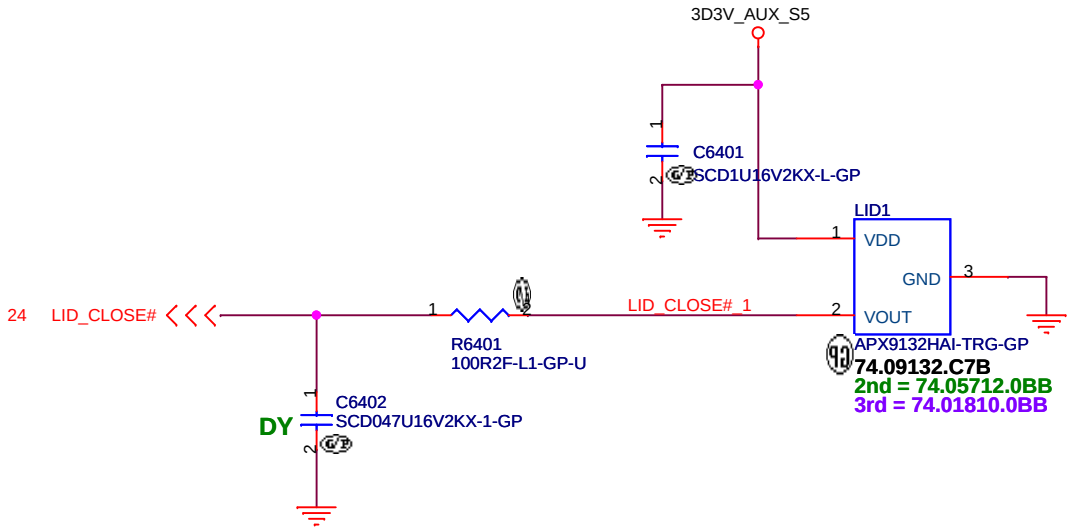
Title: **IO Board Connector**

Size	Document Number	Rev
A4	Hades_HBS 860M	SB

Date: Wednesday, May 21, 2014 Sheet 63 of 102



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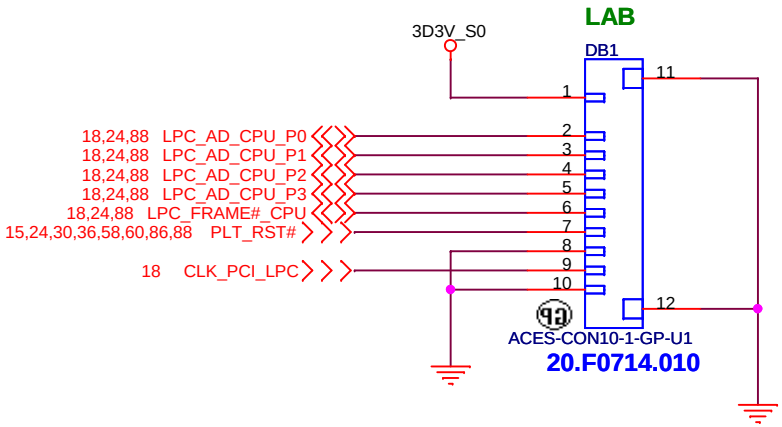
Title

Hall Sensor

Size	Document Number	Rev
A4	Hades_HBS 860M	SB

Date: Friday, April 11, 2014 Sheet 64 of 102



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Title

Dubug connector

Size	Document Number	Rev
A4	Hades HBS 860M	SB

Date: Friday, April 11, 2014 Sheet 65 of 102

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Title	SENSOR HUB	
Size A3	Document Number Hades HBS 860M	Rev SB
Date: Friday, April 11, 2014	Sheet 66 of 102	

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

SDO="H"; address="3Ah"
***SDO="L"; address="38h"**

***CS="H"; mode="I2C"**
CS="L"; mode="SPI"

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Title	G Sensor	
Size A	Document Number Hades_HBS 860M	Rev SB
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Thunderbolt (1/5)

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Custom	**Hades_HBS 860M**	**SB**

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Thunderbolt (2/5)

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Thunderbolt (3/5)

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Custom	**Hades_HBS 860M**	**SB**

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Thunderbolt (4/5)

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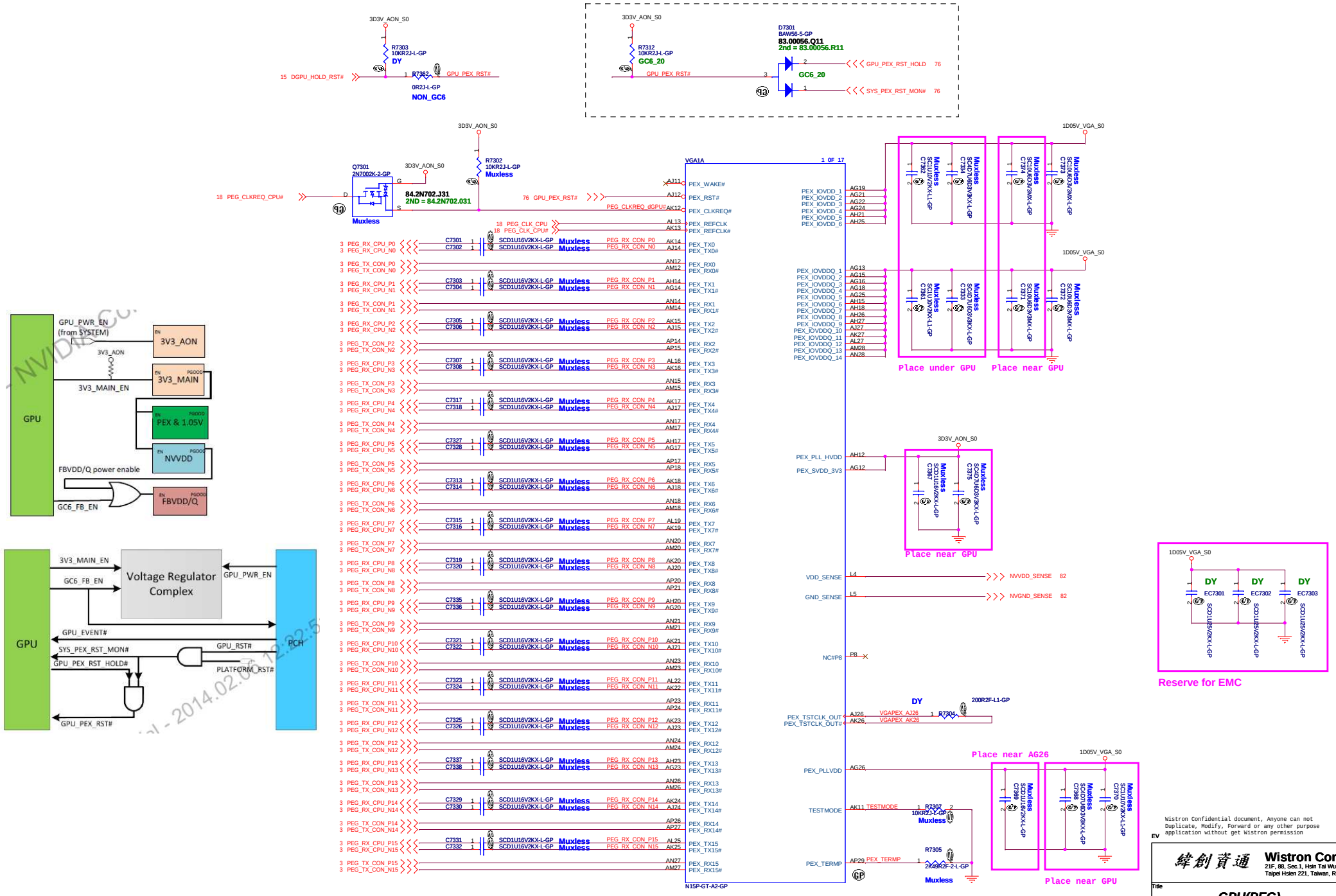
Title

Thunderbolt (5/5)

Size	Document Number	Rev
A4	**Hades HBS 860M**	**SB**

Date: Friday, April 11, 2014 Sheet 72 of 102



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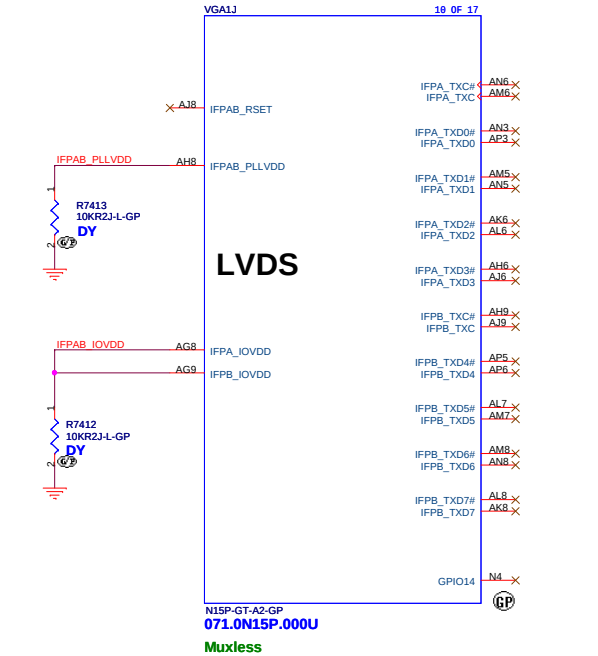
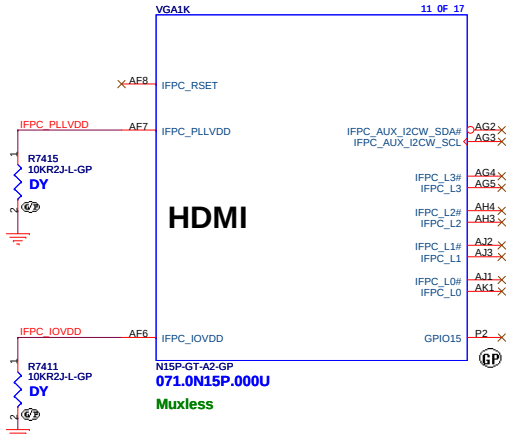
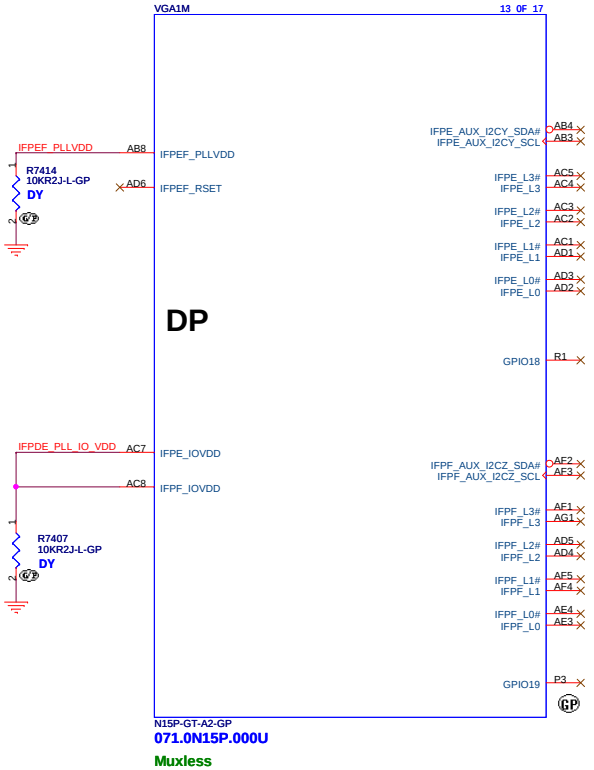
Title: GPU(PEG)

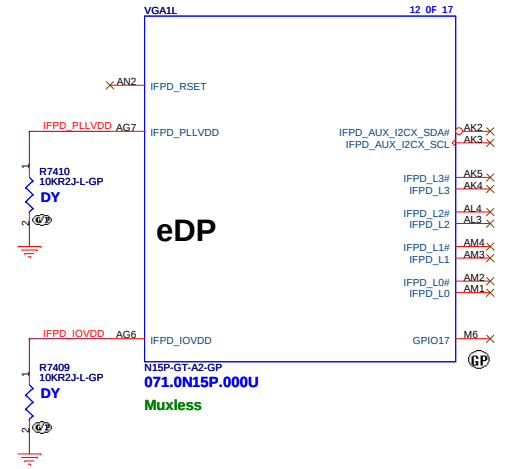
Size	Document Number	Rev
Custom	Hades_HBS 860M	SB

Date: Friday, April 11, 2014 Sheet 73 of 102









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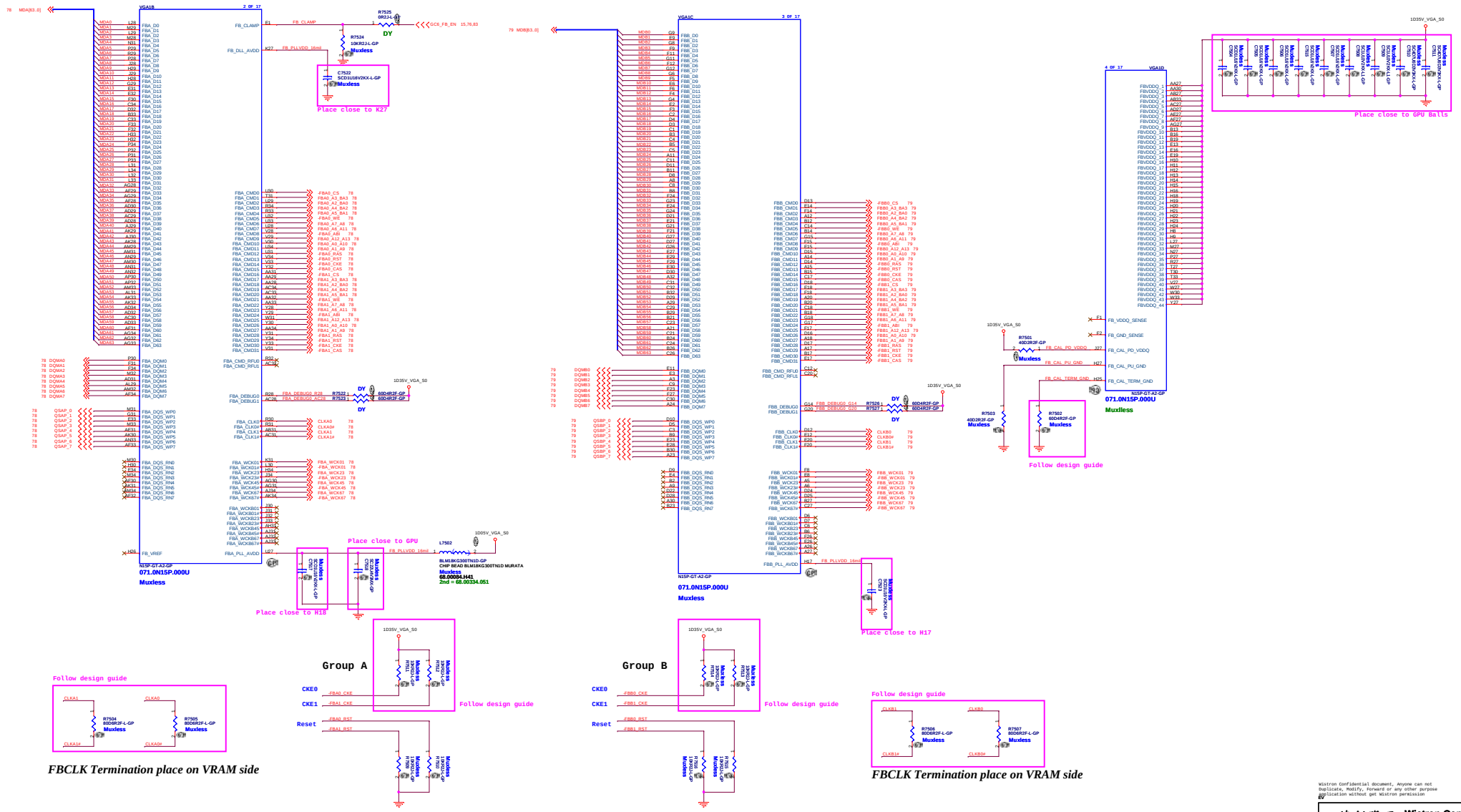
Title: *GPU (DIGITALOUT)*

Size	Document Number	Rev
Custom	Hades_HBS 860M	SB

Date: Friday, April 11, 2014 Sheet 74 of 102



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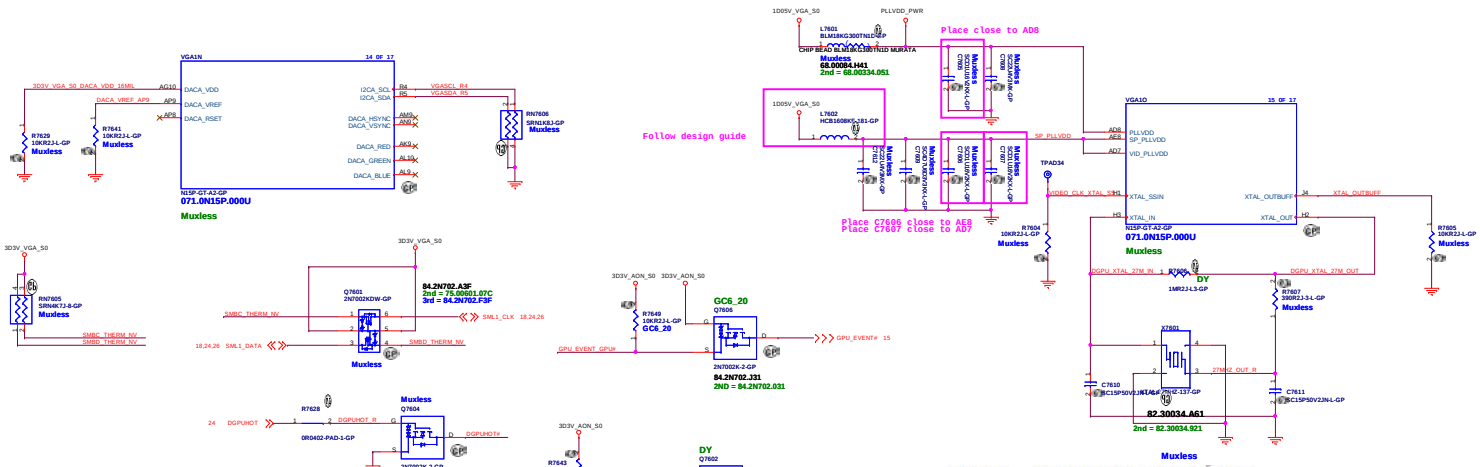
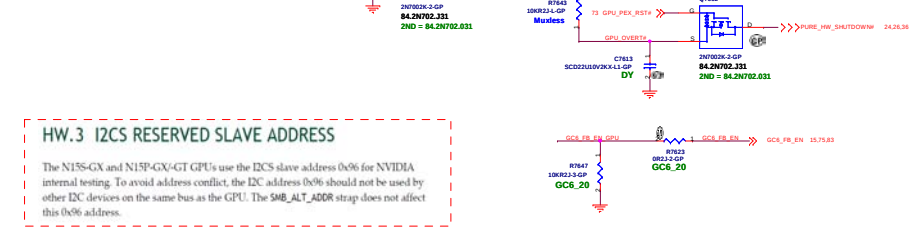
Title: GPU (VRAM I/F)

Size	Document Number	Rev
Custom	Hades HBS 860M	SB

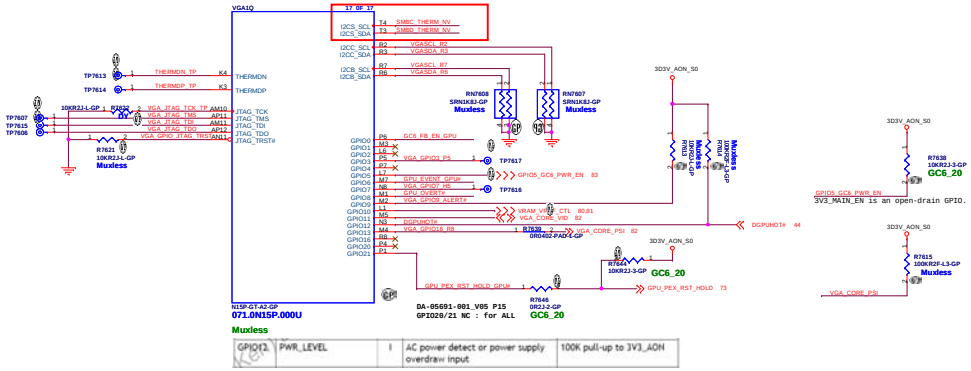
Date: Tuesday, May 27, 2014 Sheet 75 of 102



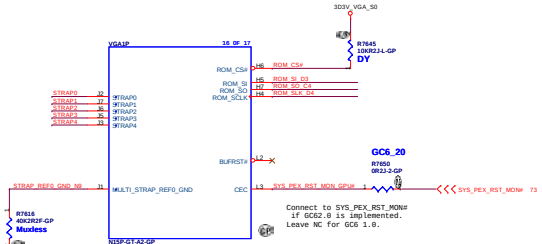


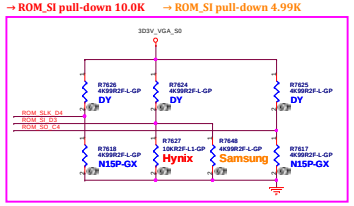
HW.3 I2CS RESERVED SLAVE ADDRESS

The N15S-GX and N15P-GX/-GT GPUs use the I2CS slave address 0x96 for NVIDIA internal testing. To avoid address conflict, the I2C address 0x96 should not be used by other I2C devices on the same bus as the GPU. The SMB_ALT_ADDR strap does not affect this 0x96 address.



GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 3V3_AON





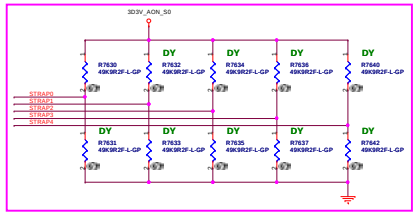


Table 2. Memory Configurations for Testing

Products	Type	VRAM Voltage	Vendor	Qty Parts	Memory Bus Width	Density	Speed Bin (MHz)	Part Number
N15S-GX	DDR3	1.5V	Hynix	8	128 bits	256MX16	1000	H5TC4G63AFR-11C
N15P-GT	DDR3	1.5V	Hynix	8	128 bits	256MX16	1000	H5TC4G63AFR-11C
	GDDR5	1.35V	Hynix	8	128 bits	256MX16	2500	H5GC4H24MFR-T2C
N15P-GX	GDDR5	1.35V	Hynix	8	128 bits	256MX16	2500	H5GC4H24MFR-T2C

Table 11. N15P-GX/GT GDDR5 Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
GDDR5	1.35V/ 1.35V		Samsung	K4G20325FD-FC03	D-die	0x0	2500	N/A	Post-production candidate
		128Mx16	Hynix	H5GC2H24BFR-T2C	B-die	0x1	2500	N/A	Post-production candidate
		256Mx16	Micron	EDW20328B8G-6A-F	B-die	0x3	2500	N/A	Post-production candidate
			Hynix	H5GC4H24MFR-T2C	M-die	0x2	2500	N/A	Production candidate
			Samsung	K4G41325FC-HC03	C-die	0x2	2500	N/A	Production candidate
			Micron	EDW4032BABG-60-F	A-die	0x4	2500	N/A	Post-production candidate

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

4.99Kohm	64.49915.6DL
10Kohm	64.10025.L0L
15Kohm	64.15025.6DL
20Kohm	64.20025.6DL
24.9Kohm	64.24925.6DL
30.1Kohm	64.30125.6DL
34.8Kohm	64.34825.6DL
45Kohm	64.45325.6DL

Table 15-3. GB2B-64 and GB4B-128 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND and stuff 50kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AON and pull-down to GND for forward compatibility.			

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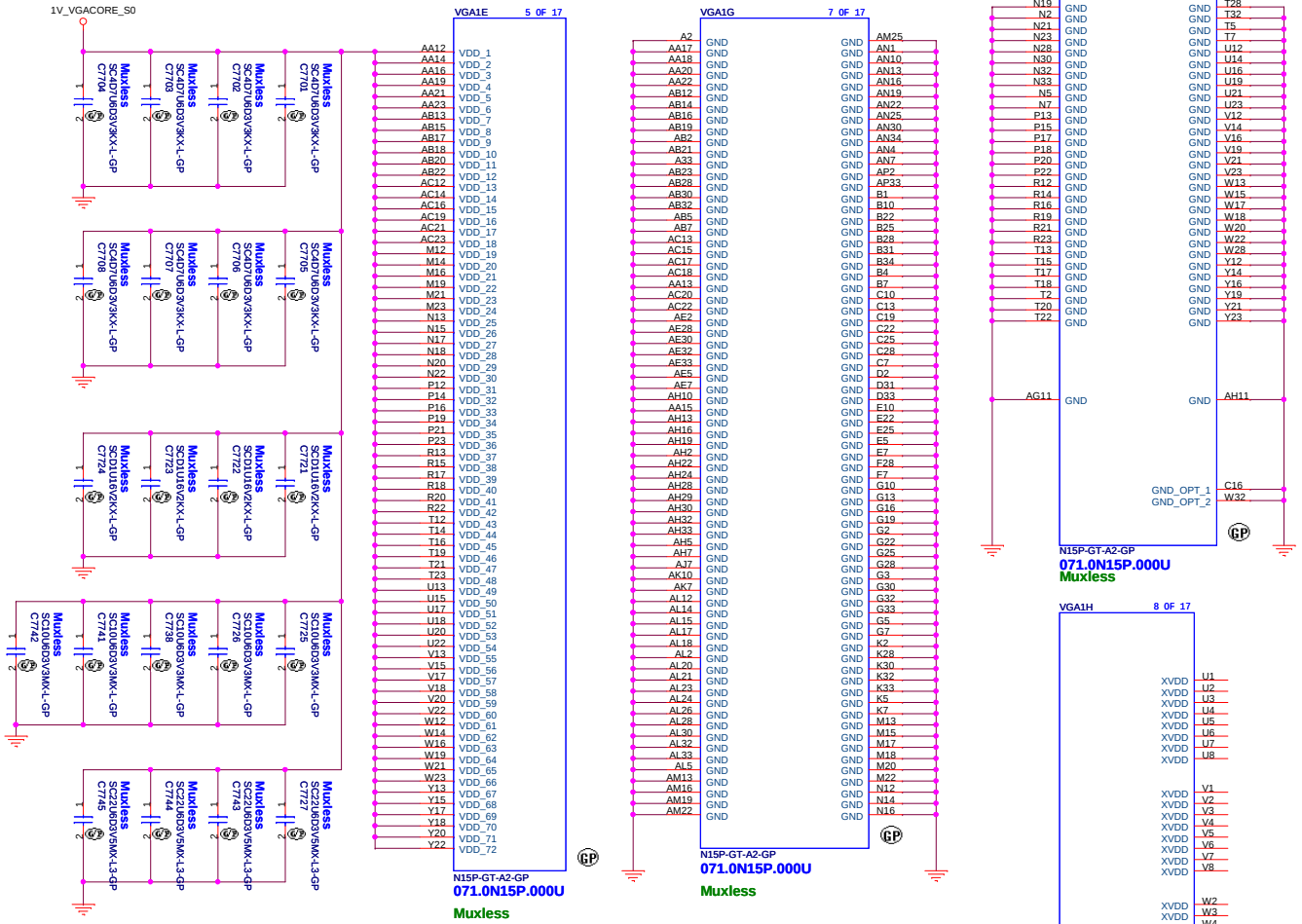
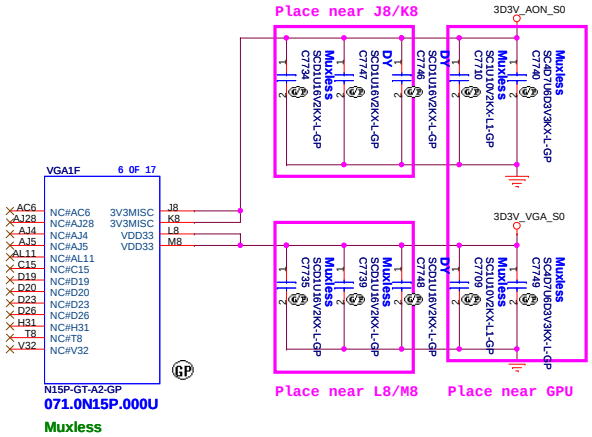
Title: GPU (GPIO/STRAP)
Size: A3 | Document Number: Hades HBS 860M | Rev: SB
Date: Thursday, May 29, 2014 | Sheet 78 of 102



4.7uF(X6S)	15
1uF(X6S)	8
22uF(X5R)	7
4.7uF(X5R)	5
330uF(POS)	1



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Title: GPU (POWER/GND)

Size: Custom | Document Number: Hades_HBS 860M | Rev: SB

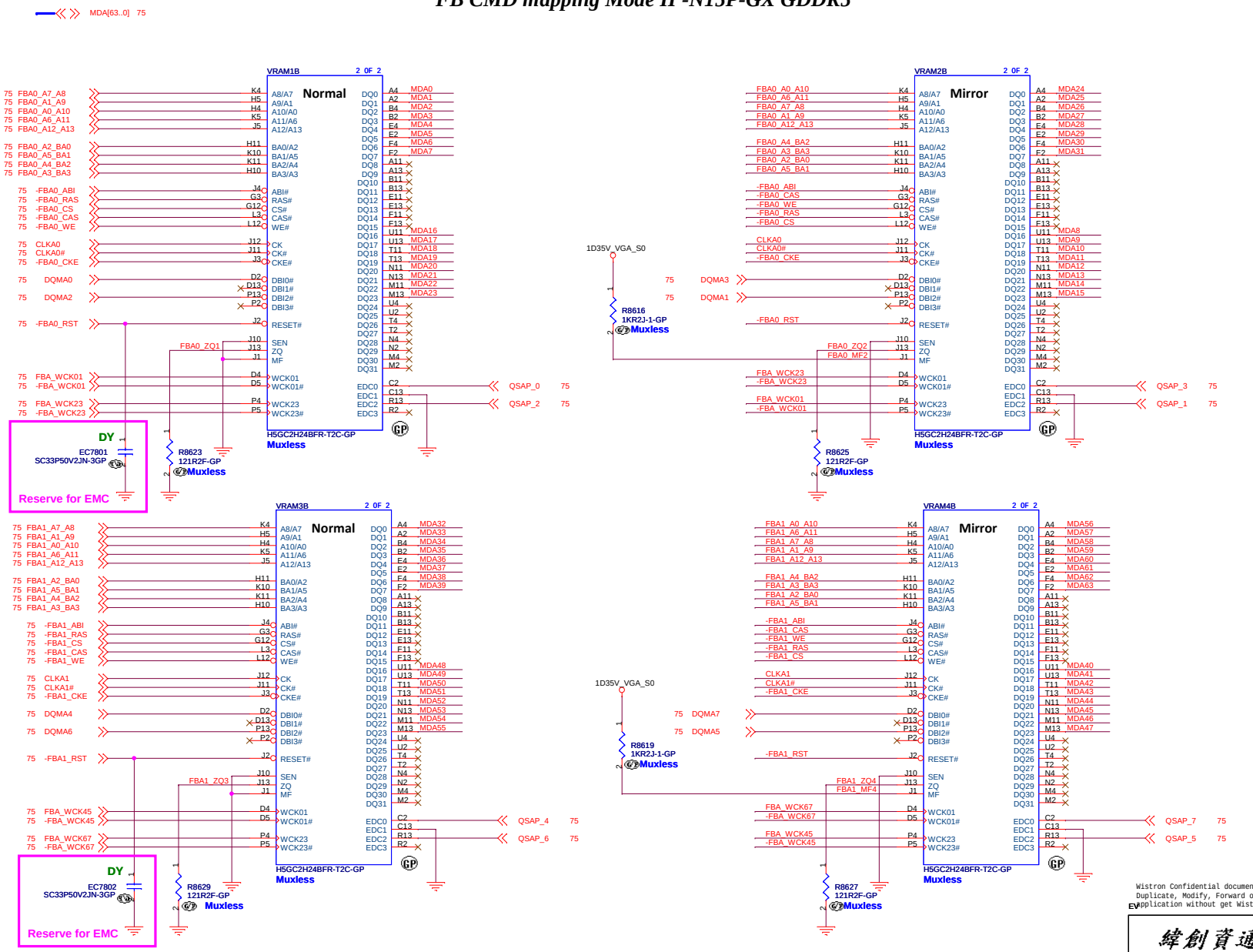
Date: Thursday, May 22, 2014 | Sheet 77 of 102

TABLE
GDDR5 VIDEO MEMORY 72.05224.A0U 72.20325.B0U

	HYNIX 2GBITS (64Mx32)	SAMSUNG 2GBITS (64Mx32)	HYNIX 4GBITS (128Mx32)	SAMSUNG 4GBITS (128Mx32)
U91 U92 U93 U94 U95 U96 U97 U98	H5GQ2H24AFR-T2C	K4G20325FD-FC04	H5GC4H24MFR (tentative)	K4G41325FC-HC03 (tentative)

LOGIC

FB CMD mapping Mode H -N15P-GX GDDR5



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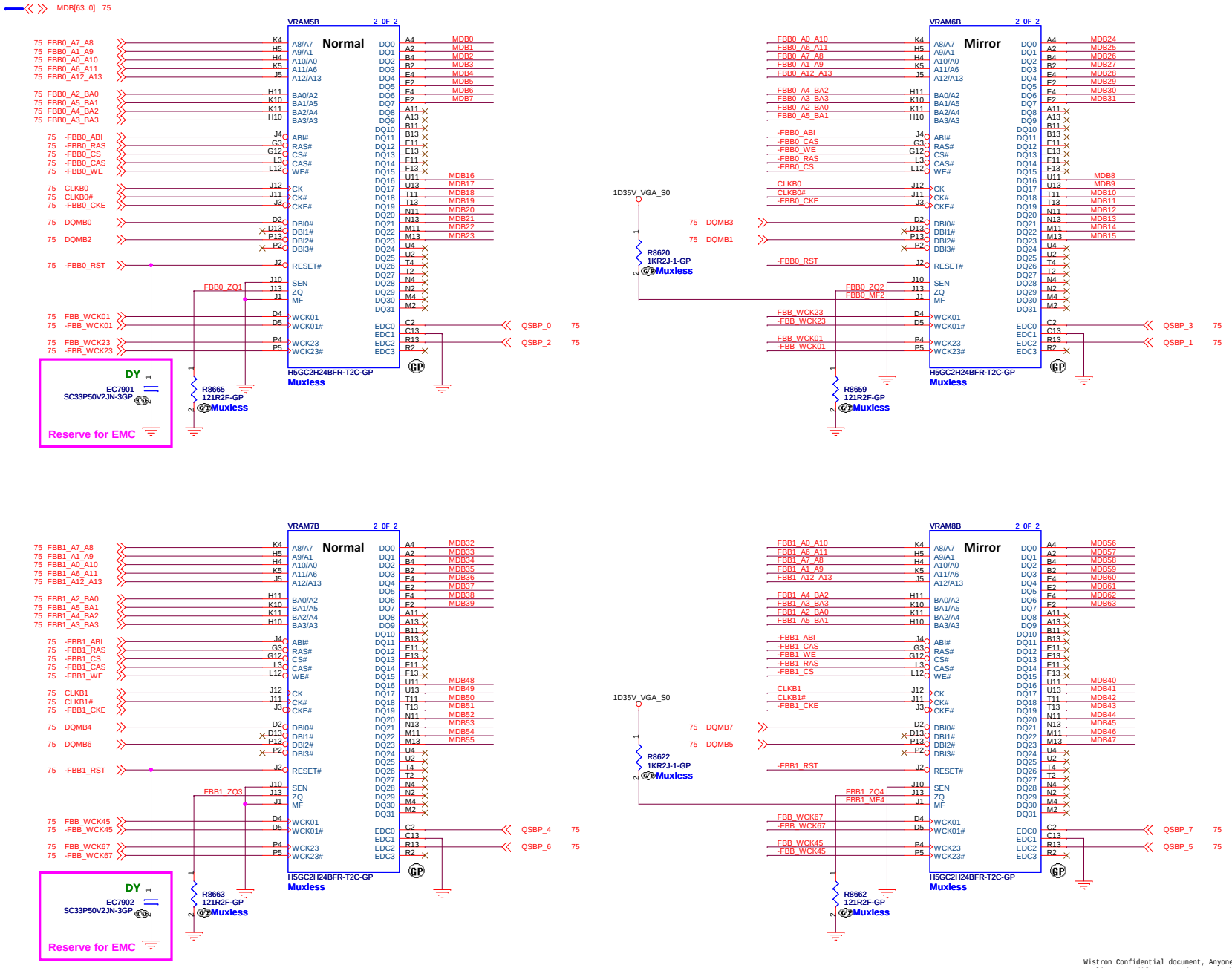
Title: VRAM A
Size: Custom
Document Number: Hades_HBS 860M
Rev: SB
Date: Friday, April 11, 2014
Sheet 78 of 102



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Title: ***VRAM B***

Size	Document Number	Rev
Custom	Hades_HBS 860M	SB

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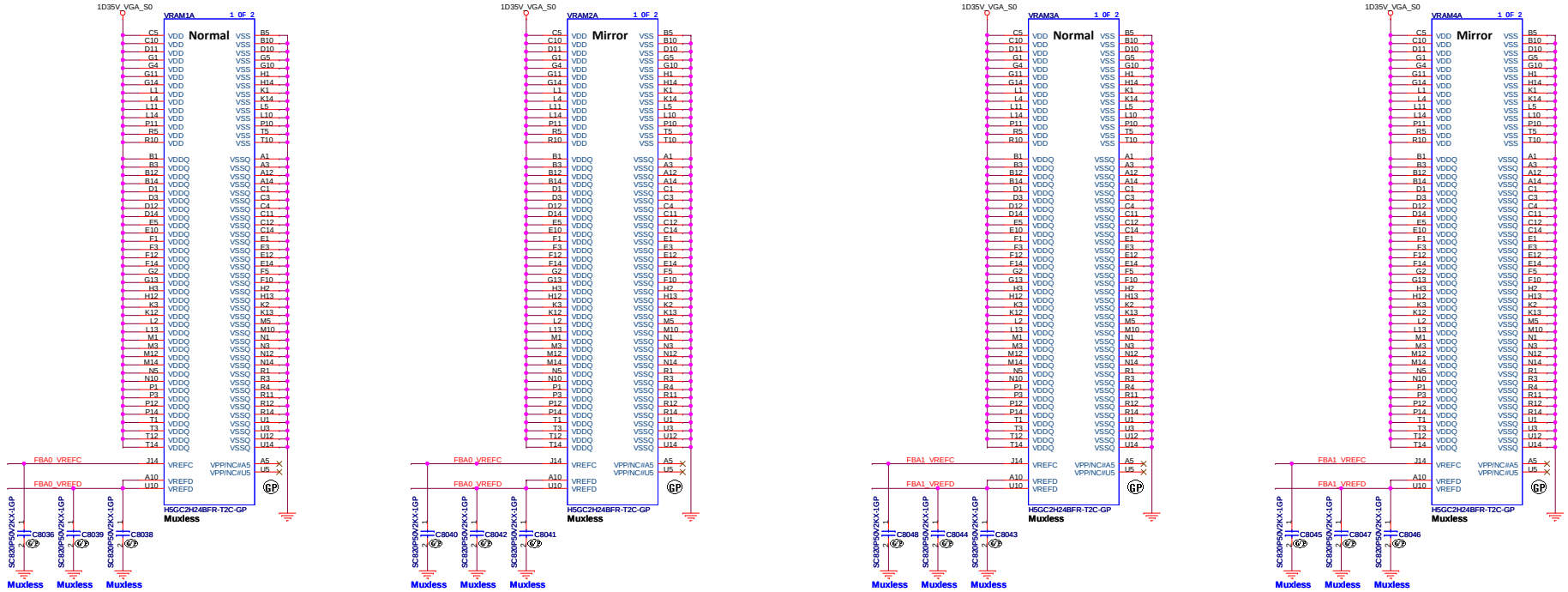
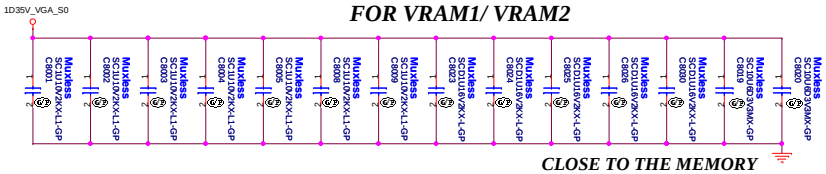
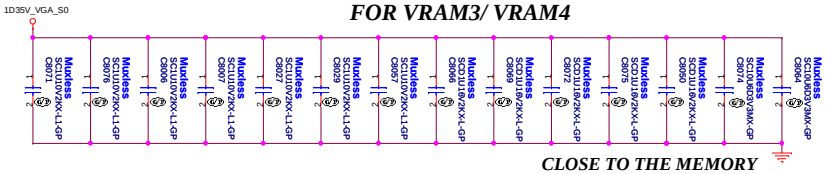


FOR VRAM1/ VRAM2



CLOSE TO THE MEMORY

FOR VRAM3/ VRAM4



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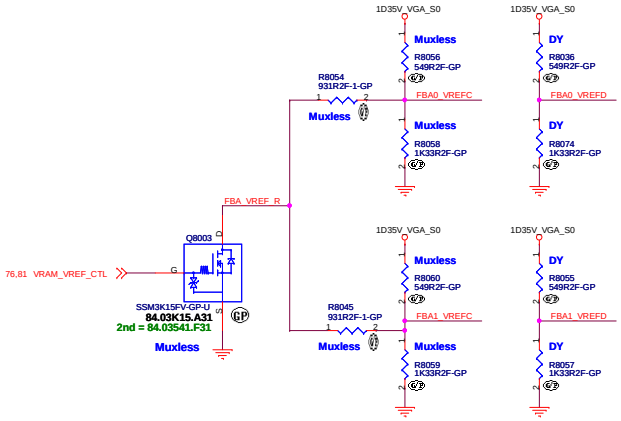

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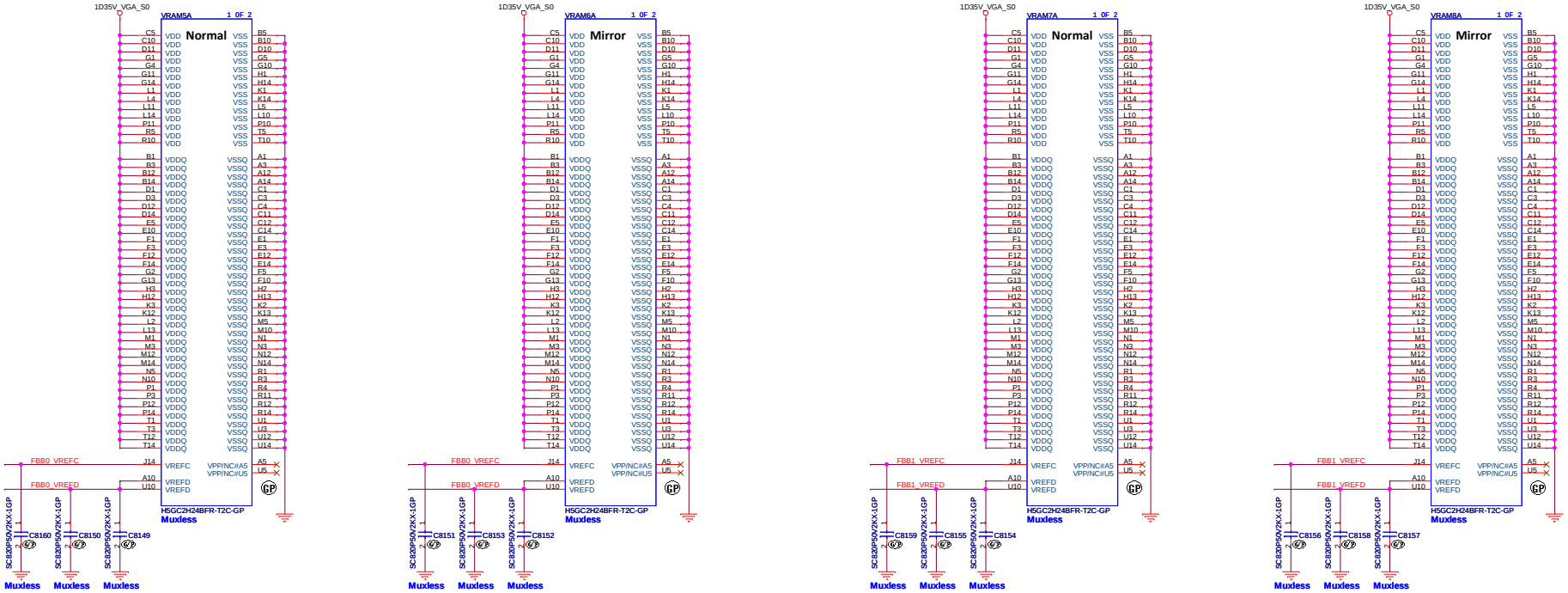
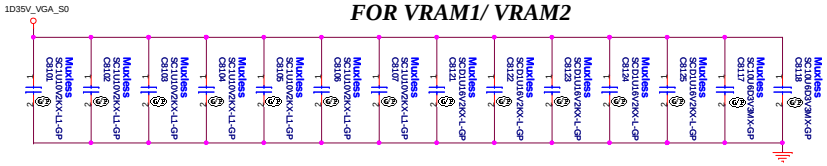
Title	VGA Power A	
Size: Custom	Document Number: Hades_HBS 860M	Rev: SB
Date: Friday, April 11, 2014	Sheet 80 of 102	

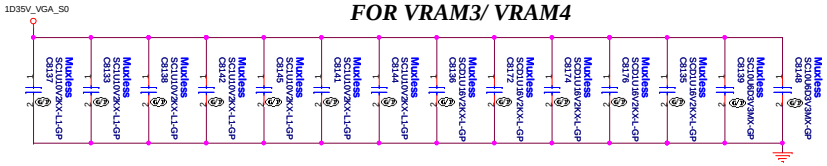


FOR VRAM1/ VRAM2

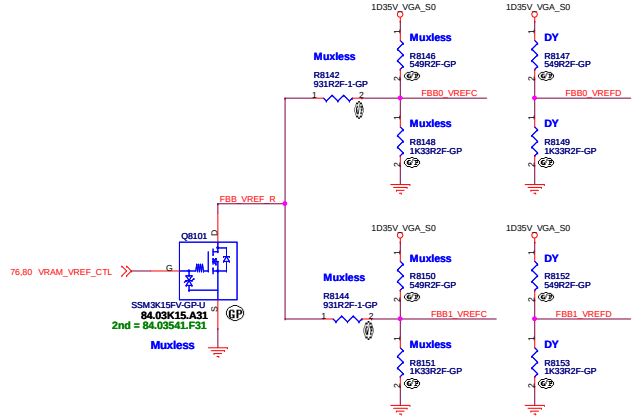


CLOSE TO THE MEMORY

FOR VRAM3/ VRAM4



CLOSE TO THE MEMORY



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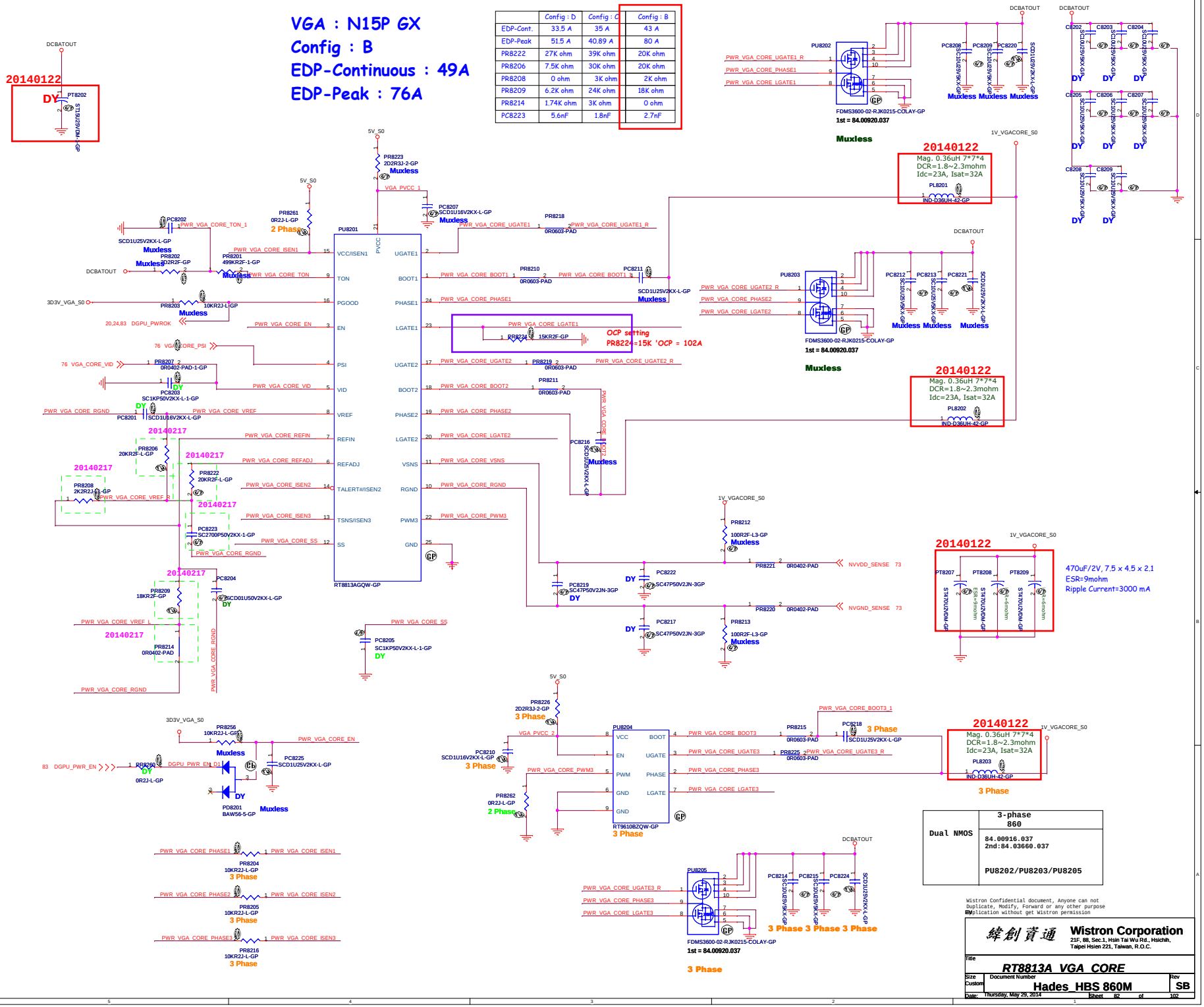
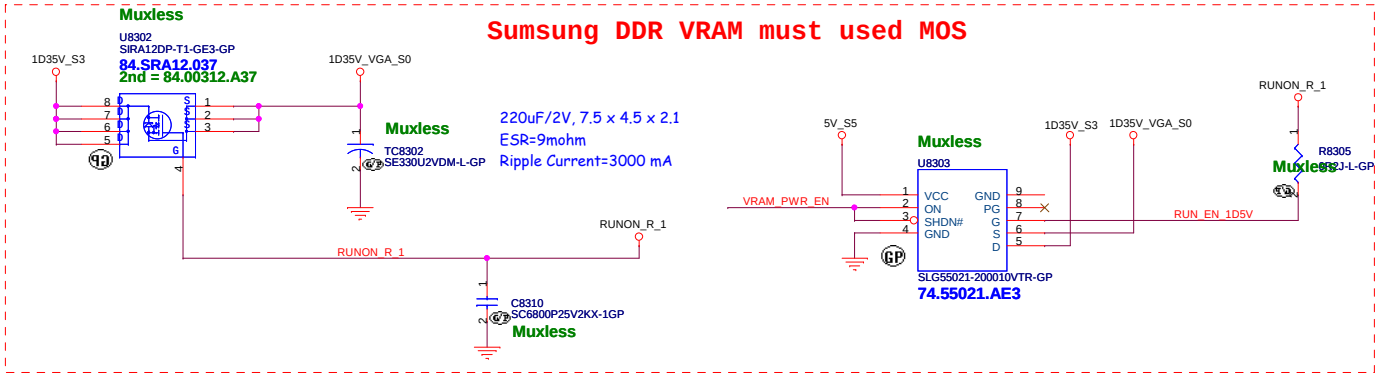
Title	VGA Power B		
Size Custom	Document Number Hades_HBS 860M		Rev SB
Date: Friday, April 11, 2014	Sheet 81 of 102		

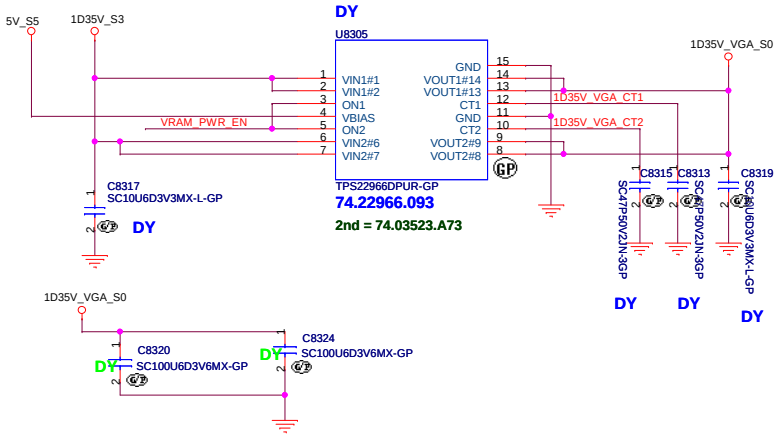
VGA : N15P GX
Config : B
EDP-Continuous : 49A
EDP-Peak : 76A

	Config : D	Config : C	Config : B
EDP-Cont.	33.5 A	35 A	43 A
EDP-Peak	51.5 A	40.89 A	80 A
PR8222	27K ohm	39K ohm	20K ohm
PR8206	7.5K ohm	30K ohm	20K ohm
PR8208	0 ohm	3K ohm	2K ohm
PR8209	6.2K ohm	24K ohm	18K ohm
PR8214	1.74K ohm	3K ohm	0 ohm
PC8223	5.6nF	1.8nF	2.7nF

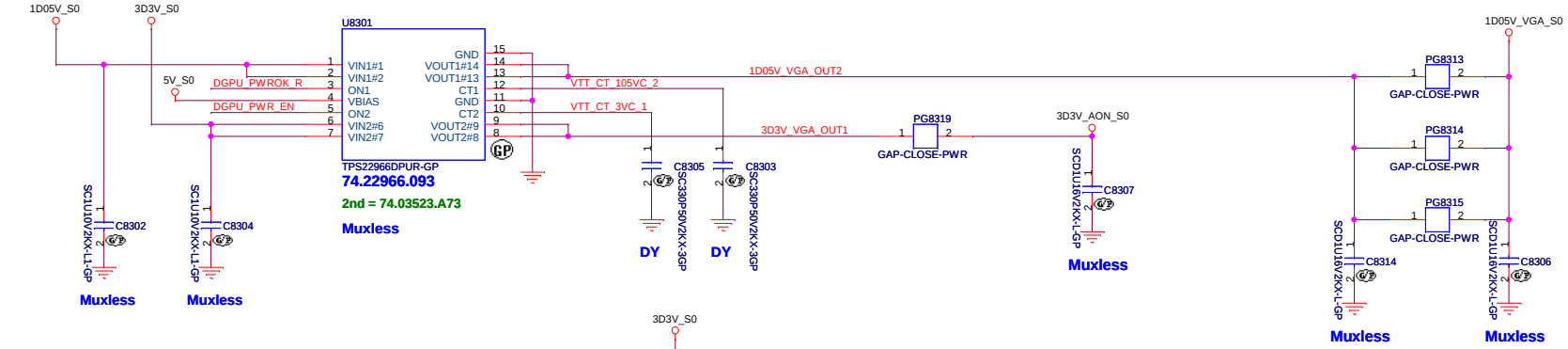


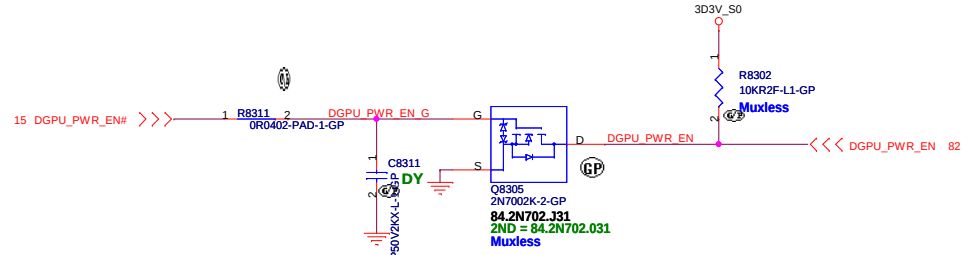
TPS22966 for VGA_1D35V(For VRAM GDDR5)

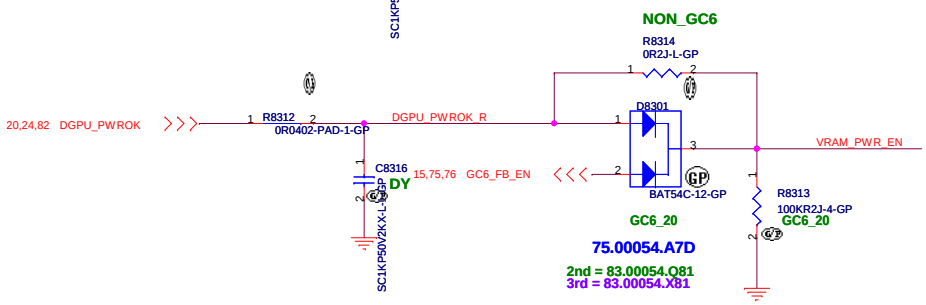


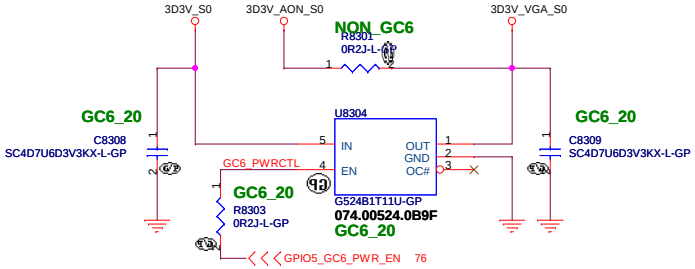


3D3V_S0 to 3D3V_VGA_S0
1D05V_VTT to 1D05V_VGA_S0









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Title: DISCRETE VGA POWER

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Custom	Hades_HBS 860M	SB

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Switchable GFX LCD(1/2)

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Switchable GFX LCD(2/2)

Size	Document Number	Rev
A4	**Hades HBS 860M**	**SB**

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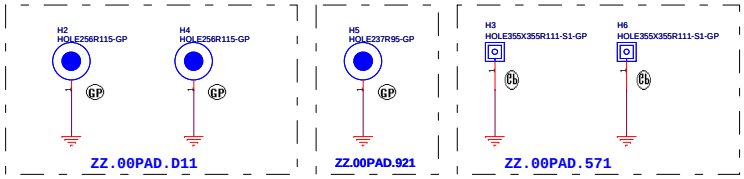

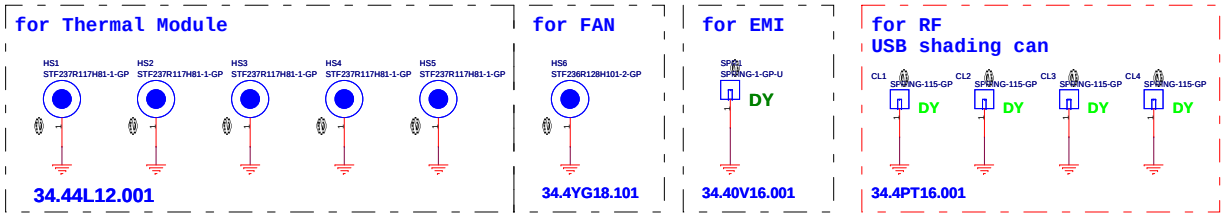

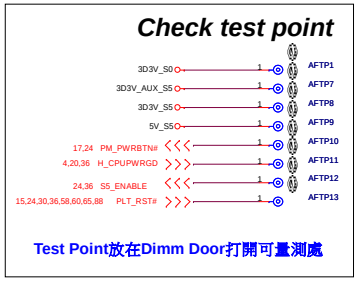

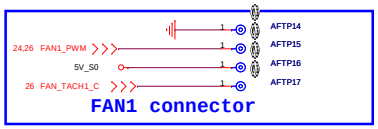

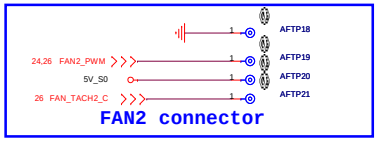

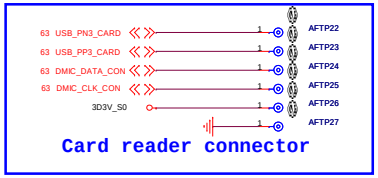

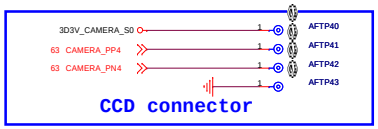

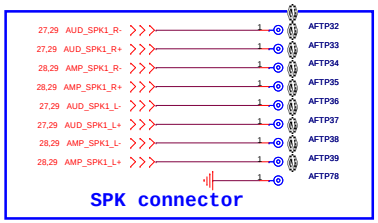

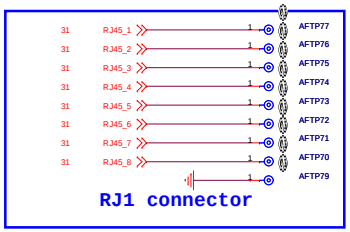

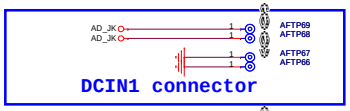

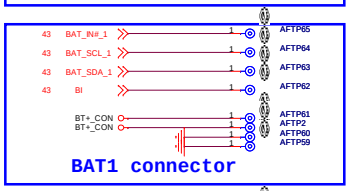

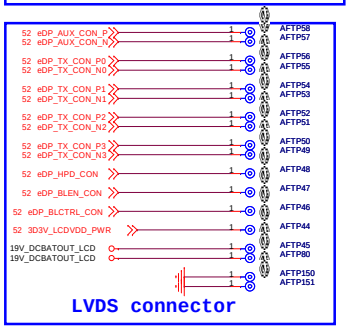

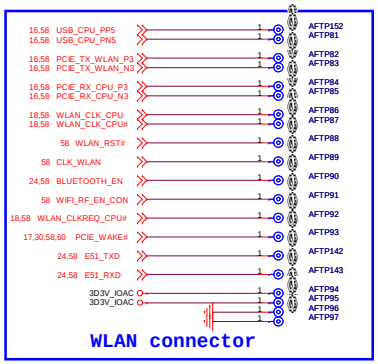

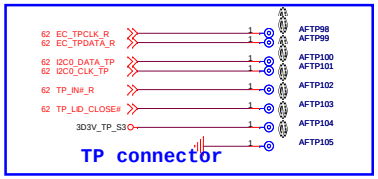

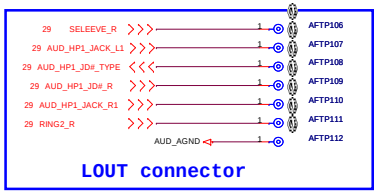

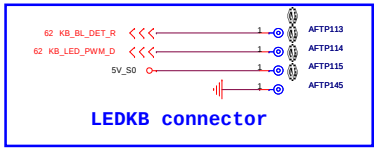

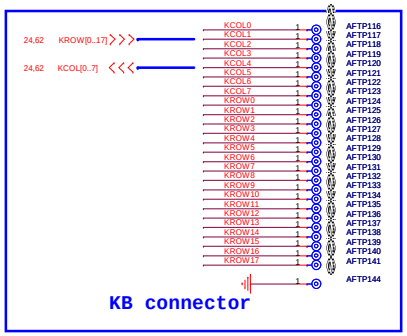

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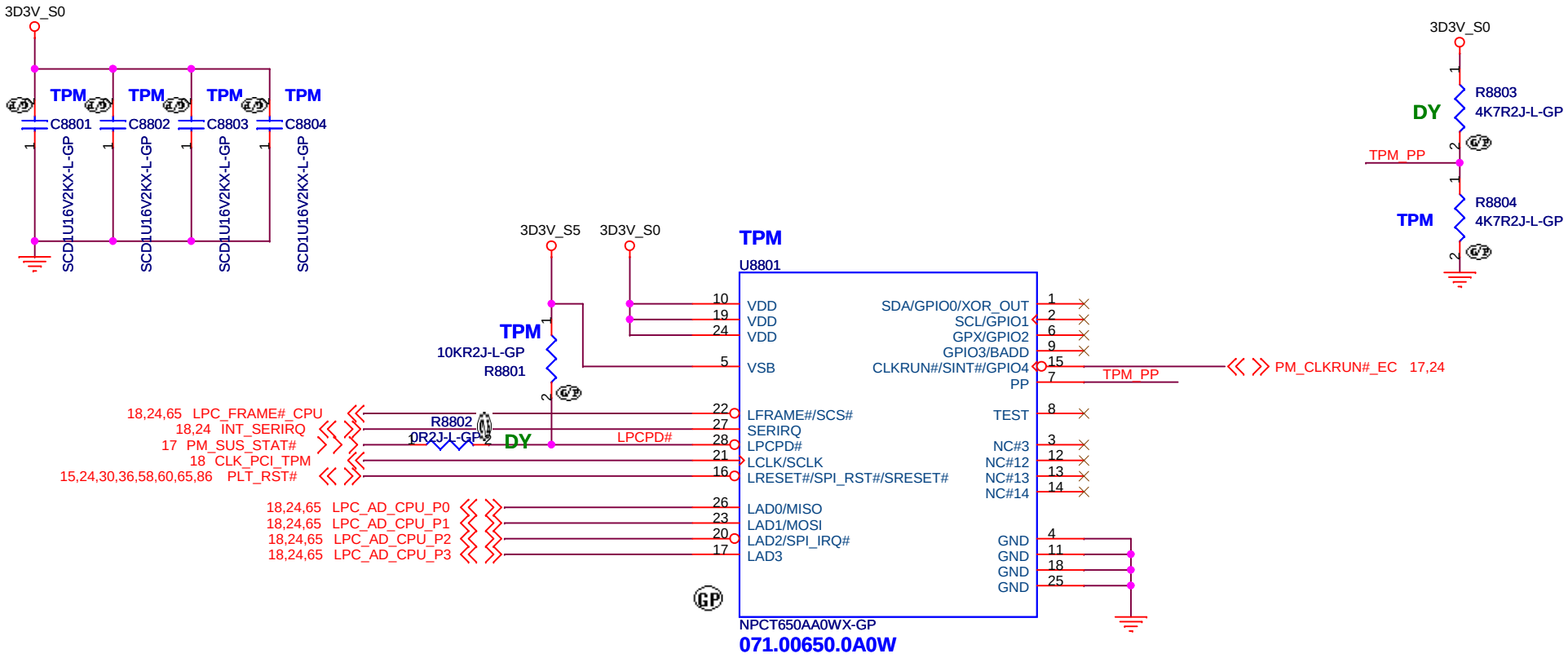

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Express Card

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Smart Card socket

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Switchable GFX eDP

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Bottom Docking

Size	Document Number	Rev
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Inter LAN WG1217LM

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LAN Switch

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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0[1]	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST#[1]	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4[1]	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST#[1]	0	System	18	HOOK7	DBR#[1]	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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Title: PCH_XDP

Size: A4 | Document Number: Hades_HBS 860M | Rev: SB

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Change History

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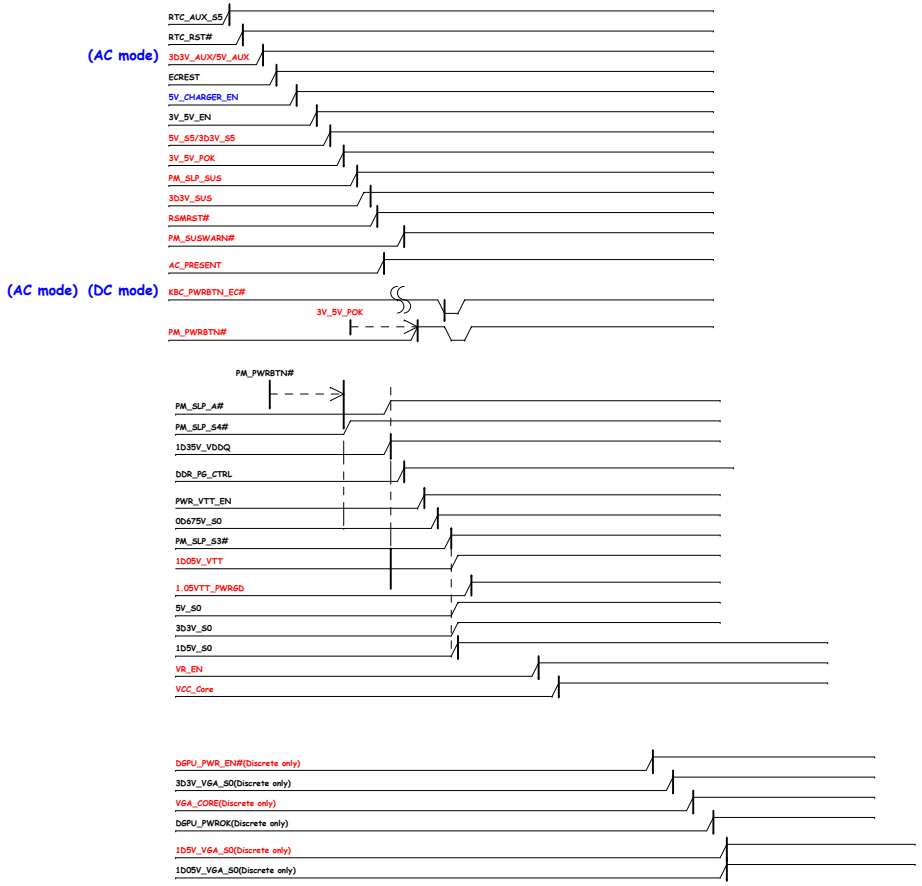
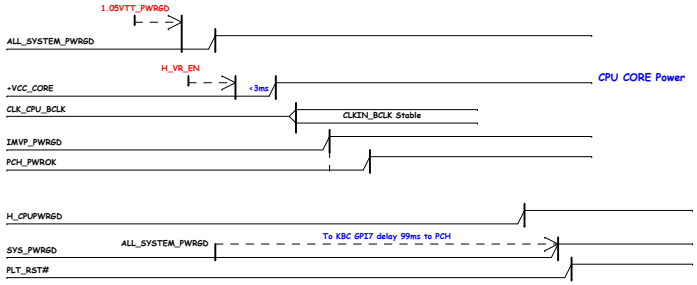
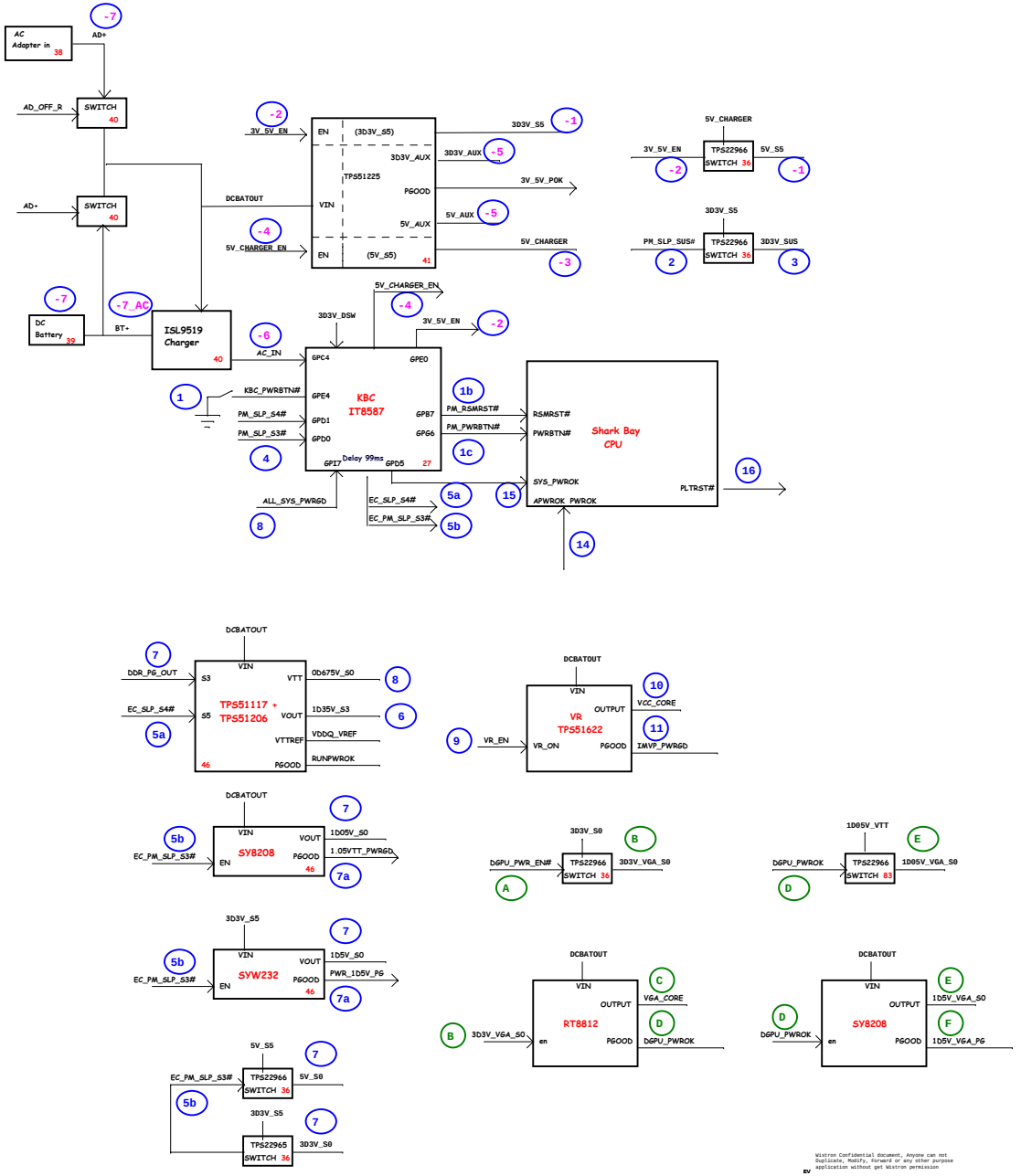
Intel-Power Up Sequence





SHARK BAY POWER UP SEQUENCE DIAGRAM



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Title	Power Sequence
Size A1	Document Number: Hades HBS 860M
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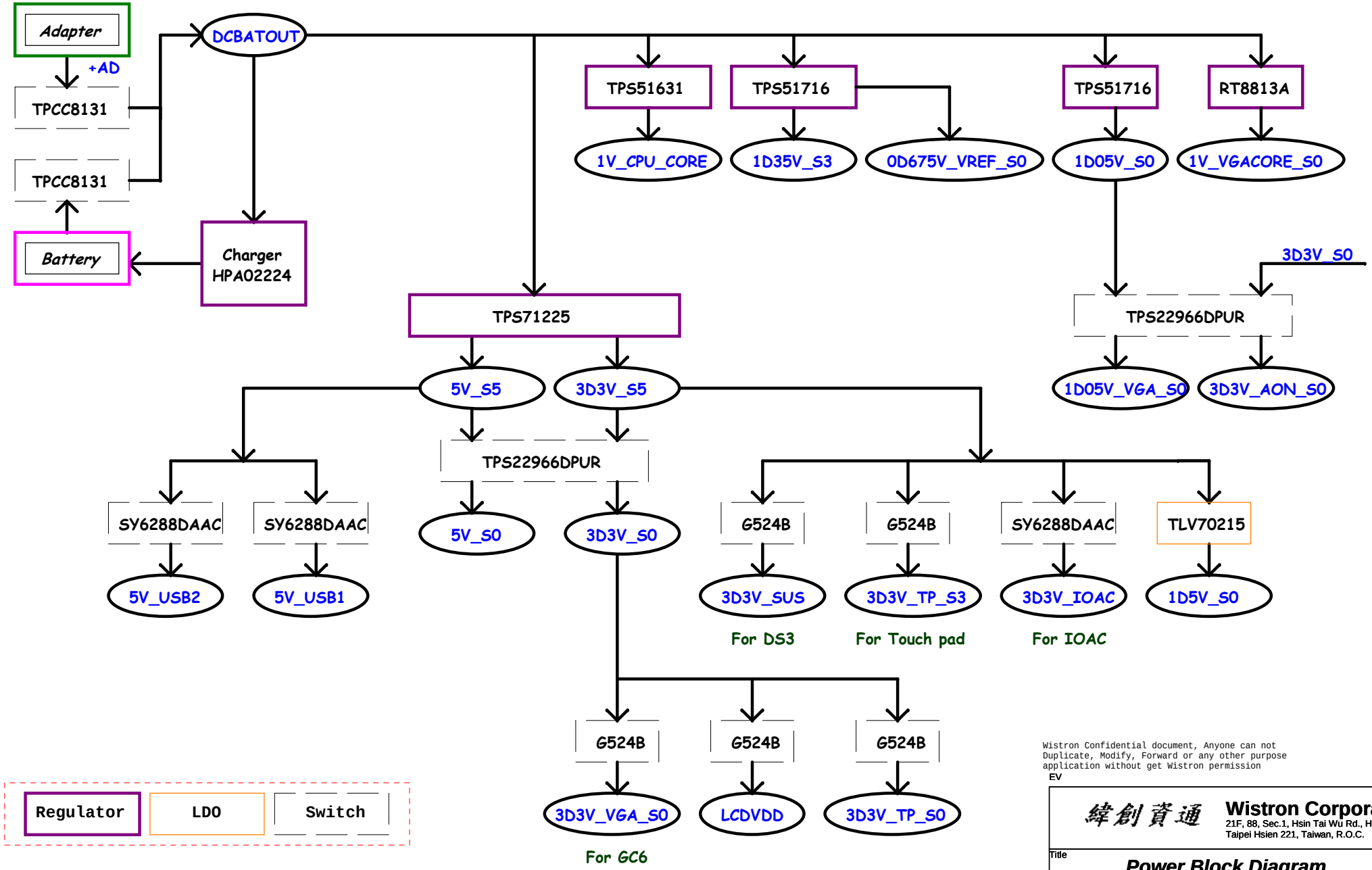

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Title: **Power Block Diagram**

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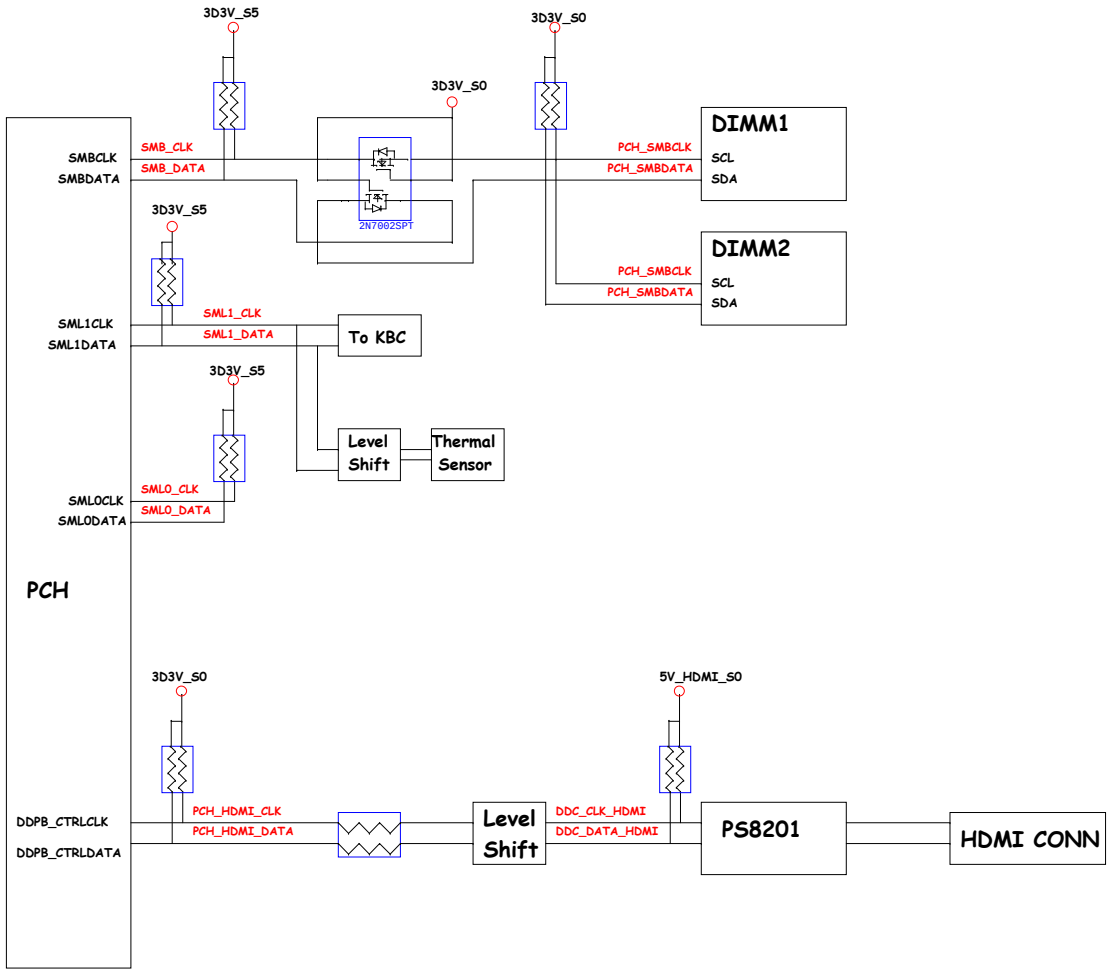
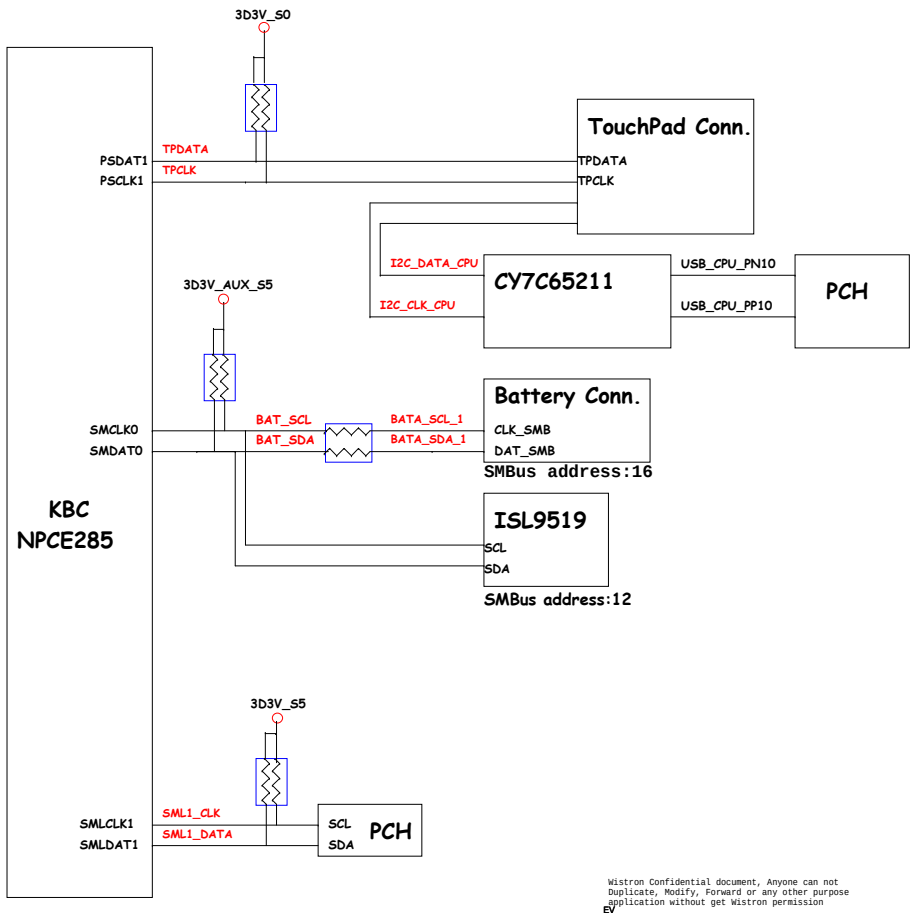
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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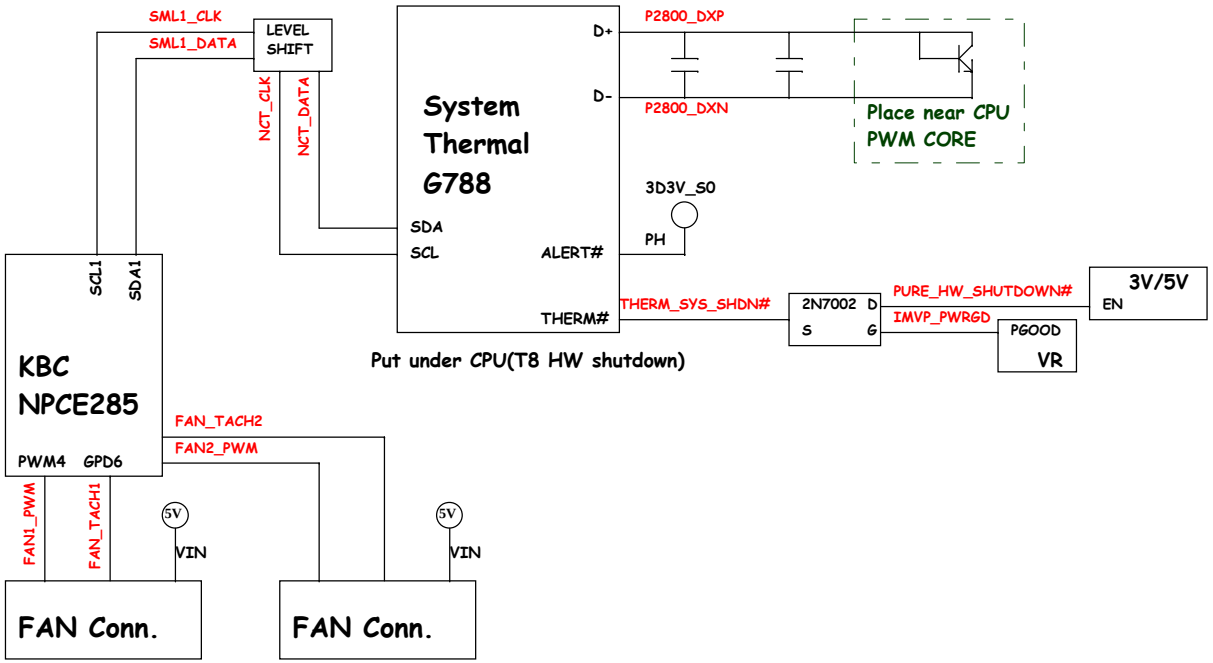
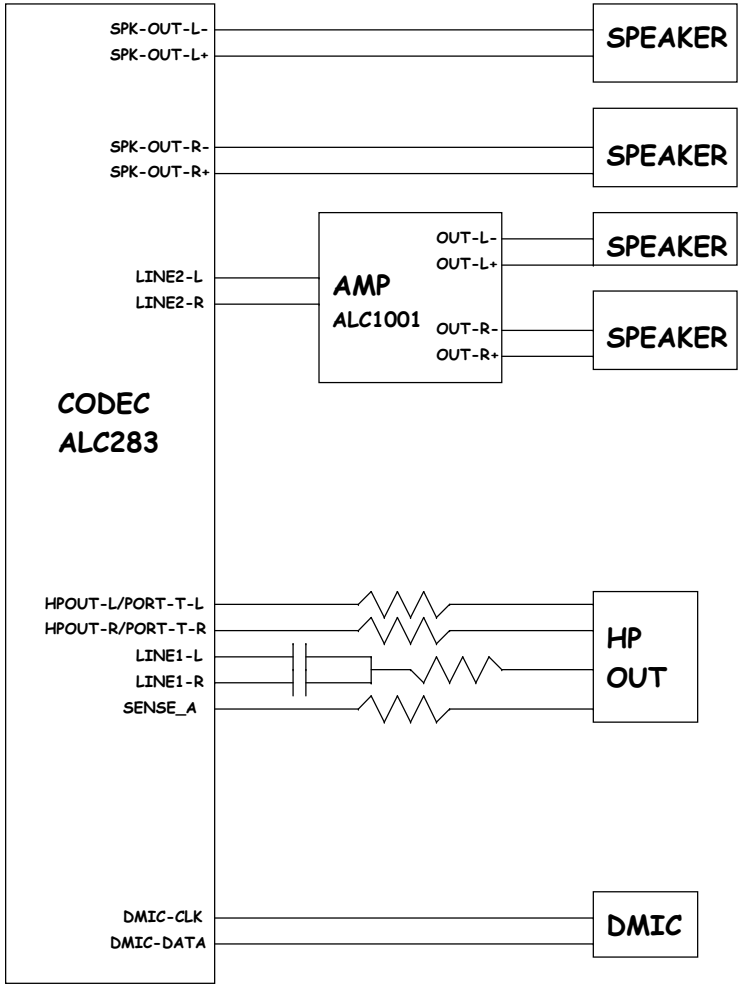
Thermal Block Diagram



Audio Block Diagram



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Title: THERMAL/AUDIO BLOCK DIAGRAM

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