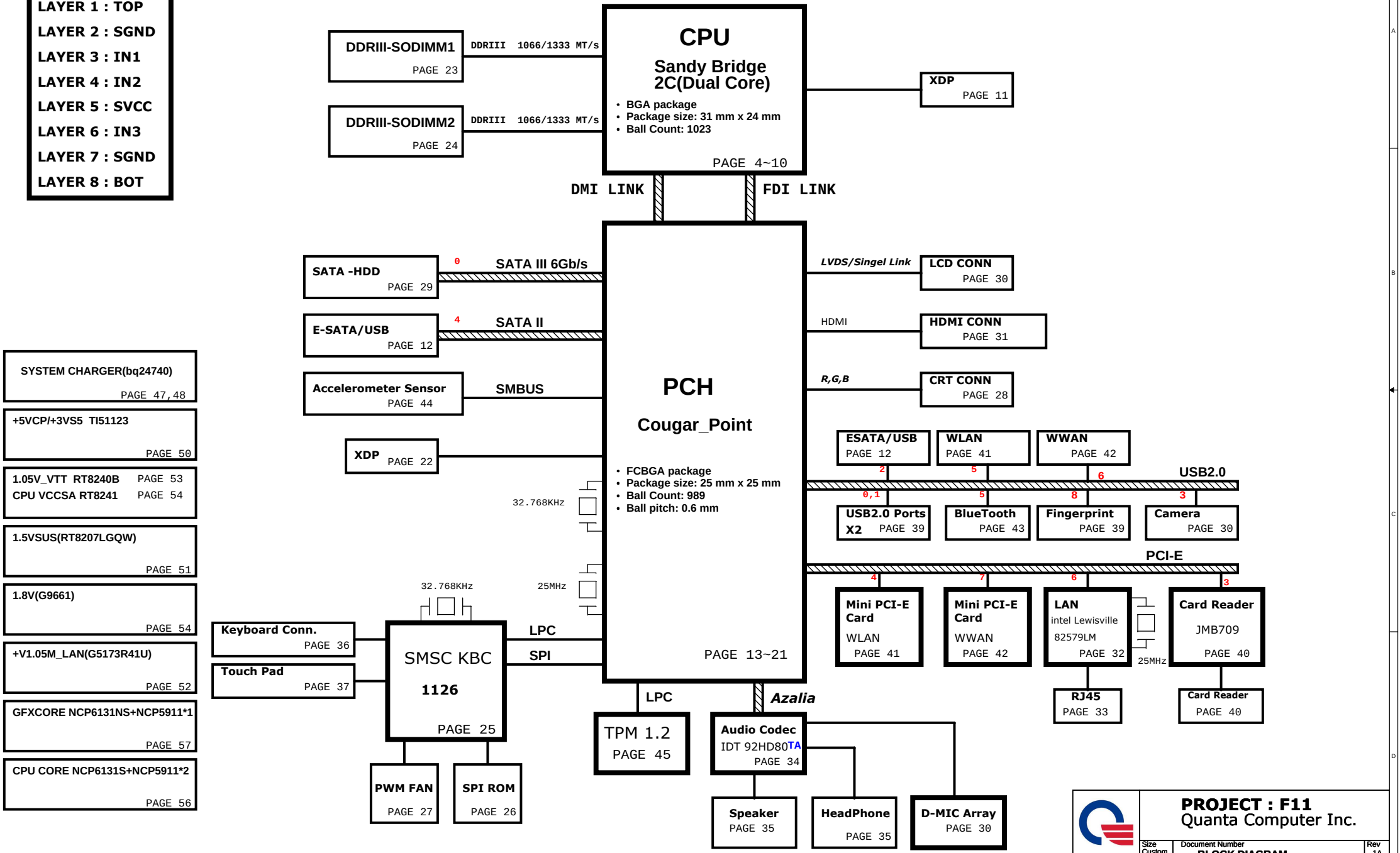
F11, Foreigner (Huron River) BLOCK DIAGRAM

01

PCB STACK UP
8L UMA. PV

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : SVCC
- LAYER 6 : IN3
- LAYER 7 : SGND
- LAYER 8 : BOT



- SYSTEM CHARGER(bq24740) PAGE 47,48
- +5VCP/+3VS5 TI51123 PAGE 50
- 1.05V_VTT RT8240B PAGE 53
  CPU VCCSA RT8241 PAGE 54
- 1.5VSUS(RT8207LGQW) PAGE 51
- 1.8V(G9661) PAGE 54
- +V1.05M_LAN(G5173R41U) PAGE 52
- GFXCORE NCP6131NS+NCP5911*1 PAGE 57
- CPU CORE NCP6131S+NCP5911*2 PAGE 56

PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Wednesday, January 19, 2011 | Sheet 1 of 58

power / State	+RTC_CELL	+VIN +3VPCU	+3VS5 +5VS5	+5VSUS +1.5VSUS	+5V +3V +1.8V_GFX +1.8V +1.5V +1.5V_CPU +1.1V_VTT +1.05V +1.0V_GFX +VGA_CORE +VCORE
S0	ON	ON	ON	ON	ON
S1	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
S4/S5 AC	ON	ON	ON	OFF	OFF
S4/S5 DC Only	ON	ON	OFF	OFF	OFF
AC/DC No Exist	ON	OFF	OFF	OFF	OFF

PCIE	Foreigner
1	X
2	X
3	JMB709
4	WLAN
5	X
6	NIC
7	WWAN
8	X

SATA	Foreigner
0	HDD
1	X
2	X
3	X
4	eSATA
5	X

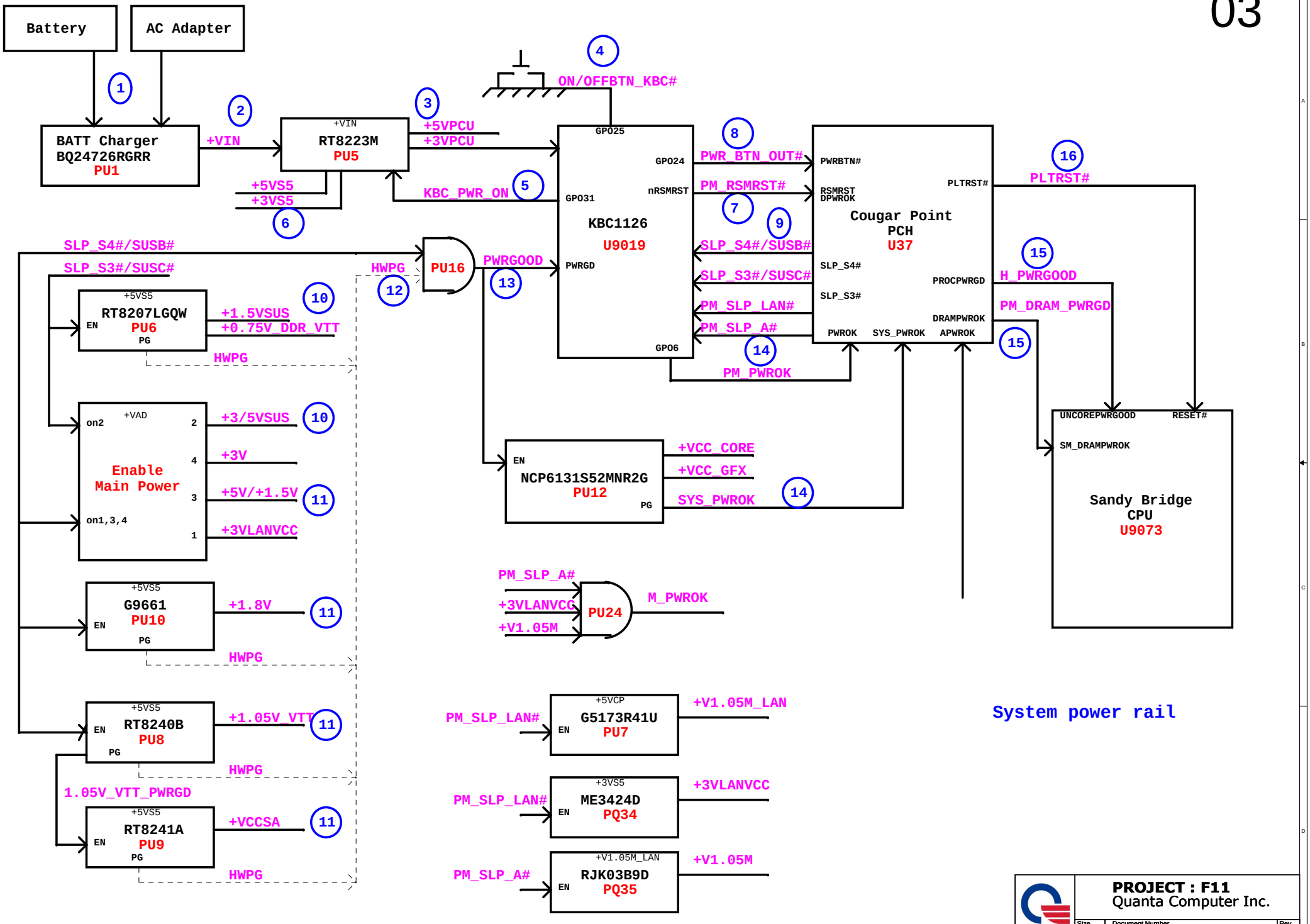
USB	Foreigner
0	CONN(USB Charger)
1	CONN
2	eSATA
3	CAMERA
4	X
5	BT or WLAN
6	X
7	X
8	Finger print
9	WWAN
10	X
11	X
12	X
13	X

	SOURCE	BATTERY 0x16	CLK GEN 0xD2	Thermal IC 0x98(Write) / 0x99(Read)	G-SENSOR 0x3A(Write) /0x3B(Read)	WLAN	SO-DIMM DIMM0: 0xA0 DIMM1: 0xA4	SMSC 1126	Intel Lan Gbe PHY:0x64 Gbe MAC:0x70
SMB_PCH_CLK SMB_PCH_DAT	PCH	X	Y	Y	Y	Y	Y	X	X
SMB_ME0_CLK SMB_ME0_DAT	PCH	X	X	X	X	X	X	Y	Y
AB1A_CLK AB1A_DATA	SMSC 1126	Y	X	X	X	X	X	X	X

PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	power rails	1A

Date: Wednesday, January 19, 2011 | Sheet 2 of 58



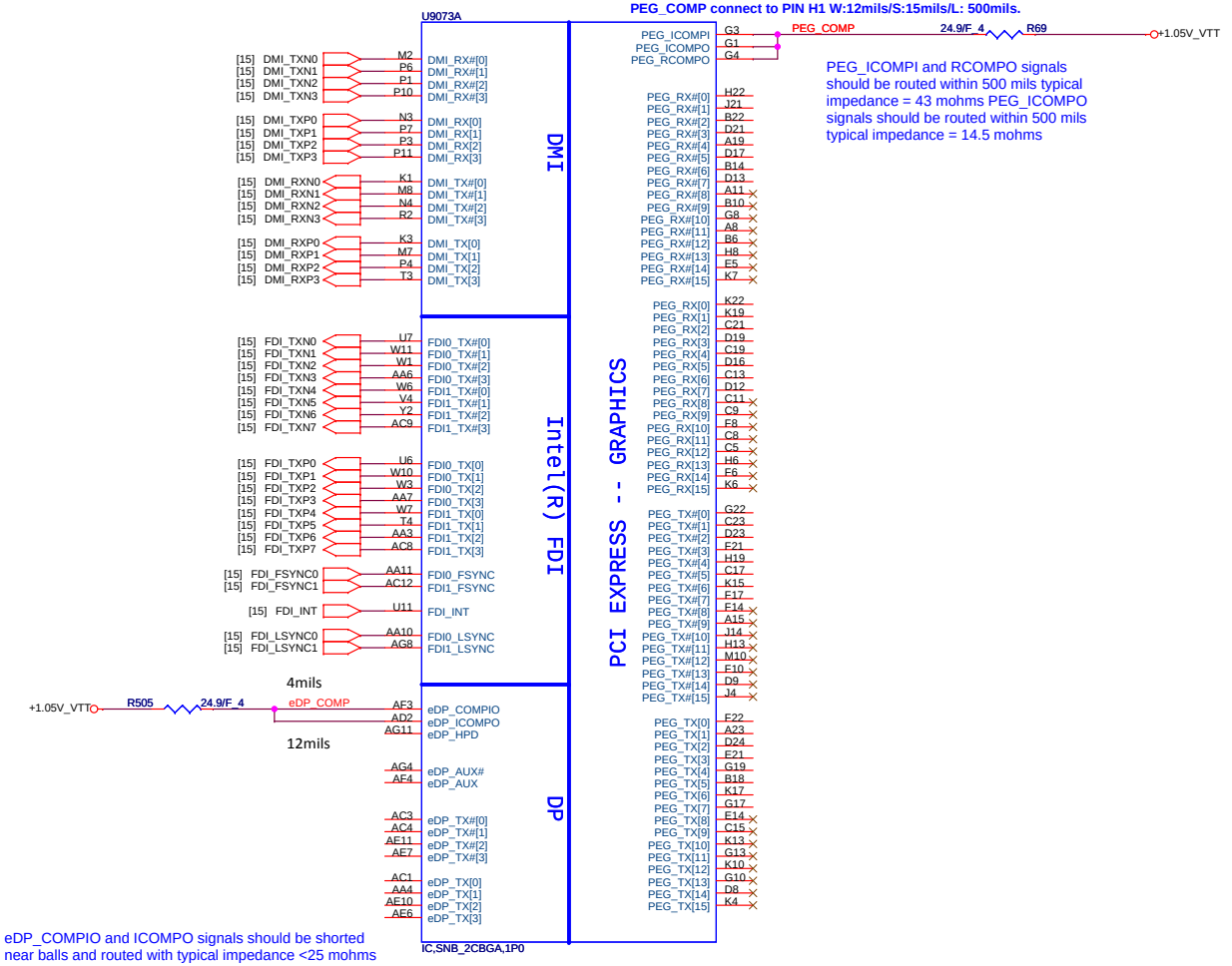
PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Power sequence	1A

Date: Wednesday, January 19, 2011 | Sheet 3 of 58

Sandy Bridge Processor (DMI,PEG,FDI)

PEG_COMP connect to PIN G2&F3 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN H1 W:12mils/S:15mils/L: 500mils.



PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 1/7 (DMI/PEG/FDI)	1A

Date: Wednesday, January 19, 2011 | Sheet 4 of 58

HP requirement
SI build,20101110

[25,48] OCP_PWM_OUT
[25] KBC_PROCHOT
D16 *RB751V-40
D17 RB751V-40
R31 *0_4
R7007 100K/F_4

Q4 2N7002W_SC70
[56] H_PROCHOT#
H_PROCHOT#
R142 56.2/F_4 H_PROCHOT#_R
C270 47P/50V_4
[27] THRMTRIP_CPU#
THRMTRIP_CPU#

SNB_IVB# N.A at SNB EDS #27637 0.7v1

[13] H_SNB_IVB#
TP32 SKTOCC#
TP33 TP_CATERR#
Placement close to EC.
[18,25] H_PECI
H_PECI

08/10

U9073B

MISC	F49 PROC_SELECT#		
	C57 PROC_DETECT#		
THERMAL	C49 CATERR#		
	A48 PECI		
	C45 PROCHOT#		
	D45 THERMTRIP#		
PWR MANAGEMENT	C48 PM_SYNC		
	B46 UNCOREPWRGOOD		
	BE45 SM_DRAMPWROK		
	D44 RESET#		
CLOCKS		BCLK / BCLK#	J3 H2 → CLK_CPU_BCLKP [14], CLK_CPU_BCLKN [14]
		DPLL_REF_CLK / DPLL_REF_CLK#	AG3 AG1 → R37 1K/F_4, R38 1K/F_4 → +1.05V_VTT
		BCLK_ITP / BCLK_ITP#	N59 N58 → CLK_XDP_ITP_P [11], CLK_XDP_ITP_N [11]
DDR3 MISC		SM_DRAMRST#	AT30 CPU_DRAMRST#
		SM_RCOMP[0] / SM_RCOMP[1] / SM_RCOMP[2]	BE44 BE43 BG43 → SM_RCOMP_0 R155 140/F_4, SM_RCOMP_1 R506 25.5/F_4, SM_RCOMP_2 R501 200/F_4
JTAG & BPM		PRDY# / PREQ#	N53 XDP_PRDY#_R, N55 XDP_PREQ#_R
		TCK / TMS / TRST#	L56 XDP_TCLK_R, L55 XDP_TMS_R, J58 XDP_TRST#_R
		TDI / TDO	M60 XDP_TDI_R, L59 XDP_TDO_R
		DBR#	K58 XDP_DBR#_R
		BPM#[0] BPM#[1] BPM#[2] BPM#[3] BPM#[4] BPM#[5] BPM#[6] BPM#[7]	G58 XDP_BPM0_R, E55 XDP_BPM1_R, E59 XDP_BPM2_R, G55 XDP_BPM3_R, G59 XDP_BPM4_R, H60 XDP_BPM5_R, J59 XDP_BPM6_R, J61 XDP_BPM7_R

IC,SNB_2CBGA,1P0

SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils;

8/9 Modify R506

eDP set to No Staff

Processor pull-up (CPU)

+1.05V_VTT
H_PROCHOT# R187 62_4
XDP_TMS R590 51_4
XDP_TDI_R R201 51_4
XDP_PREQ# R204 *51_4
XDP_TCLK R593 51_4
XDP_TRST# R588 51_4

SM_DRAMPWROK Processor Input.

+3V HP request 8/5
R21 200/F_4
C25 0.1U/10V_4
+3VS5
+1.5V
R5 200/F_4

U9077
74LVC2G07GW
0.8~1.1
AL2G0007000
IC(6P) 74LVC2G07GW (SC-88)

[15] PM_DRAM_PWRGD
[25,30,49,56] PWR_GOOD

PV
[15] PM_SYNC
R509 *0_4/SP PM_SYNC_R
PV
[11,18] H_PWRGOOD
R515 *0_4/SP PWRGOOD_R
R516 10K/F_4

PM_DRAM_PWRGD_C
130/F_4 R18
PM_DRAM_PWRGD_R

CPU_PLTRST#_R

R14 *39_4
8/12 Add HP request
[13,15] PM_SLP_S3
Q8005 *2N7002EGP_SC70

CPU RESET#

+1.05V_VTT
R534 75/F_4
U38
74LVC1G07GW
PLTRST#
CPU_PLTRST#
R526 43_4/F CPU_PLTRST#_R
+3V
C720 0.1U/10V_4
[11,13,17,26,32,34,40,41,42,45] PLTRST#
R537 *1.5K/F_4 CPU_PLTRST#_R
R536 *750/F_4

XDP Option

Total -->Within 6"

XDP_BPM4_R / XDP_BPM7_R	RP9017 0_4P2R_4	XDP_BPM4 / XDP_BPM7	XDP_BPM4 [11], XDP_BPM7 [11]
XDP_TMS_R / XDP_TCLK_R	RP9018 0_4P2R_4	XDP_TMS / XDP_TCLK	XDP_TMS [11], XDP_TCLK [11]
XDP_BPM1_R / XDP_TDI_R	RP9019 0_4P2R_4	XDP_BPM1 / XDP_TDI	XDP_BPM1 [11], XDP_TDI [11]
XDP_BPM0_R / XDP_PREQ#_R	RP9020 0_4P2R_4	XDP_BPM0 / XDP_PREQ#	XDP_BPM0 [11], XDP_PREQ# [11]
XDP_BPM3_R / XDP_PRDY#_R	RP9021 0_4P2R_4	XDP_BPM3 / XDP_PRDY#	XDP_BPM3 [11], XDP_PRDY# [11]
XDP_TRST#_R / XDP_BPM2_R	RP9022 0_4P2R_4	XDP_TRST# / XDP_BPM2	XDP_TRST# [11], XDP_BPM2 [11]
XDP_BPM5_R / XDP_BPM6_R	RP9023 0_4P2R_4	XDP_BPM5 / XDP_BPM6	XDP_BPM5 [11], XDP_BPM6 [11]
XDP_TDO_R	R10290 0_4	XDP_TDO	XDP_TDO [11]
XDP_DBR#_R	R10291 0_4	XDP_DBRST#	XDP_DBRST# [11,15,22]

Remove from MV

DDR3 DRAM RESET

+1.5VSUS
R35 1K/F_4
R30 *0_4
Q9012 2N7002W_SC70
[23,24] DDR3_DRAMRST#
R34 1K/F_4
CPU_DRAMRST#
CPU_DRAMRST#_R
8/4
[9,14] PCH_DDR_RST#
C27 0.047U/10V_4
R25 4.99K/F_4

PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 2/7 (CLK/MISC/JTAG)	1A

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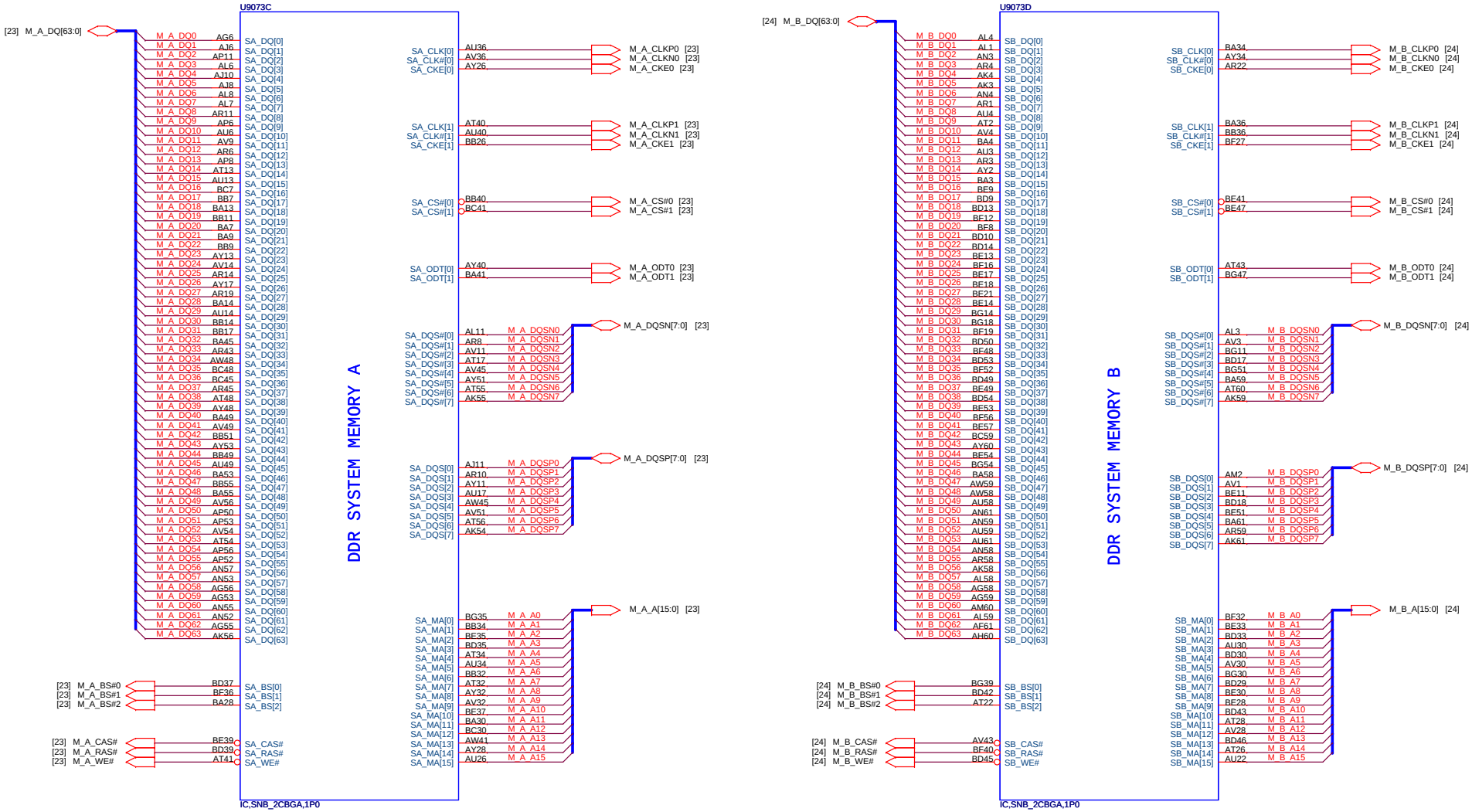
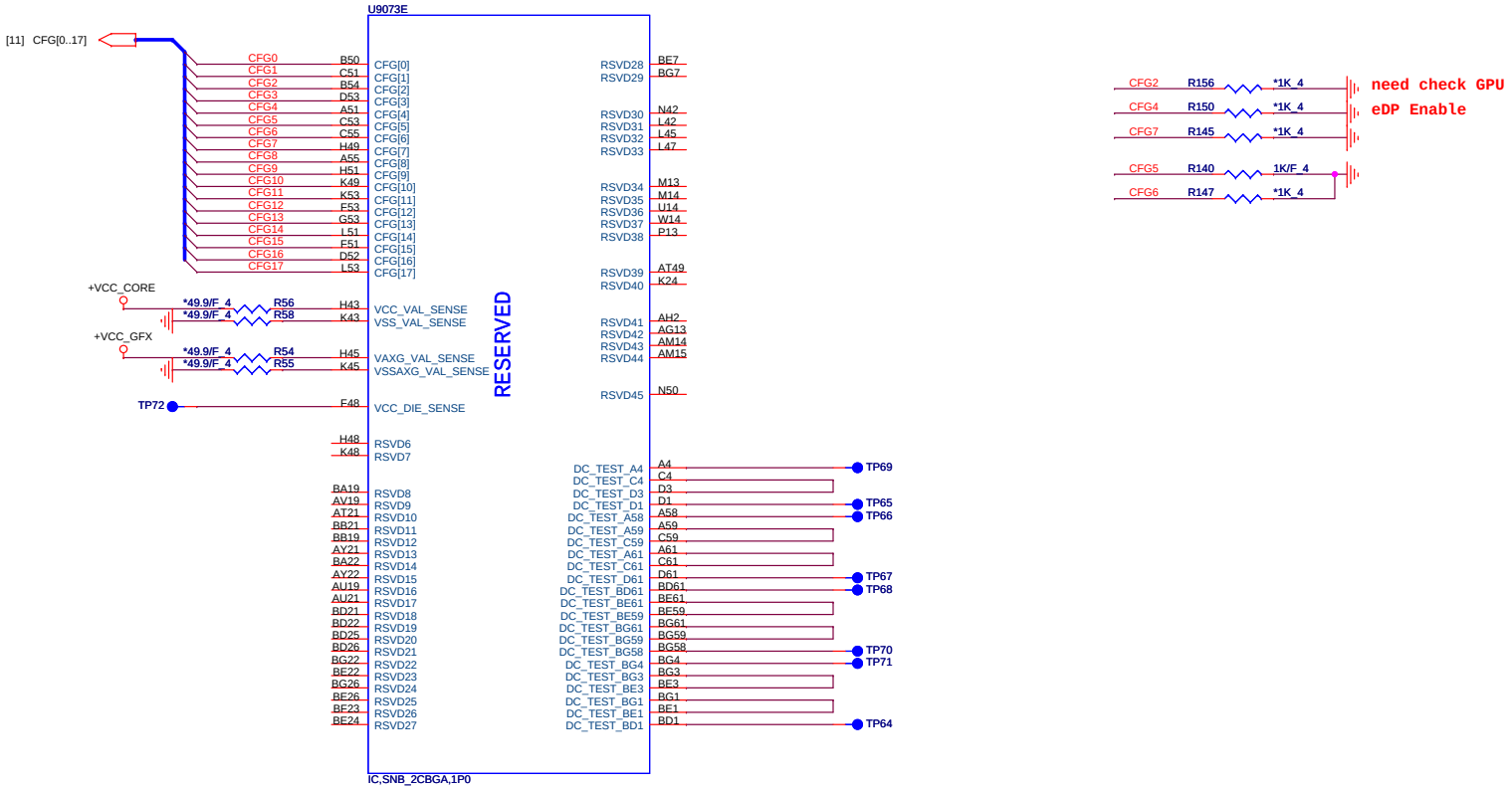
Sandy Bridge Processor (DDR3)



PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 3/7 (DDR3 I/F)	1A

Date: Wednesday, January 19, 2011 | Sheet 6 of 58



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 4/7 (CFG/RSVD)	1A

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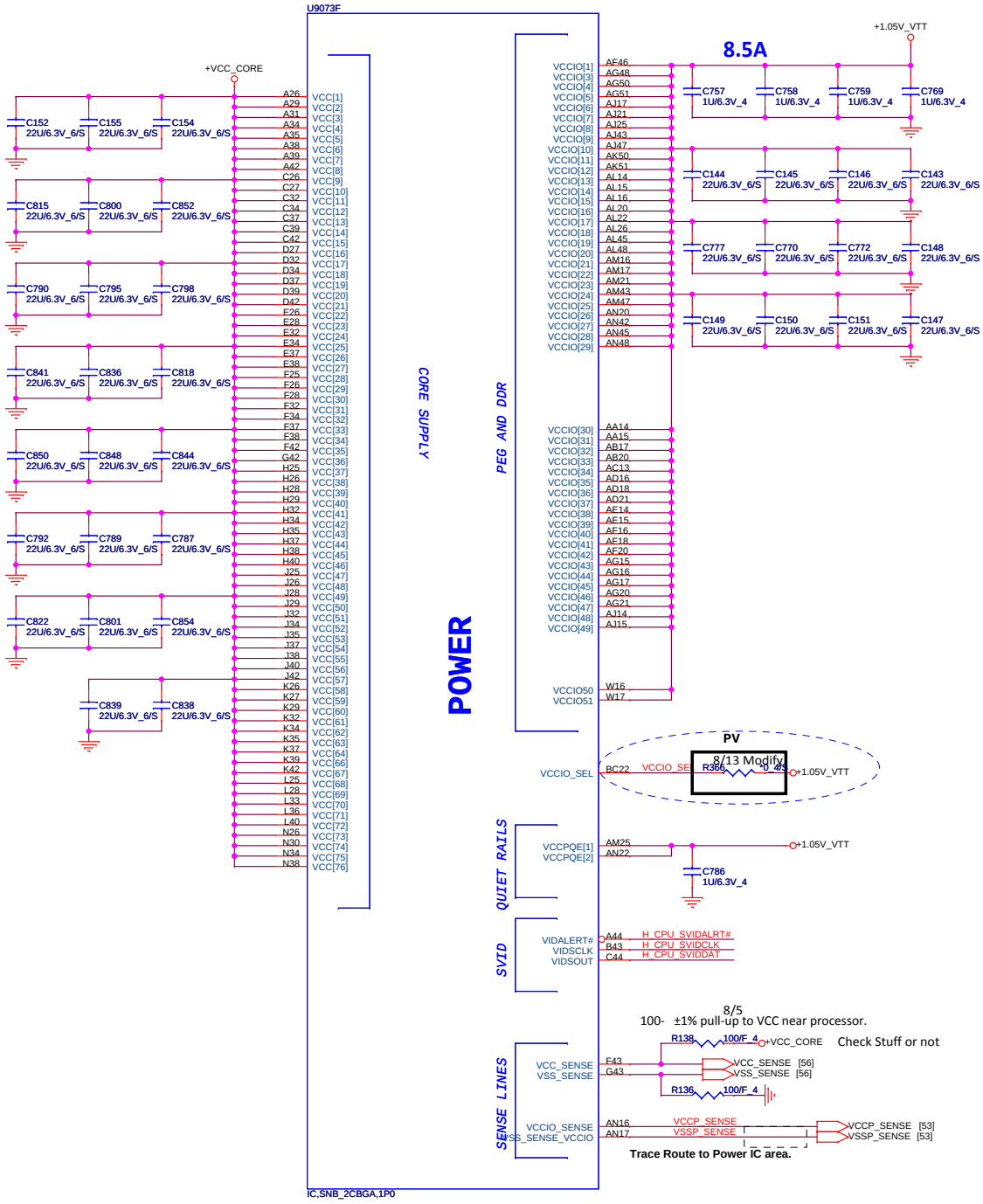
22uf *23

330uf *4



22uf *12

1uf*4

330uf *2

8/3

SVID CLK

Set to no-stuff

Place PU resistor close to VR

R121 +54.9/F_4 +1.05V_VTT

H_CPU_SVIDCLK

VR_SVID_CLK [56]

SVID ALERT

R98 75/F_4 +1.05V_VTT

Place PU resistor close to CPU

H_CPU_SVIDALRT# R91 43_4/F

VR_SVID_ALERT# [56]

SVID DATA

Place PU resistor close to CPU

R109 130/F_4 +1.05V_VTT

H_CPU_SVIDDAT

VR_SVID_DATA [56]

PROJECT : F11

Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 5/7 (POWER1)	1A

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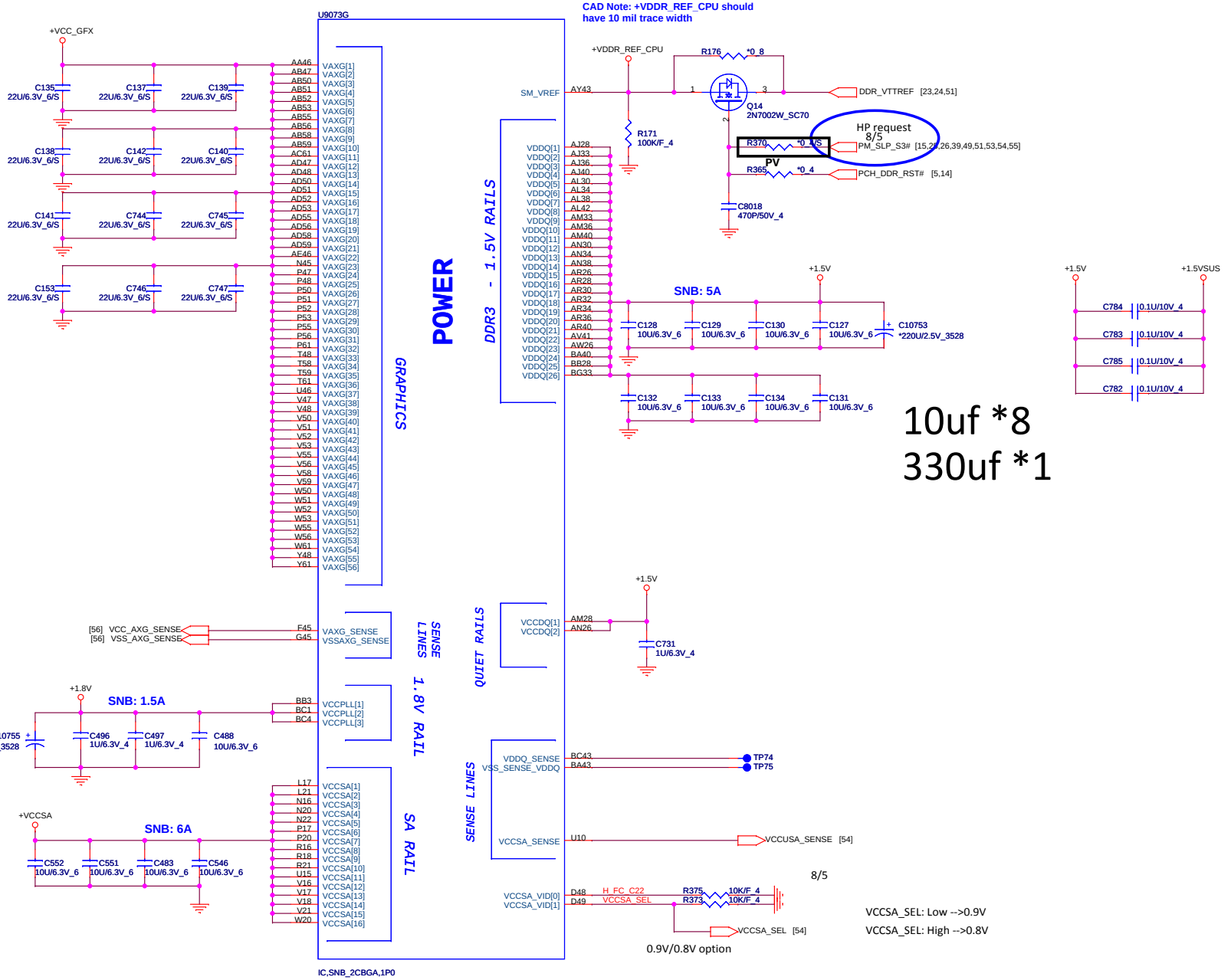
22uf *12

330uf *3



10uf *8

330uf *1

10uf *1

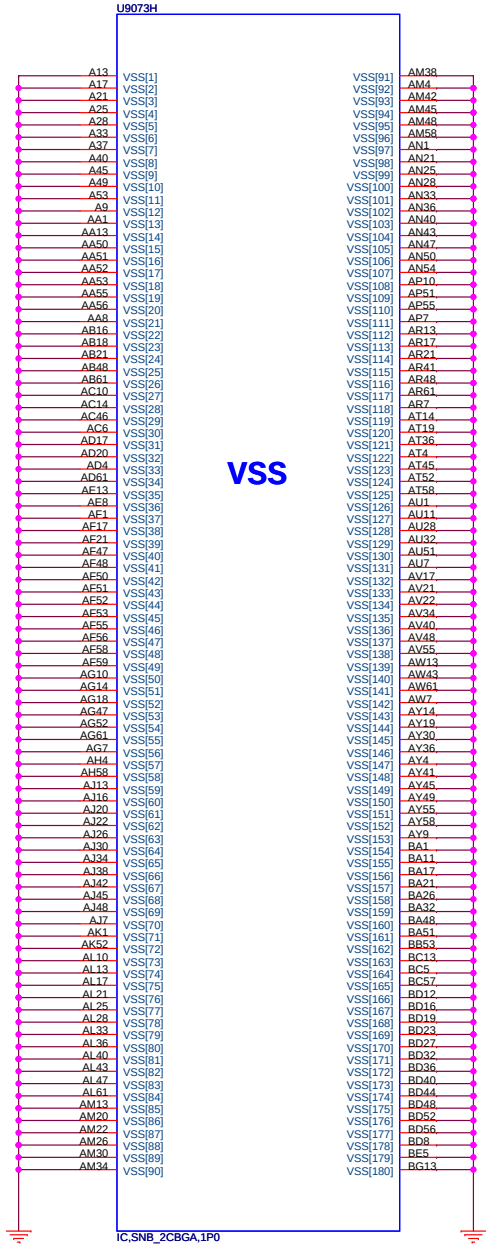
1uf *2

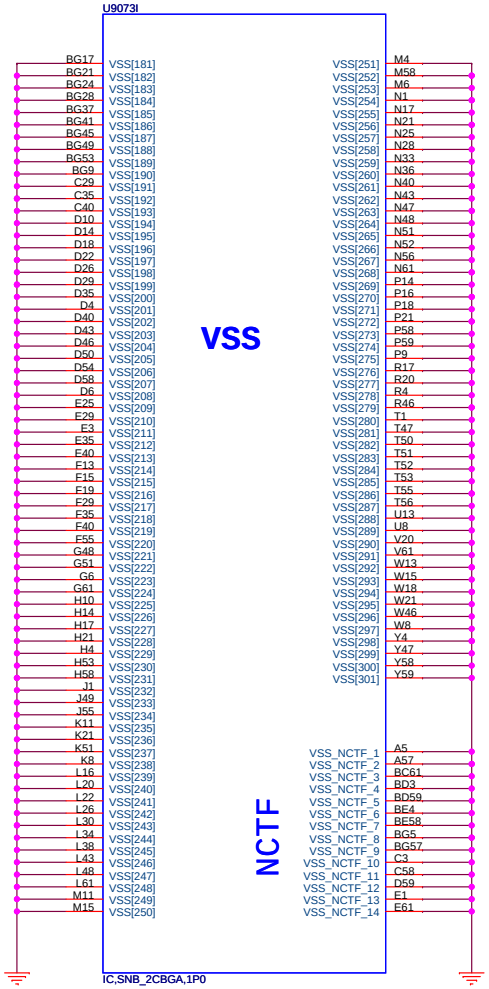
330uf *1

10uf *4

330uf *1

PROJECT : F11 Quanta Computer Inc.		
Size: Custom	Document Number: SNB 6/7 (POWER2)	Rev: 1A
Date: Wednesday, January 19, 2011	Sheet 9 of 58	





PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 7/7 (GND)	1A

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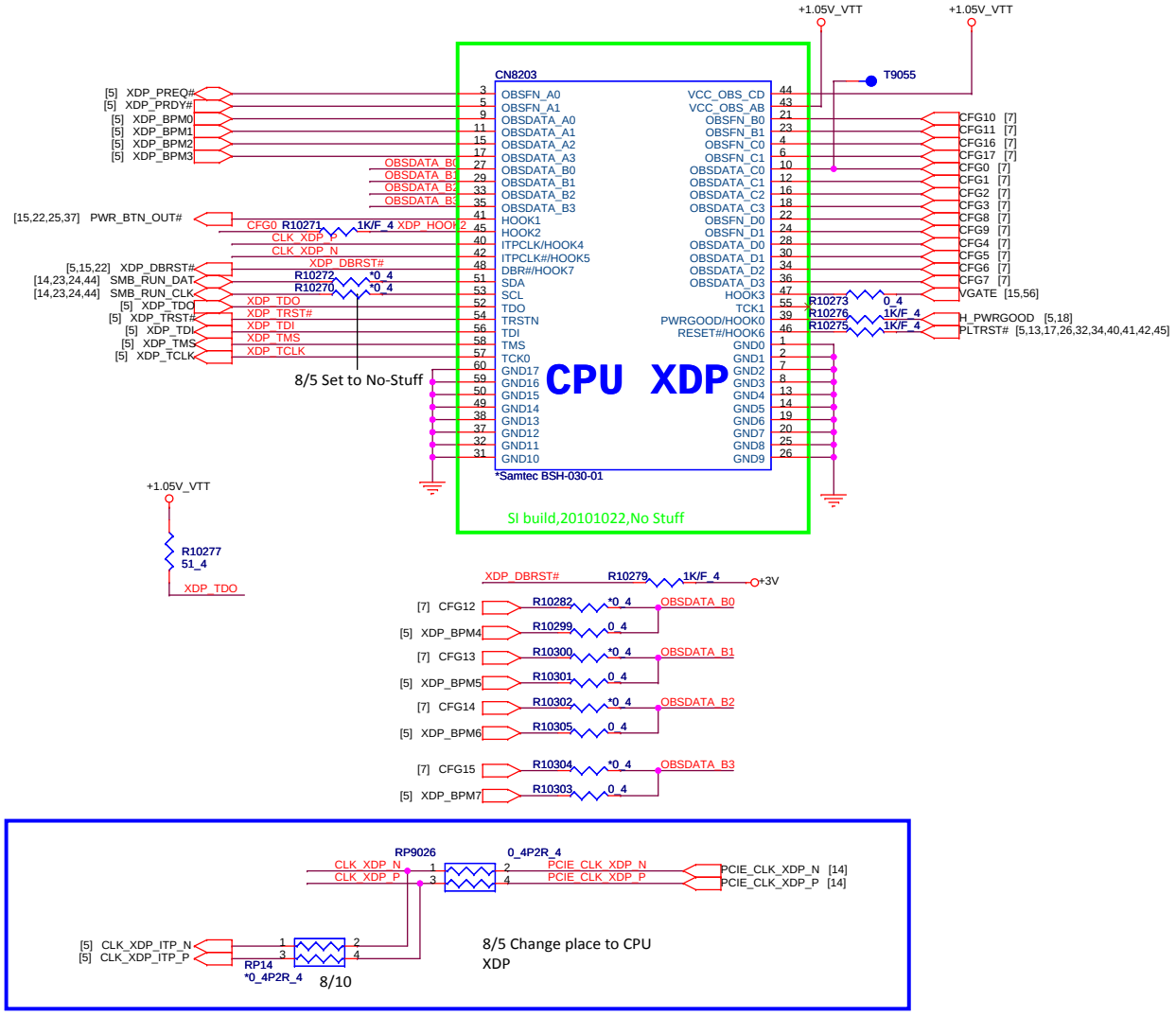
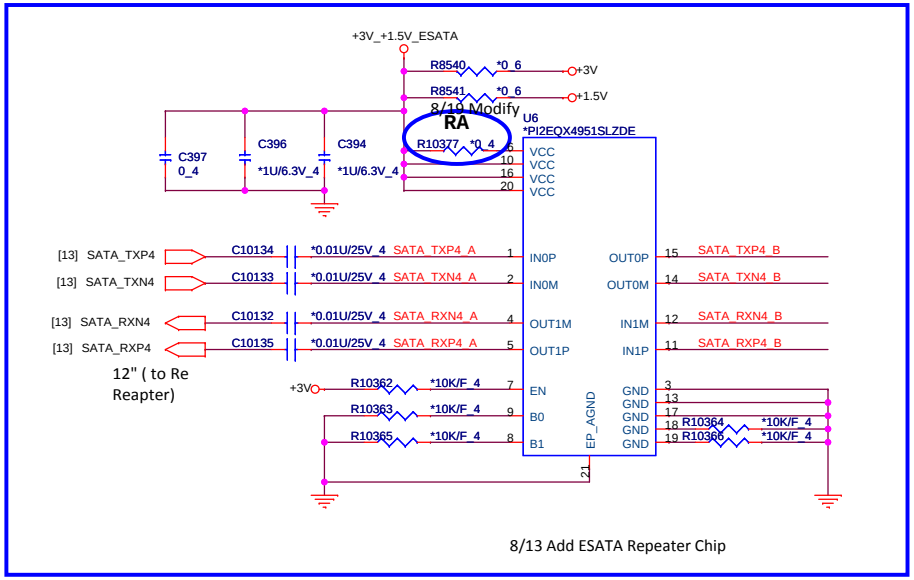
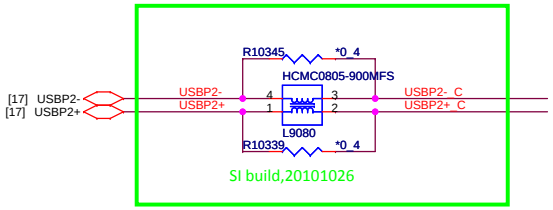


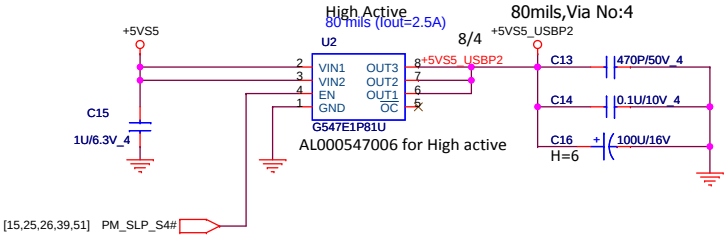
PROJECT : F11	
Quanta Computer Inc.	
Size: Custom	Document Number: CPU XDP
Rev: 1A	
Date: Wednesday, January 19, 2011	Sheet 11 of 58

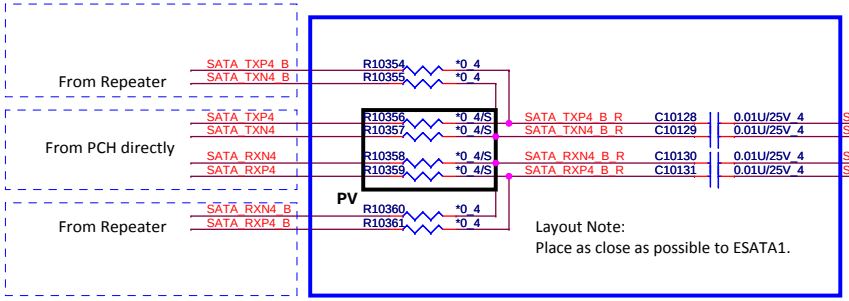
Signals		2EQX4951SL	3EQX4951ST
U6#6	RA	0 ohm	NC

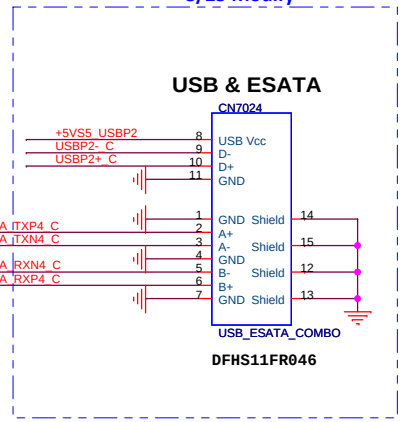




Standard USB







PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ESATA CONN/Repeater	1A

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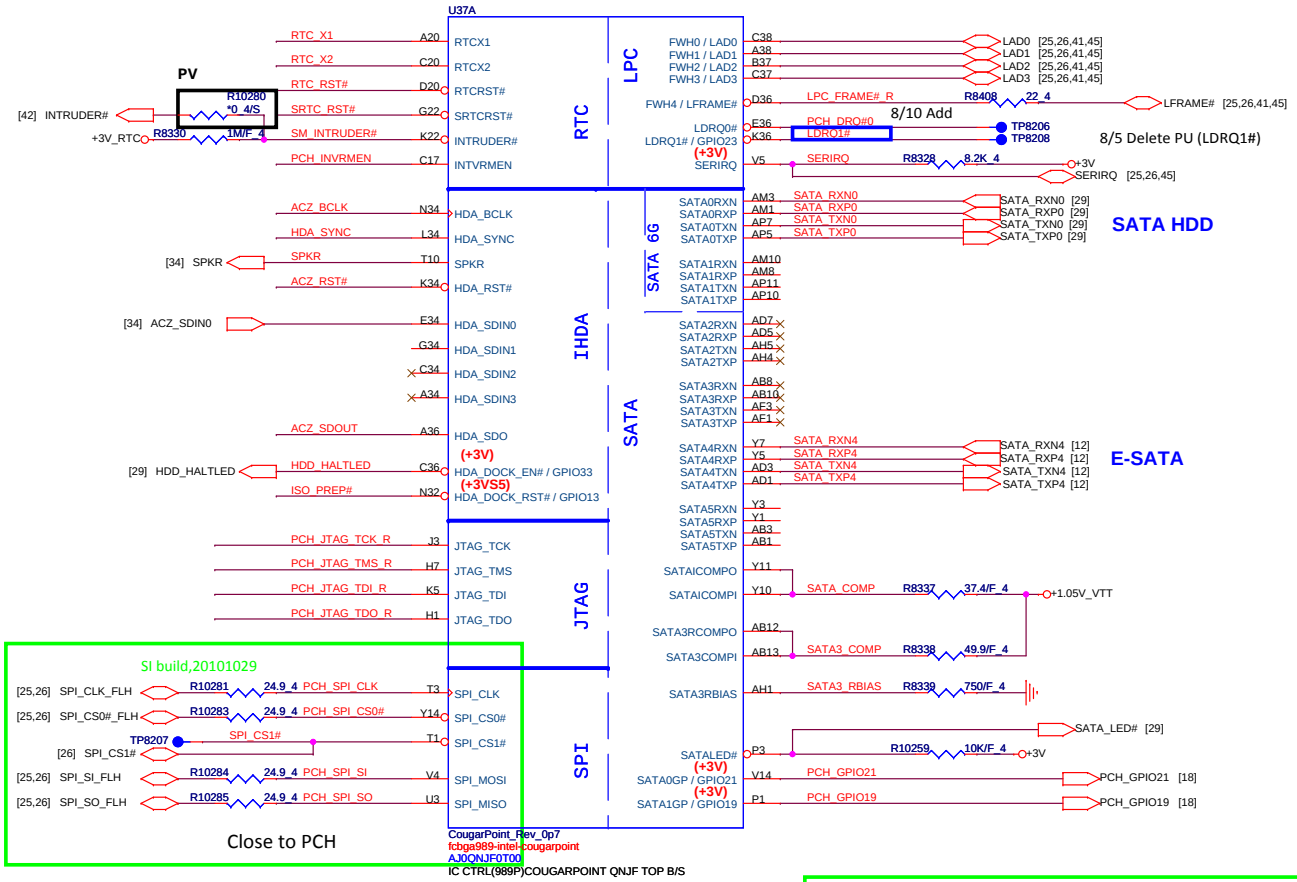
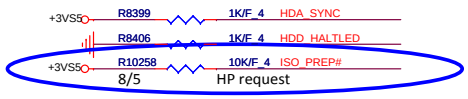
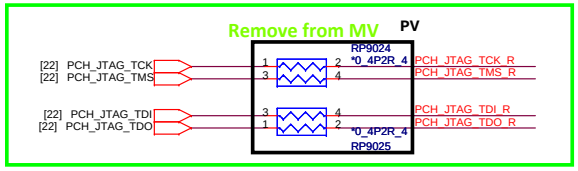
Cougar Point (HDA,JTAG,SATA)



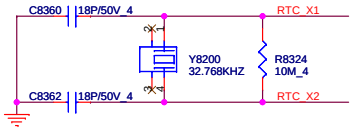




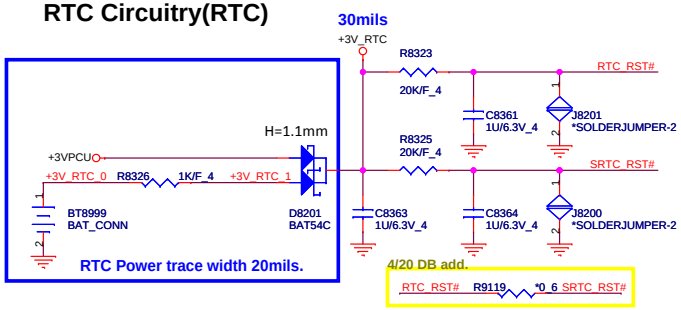
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR Different from Calpella	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R8349 *1K_4 +3V
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R8351 330K/F_4 +3V_RTC
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R8359 *1K_4 NV_ALE [17]
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R8360 2.2K_4 R8361 4.7K/F_4 NV_CLE [17] H_SNB_IVB# [5] N.A at CPT EDS 0.7
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	SPI_SI_FLH R8398 *1K/F_4 +3V

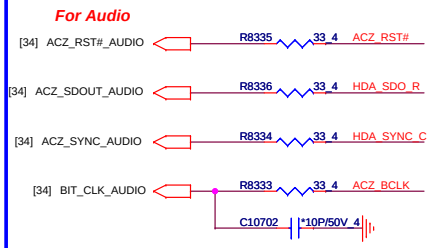
RTC Clock 32.768KHz



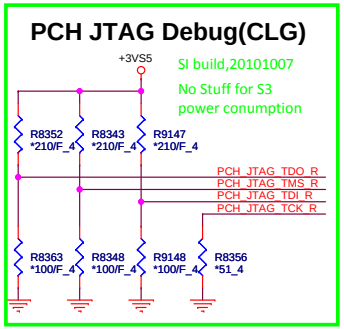
RTC Circuitry(RTC)

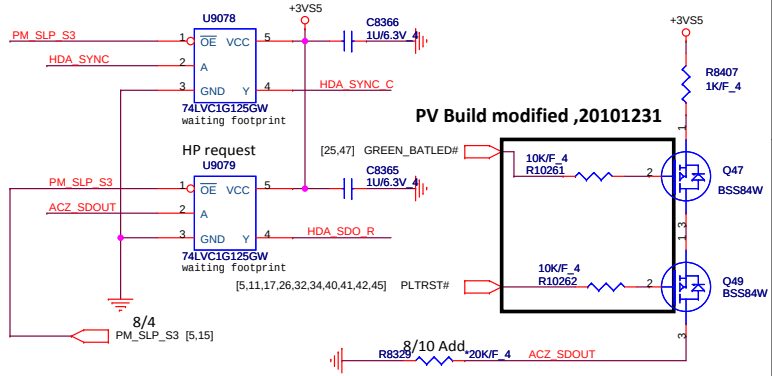


HDA Bus(CLG)



PCH JTAG Debug(CLG)





PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/9 (SATA/HDA/SPI)	1A

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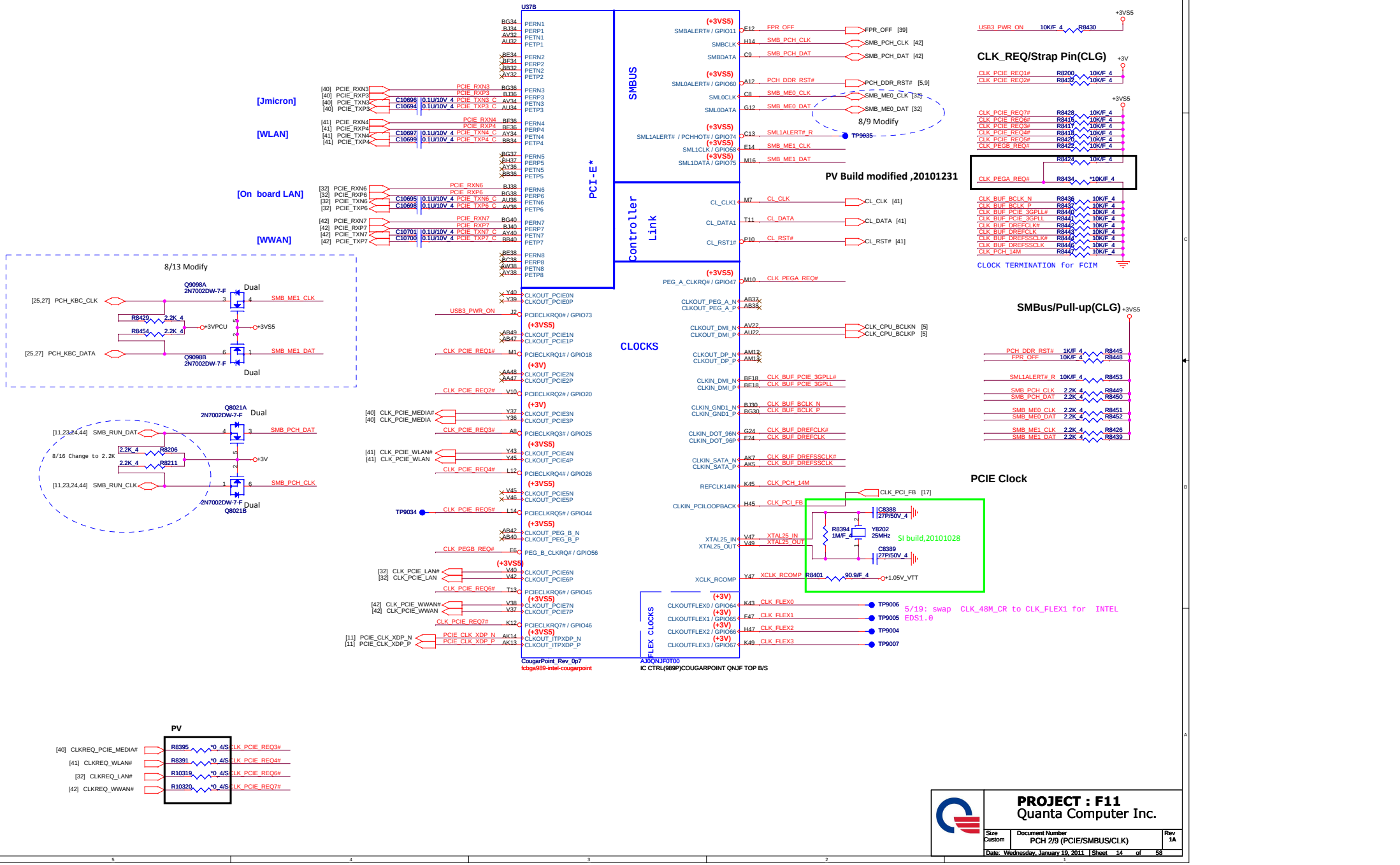
Cougar Point-M (PCI-E,SMBUS,CLK)

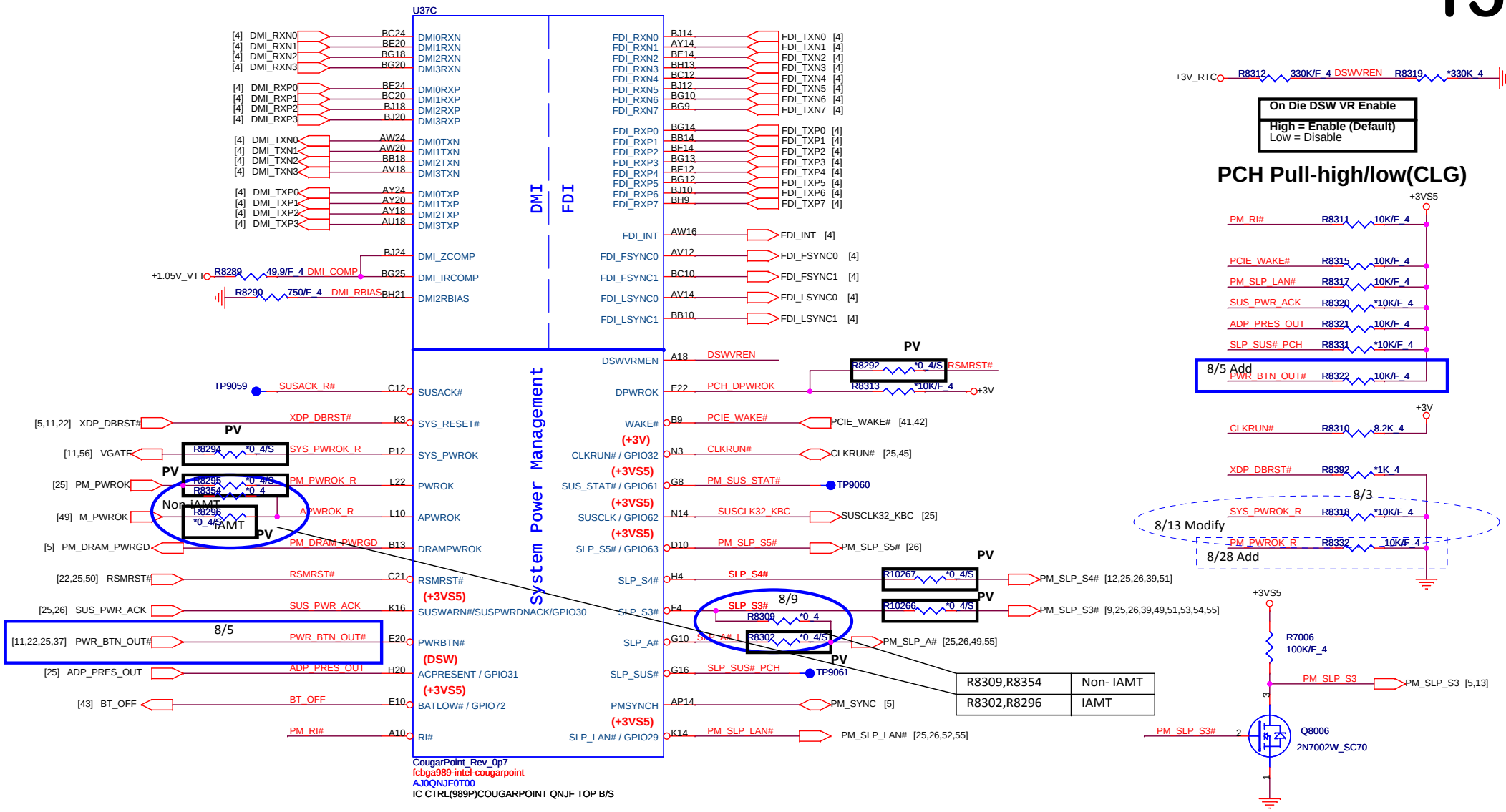


PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/9 (PCIE/SMBUS/CLK)	1A

Date: Wednesday, January 19, 2011 | Sheet 14 of 58

Cougar Point (DMI,FDI,PM)

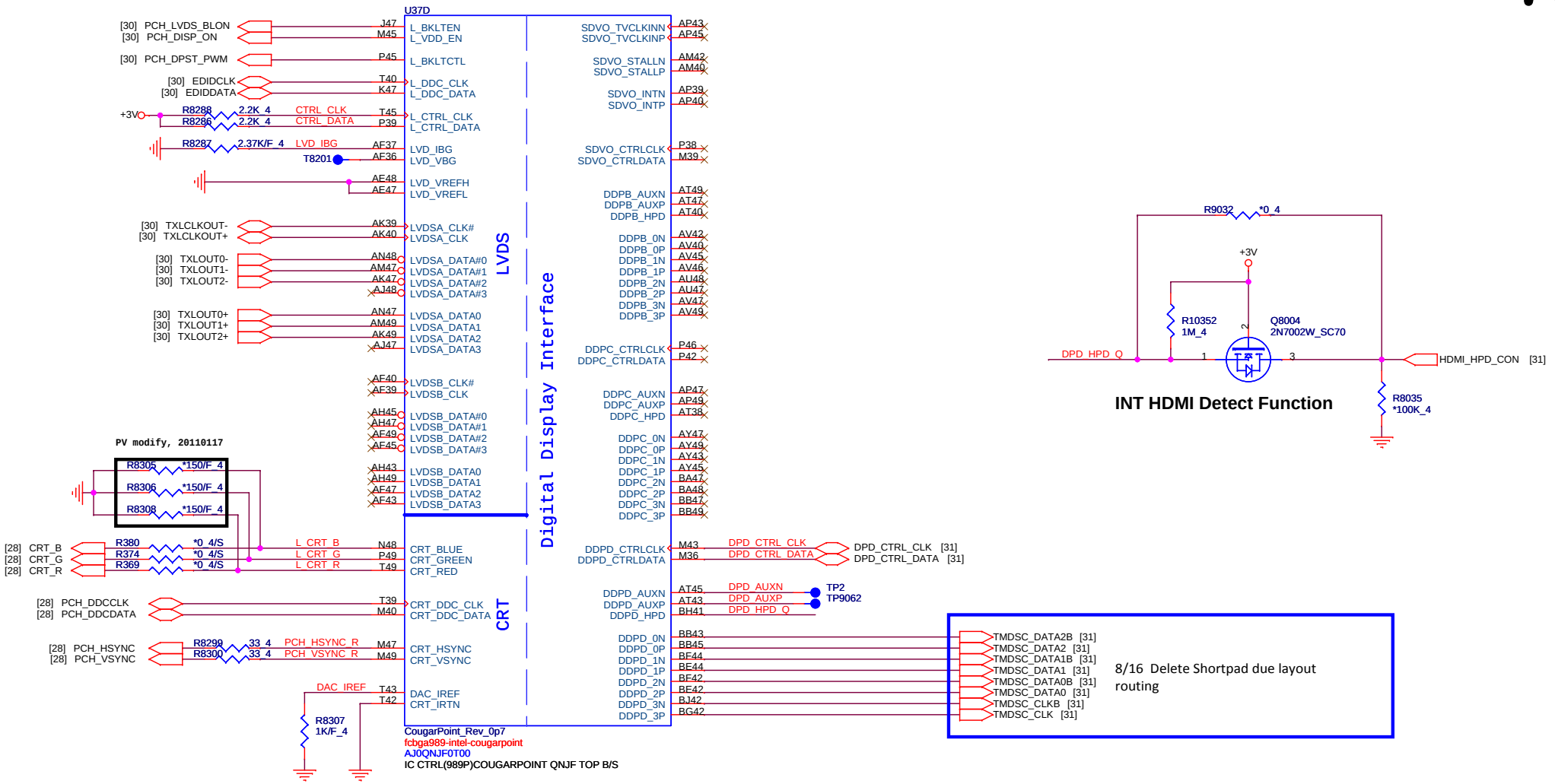


PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
B	PCH 3/9 (DMI/FDI/PM)	1A

Date: Wednesday, January 19, 2011 Sheet 15 of 58

Cougar Point (LVDS,DDI)



INT HDMI Detect Function

PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
B	PCH 4/9 (LVDS/DDP/CRT)	1A

Date: Wednesday, January 19, 2011 Sheet 16 of 58

Cougar Point-M (PCI,USB,NVRAM)

U37E

RSVD

NVRAM

PCI

USB

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJ0QNJF0T00
IC CTRL(989P)COUGARPOINT QNJF TOP B/S

SI build,20101007 Remove Gate

PLTRST#(CLG)

+3VS5 C8390 *0.1U/10V_4

PCI_PLTRST# → U8208 *TC7SH08FU → PLTRST#

R8427 100K/F_4

R9023 *0_4/S

PLTRST# [5,11,13,26,32,34,40,41,42,45]

PV

PCI/USBOC# Pull-up(CLG)

+3V R8412 8.2KX4

PCI_PIRQC#
PCI_PIRQB#
PCI_PIRQA#
PCI_PIRQD#

+3VS5 R8551 10K_10P8R_6

USB_OC4#
USB_OC1#
USB_OC2#
USB_OC3#
USB3_VBUS_ON
CPPE#_R
USB_OC5#

+3V R8552 10K_10P8R_6

GPIO52
ACCEL_INT
GPIO55
USB30_SMI#
GPIO54
SATA_ODD_DA#
GPIO50
NMI_SMI_DBG#

PV

8/10 LANLINK_STATUS_R R10260 *0_4/S LANLINK_STATUS [32]

8/12 LANLINK_STATUS 10K/F_4 R8425 +3VS5

8/16 GPIO51 10K/F_4 R8419 +3V

CAMERA_ON 10K/F_4 R8423

PV modify, 20110117

WLAN/BT Option

RP9027 *0_4P2R_4

USBP5- USB_PN5_C [41]
USBP5+ USB_PP5_C [41]

8/3

USB_BIAS R8388 22.6/F_4

8/12 Change R10265 to 0402

USB3_VBUS_ON_R [18] R10265 *0_4/S USB3_VBUS_ON

PV

[30] CAMERA_ON

[25,26] NMI_SMI_DBG#
[44] ACCEL_INT

+3VS5 R8438 *10K/F_4 PCI_PME#

[25] CLK_PCI_KBC
[14] CLK_PCI_FB
[45] CLK_PCI_TPM
[26,41] CLK_33M_DEBUG

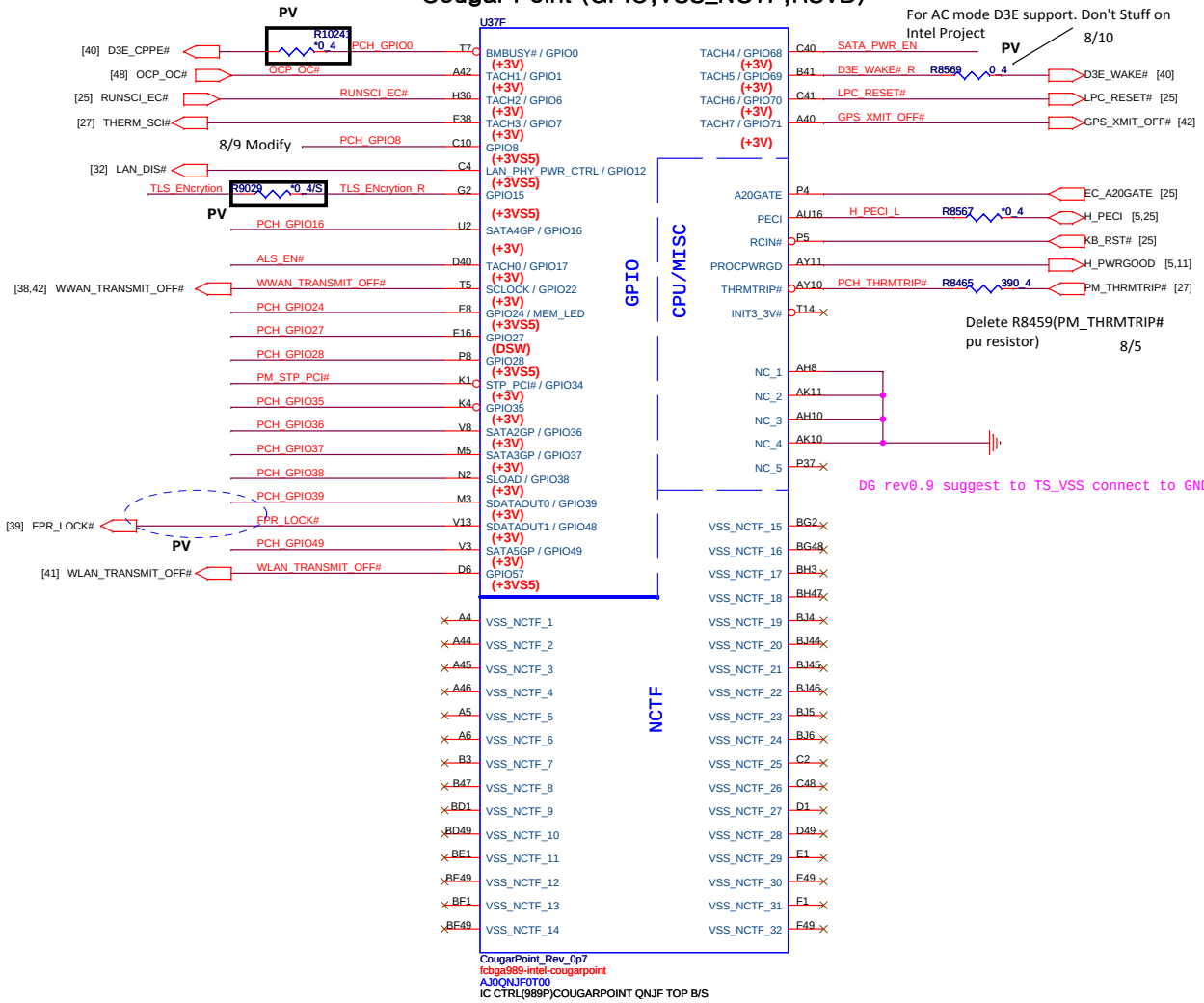
TP8219

R8403 22_4 CLK_33M_KBPCI_R
R8402 22_4 CLK_PCI_FB_R
R8405 22_4 CLK_PCI_TPM_R
R8404 22_4 CLK_33M_DEBUG_R

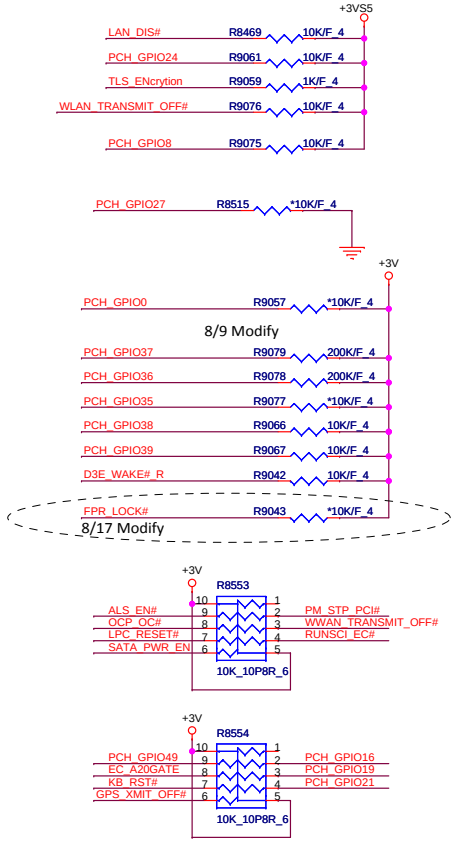
CLK_PCI_FB

Project	
PROJECT : F11	Quanta Computer Inc.
Size: B	Document Number: PCH 5/9 (PCI/USB/NVM)
Rev: 1A	
Date: Wednesday, January 19, 2011	Sheet 17 of 58

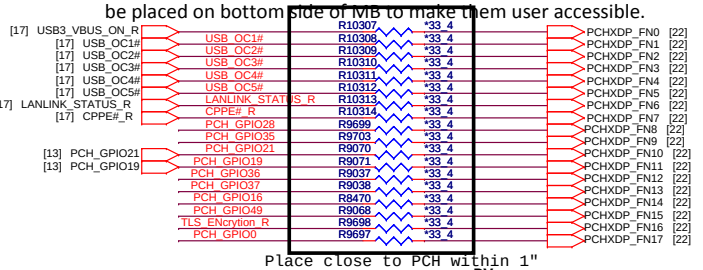
Cougar Point (GPIO,VSS_NCTF,RSVD)



GPIO Pull-up/Pull-down(CLG)



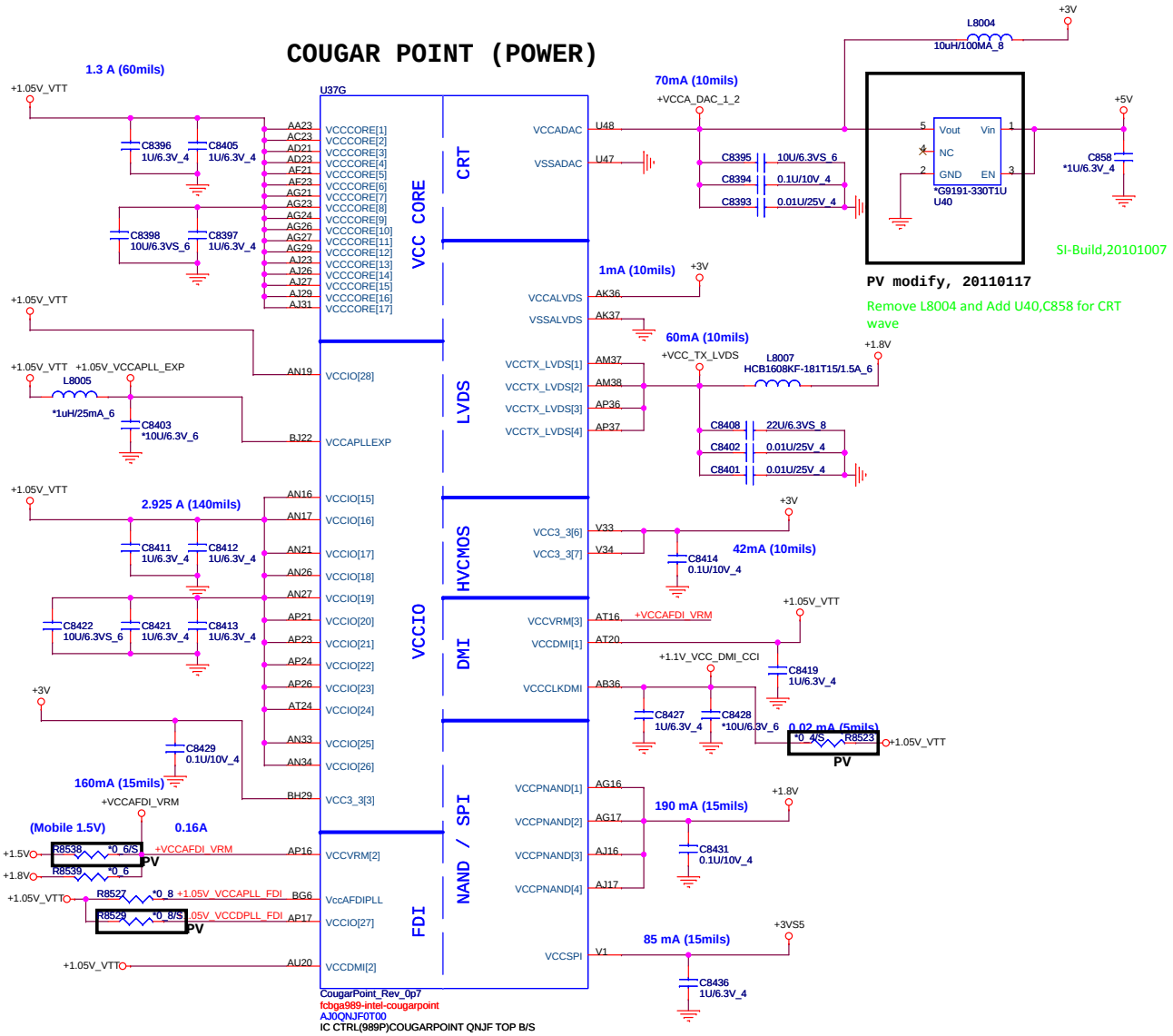
Layout note: 33 and 0 ohm related to XDP connector should be placed
in close proximity to each other. In additon, these should be placed on bottom side of MB to make them user accessible.



PROJECT : F11
Quanta Computer Inc.

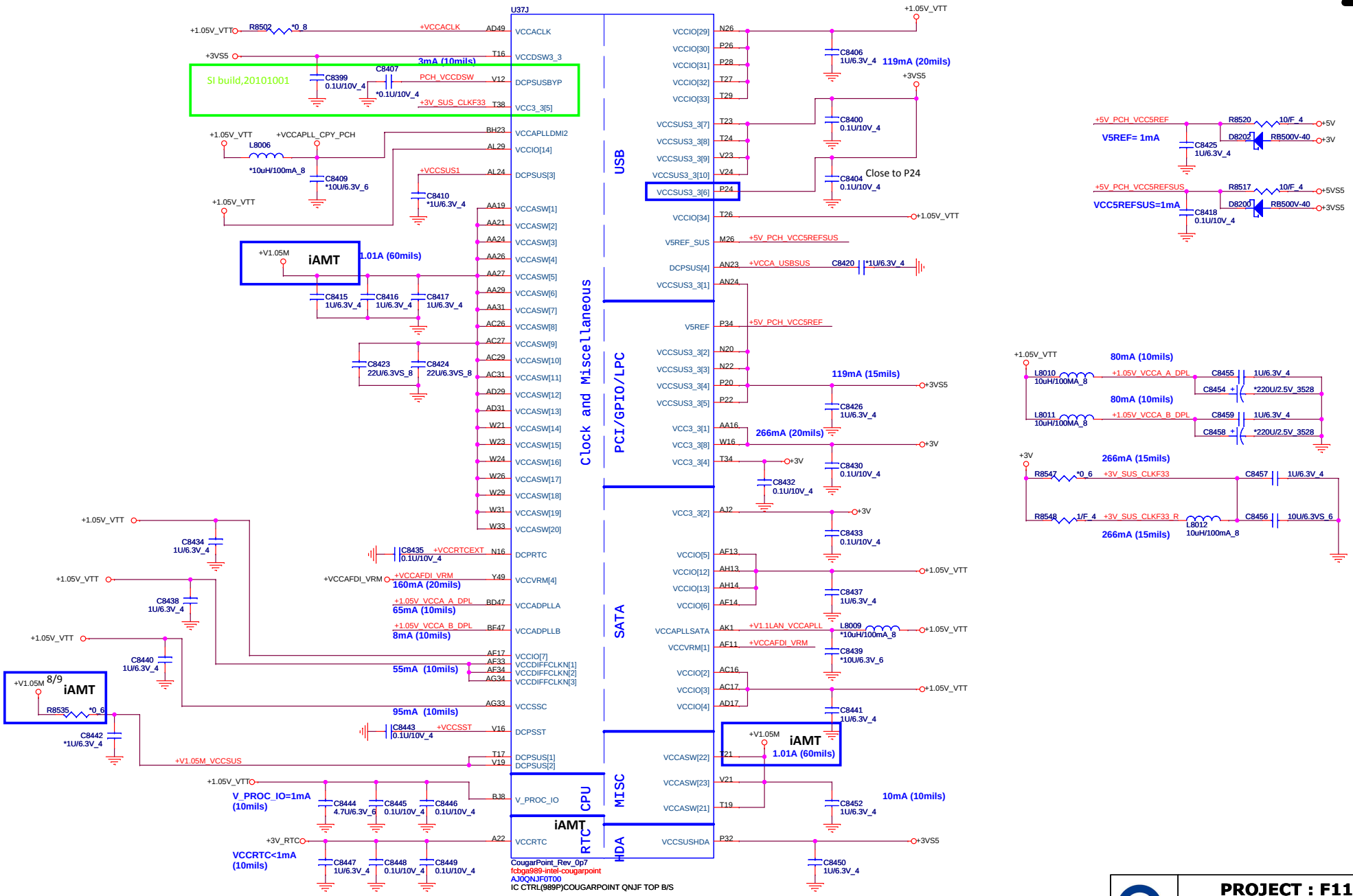
Size	Document Number	Rev
Custom	PCH 6/9 (GPIO/NTCF/RSVD)	1A
Date: Wednesday, January 19, 2011	Sheet 18 of 58	

COUGAR POINT (POWER)



PROJECT : F11 Quanta Computer Inc.		
Size: Custom	Document Number: PCH 7/9 (POWER1)	Rev: 1A
Date: Wednesday, January 19, 2011	Sheet 19 of 58	

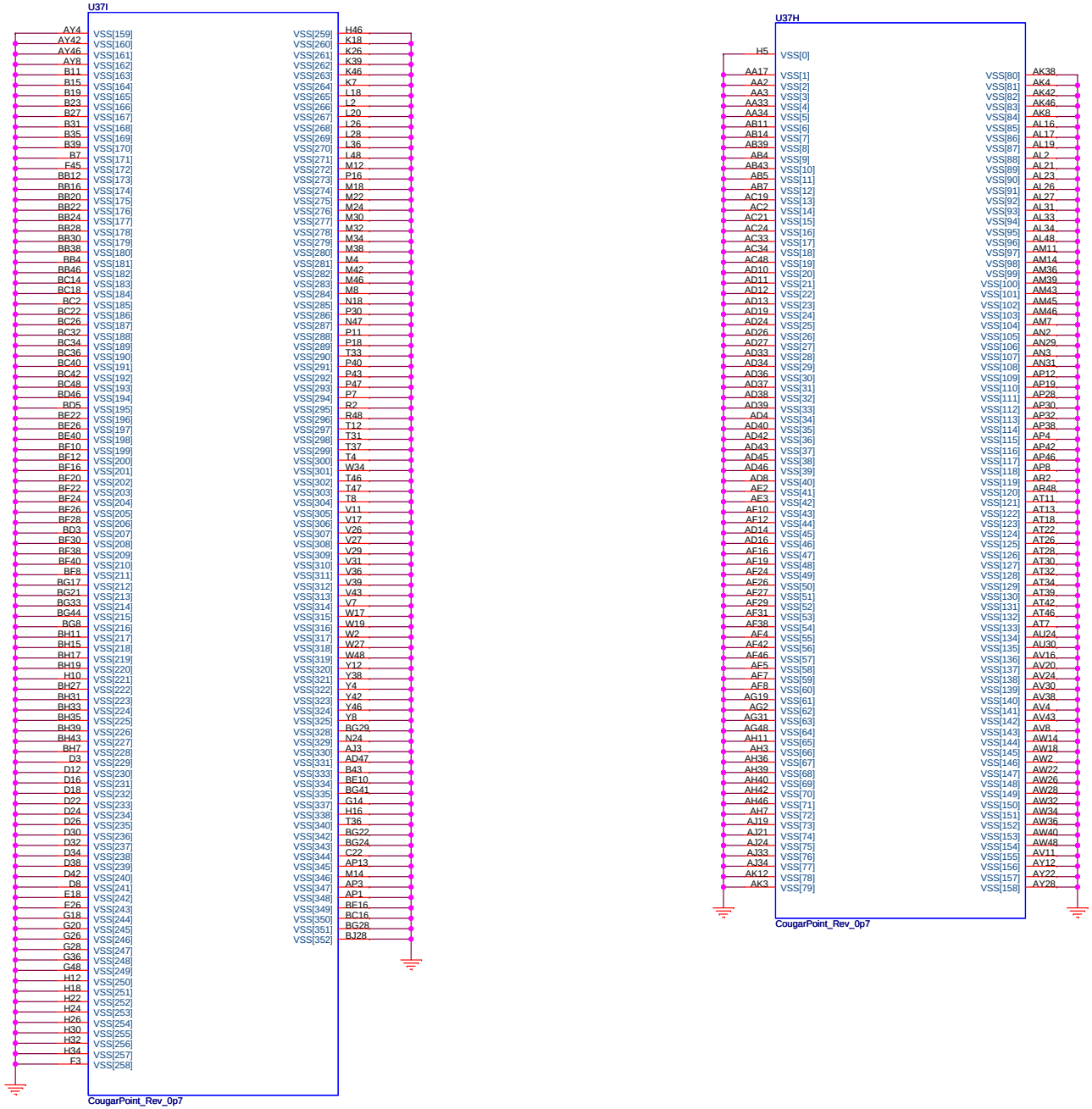
Cougar Point-M (POWER)



PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 8/9 (POWER2)	1A

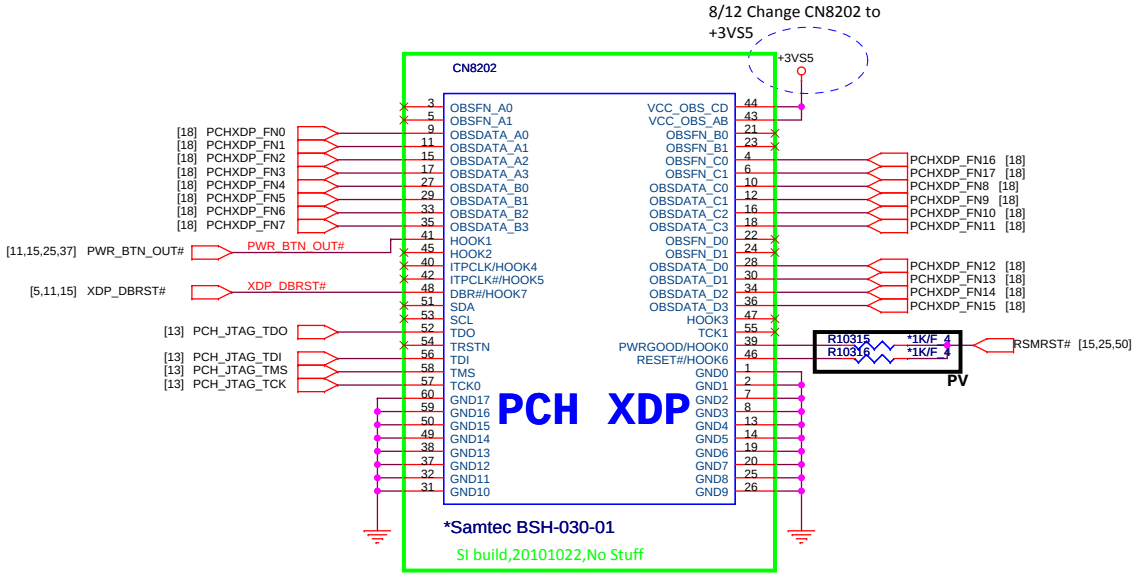
Date: Wednesday, January 19, 2011 | Sheet 20 of 58



PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 9/9 (GND)	1A

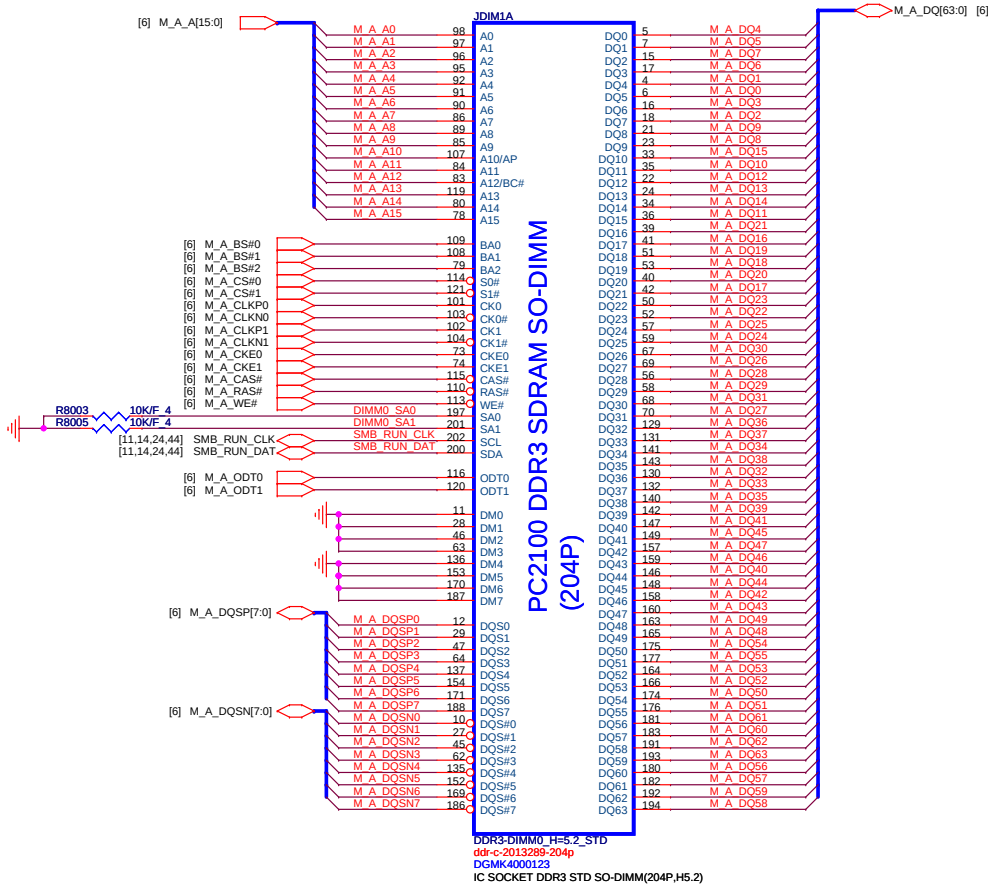
Date: Wednesday, January 19, 2011 Sheet 21 of 58

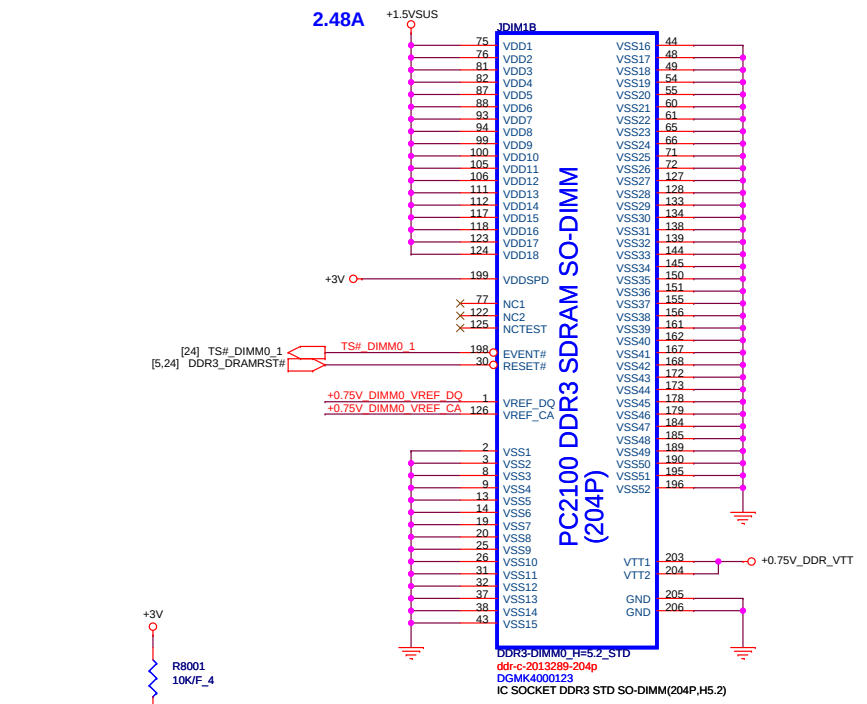


PROJECT : F11
Quanta Computer Inc.

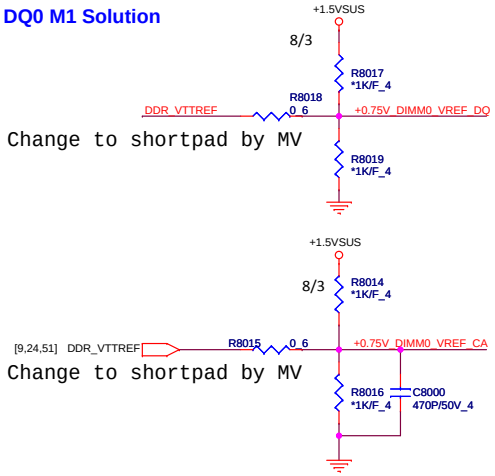
Size	Document Number	Rev
Custom	PCH XDP	1A

Date: Wednesday, January 19, 2011 Sheet 22 of 58

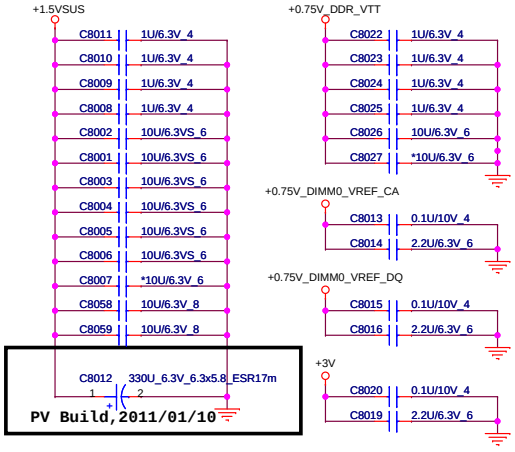




VREF DQ0 M1 Solution



Place these Caps near So-Dimm0.



PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM0-STD (5.2H)	1A

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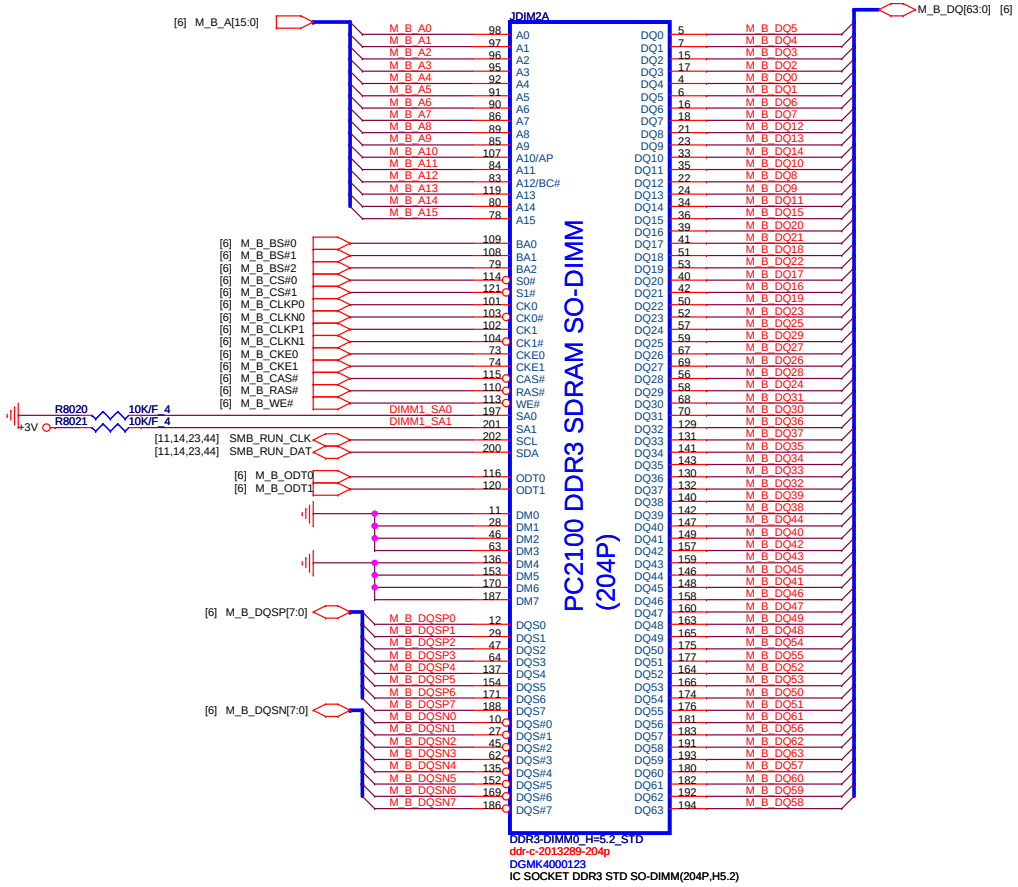
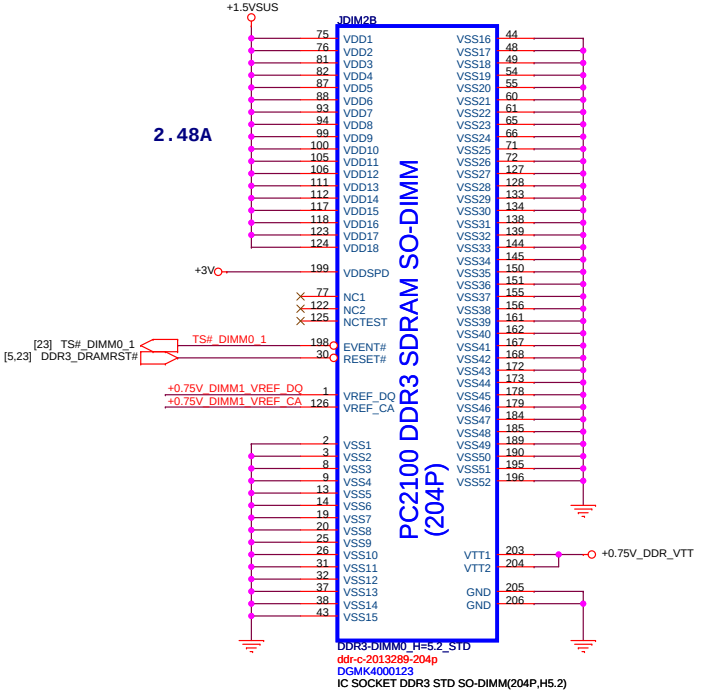
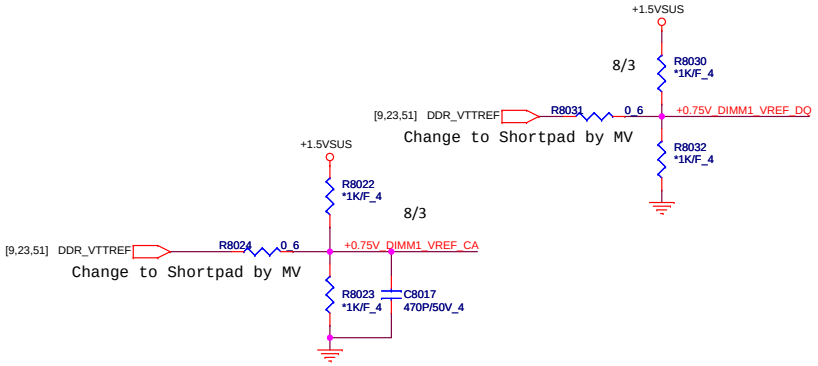
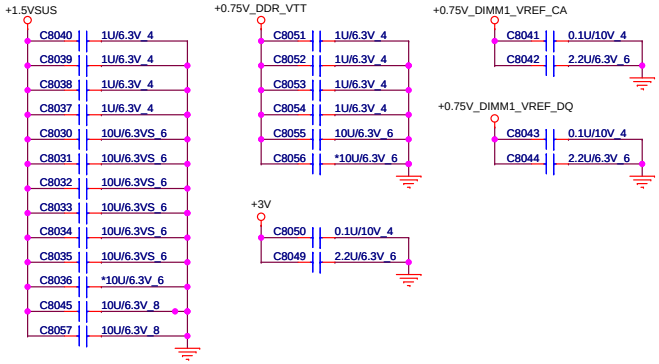




VREF DQ1 M1 Solution



Place these Caps near So-Dimm1.



PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM1-STD (5.2H)	1A

Date: Wednesday, January 19, 2011 | Sheet 24 of 58

U9019
KBC1126-NU
SI build,20101014
10/14 Modify Footprint to LQFP128-16X16-4

8/11 Change KSOUT12/13 to Test point

8/16 Del R9307 (no Num Lock support)

SI Build, 20101021 ,RF

SI build,20101110
HP requirement(U9019#127 and R9238)

Remove by MV

Close to EC

SI build,20101029

8/17 Delete
R9200,R9199,C7149,C7143,Y7000,R9285

PV modify, 20110117

SI build,20101011

SI build,20101001

PV Build modified ,20101231

SI build,1014
Remove R202

8/24 Modify

8/20 Modify
8/24 Modify

PV Build modified ,20101231

MB ID: 1=13"&14",
0=15&17.
for numeric keyboard

8/16 Add

Remove from MV

Remove from MV
Remove U9080,C9981 and stuff
R9286,R9290

use 0 ohm for production

LQFP128-16X16-4
PAS Rev 0.02 1-11-2010

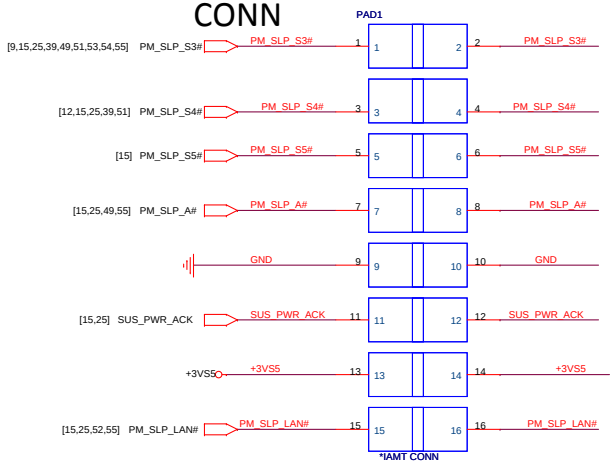
8/10

PROJECT : F11
Quanta Computer Inc.

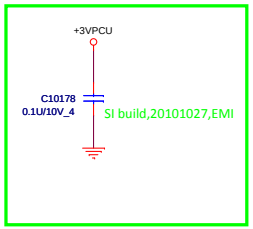
Size	Document Number	Rev
Custom	SMSC KBC1126	1A

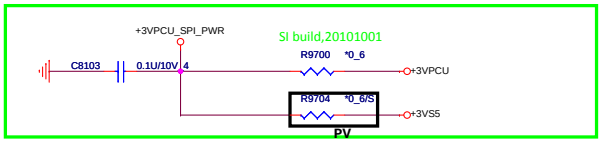
Date: Wednesday, January 19, 2011 | Sheet 25 of 58

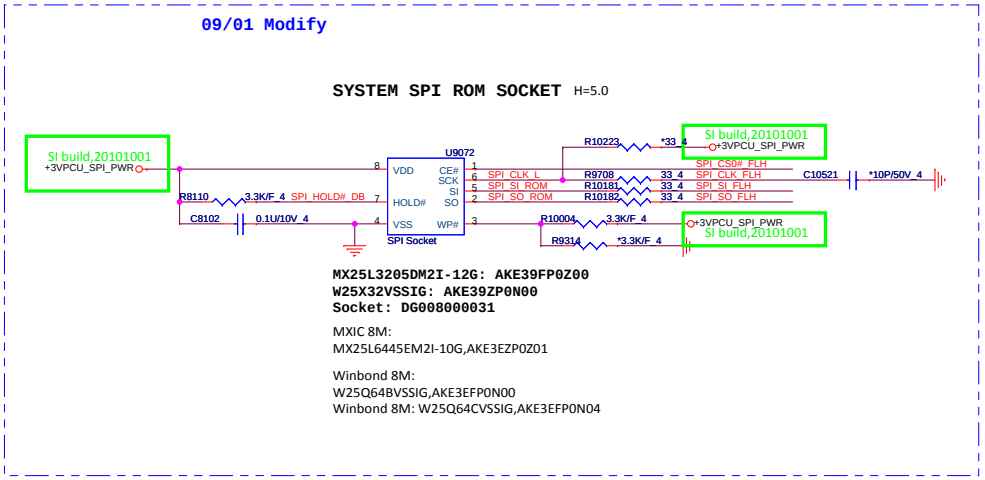
AMT/ME COMPLIANCY TEST CONN



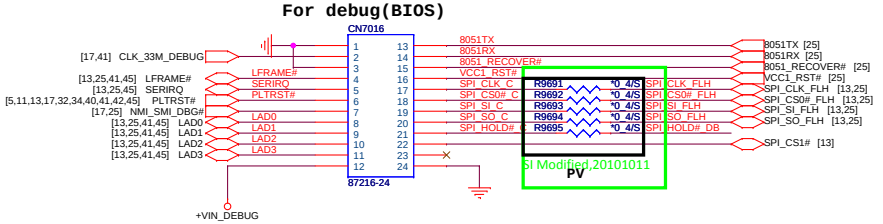
To place this on bottom side on M/B beneath door to make this user accessible. In addition, all signals should be routed within close proximity of each other (~10cm/4.5in)

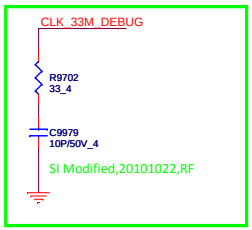






debug connector CN7016 within 1” of both U9072 and KBC1126





[47,50] +VIN_DEBUG

PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EC SPI ROM/IAMT CONN	1A

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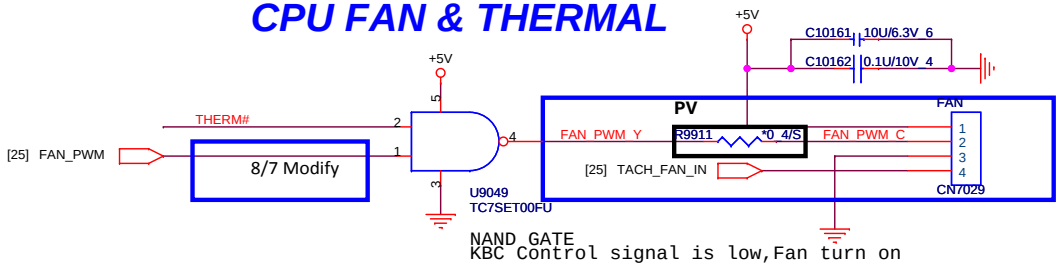
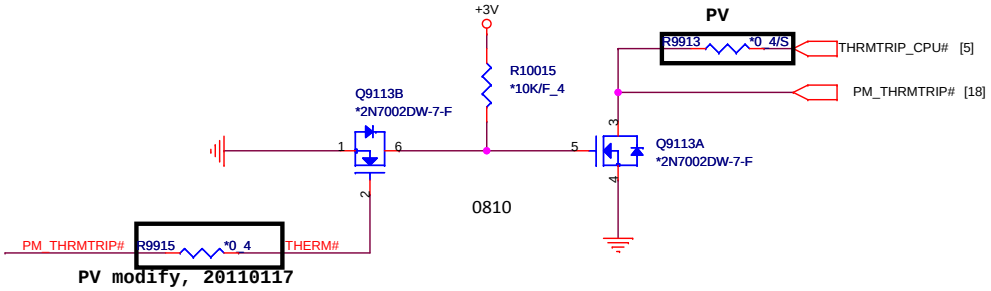
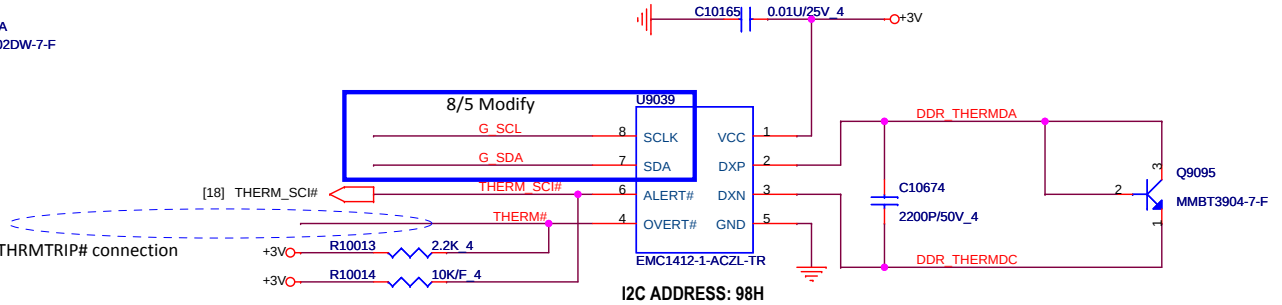
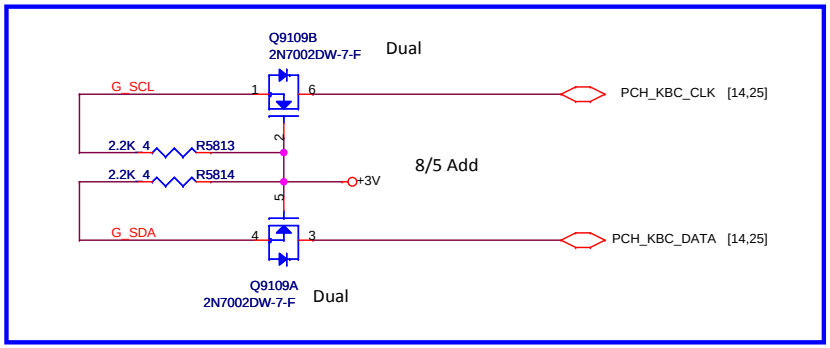
CPU FAN & THERMAL









PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
B	Thermal / FAN	1A

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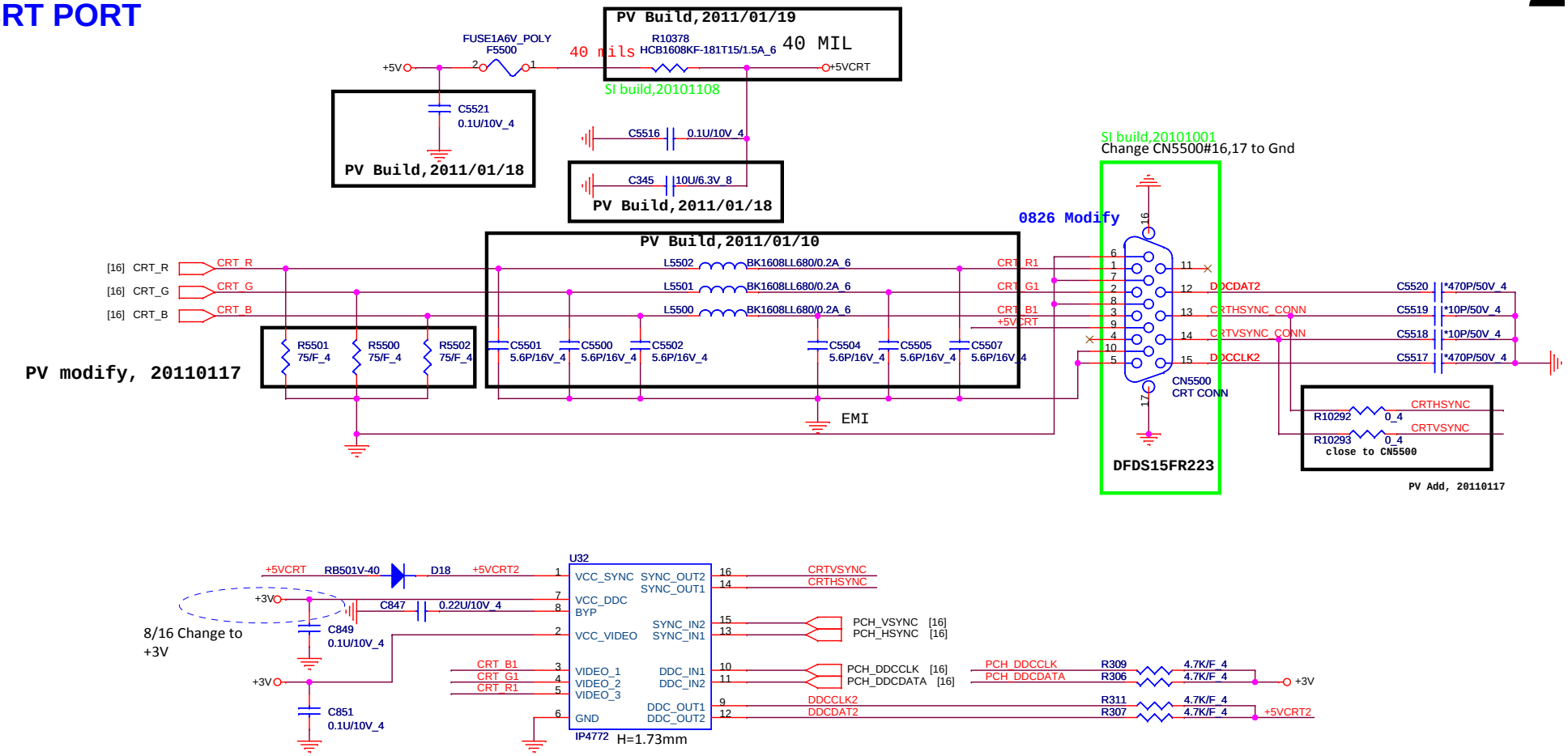
CRT PORT

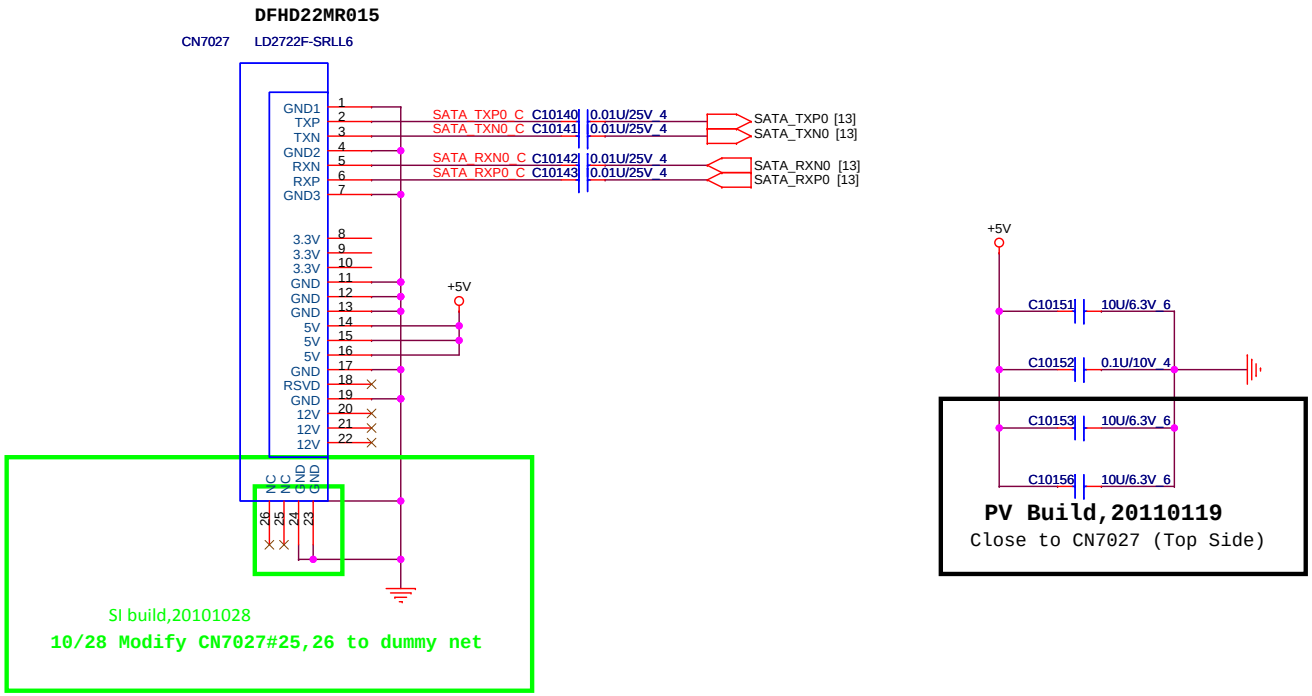


PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
B	CRT	1A

Date: Wednesday, January 19, 2011 Sheet 28 of 58

SATA HDD CONNECTOR

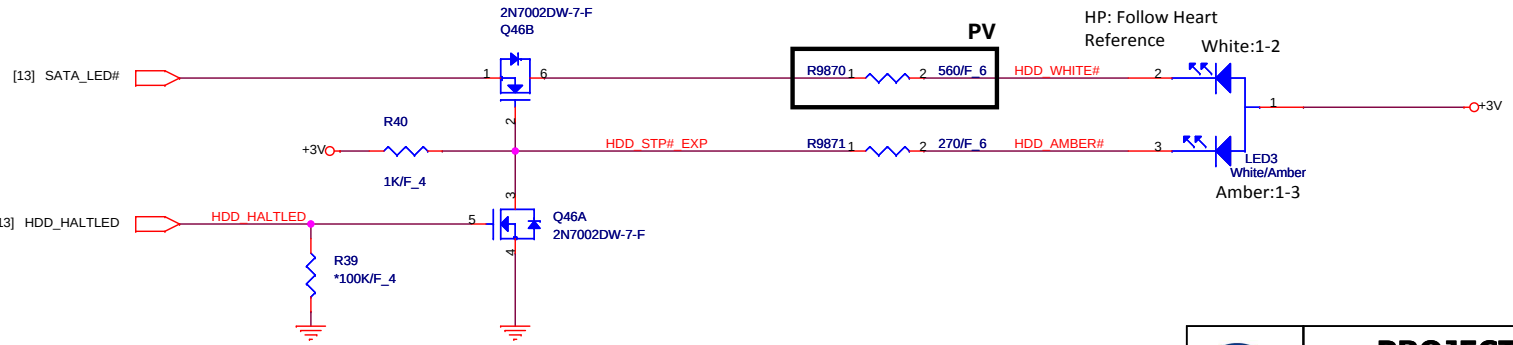


LED

8/10

8/5

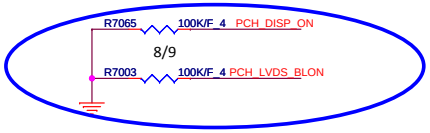
HP: Follow Heart Reference

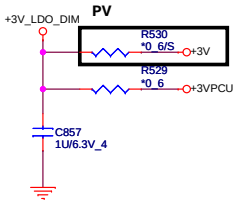


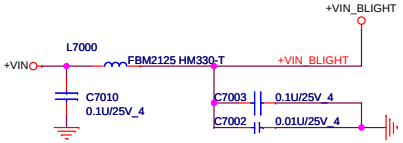
PROJECT : F11
Quanta Computer Inc.

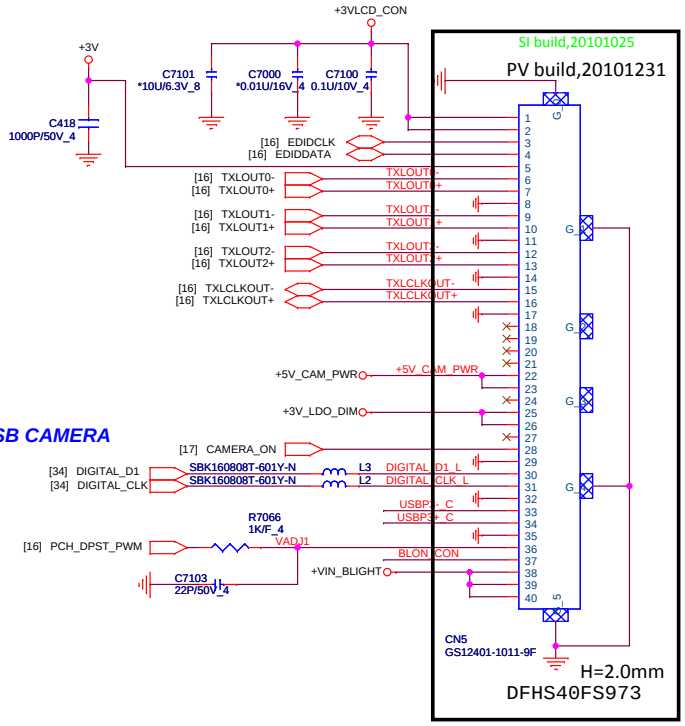
Size	Document Number	Rev
B	HDD/HDD LED	1A

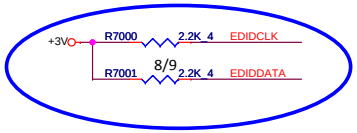
Date: Wednesday, January 19, 2011 Sheet 29 of 58

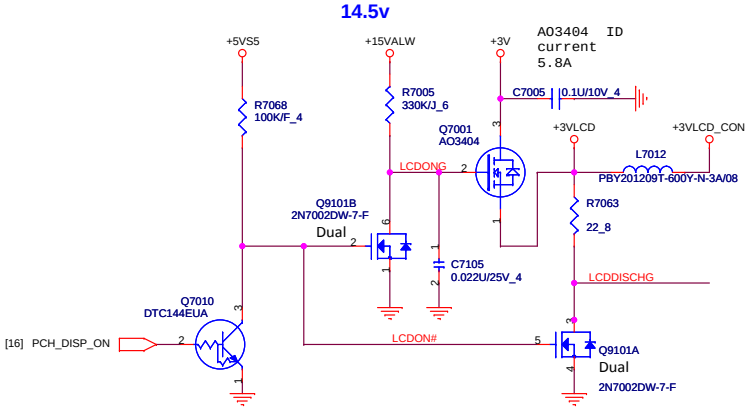


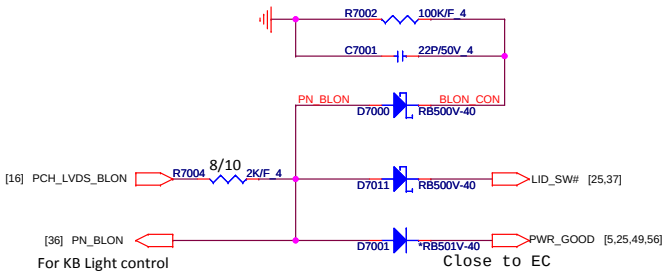


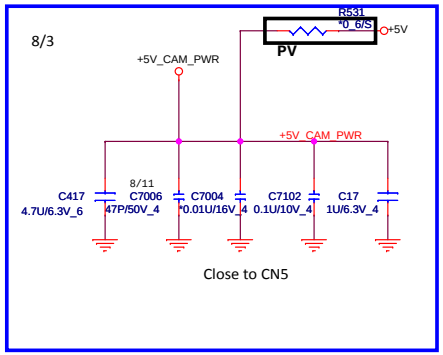


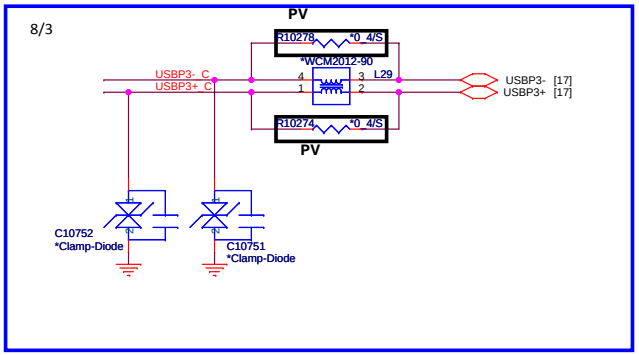












[5,11,12,13,14,15,16,17,18,19,20,23,24,25,27,28,29,31,34,36,37,38,39,40,42,44,45,48,49,51,55,56] +3V
[13,14,25,26,34,36,37,38,47,48,50] +3VPCU
[19,20,27,28,29,31,34,36,37,47,48,49,55,58] +5V
[12,20,39,49,50,51,53,54,56,57] +5VS5
[50,55] +15VALW
[47,50,51,53,54,55,57,58] +VIN

PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM/DMIC	1A
Date: Wednesday, January 19, 2011	Sheet 30 of 58	

8/31 Modify

HDMI PORT

HDMI CON_COM

Place close to Connector

8/16 Add (EMI request)

PV Build,20110119

+5VHDMI
D9029 RB501V-40
D5800 RB501V-40
R5811 2.2K_4
R5812 2.2K_4
C5800 *10P/50V_4
C5810 *10P/50V_4

CN27
HDMI_IN_D2 1
HDMI_IN_D2# 3
HDMI_IN_D1 4
HDMI_IN_D1# 6
HDMI_IN_D0 7
HDMI_IN_D0# 9
HDMI_IN_CLK 10
HDMI_IN_CLK# 12
D2+ D2- D1+ D1- D0+ D0- CK+ CK-
SHELL1 SHELL2 SHELL3 SHELL4 20 21 22 23
D2 Shield D1 Shield D0 Shield CK Shield GND 2 5 8 11 17

HDMISCL 15
HDMISDA 16
DDC CLK CE Remote 13
DDC DATA NC 14
+5V 18
HP DET 19
HDMI_HPD_CON
HDMI CONN

C562 *10P/50V_4
C571 *10P/50V_4
+5VCRT
R10383 0_6
PV Build,20110118
C819 0.01U/25V_4
C817 *0.01U/25V_4

8/3

[16] TMDSC_CLKB C479 0.1U/10V_4 IN_CLK#
[16] TMDSC_CLK C478 0.1U/10V_4 IN_CLK
[16] TMDSC_DATA0B C482 0.1U/10V_4 IN_D0#
[16] TMDSC_DATA0 C481 0.1U/10V_4 IN_D0
[16] TMDSC_DATA1B C485 0.1U/10V_4 IN_D1#
[16] TMDSC_DATA1 C484 0.1U/10V_4 IN_D1
[16] TMDSC_DATA2B C490 0.1U/10V_4 IN_D2#
[16] TMDSC_DATA2 C486 0.1U/10V_4 IN_D2

[16] HDMI_HPD_CON
D29 BAV99
+5V
Close to Connector
8/9 Modify
R472 20K/F_4

8/9 Modify
+3V
Q38 2N7002W_SC70
R520 100K/F_4
C677 0.1U/10V_4

R510 680/F_4 IN_D2
R508 680/F_4 IN_D2#
R511 680/F_4 IN_D1
R507 680/F_4 IN_D1#
R502 680/F_4 IN_D0
R504 680/F_4 IN_D0#
R519 680/F_4 IN_CLK
R521 680/F_4 IN_CLK#

+3V
R207 2.2K_4
[16] DPD_CTRL_CLK R469 33_4 HDMI_SCL HDMISCL
8/6 Add Level shift circuit
Q9112B 2N7002DW-7-F
Q9112A 2N7002DW-7-F
[16] DPD_CTRL_DATA R470 33_4 HDMI_SDATA HDMISDA
R208 2.2K_4
+3V

Close to Connector

PV
*0_4/S R10367
*W21HN900SQ2L L9090
*0_4/S R10368
*0_4/S R10369
L9091
*0_4/S R10370
*0_4/S R10371
L9092
*0_4/S R10372
*0_4/S R10373
L9093
*0_4/S R10374

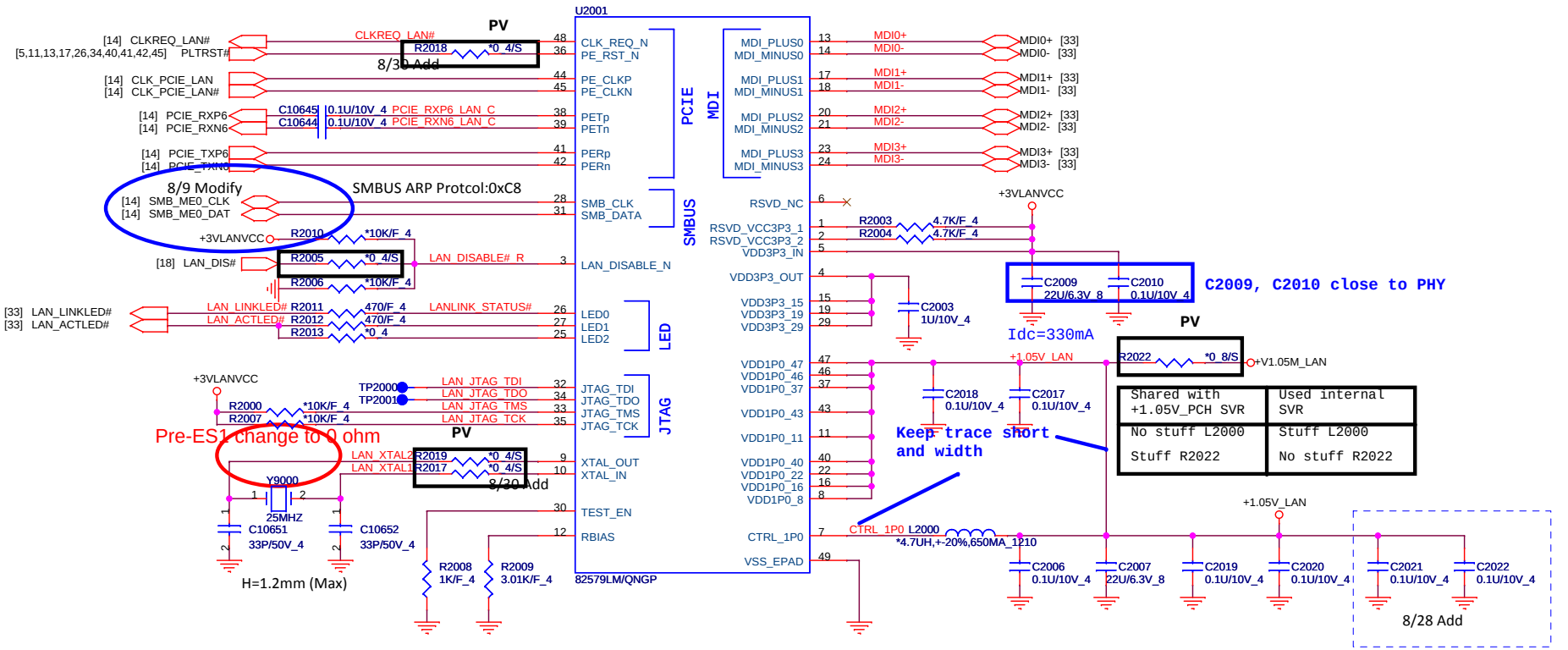
IN_D2 IN_D2# HDMI_IN_D2 HDMI_IN_D2#
IN_D1# IN_D1 HDMI_IN_D1# HDMI_IN_D1
IN_D0 IN_D0# HDMI_IN_D0 HDMI_IN_D0#
IN_CLK IN_CLK# HDMI_IN_CLK HDMI_IN_CLK#

8/16 Add (EMI request)

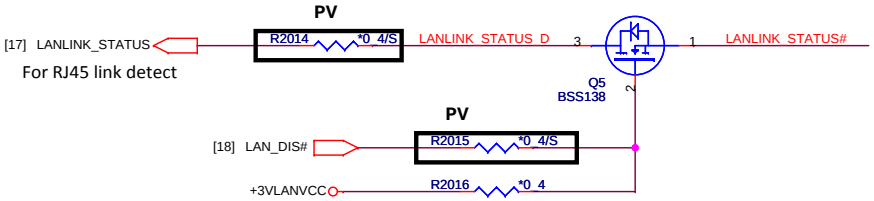
PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI Conn	1A
Date: Wednesday, January 19, 2011	Sheet 31 of 58	

[5,11,12,13,14,15,16,17,18,19,20,23,24,25,27,28,29,30,31,34,36,37,38,39,40,42,44,45,48,49,51,55,56] +3V
[33,49,55] +3VLANVCC
[52,55] +V1.05M_LAN



SI Build, 20101021, Stuff C2020,C2018.C2022,C2019,C2017-->RF

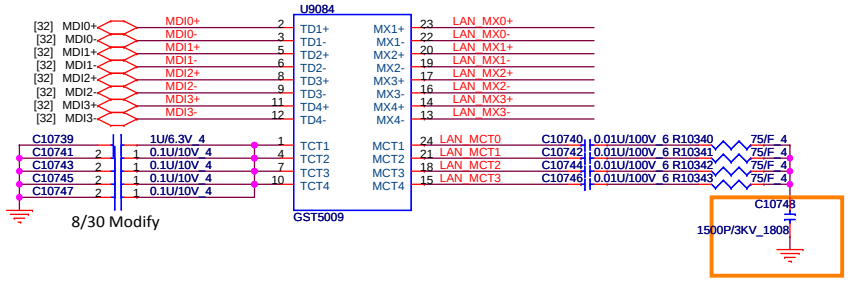


PROJECT : F11
Quanta Computer Inc.

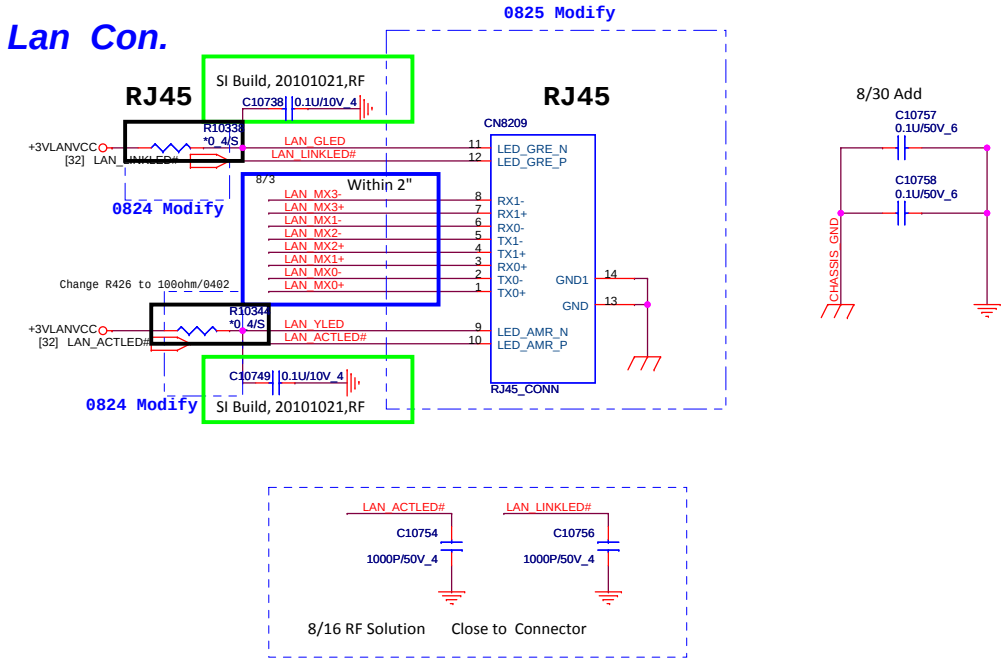
Size	Document Number	Rev
B	Intel Lewisville 82579LM	1A

Date: Wednesday, January 19, 2011 Sheet 32 of 58

Transformer for 10/100/1000



Lan Con.



PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RJ45 CONN	1A

Date: Wednesday, January 19, 2011 | Sheet 33 of 58

Port A: (Unused)
Port B: Capless Headphone Jack
Port C: External Mic Jack
Port D: Internal Speakers
Port E: (Unused)
Port F: (Unused)

0820 Modify Del L18

Close to CODEC

ALL CAPS CONNECTED TO THE 92HD80Bx
SHOULD BE X7R OR X5R--NO Y5V

U17 92HD80B1X5NLGXTA58

HDA Bus

TO Digital MIC

8/5 Follow Intel (33 ohm)

SENSE_A -->EXT MIC/Headphone out

Port B:TO Combo Headphone Jack

Port C:From Combo MIC

TO External Speaker

Analog

Digital

COMMUNICATION WITH KBC
MUTE_LED_CNTRL is the control for the mute LED
0 when system default audio is not muted (in MSFT)
1 when system default audio is muted (in MSFT)
A_SD# is the state of the speaker as controlled by hardware.
0 when speaker is muted by hardware
(e.g., during OS boot or via BIOS setting)
1 when speaker is not muted by hardware

DGND and AGND
must be shorted
together
on internal GND plane
directly under the codec

0923
1. Pin 49 tied to DGND as IDT request
2. Add 12 via from Pin 49 to DGND

25mils trace width request

Analog audio ground must not have more than one DC connections to digital ground and should be located directly under codec. An 80 mil copper bridge between AGND and DGND preferred. Audio ground cannot be directly shorted to digital ground at the audio jacks for any reason (EMI/ESD/other).

0820 Modify
SI Build, 20101021,EMI

0827 Modify
SI Build, 20101028

SI build,20101016 EMI

SI modify, 20101108

>40mils trace

PV

For Combo Audio Jack

Hp request

SI build,20101001
Change net connection

Change net connection
SI build,20101013

PV Build modified ,20101231

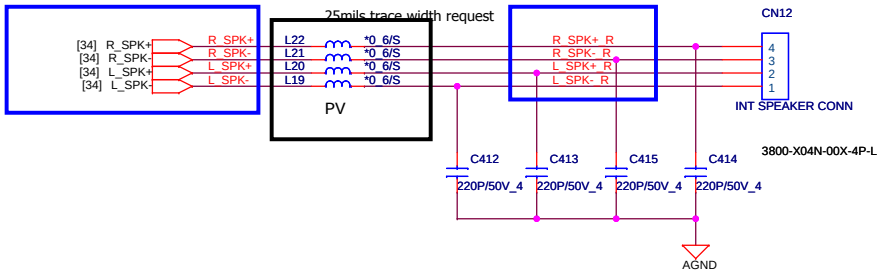
comparator

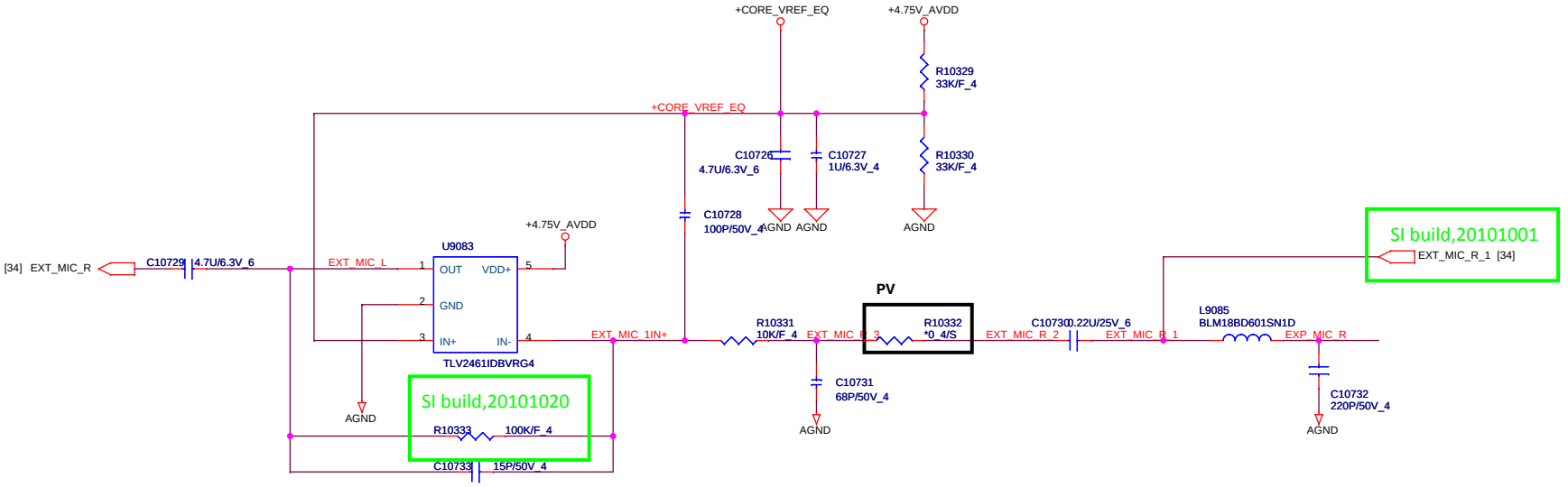
FOR EMI

PROJECT : F11
Quanta Computer Inc.

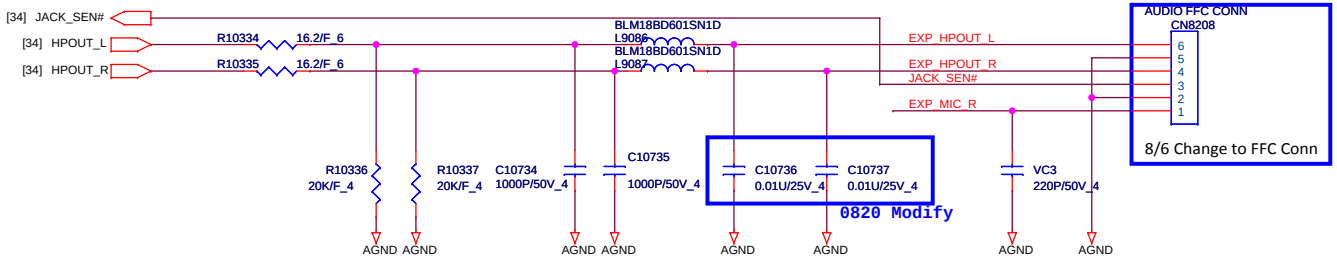
Size: Custom | Document Number: Azalia 92HD80B1 | Rev: 1A
Date: Wednesday, January 19, 2011 | Sheet 34 of 58

INT. SPEAKER





Combo Jack (Headphone/MIC)



PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SPKR/Audio Jack/Pre-AMP	1A

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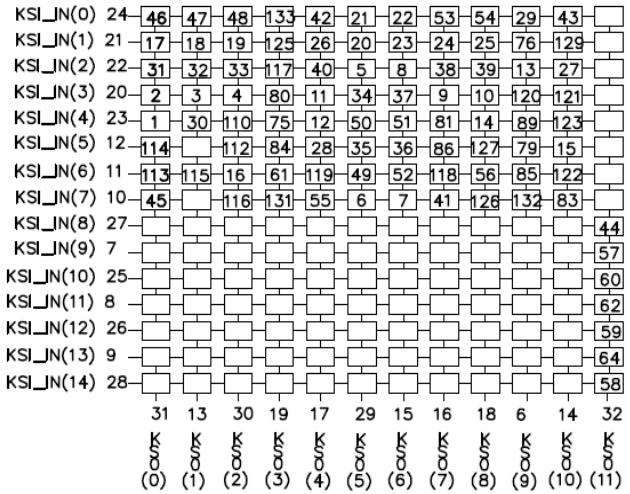
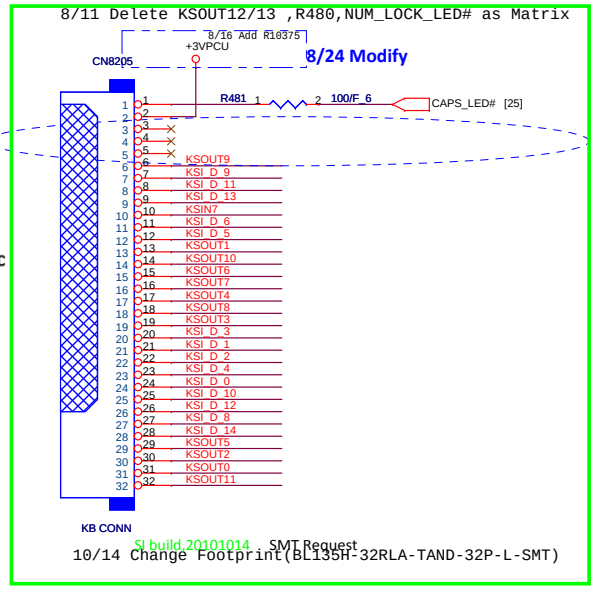
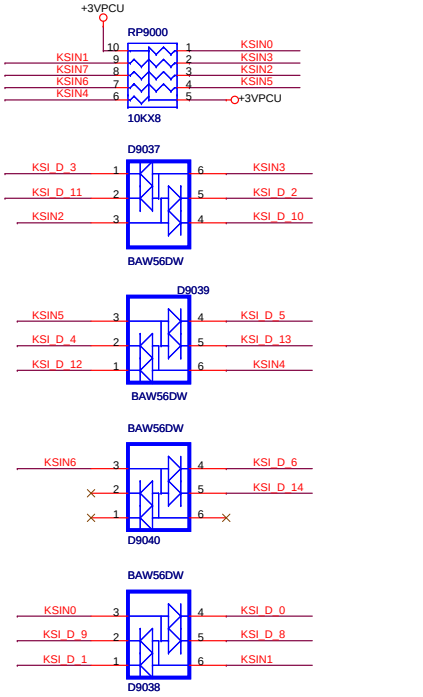
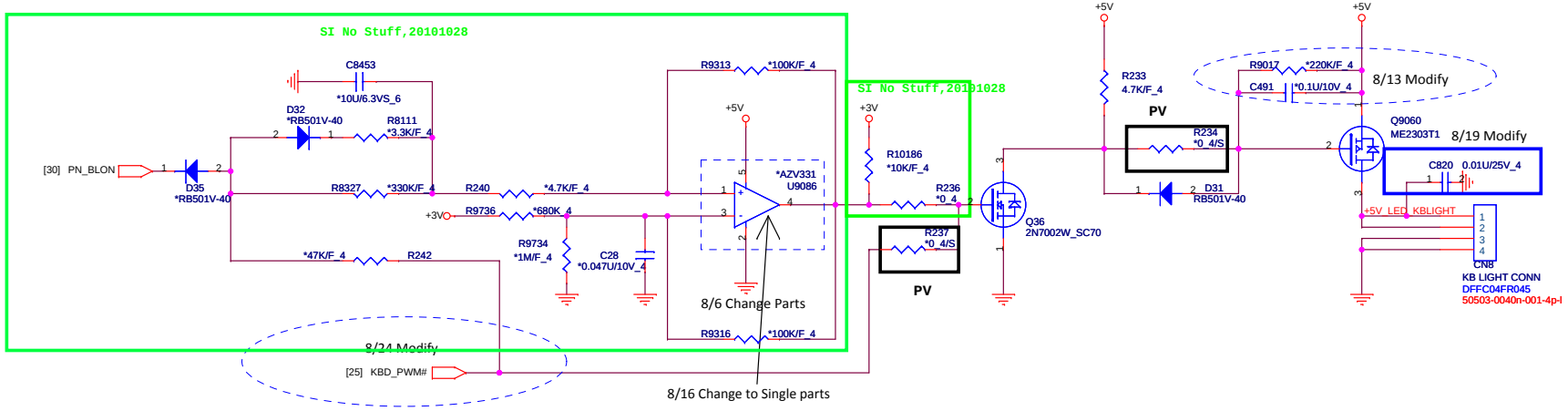






KEYBOARD LIGHT CONTROL



PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB,KB Light Control	1A

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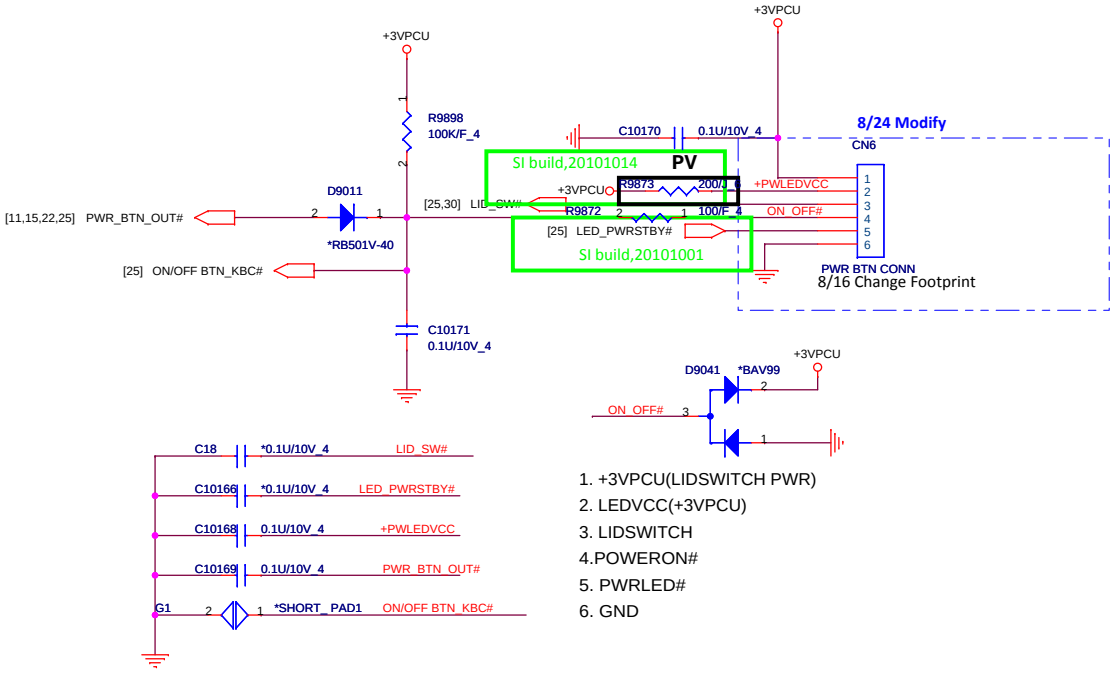
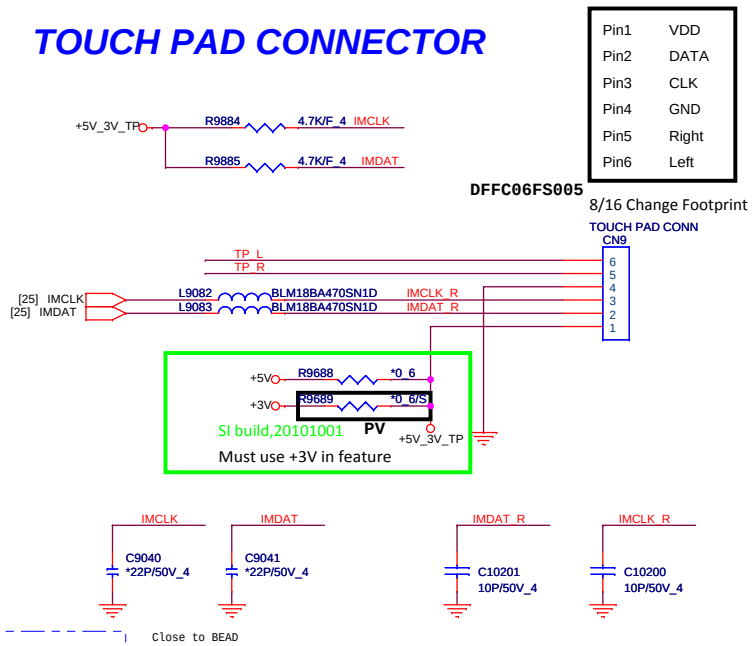
POWER BOTTON CONNECT



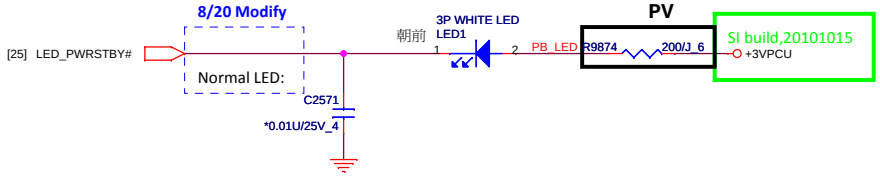
1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

TOUCH PAD CONNECTOR



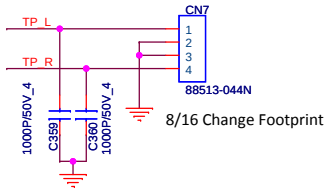
09/01 Modify

PWR LED



SI build,20101001

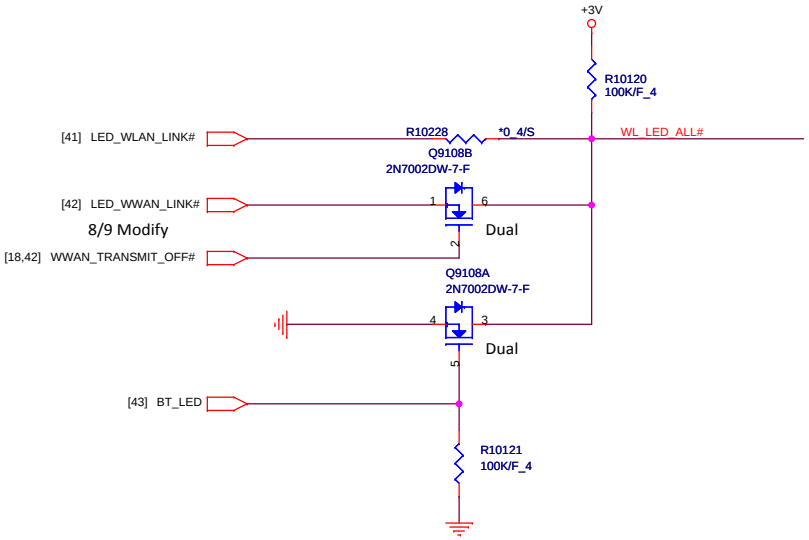
TOUCH PAD SW CONN



PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Touch Pad,TP SW,PWR CONN	1A

Date: Wednesday, January 19, 2011 | Sheet 37 of 58



Function Board(Mute/Quickweb/Wireless)

KSI0 (MUTE)

Mute LED: Amber when
Mute(Single Color)

KSI1 (WIRELESS)

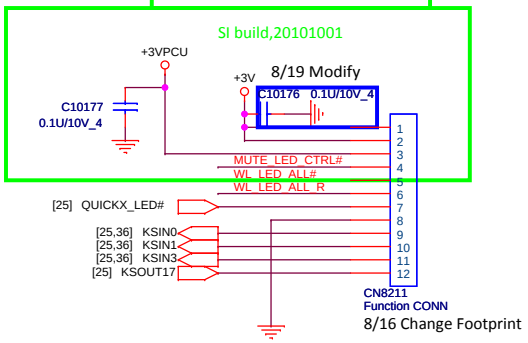
Dual Color (White/Amber)
Wireless LED: Wireless ON(White) and Wireless OFF(Amber)

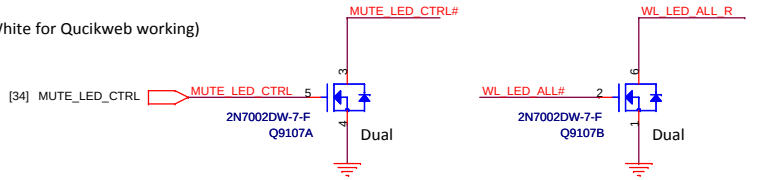
KSI3 (QUICKX)

Quickweb LED: (White for Qucikweb working)

SI build,1001

Change CN8211#3 to +3VPCU from MUTE_LED_CTRL due QUICKX_LED# power source change to +3VPCU , Also add C10177 and close to CN8211





PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	FUNCTION BOARD	1A

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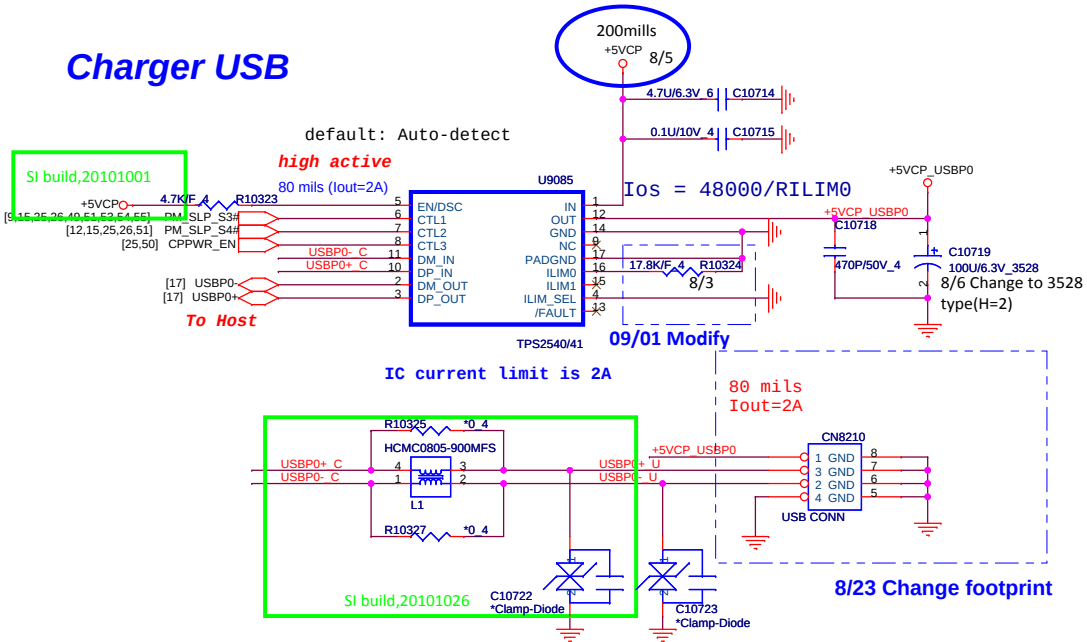
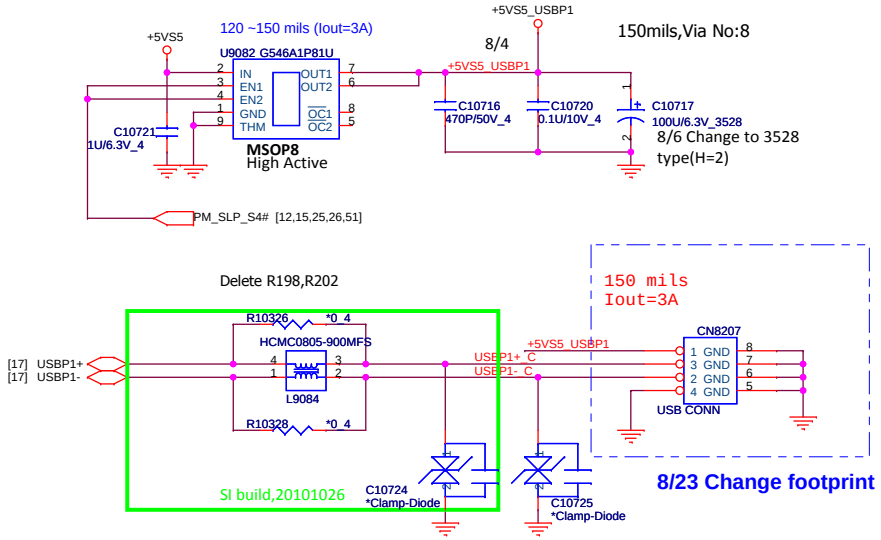
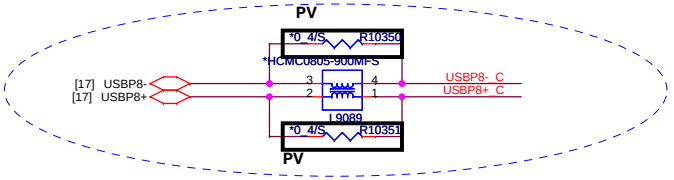
Right SIDE USBX2(Powered USB and Charger USB)

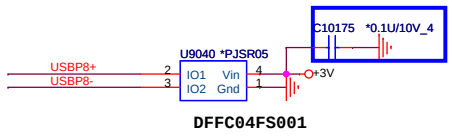
Charger USB



Powered USB

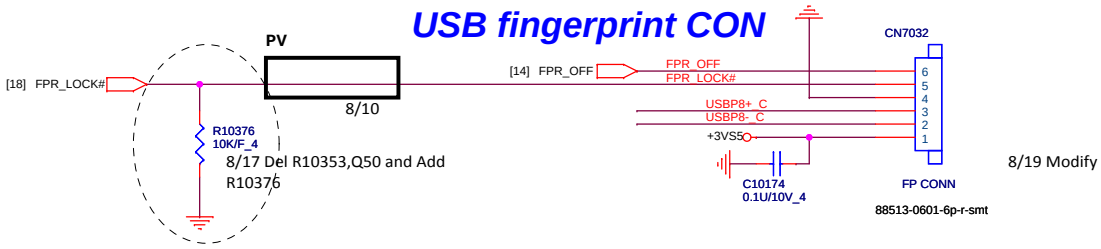






CTL1	CTL2	CTL3	TPS2540 Control Truth Table
0	0	0	Out Discharge ,Power switch OFF
0	X	1	Dedicated Charging Port,Auto detect Mode
X	1	0	Standard Downstream Port ,USB 2.0 Only
1	0	0	Dedicated Charging Port, BC Specification 1.1 Only
1	0	1	Dedicated Charging Port, Apply
1	1	1	Charging Downstream Port, BC Specification 1.1

USB fingerprint CON



PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB/FP	1A

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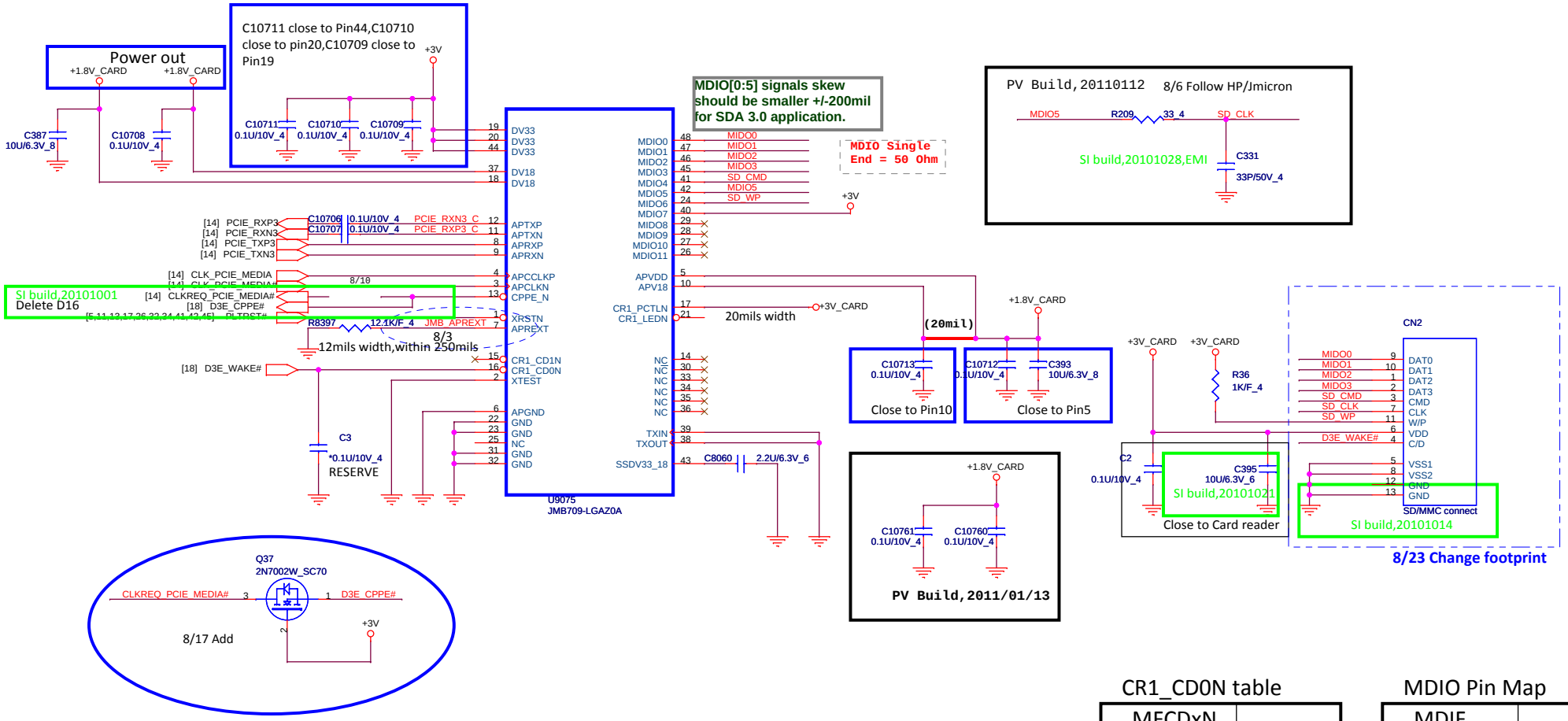

CR1_CD0N table

MFCDxN		Card type
1	0	
H	L	SD/MMC

MDIO Pin Map

MDIF		
00	SD	MMC
00	D0	D0
01	D1	D1
02	D2	D2
03	D3	D3
04	CMD	CMD
05	CLK	CLK
06	WP	WP

PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	JMB709 & CR SOCKET	1A

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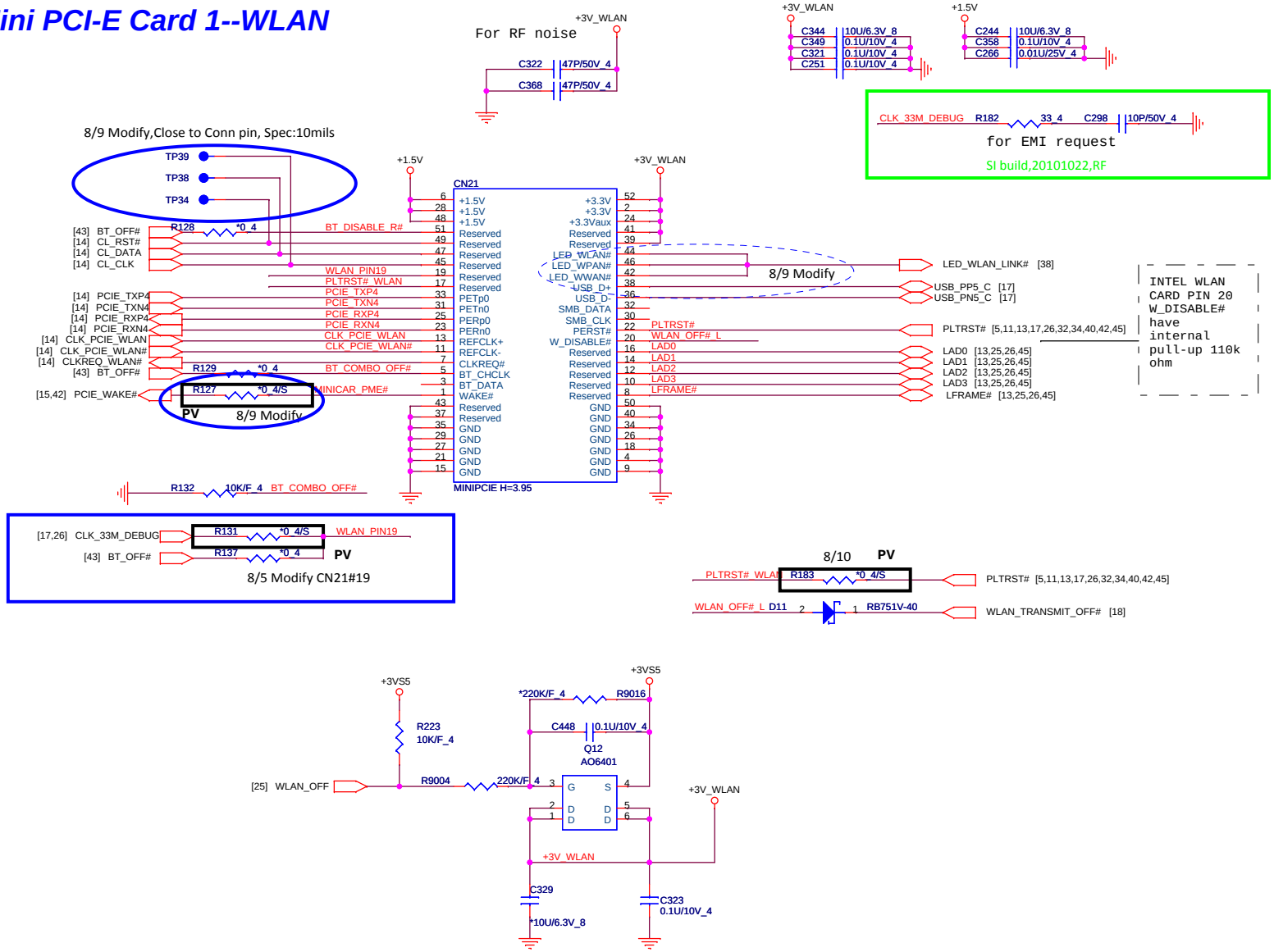
Mini PCI-E Card 1--WLAN



Quanta Debug Card: Pin16,14,12,10,8,19,17

PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	WLAN	1A

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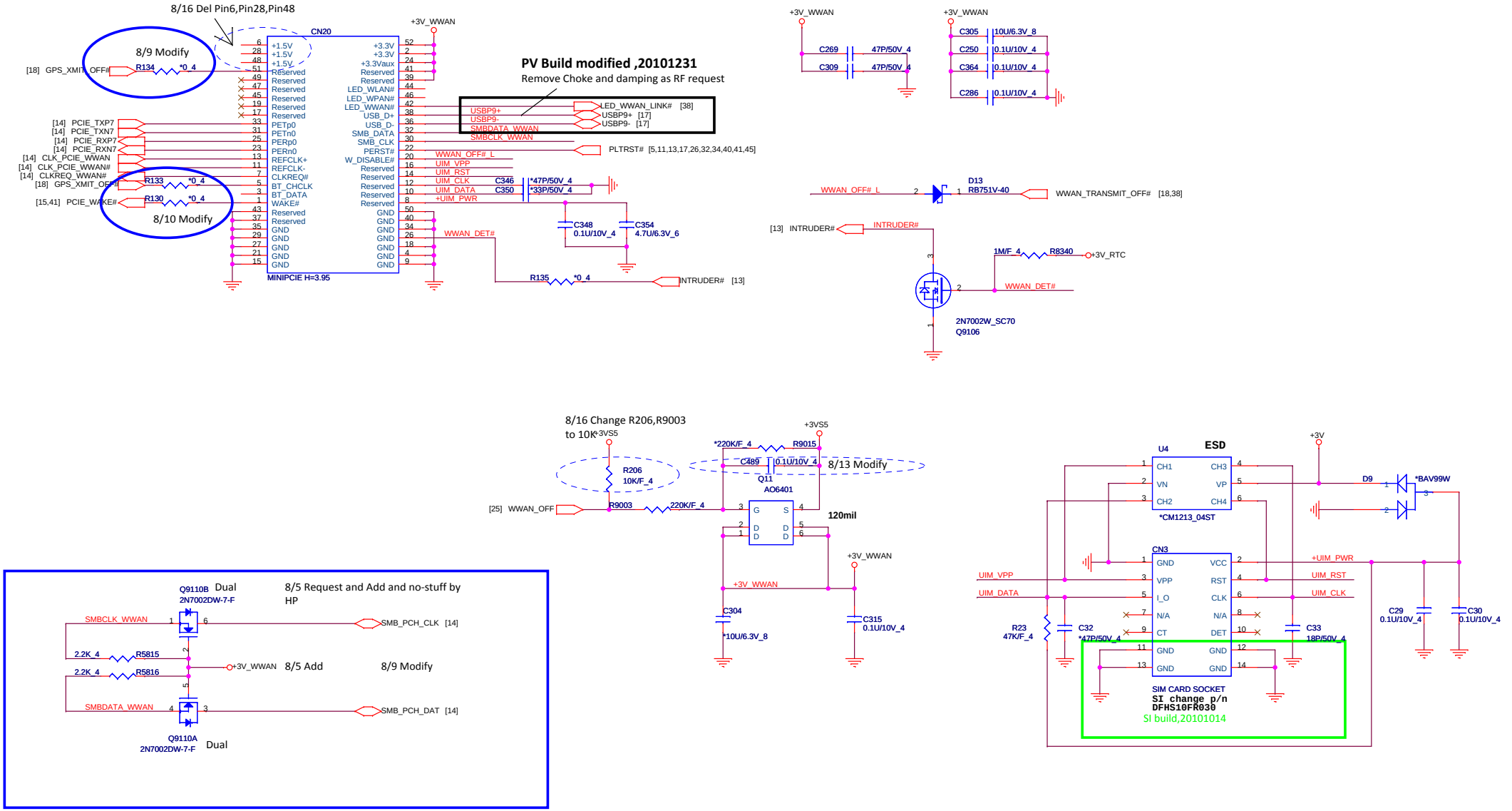
Mini PCI-E Card 2 --WWAN



PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	WWAN	3A

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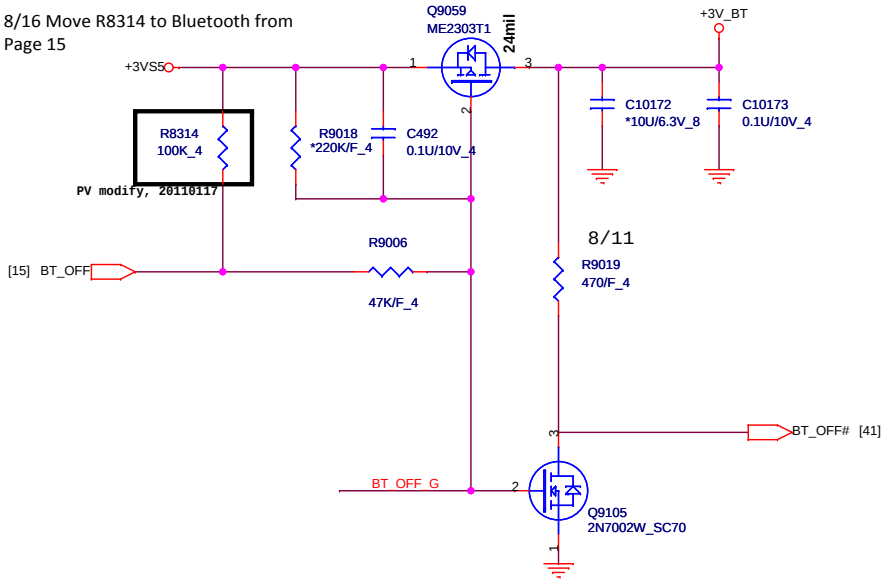
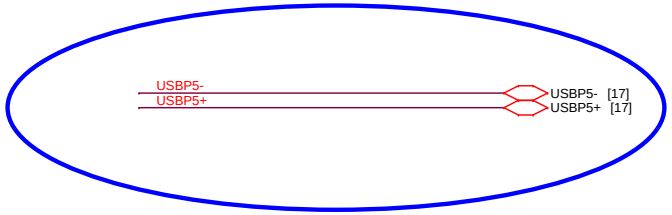
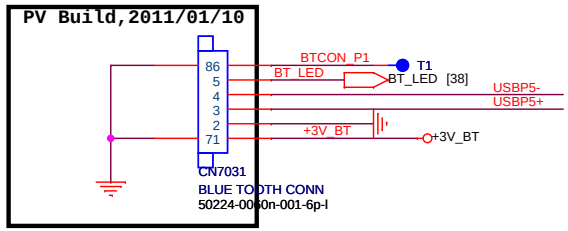
BLUETOOTH

8/16 Move R8314 to Bluetooth from Page 15





Remove L9081,R10347,R10346 by PV Build
PV Build,2011/01/18



PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
B	LCD CONN	1A

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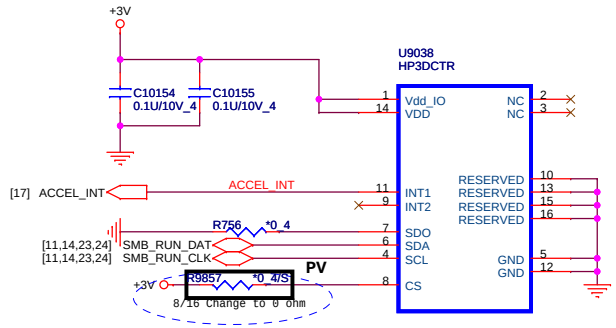
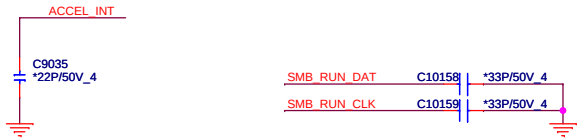
Accelerometer Sensor



8/9 Modify



PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	**Accelerometer Sensor**	1A

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SI Build, 20101021

CLK_PCI_TPM

R464
33_4

C796
10P/50V_4

FOR EMI

TPM (1.2)

8/5 Add (Follow Heart)

+3VS5

U41

[13,25,26,41] LAD0	LAD0	26	LAD0	VDD	10
[13,25,26,41] LAD1	LAD1	23	LAD1	VDD	19
[13,25,26,41] LAD2	LAD2	20	LAD2	VDD	24
[13,25,26,41] LAD3	LAD3	17	LAD3	VSB	5
[17] CLK_PCI_TPM	CLK_PCI_TPM	21	LCLK		
				GND	4
[13,25,26,41] LFRAME#	LFRAME#	22	LFRAME#	GND	11
[5,11,13,17,26,32,34,40,41,42] PLTRST#	PLTRST#	16	LRESET#	GND	18
	LPCPD# TPM	28	LPCPD#	GND	25
[13,25,26] SERIRQ	SERIRQ	27	SERIRQ		
				GPIO	6
		9	TEST/BADD	GPIO2	2
[15,25] CLKRUN#	CLKRUN#	15	CLKRUN#	PP	7
				TESTI	8
		1	NC		
		3	NC	XTALI/32K IN	13
		12	NC	XTALO	14

SLB9635TT1.2-FW3.17

TPM_PP

TPM_XIN

TPM_XOUT

H=2.54mm

+3V

R461
4.7K/F_4

C255
0.1U/10V_4

C254
0.1U/10V_4

C253
0.1U/10V_4

C252
0.1U/10V_4

R10375 10M_4

8/16 Add R10375
SI build,20101001

Y7001
32.768KHZ

C794
12P/50V_4

C797
12P/50V_4

Address

	BADD
HIGH	4EH/4F

(default)

+3V

R450
4.7K/F_4

LPCPD# TPM

TPM_PP

*4.7K/F_4

R452

+3V

*0_4/S

R451

PV

PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
B	TPM	1A

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8/16 Modify Hole footprint

H30 *H-TC315BC228D110P2

H31 *H-TC315BC228D110P2

PV Build,20110112

Remove H33

8/16 Add Hole footprint

H41 *H-TC276BC177D146P2

H42 *H-TC276BC177D146P2

H43 *H-TC276BC177D146P2

H44 *H-TC276BC177D146P2

CPU BKT

H27 *H-c138d87p2

H28 *H-c276d110p2

H29 *H-c276d110p2

H34 *H-O165X150D102X87P2

H37 *H-E276X284D126P2

H38 *H-E276X284D126P2

H39 *H-E276X284D126P2

H40 *H-TC276BSD110P2-1

H32 *H-TC276BSD110P2-1

PAD2 *SPAD-RE335X315

PAD3 *SPAD-RE366X287

PAD4 *SPAD-RE366X421

PAD5 *SPAD-E386X496B

8/17 Add

H45 *H-C122D102

H46 *H-C122D102

PAD6 *SPAD-F11

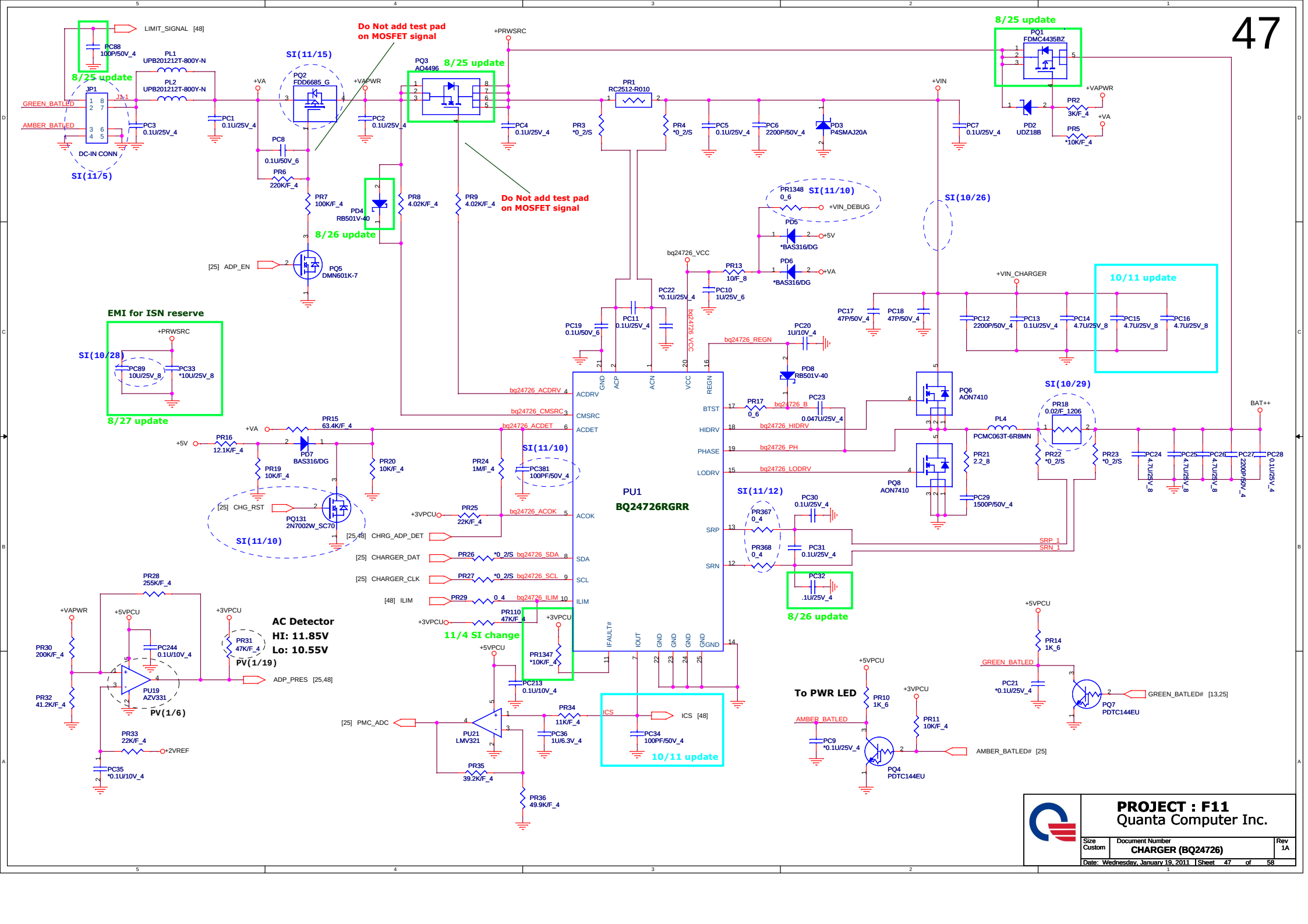
PV ADD, 20110113

H35 *H-SSbsd110p2

H36 *H-O165X150D102X87P2

20101028 SI add

	PROJECT : F11 Quanta Computer Inc.	
Size Custom	Document Number **HOLE**	Rev 1A
Date: Wednesday, January 19, 2011	Sheet 46 of 58	



PROJECT : F11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CHARGER (BQ24726)	1A

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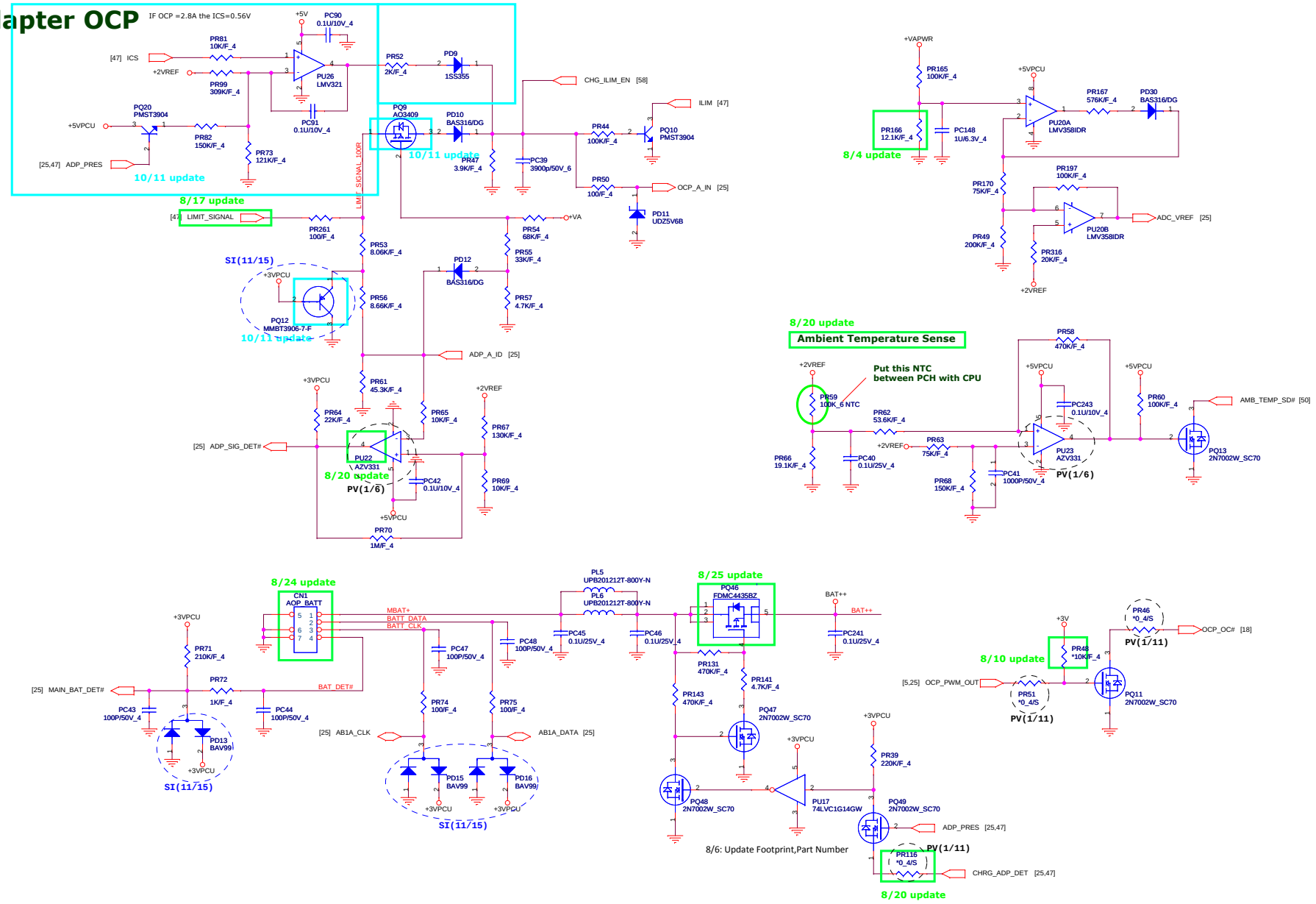
Adapter OCP


IF OCP =2.8A the ICS=0.56V
10/11 update
8/17 update
10/11 update
10/11 update
8/4 update
8/20 update
Ambient Temperature Sense
Put this NTC
between PCH with CPU
8/20 update
PV(1/6)
8/24 update
8/25 update
8/10 update
PV(1/11)
8/6: Update Footprint,Part Number
8/20 update
SI(11/15)
SI(11/15)
SI(11/15)
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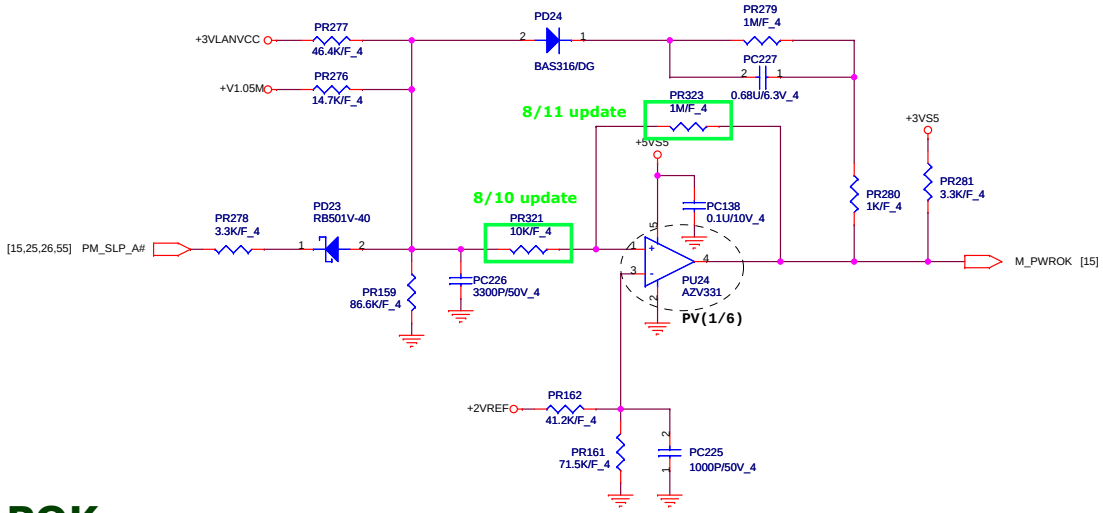
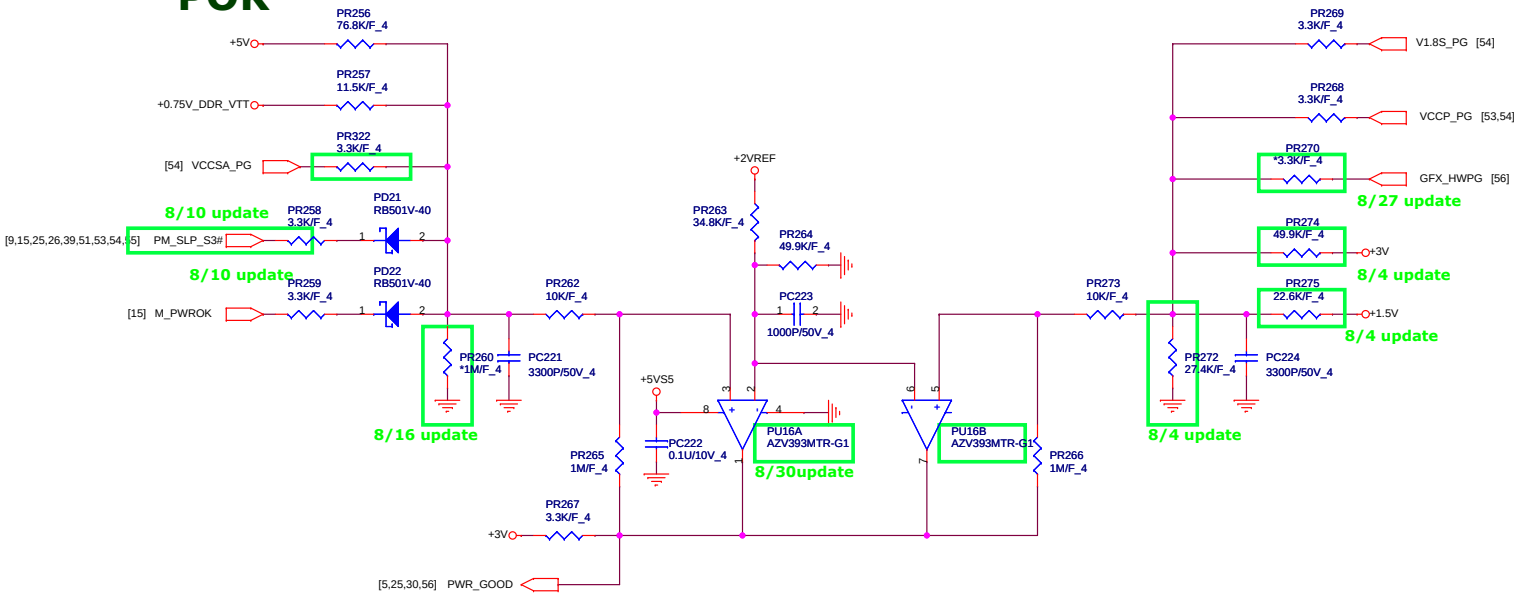
POK CKT

PM_SLP_S4# = SUSON
PM_SLP_S3# = MAINON
+V5S = +5V
+V3S = +3V
+V0.75S =+0.75V_DDR_VTT

For iAMT



POK



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DC/DC +3VPCU/+5VPCU/+5VS5 /+3VS5

+5V +/- 5%
Countinue current:5A
Peak current:6A
OCP minimum:7.5A

+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

TPS51123

Place these CAPs close to FETs

Place these CAPs close to FETs

5V --- 400KHz
3V --- 500KHz

Rdson=14m ohm

Rdson=14m ohm

8/16 update

8/16 update

8/25 update

8/25 update

8/20 update

8/4 update

8/10 update

8/16 update

SI(11/15)

PV(1/11)

PV(1/6)

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Custom	3/5VS5 (RT8223M)	1A

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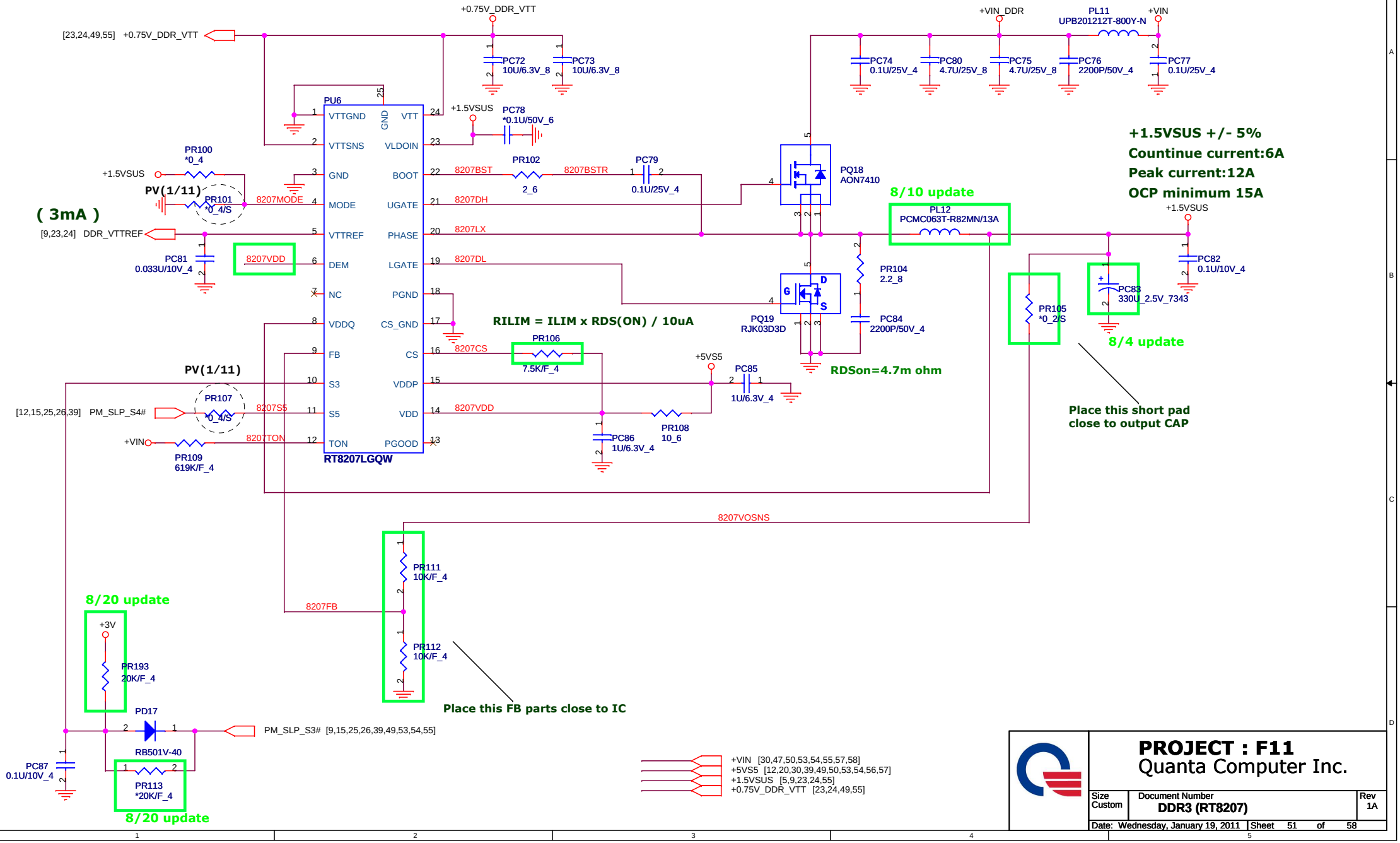
(VTT/2A)



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Custom	DDR3 (RT8207)	1A

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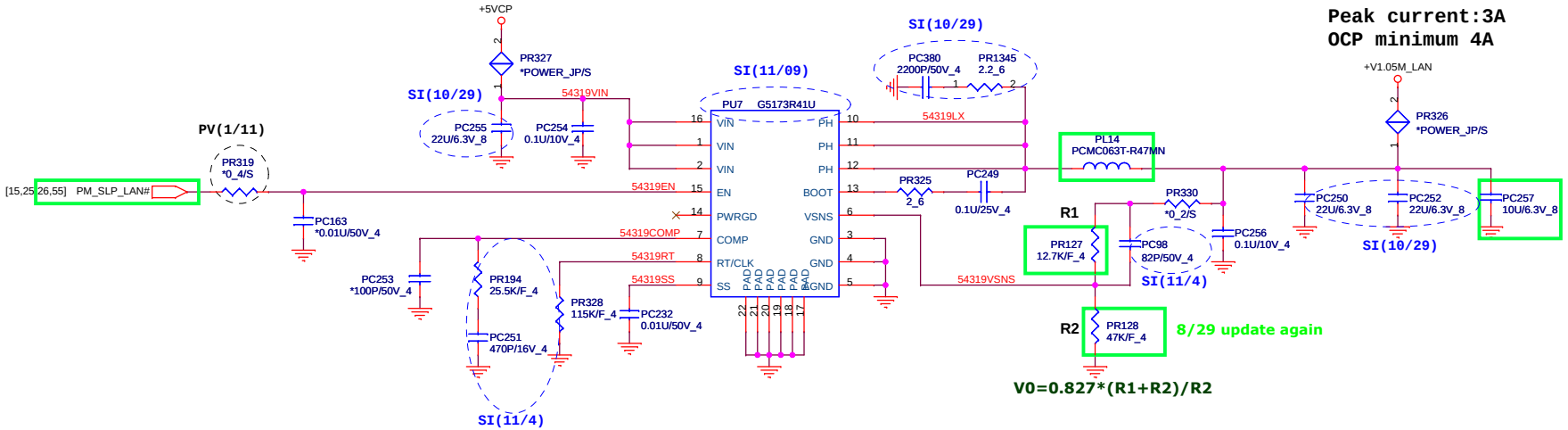
+1.05V_LAN +/- 5%
Countinue current:2.1A
Peak current:3A
OCP minimum 4A



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Size	Document Number	Rev
Custom	+1.05V_IAMT(RT8238A)	1A

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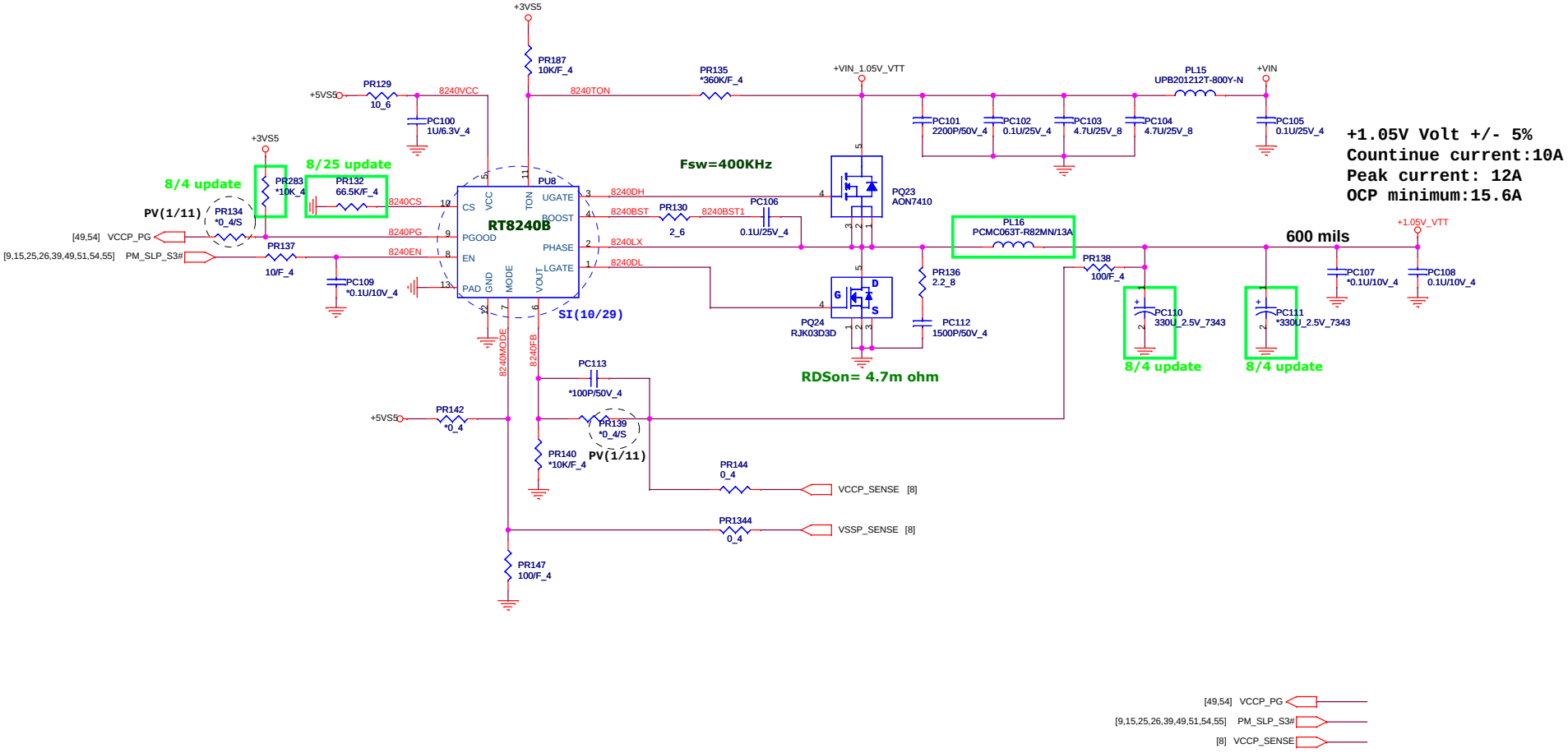

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Size	Document Number	Rev
Custom	+1.05V_VTT (RT8209A)	1A

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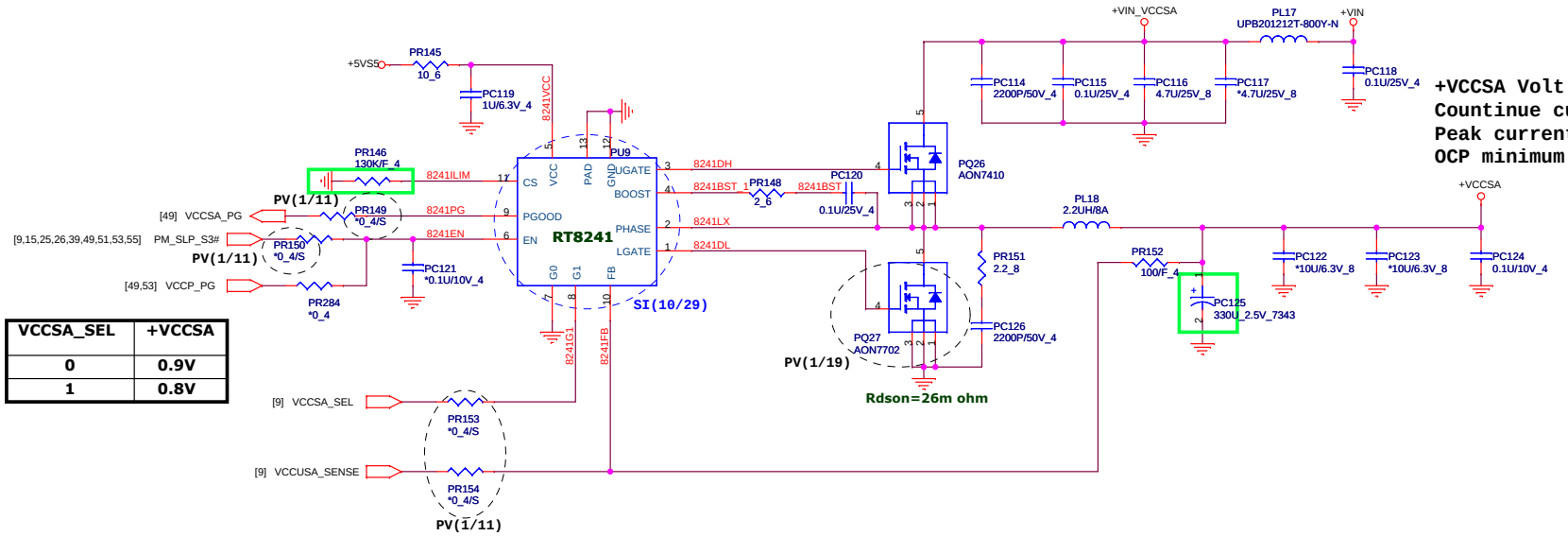
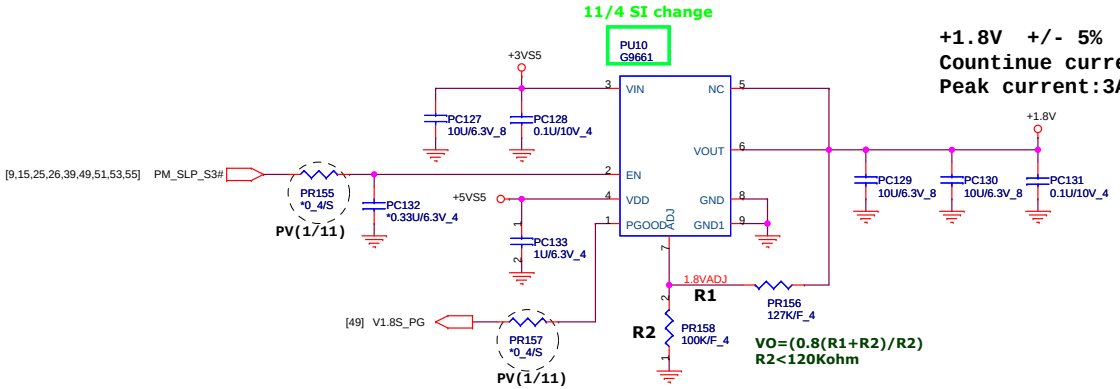


VCCSA_SEL	+VCCSA
0	0.9V
1	0.8V

+VCCSA Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7A

11/4 SI change



+1.8V +/- 5%
Countinue current: 2.0A
Peak current:3A

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Custom	VCCSA (RT8241A)	1A

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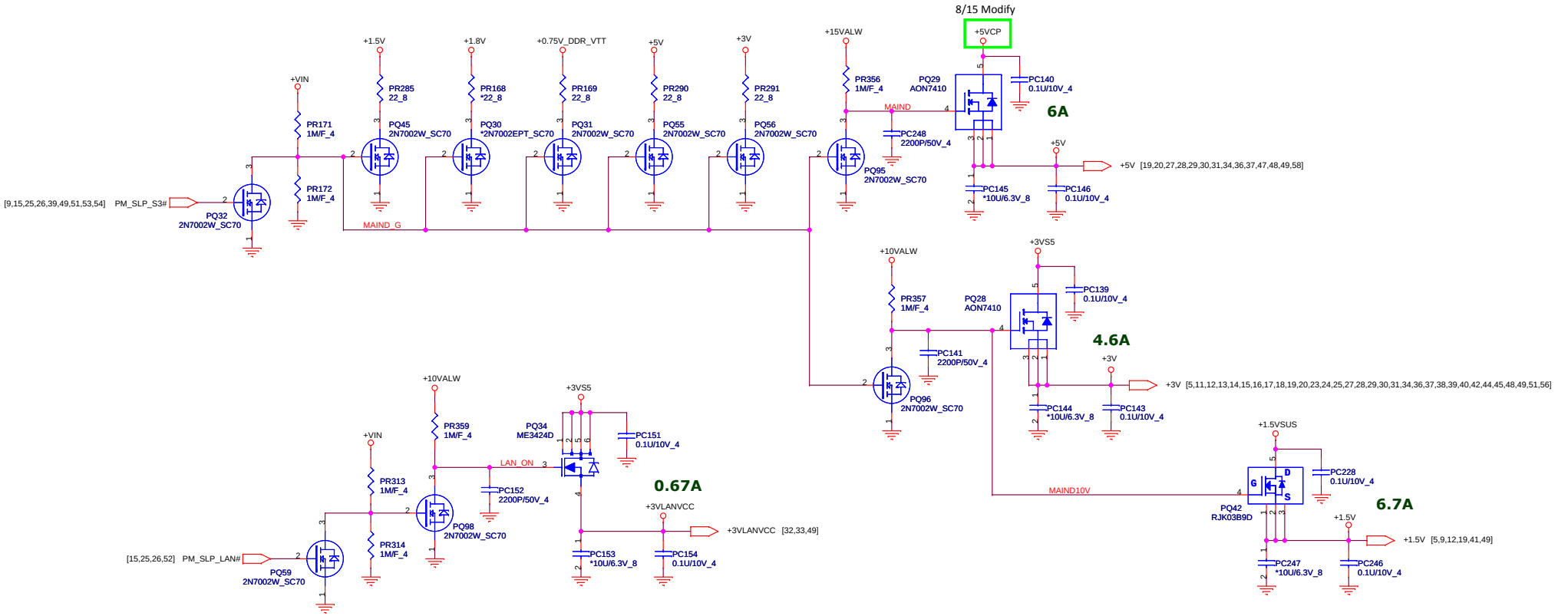

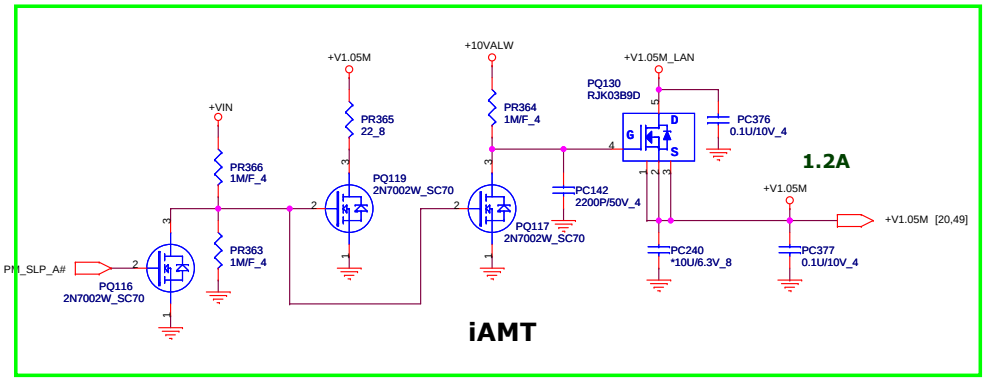

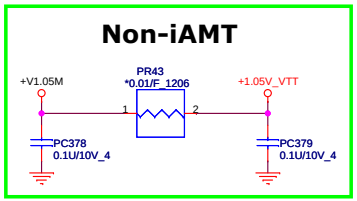

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Size	Document Number	Rev
Custom	Dis-charge IC (G5934)	1A

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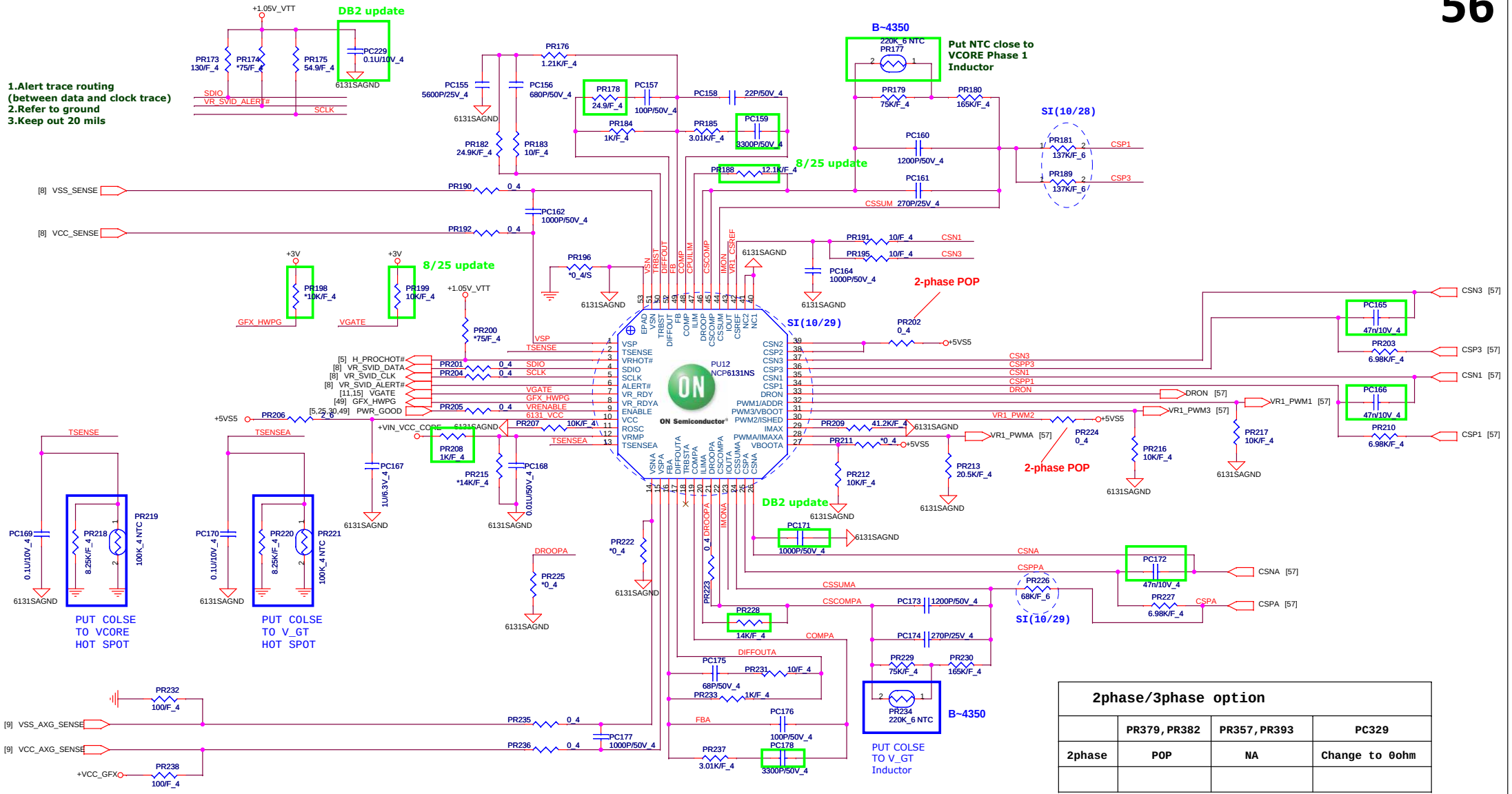

2phase/3phase option			
	PR379,PR382	PR357,PR393	PC329
2phase	POP	NA	Change to 0ohm

UMA(Switchable)/Discrete Only option			
	PC336,PC340 PC343,PC337 PC342	PR427,PR433,PR430,PR431,PR423,PR435 PC338,PR424,PR428,PR432,PC339,PC341 PR425,PR426,PR429,PR420,PR422,PR380 PR399,PR421,PC352,PR417,PR418,PC354 PC419	PR434,PR436 PR378
UMA	POP	POP	NA
Discrete	Change to 0 ohm	NA	POP

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Size	Document Number	Rev
Custom	CPU Core1 (NCP6131S)QC	1A

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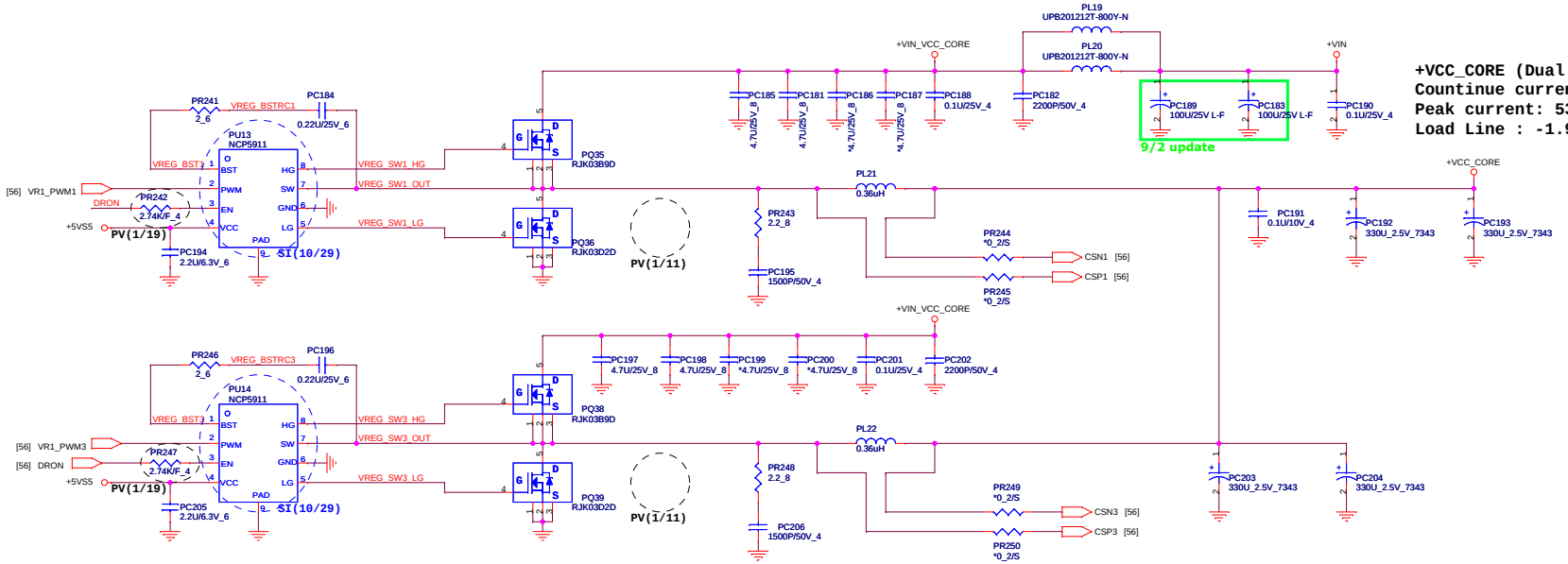

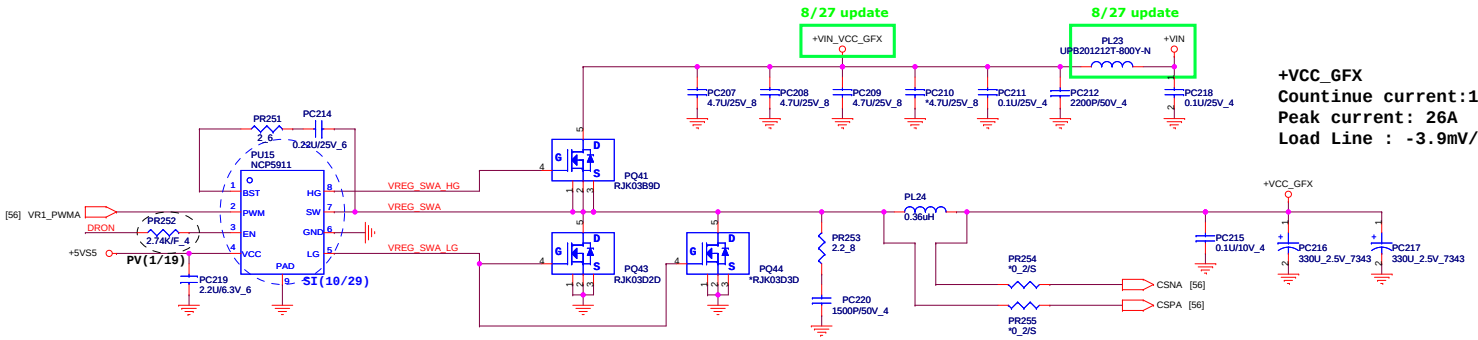

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Size	Document Number	Rev
C	CPU Core2 (NCP5911)QC	1A

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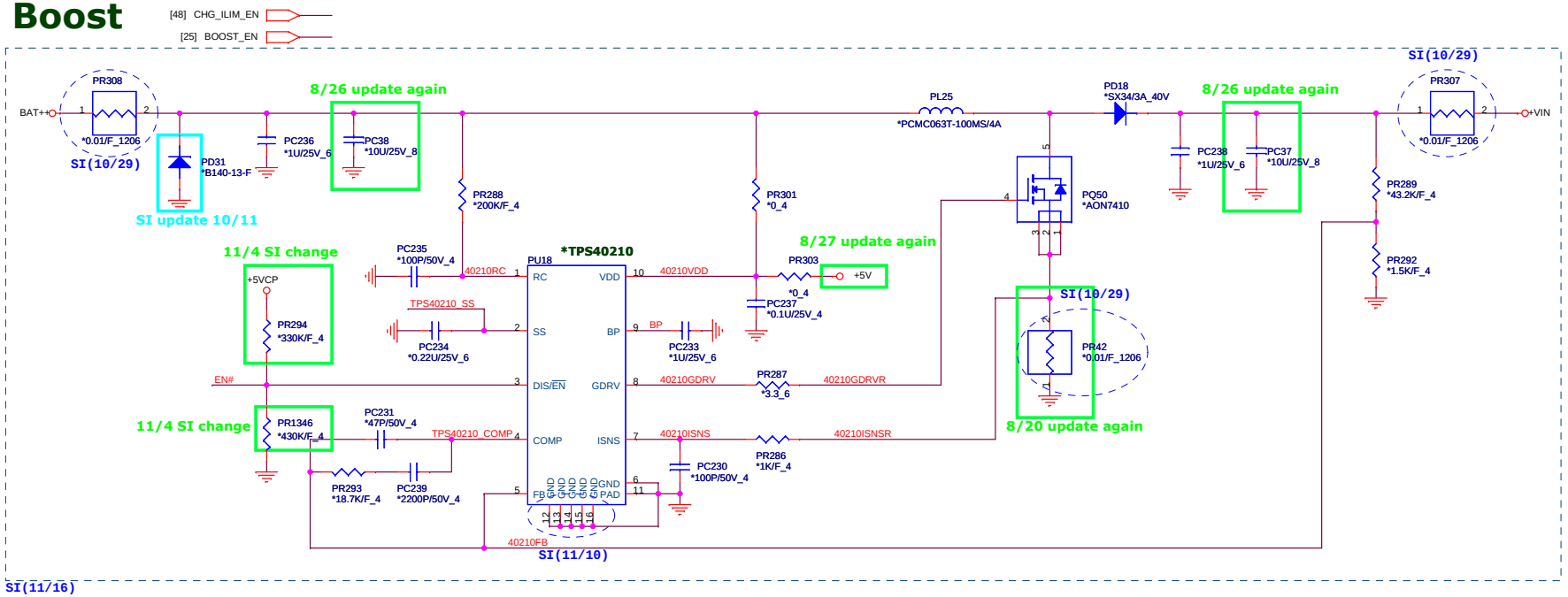
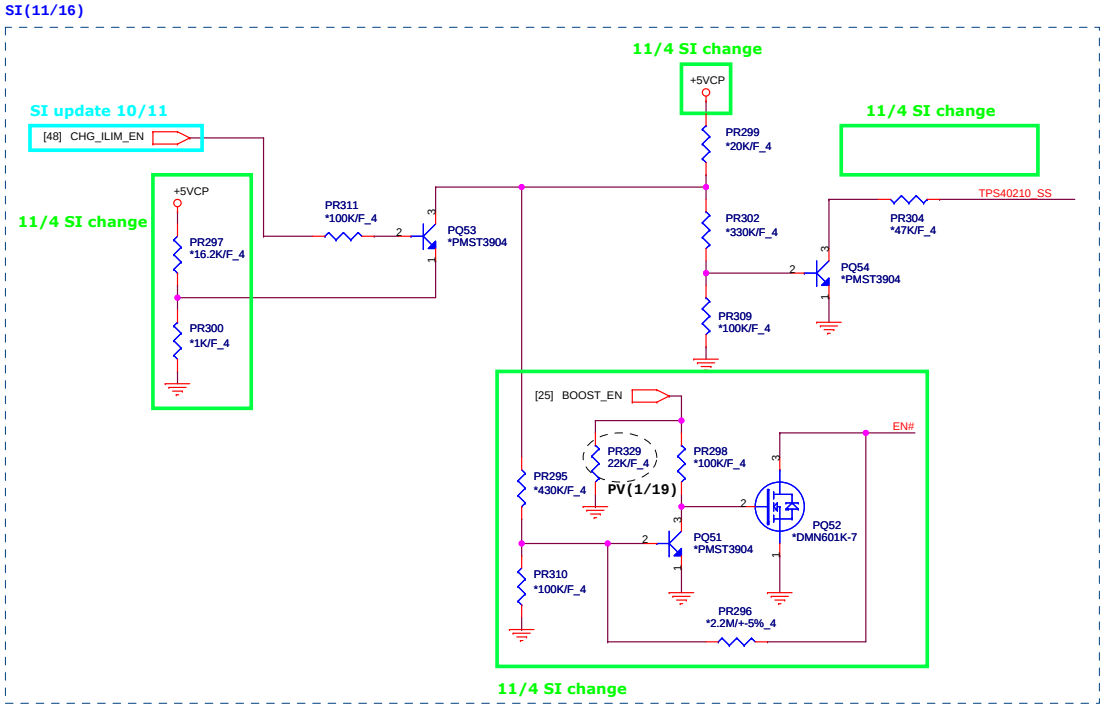
Turbo Boost





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Size	Document Number	Rev
Custom	CHARGERII	1A

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