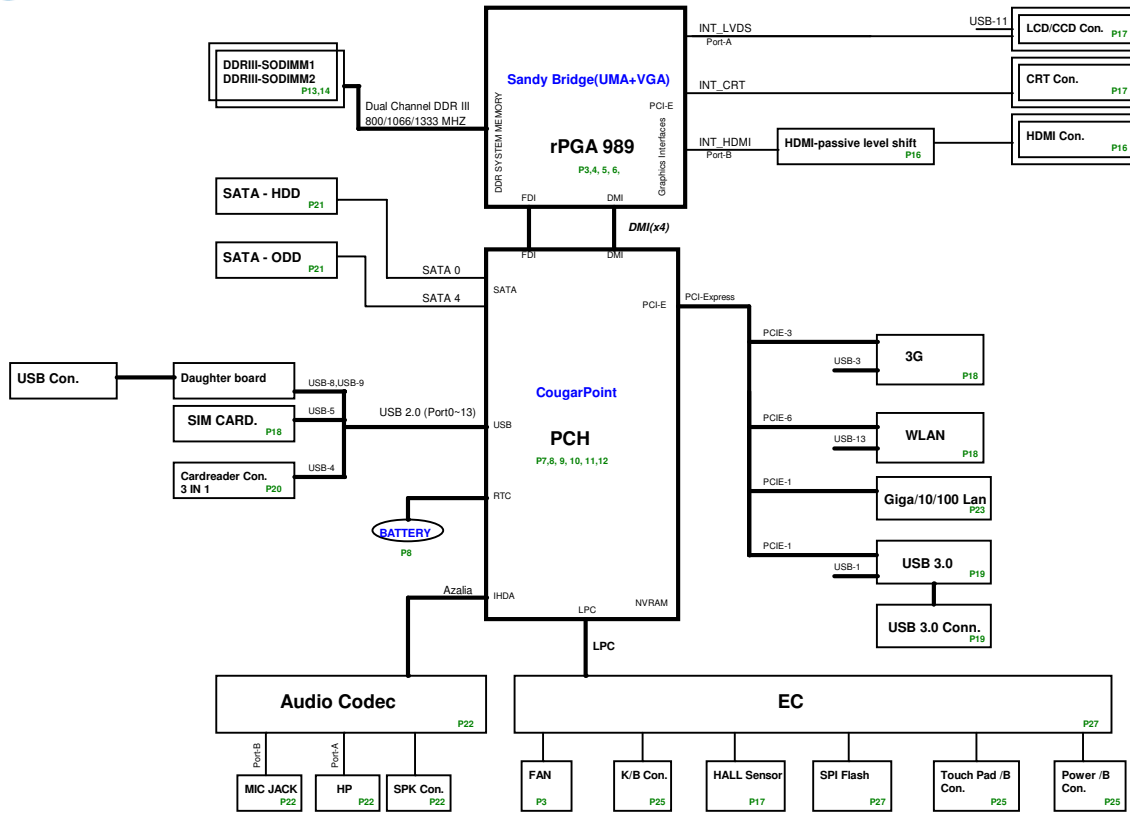


LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : SVCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT



BU5 Block Diagram

01



POWER SYSTEM

ISL88731C	P28
PM6686	P29
UP6163	P30
RT8240	P31
TPS51461	P32
ISL9583SHRTZ	P33
G966A	P34

+VCC_CORE

+1.5V

+1.5VSUS

+VTT

+1.05V

+1.8V

+1.5V_S5

+3VPCU

+3V_S5

+3V

+5VPCU

+5V_S5

+5V

+SMDDR_VTERM

+SMDDR_VREF

+VCCSA

Table of Contents

PAGE	DESCRIPTION	BOI-FUNCTIONS
1	Schematic Block Diagram	
2	Front Page	
3-6	Processor	CPU
7-12	PCH	CLG
8	RTC	RTC
13-14	DDRIII SO-DIMM	DDR
17	VGA Connector	VGA
16	LCD Panel	LDS
	CRT & CRT BUS SWITCH	CRT
	CCD	CCD
	HALL SENSOR&BACK LIGHT SWITCH	HSR
19	Display Port	DPP
20	HDMI comm part	HDM
	HDMI for GM	HMG
21	SATA ODD	ODD
	Main SATA HDD & 2nd SATA HDD	HDD
	G-Sensor	H3D
22	5 IN 1 Card reader	MMC
	IEEE1394	FW
23	MINI Card (Wi-Fi & WIMAX)	WLN
	MINI Card 2nd	MNC
	MINI Card 3rd	MNC
	TMA Connector	TMA
24	INT KeyBoard & K/B LED Power	KBC
	LED Board	LED
	TP&FP board	TPD,FPD
	Bluetooth Connector	BTM
	Felica Connector	FEC
	MMB Connector	MMB
	Power SW	PSW
	B-CAS Connector	BCS
25	New Card (Express Card)	EXC
	E-SATA comb USB	ESA
	USB Connector	USB
	Audio & USB Board	USB,ADO
	Light Sensor	LSN
	Satellite LED	LED
	RF LED / WIMAX LED / Kill SW	KSW
26	EC WP8763LDG/WPC8769L(O)	KBC
	CIR	CIR
27	Codec (CX20583)	ADO
28	FM Tunner	FMM
	Modem Connector	MDM
	HOLE	
29	Atheros LAN	LAN
30	NVRAM Connecytor	NVR
31	Charger (ISL6251A)	PWM
32	System 5V/3V (ISL6237)	PWM
33	CPU CORE (ISL62882)	PWM

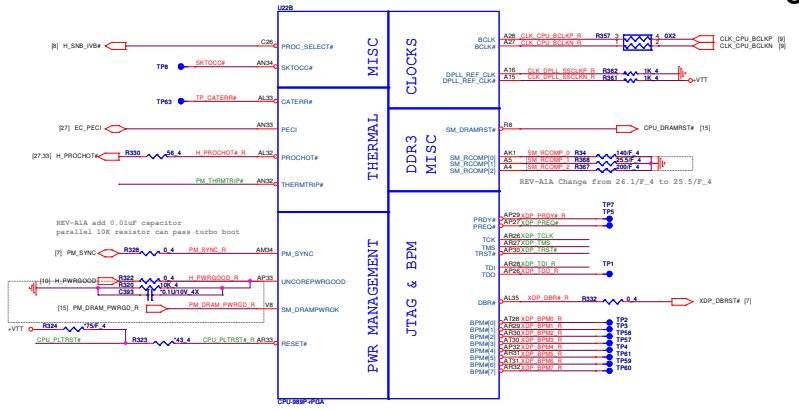
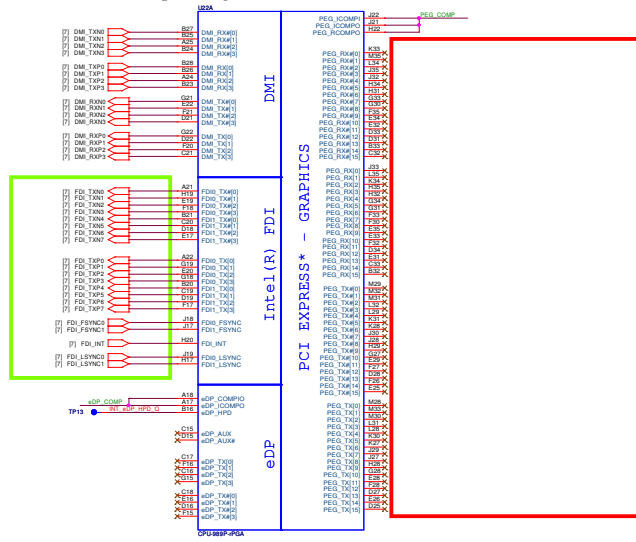
POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0-S5
+VCCRTC	+3.0V~+3.3V		S0-S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0-S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0-S5
+5VPCU	+5V	AC/DC Insert enable	S0-S5
+5V_TMA	+5V	MAIN_ON	S0
WIMAX_P	+3.3V	WMAX_P for EC	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_S5	+1.5V	S5_ON	S0-S5
+1.5V_SUS	+1.5V	SUSON	S0-S3
+VCC_CORE		VRON	S0
+VTT	+1.05V~+1.1V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		GFXVR_EN	S0

GND PLANE	PAGE
 GND_SIGNAL	32
 CARD_GND	21
 AGND_DC/DC	31
 GND	ALL

ITEM	Value Code	FUNCTIONS
1	EV@	DISCRETE
2	IV@	UMA
3	U3@	USB 3.0
4	U2@	USB 2.0 (colay W USB 3.0)
5	HM@	HDMI
6	IHM@	Internal HDMI
7	EHM@	External HDMI
8	3G@	3G
9	C@	Cost issue
10	MDC@	Modem
11	S3@	S3 Power Reduction
12	NS3@	No S3 Power Reduction
13	E@	EMI
14	51@	1G LAN
15	52@	10/100 LAN
16	GS@	G-SENSOR
17	NGS@	No G-SENSOR

PAGE	DESCRIPTION	BOI-FUNCTIONS
34	VAXG (ISL62881)	PWM
35	+VTT (UP6111A)	PWM
36	+1.05V (UP6111AQDD)	PWM
37	DDR 1.5V (TPS51116)	PWM
38	Discharge (1.5V_S5/1.8V)	PWM
39	Power Tree Table	
40	PCH Power Plane	
41	Power Management	
42	Change List	

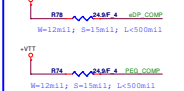
Sandy Bridge Processor (DMI, PEG, FDI)



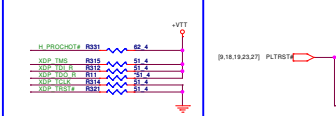
FDI Disabling (Discrete Only)
<CPU>



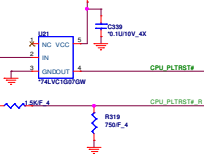
DP & PEG Compensation



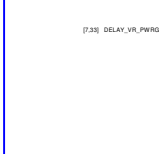
Processor pull-up <CPU>	Level Shift <CPU>
-------------------------	-------------------



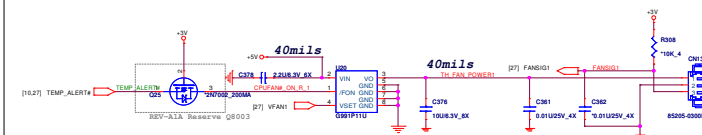
+3V_{SS}



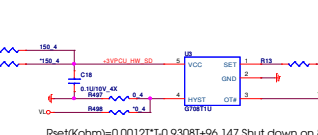
Thermal Trip<CPU>



FAN Control-->For one FAN solution <THC>

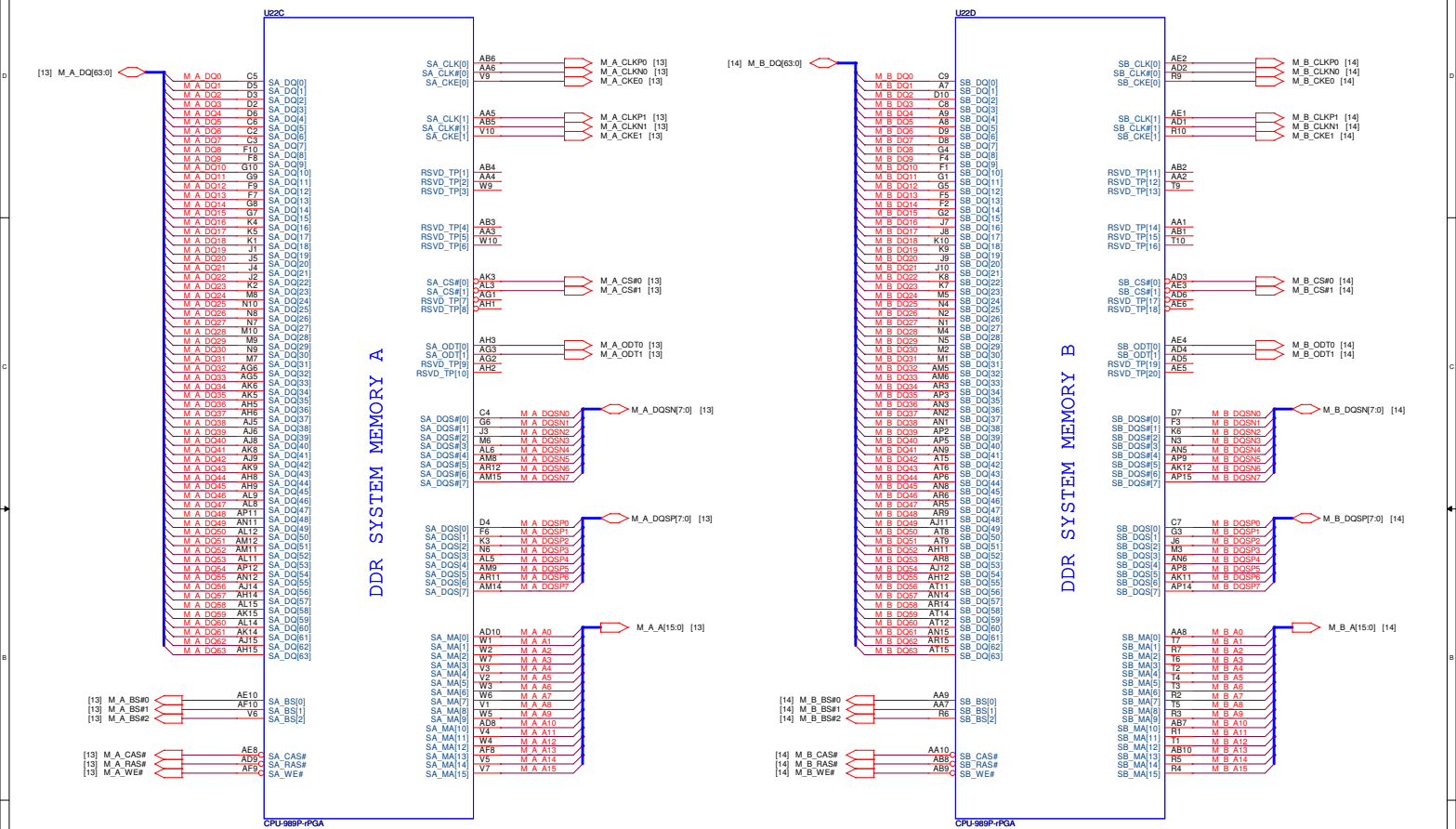


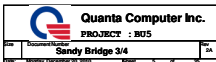
CPU Thermal sensor / MB Local TEMP <THC>

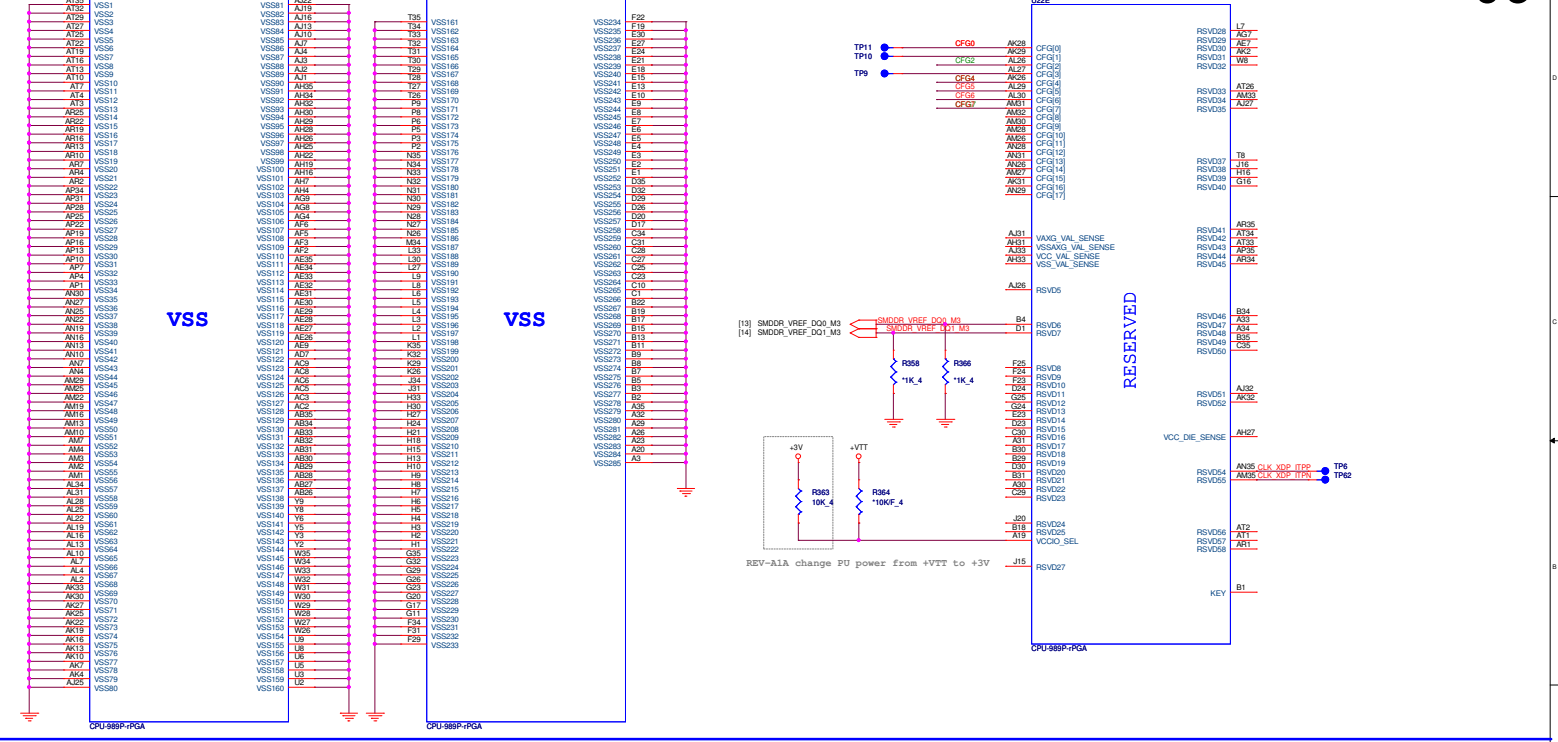


REV-C3A Change VCC PIN5 of U3 from +3VPCU to V2
Add R496,R497,R499
Reverse R14,R498,R31,R24,Q3

Sandy Bridge Processor (DDR3)







Processor Strapping

The CFG signals have a default value of "1" if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB of assertion	PEG wait for BIOS training

REV-A1A change PU power from +VTT to +3V

CFG6 [6.5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled; function 2 disabled
01: Reserved - (Device 1 function 1 disabled; function 2 enabled)
00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

REV-A1A change to 5% tolerance

CFG6 [6.5] (PCIe Port Bifurcation Straps)

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10: x8, x8 - Device 1 function 1 enabled; function 2 disabled
01: Reserved - (Device 1 function 1 disabled; function 2 enabled)
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REV-A1A change to 5% tolerance

CFG6 [6.5] (PCIe Port Bifurcation Straps)

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01: Reserved - (Device 1 function 1 disabled; function 2 enabled)
00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

Quanta Computer Inc.

PROJECT :BU5

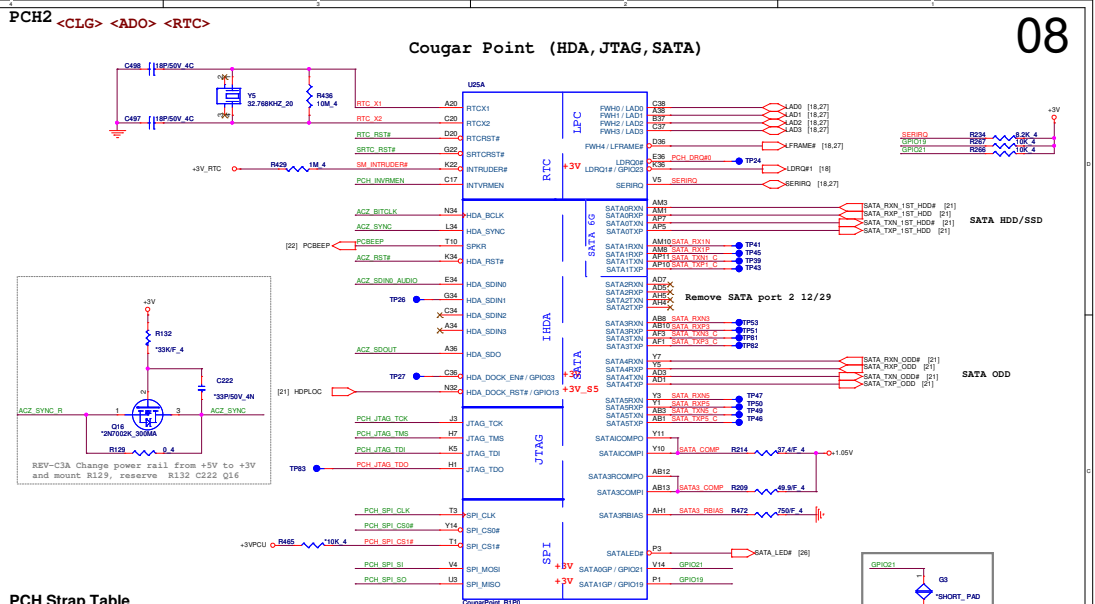
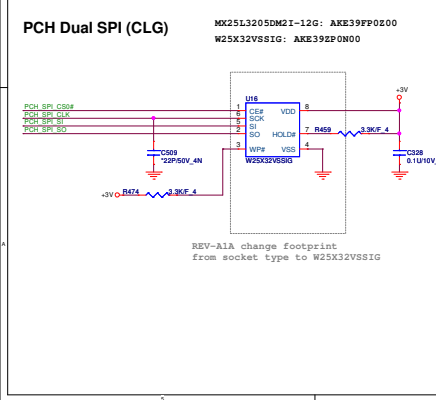
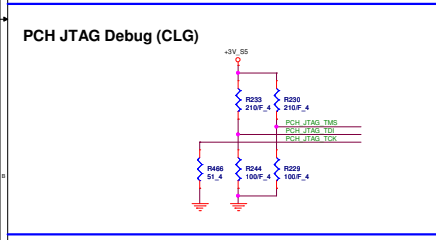
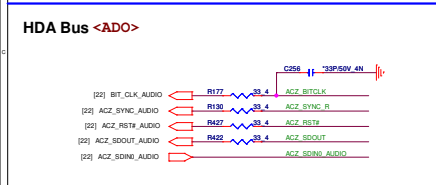
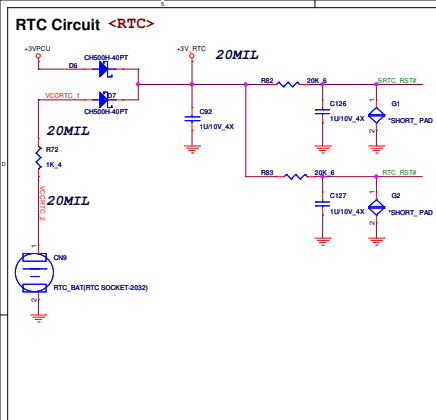
Sandy Bridge 4/4

Monday, December 25, 2010

Print 6 of 35

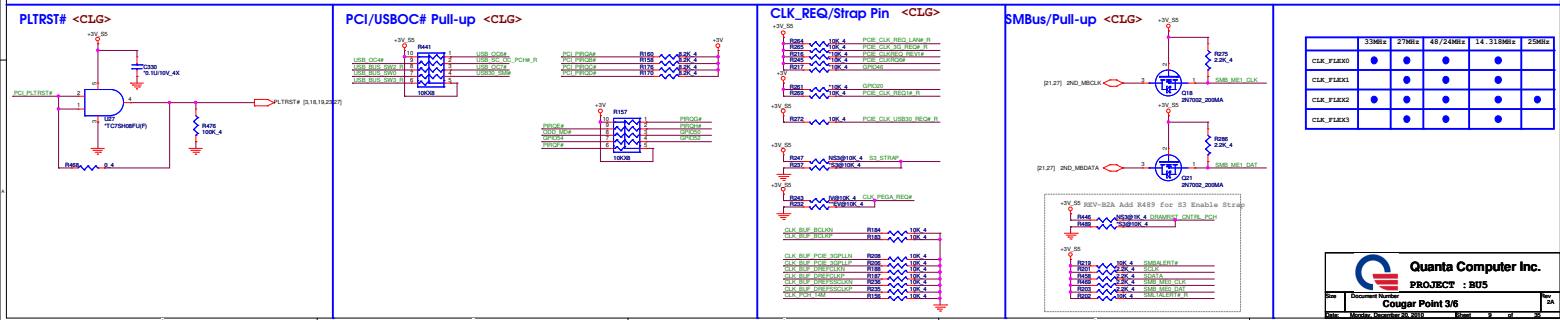
Cougar Point (LVDS,DDI)


Quanta Computer Inc.
PROJECT : BU5
Cougar Point 1/6
 Date: Monday, December 23, 2016 Sheet: 7 of 36



Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V0 R238 10K.4 PCBEEP									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R463 10K.4 PCI_GNT3# [9]									
INTRVMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R438 200K.4 PCH_INVRMEN									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>GNT1#</th><th>GPIO19</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></tbody></table>	GNT1#	GPIO19	Boot Location	1	1	SPI *	0	0	LPC	R399 10K.4 GNT1# [9] R478 10K.4 GPIO19
GNT1#	GPIO19	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK											
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V0 R429 10K.4 ACZ_SDOOUT ACZ_SDOOUT [27]									
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R463 200K.4 DF_TVS [10] R464 10K.4 H_SNB_VB# [5]									
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	+3VPCU R222 10K.4 PLL_ODDVR_EN [10]									
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_R50 R138 10K.4 ACZ_SYNC									
GPIO15	TLS Confidentiality	RSMRST	0 = Default: TLS no Confidentiality 1 = TLS Confidentiality	+3V_R50 R465 1K.4 GPIO15 [10]									
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	+3V_RTC R443 300K.4 DSWVRMEN [7]									
INIT3_3V#	Reserved	PWROK	1 = Default (weak pull-up 20K)	Should not pull low, leave as No Connect									
GNT2# / GPIO53	ESI Strap (Server Only)	PWROK	1 = Default. Should not be pulled low for desktop and mobile	Should not pull low for desktop and mobile									
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected	1 = PU to 3V									
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected	1 = PU to 3V									
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC									
DDPD_CTRLDATA	Port D Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC									
SATA3GP / GPIO37	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled									
SATA2GP / GPIO36	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled									

Cougar Point-M (PCI-E, SMBUS, CLK)

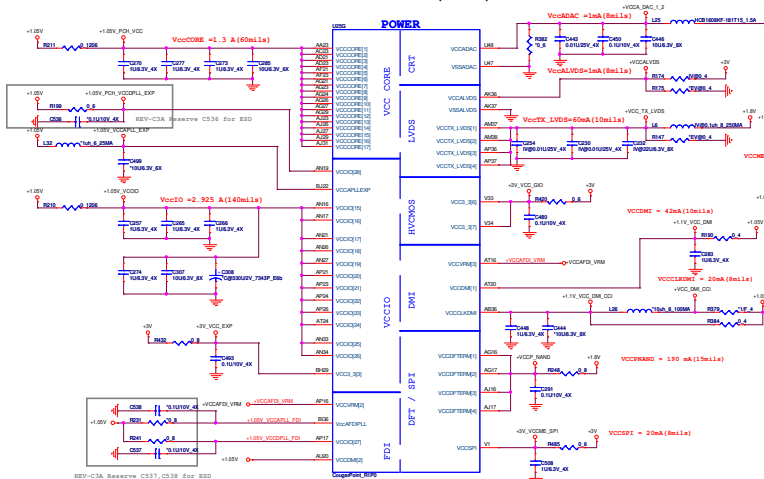


 **Quanta Computer Inc.**
PROJECT : BU5
 Size Document Number Cougar Point 3/6 Rev 2/8
 Date: Monday, December 20, 2010 Sheet 9 of 30

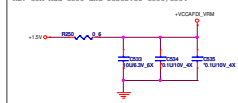


 Quanta Computer Inc. PROJECT : BU5	
Size	Document Number Cougar Point 4/6
Date: Monday, December 20, 2010	Sheet 10 of 35 Rev 2A

COUGAR POINT (POWER)



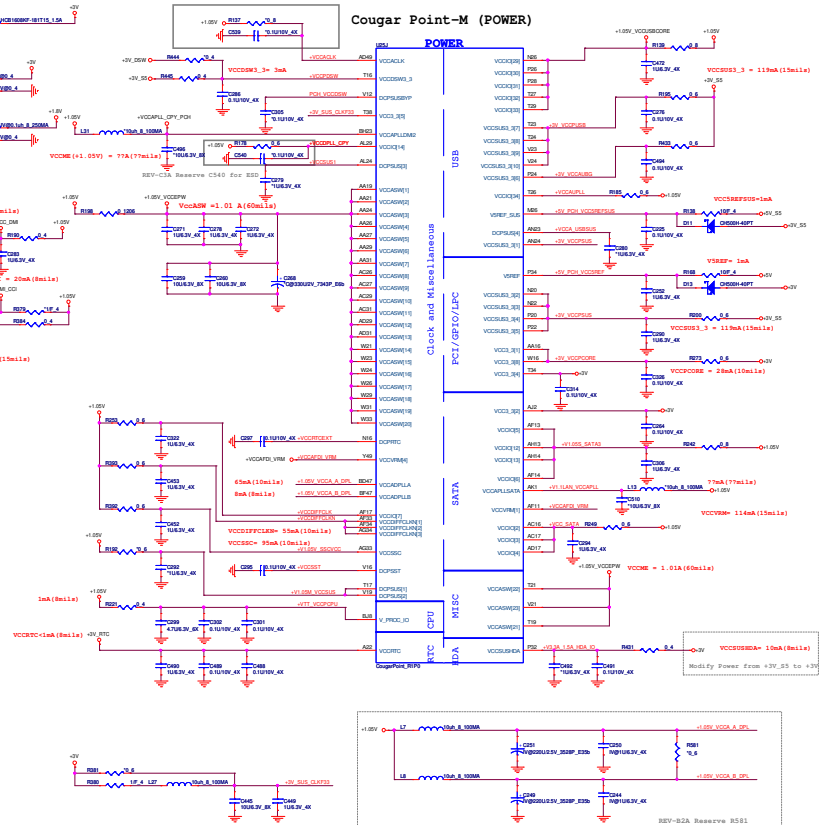
REV-C3A Add C533 and resistor C535, C534



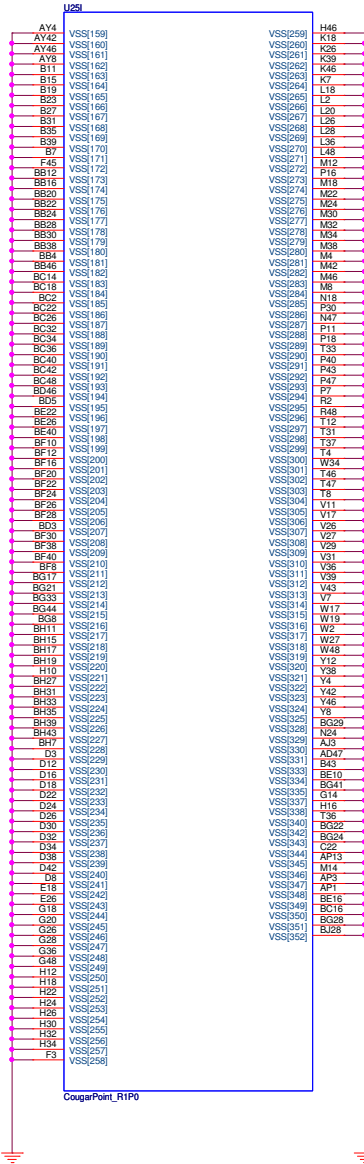
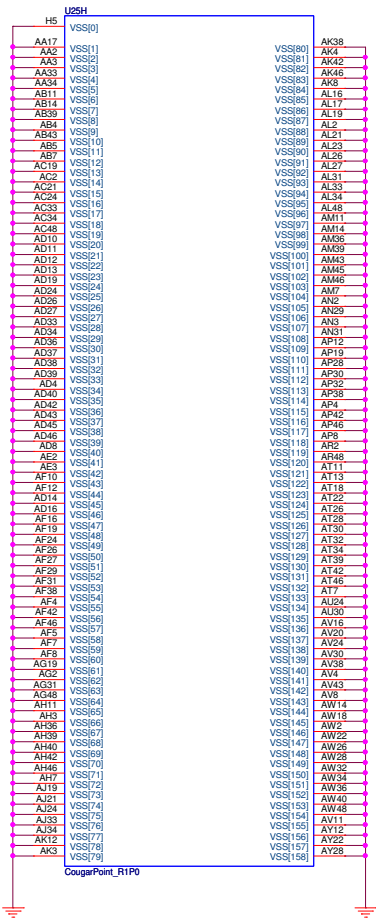
REV-C3A Reserve D23

REV-C3A Reserve C539 For B20

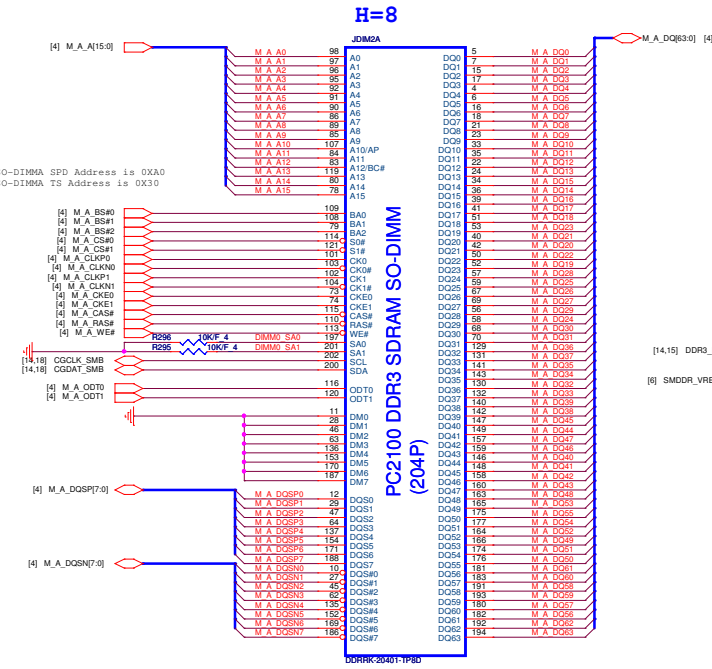
Cougar Point-M (POWER)



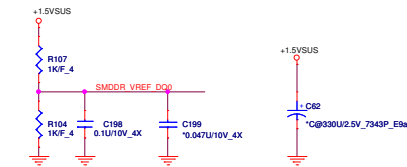
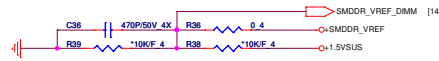
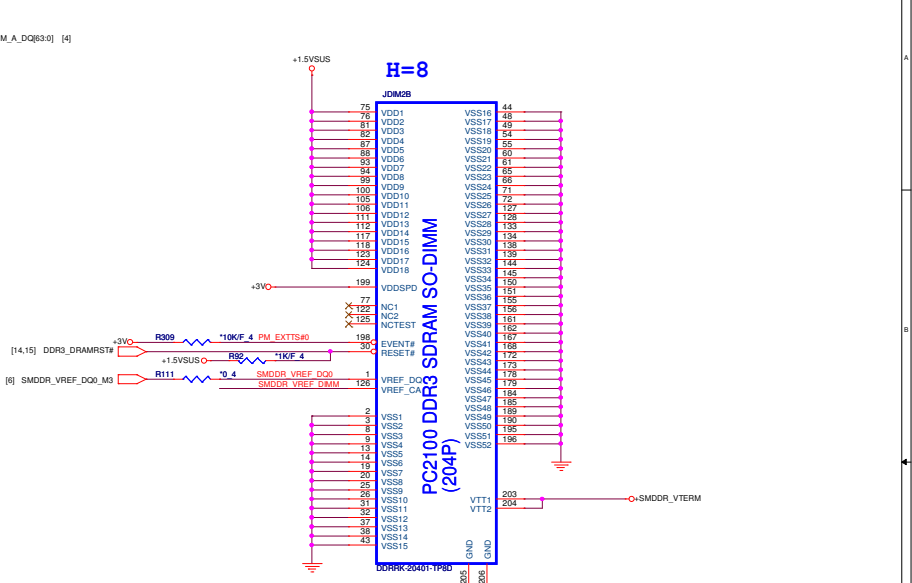
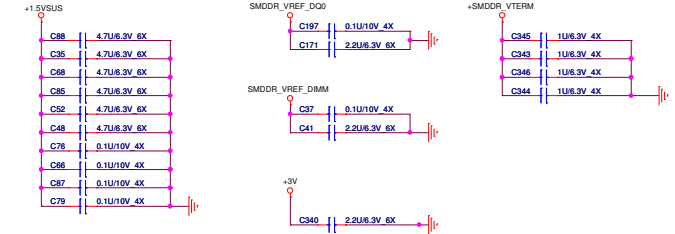
IBEX PEAK-M (GND)



<DDR>



Place these Caps near So-Dimm0.



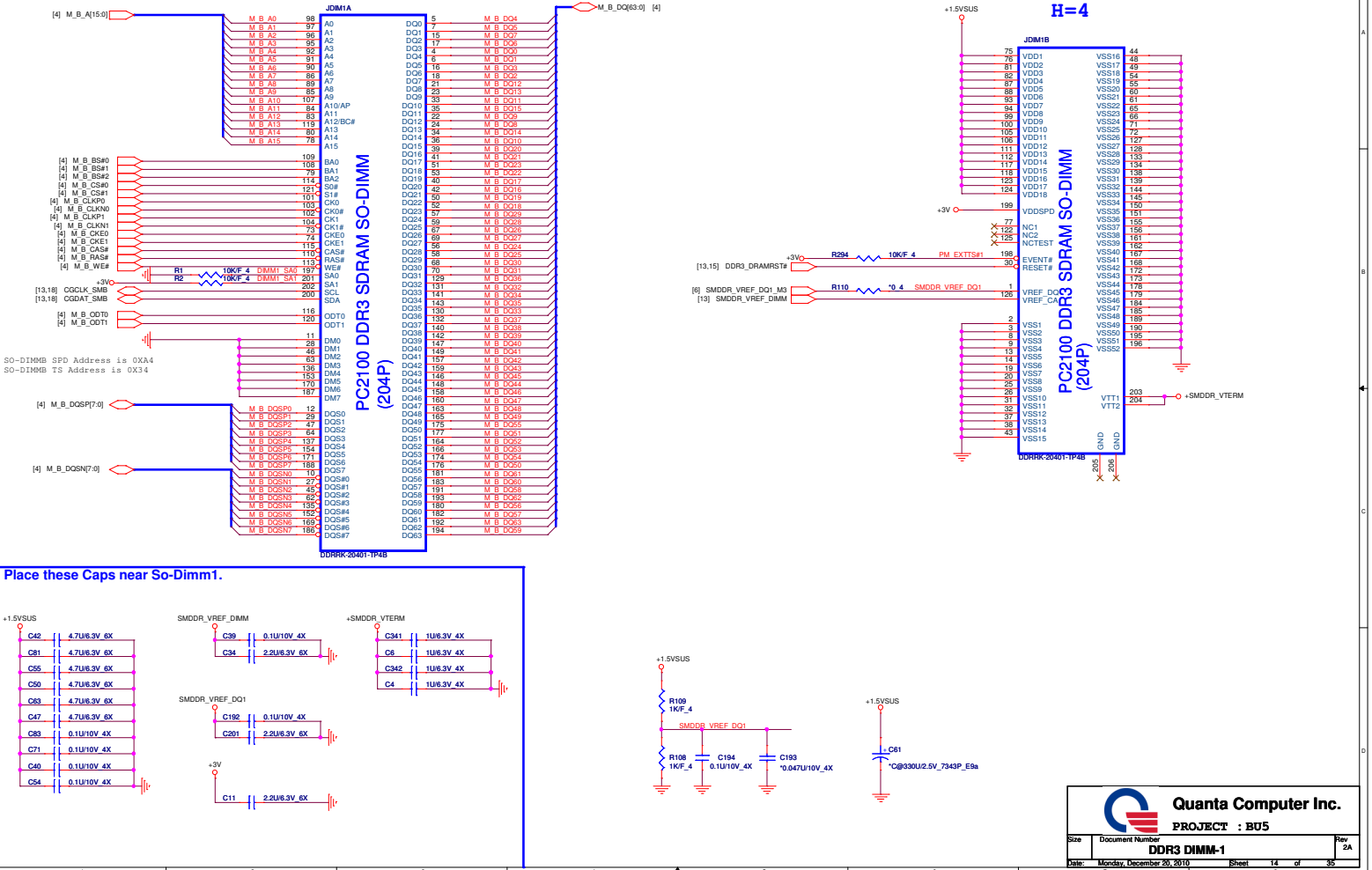


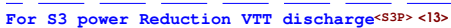
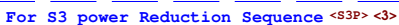
Quanta Computer Inc.
PROJECT : BU5

Size	Document Number	Rev
DDR3 DIMM-0		2A
Date:	Monday, December 20, 2010	Sheet 13 of 35

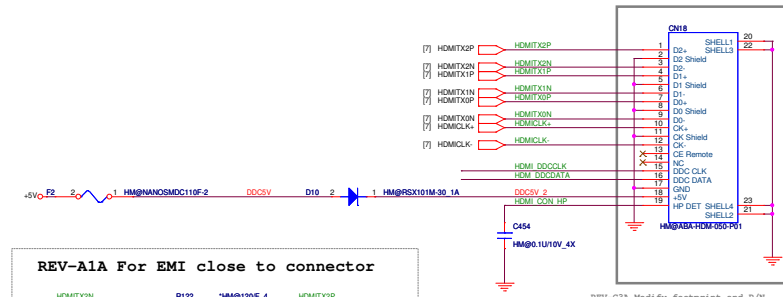
H=4

H=4





HDMI Conn <HDM>

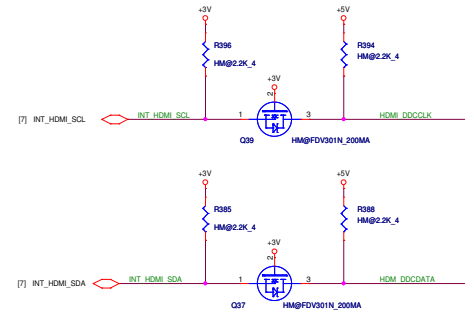


REV-A1A For EMI close to connector

HDMITX2N	R125	100k	HDMITX2P
HDMITX1N	R126	100k	HDMITX1P
HDMITX0N	R134	100k	HDMITX0P
HDMICLK+	R128	100k	HDMICLK-

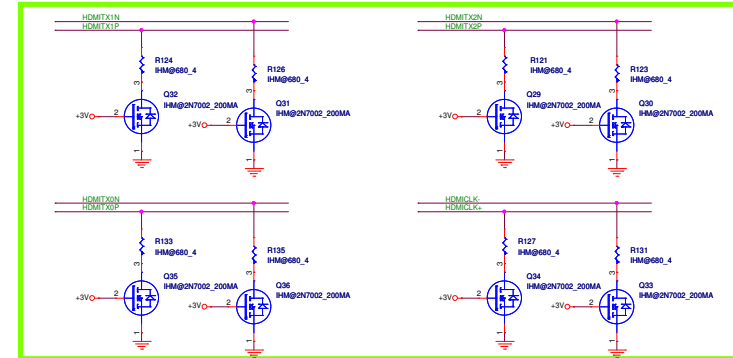
REV-C3A Modify footprint and P/N
Add pin22, pin23

HDMI-SMBus <HDM>

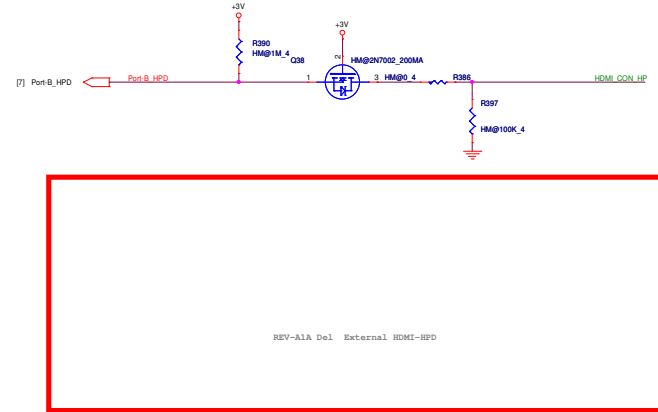


REV-A1A Nvidia Comment +3V_GFX to instead of +3V
as below power rails to avoid power leakage issue

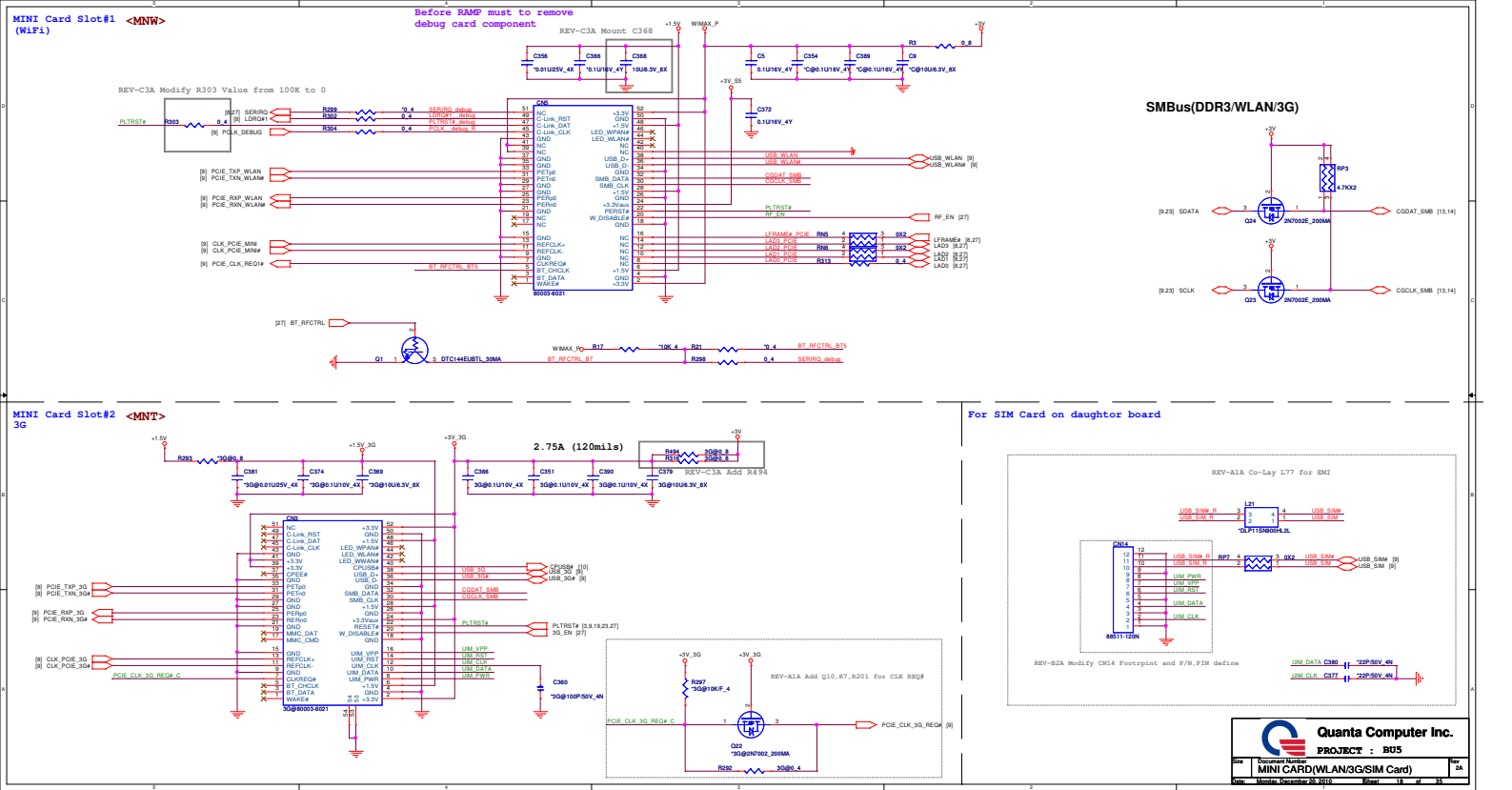
HDMI-passive level shift <HDM>

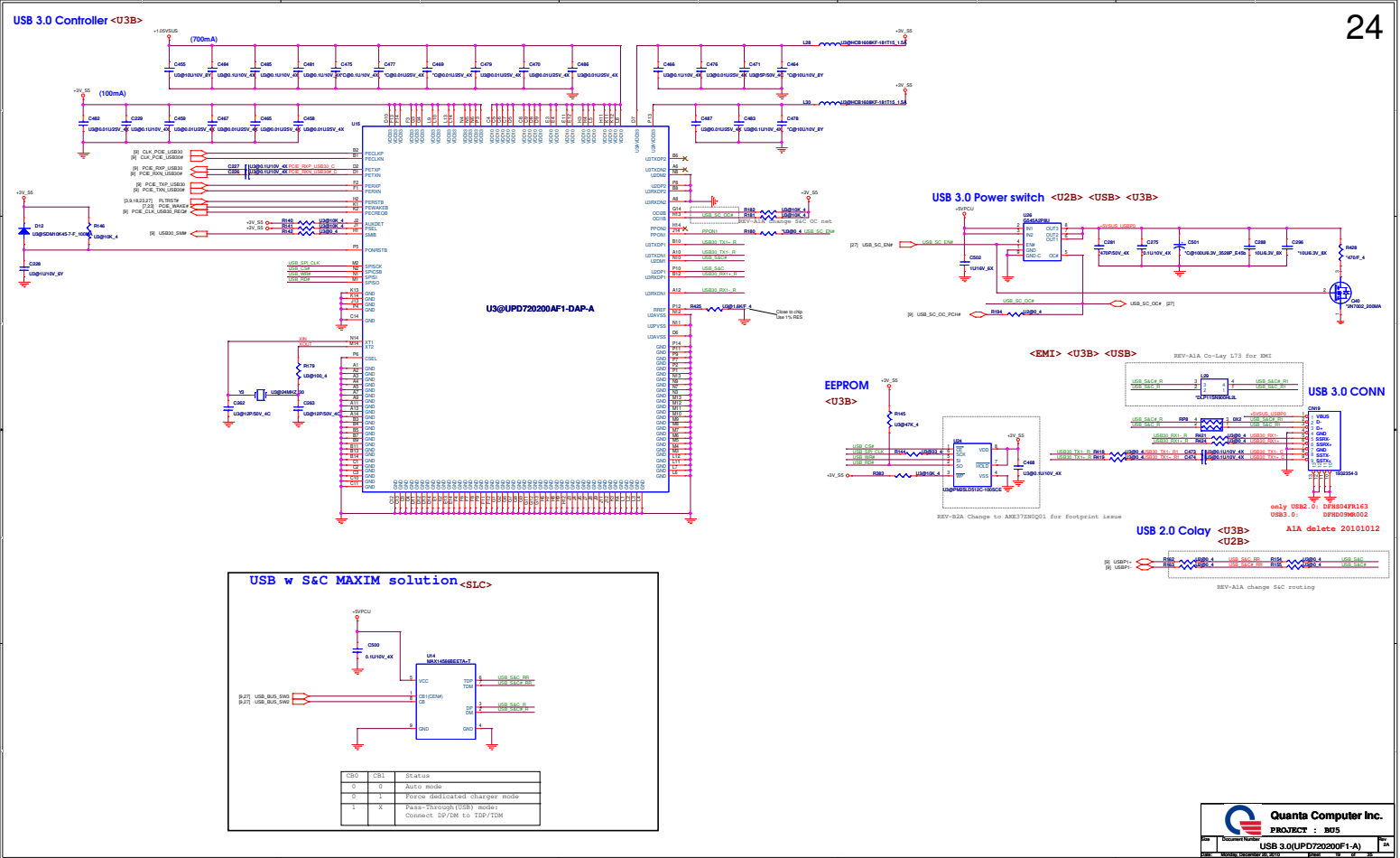


HDMI-HPD <HDM>

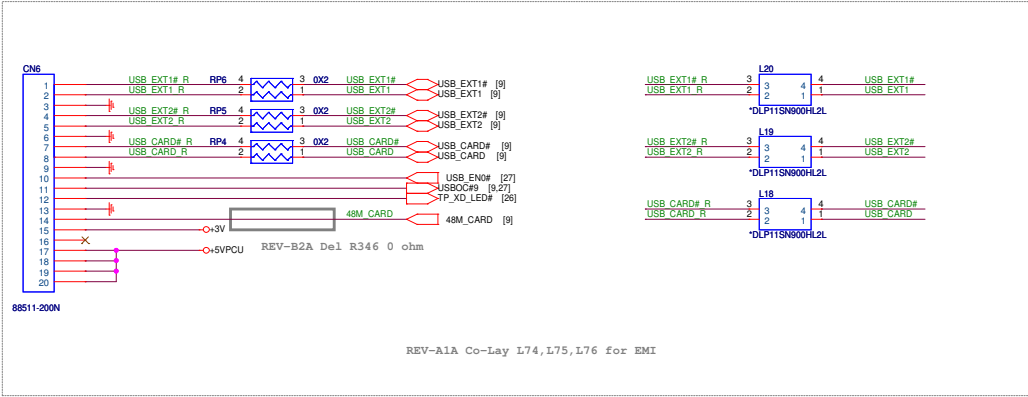


REV-A1A Del External HDMI-HPD





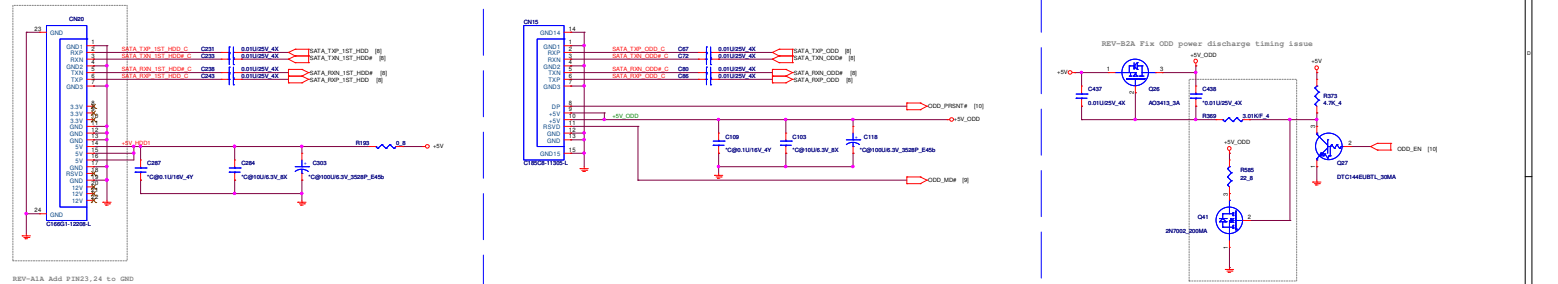
USB2.0 Left 1
USB2.0 Left 2 <U2B> <MMC> <USB> <EMI>



HDD Interface <H1D>

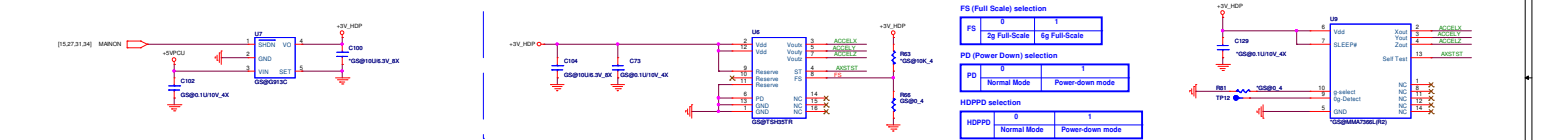
ODD Interface <ODD>

ODD Zero power . (Only for Intel) <OZP>



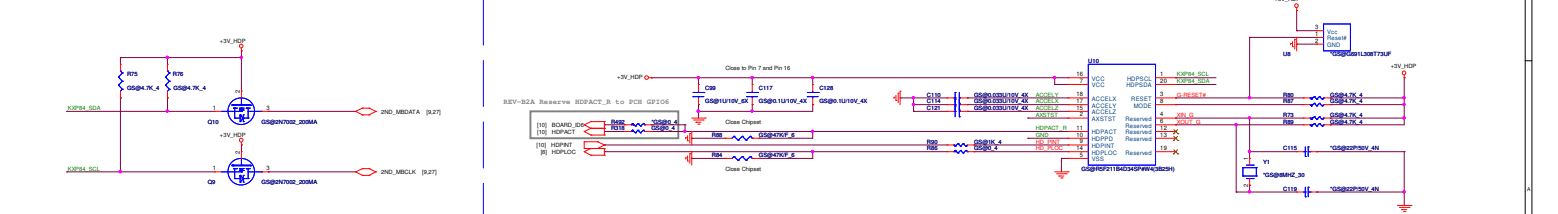
3D-LDO Power <GSR>

3D-Sensor IC <GSR>

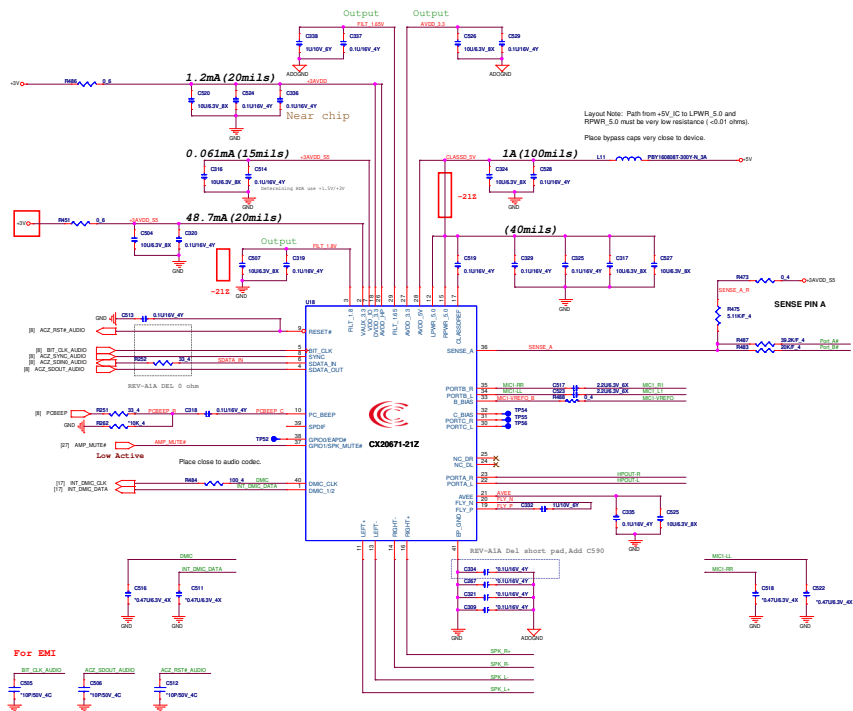


3D-SMBus <GSR>

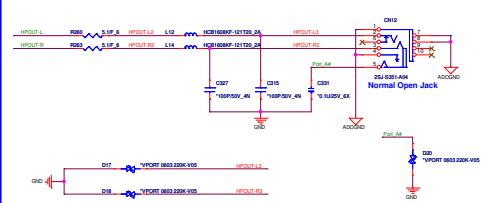
3D-u-micro P <GSR>



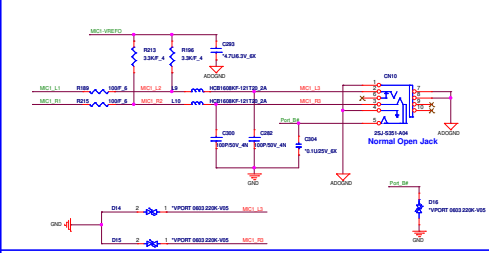
Codec (CX20671-21Z) <ADO> <EMI>



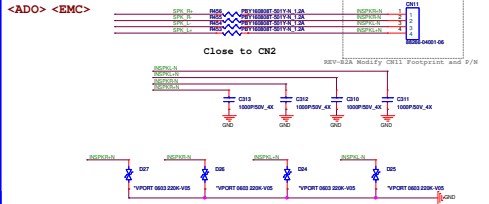
HP <ADO> <EMC>

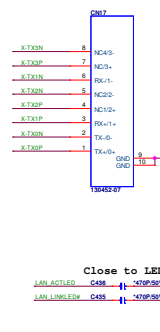
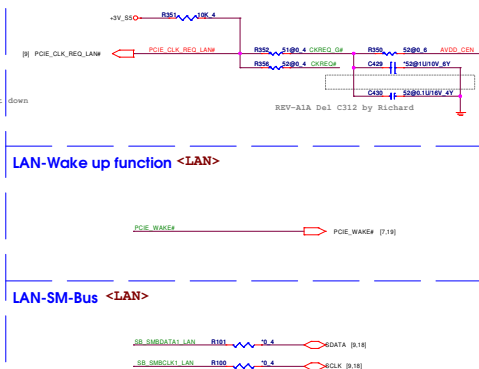


External MIC <ADO> <EMC>



Internal Speaker





LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SNR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
	1	Normal function
CKREQ# or CKREQ_#	0	ATE test mode

Power on Strapping pin

LAN_UNKLED#

+3V_S5

R335 5.1K

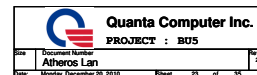
R355 5.1K

5.1K

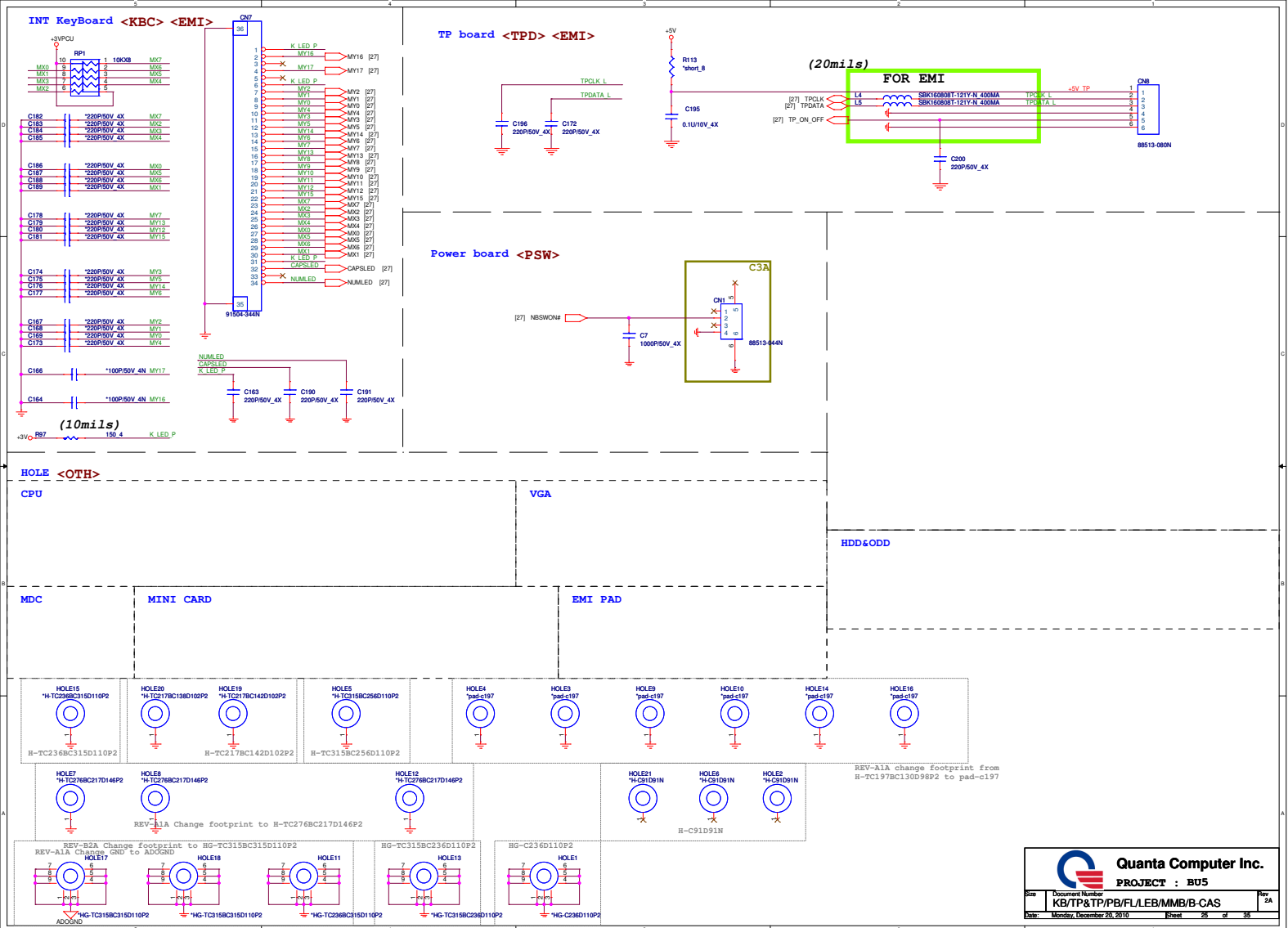
R334 5.1K

R354 5.1K

5.1K

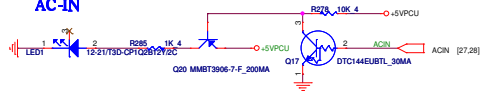






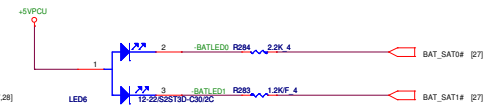
LED <LED>

AC-IN



BATTERY

D3A : LED luminance to light,15-ohm change 2.2K-ohm.

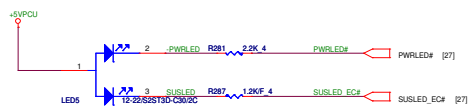


RF LED

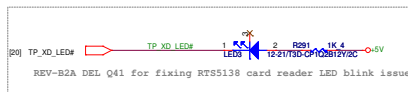


POWER

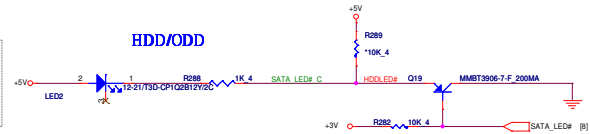
D3A : LED luminance to light,15-ohm change 2.2K-ohm.



CARDREADER

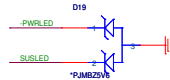


HDD/ODD

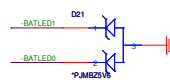


ESD Protect <EMC>

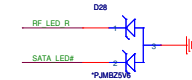
FOR POWER LED



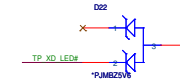
FOR BATTERY LED



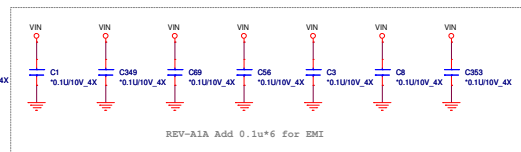
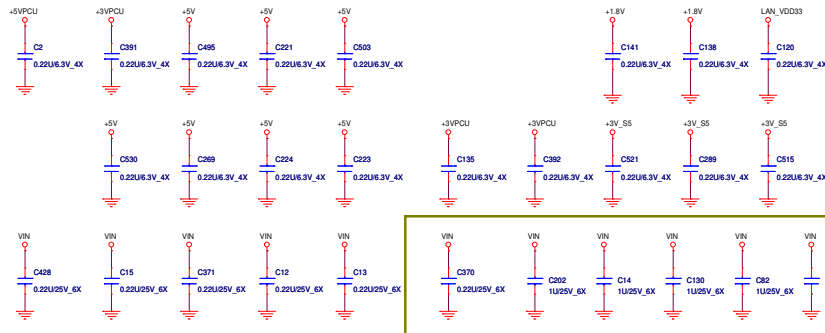
FOR HDD/W-LAN LED



FOR 3G/CARDREADER LED



<EMI>



REV-A1A Add 0.1u*6 for EMI



Quanta Computer Inc.

PROJECT : BU5

Size	Document Number	Rev
LED/HOLE		2A
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SMBUS	Devices
1	Buttons

1	Battery	12H
2	CPU Board Thermal Sensor	
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H

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13MS  UMA = 000
13MS  UCB = 001

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