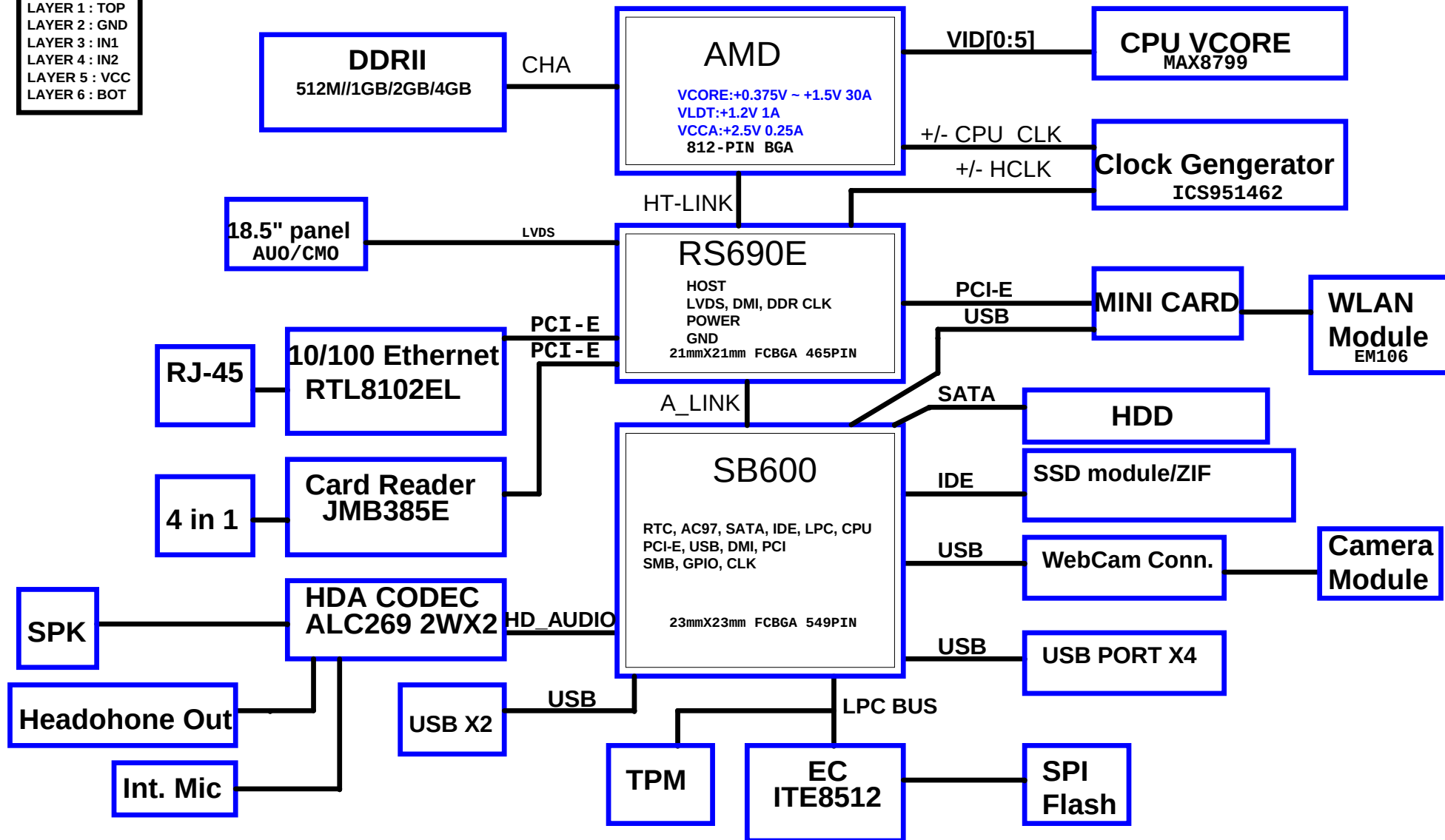


PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

BENQ(EL3) LCDPC Block Diagram

Quanta Computer Inc.

PROJECT : BENQ

Size

Document Number

Rev

Block Diagram

1A

Date: Tuesday, January 06, 2009

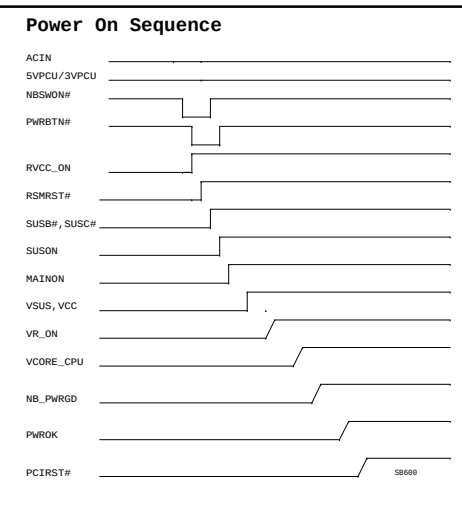
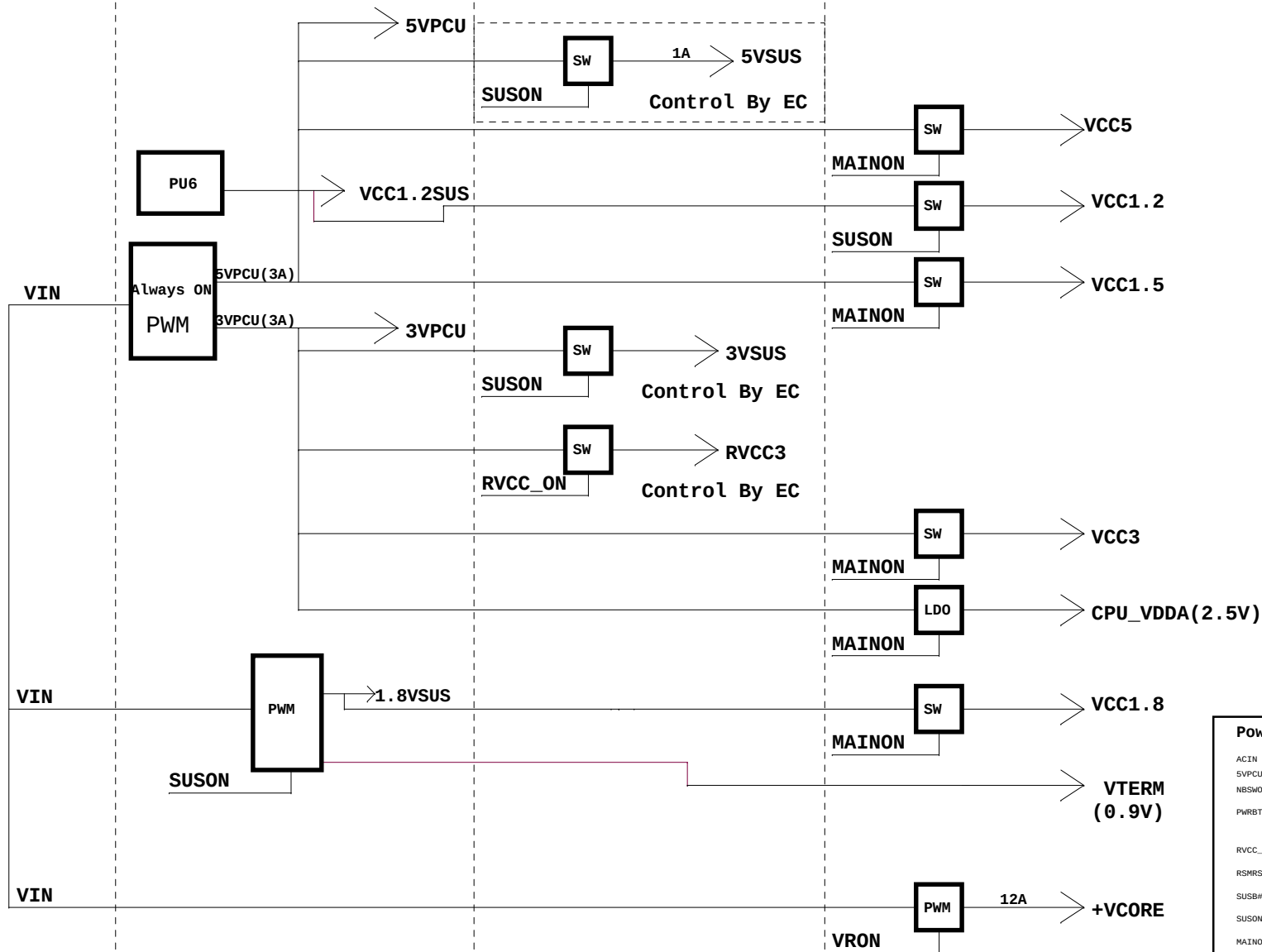
Sheet 1 of 35

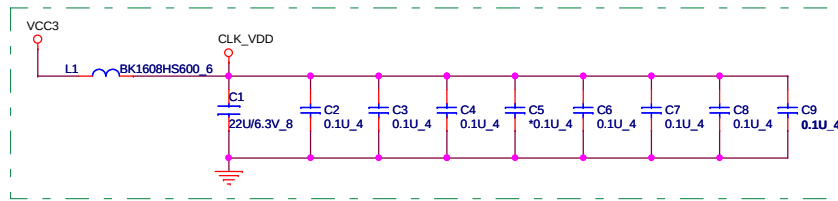
DCIN

ALWAYS ON

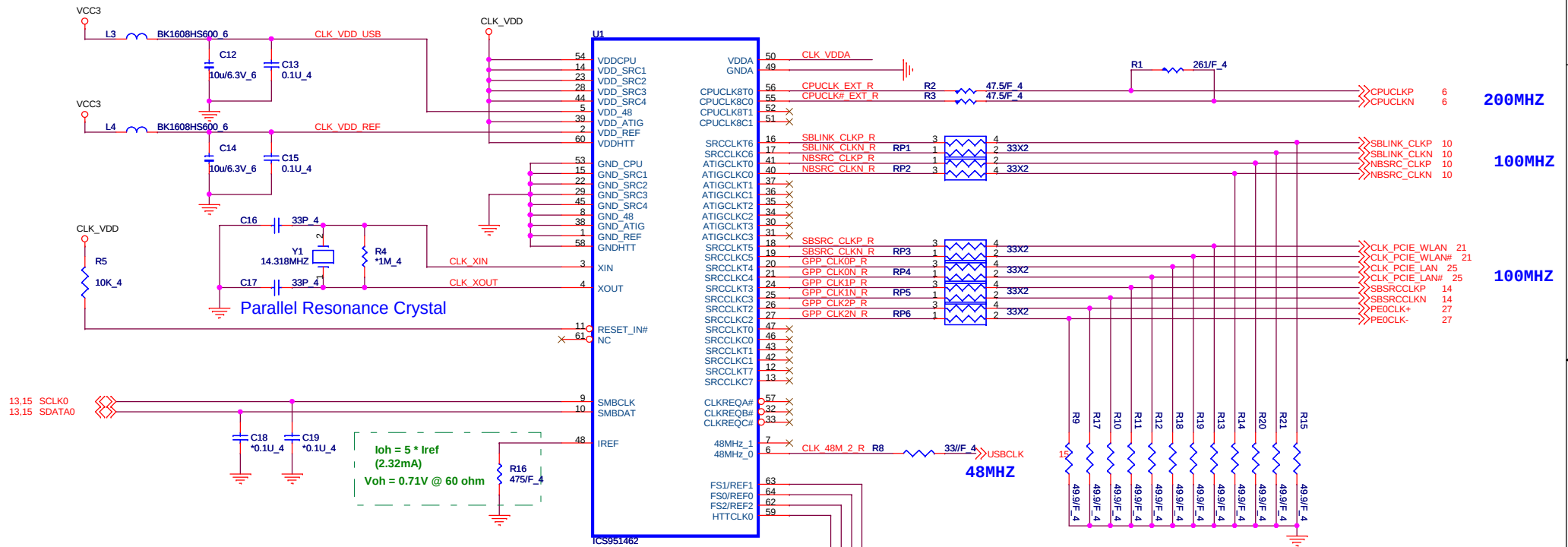
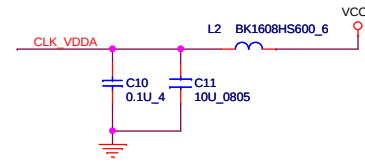
S4 OFF

S3 OFF





Put Decoupling Caps close to Clock Gen. power pin

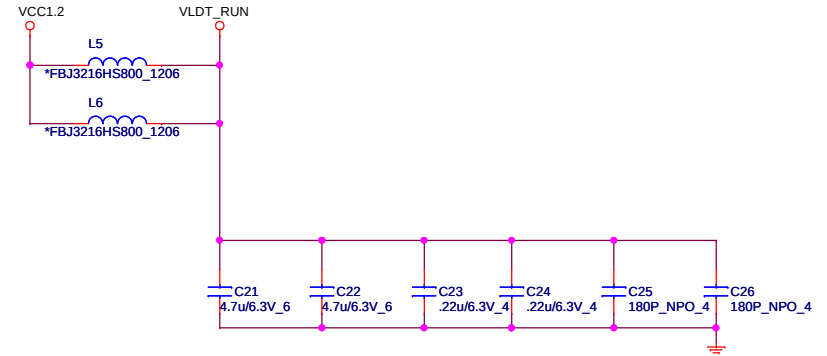
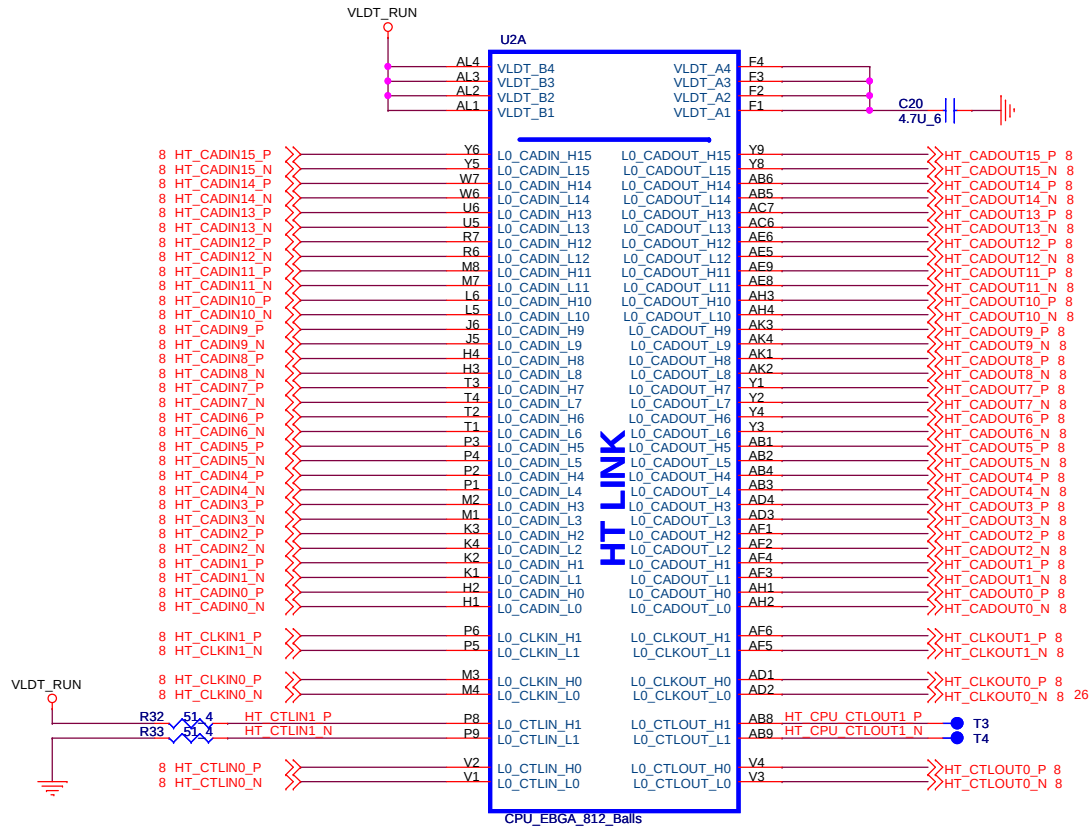


CLKREQA# CONTROL SRC5,6,7
CLKREQB# CONTROL SRC2,3,4 ATIG3
CLKREQC# CONTROL SRC0,1 ATIG0,1,2

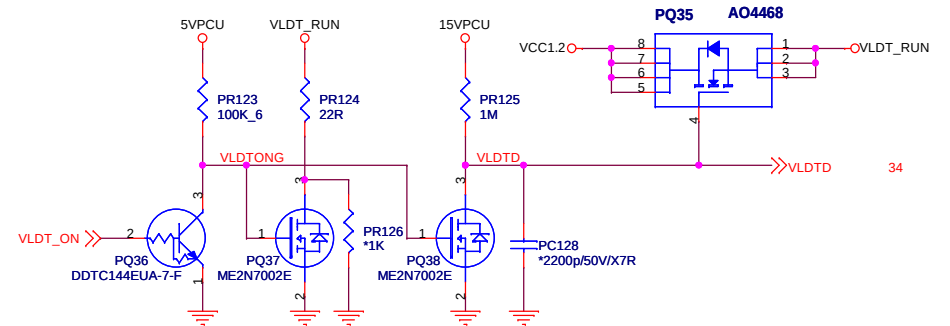
EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal operation

LAYOUT NOTE: VLDT must be routed as a pour or a trace at least 100 mils wide.
VLDT may be routed from the source to either ALx balls or Fx balls. Choose whichever makes routing simpler.



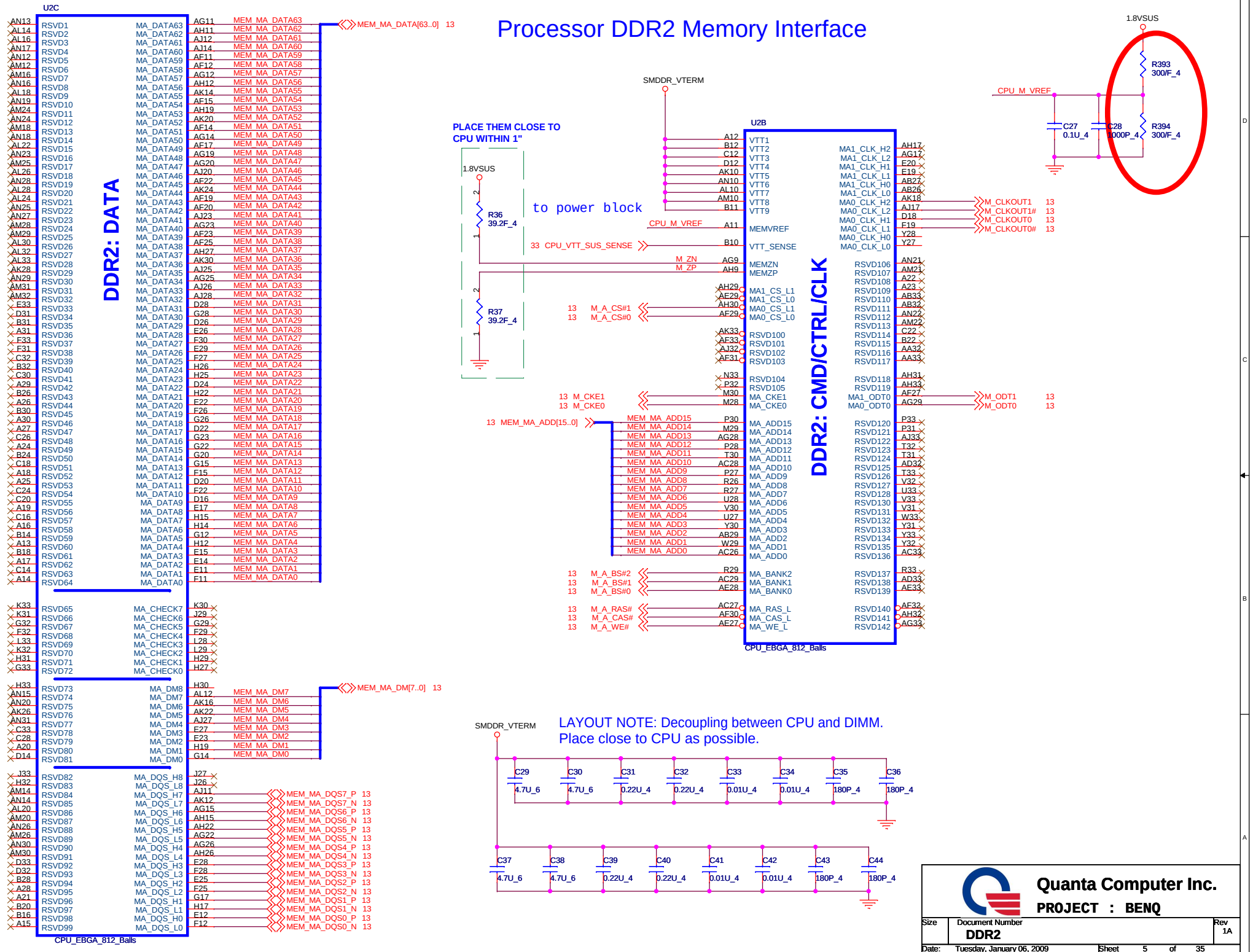
VLDT_RUN

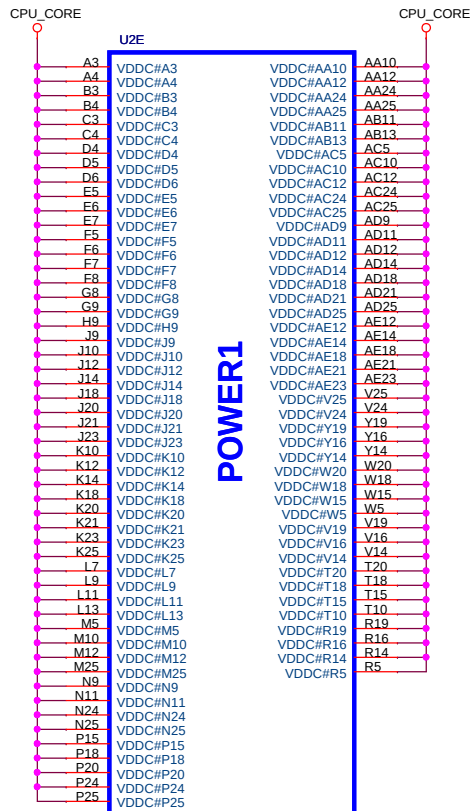


Quanta Computer Inc.
PROJECT : BENQ

Size	Document Number	Rev
	HT LINK	1A
Date:	Tuesday, January 06, 2009	Sheet 4 of 35

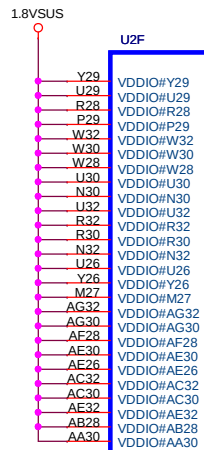
Processor DDR2 Memory Interface





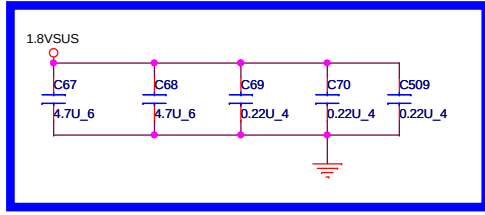
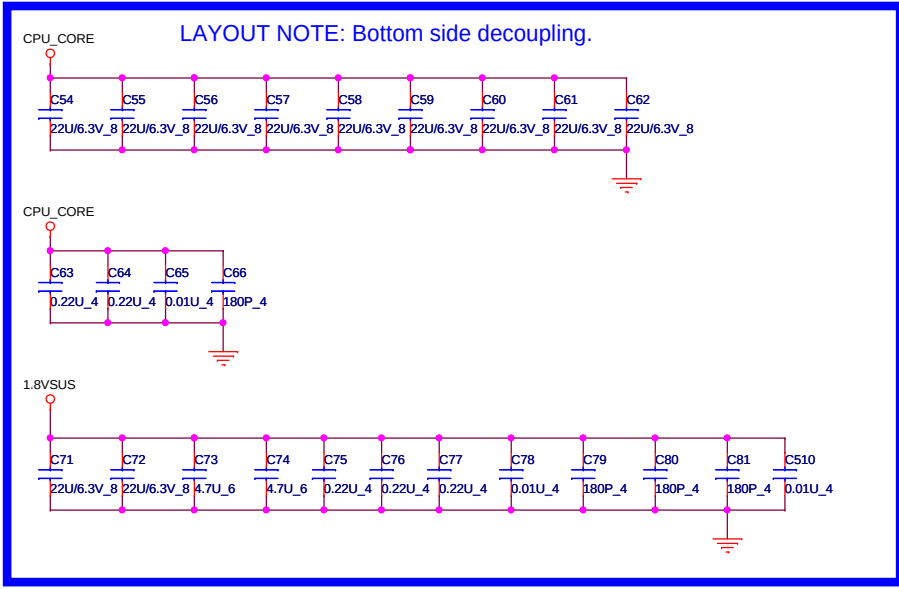
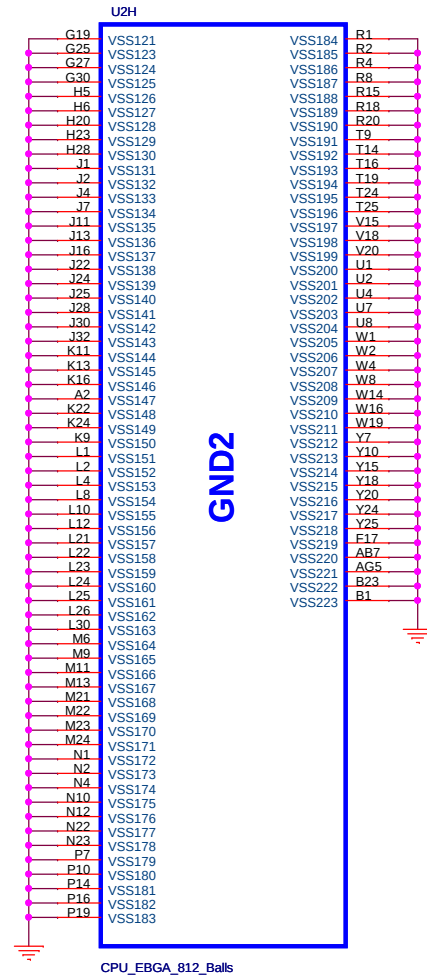
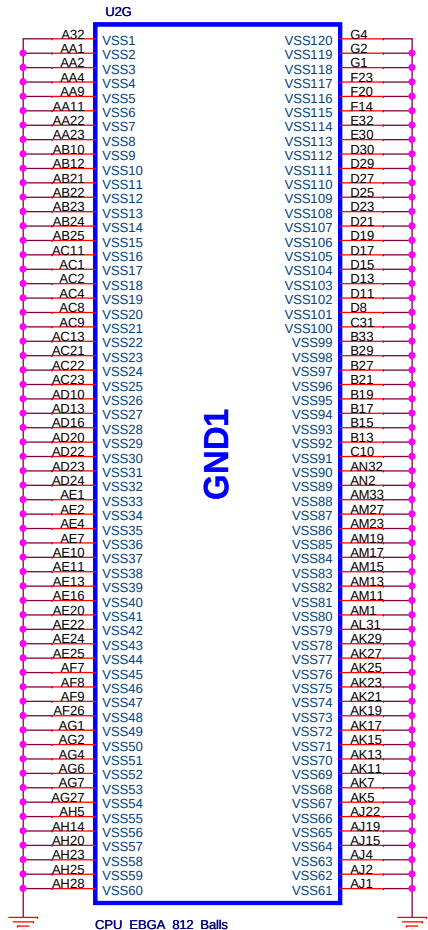
POWER1

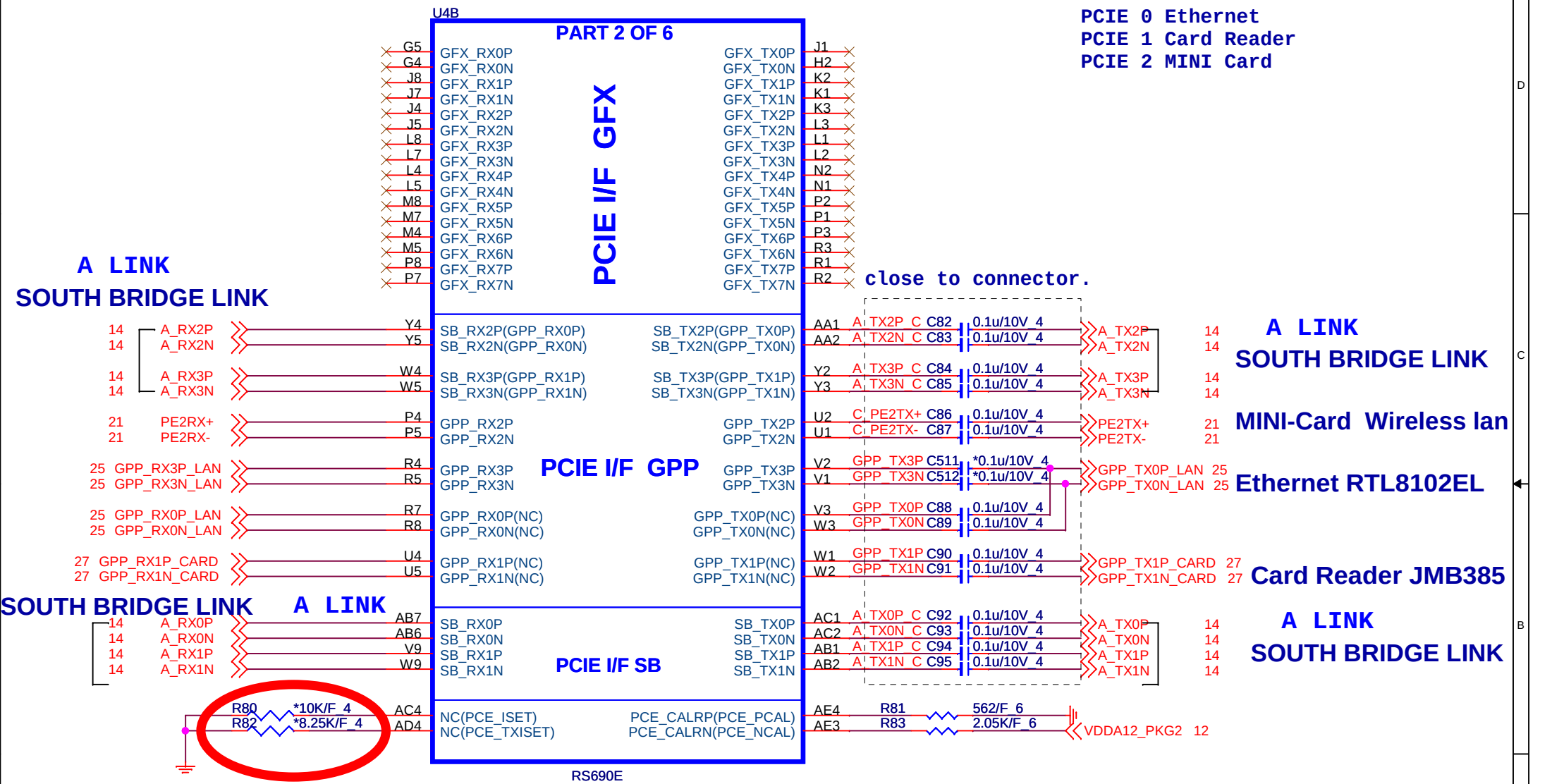
CPU_EBGA_812_Balls



POWER2

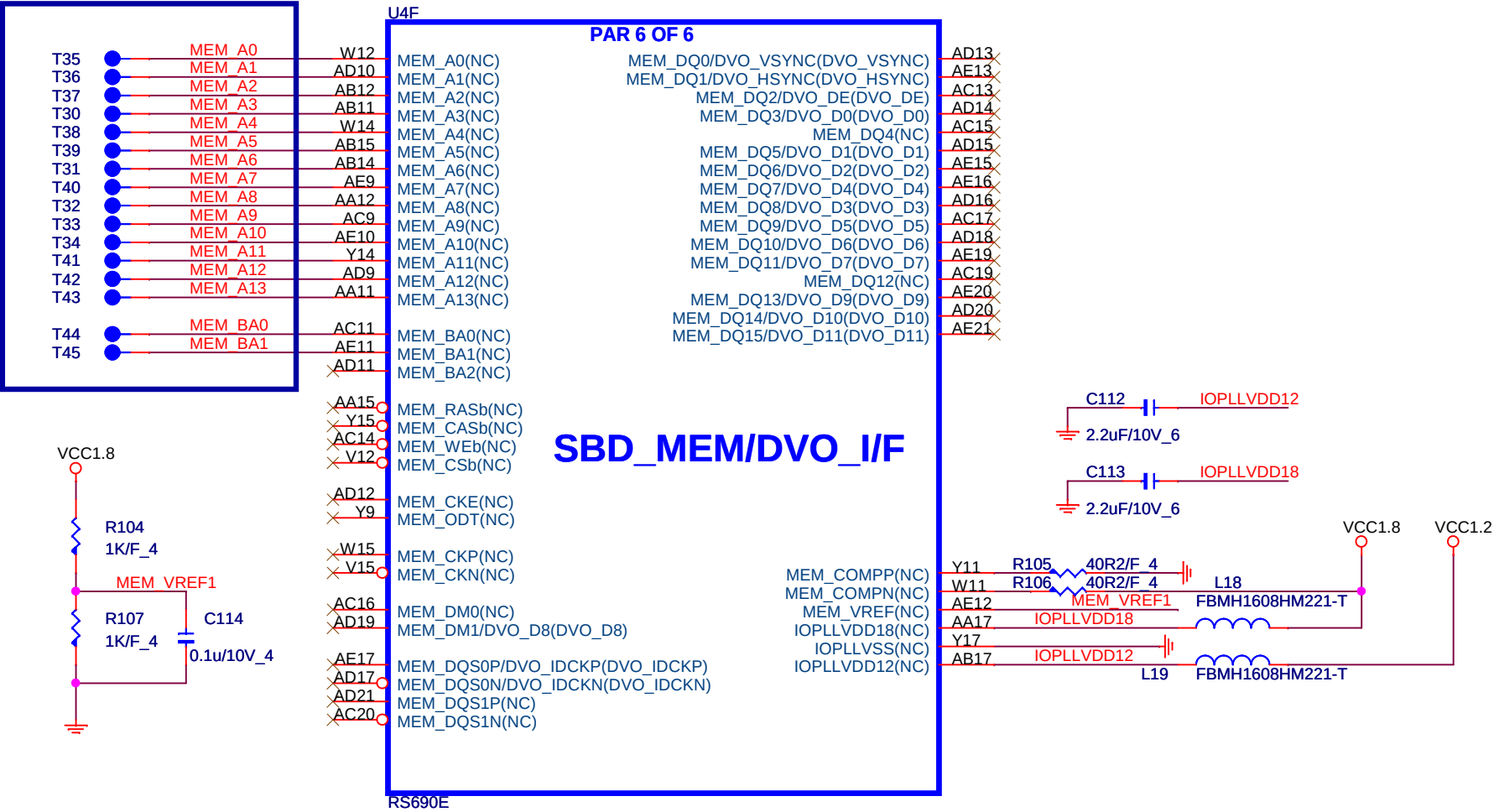
CPU_EBGA_812_Balls



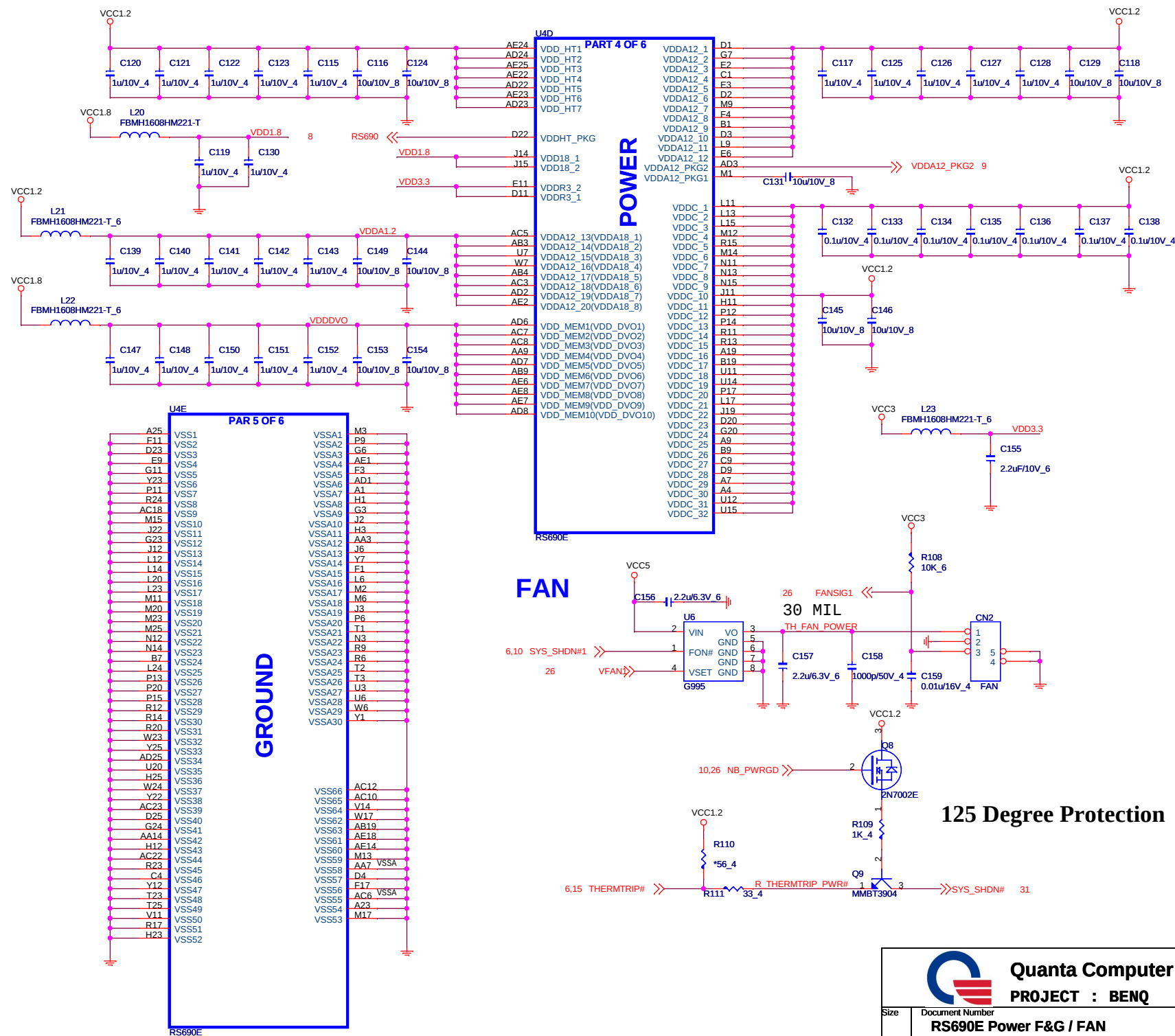


Quanta Computer Inc.
PROJECT : BENQ

DESIGN NOTE:THE FOLLOWING DEBUG
POINTS SHOULD BE PROVIDED.

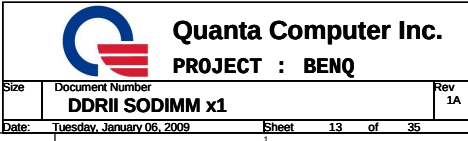


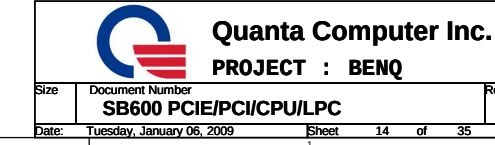
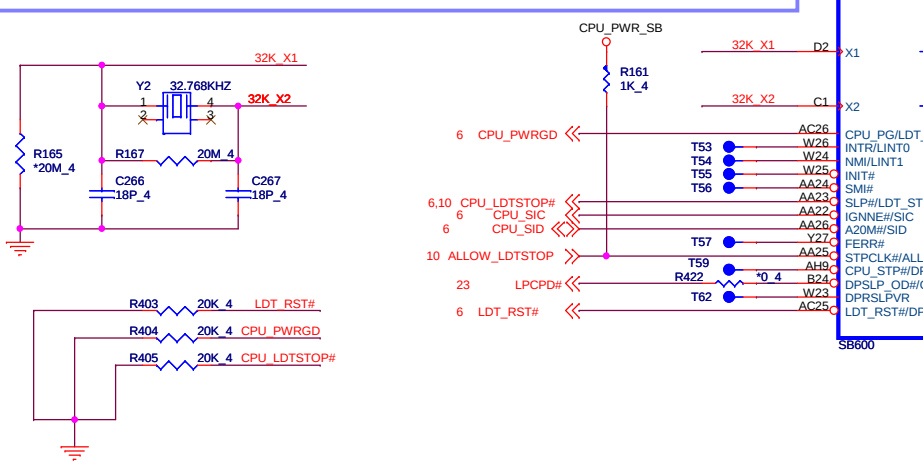
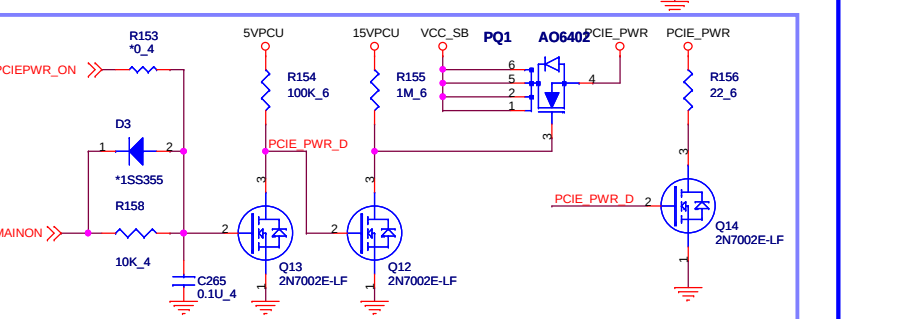
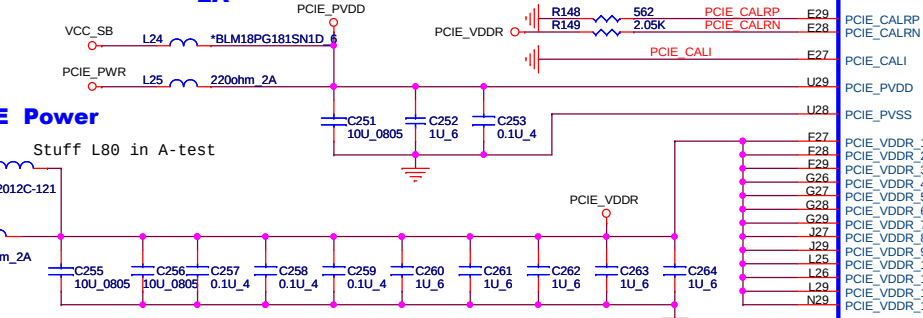
Quanta Computer Inc.
PROJECT : BENQ

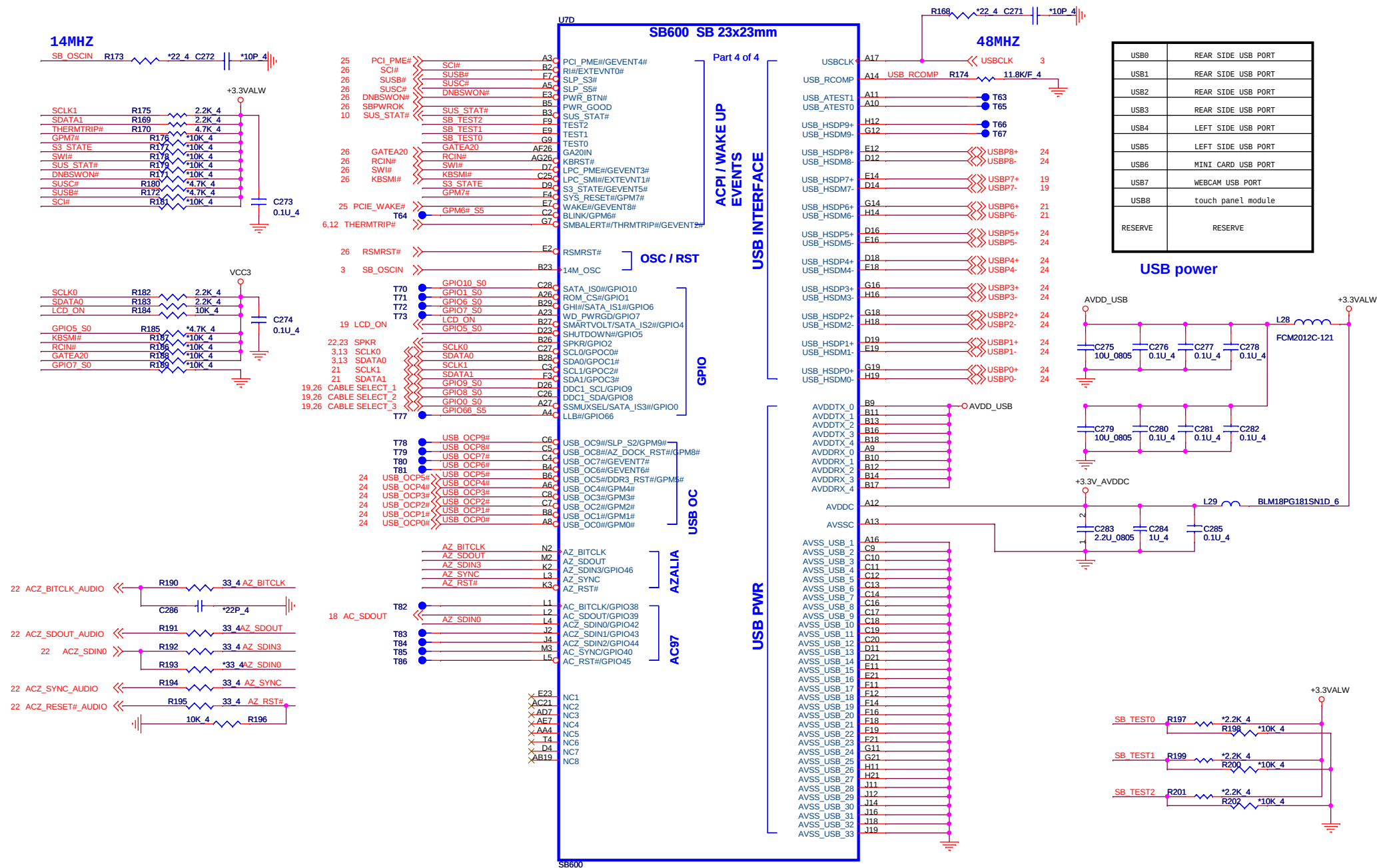


Quanta Computer Inc.
PROJECT : BENQ

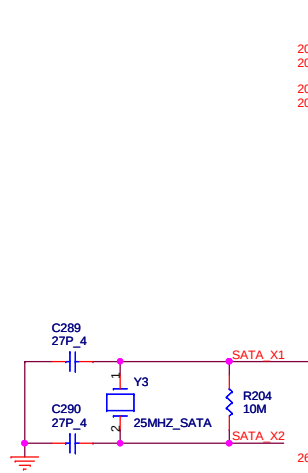
Size	Document Number	Rev
	RS690E Power F&G / FAN	1A
Date:	Tuesday, January 06, 2009	Sheet 12 of 35



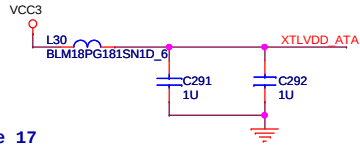




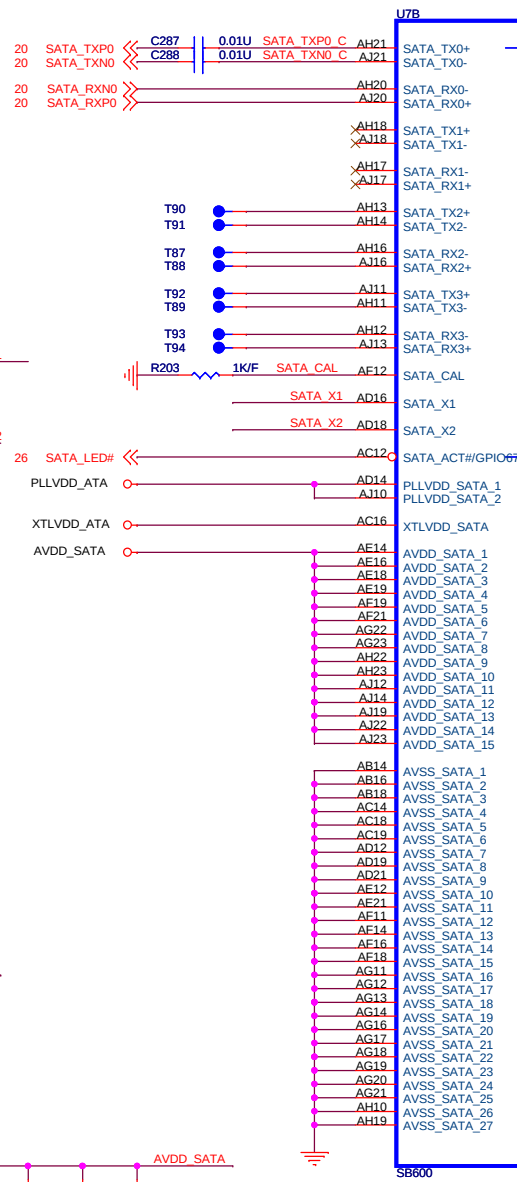
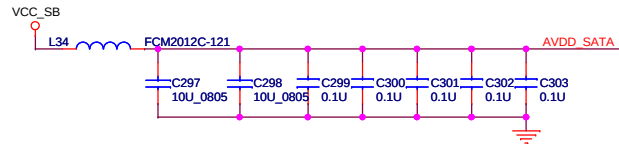
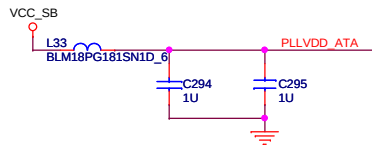
USB0	REAR SIDE USB PORT
USB1	REAR SIDE USB PORT
USB2	REAR SIDE USB PORT
USB3	REAR SIDE USB PORT
USB4	LEFT SIDE USB PORT
USB5	LEFT SIDE USB PORT
USB6	MINI CARD USB PORT
USB7	WEBCAM USB PORT
USB8	touch panel module
RESERVE	RESERVE



SATA Power



From page 17



SB600 SB 23x23mm

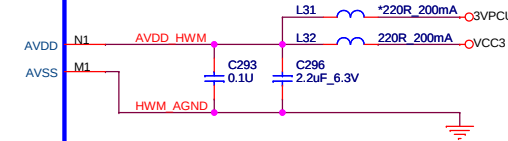
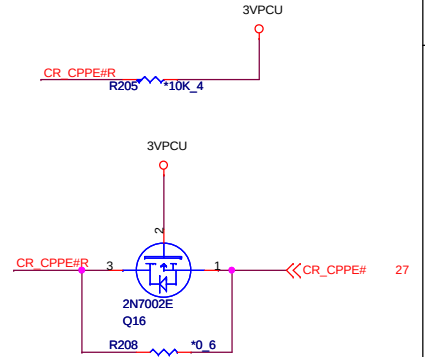
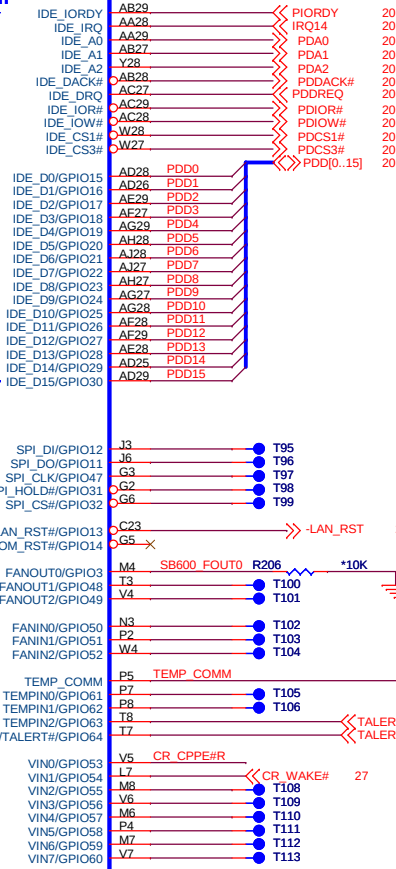
Part 2 of 4

SERIAL ATA

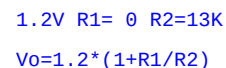
SERIAL ATA POWER

SPI ROM

HW MONITOR

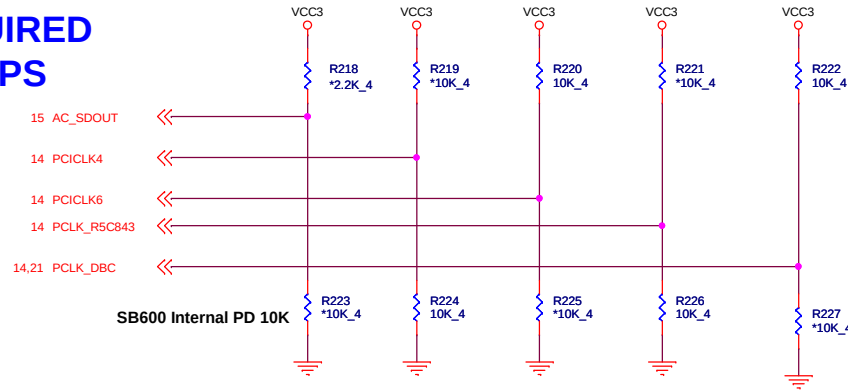


Quanta Computer Inc.
PROJECT : BENQ



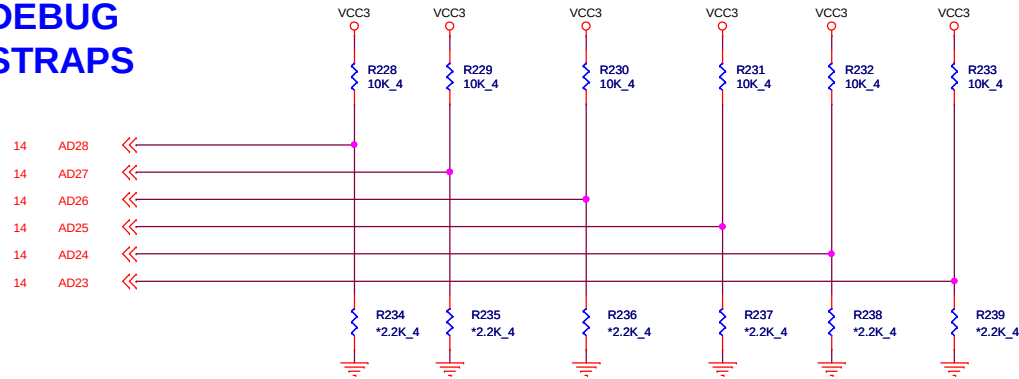
Size	Document Number	Rev
	SB600 POWER/DECOUPLING	1A
Date:	Tuesday, January 06, 2009	Sheet 17 of 35

REQUIRED STRAPS



				PCLK_R5C843	PCLK_DBC
	AC_SDOUT	PCICLK4	PCICLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

DEBUG STRAPS

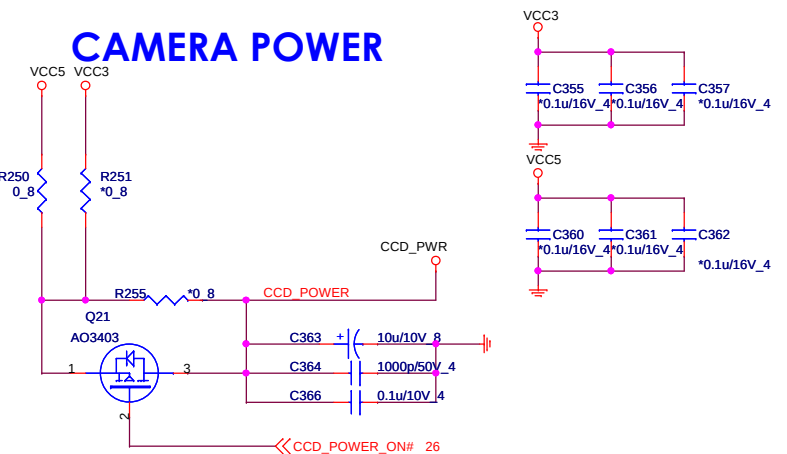
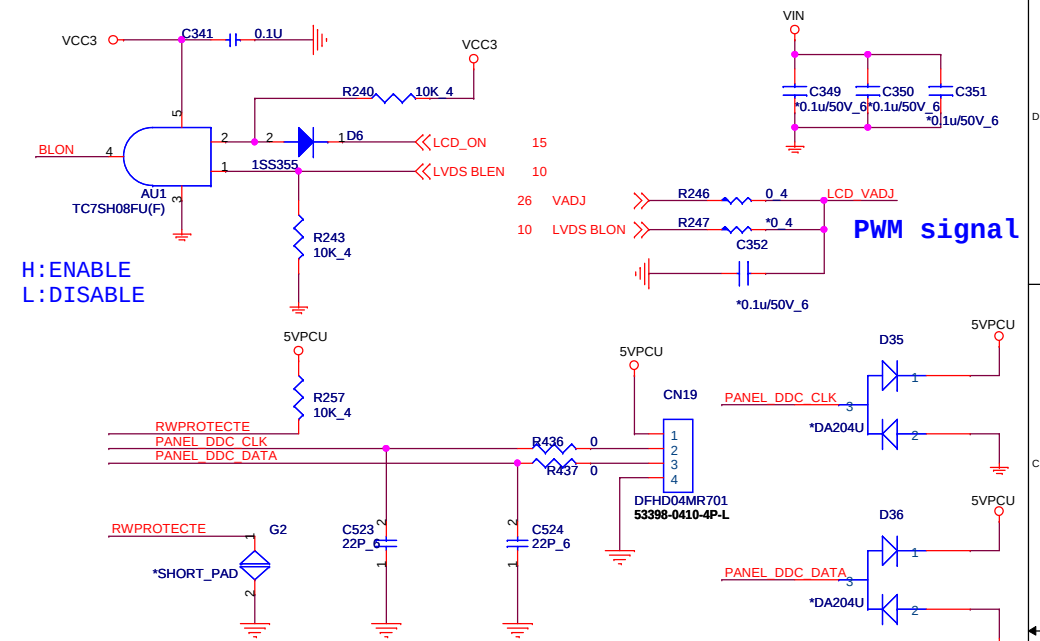


	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

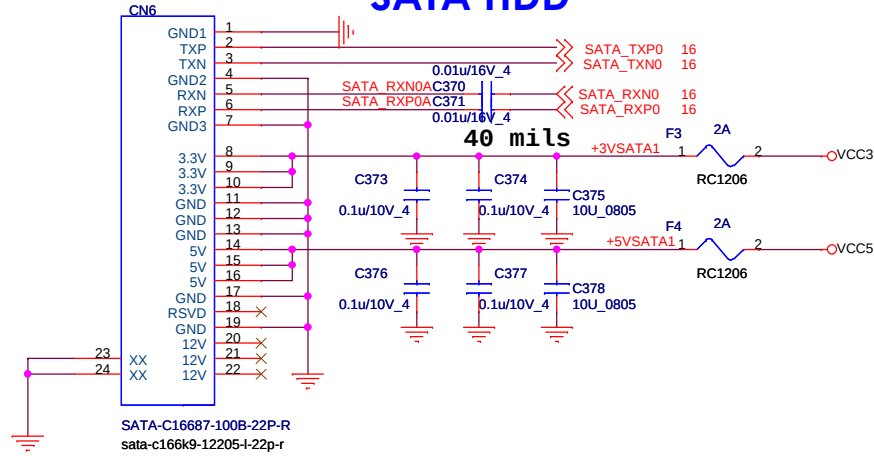


Quanta Computer Inc.
PROJECT : BENQ

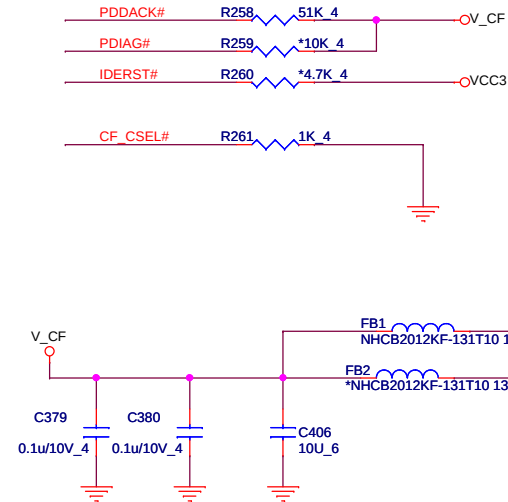
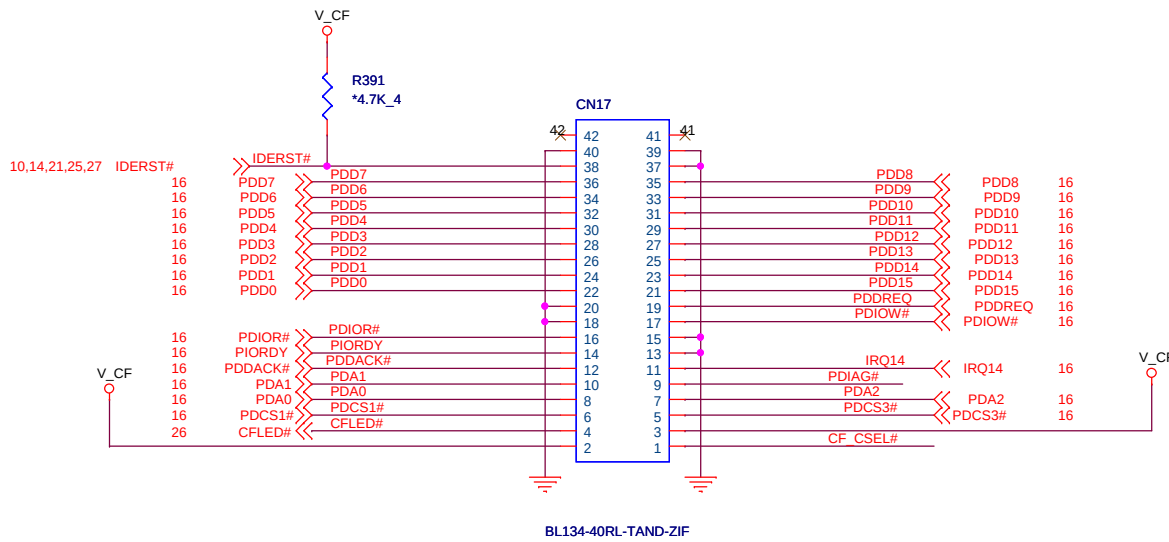
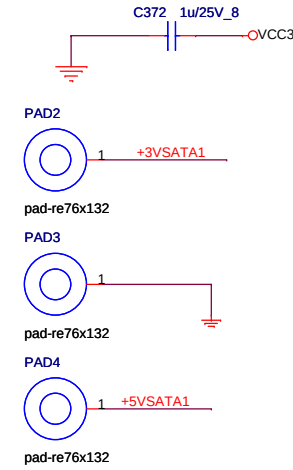
BACKLIGHT ON/OFF CONTROL



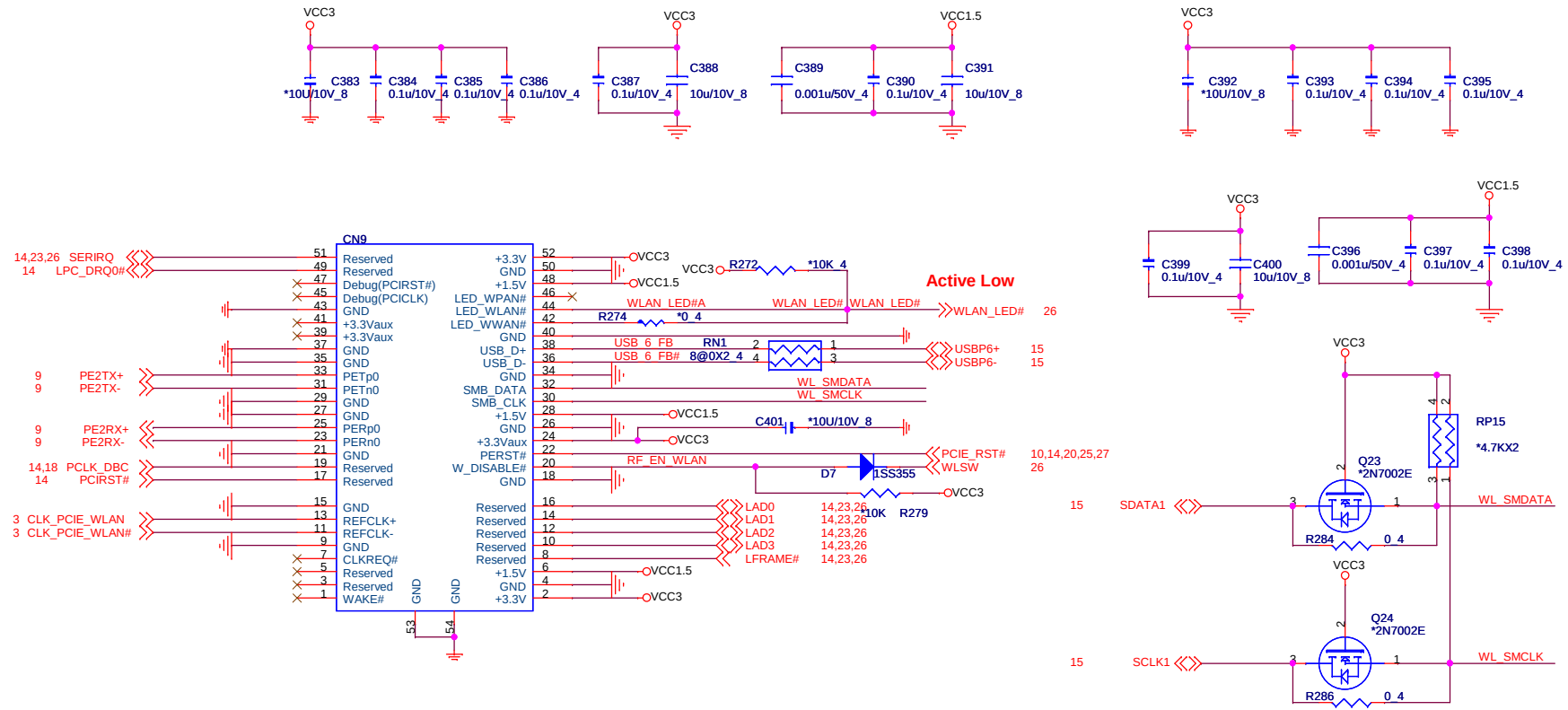
SATA HDD

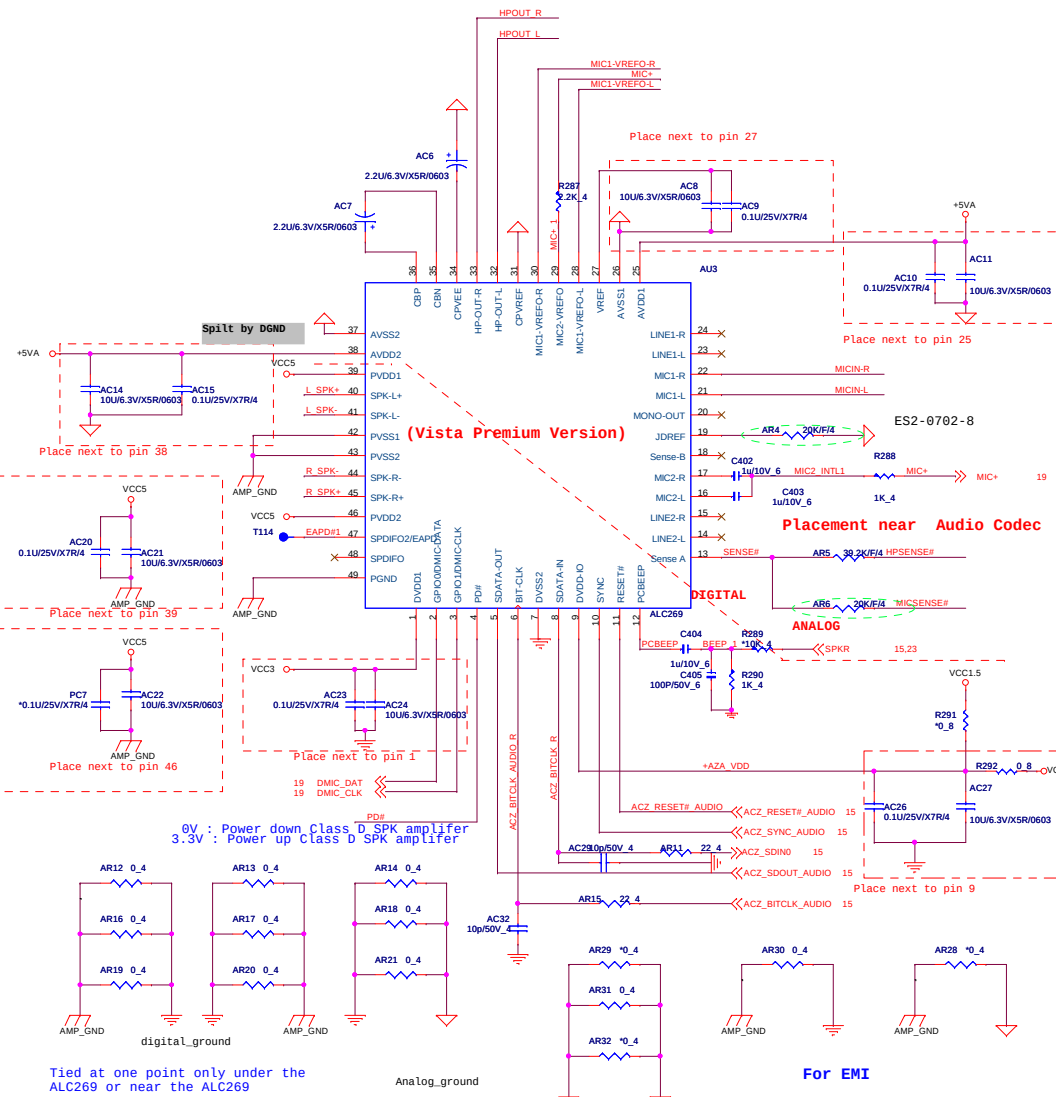


FOR EMI



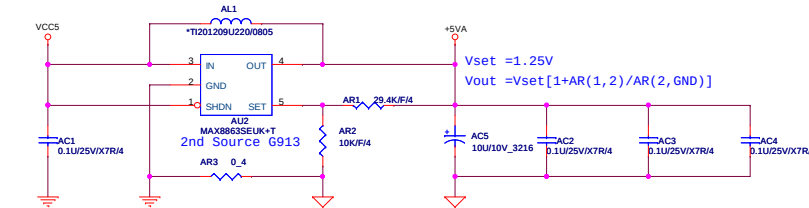
21.5" MINI-Card I (WLAN/ WiMAX)



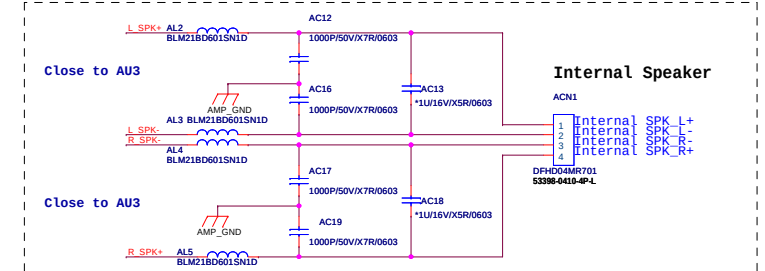


Demodulation Filter

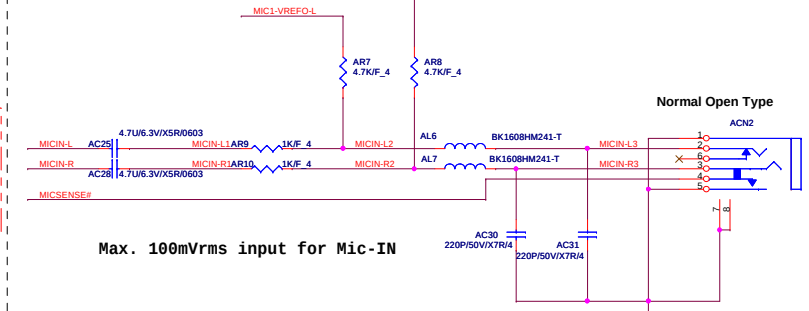
Place close to Codec



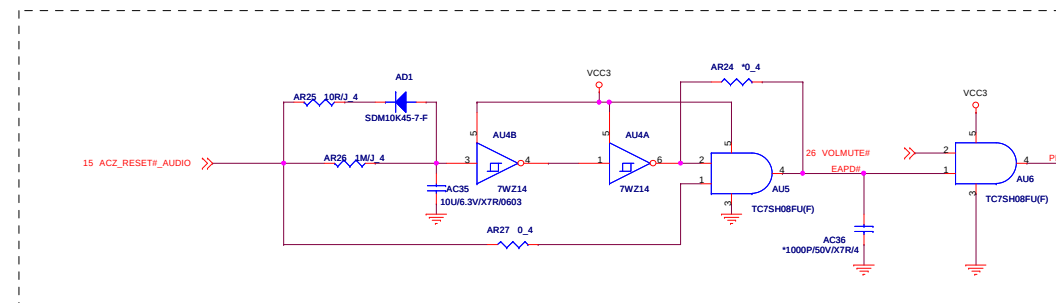
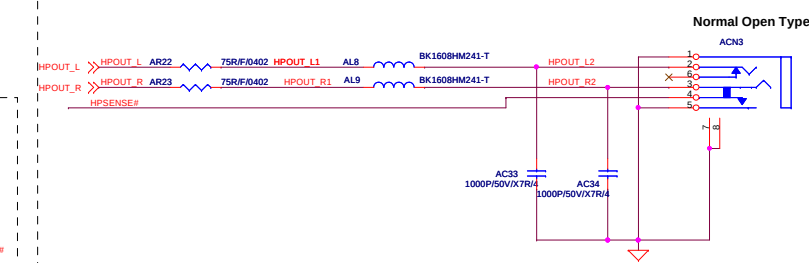
ES2-0707-1



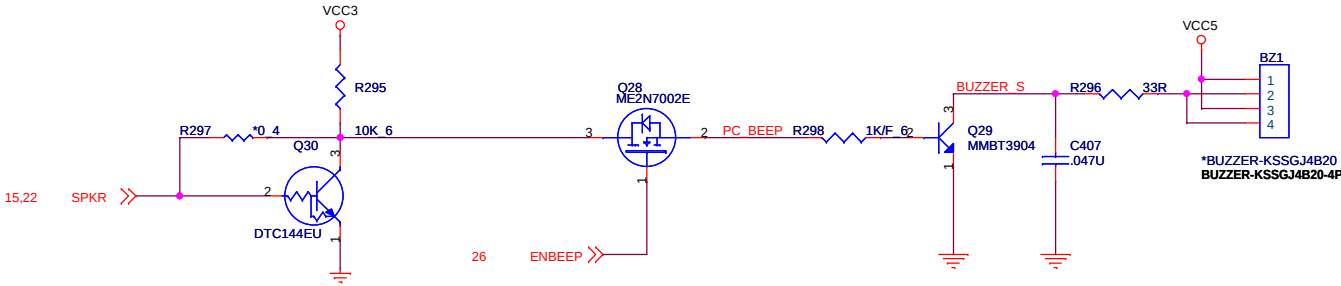
MIC-IN Jack



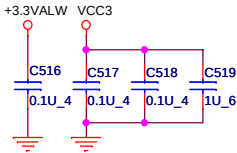
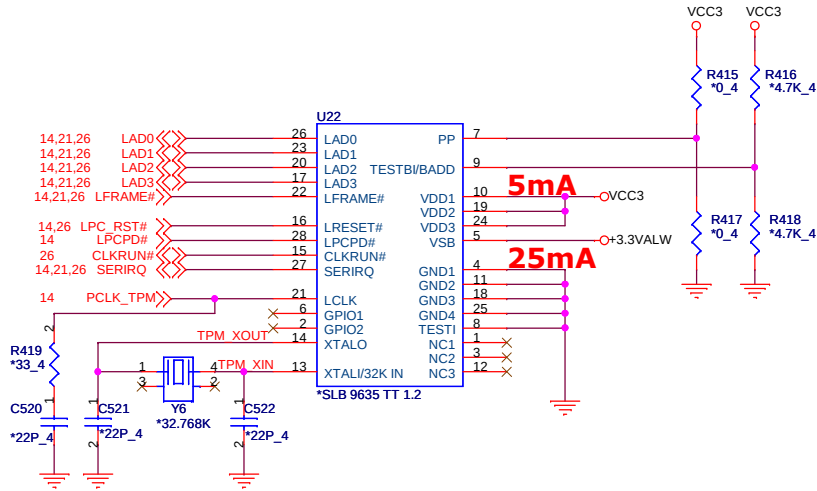
Headphone-OUT



BUZZER



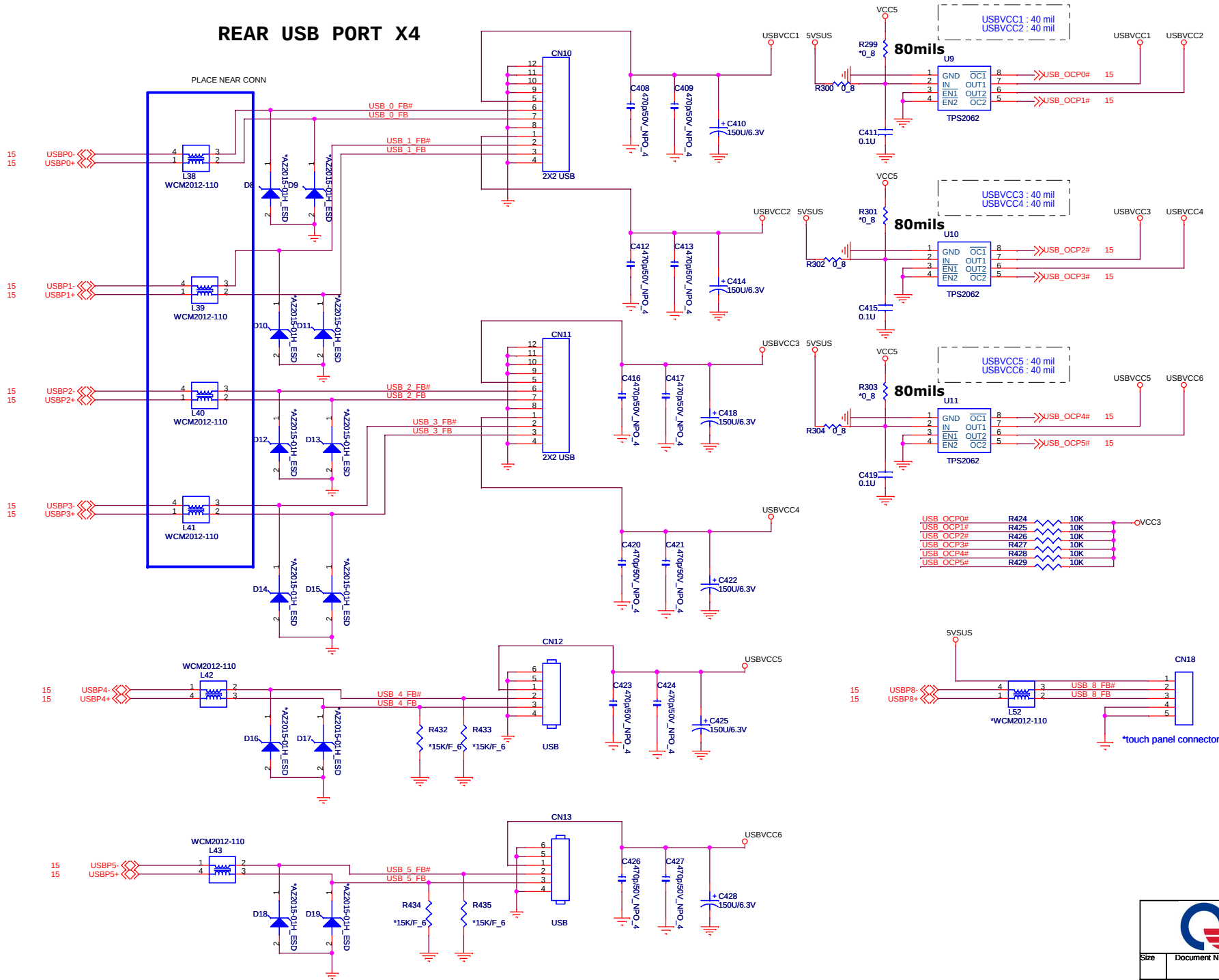
TPM1.2



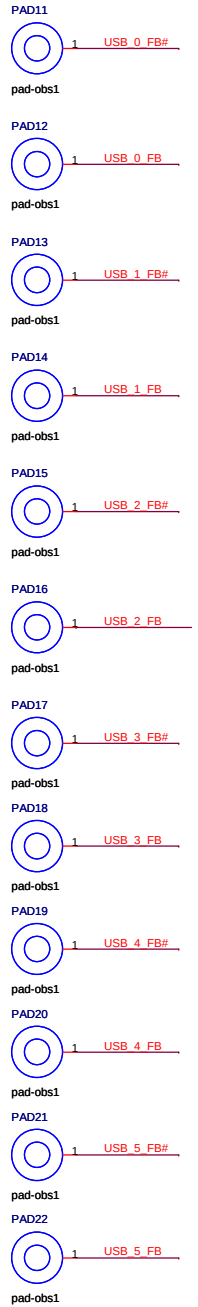
I/O Address		
BADDR	Index	Data
0	2E	2F
1	4E	4F

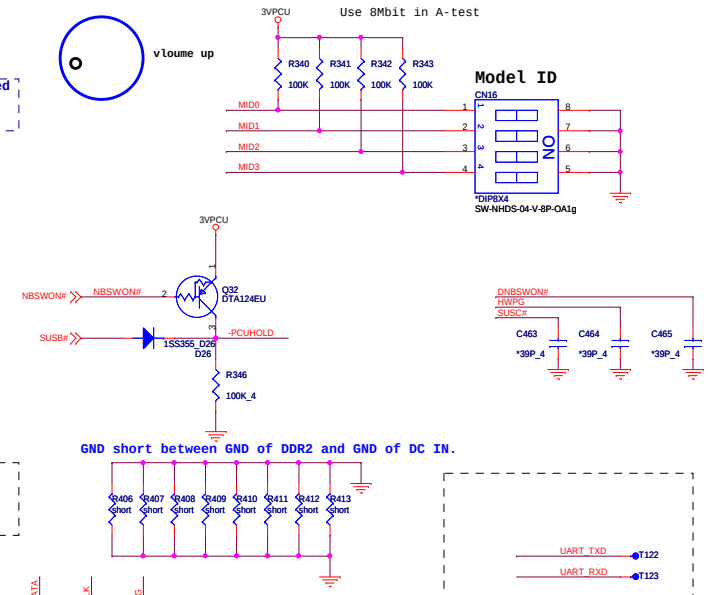
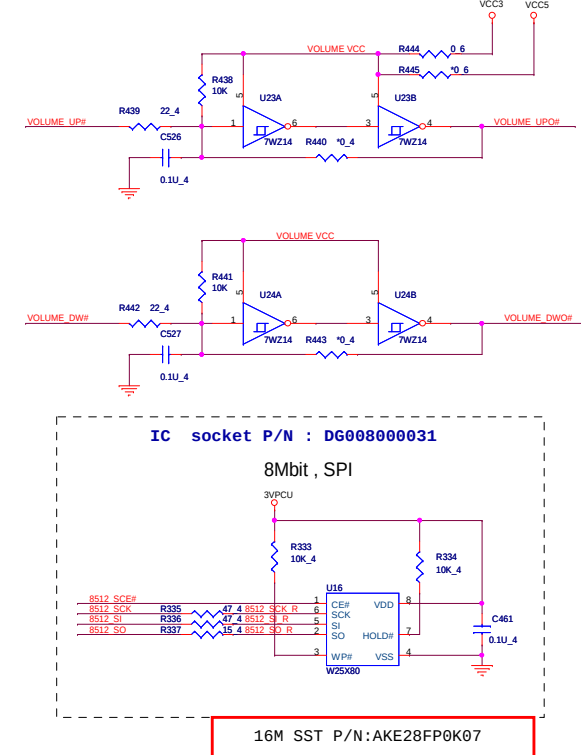
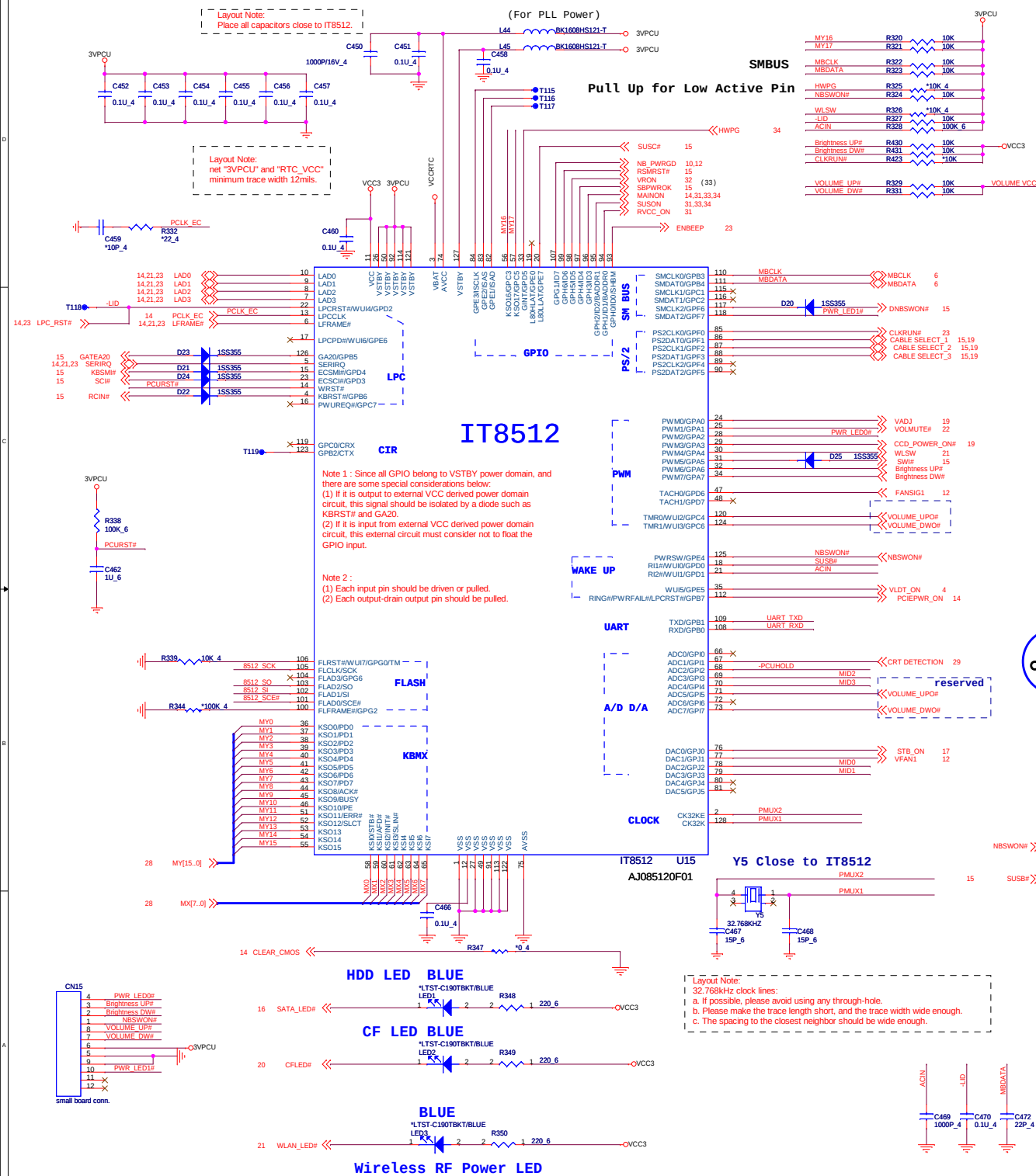
USB on M/B

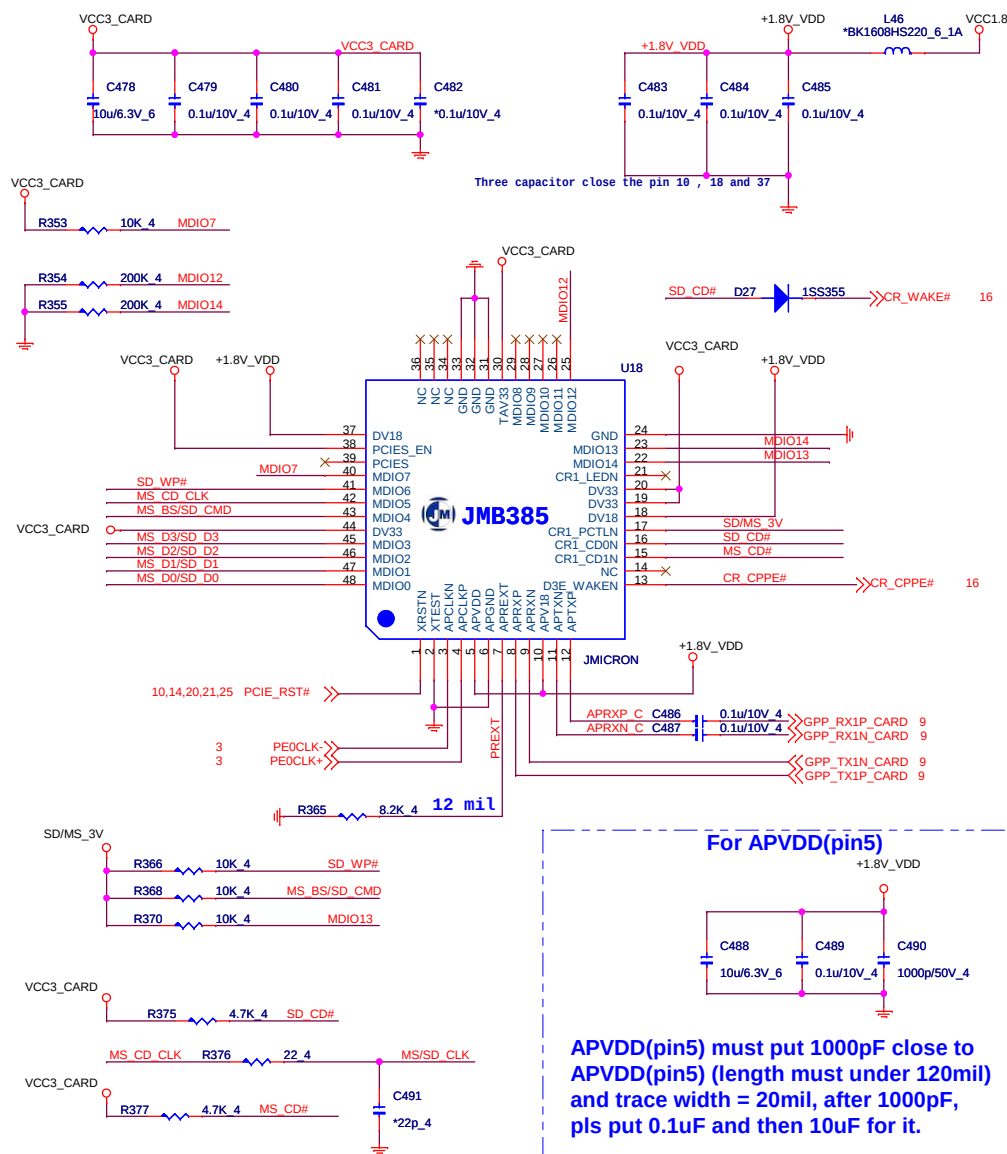
REAR USB PORT X4



PAD



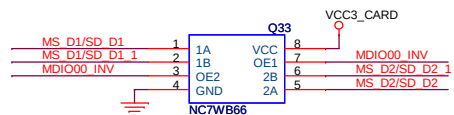




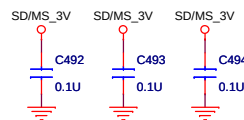
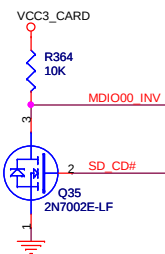
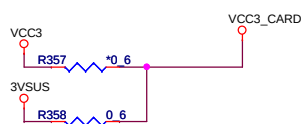
Use 0805 type and over 20 mils trace width on both side

250mA 30mil SD/MS_3V

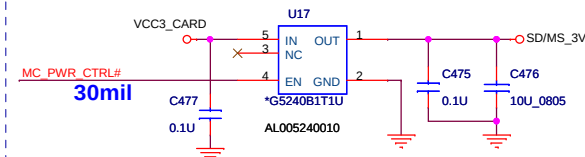
Memory Card Power Supply



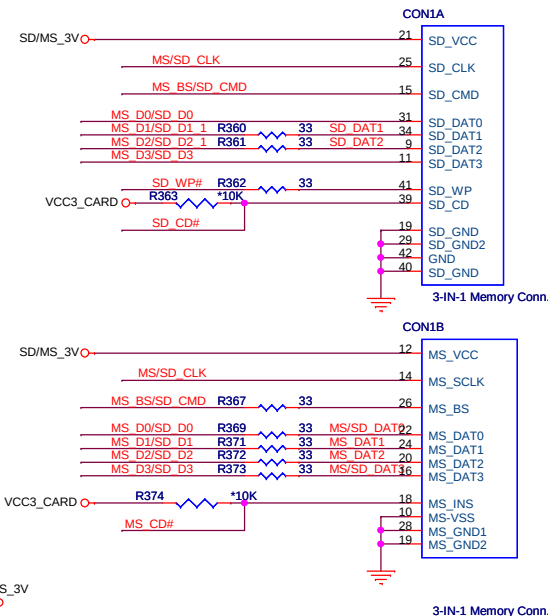
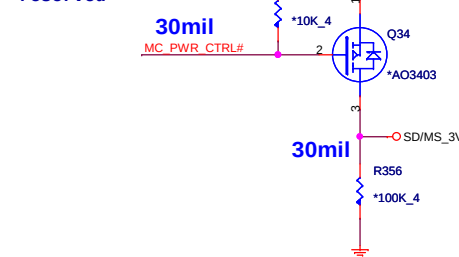
* To Avoid SONY MS Duo Adaptor Issue On SD



reserved

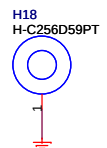
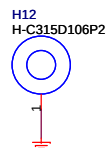
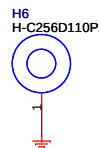
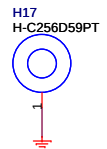
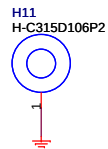
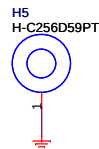
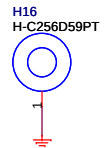
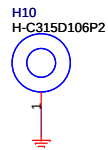
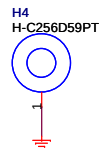
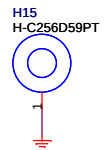
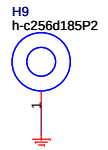
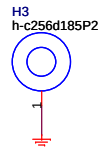
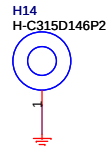
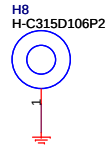
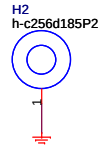
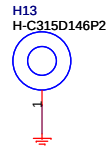
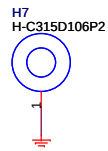
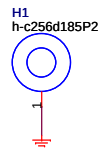


reserved

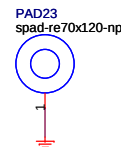
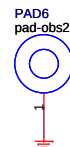
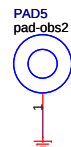
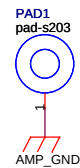


Need to change drill hole size

SCREW HOLE



PAD



AMP_GND

Keyboard CONN Reserved for EC Debug

KEYBOARD

*88502-2401-24P-L

24	24	MX2	MX2	26
23	23	MX4	MX4	26
22	22	MX1	MX1	26
21	21	MX7	MX7	26
20	20	MX3	MX3	26
19	19	MX0	MX0	26
18	18	MX6	MX6	26
17	17	MX5	MX5	26
16	16	MY4	MY4	26
15	15	MY1	MY1	26
14	14	MY3	MY3	26
13	13	MY5	MY5	26
12	12	MY6	MY6	26
11	11	MY7	MY7	26
10	10	MY8	MY8	26
9	9	MY9	MY9	26
8	8	MY10	MY10	26
7	7	MY14	MY14	26
6	6	MY11	MY11	26
5	5	MY2	MY2	26
4	4	MY0	MY0	26
3	3	MY12	MY12	26
2	2	MY13	MY13	26
1	1	MY15	MY15	26

CON2

MX3	7	8	CP1
MX0	5	6	*220pX4_4
MX6	3	4	
MX5	1	2	
MY10	7	8	CP2
MY14	5	6	*220pX4_4
MY11	3	4	
MY2	1	2	
MY4	7	8	CP3
MY1	5	6	*220pX4_4
MY3	3	4	
MY5	1	2	
MY6	7	8	CP4
MY7	5	6	*220pX4_4
MY8	3	4	
MY9	1	2	
MX2	7	8	CP5
MX4	5	6	*220pX4_4
MX1	3	4	
MX7	1	2	
MY0	7	8	
MY12	5	6	CP6
MY13	3	4	*220pX4_4
MY15	1	2	

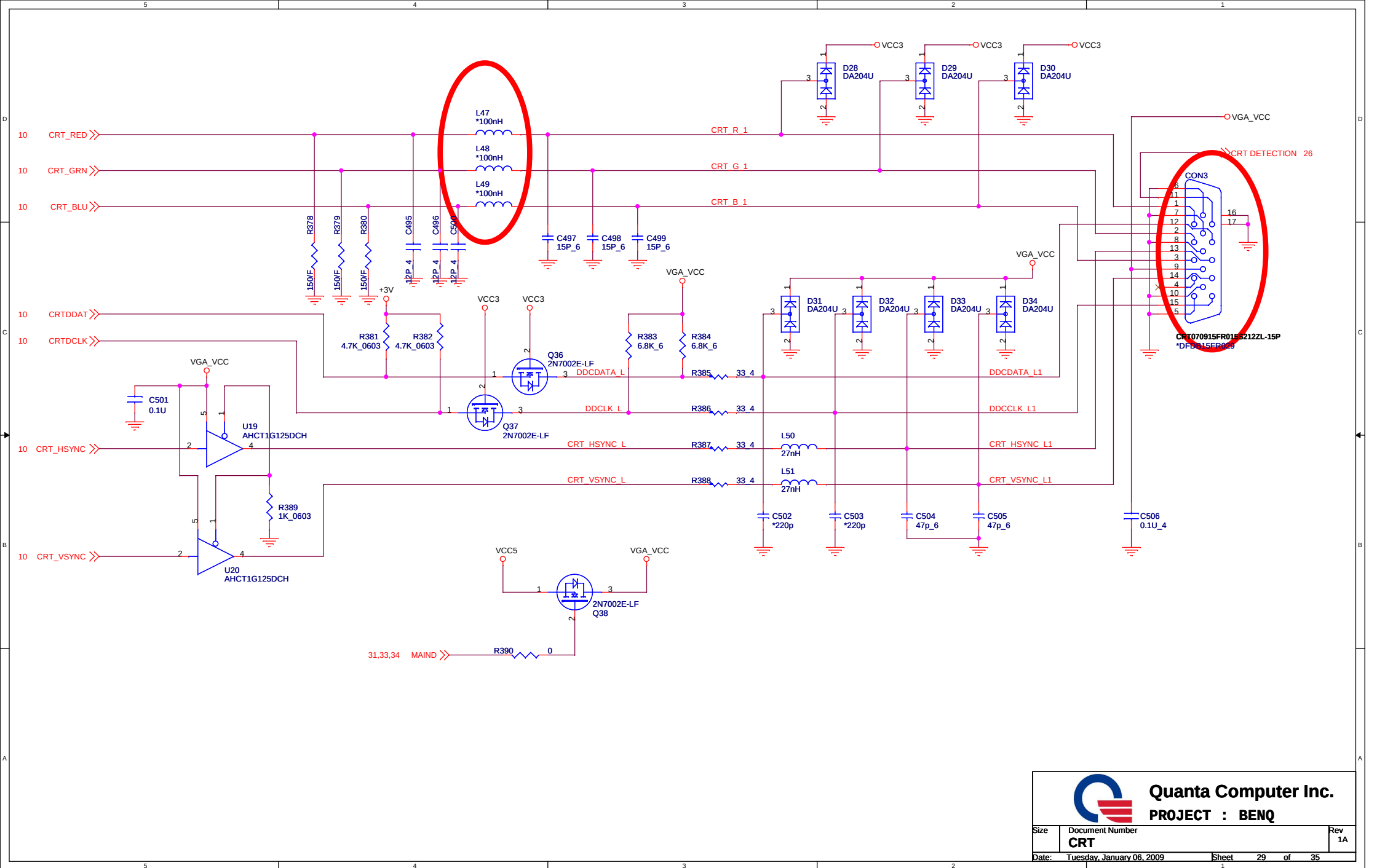
Ø402 size

SATA screw hole H19 ; H20



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Size	Document Number	Rev 1A
SCREW HOLE/DEBUG KEY		
Date:	Tuesday, January 06, 2009	Sheet 28 of 35

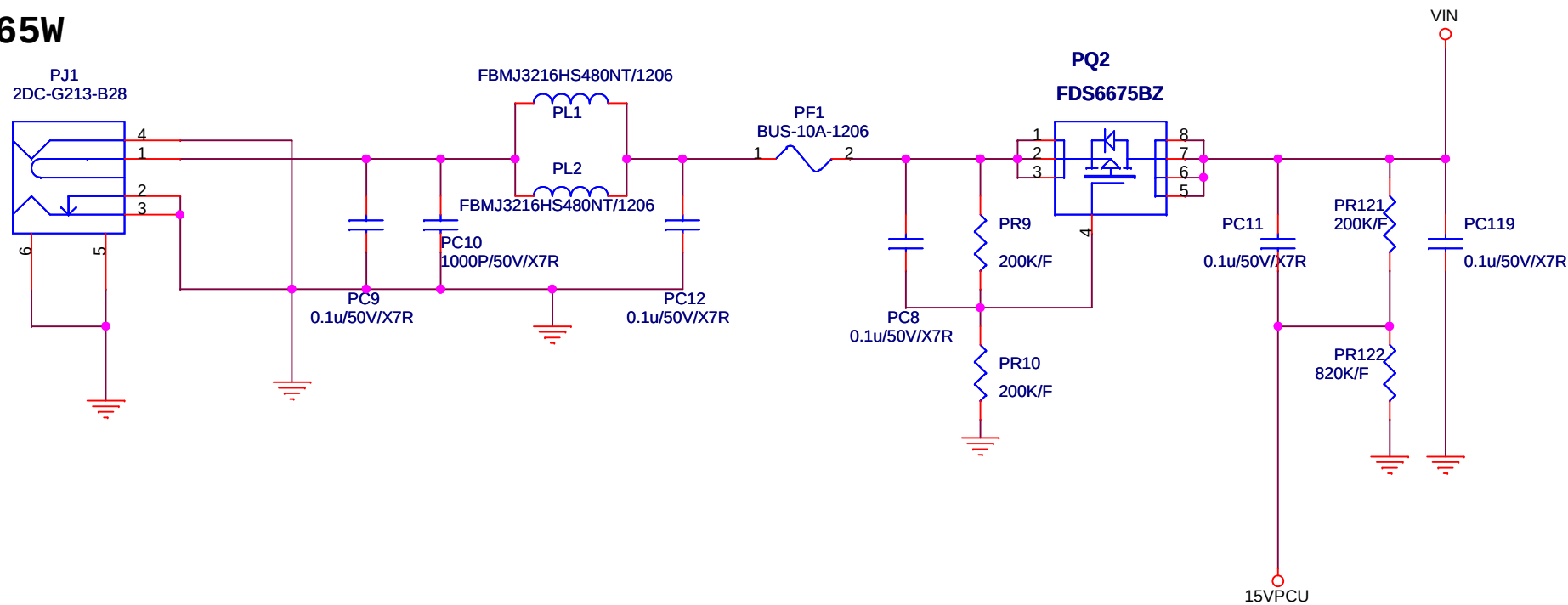


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PROJECT : BENQ

Size	Document Number	Rev
	CRT	1A
Date:	Tuesday, January 06, 2009	Sheet 29 of 35

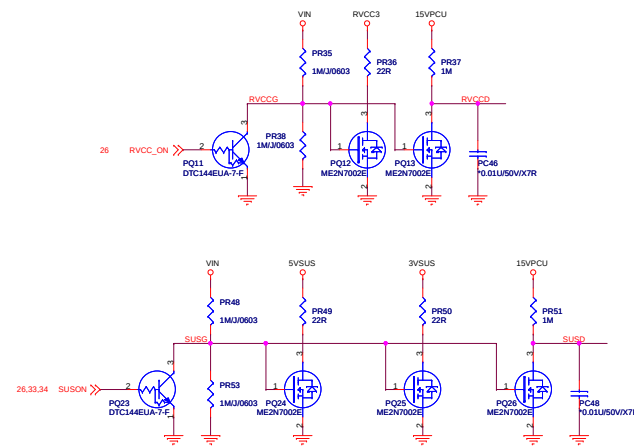
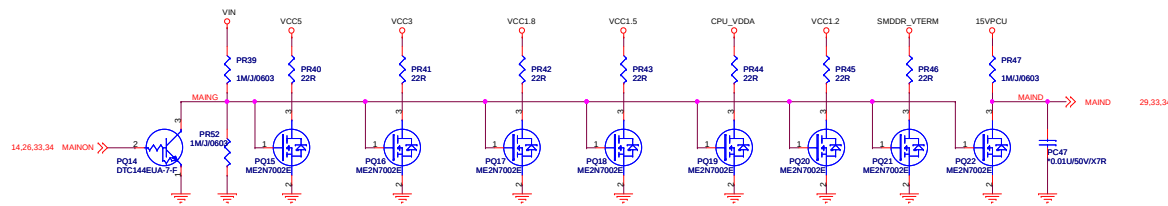
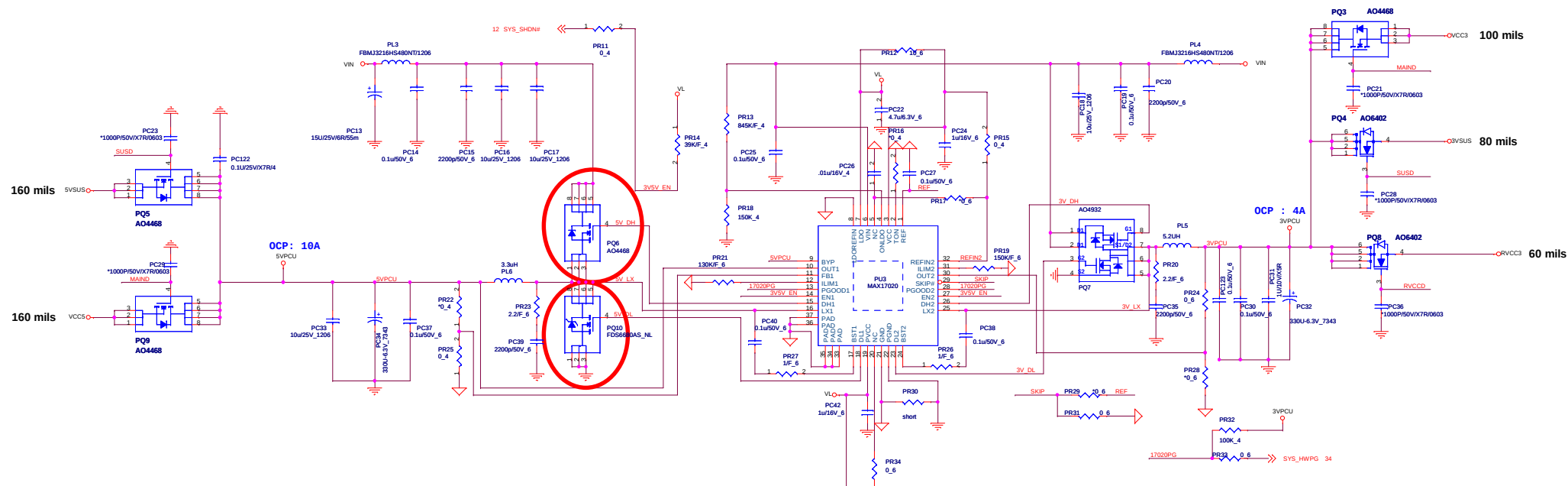
DC IN JACK

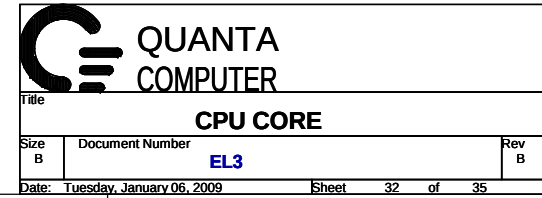
65W

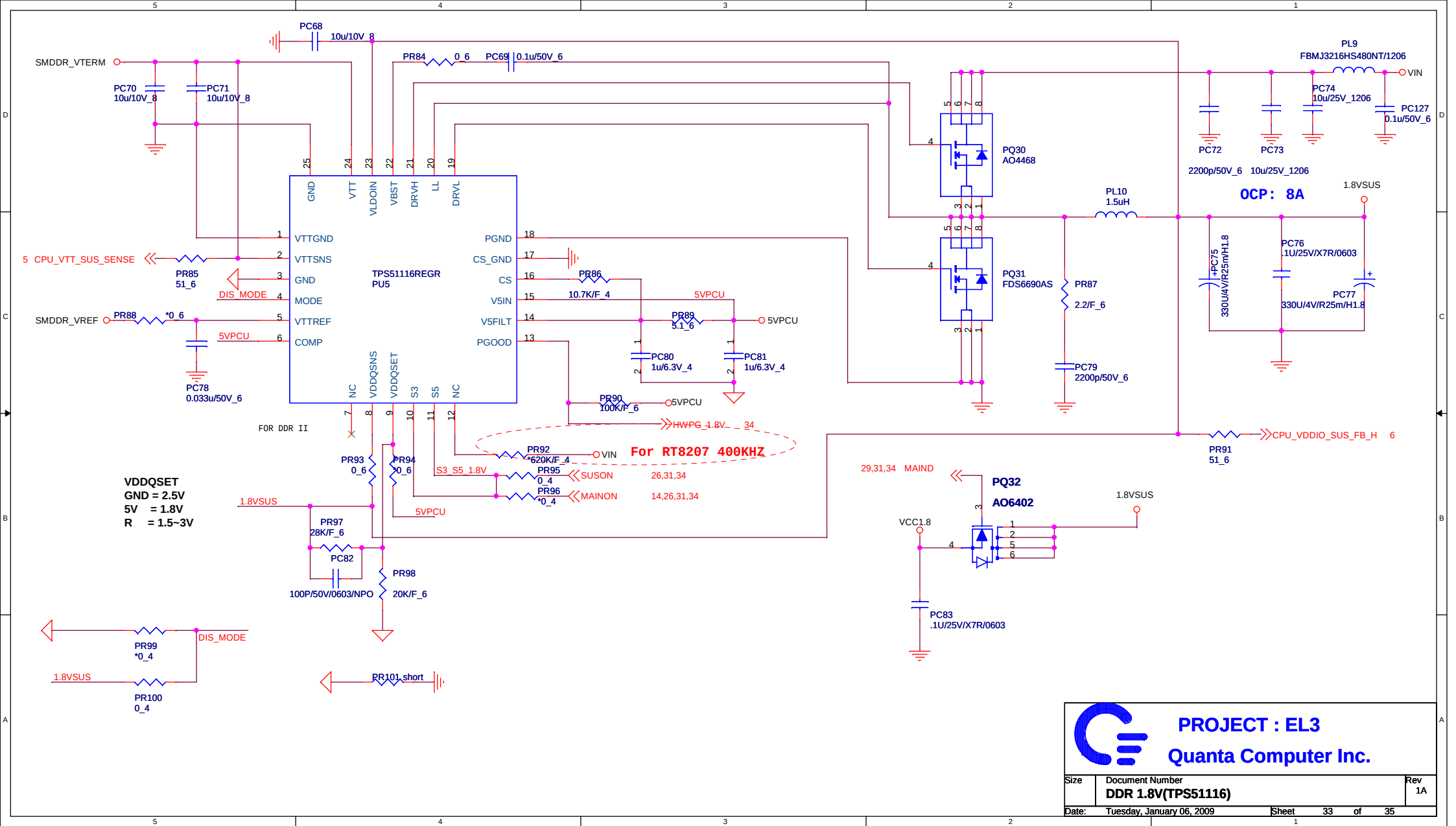


Quanta Computer Inc.
PROJECT : EL3

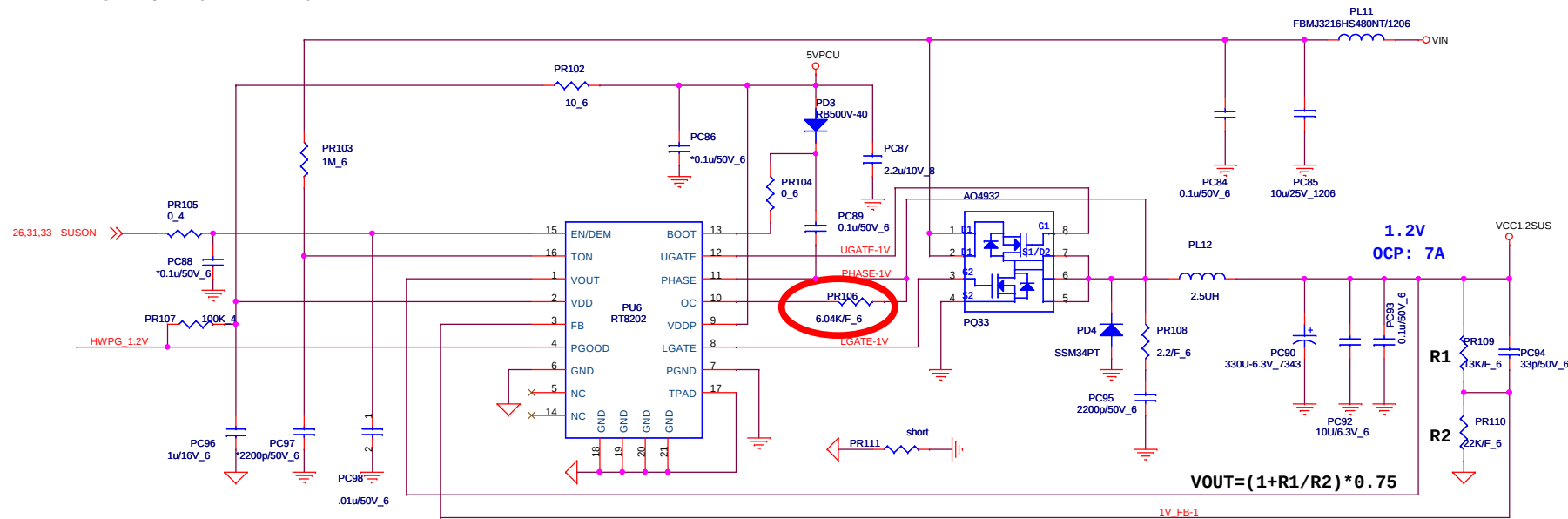
Size	Document Number	Rev
	DC IN	2B
Date:	Tuesday, January 06, 2009	Sheet 30 of 35



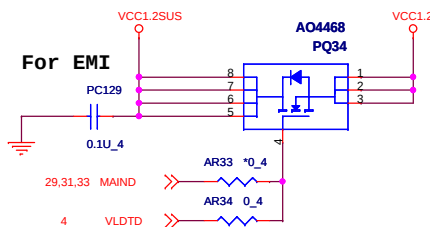
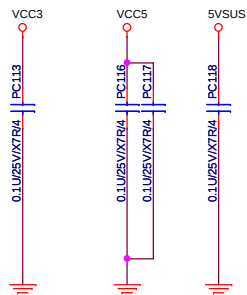
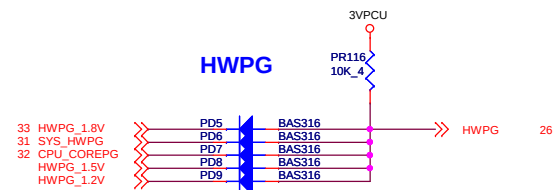
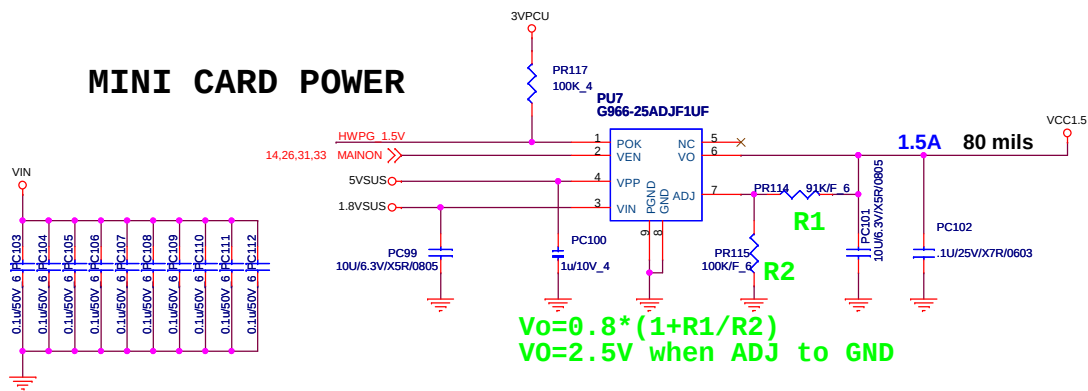




TON=3.85p*1M*1/(Vin-0.5)
Frequency=1/(0.0036767)=272K



MINI CARD POWER



DATE	Description	Note	Page
2008 1006	1.page 3 pin9&pin10 short issue 2.page 5 change U2B VTT net SMDDR to SMDDR_VTERM 3.page 6 U2 E1&E2 symbol pin swap;AL6&AM5 pin swap 4.page 6 TALERT# pull high high 4.7K(CS24702FB10) 5.page 14 add LPC_RST to U7 A_RST 6.page 16 Y3 change P/N:BG625000A09 7.page19 add L37 P/N:CX201290009 8.page19 reserve the EEPROM 24c02 to panel edid data 9.page 21 USB6+/USB6- pin swap 10.page 24 change CN10 and CN11 pin symbol define 11.page 26 reserve LPC_RST# to SB600 12.page 27 update the CON1 symbol pin define 13.page 17 add D5 P/N:BC001010Z17 14.page 31add PQ11,PQ23,PQ14 P/N:BA001440013 15.page 34 delete PC97 for 1.2VSUS output 16.page 34 HWP61.5V add resistor 10k to VCC3 17.page 25 pin 10 of CN15 Vcc 5V change to PWR_LED1#		
	18.Page 26 Add R430,R431 for brightness up and down. 19.C472, C473 changes to 22P. 20.The pin S3 and pin S5 of PU5 short and delete PR96. 21.Add R432,433,434,435 for USB detection. 22. Page 30 Add PC119,PR121,PR122 for 15VPCU. 23. Page 34 Change PR110 to 20.5K/F_6, Change PL12 to 2.5uH . 24. Page 31 Del PC41,PC43,PC44,PC45,PD1,PD2 for 15VPCU 25. Page 32 Change PR62 to 1.2R_4 26. Page 33 Change PR97 to 29.4K/F_6 27. Add the PC129 and C525 for EMI solution. 28. Add PQ35 ~ 38 for HT voltage (1.2V). 29. Add R424 ~ R429 for USB detection. 30. Add R448 for RTC clock. 31. Change the PQ06 and PQ10.		



Quanta Computer Inc.

PROJECT : EL3

Size	Document Number	Rev
	CHANGE LIST	C
Date: Tuesday, January 06, 2009	Sheet	35 of 35