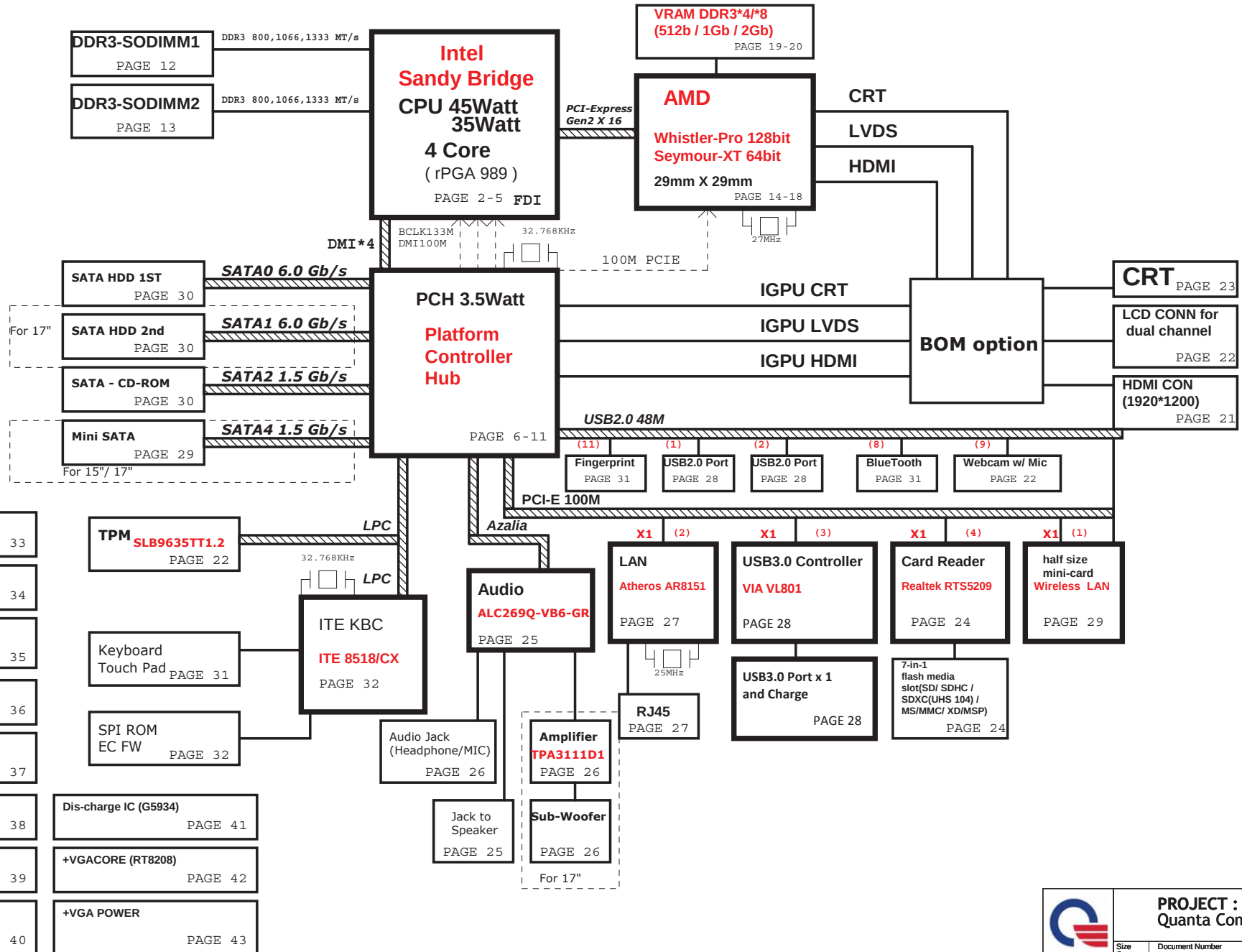


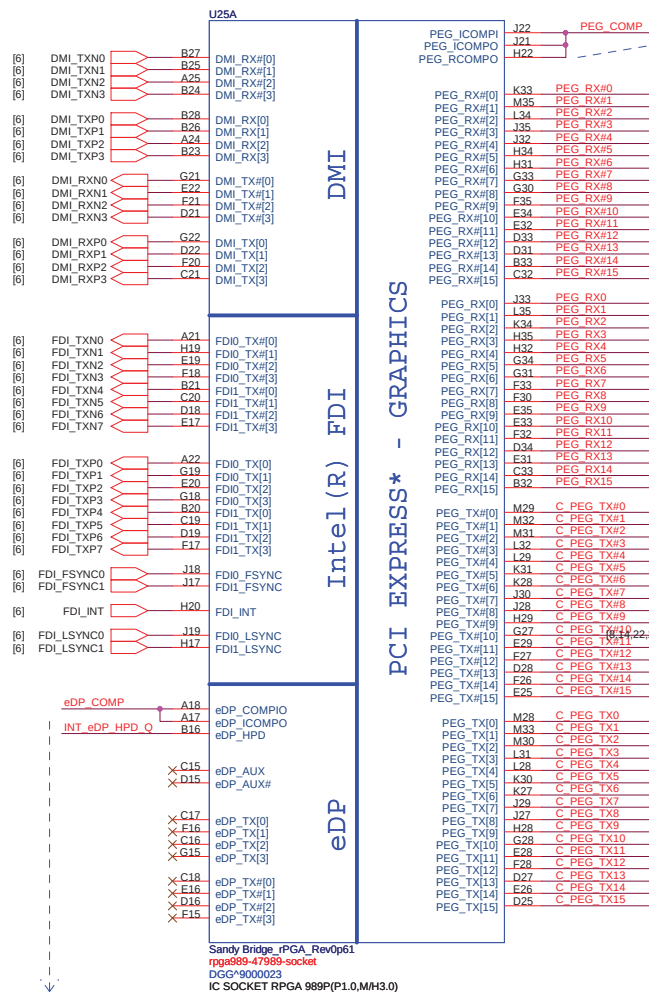
LG2/4 (14"/15.6") MUXLESS and Dis. BLOCK DIAGRAM 01

PCB 8L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT

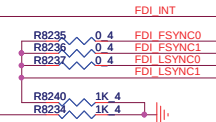


Sandy Bridge Processor (DMI,PEG,FDI)



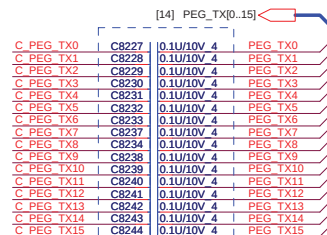
eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils

**FDI disable
(DIS only stuff)**

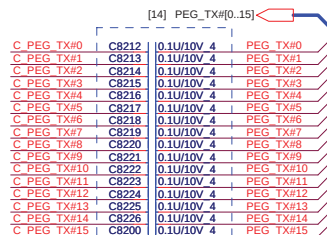


FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

PEG x16 disable (UMA only remove)

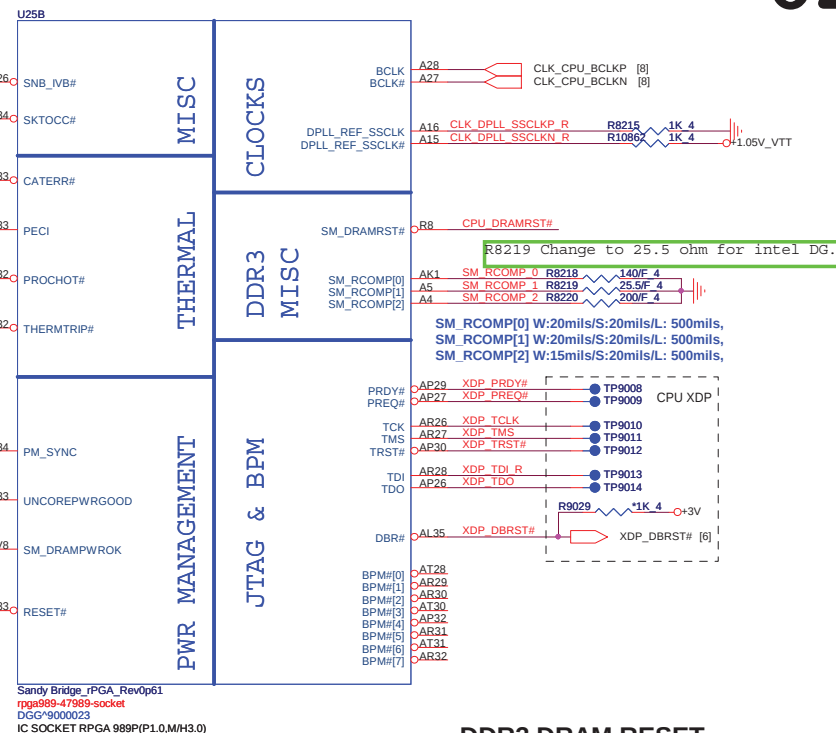


0.22uF AC coupling Caps for PCIE GEN1/2/3

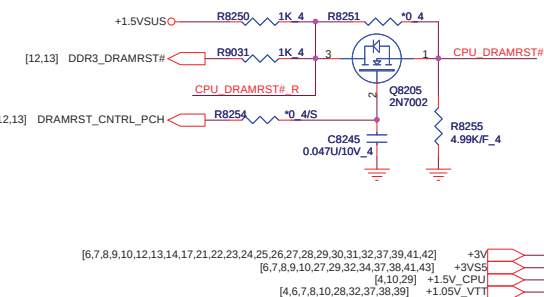


0.22uF AC coupling Caps for PCIE GEN1/2/3

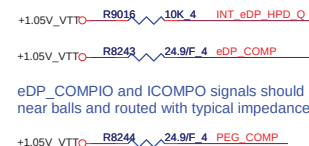
Sandy Bridge Processor (CLK,MISC,JTAG)



DDR3 DRAM RESET



DP & PEG Compensation



eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms
PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

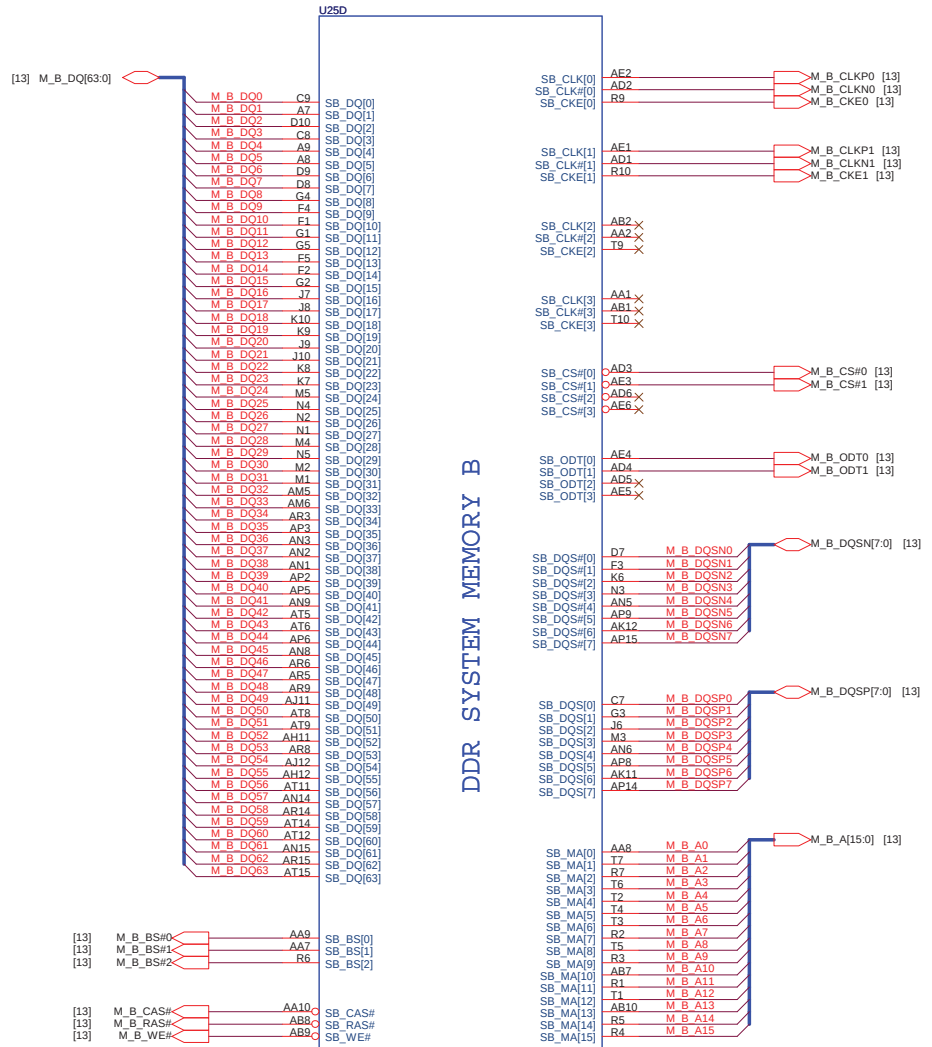
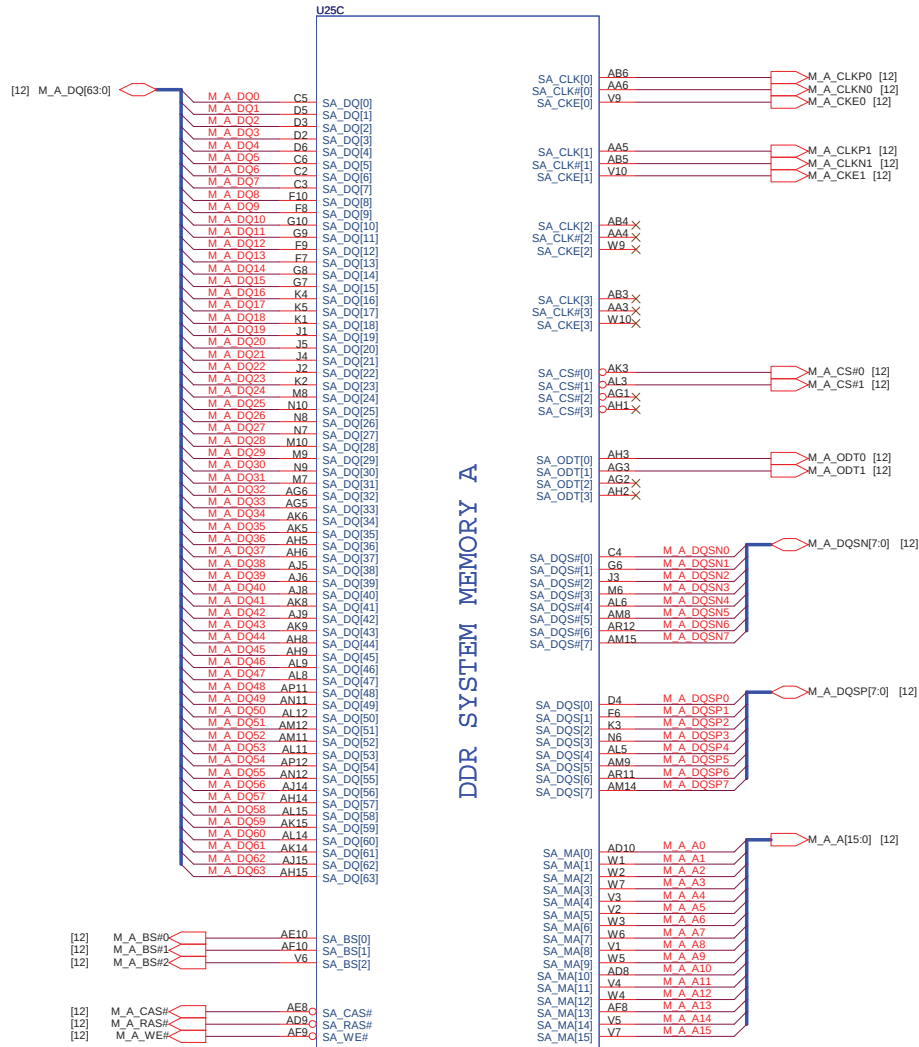
Processor pull-up (CPU)

PROCTHOT# with two VR topology ..100ohm
PROCTHOT# with one VR topology ..62 ohm



PROJECT : LG2/4 DIS
Quanta Computer Inc.

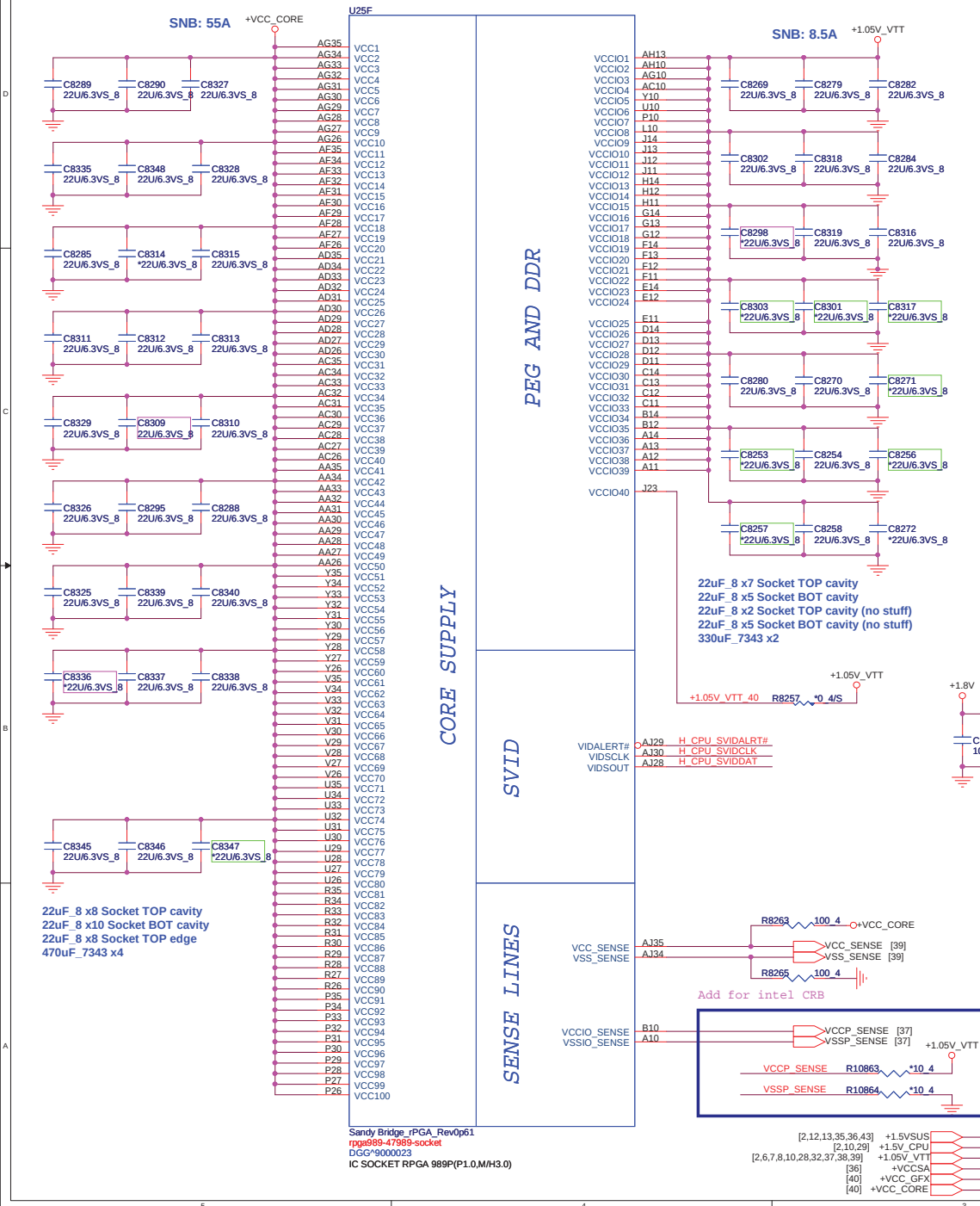
Sandy Bridge Processor (DDR3)



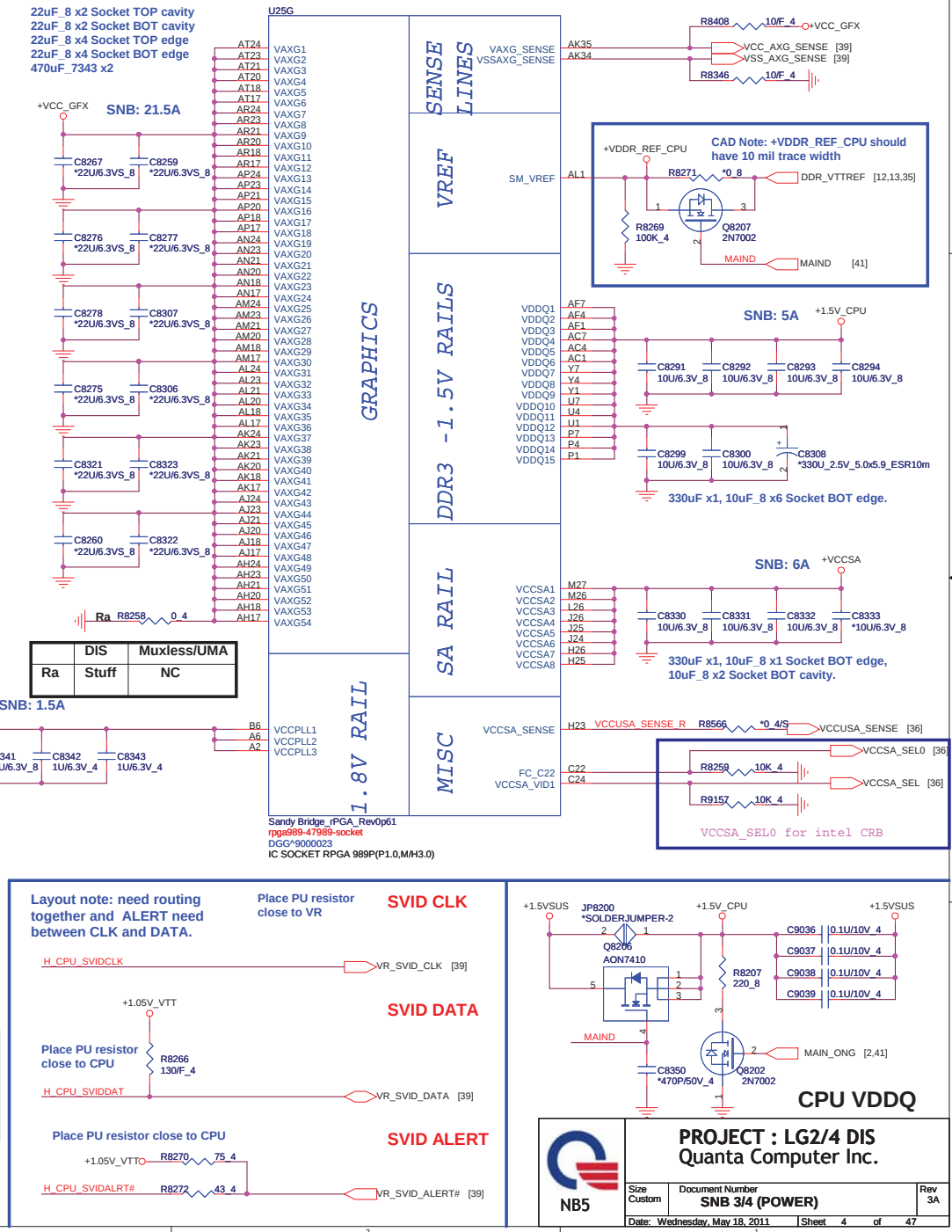
PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 214 (DDR3 I/F)	3A
Date: Wednesday, May 18, 2011	Sheet 3 of 47	

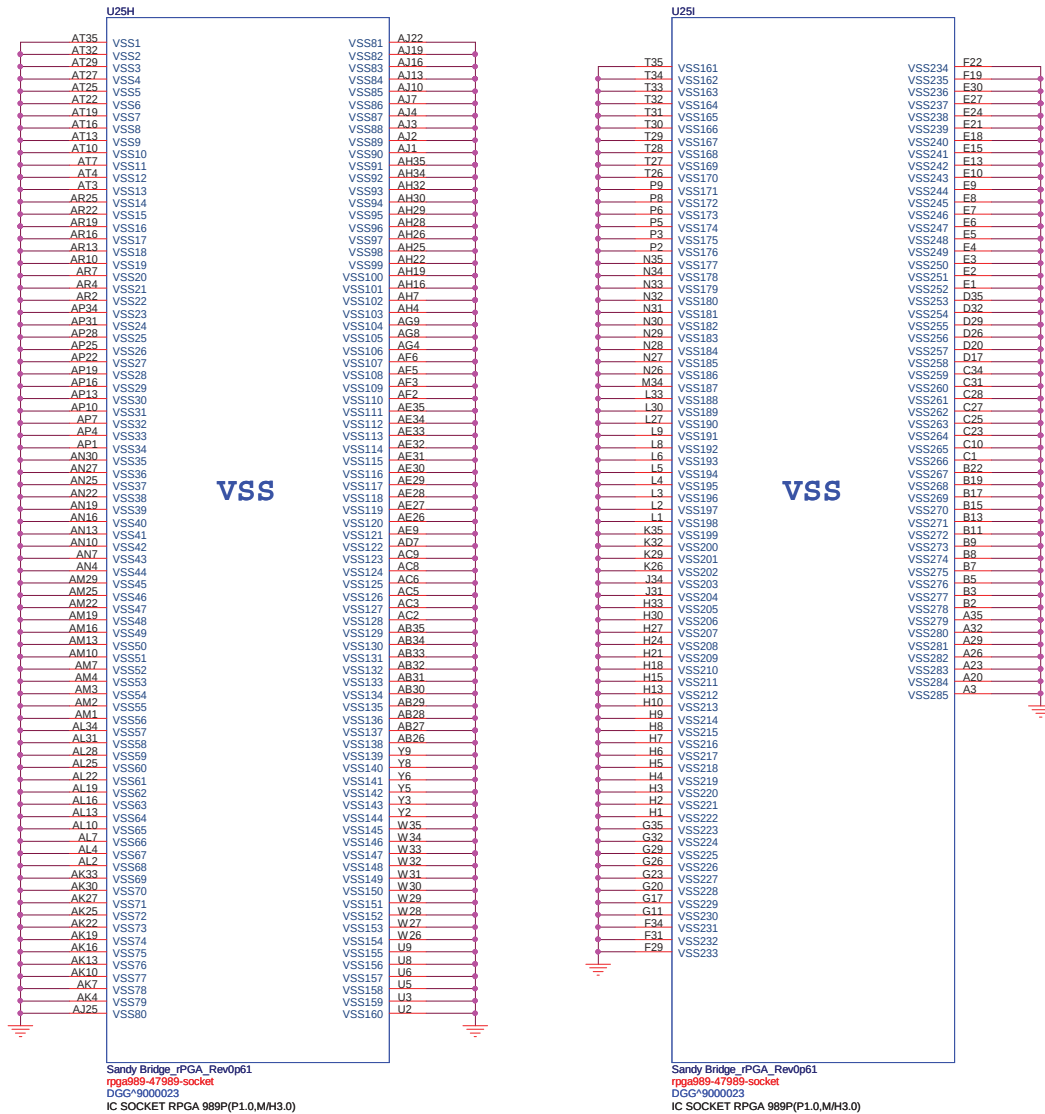
Sandy Bridge Processor (POWER)



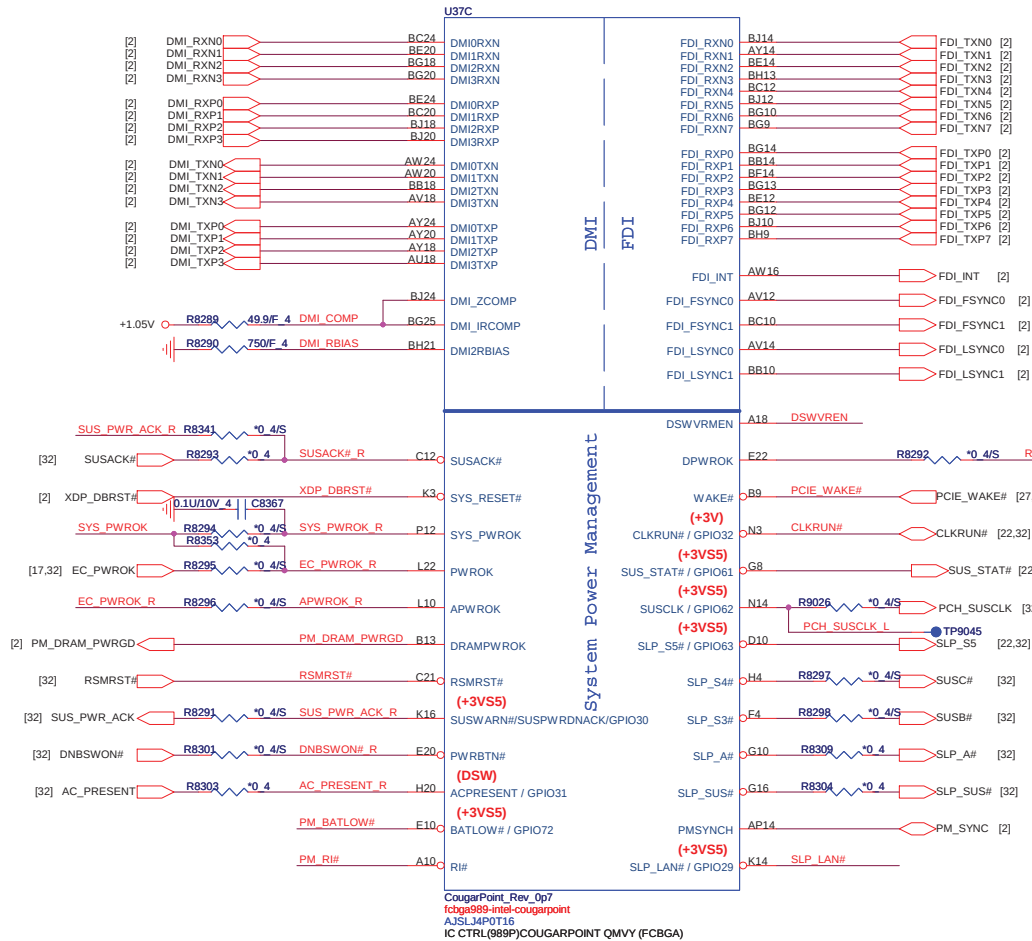
Sandy Bridge Processor (GRAPHIC POWER)



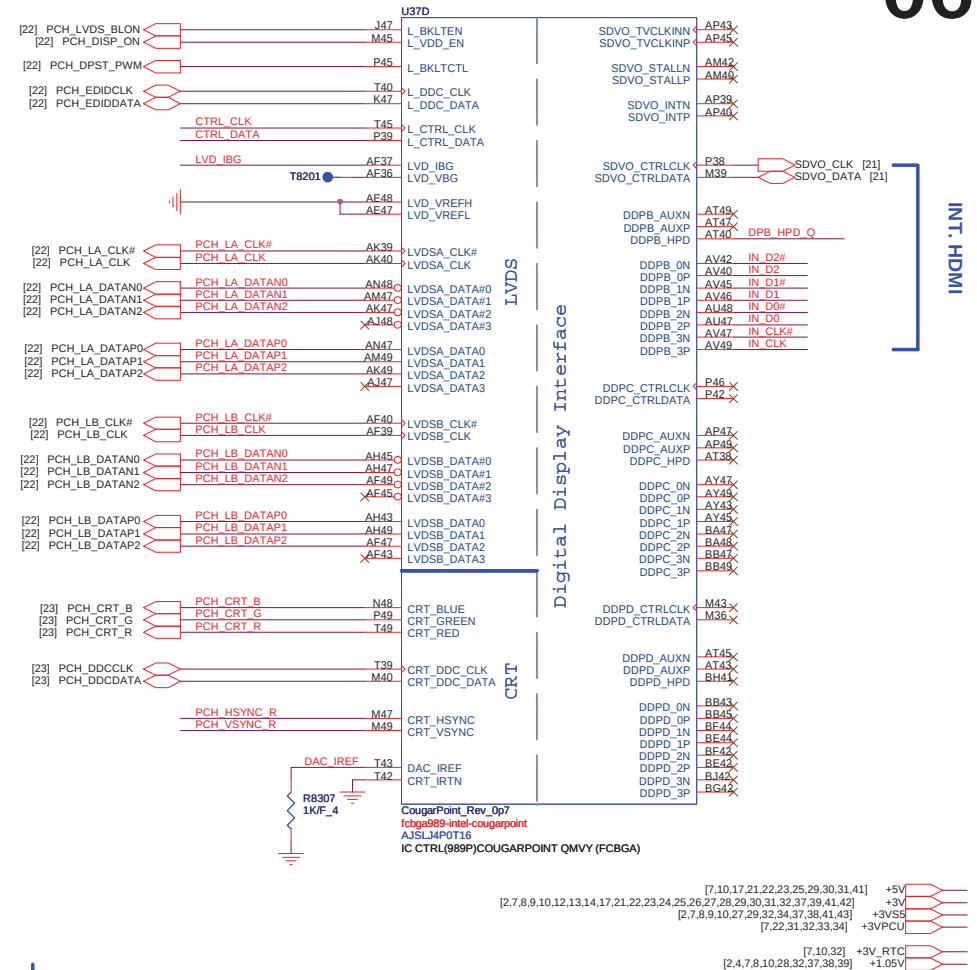
Sandy Bridge Processor (GND)



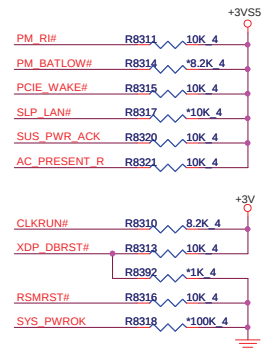
Cougar Point (DMI, FDI, PM)



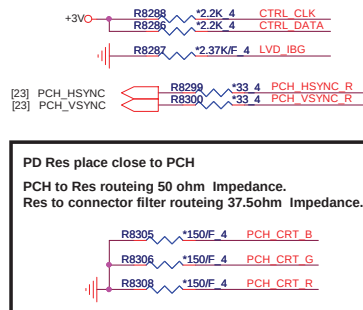
Cougar Point (LVDS,DDI)



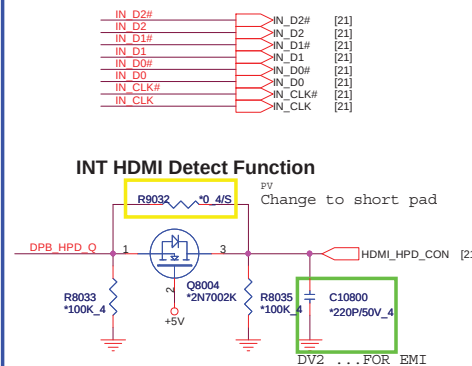
PCH Pull-high/low(CLG)



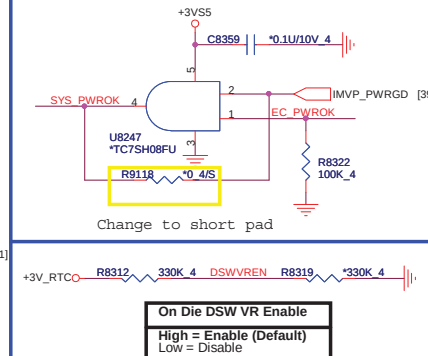
**INT LVDS & CRT disable
(DIS only remove)**



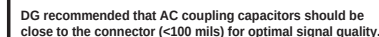
INT HDMI disable (DIS only remove)



System PWR_OK(CLG)



07



MINISATA (SATA1 1.5Gb/s)

RTC Power trace width 20mils.

RTC_RST#

SRTC_RST#

R8323 20K/F_4

R8325 20K/F_4

R8393 0.6/S

R8326 1K_4

C8361 1U/6.3V_4

C8363 1U/6.3V_4

C8364 1U/6.3V_4

D8201 BAT54C

BAT_CONN CN8200

+3V_RTC_0

+3V_RTC_1

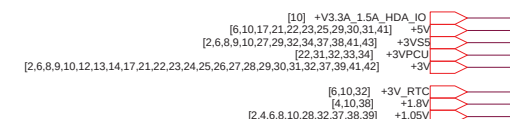
+3V_RTC_2

+3VPCUO

R9119 0.6

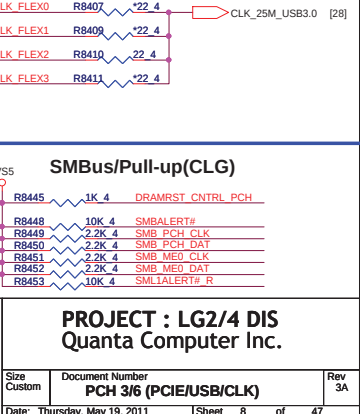
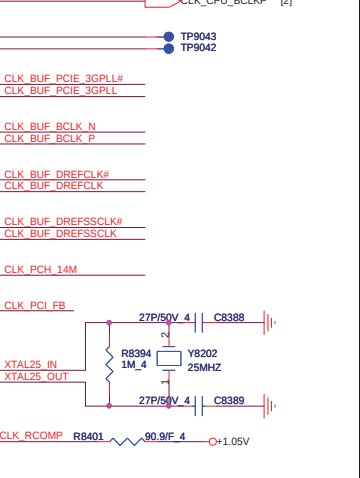
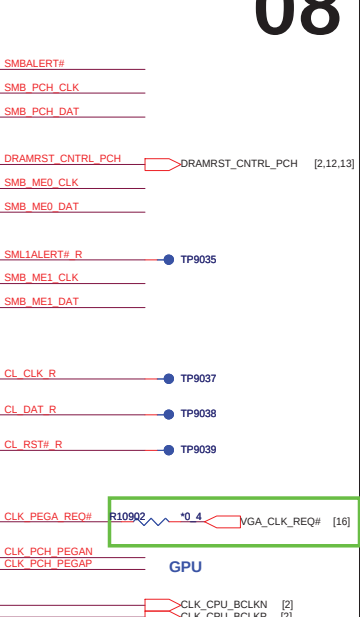
[illegible]

Pin Name	Strap description	Sampled	Configuration	Circuit						
SPKR Different from Calpella	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode							
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)							
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up							
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)							
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <thead> <tr> <th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>SPI LPC</td></tr> </tbody> </table>	GNT1#	GNT0#	Boot Location	0	0	SPI LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GNT1#	GNT0#	Boot Location								
0	0	SPI LPC								
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK								
GNT2# / GPIO53	ESi strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN						
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)							
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm							
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.6V (weak pull-down) 1 = Support by 1.5V							
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)							
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)							
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)							
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable							

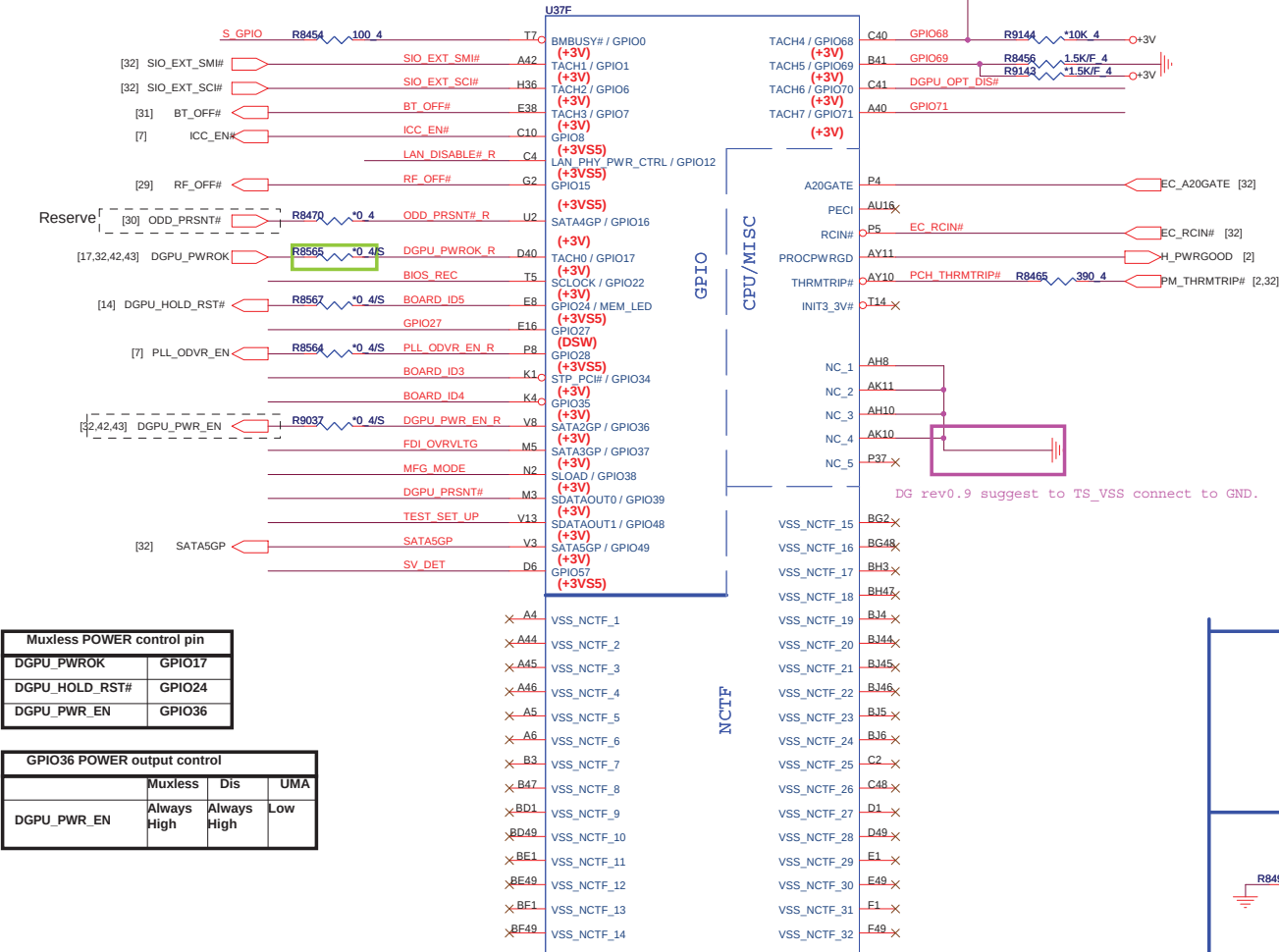


 NB5	PROJECT : LG2/4 DIS Quanta Computer Inc.		
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Cougar Point-M (PCI, USB, NVRAM)



Cougar Point (GPIO,VSS_NCTF,RSVD)



Muxless POWER control pin

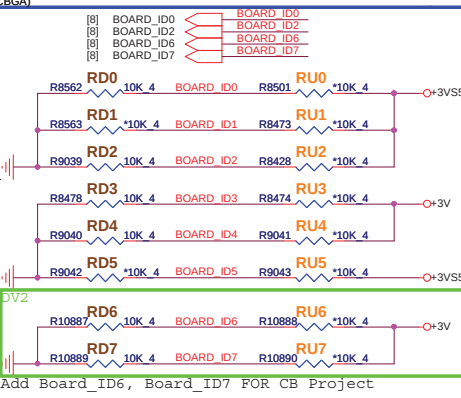
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

GPIO36 POWER output control

	Muxless	Dis	UMA
DGPU_PWR_EN	Always High	Always High	Low

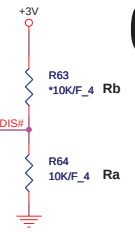
BOARD ID SETTING

Board ID	ID0	ID1	ID2	ID3	ID4	ID6	ID7	GPIO70	GPIO39
LG/CB	0=LG 1=CB								
15.6" / 14"			14"15" 17"	LG6					
17"			ID2 ID3	1 0 0 1 0 0 1 1					
doby					1=YES 0=NO				
DIS/Muxless								1= Muxless 0=DIS	
UMA/VGA								1= VGA 0=UMA	



	Ra	Rb
UMA/Muxless	NC	Stuff
DIS	Stuff	NC

DGPU_OPT_DIS#:
High : Muxless.
Low: Discrete.



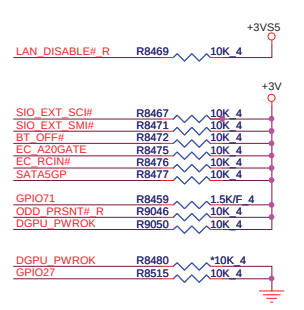
MFG-TEST



SGPIO



GPIO Pull-up/Pull-down(CLG)



Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

BIOS RECOVERY High = Disable (Default)
Low = Enable

TEST SET UP
High = Strong (Default)

TEST DETECT
Low = Default

DMI TERMINATION VOLTAGE OVERRIDE
Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

FDI TERMINATION VOLTAGE OVERRIDE
LOW - Tx, Rx terminated to same voltage

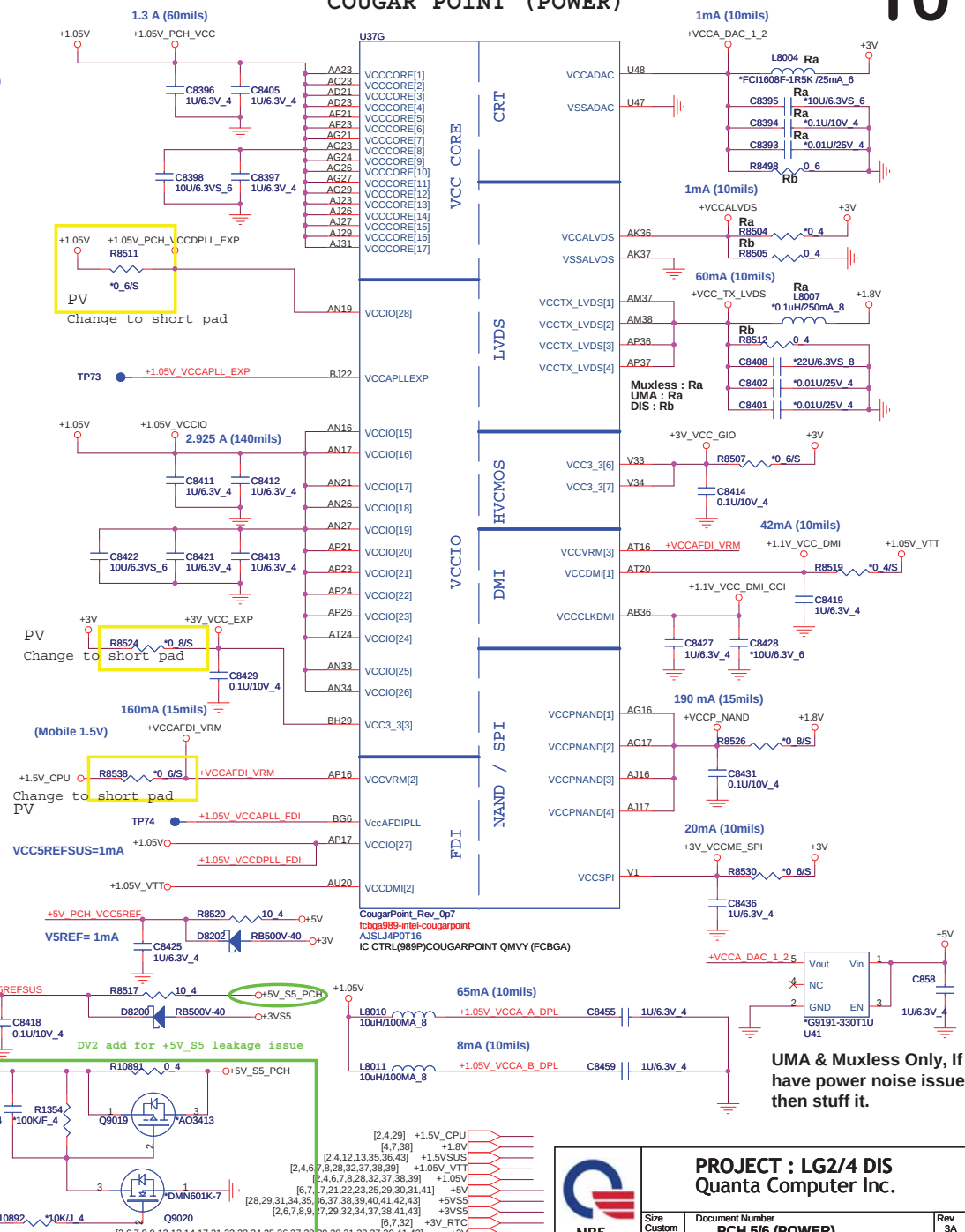
GFX Present

	DIS/Muxless	UMA
Stuff	Ra	Rb
NC	Rb	Ra

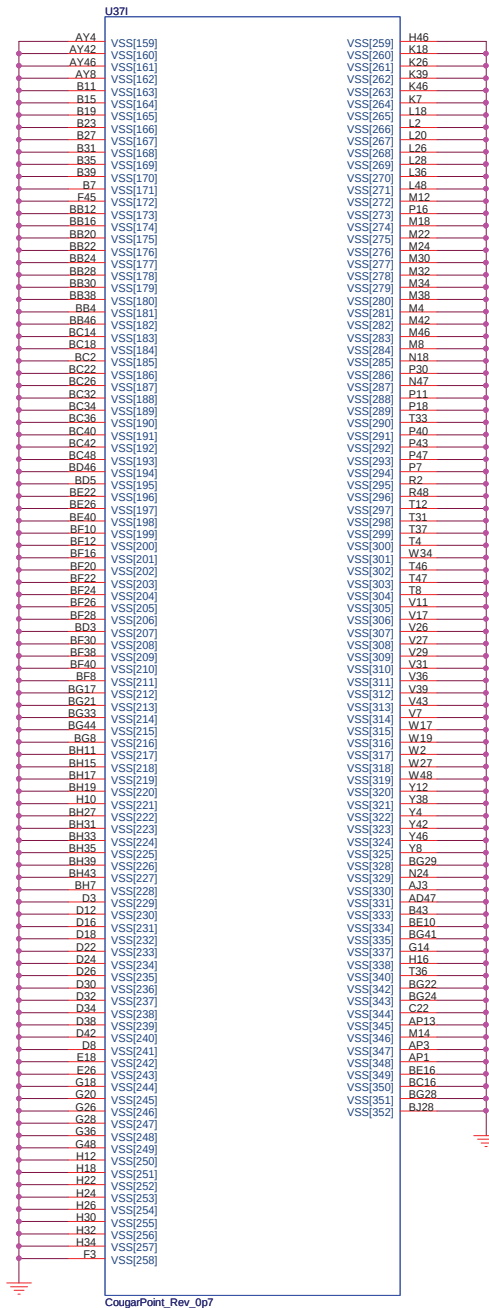
PROJECT : LG2/4 DIS
Quanta Computer Inc.

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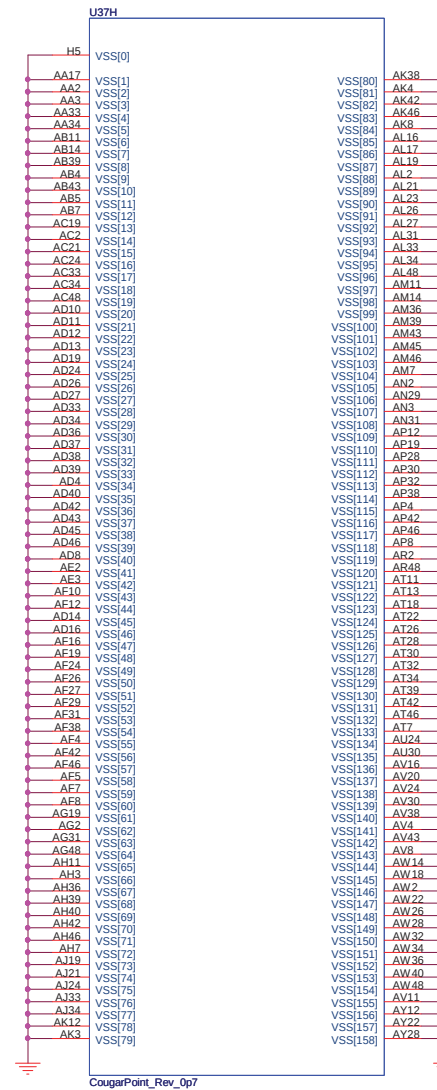
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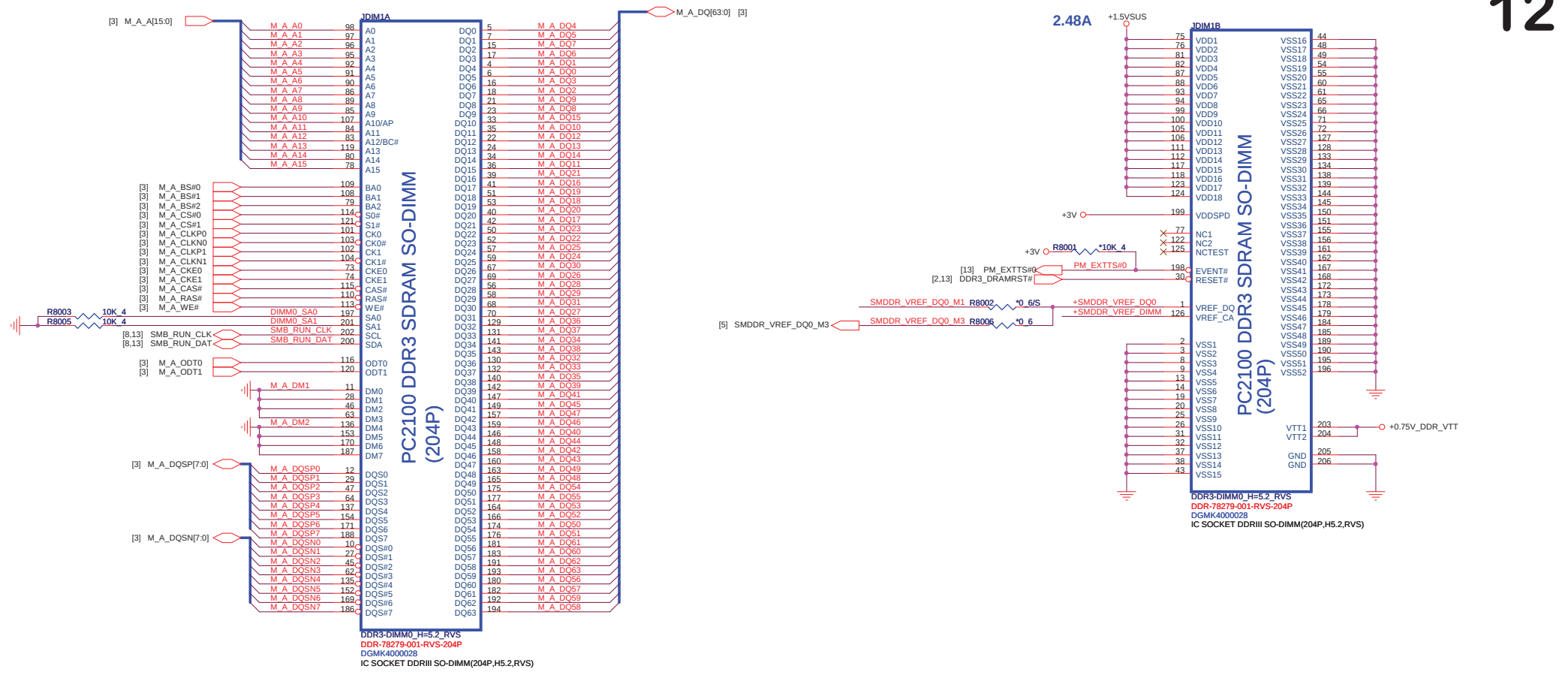


IBEX PEAK-M (GND)

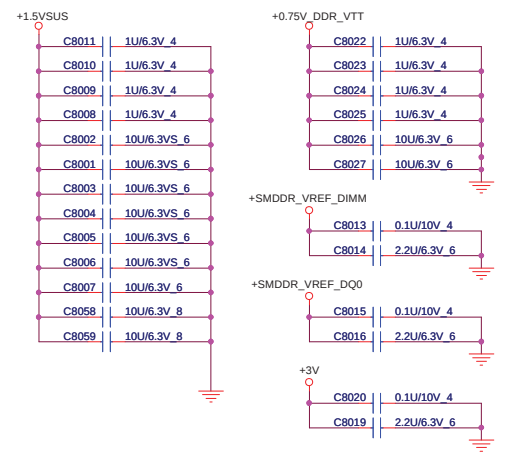


IBEX PEAK-M (GND)

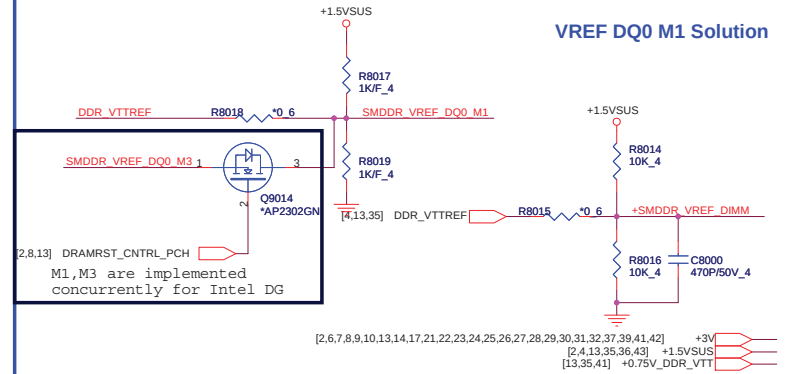


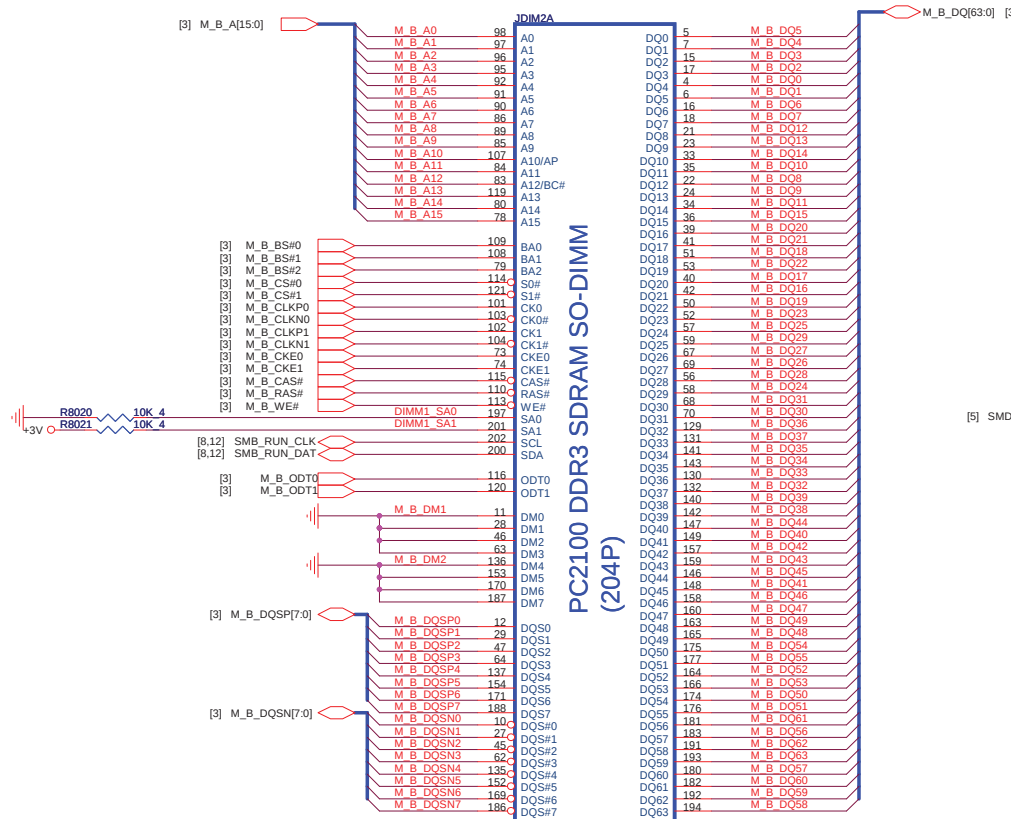


Place these Caps near So-Dimm0.



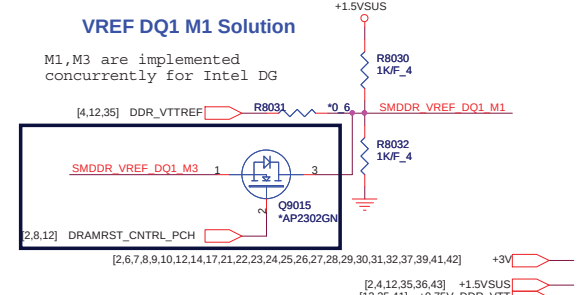
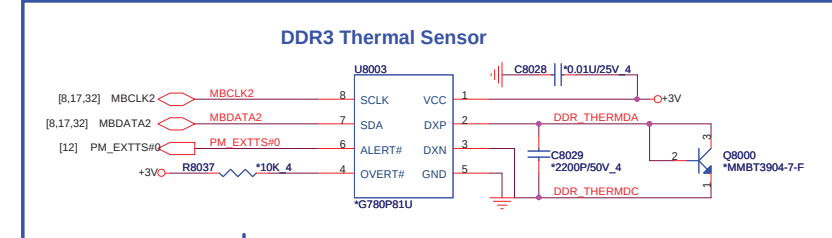
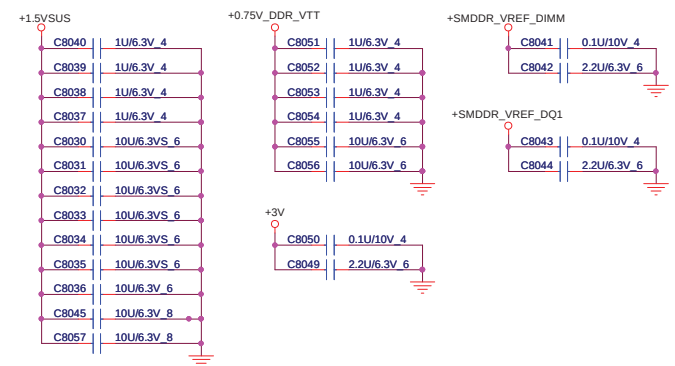
VREF DQ0 M1 Solution

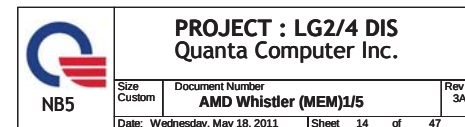




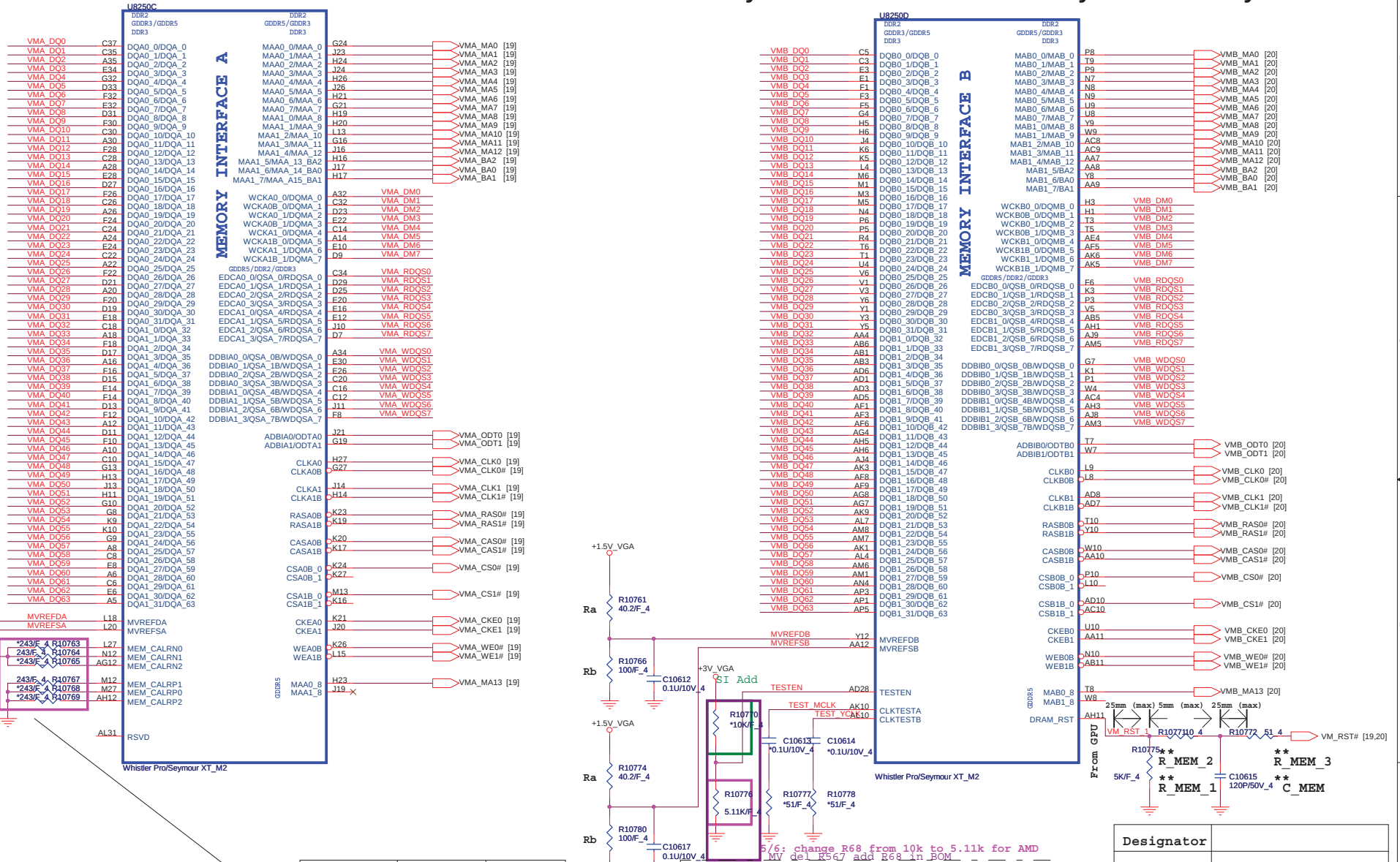
DDR3-DIMM1_H=9.2_RVS
DDR-AS0A626-UARN-7F-204P
DGMK4000029
IC SOCKET DDRIII SO-DIMM(204P,H9.2,RVS)

Place these Caps near So-Dimm1.





Seymour Use Channel B Memory Interface Only



DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

	For Whistler	For Seymour
MEM_CALRNP0	stuff	NC
MEM_CALRNP1	stuff	stuff
MEM_CALRNP2	stuff	NC
MVREFDA	stuff	NC
MVREFSA	stuff	NC

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

** This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and | Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

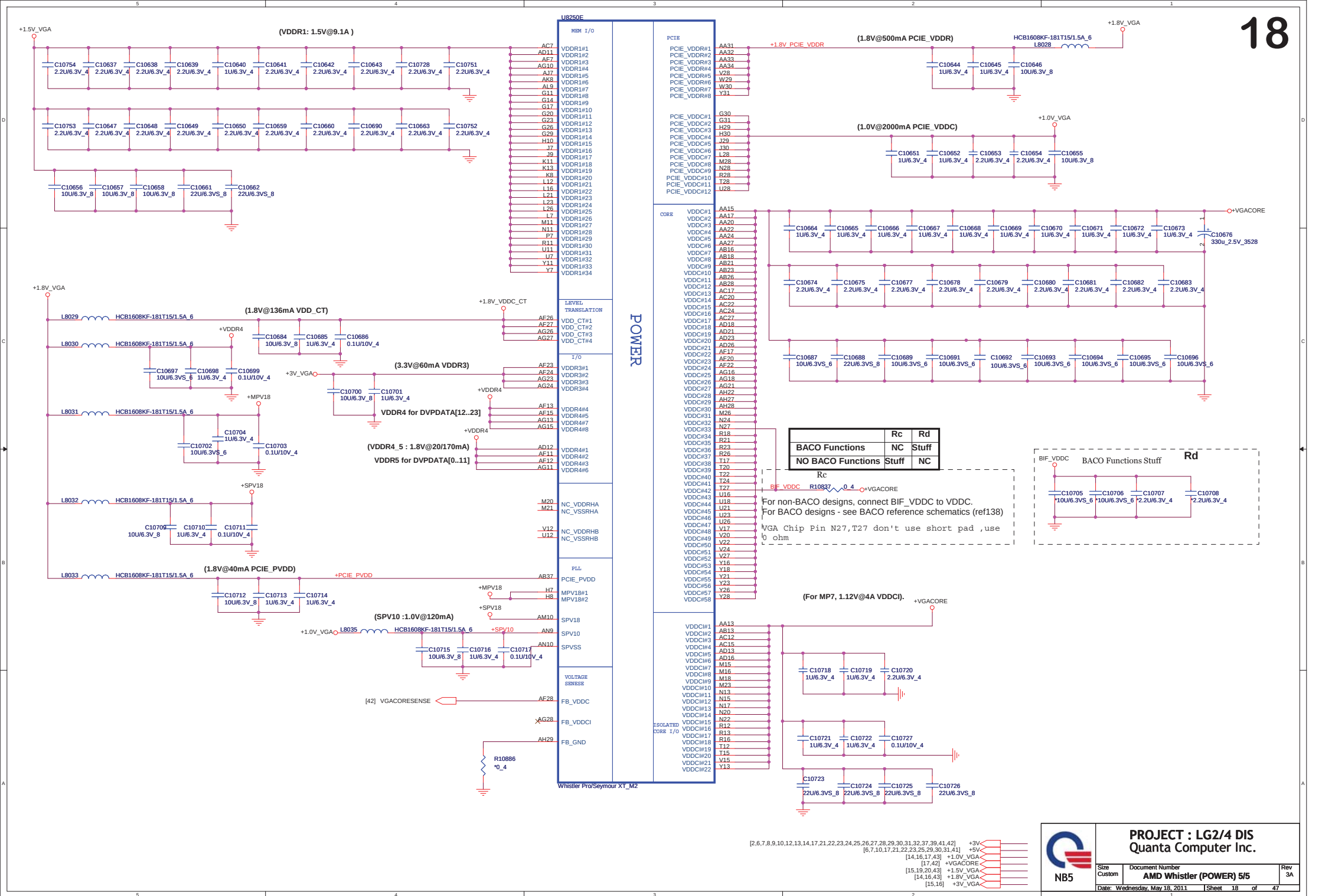
[18,19,20,43] +1.5V_VGA

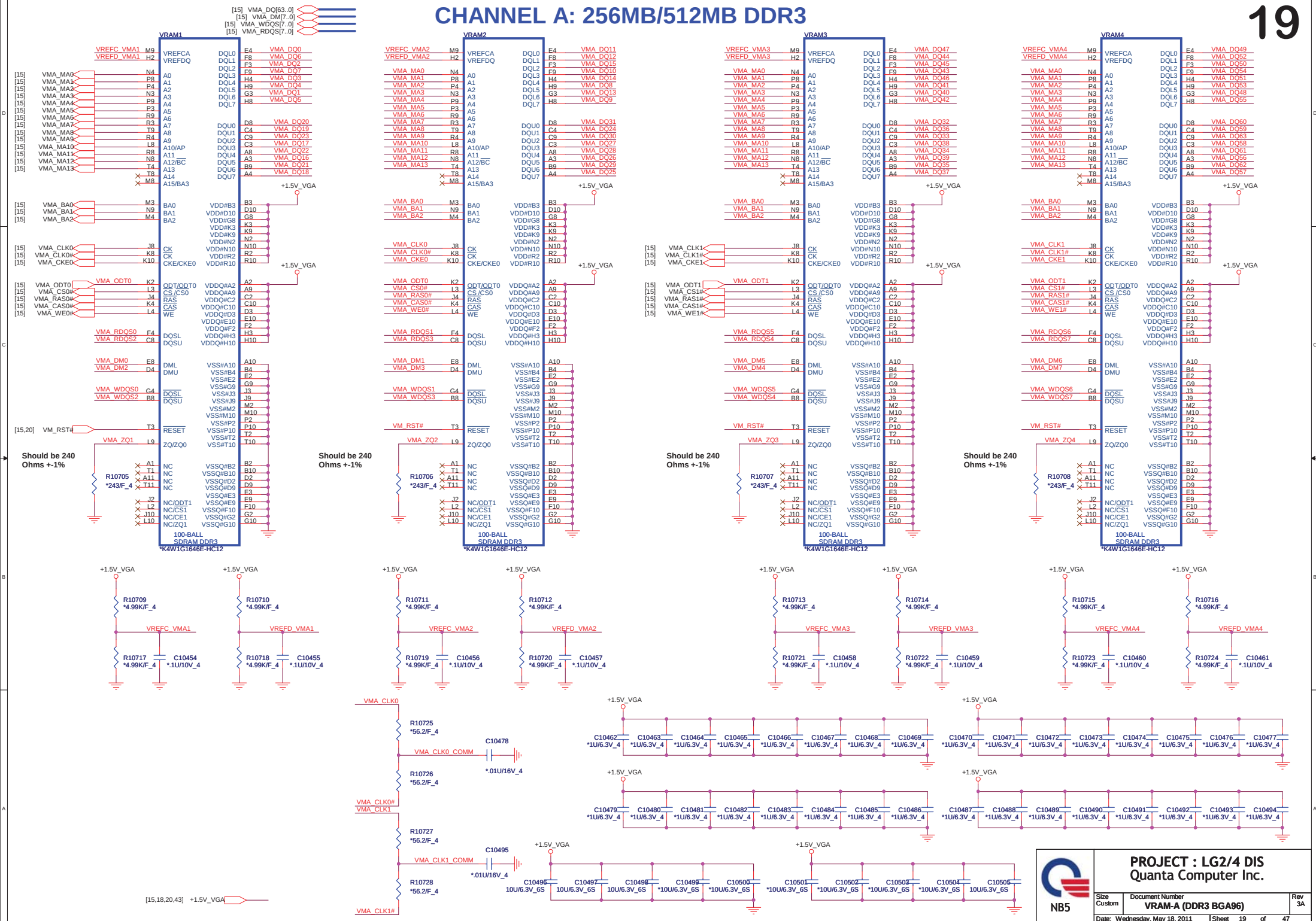


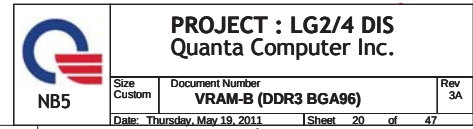


Reserve for support BACO mode

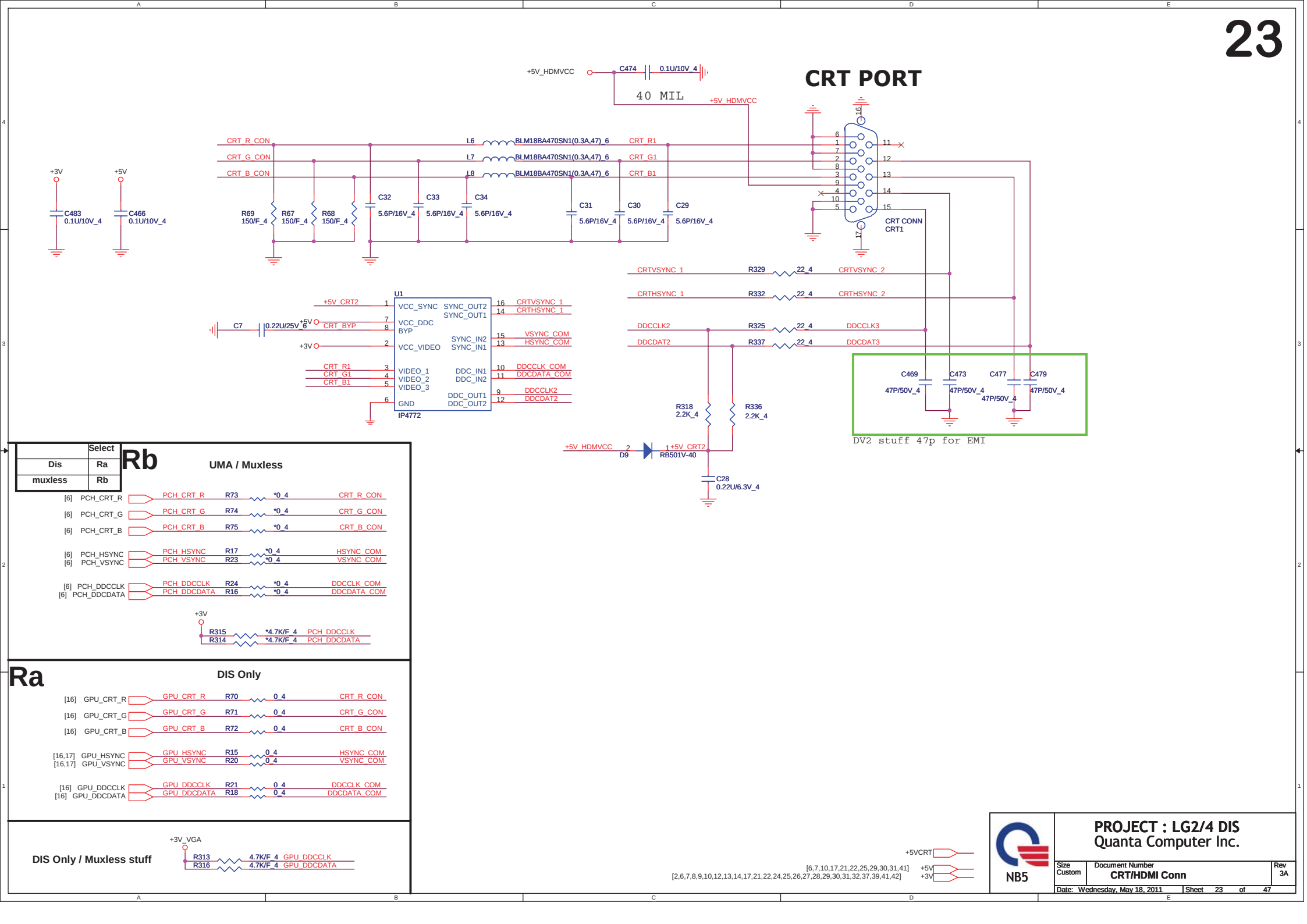
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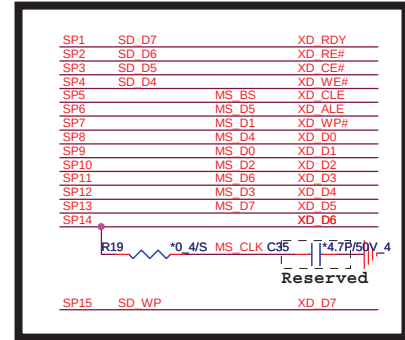
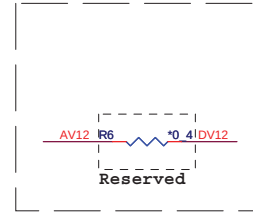
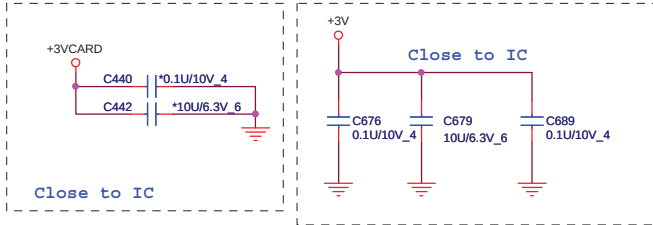






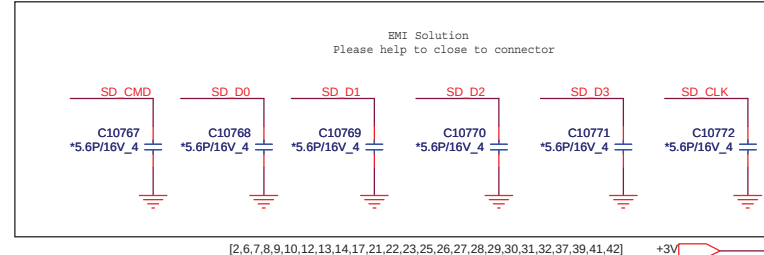
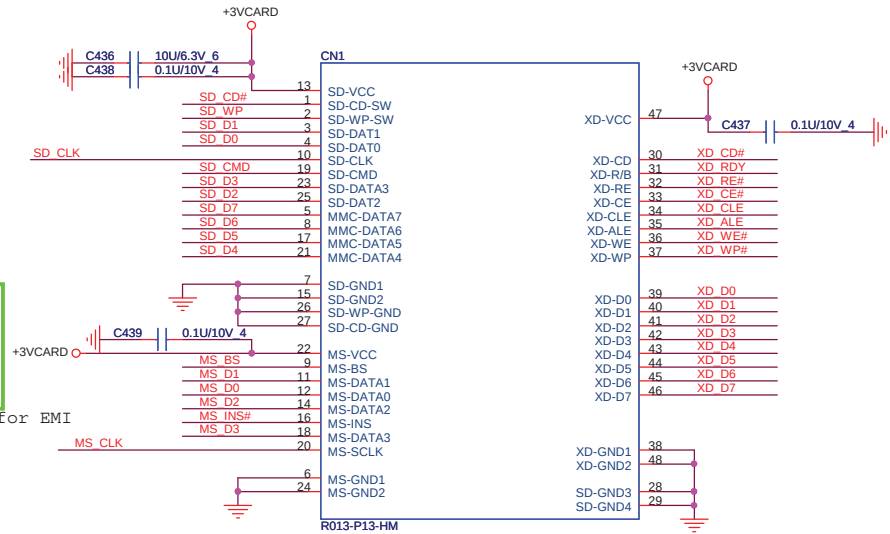
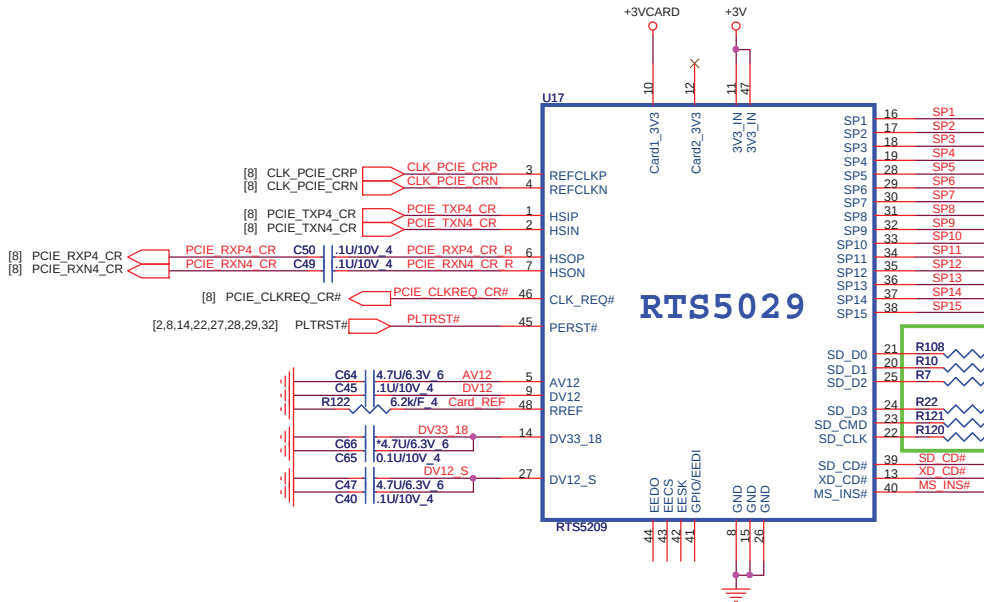
[6, 7, 10, 17, 22, 23, 25, 29, 30, 31, 42]
[2, 6, 7, 8, 9, 10, 12, 13, 14, 17, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 37, 39, 41, 42]





Share Pin

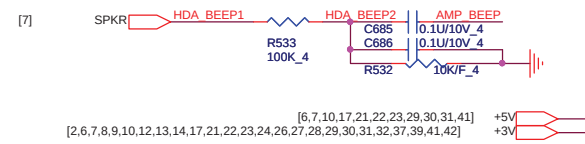
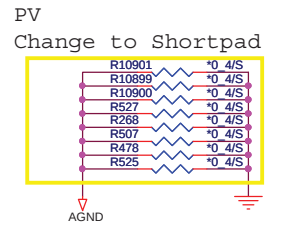
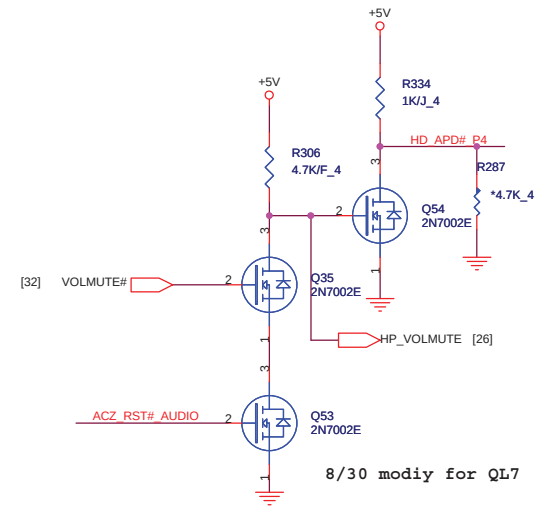
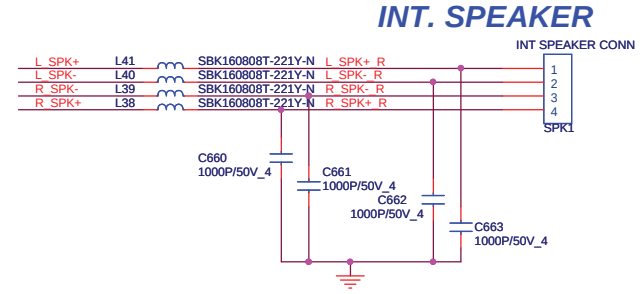
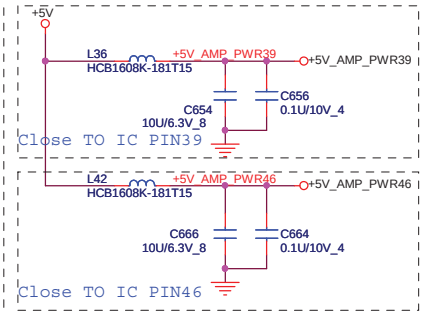
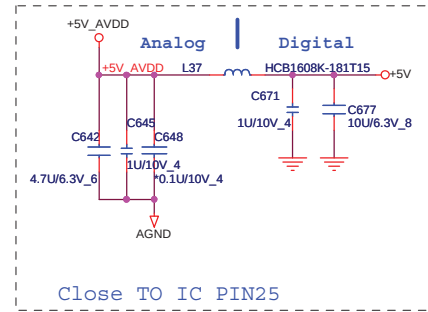
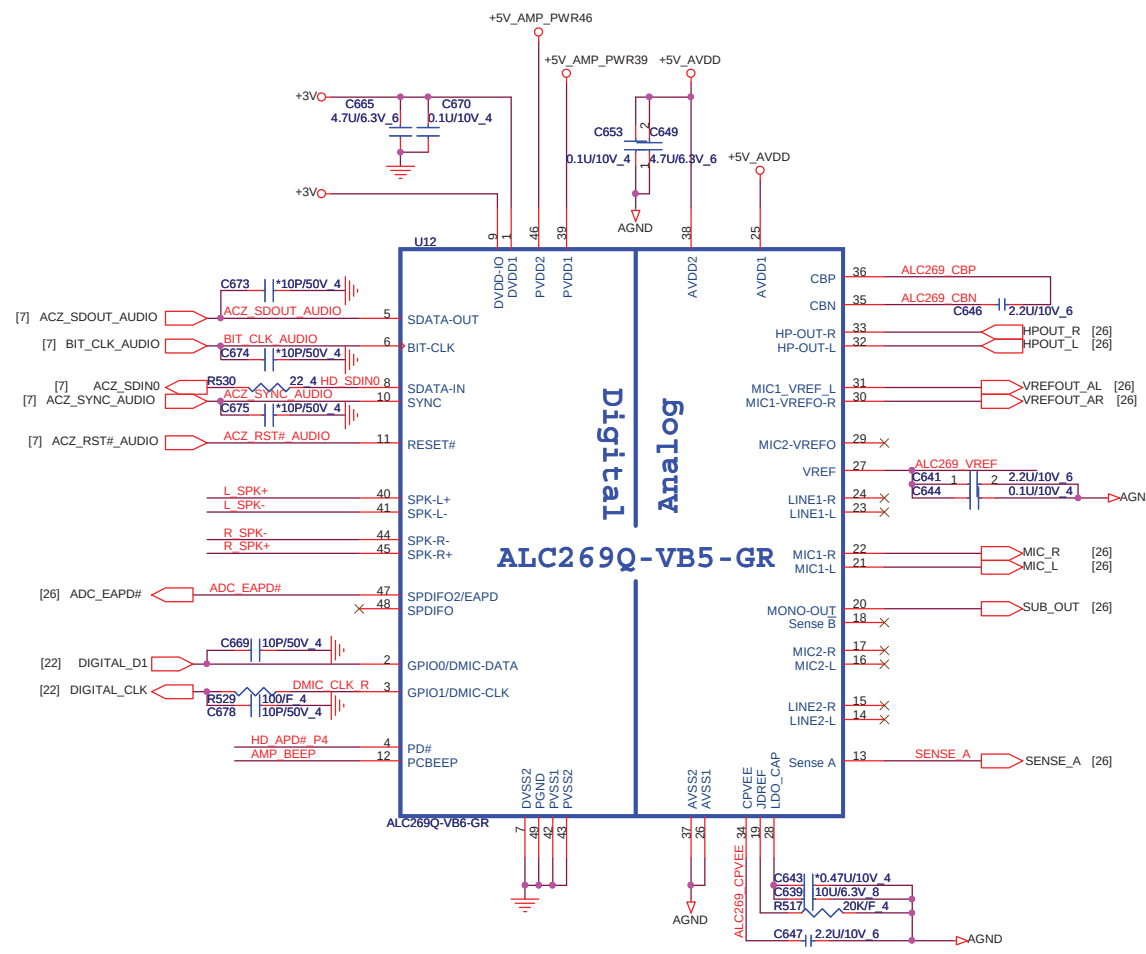
7-in-1 flash media slot(SD / SDHC / SDXC(UHS 104) / MS/MMC/ XD/ MSP)

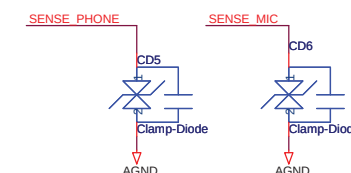
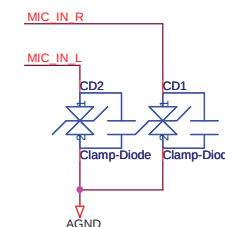
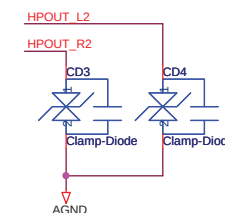




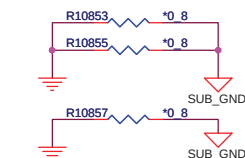
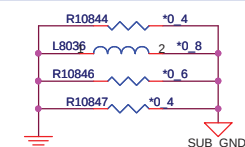
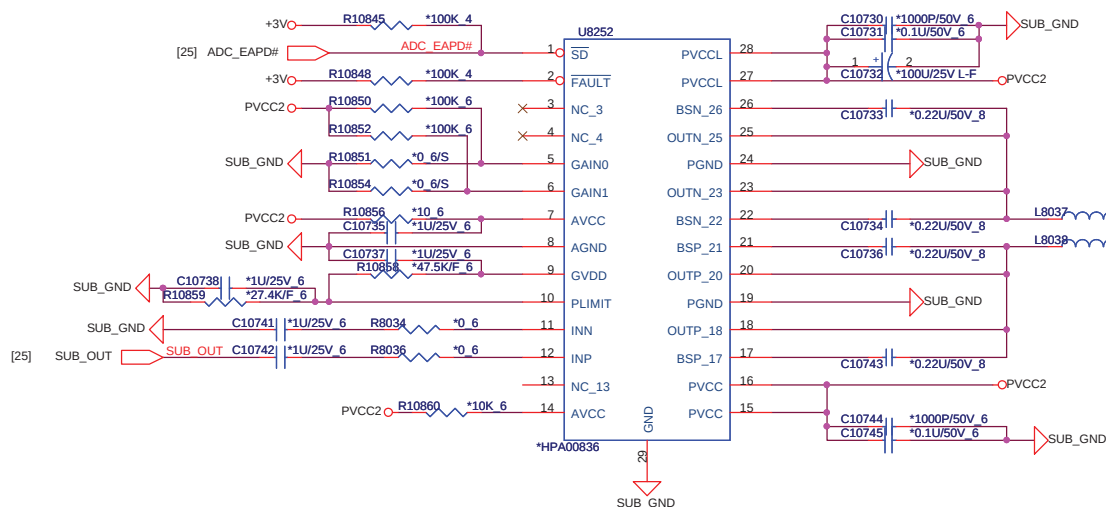
PROJECT : LG2/4 DIS
Quanta Computer Inc.

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PV change to short pad



GAIN1	GAIN0	dB
0	0	12
0	1	18
1	0	23.6
1	1	36

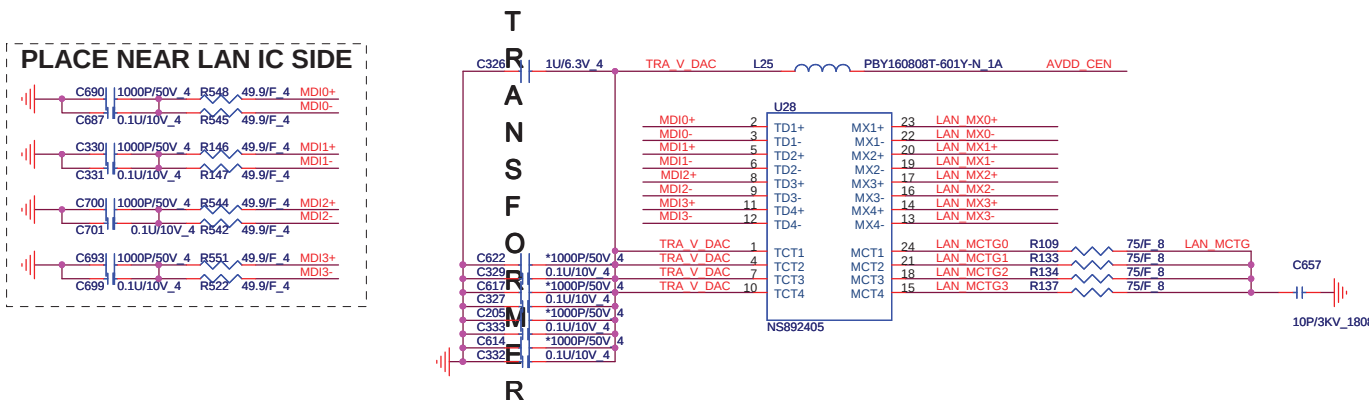
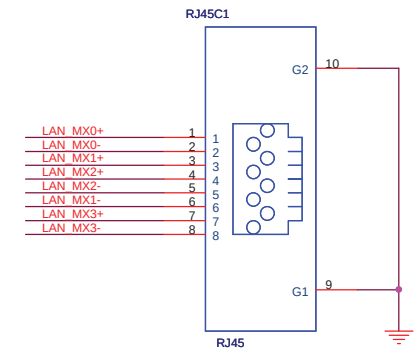
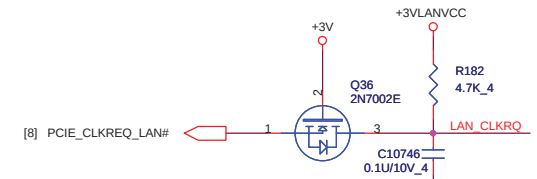
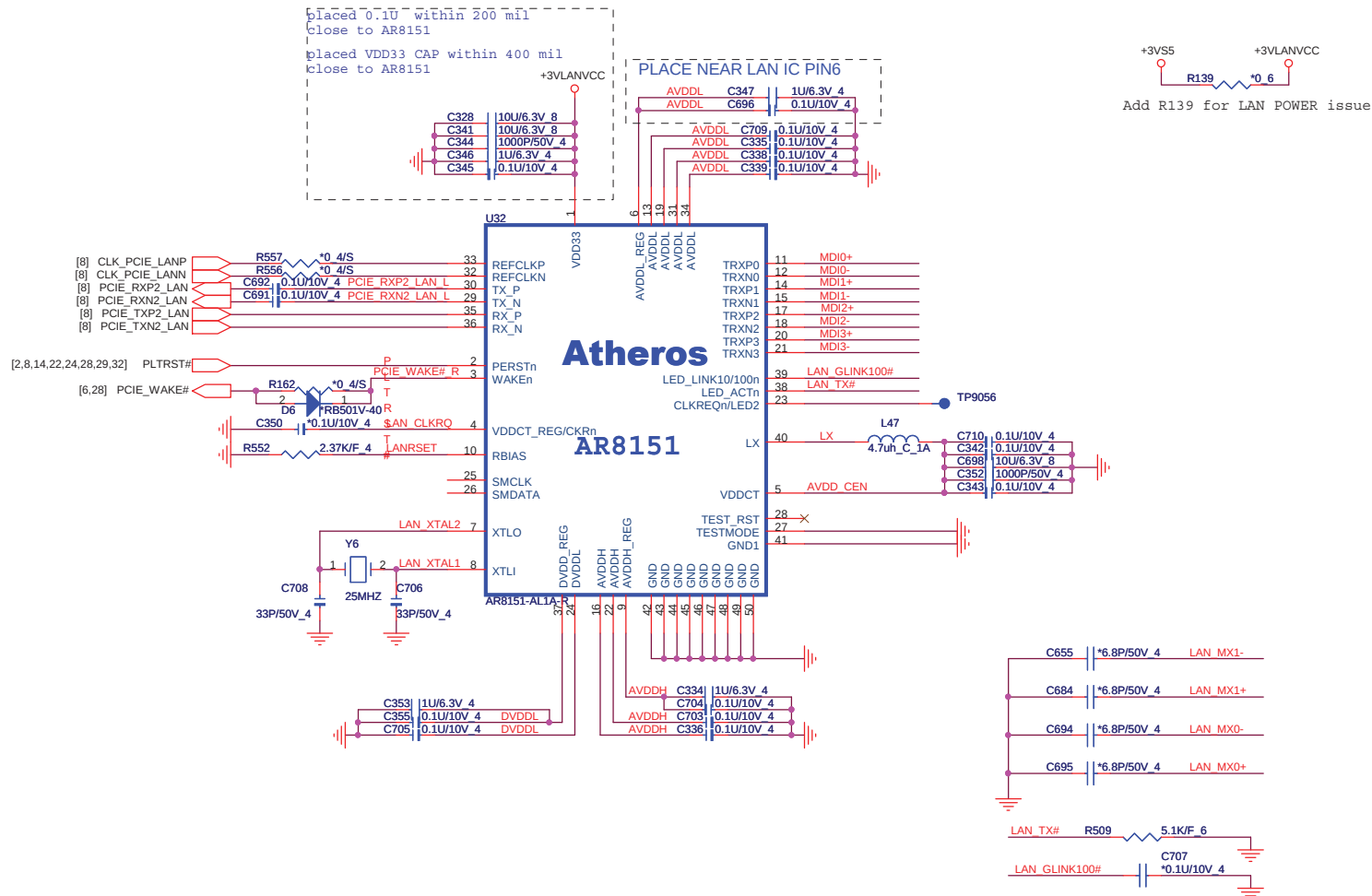
[22,29,33,34,35,36,37,40,41,42,43] +VIN
[6,7,10,17,21,22,23,25,29,30,31,41] +5V
[2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,27,28,29,30,31,32,37,39,41,42] +3V



PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size Custom	Document Number Audio Jack/Accelerometer	R
Date: Wednesday, May 18, 2011	Sheet 26 of 47	

Atheros Lan

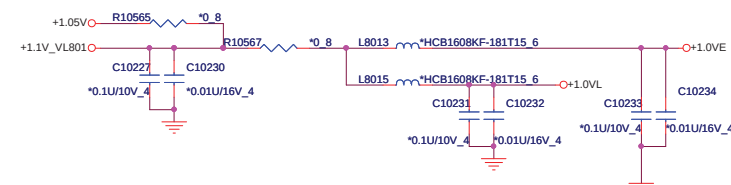
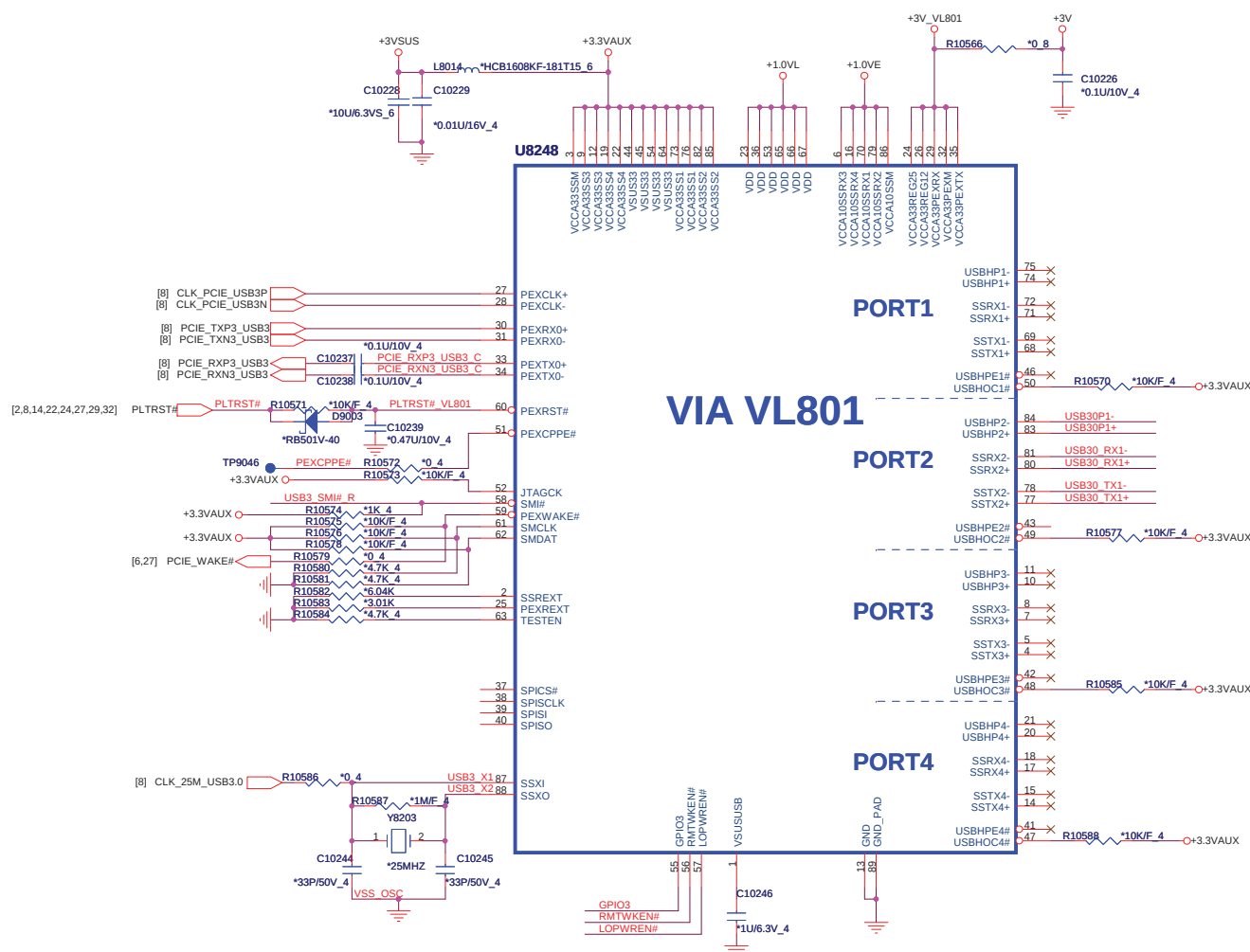


[2,6,7,8,9,10,29,32,34,37,38,41,43] +3VS5
[41] +3VLANVCC
[2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,26,28,29,30,31,32,37,39,41,42] +3V



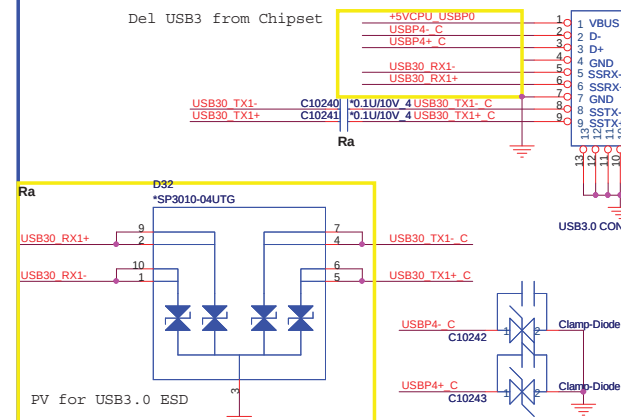
PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size Custom	Document Number LAN AR8151/RJ45	Rev 3A
Date: Wednesday, May 18, 2011		Sheet 27 of 47



USB3.0/USB2.0 x1 COMBO

Del USB3 from Chipset



CTL1	CTL2	CTL3	TPS2540 Control Truth Table
0	0	0	Out Discharge ,Power switch OFF
0	X	1	Dedicated charging port, auto-detect (DCP)
X	1	0	Standard downstream port, USB 2.0 Mode.(SDP)
1	1	1	Charging downstream port, BC1.2 (draft).(CDP)

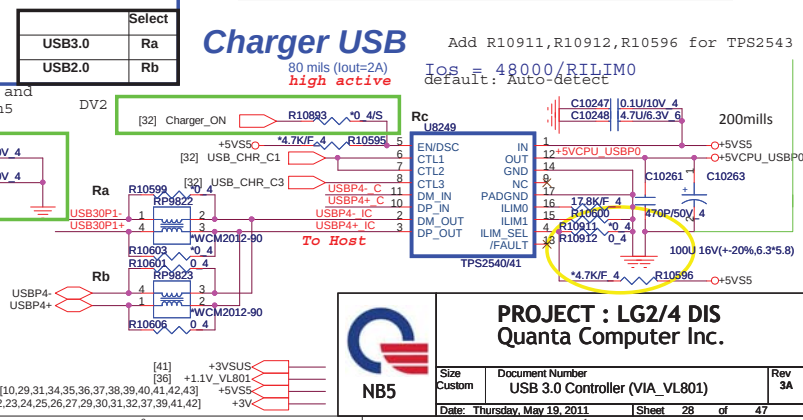
LGE SPEC	S0/S3		S4/S5	
	AC Mode	DC Mode	AC Mode	DC Mode
change mode	CDP	CDP	DCP	DCP
user define Battery % and wake up from USB		SDP		OFF

Charger USB

Add R10911,R10912,R10596 for TPS2543

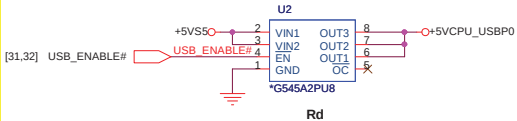
80 mils (lout=2A)
high active

`Ios = 48000/RILIM0`
default: Auto-detect



	Power switch select
LG	Rc
CB	Rd

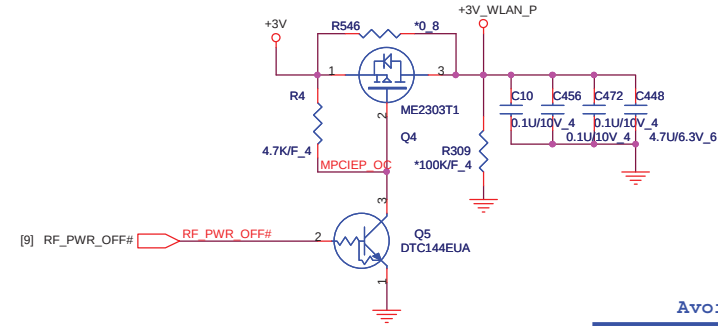
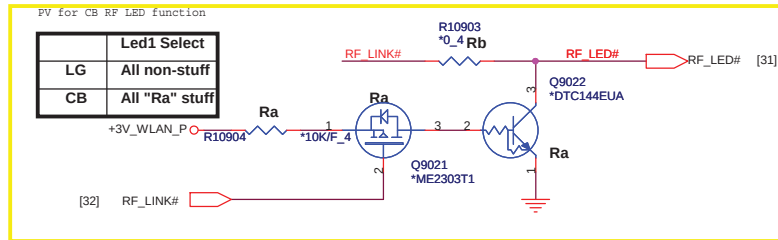
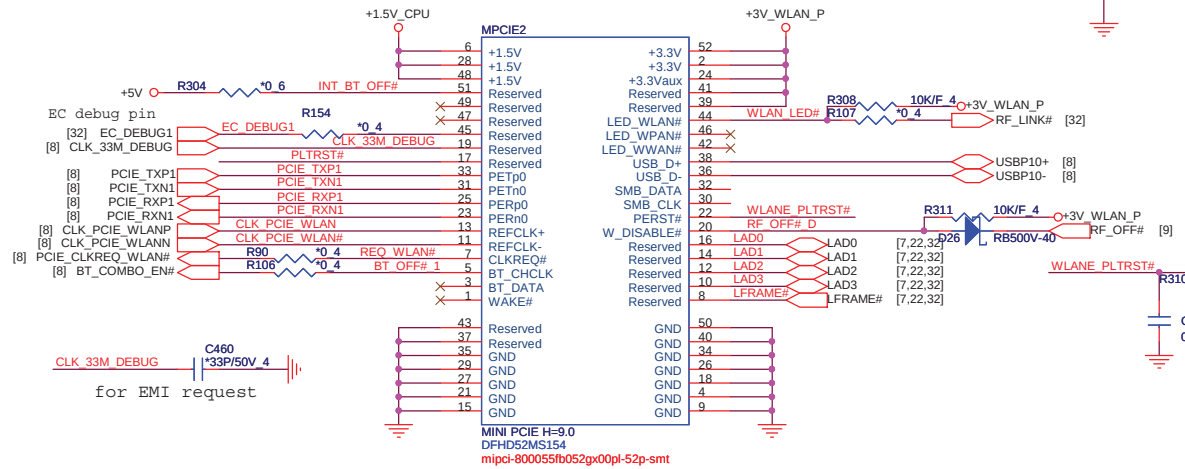
PV USB Power switch for CB



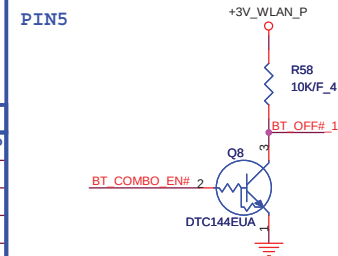
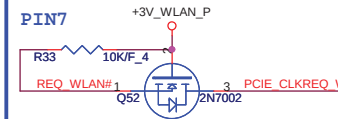
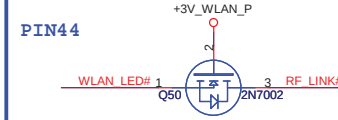
PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size Custom	Document Number USB 3.0 Controller (VIA_VL801)	Rev 3A
Date: Thursday, May 19, 2011	Sheet 28 of 47	

Mini PCI-E Card 1 - Half WLAN

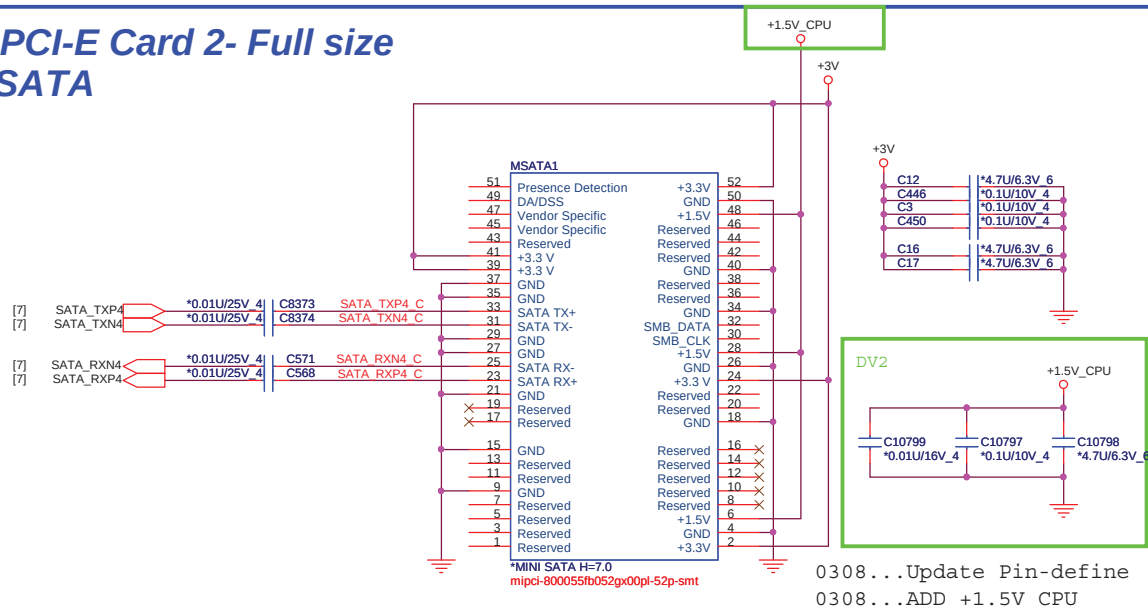


Avoid leakage issue

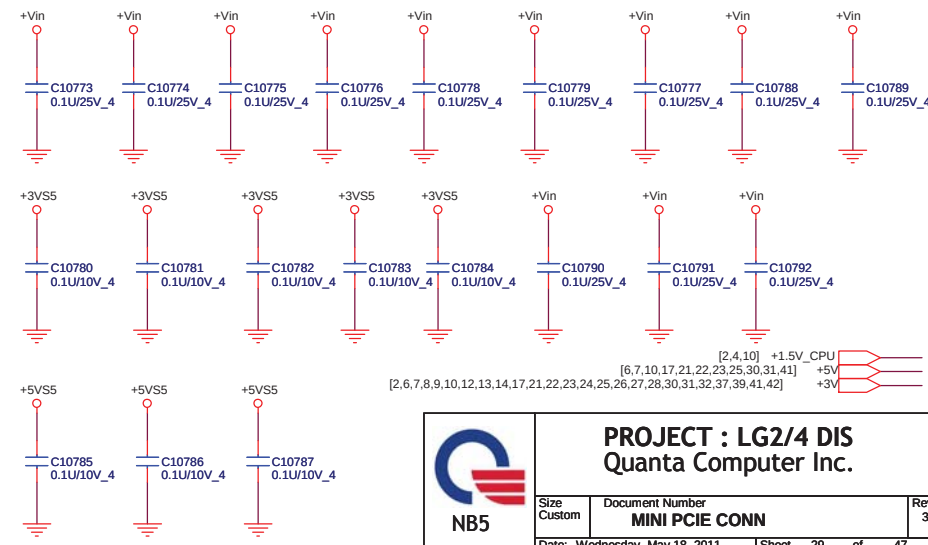


LGE mini-pcie power status		
WLAN	Bluetooth	+3V WLAN P
Radio-ON	Radio-ON	Power-ON
Radio-ON	Radio-OFF	Power-ON
Radio-OFF	Radio-ON	Power-ON
Radio-OFF	Radio-OFF	Power-OFF

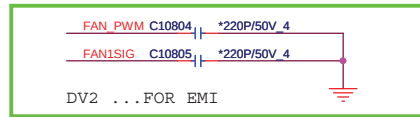
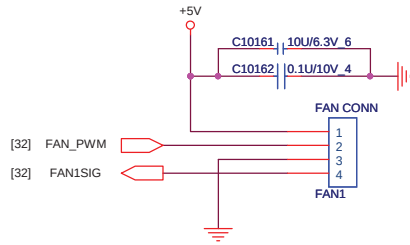
Mini PCI-E Card 2- Full size MINISATA



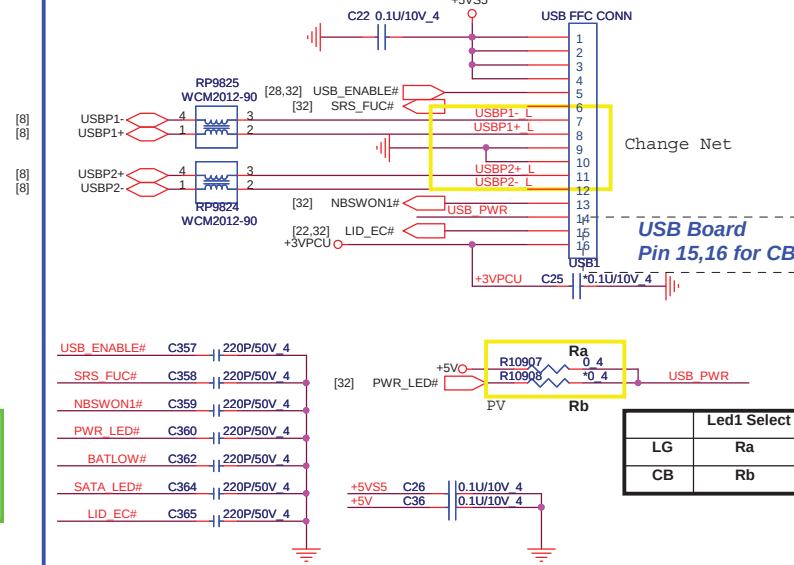
Power Plan Cap for EMI



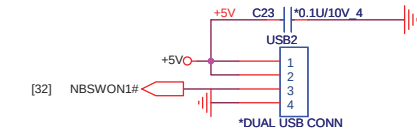
CPU FAN



USB / Power LED & SW for 14"/15"/17" To USB Board



Power SW for 17"

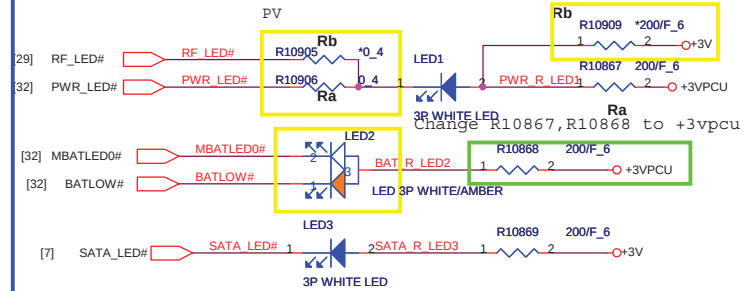


LED Select Pin

Led1 Select	
LG	Ra
CB	Rb

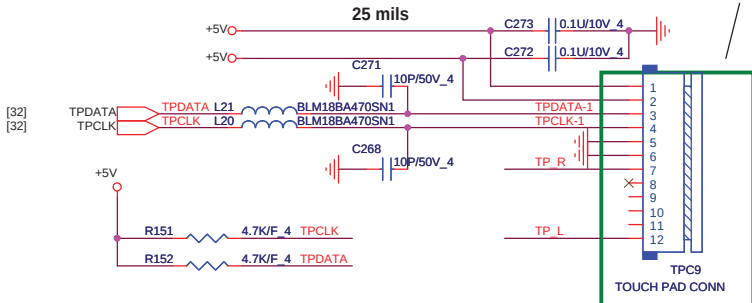
Led2 P/N	
LG	BEWH0051Z00
CB	BEWY0007ZA0

10 mils (250mA)

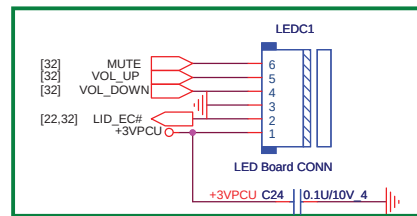


TOUCH PAD CONNECTOR To Click Board & FP

Update TPC9 footprint & P/N...0303

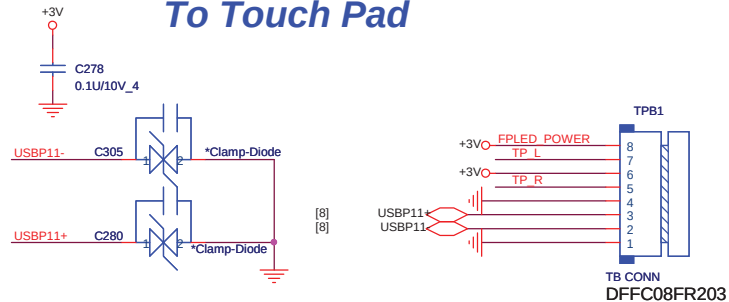


LID / MUTE / VU UP / VU DO To AD Function Board

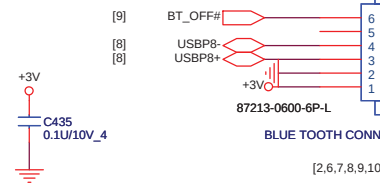


Update LEDC1 footprint & P/N...0303
DV2 ...FOR EMI

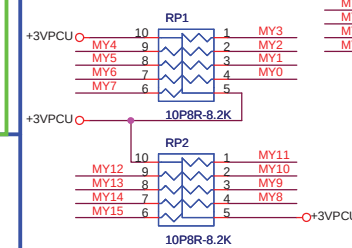
TP Button CONNECTOR To Touch Pad



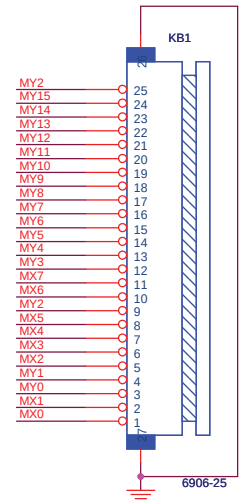
BLUETOOTH



KEYBOARD PULL-UP



KEYBOARD Con.

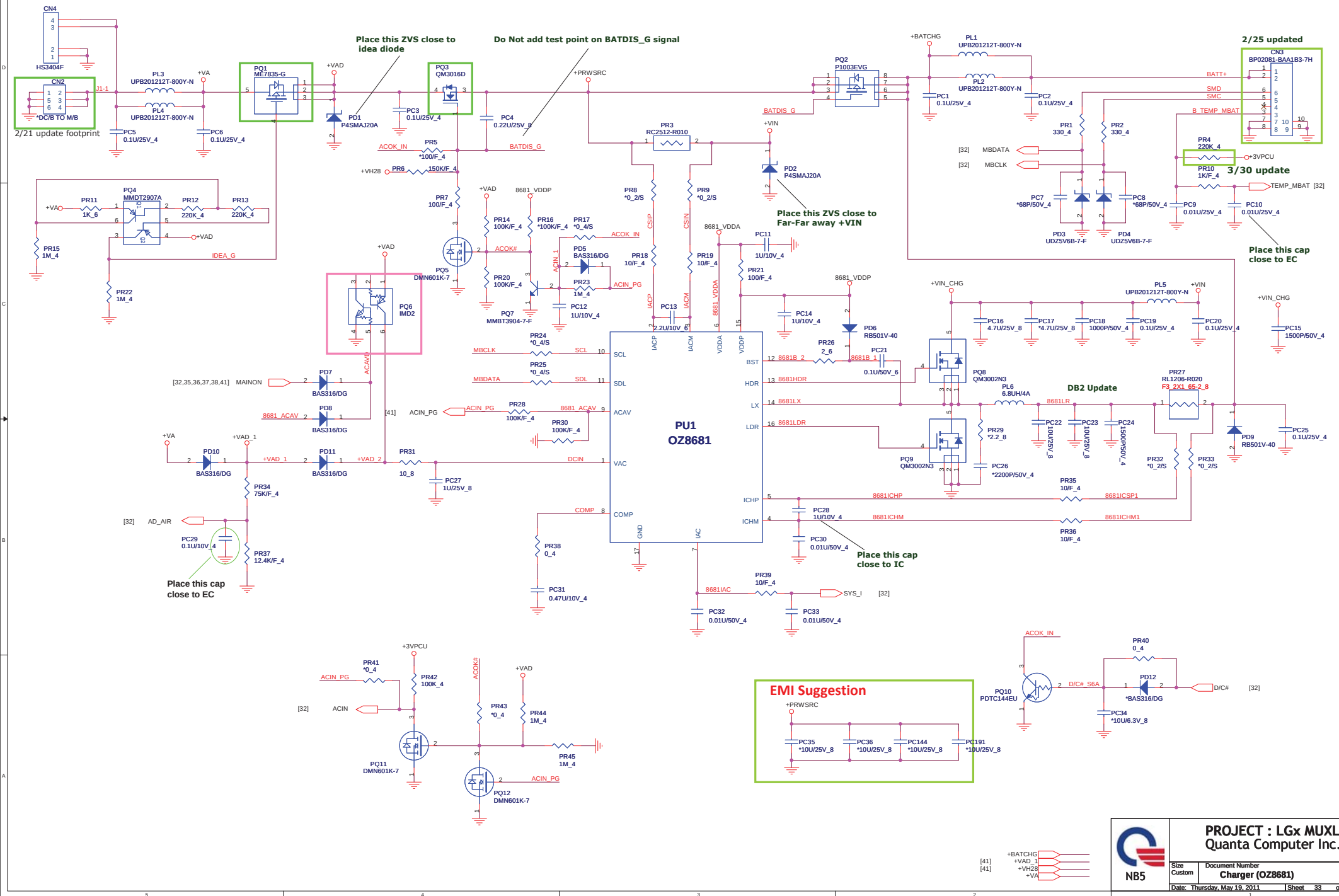


PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT/USB/eSATA	3A
Date: Wednesday, May 18, 2011	Sheet 31 of 47	

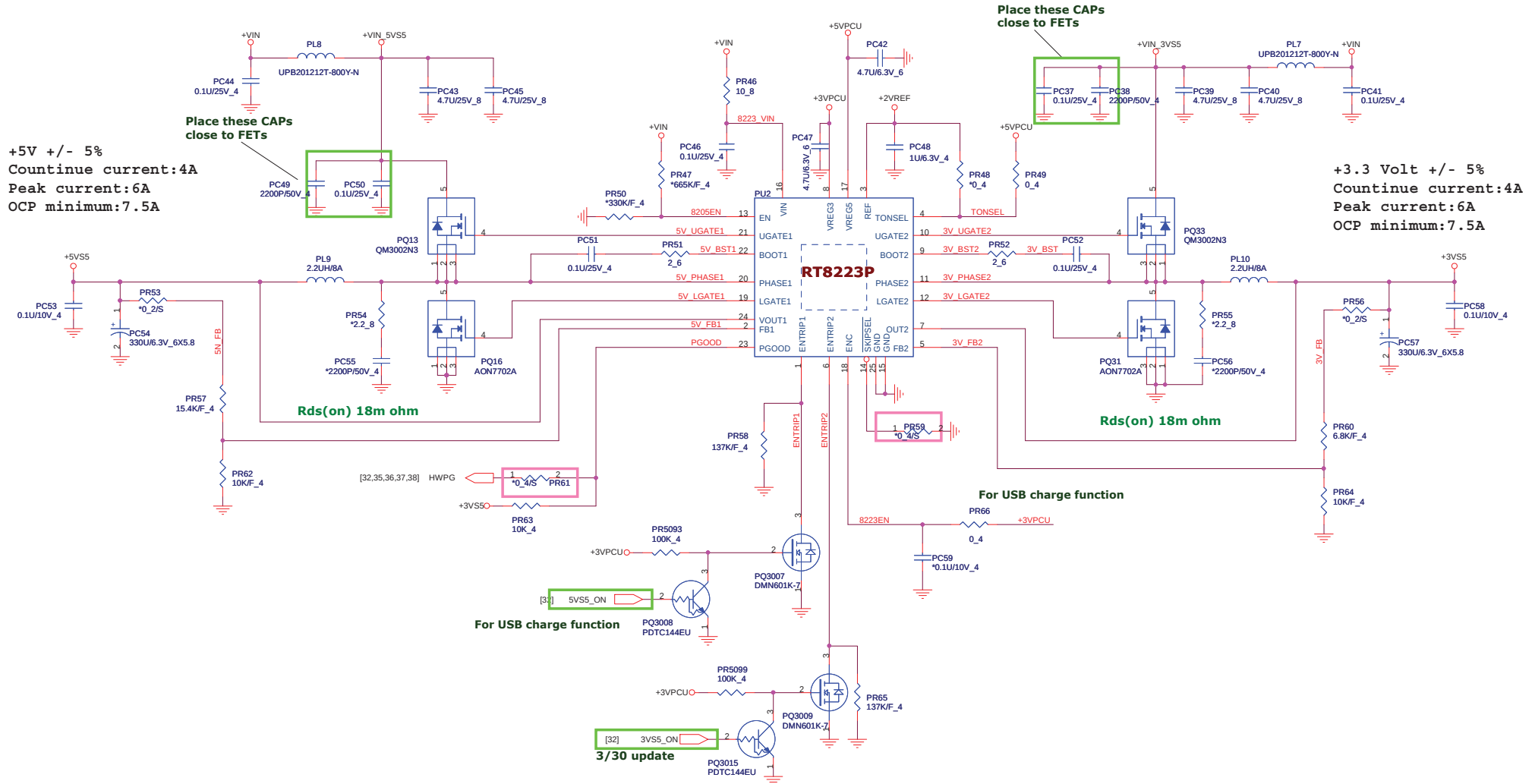
**TOP DC_JACK
90W/120W(QC)**

LG2_DIS only



+5V +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A



LG2_DIS only

(VTT/2A)

+0.75V_DDR_VTT

(3mA)

[4,12,13] DDR_VTTREF

$$RILIM = ILIM \times RDS(ON) / 10\mu A$$

RDSon=4.7m ohm

+1.5VSUS +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A

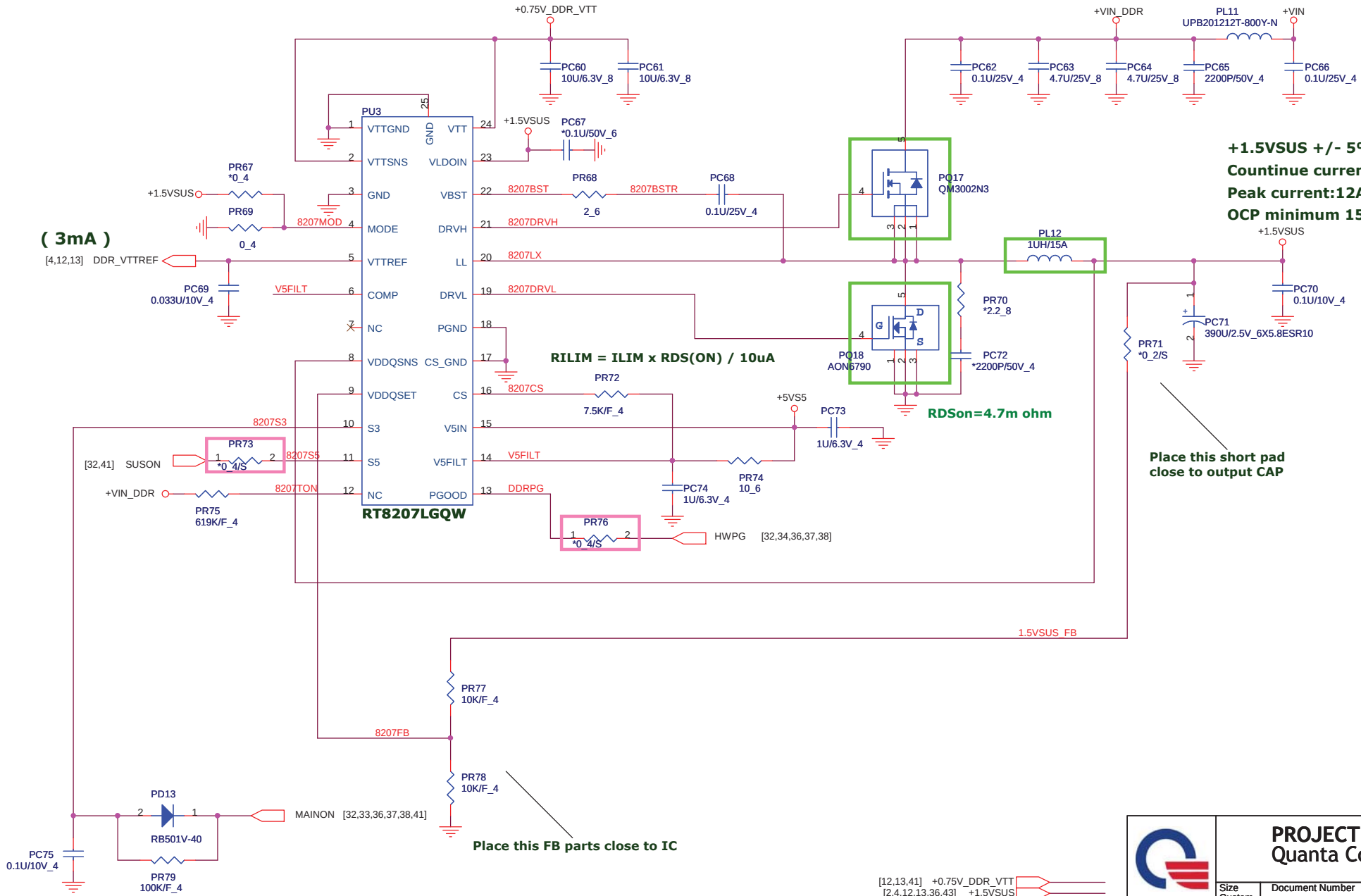
Place this short pad
close to output CAP

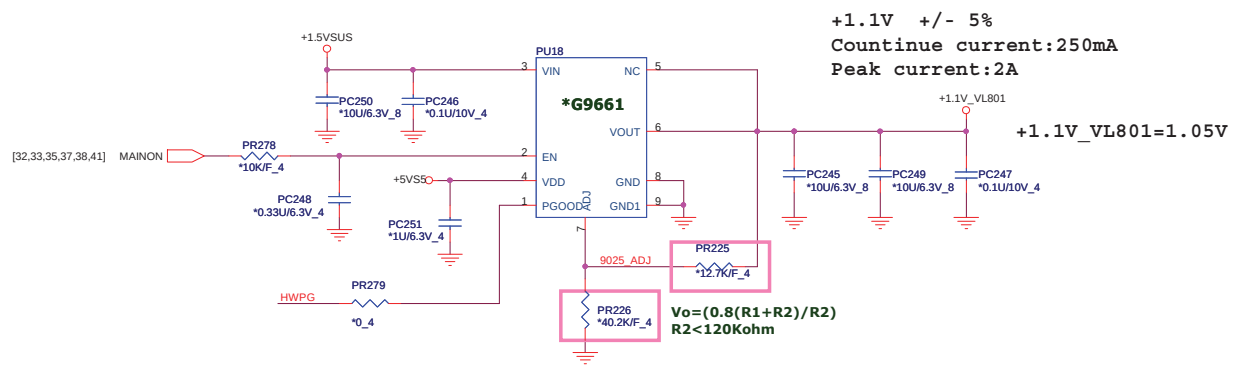
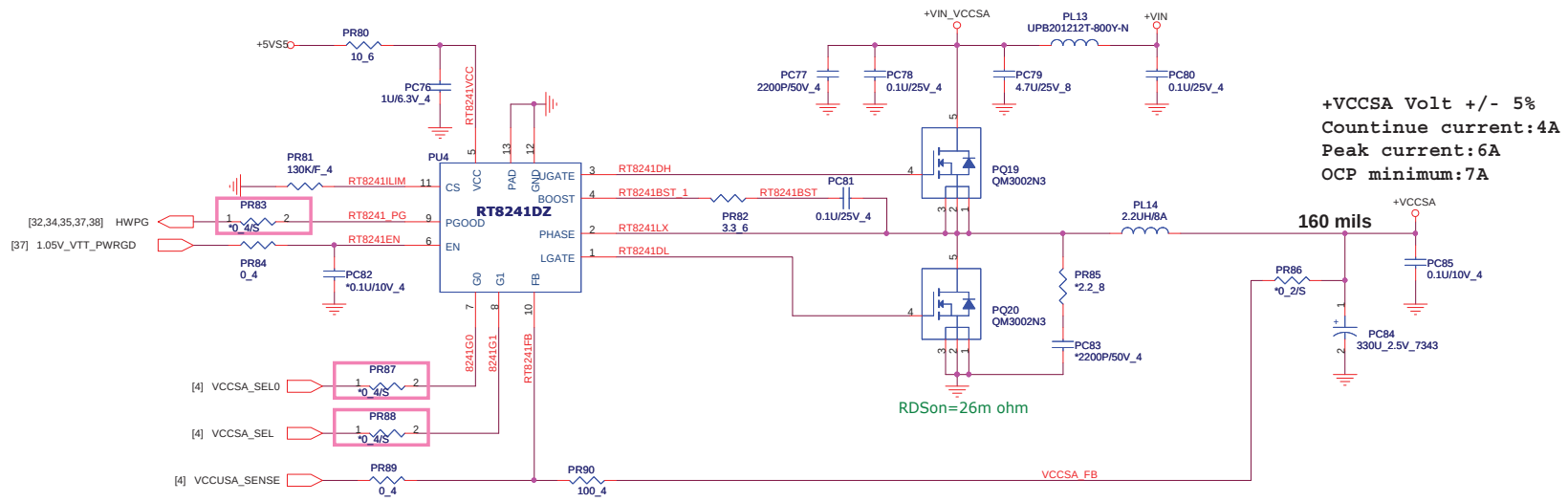
Place this FB parts close to IC

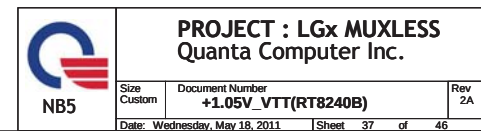


PROJECT : LGx MUXLESS
Quanta Computer Inc.

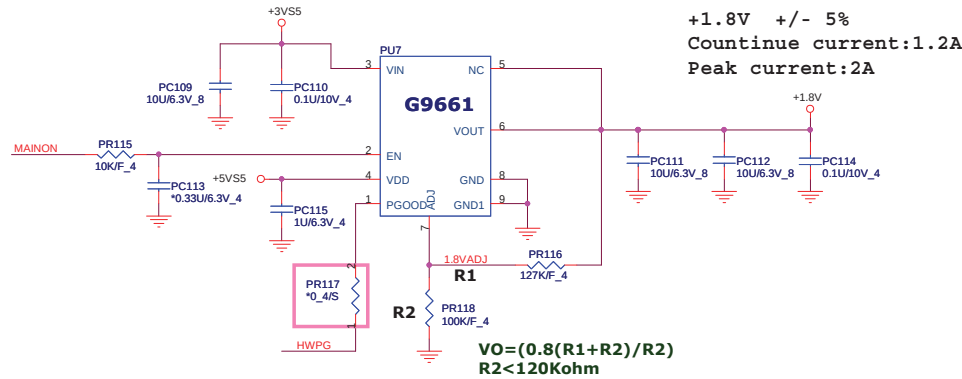
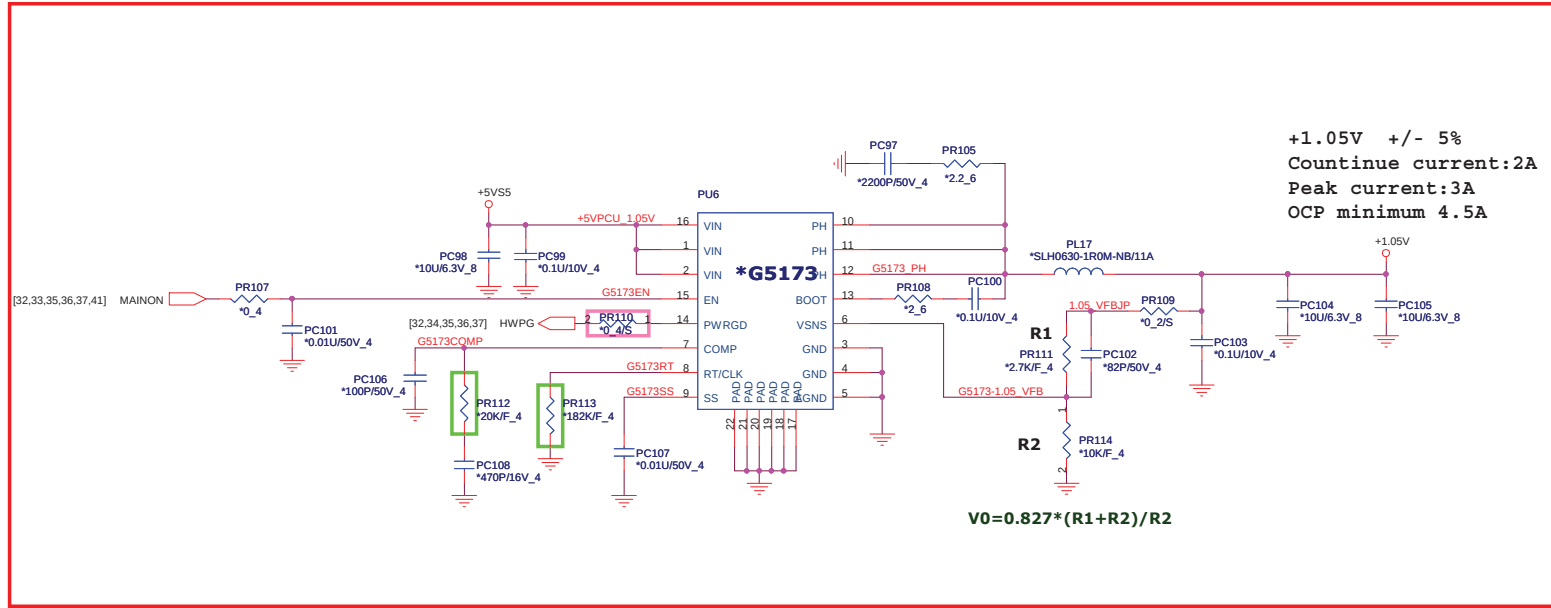
Size	Document Number	Rev
Custom	DDR3 (RT8207)	2A
Date: Wednesday, May 18, 2011	Sheet 35 of 47	



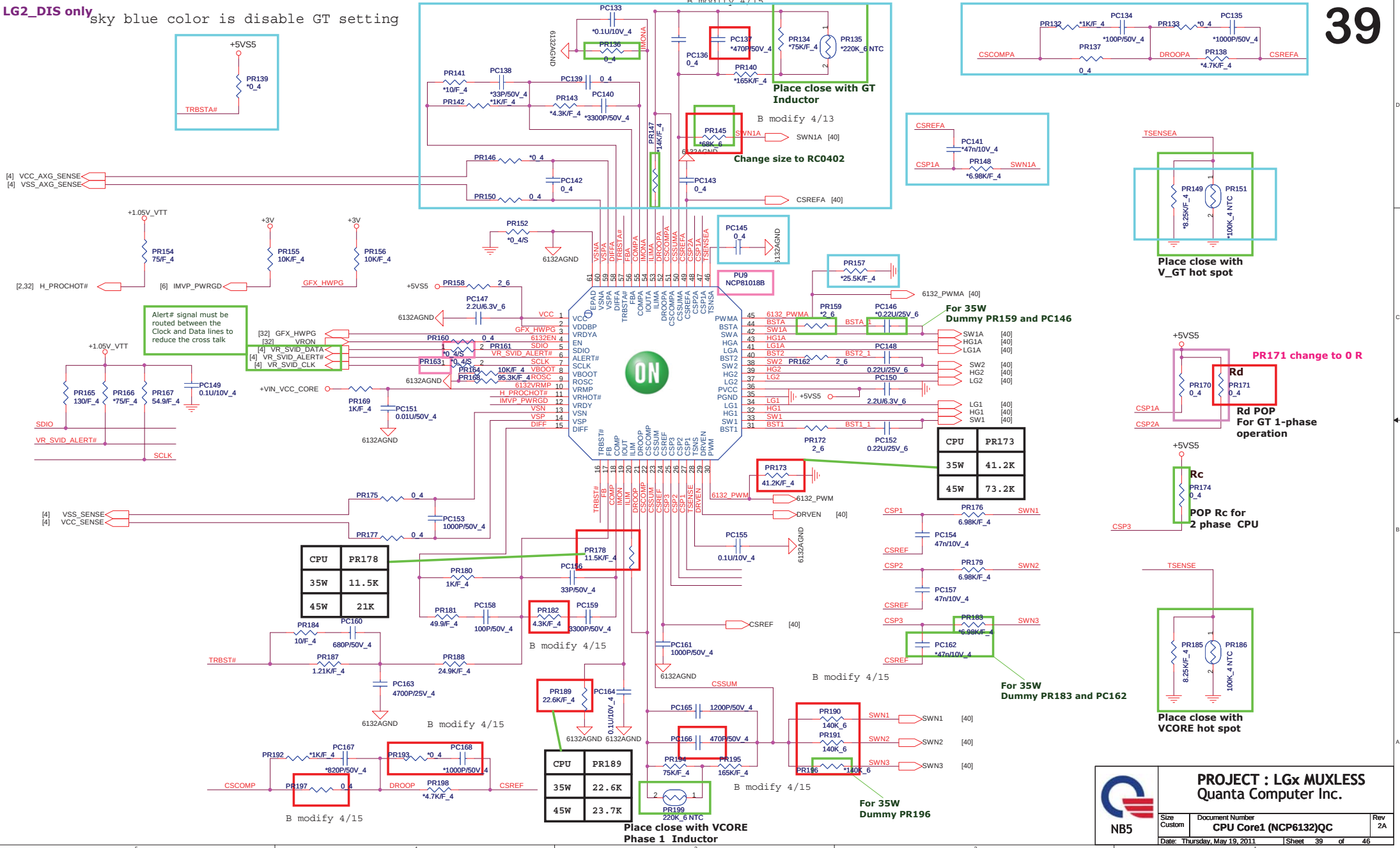


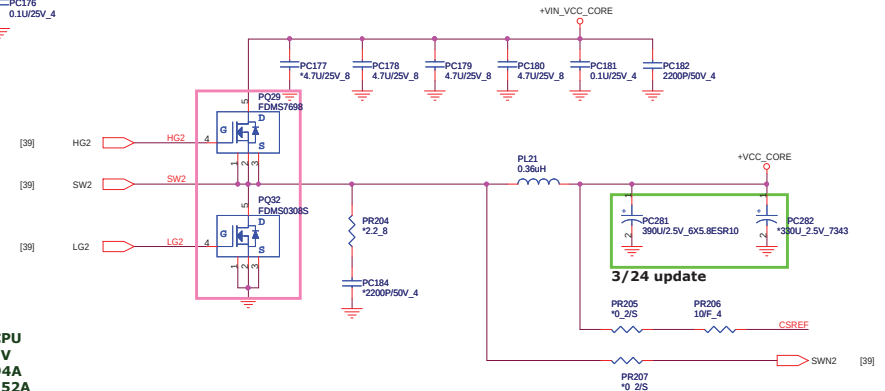
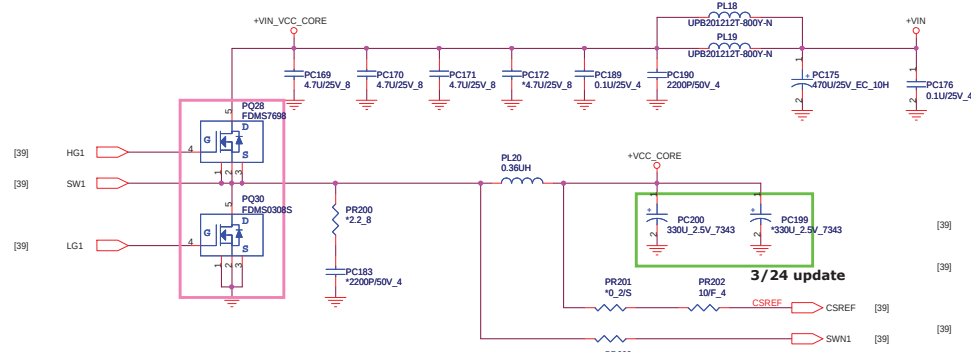


B modify 4/7

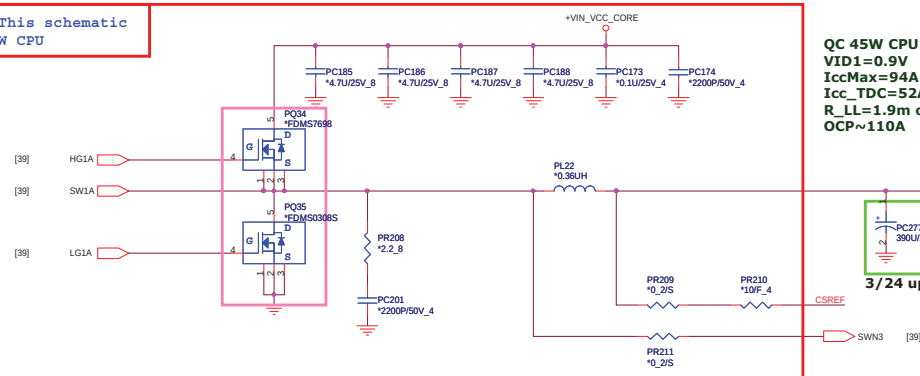


LG2_DIS only sky blue color is disable GT setting

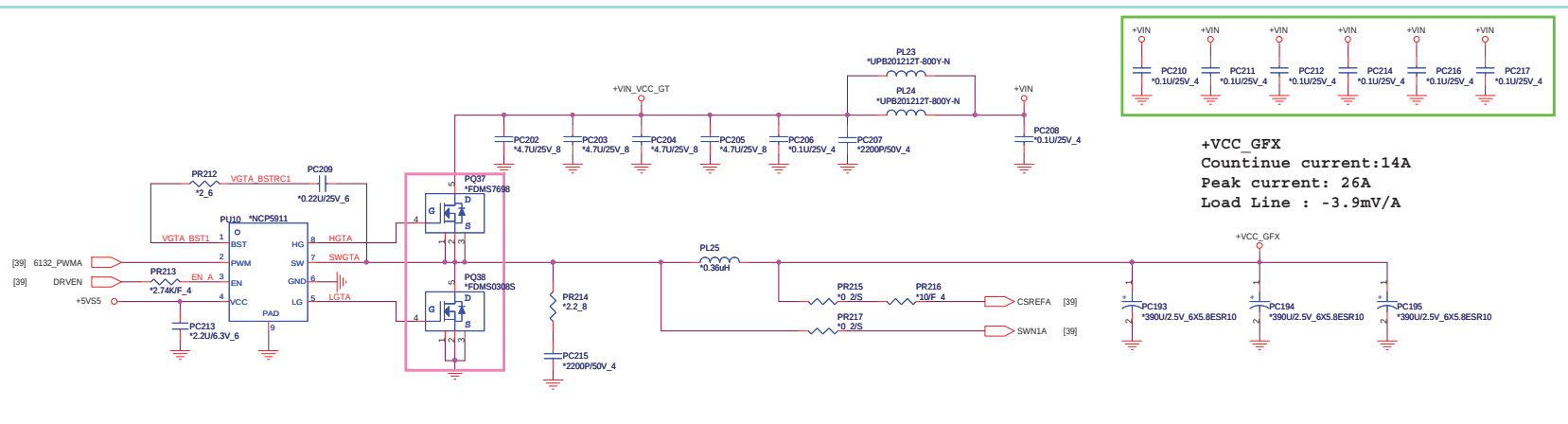
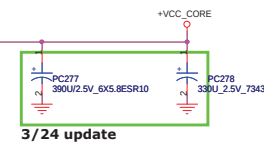




Dummy This schematic
For 35W CPU

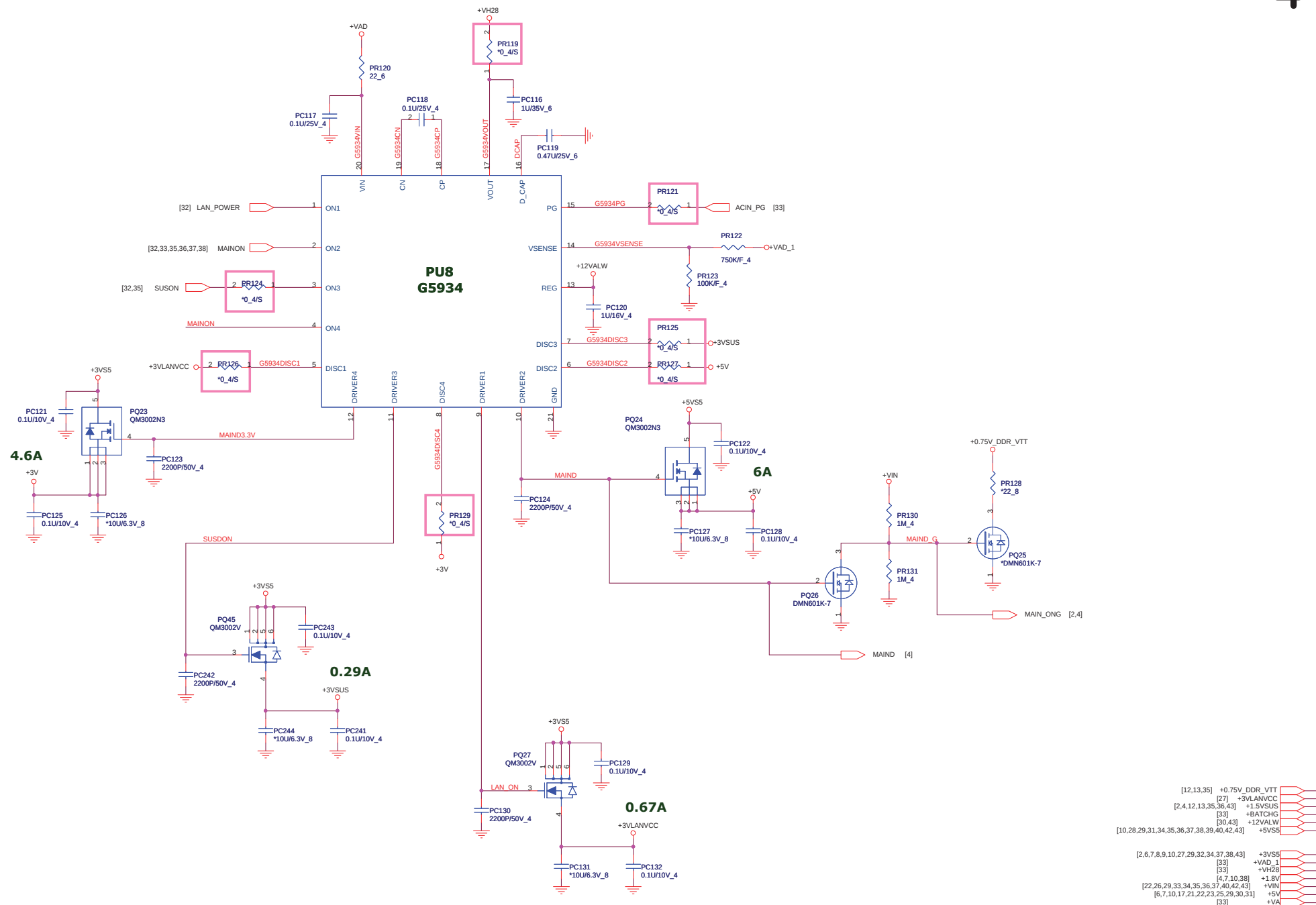


QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_TDC=52A
R_LL=1.9m ohm
OCP~110A



```
+VCC_GFX
Countinue current:14A
Peak current: 26A
Load Line : -3.9mV/A
```

sky blue color is disable GT setting

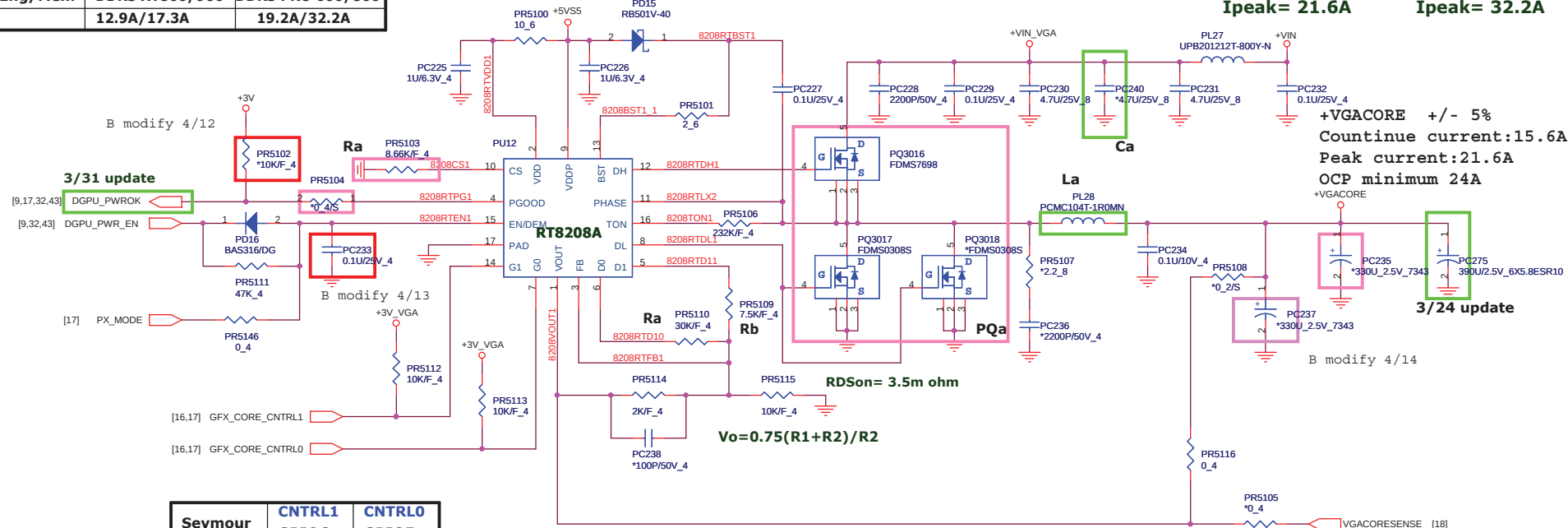


VGA Core

LG2_DIS only
VGA chip only Seymour

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	Seymour (OCP 24A)	Whistler
Ca	PC240 X	V
Cb	PC235 PC237 X	V
PQa	PQ3018 X	V
La	1U/15A	0.45U25A
Ra	8.66K-ohm	8.66K-ohm
Eng/Mem	DDR3 XT800/900	DDR3 PRO 600/800
	12.9A/17.3A	19.2A/32.2A



Seymour-XT 64bit
Irms= 15.6A
Ipeak= 21.6A

Whistler
Irms= 19.2A
Ipeak= 32.2A

+VGACORE +/- 5%
Countinue current:15.6A
Peak current:21.6A
OCP minimum 24A

Seymour	CNTRL1 GPIO6	CNTRL0 GPIO5
0.9V	0	0
0.95V	0	1
1.1V	1	0
1.15V	1	1

default

Whistler	CNTRL1 GPIO6	CNTRL0 GPIO5
0.9V	0	0
1.0V	0	1
1.05V	1	0
1.15V	1	1

Ra --> 15K-ohm
Rb --> 10K-ohm

[2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,26,27,28,29,30,31,32,37,39,41] +3V
[10,28,29,31,34,35,36,37,38,39,40,41,43] +3V_GFX
[17,18] +5VSS
[22,26,29,33,34,35,36,37,40,41,43] +VIN



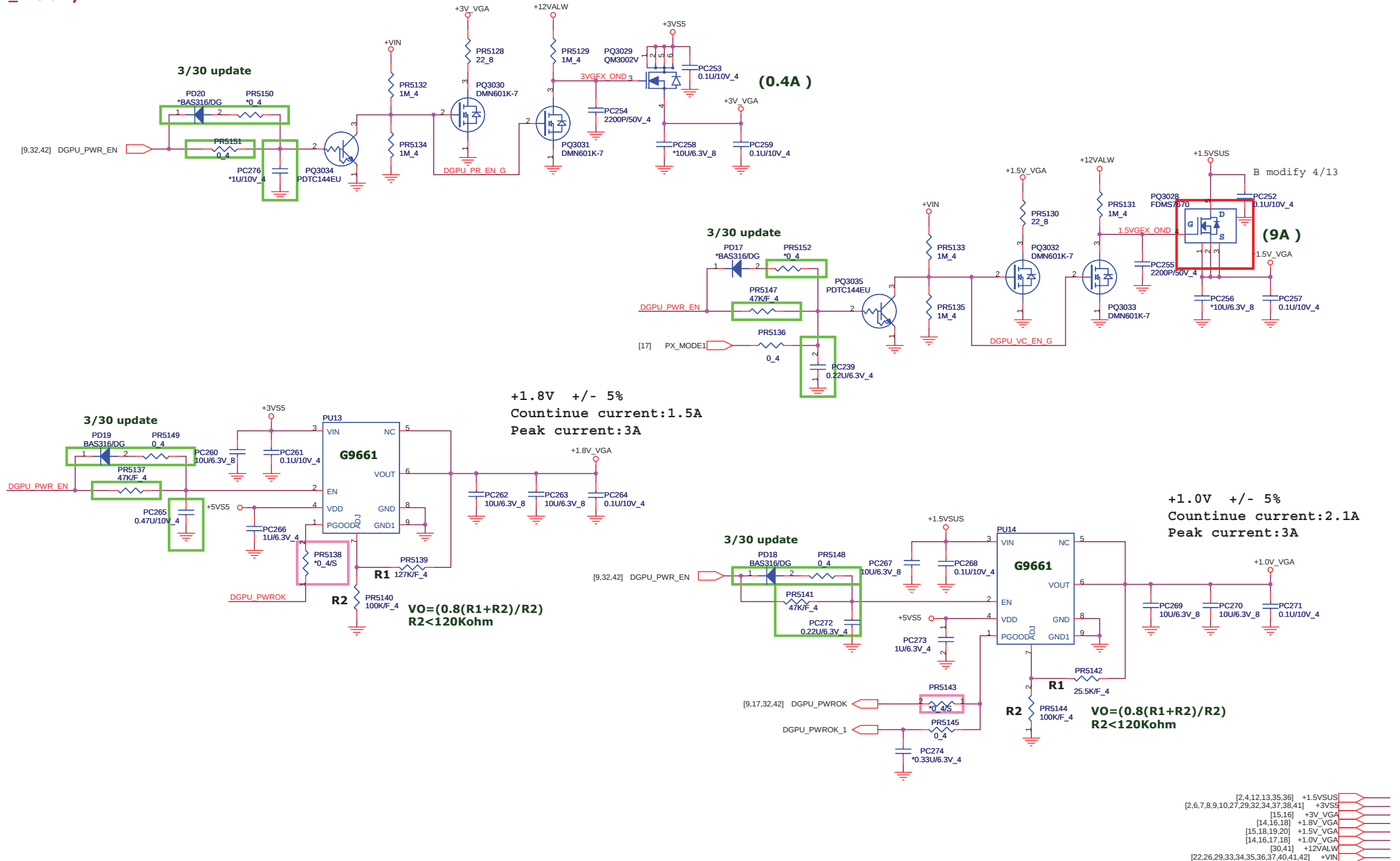
PROJECT : LGx MUXLESS
Quanta Computer Inc.

Size Custom Document Number +VGACORE (RT8208) Rev 2A
Date: Wednesday, May 18, 2011 Sheet 42 of 46

VGA Core

LG2_DIS only

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LG2/4 Power rail map

