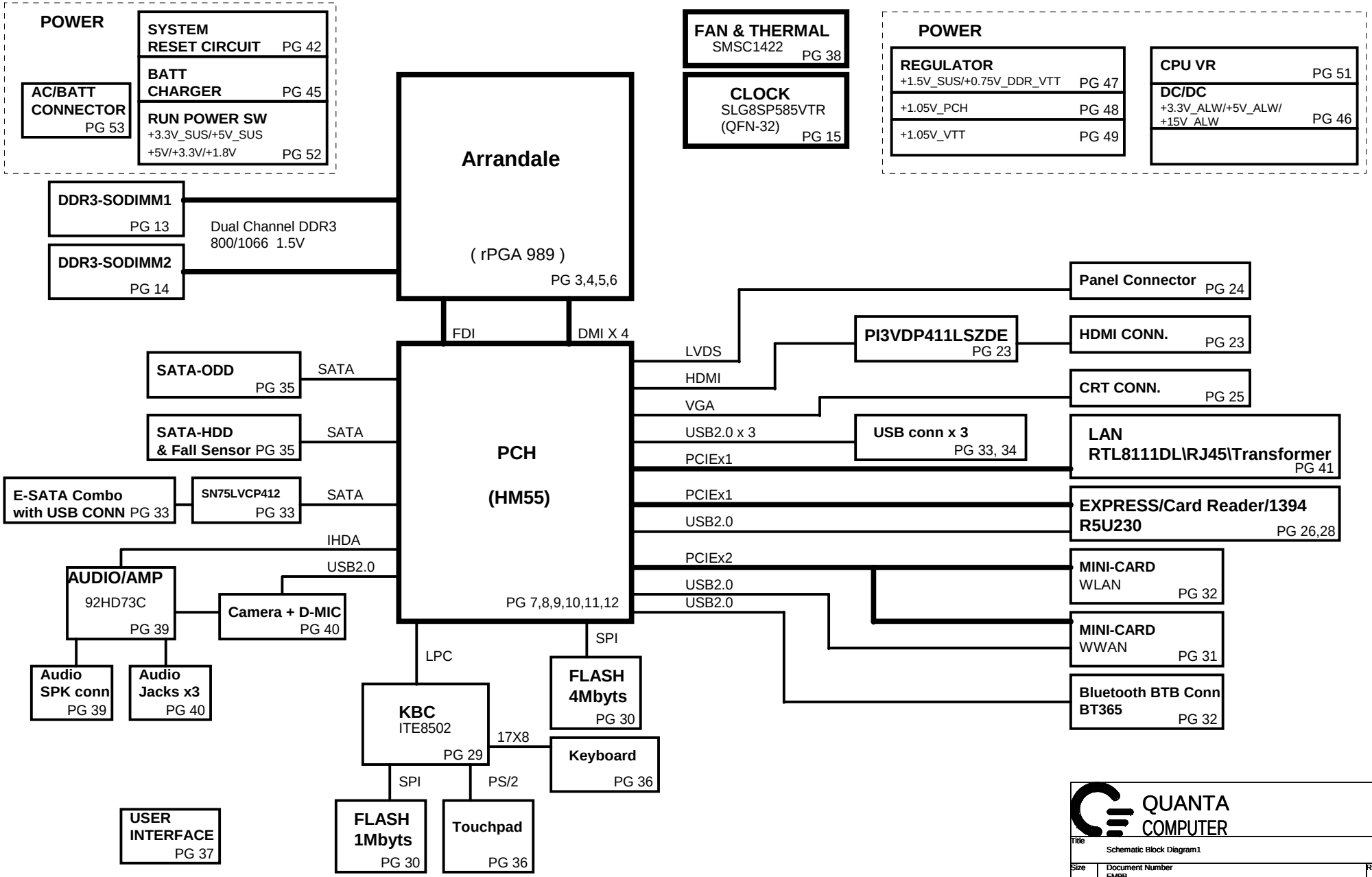
FM9B HANKS Intel UMA

VER : 3A
PWA:
PWB:



QUANTA COMPUTER

Title	Schematic Block Diagram1	
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Table of Contents

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+5V_ALW2	+5V	37,46,52,53	LARGE POWER	MAIN POWER	S0~S5
+5V_ALW	+5V	13,33,44,46,47,48,49,50,51,52	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	29,30,35,36,37,42,44,45,46,47,51,52,53	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	11,33,34,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	07,08,09,10,11,13,14,19,24,28,29,37,41,42,44 ,48,49,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30 ,31,32,33,35,37,38,39,40,41,42,46,51,52,60	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44,52	SDVO POWER	RUN_ON	
+1.05V_VTT	+1.1V	03,05,10,11,49,60	CPU POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,28,31,32,52	Express Card/Min Card	RUN_ON	
+5V_HDD	+5V	35	HDD Power	HDDC_EN	
+1.05V_PCH	+1.05V	08,09,11,15,48	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	35	MOD Power	MODC_EN	

GND PLANE	PAGE	DESCRIPTION
GND	ALL	

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Title	Index & Power Status	
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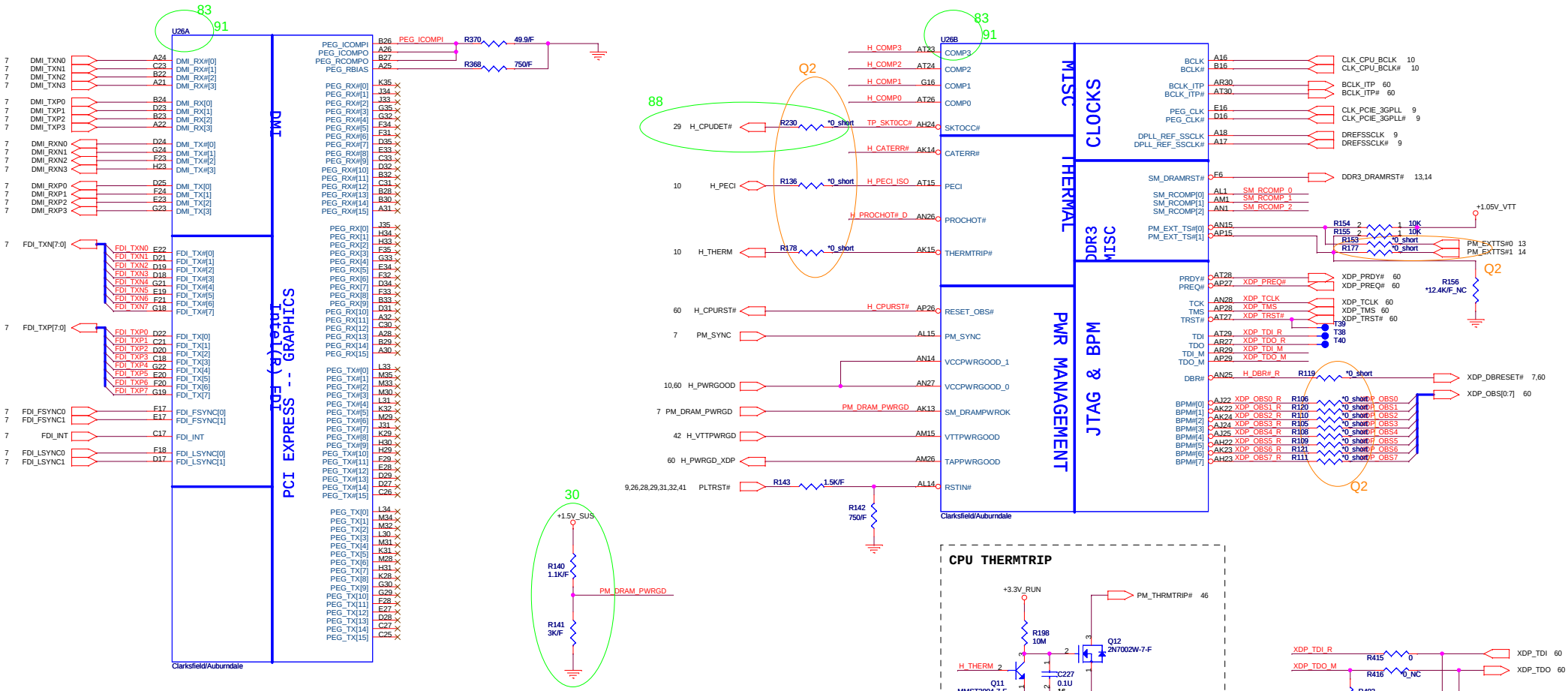
U26A
DMI
PCI EXPRESS -- GRAPHICS
Intel(R) FDI
Clarksfield/Auburndale
U26B
MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
Clarksfield/Auburndale
Q2
CPU THERMTRIP
Processor Pullups
Processor Compensation Signals
DDR3 Compensation Signals
QUANTA COMPUTER
AUBURNDA 1/4
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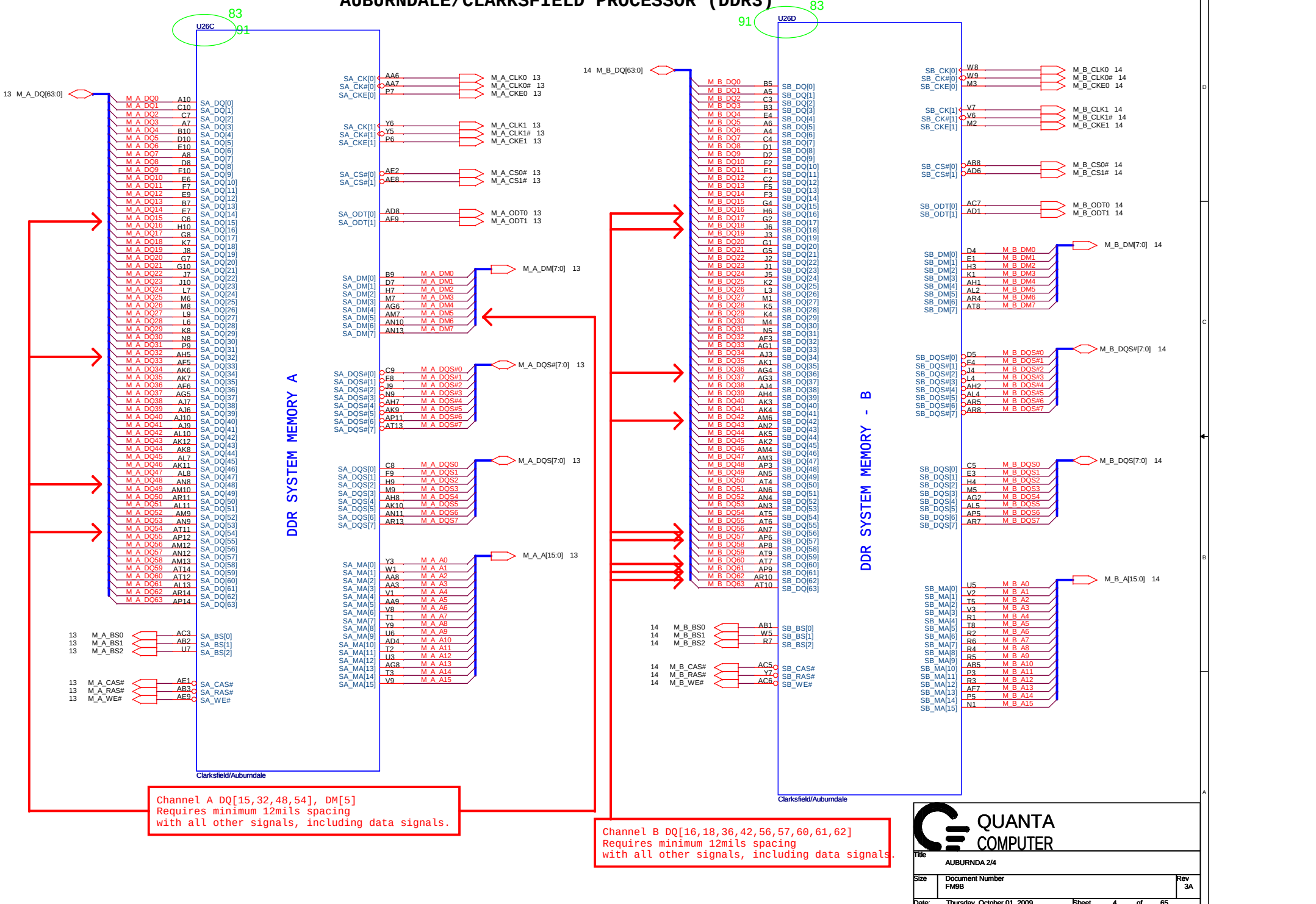
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



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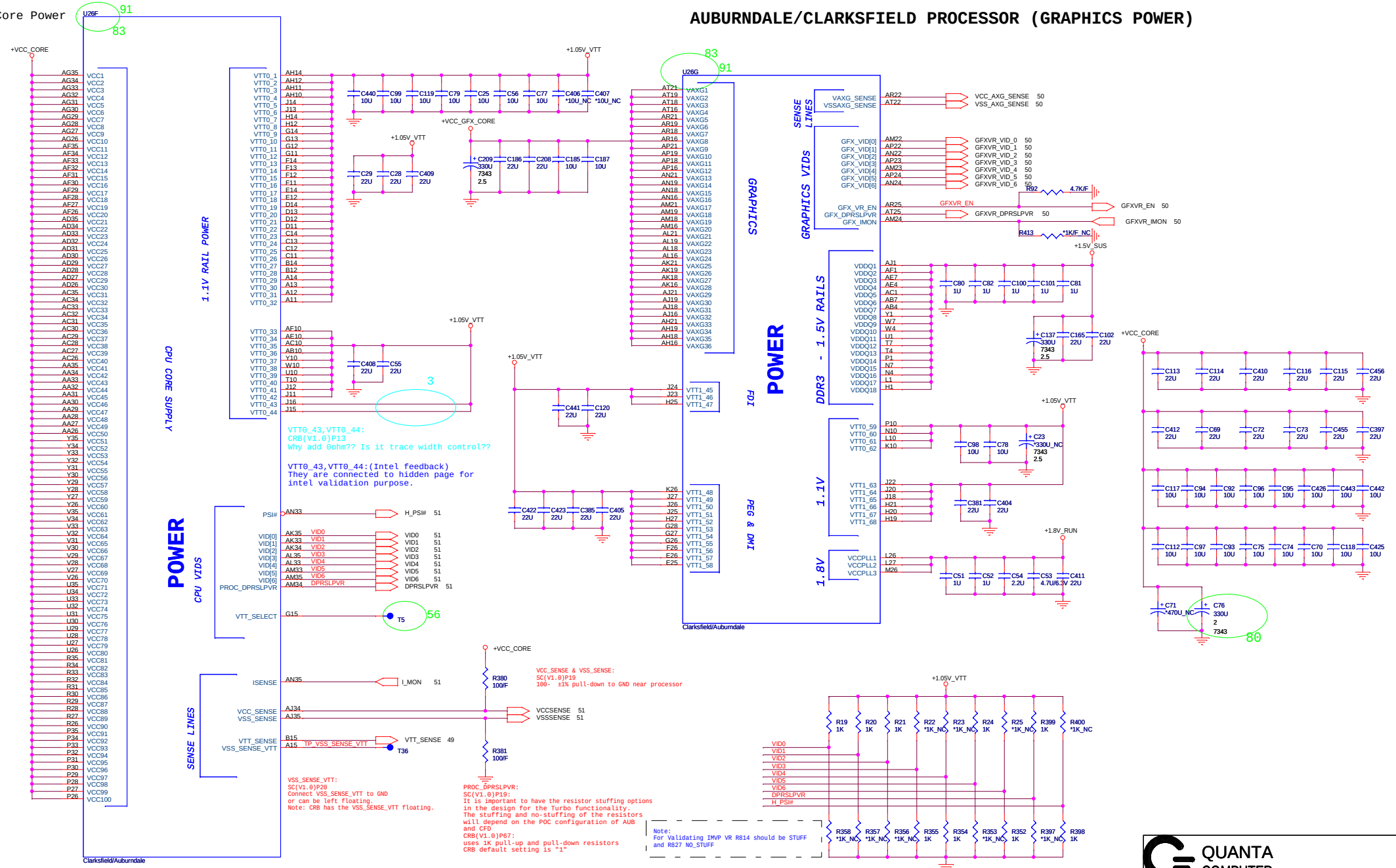
AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

CPU Core Power



AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

QUANTA COMPUTER			
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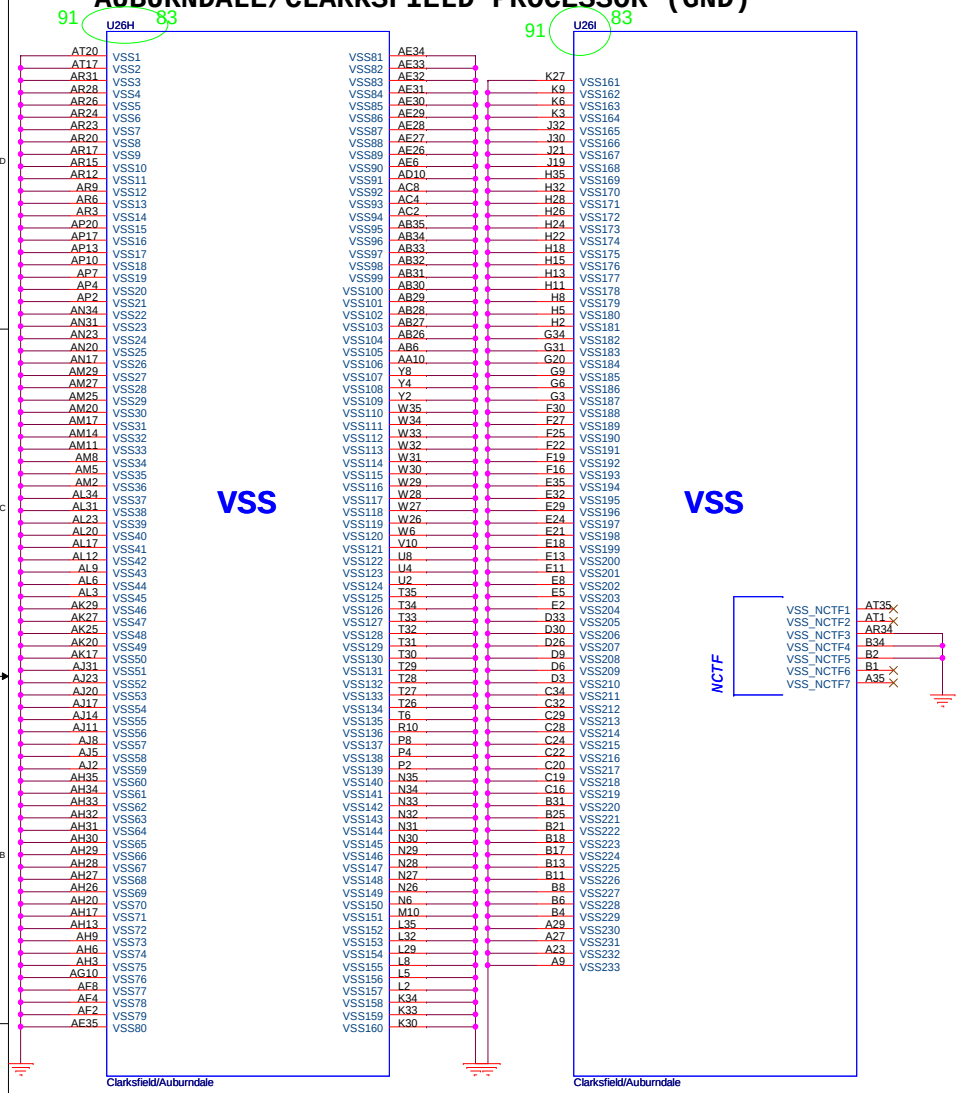
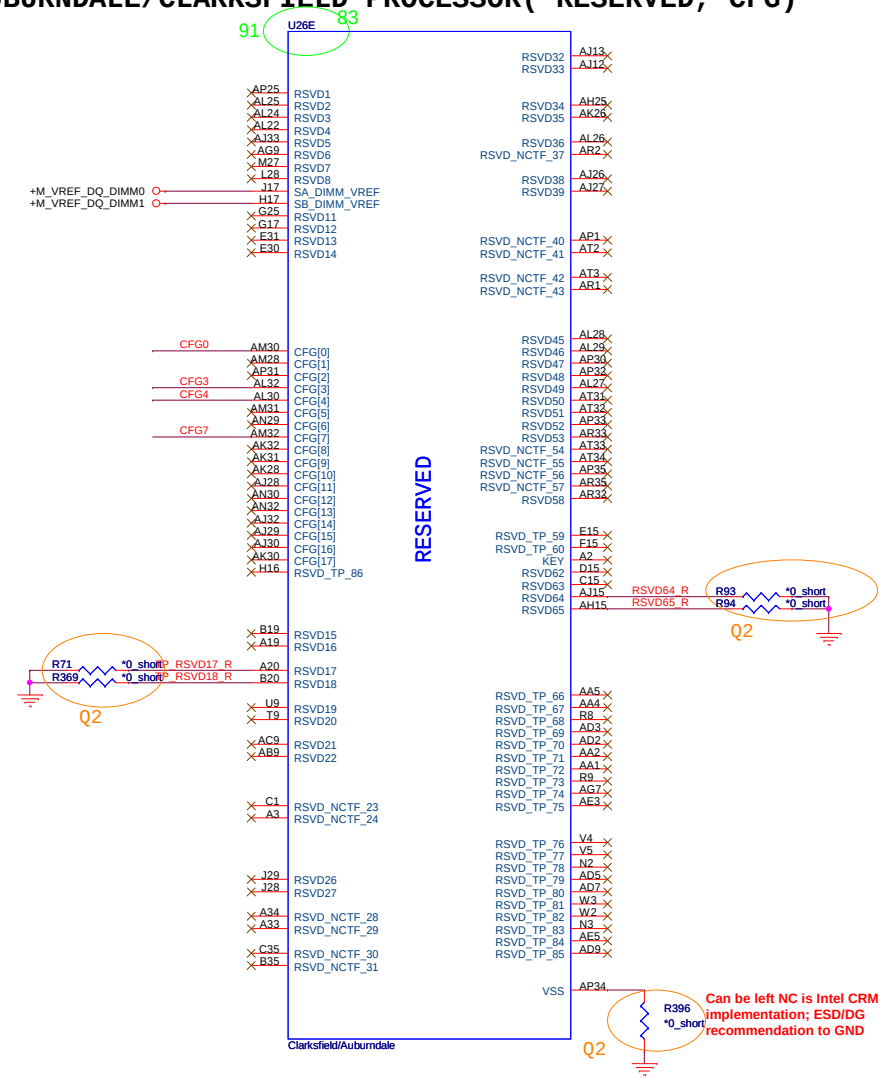
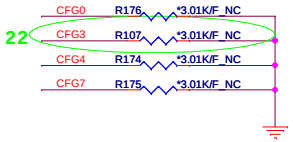
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

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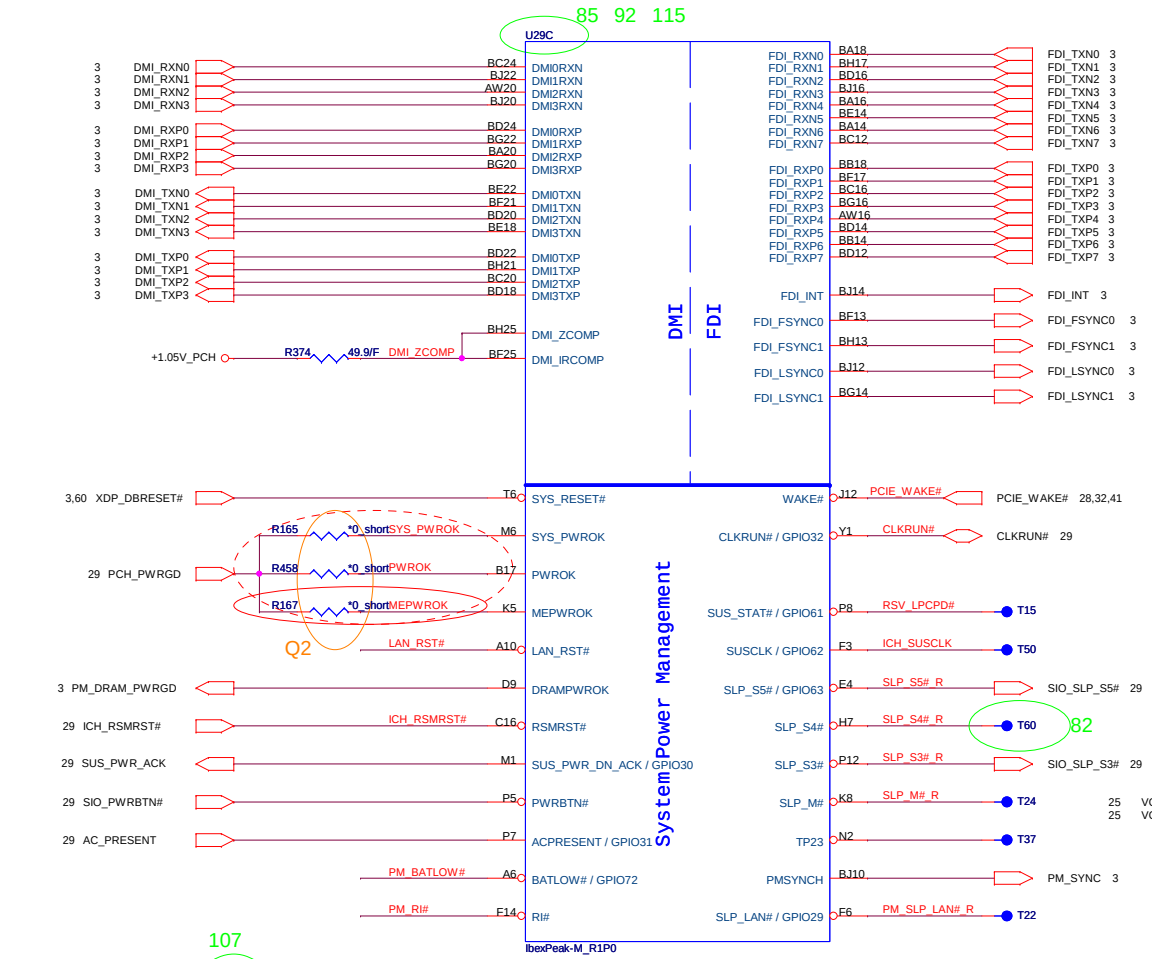
IBEX PEAK-M (DMI,FDI,GPIO)



85 92 115

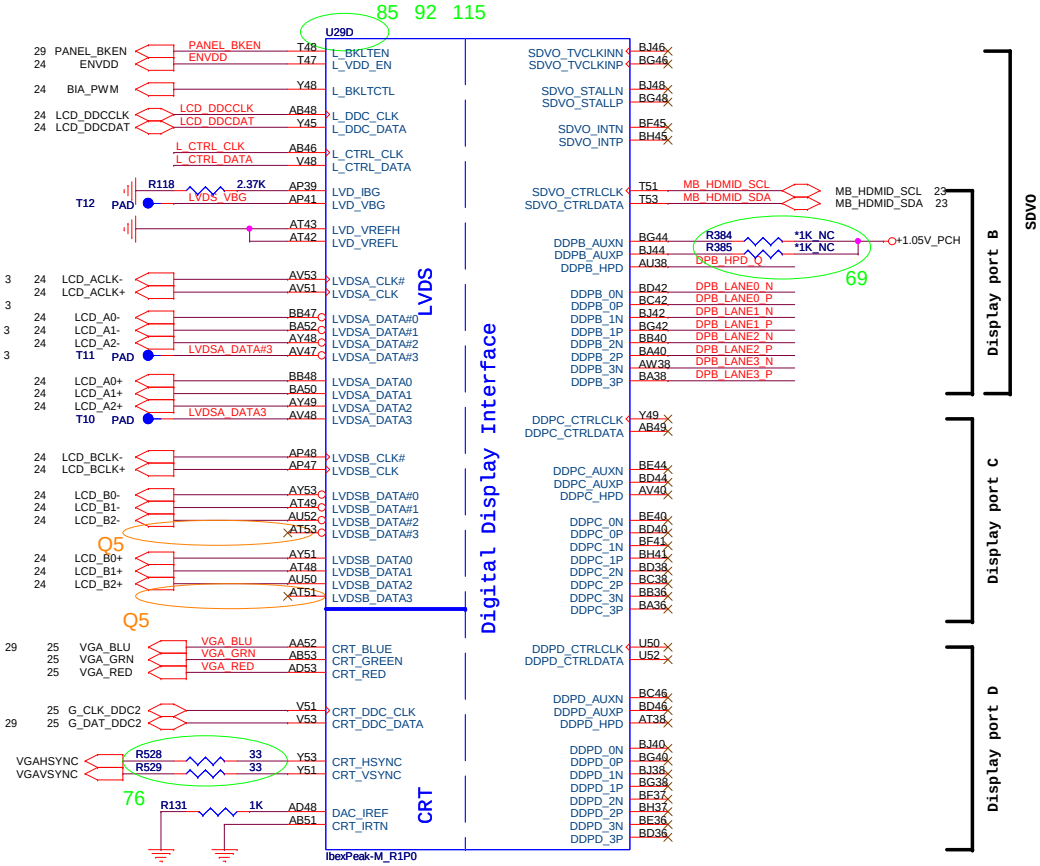
3,60 XDP_DBRESET#
R165 *0_short SYS_PWROK
29 PCH_PWRGD
R458 *0_short PWROK
R167 *0_short MEPWROK
Q2
LAN_RST#
3 PM_DRAM_PWRGD
29 ICH_RSMRST#
29 SUS_PWR_ACK
29 SIO_PWRBTN#
29 AC_PRESENT
PM_BATLOW#
PM_RI#
PCIE_WAKE# J12
CLKRUN# Y1
RSV_LPCPD# P8
ICH_SUSCLK F3
SLP_S5# _R E4
SLP_S4# _R H7
SLP_S3# _R P12
SLP_M# _R K8
T15
T50
SIO_SLP_S5# 29
T60
82
SIO_SLP_S3# 29
T24
T37
PM_SYNC 3
PM_SLP_LAN# _R F6
T22
PCIE_WAKE# 28,32,41
CLKRUN# 29

107
+3.3V_RUN
CLKRUN# R410 10K
LCD_DDCDAT R132 2.2K
LCD_DDCCLK R133 2.2K
L_CTRL_CLK R134 10K
L_CTRL_DATA R135 10K
37 XDP_DBRESET# R350 1K
+3.3V_SUS
PM_RI# R480 10K
PCIE_WAKE# R188 1K
PM_BATLOW# R465 8.2K

107
PCH_PWRGD R168 10K
ICH_RSMRST# R477 10K
LAN_RST# R461 10K

Close to VGA side
VGA_BLU R405 150/F
VGA_GRN R404 150/F
VGA_RED R403 150/F
PANEL_BKEN R173 100K
ENVDD R170 100K

IBEX PEAK-M (LVDS,DDI)



85 92 115

29 PANEL_BKEN
24 ENVDD
24 BIA_PWM
24 LCD_DDCCLK
24 LCD_DDCDAT
L_CTRL_CLK
L_CTRL_DATA
R118 2.37K
T12 PAD
LVDS_VBG
24 LCD_ACLK-
24 LCD_ACLK+
24 LCD_A0-
24 LCD_A1-
24 LCD_A2-
T11 PAD
LVDSA_DATA#3
24 LCD_A0+
24 LCD_A1+
24 LCD_A2+
T10 PAD
LVDSA_DATA3
24 LCD_BCLK-
24 LCD_BCLK+
24 LCD_B0-
24 LCD_B1-
24 LCD_B2-
Q5
24 LCD_B0+
24 LCD_B1+
24 LCD_B2+
Q5
25 VGA_BLU
25 VGA_GRN
25 VGA_RED
25 G_CLK_DDC2
25 G_DAT_DDC2
25 VGAHSYNC
25 VGAVSYNC
R528 33
R529 33
76
R131 1K
MB_HDMID_SCL 23
MB_HDMID_SDA 23
R384 *1K_NC
R385 *1K_NC
+1.05V_PCH
DPB_HPD
69

For UMA HDMI Function

+3.3V_RUN
R436 2.2K
R438 2.2K
MB_HDMID_SCL
MB_HDMID_SDA
+5V_RUN
Q45 2N7002K-T1-E3
DPB_HPD_Q
R383 100K
R382 *0_NC
MB_HDMID_HPD 23

DPB_LANE0_N C47 0.1U
DPB_LANE0_P C48 0.1U
DPB_LANE1_N C50 0.1U
DPB_LANE1_P C49 0.1U
DPB_LANE2_N C65 0.1U
DPB_LANE2_P C66 0.1U
DPB_LANE3_N C68 0.1U
DPB_LANE3_P C67 0.1U
HDMID_DATA2_N 23
HDMID_DATA2_P 23
HDMID_DATA1_N 23
HDMID_DATA1_P 23
HDMID_DATA0_N 23
HDMID_DATA0_P 23
HDMID_CLK_N 23
HDMID_CLK_P 23

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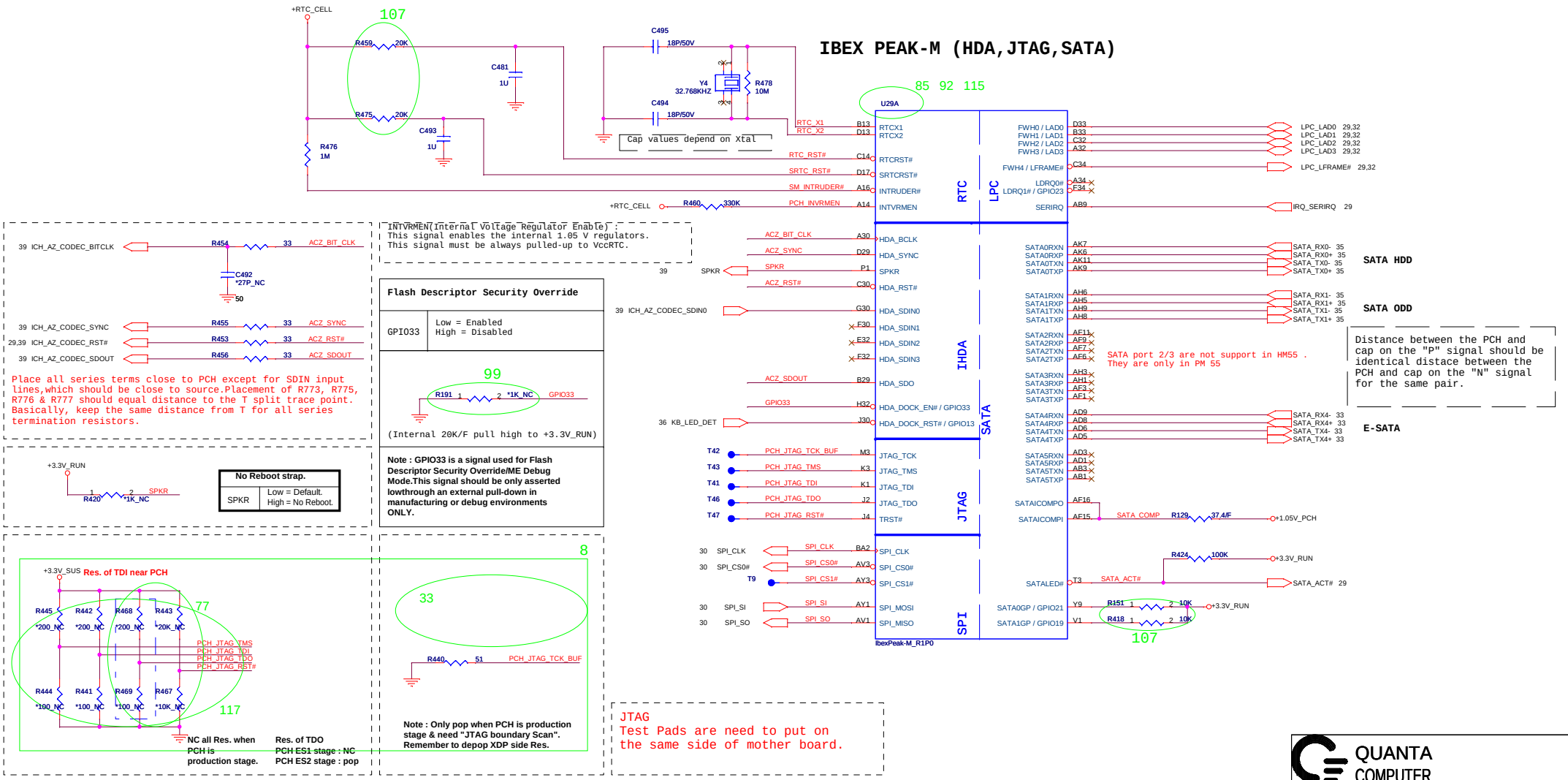
IBEX PEAK-M (HDA,JTAG,SATA)



Title	IBEX PEAK-M 1/6		
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IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

Place TX DC blocking caps close PCH.

PCI-E port 7/8 are not support in HM55 . They are only in PM 55

USB port 6/7 are not support in HM55 . They are only in PM 55

PCIRST#:
DG(V1.0) P277
Can be left unconnected.

PAR:
SC(V1.0) P36
Can be left unconnected if not using PCI.

PME:
DG(V1.0) P277
Can be left unconnected.

CLKOUT_PCI[0..4]:
22 ohm series resistor is recommend (single & double load) on PDG v1.1

OC0#~OC7#:
DG(V1.0)P214

Pin	Default Port Mapping
OC0#	Port0,Port1
OC1#	Port2,Port3

CLKOUT_PEG_A_P/N,CLKOUT_PEG_B_P/N, CLKOUT_DMI_P/N,support GEN-1 and GEN-2

CLKOUTFLEX[0..3]:
PDG v1.1: 22 ohm series resistor is recommend (PCI & non PCI routing, single & double load)

DG(V1.1) P256: XTAL_OUT and XTAL_IN are the signal names for the PHY. Intel feedback:
Fully-Integrated Clocking is a stretch goal for Calpella platforma nd maybe enabled in ES2 Si. Recommend customers to have 25-MHz crystal as a BOM stuff option.

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +V3.3A.PCIECLKRQ{1,2} should have a 10K pull-up to +3.3S

SML0CLK/SML0DATA:
DG(V1.1) P255: The 82577 SMBus signals (SMB_DATA and SMB_CLK) cannot be connected to any other devices other than the PCH. Connect the SMB_DATA and SMB_CLK pins to the PCH SML0DATA and SML0CLK pins, respectively.

CLKIN_PCILOOPBACK:
PDG (V1.1): 22 ohm series resistor is recommend

Note : place these resistors near to PCIe Slots

Reserve capacitor pads for improving WWAN.

Add Buffers as needed for Loading and fanout concerns.

Non-iAMT

PCIE Clock Request

25MHz Clock for DCI Function

Boot BIOS Strap

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved (NAND)
1	1	SPI

Title	IBEX PEAK-M 3/6
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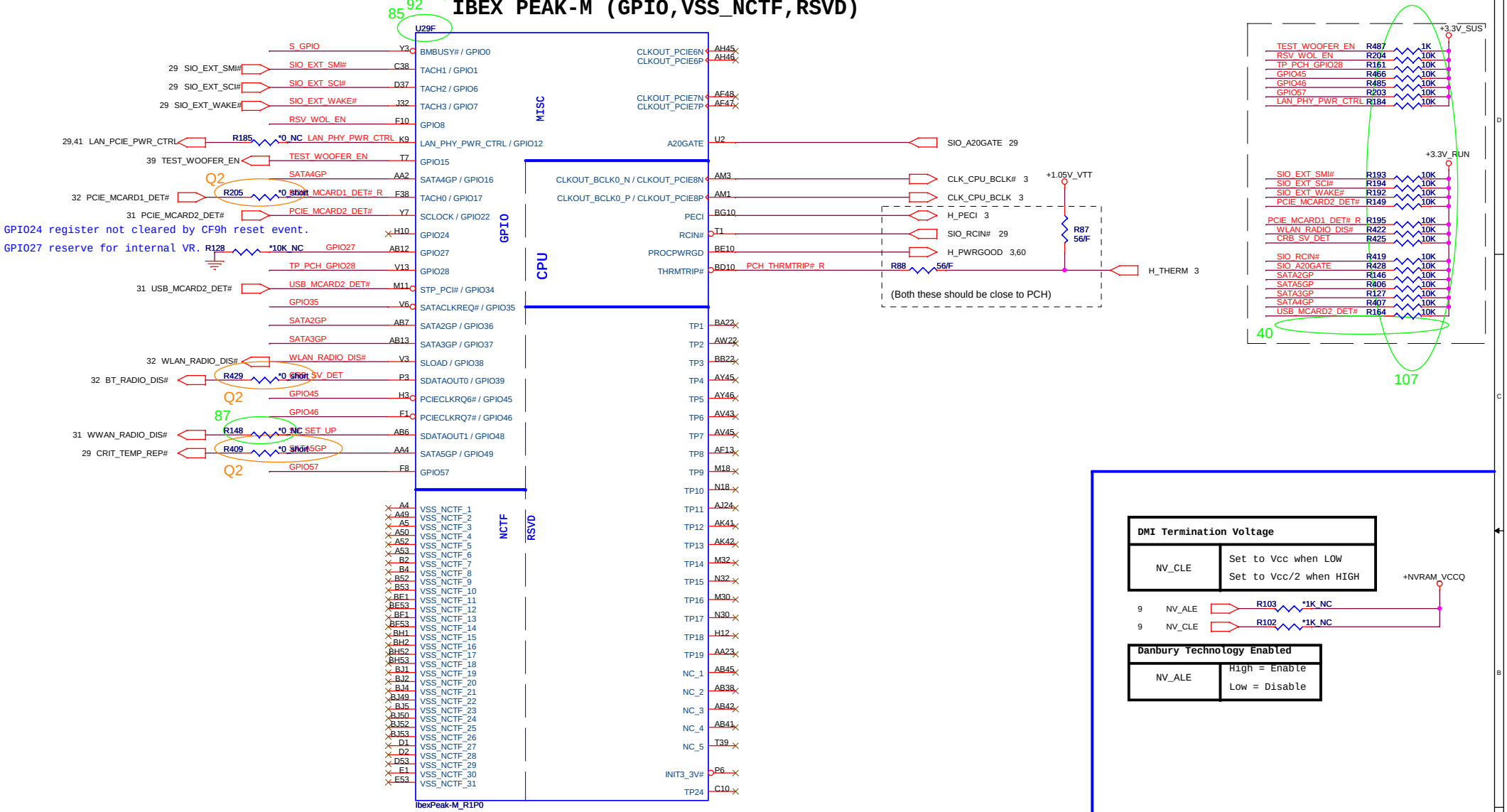
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



GPIO24 register not cleared by CF9h reset event.

GPIO27 reserve for internal VR.

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

+NVRAM_VCCQ

9 NV_ALE R103 *1K_NC

9 NV_CLE R102 *1K_NC

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

107 R150 10K GPIO35

R437 *1K_NC GNT3# 9

A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

34 R186 *1K_NC RSV_WOL_EN

Integrated Clock Chip Enable (Reserve to validate for future platforms)	
RSV_WOL_EN	Enable when sampled low Disable when sampled high

107 +3.3V_RUN

S_GPIO R408 10K

SV_SET_UP R147 10K

6

BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is
for intel BIOS validation purpose.

SV_SET_UP	1-X High = Strong (Default)

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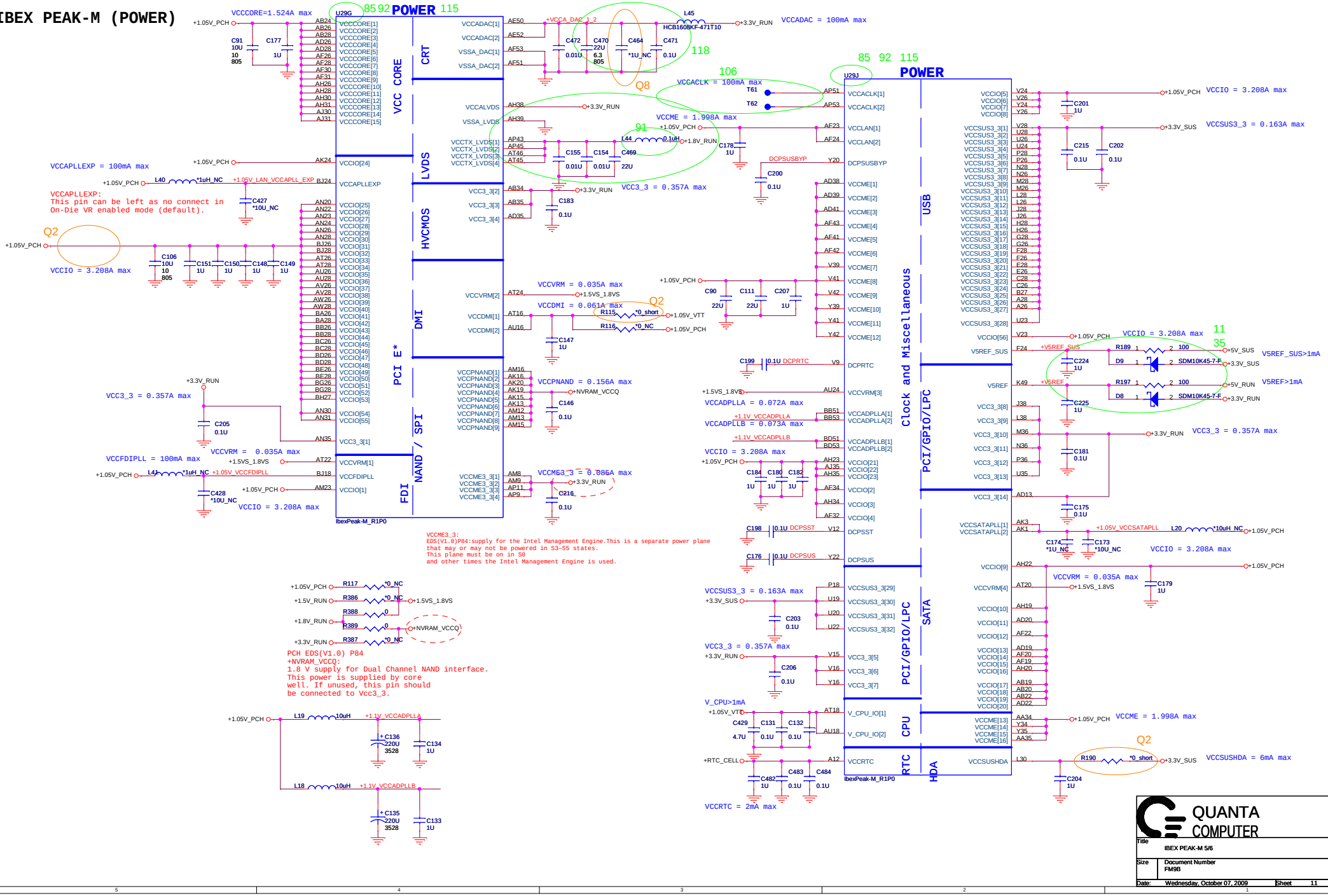
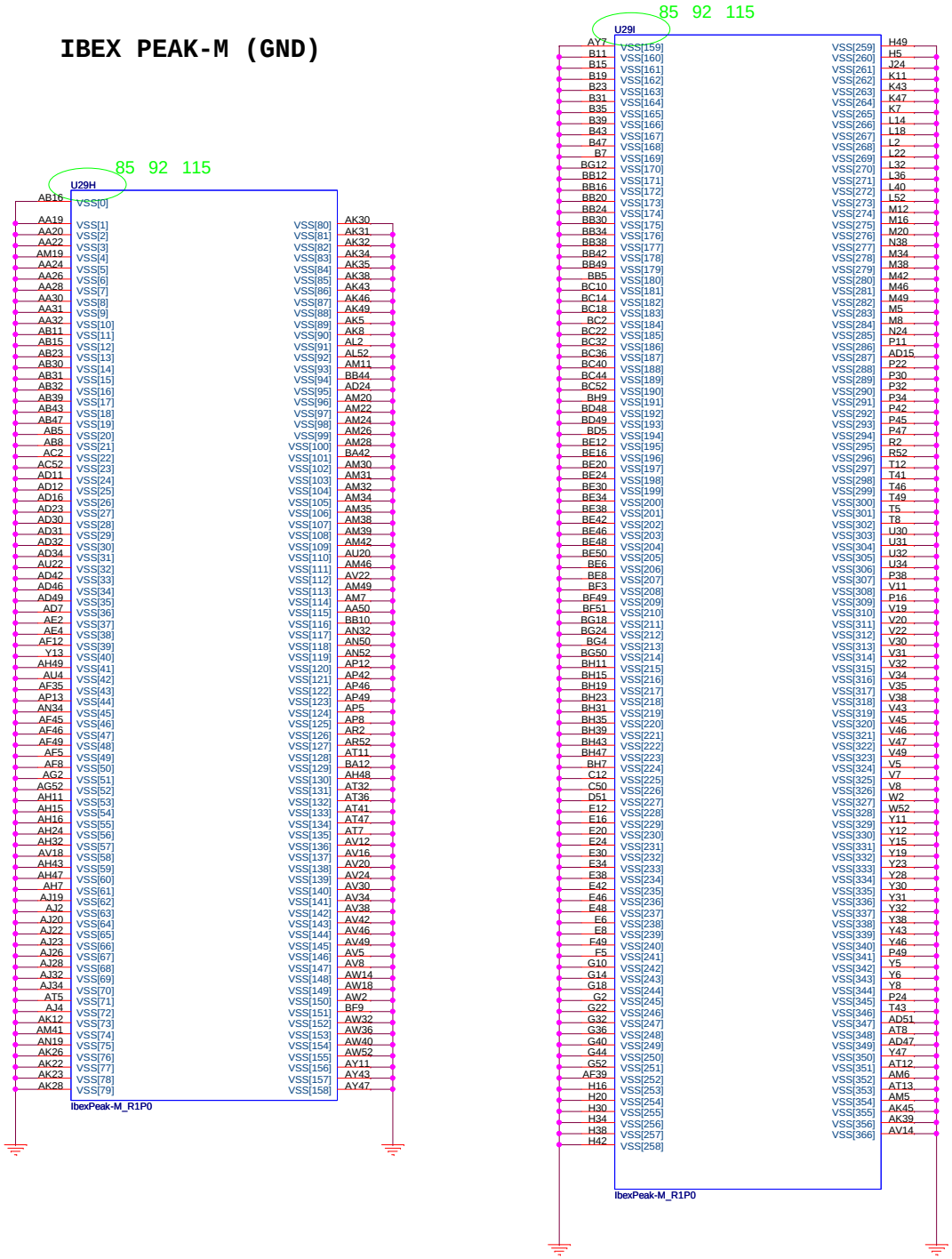
IBEX PEAK-M (POWER)



IBEX PEAK-M (GND)



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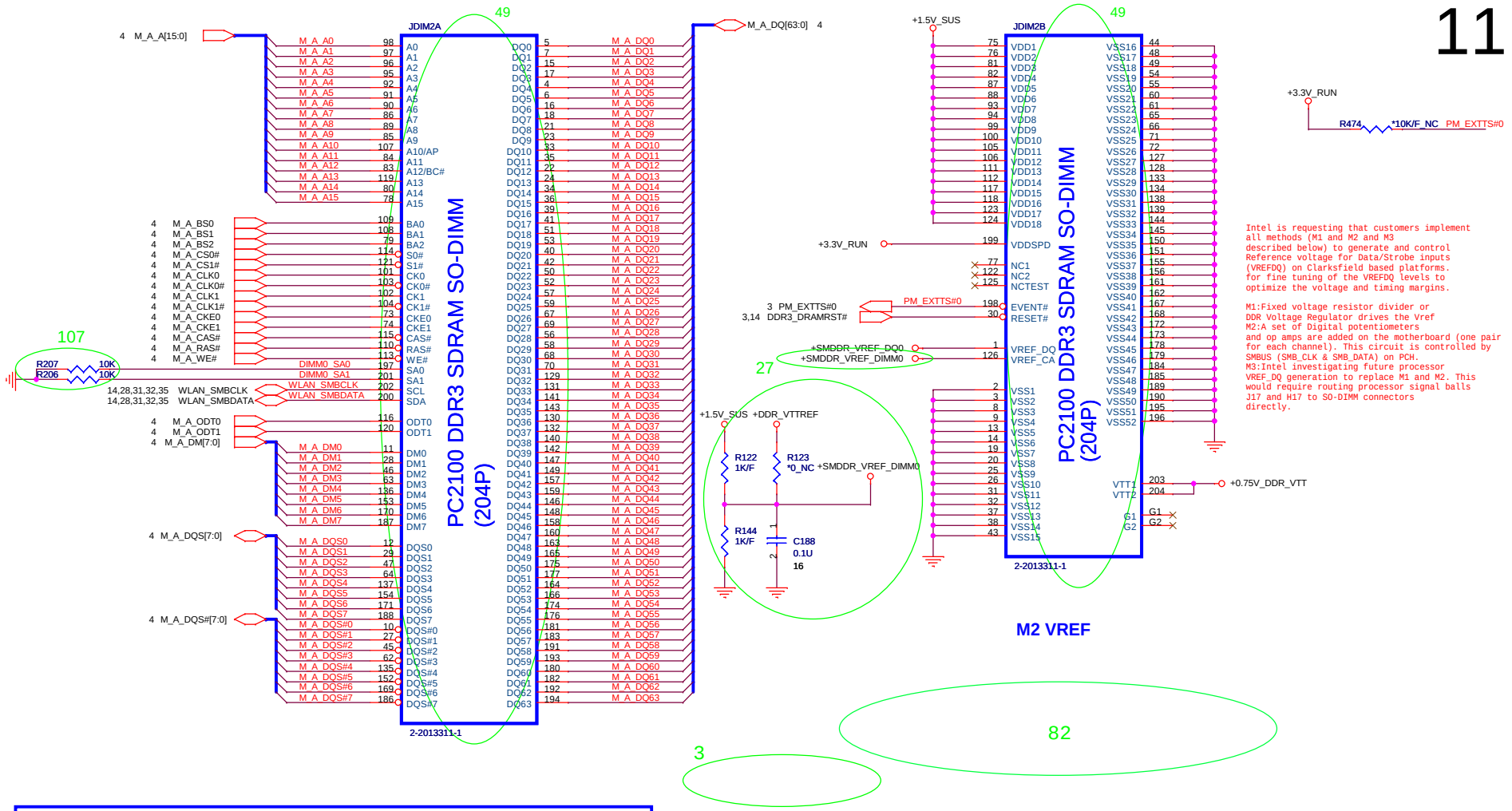

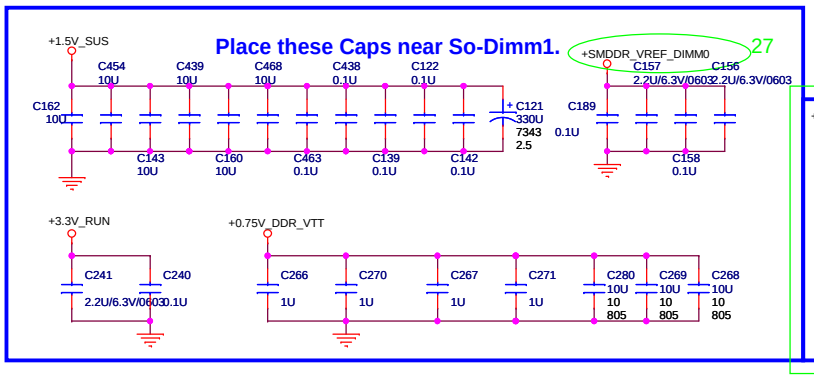

VREF_DQ	R57	R56	R40 (+DDR_VTTREF)
M1	Stuff	X	X
M3	X	Stuff	X

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Title	DDR3 DIMM-0	
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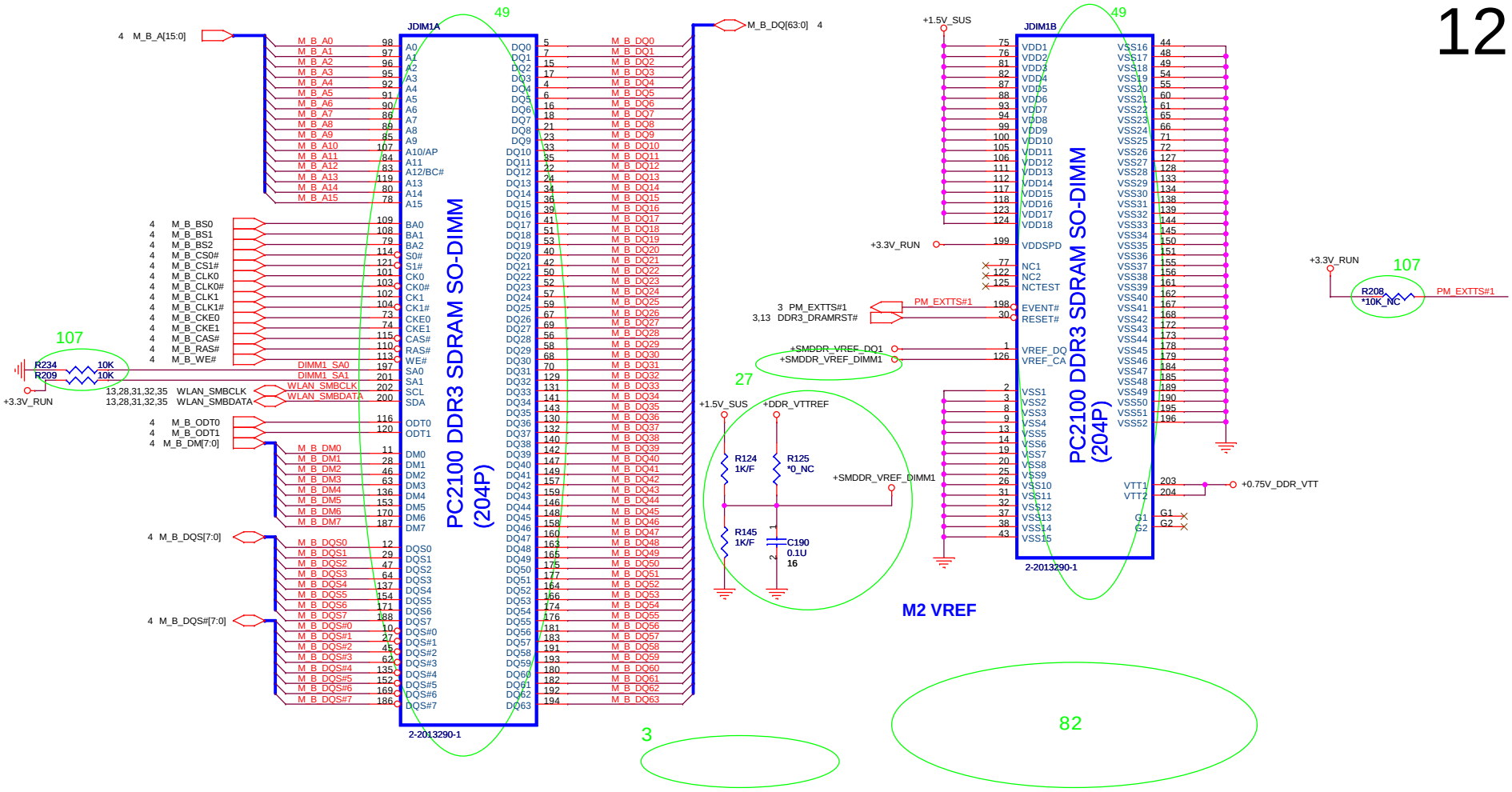

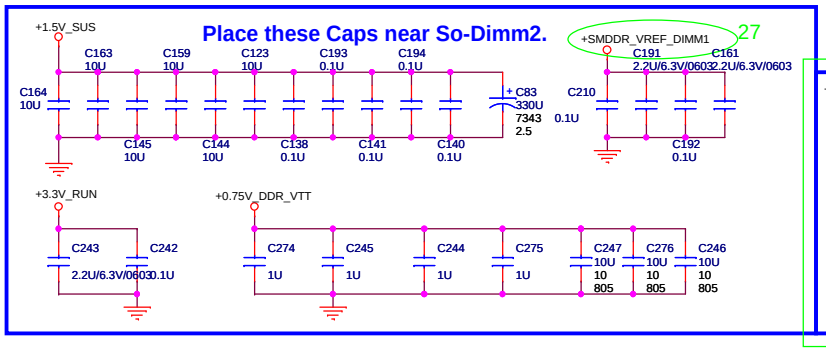

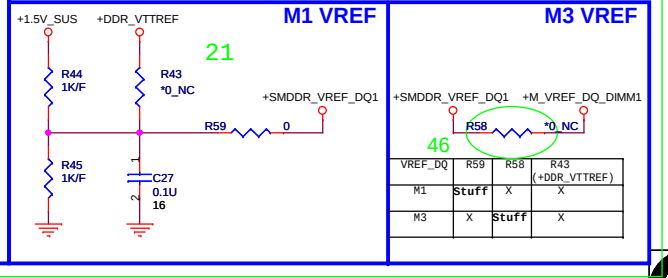

VREF_DQ	R59	R58	R43 (+DDR_VTTREF)
M1	Stuff	X	X
M3	X	Stuff	X

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Title	DDR3 DIMM-1	
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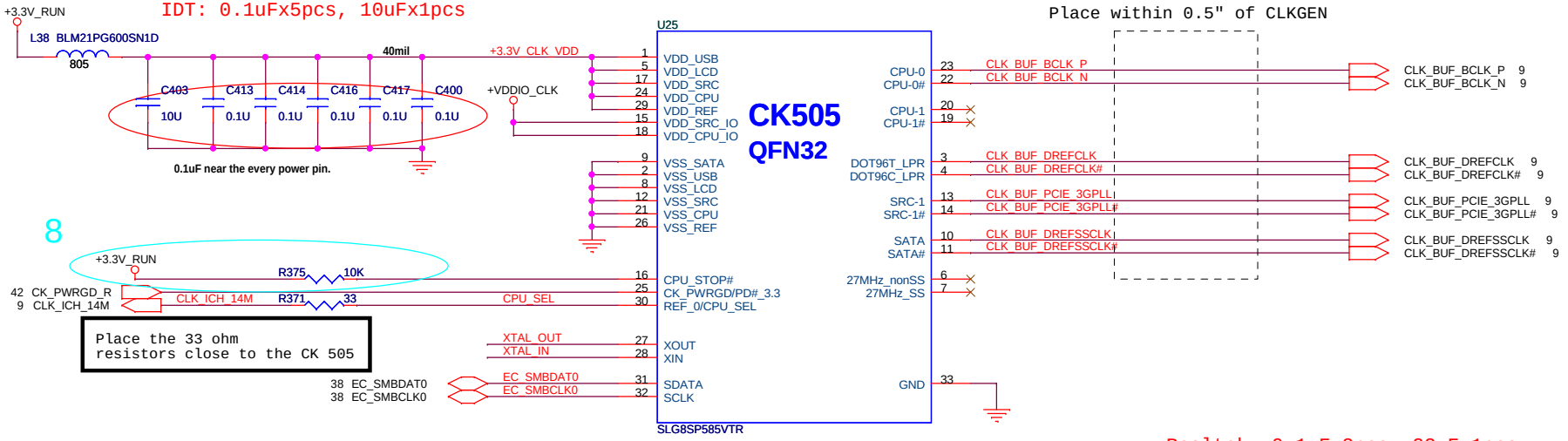
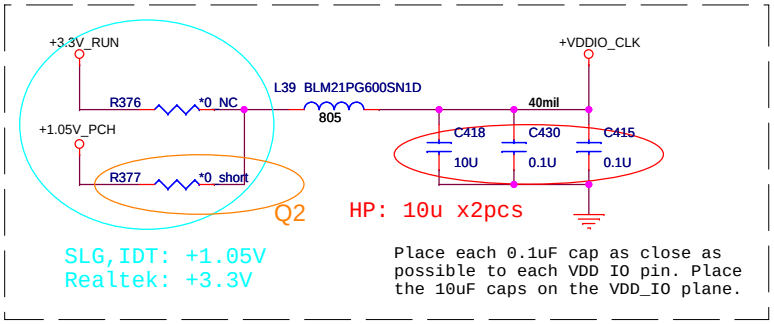
Realtek: 0.1uFx6pcs, 22uFx1pcs
IDT: 0.1uFx5pcs, 10uFx1pcs



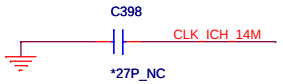
Place within 0.5" of CLKGEN

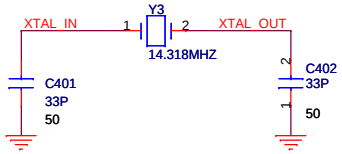
8

Realtek: 0.1uFx3pcs, 22uFx1pcs
IDT: 0.1uFx2pcs, 10uFx1pcs



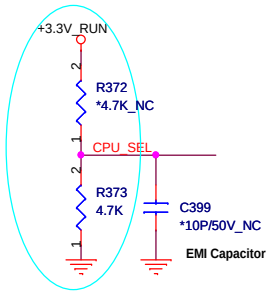
Add capacitor pads for improving WWAN.





+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V,Max3.465V.
Realtek date sheet(V1.2) P11: Min 1.05V,Max 3.3V.
IDT date sheet(V0.7) P10: Min 0.9975V,Max 3.465V.

7



PIN 30	CPU_0	CPU_1
0(default)	133MHz	133MHz
1(0.7V-1.5V)	100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet(V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet(V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.

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QUANTA COMPUTER

Title	VGA-M92-S (VRAM)	
Size	Document Number FM9B	Rev 3A
Date: Thursday, October 01, 2009	Sheet 20 of 65	

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QUANTA COMPUTER

Title	VGA-M92-XT (PCIe)	
Size	Document Number FM9B	Rev 3A
Date: Thursday, October 01, 2009	Sheet 21 of 65	

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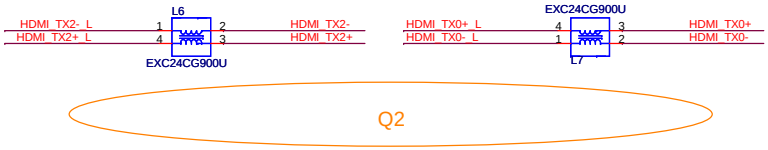
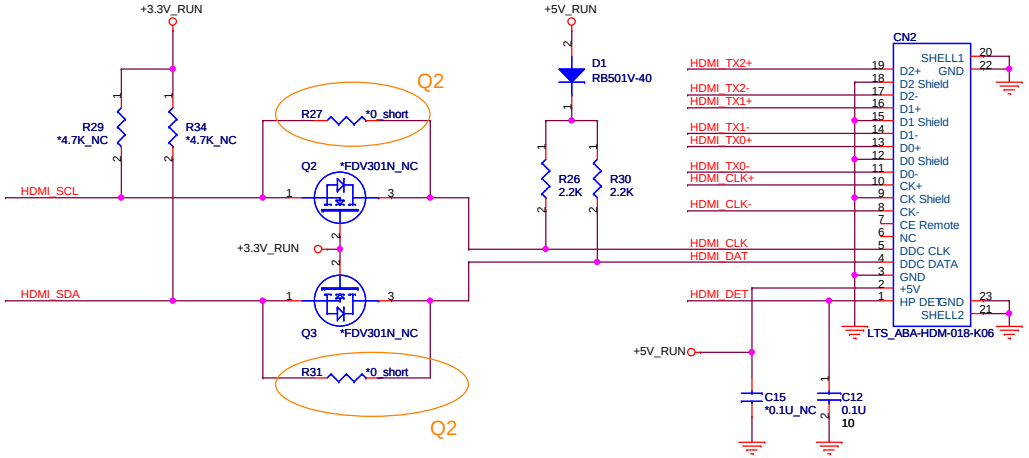
QUANTA COMPUTER

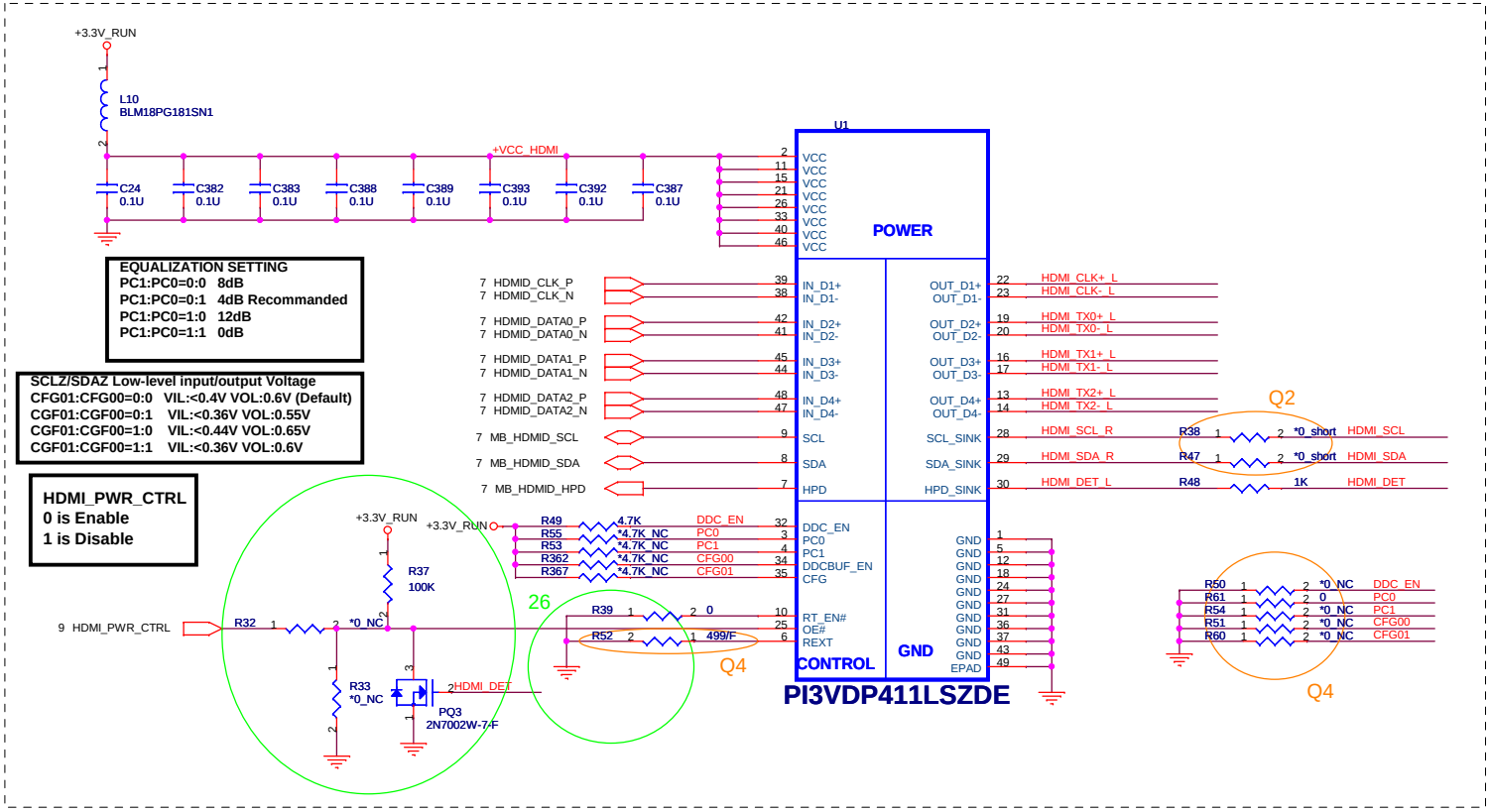
Title	VGA-M92-XT (PCIe)	
Size	Document Number FM9B	Rev 3A
Date: Thursday, October 01, 2009	Sheet 22 of 65	

HDMI

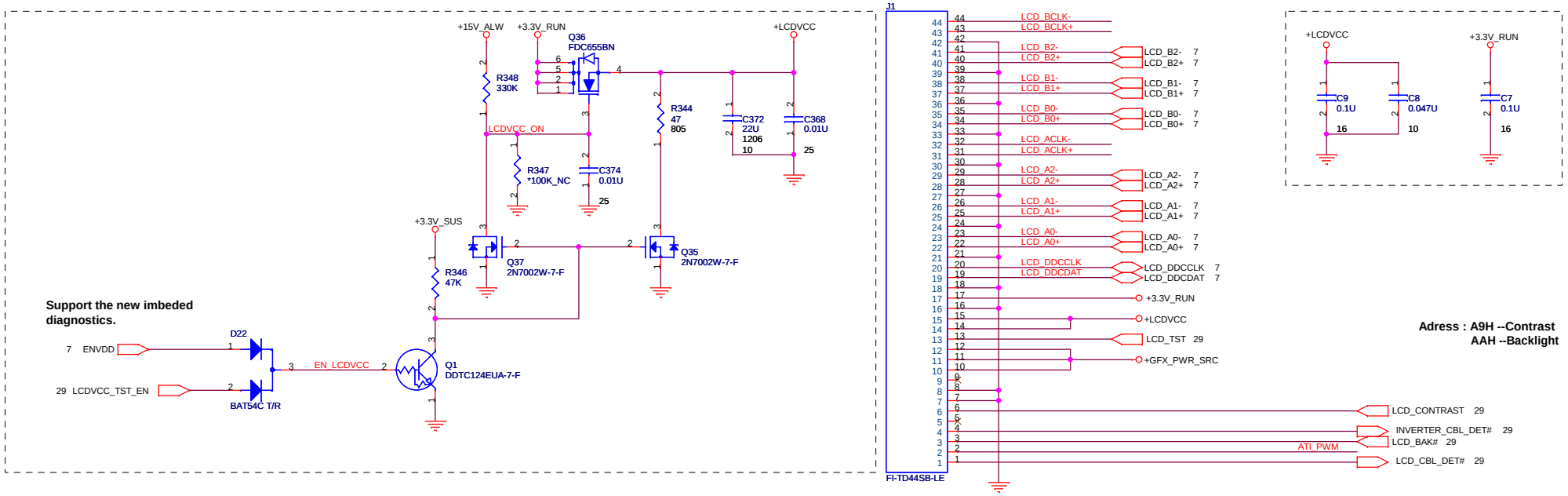


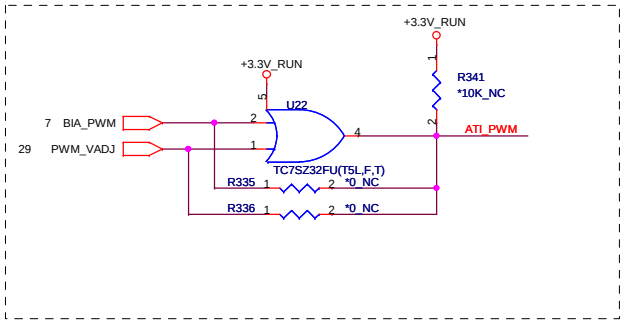
Reserve for EMI and close to HDMI CONN

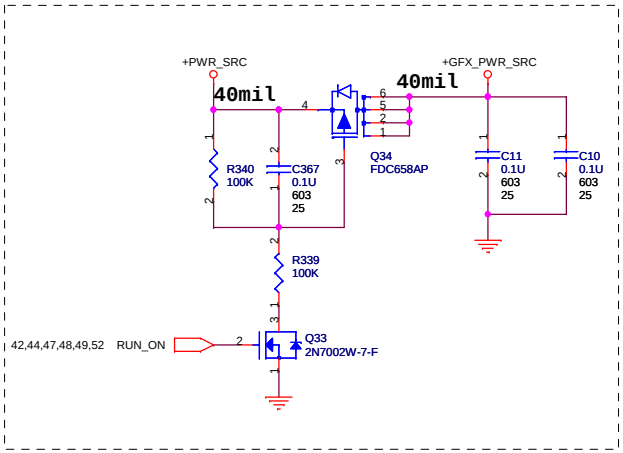


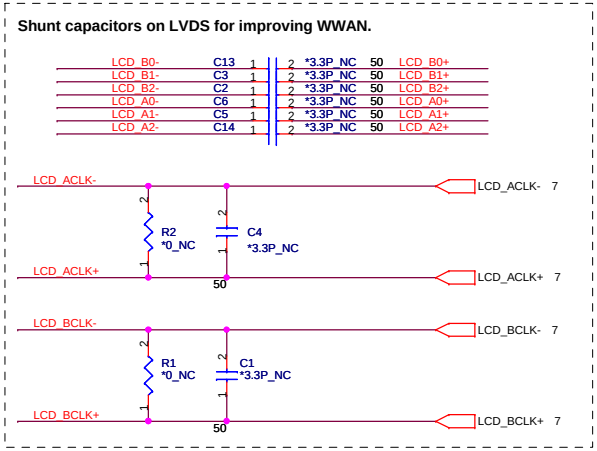


QUANTA COMPUTER		
Title: VGA-M82-S (PCIe)		
Size	Document Number: FM9B	Rev: 3A
Date: Monday, October 12, 2009	Sheet 23 of 65	



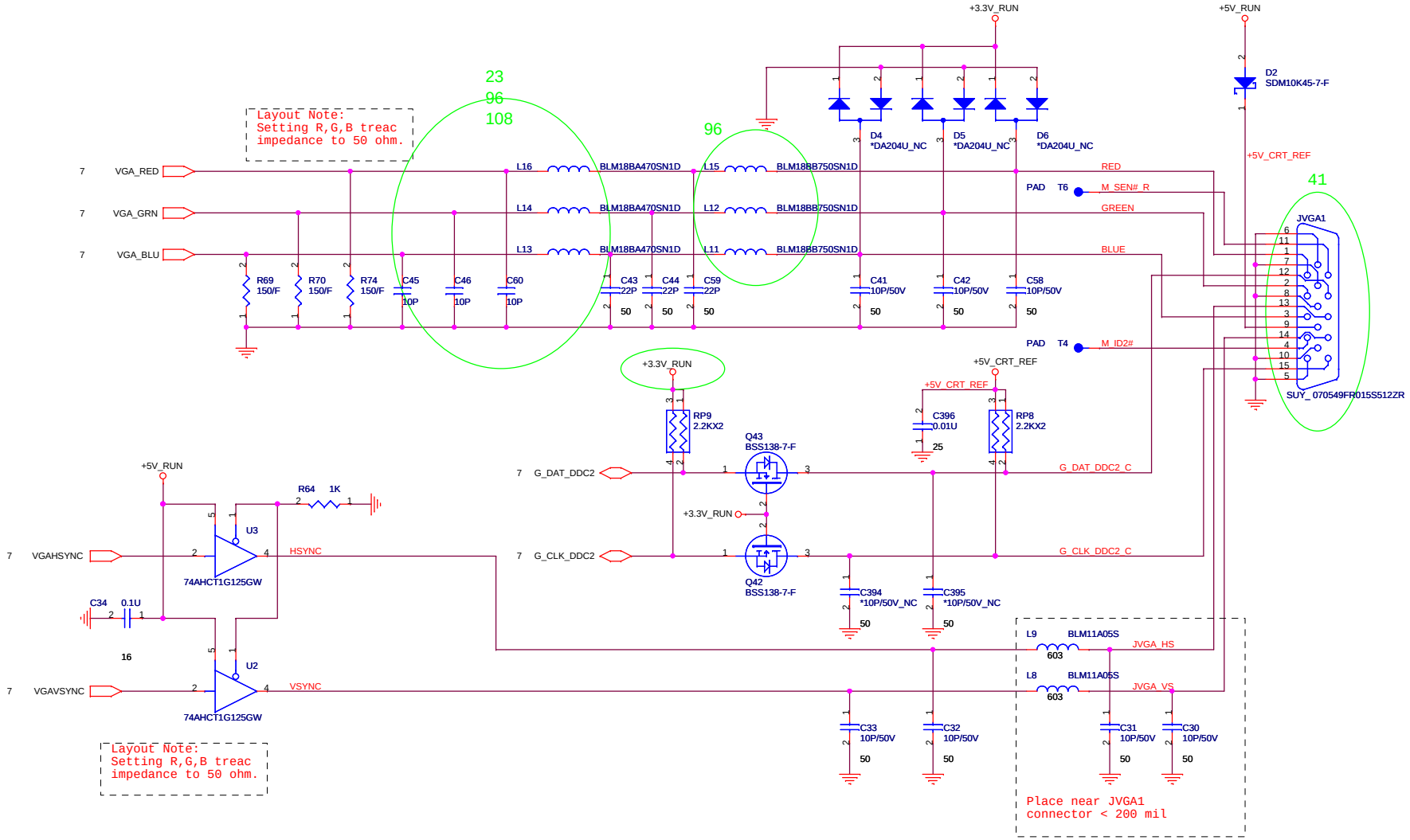






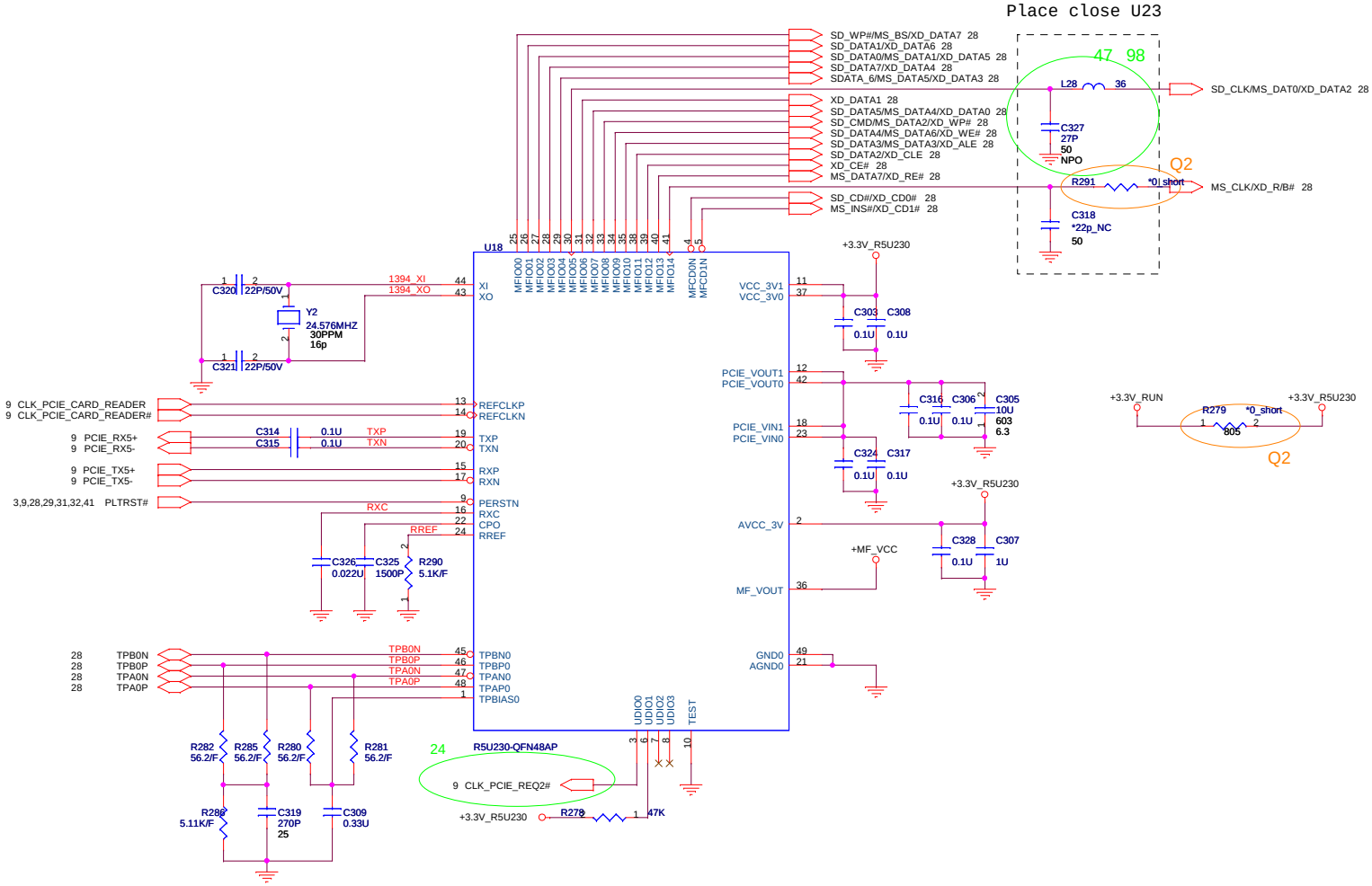
QUANTA COMPUTER

Title	LCD CONN & CK-SSCD	
Size	Document Number FM9B	Rev 3A
Date: Thursday, October 01, 2009	Sheet 24 of 65	



QUANTA COMPUTER

Title	CRT&TV CONN	
Size	Document Number FM9B	Rev 3A
Date: Thursday, October 01, 2009	Sheet 25 of 65	



MFIO Pin Assignment Table

MFIO	SD8	MS8	XD
00	WP	BS	D7
01	D1	-	D6
02	D0	D1	D5
03	D7	-	D4
04	D6	D5	D3
05	**CLK**	D0	D2
06	-	-	D1
07	D5	D4	D0
08	CMD	D2	WP#
09	D4	D6	WE#
10	D3	D3	ALE
11	D2	-	CLE
12	-	-	CE#
13	-	D7	RE#
14	-	**CLK**	R/B#

QUANTA COMPUTER

Title	5 IN 1 CONTROLLER	
Size	Document Number FM9B	Rev 3A
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QUANTA COMPUTER

Title	IEEE 1394	
Size	Document Number FM9B	Rev 3A
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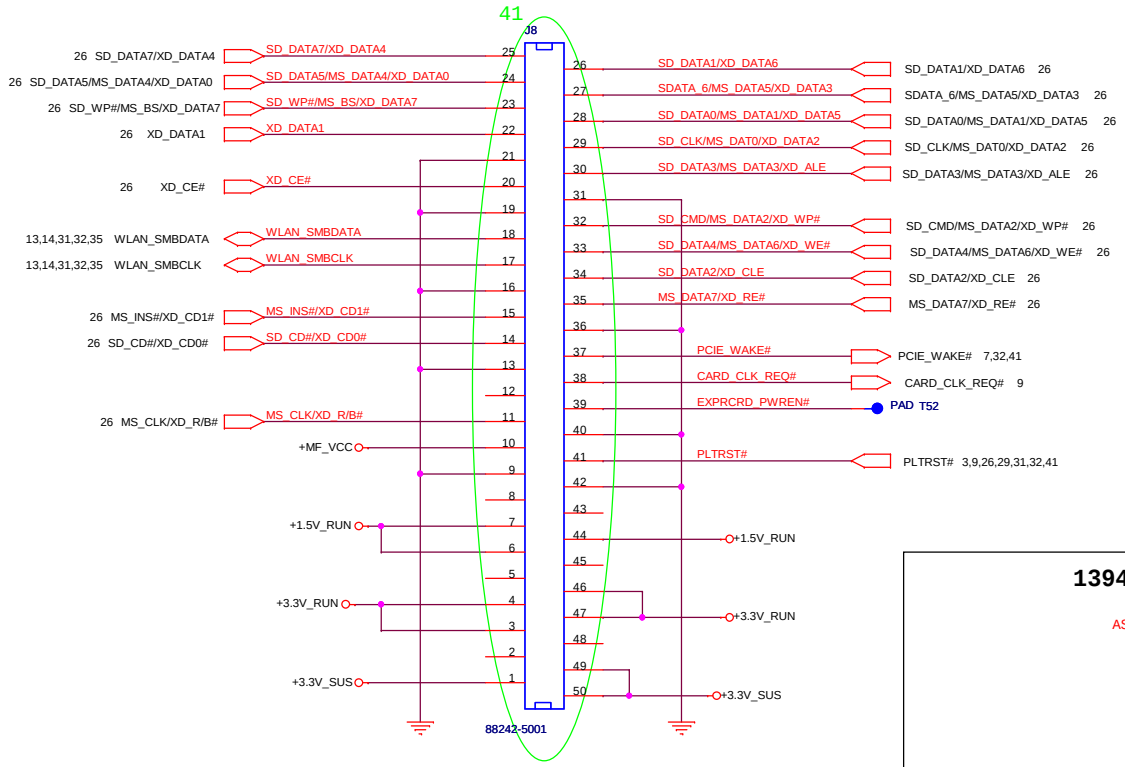
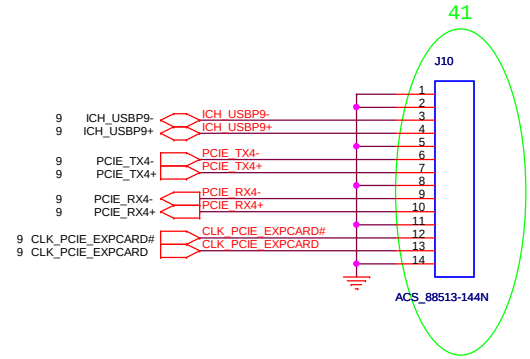
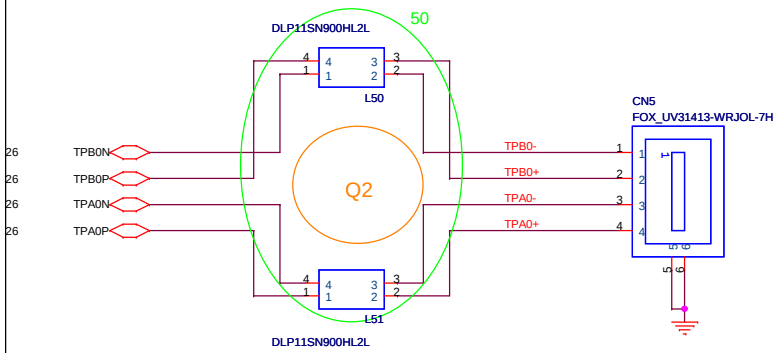
Express Card/CARD READER





1394 CONNECTOR

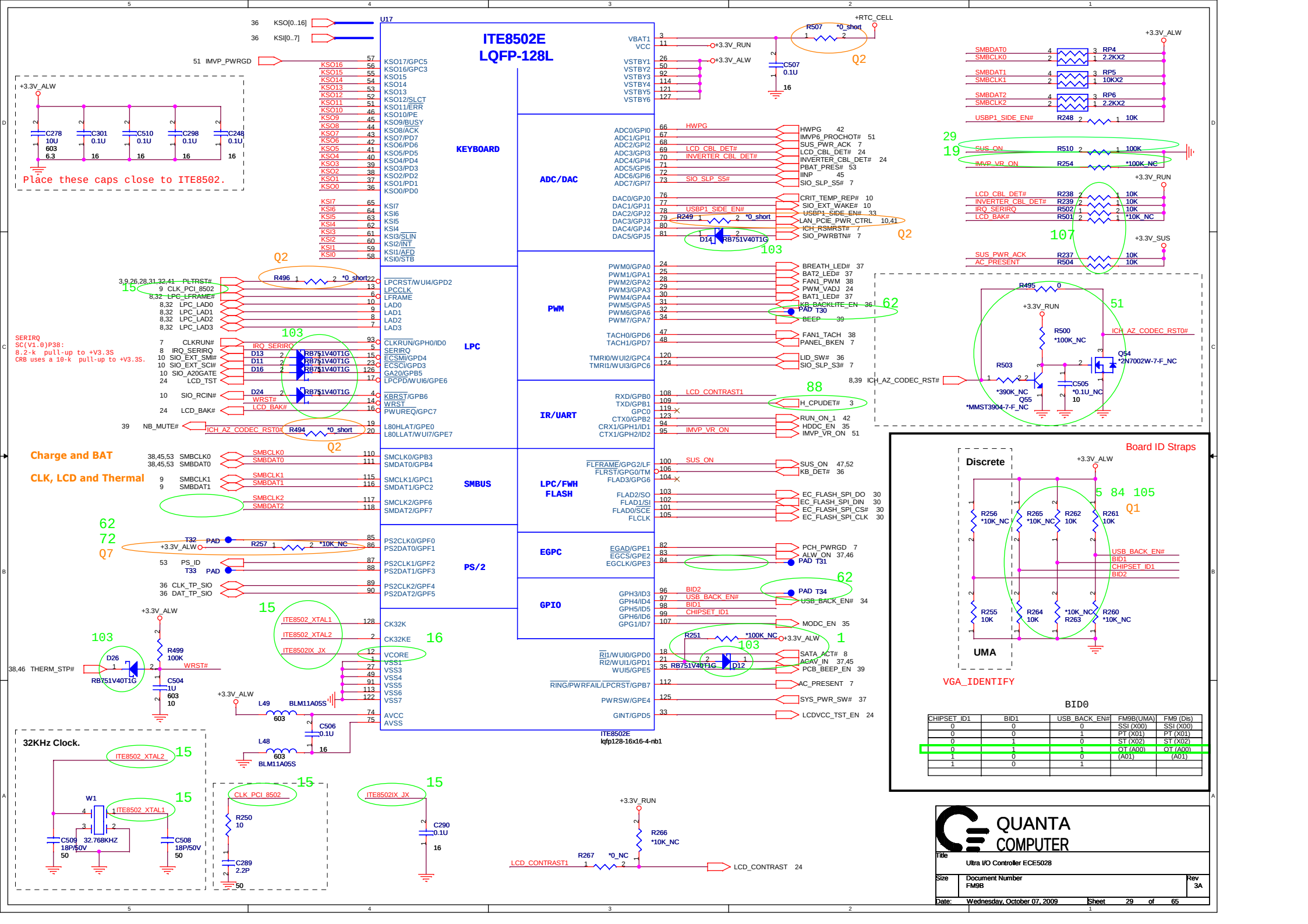
AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.



*TPA0P/TPA0N,TPB0P/TPB0N pair trace : As close as possible.
*TPA0P/TPA0N,TPB0P/TPB0N pair trace : Same length electrically.

QUANTA COMPUTER

Title	ExpressCard/SmartCard	
Size	Document Number FM9B	Rev 3A
Date: Thursday, October 01, 2009	Sheet 28 of 65	

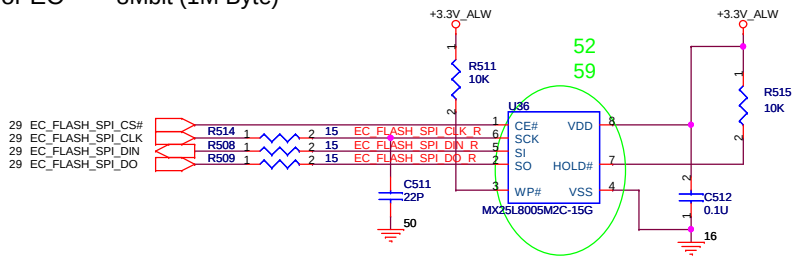


CHIPSET_ID1	BID1	USB_BACK_EN#	FM9B(UMA)	FM9 (Dis)
0	0	0	SSI (X00)	SSI (X00)
0	0	1	PT (X01)	PT (X01)
0	1	0	ST (X02)	ST (X02)
0	1	1	OT (A00)	OT (A00)
1	0	0	(A01)	(A01)
1	0	1		

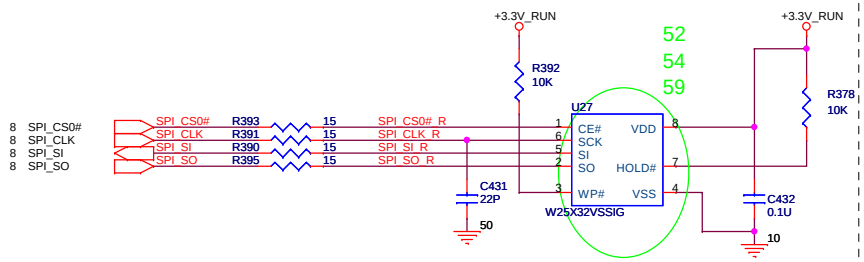
QUANTA COMPUTER

Title	Ultra I/O Controller ECE5028	
Size	Document Number FM9B	Rev 3A
Date:	Wednesday, October 07, 2009	Sheet 29 of 65

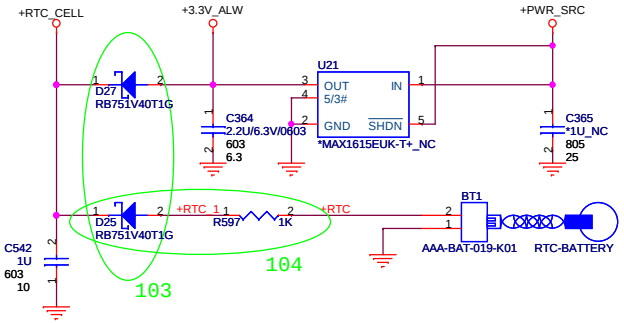
For EC 8Mbit (1M Byte)



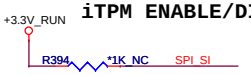
For PCH 32Mbit (4M Byte)



RTC BATTERY



iTPM ENABLE/DISABLE



TPM Function	R712
Enable	Mount
Disable	NC (Default)

QUANTA COMPUTER

Title	Ultra I/O Controller ECE5028	
Size	Document Number FM9B	Rev 3A
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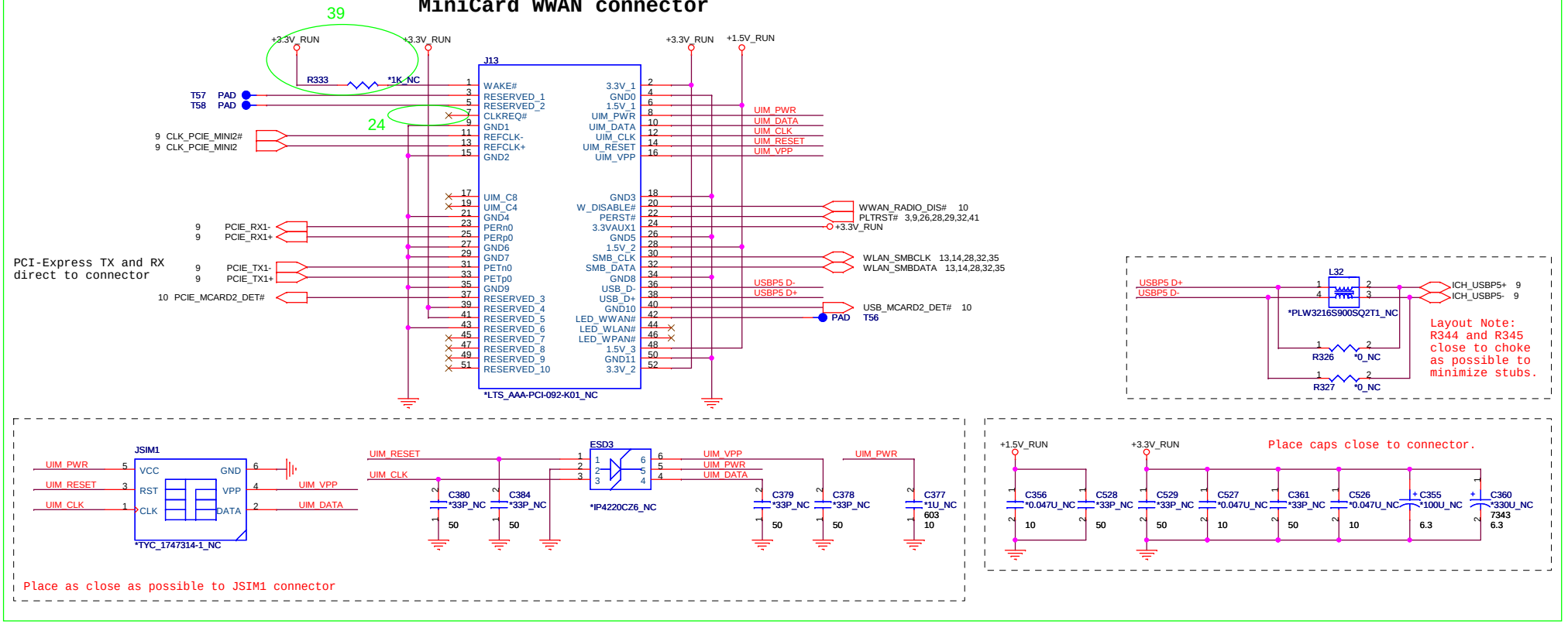
MiniCard WWAN connector



Title	MINI-PCI	
Size	Document Number FM9B	Rev 3A
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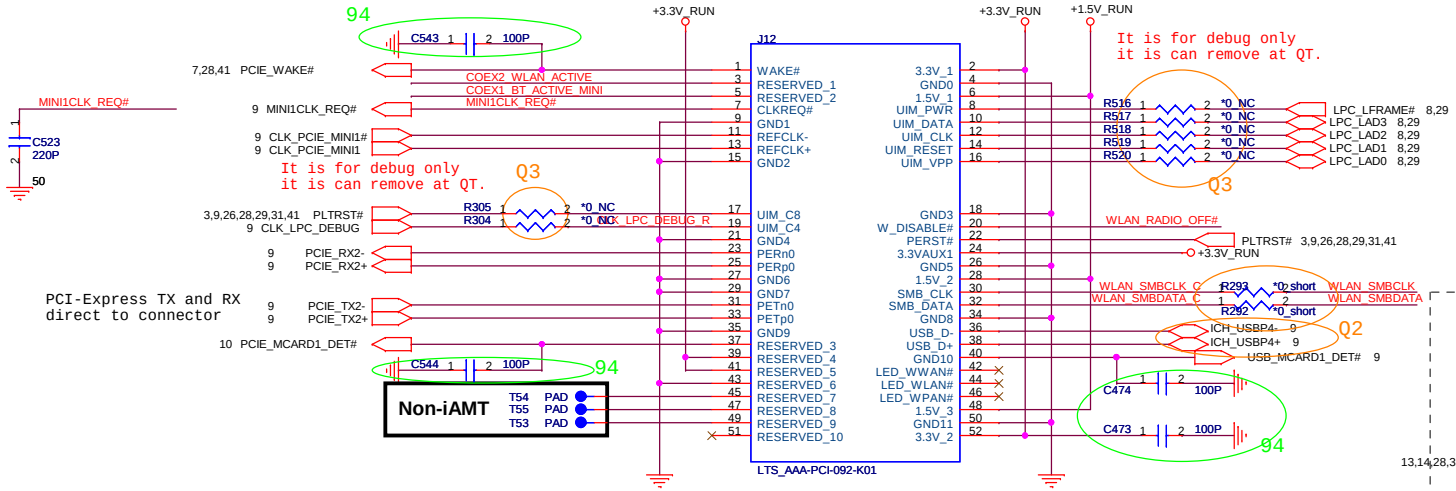
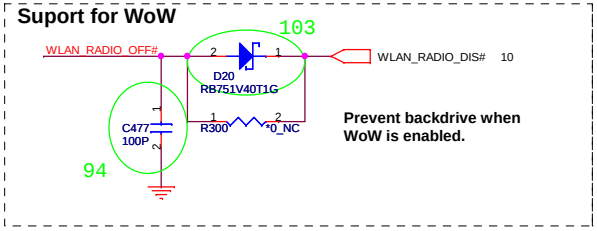
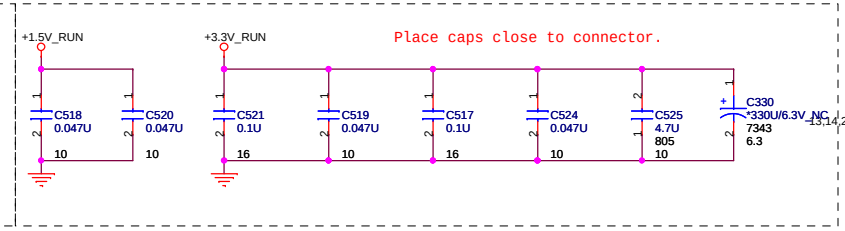
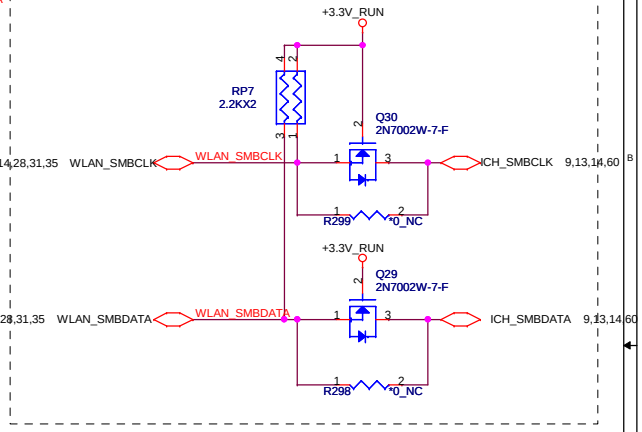
QUANTA COMPUTER

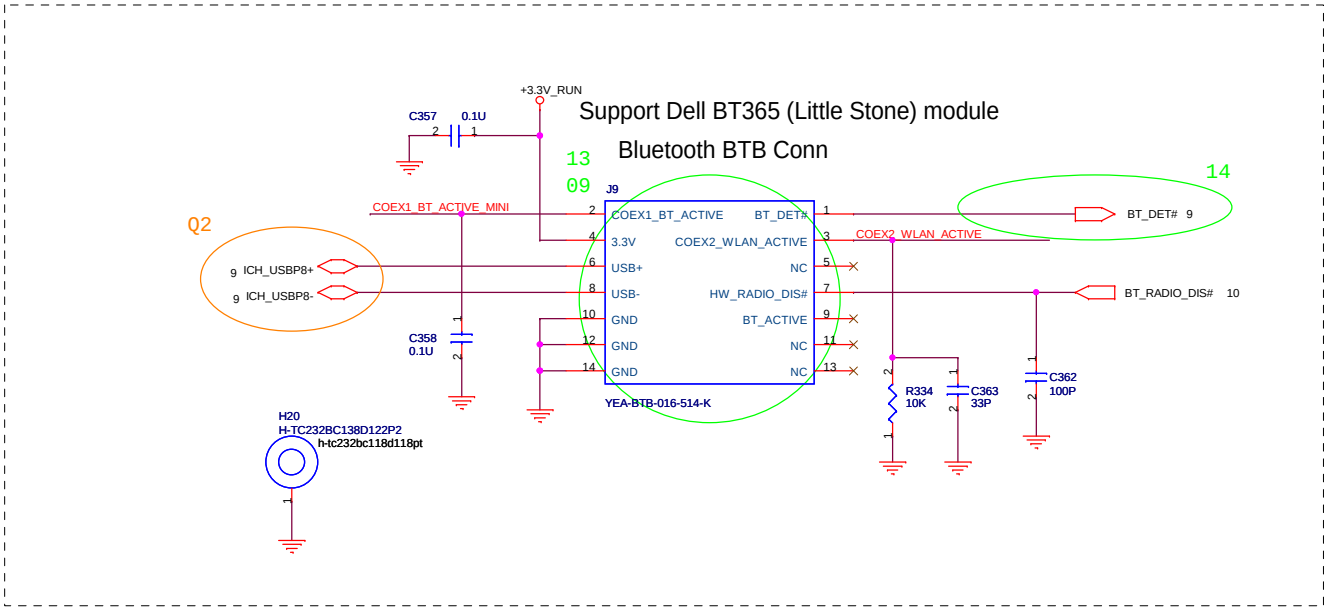
MiniCard WLAN connector











QUANTA COMPUTER		
Title	MDC CONN.	
Size	Document Number FM9B	Rev 3A
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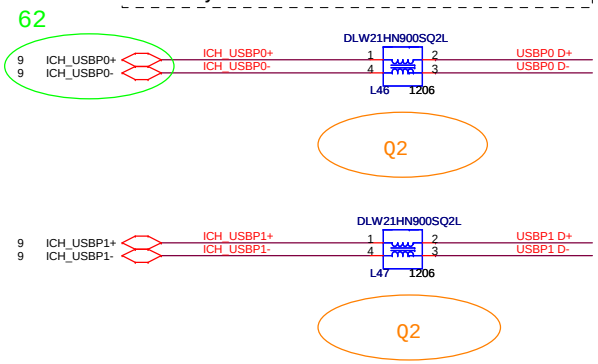
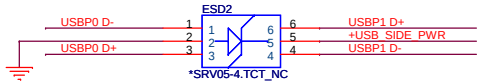
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



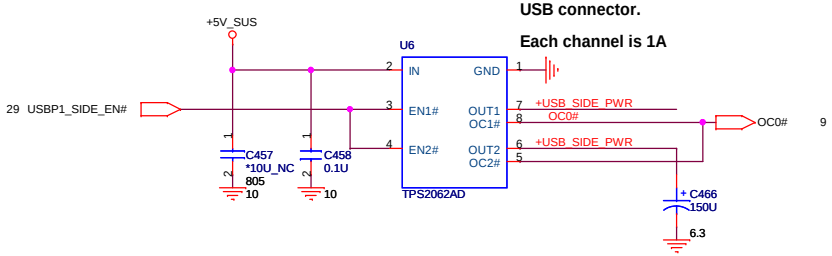
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

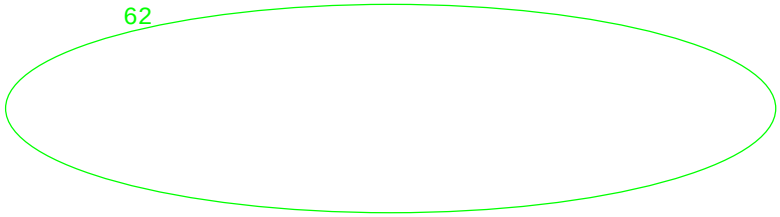
Place ESD diodes as close as USB connector.



Place one 150uF cap by each USB connector.

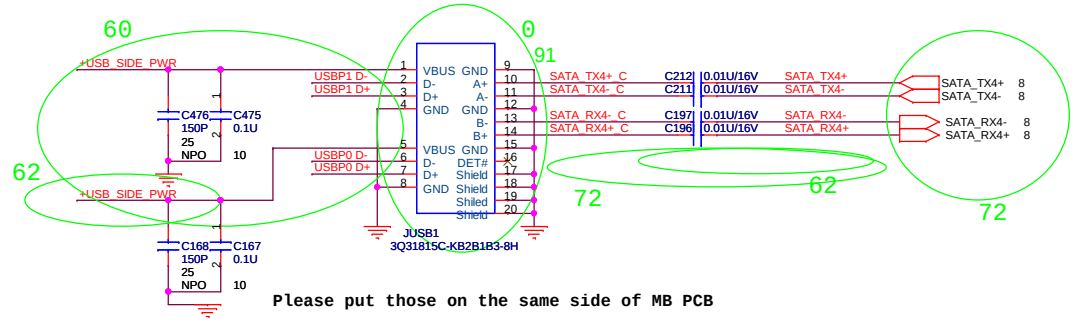
Each channel is 1A





Side External USBX2

PN is old, Because New Part can't ready before SST build.

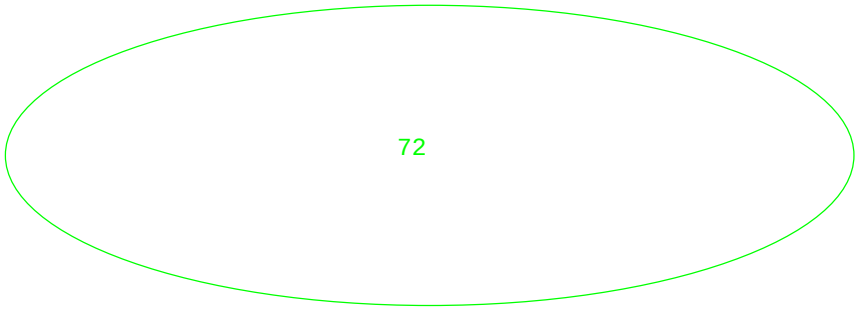


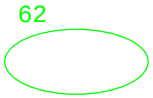
Please put those on the same side of MB PCB

USBx2 & ESATA COMBO

USB BUS SW

E-SATA Re-driver





QUANTA COMPUTER

Title	SERIAL PORT & USB	
Size	Document Number FM9B	Rev 3A
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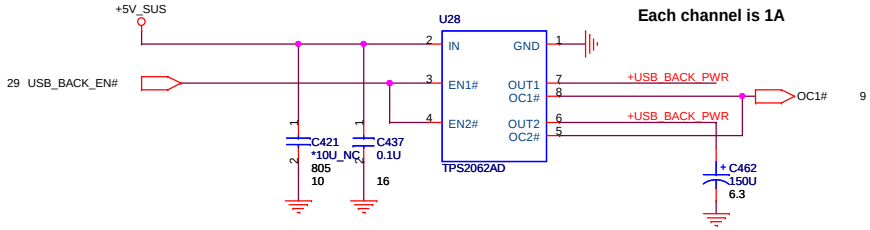
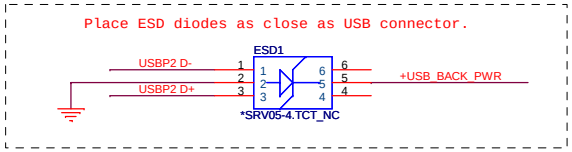
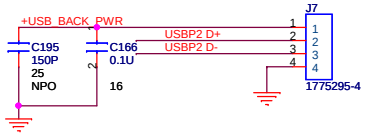
Q2

Place one 150uF cap by each USB connector.

Each channel is 1A







QUANTA COMPUTER

Title	Right USB	
Size	Document Number FM9B	Rev 3A
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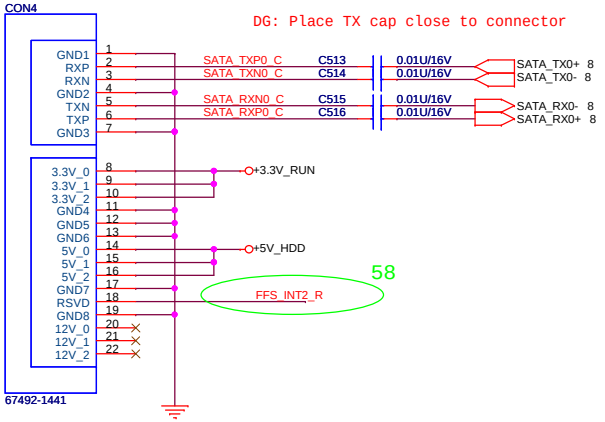
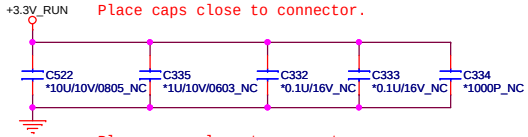
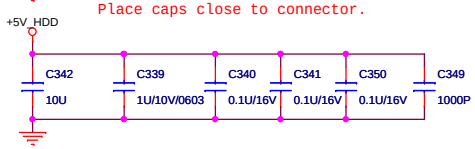
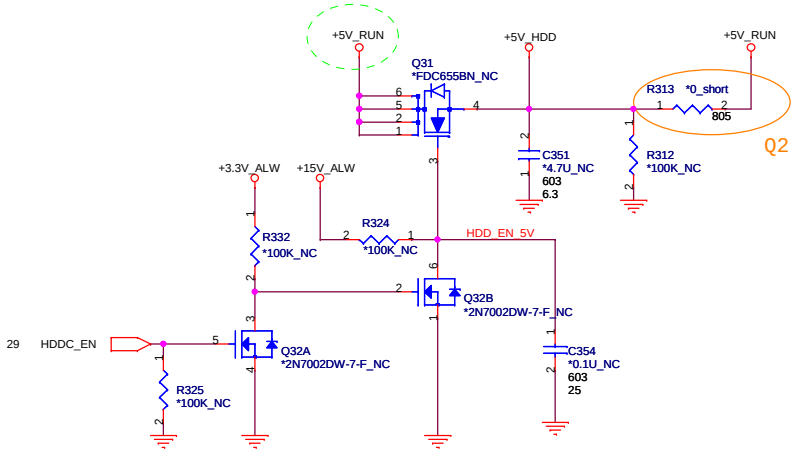
SATA Connector.

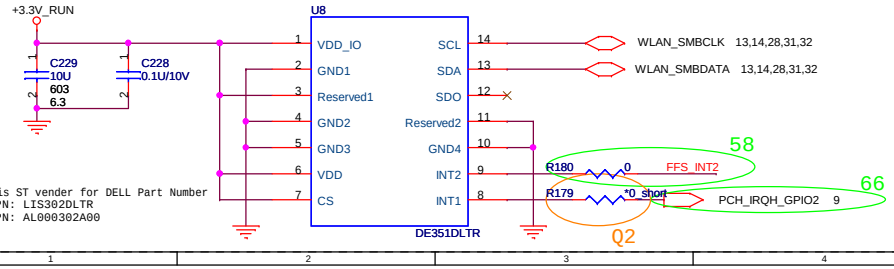




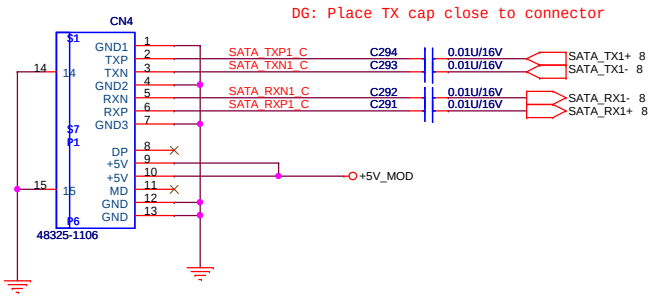


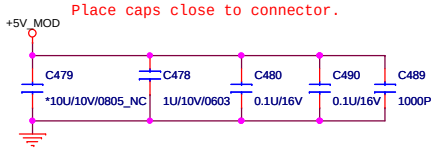


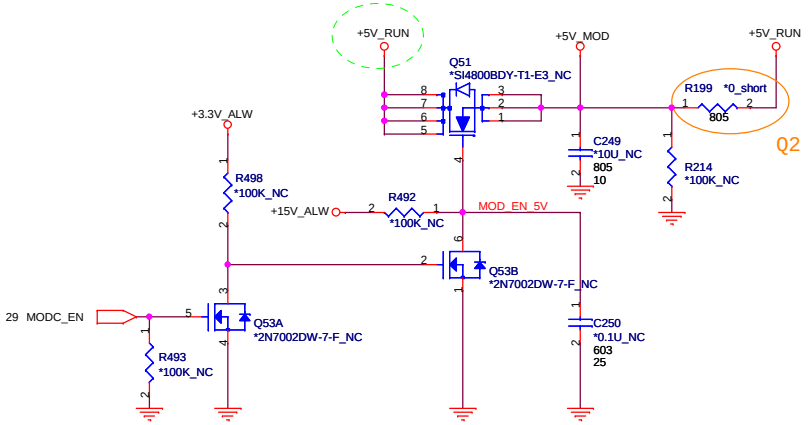
3-axis Fall Sensor (HDD data protector)

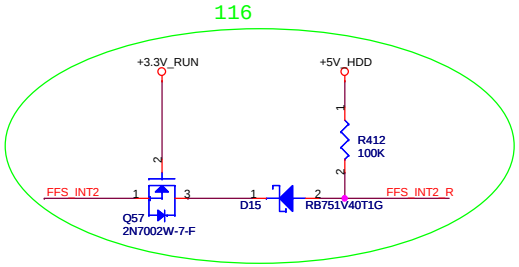


ODD Connector





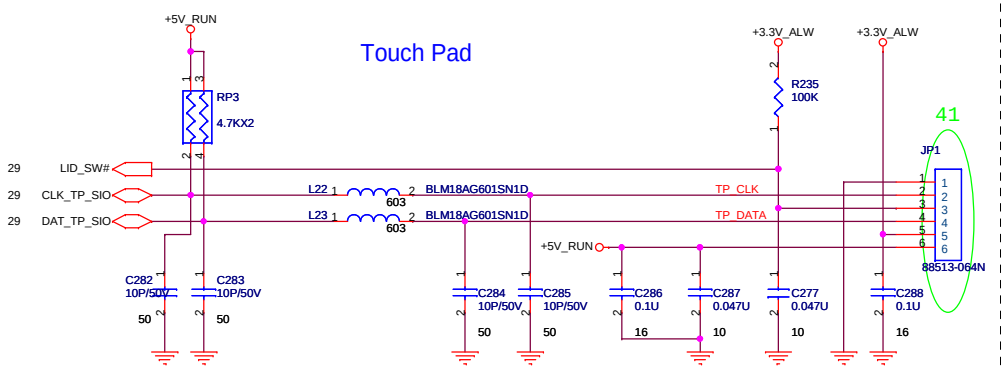




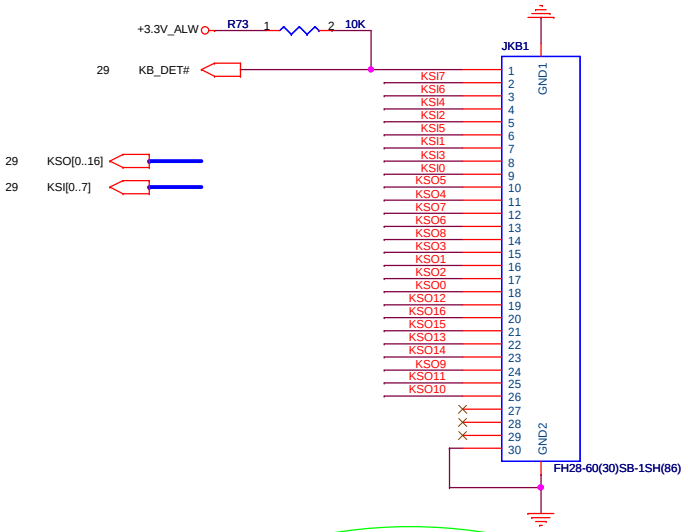
QUANTA COMPUTER

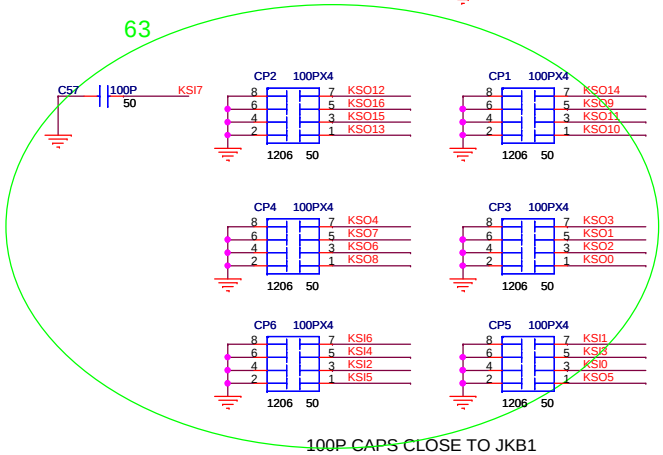
Title	SATA (HDD&CD_ROM)	
Size	Document Number FM9B	Rev 3A
Date: Monday, October 05, 2009	Sheet 35 of 65	

Touch Pad



KEYBOARD CONNECTOR

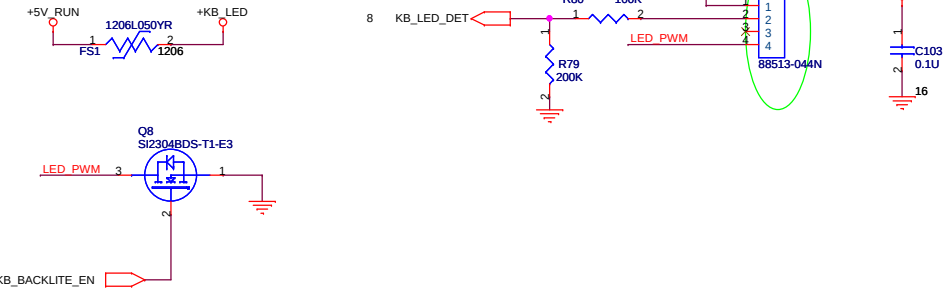




100P CAPS CLOSE TO JKB1

Key board illumination

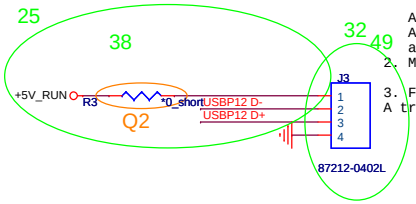
+KB_LED power trace width >10 mil



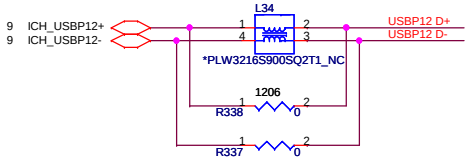
QUANTA COMPUTER		
Title	TOUCH PAD, BULE TOOTH & FIR	
Size	Document Number FM9B	Rev 3A
Date: Thursday, October 01, 2009	Sheet 36 of 65	

Touch Screen Module

Note:
1. VBUS IND:VBUS indication should be supplied to single the DuoSense to connect According to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
2. Maximum cable resistance on VCC, GND should be 150m ohm.
3. FPC cable should support 12MHz USB singles. A tri-state should indicate no connection.

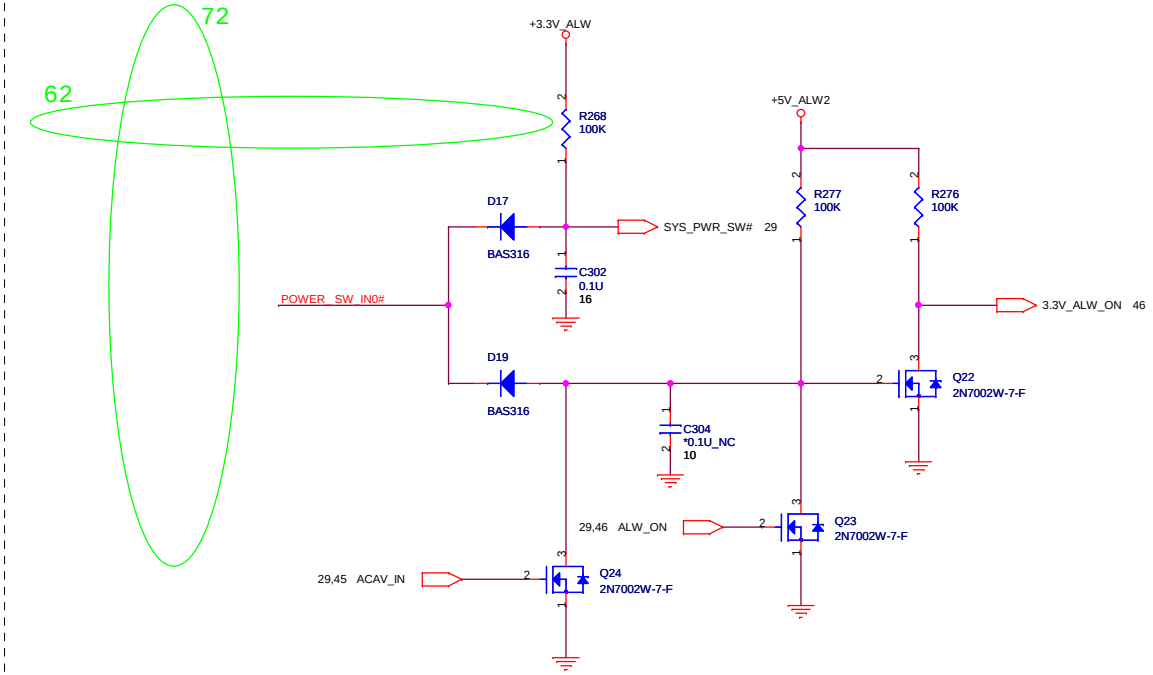


Need check the connector footprint and symble.

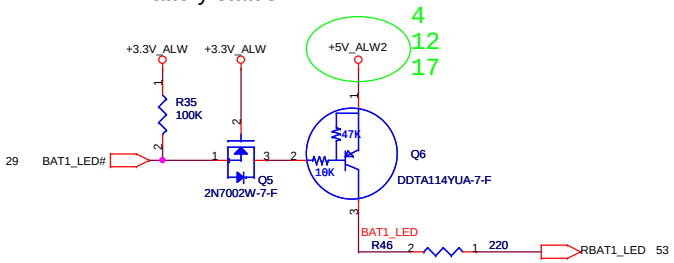


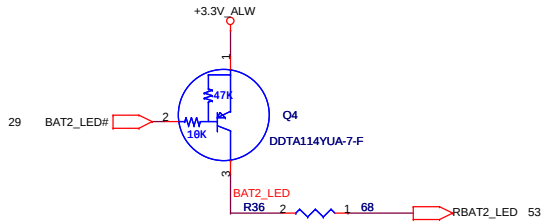
Power button Cable

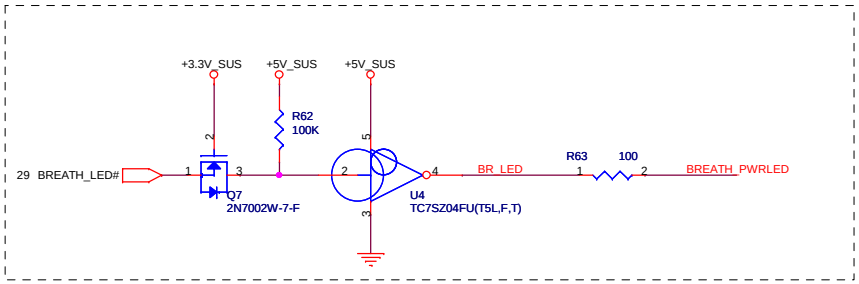
3VALW ON POWER LOGIC

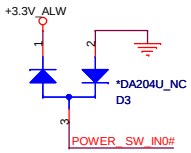


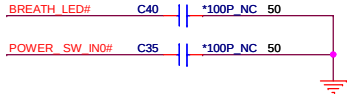
Battery status.





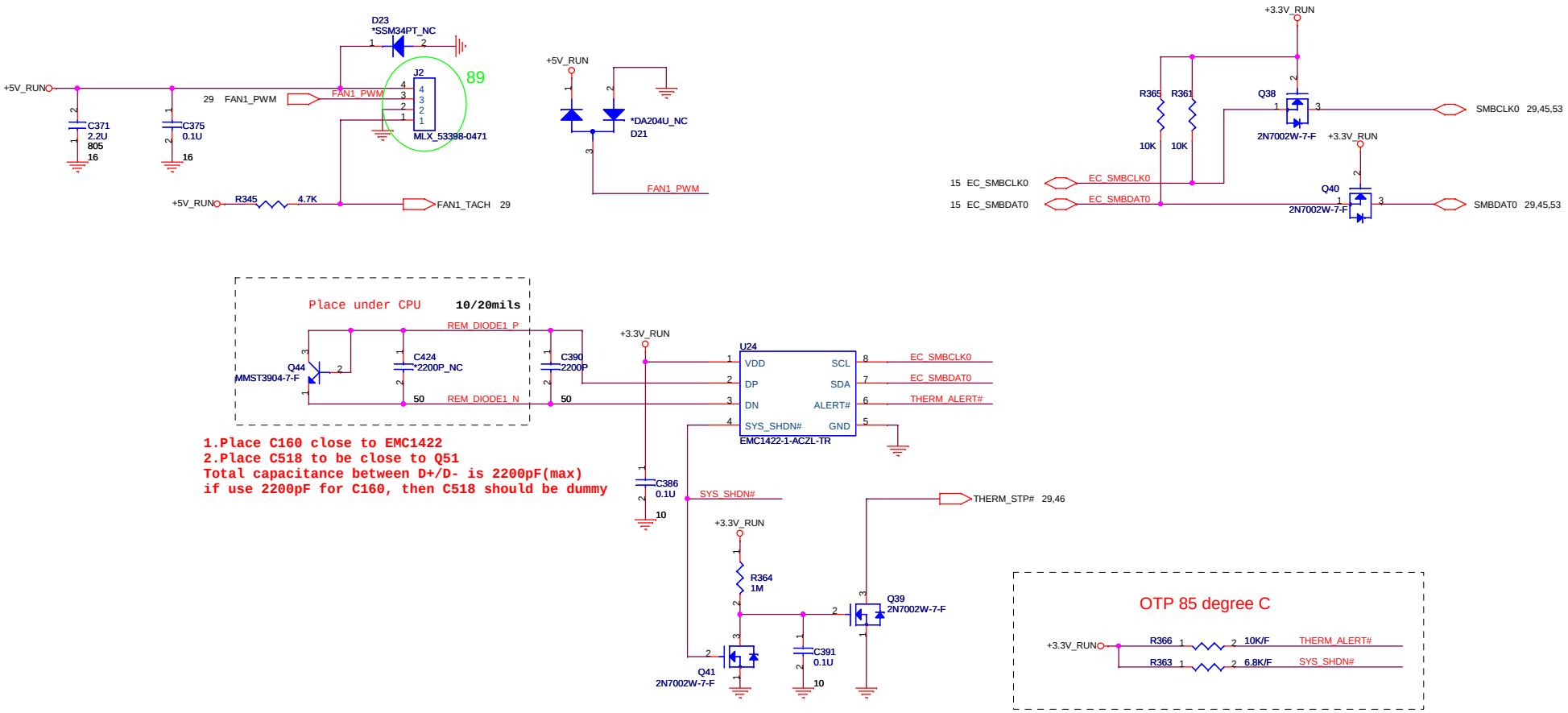






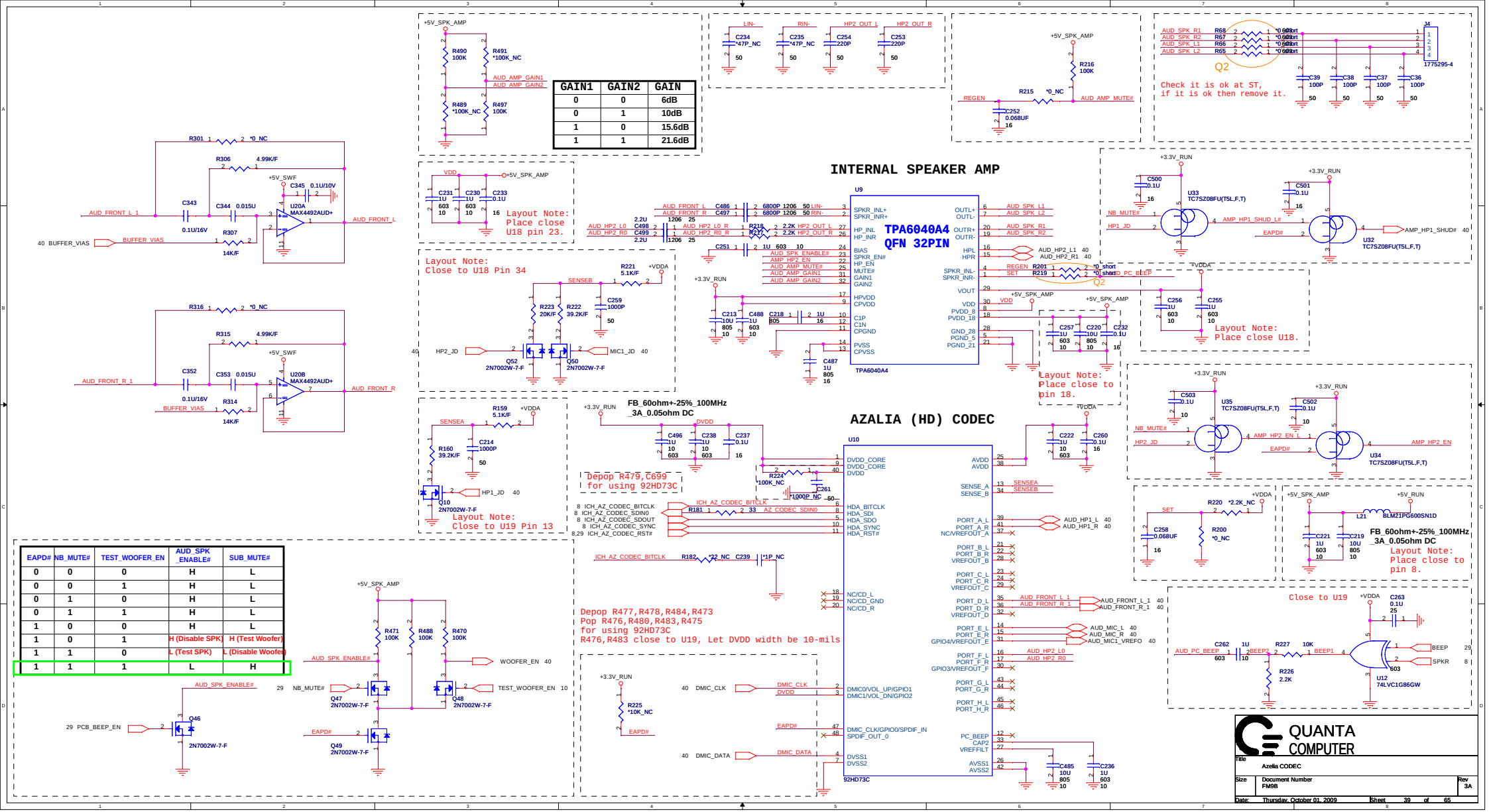
QUANTA COMPUTER

Title	SWITCH, KEYBOARD & LED&Touch Screen Module	
Size	Document Number FM9B	Rev 3A
Date: Monday, October 05, 2009	Sheet 37 of 65	

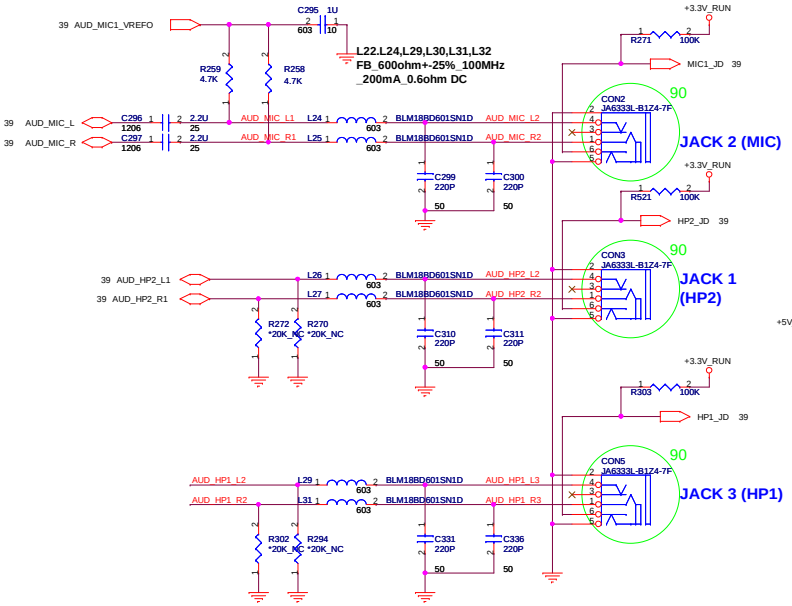


QUANTA COMPUTER

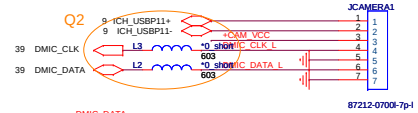
Title	FAN & THERMAL	
Size	Document Number FM9B	Rev 3A
Date: Thursday, October 01, 2009	Sheet 38 of 65	

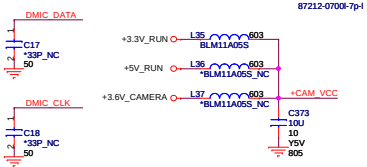

INTERNAL SPEAKER AMP
TPA6040A4
QFN 32PIN
AZALIA (HD) CODEC
92HD73C
GAIN1 GAIN2 GAIN
0 0 6dB
0 1 10dB
1 0 15.6dB
1 1 21.6dB
EAPD# NB_MUTE# TEST_WOOFER_EN AUD_SPK ENABLE# SUB_MUTE#
0 0 0 H L
0 0 1 H L
0 1 0 H L
0 1 1 H L
1 0 0 H L
1 0 1 H (Disable SPK) H (Test Woofer)
1 1 0 L (Test SPK) L (Disable Woofer)
1 1 1 L H
Layout Note: Place close U18 pin 23.
Layout Note: Close to U18 Pin 34
Layout Note: Close to U19 Pin 13
Layout Note: Place close to pin 18.
Layout Note: Place close U18.
Layout Note: Place close to pin 8.
Depop R479,C699 for using 92HD73C
Depop R477,R478,R484,R473 Pop R476,R480,R483,R475 for using 92HD73C
R476,R483 close to U19, Let DVDD width be 10-mils
Check it is ok at ST, if it is ok then remove it.
FB_60ohm+-25%_100MHz _3A_0.05ohm DC
QUANTA COMPUTER
Azelia CODEC
Document Number FM9B
Thursday, October 01, 2009

Headphone Jack
Stereo MIC Jack

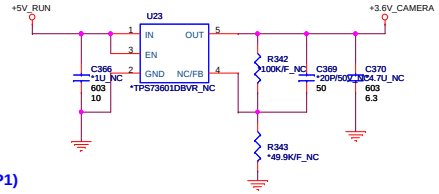


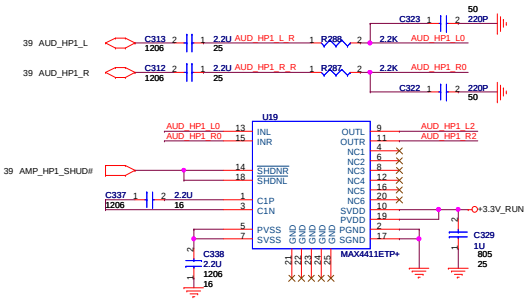
Array Microphone & Camera





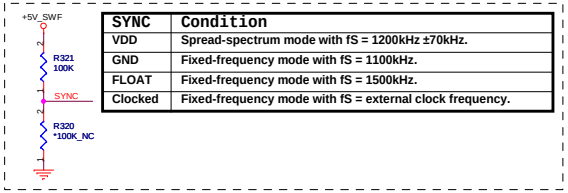
Q2



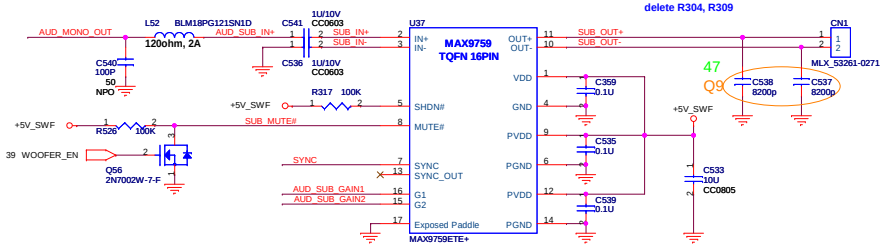


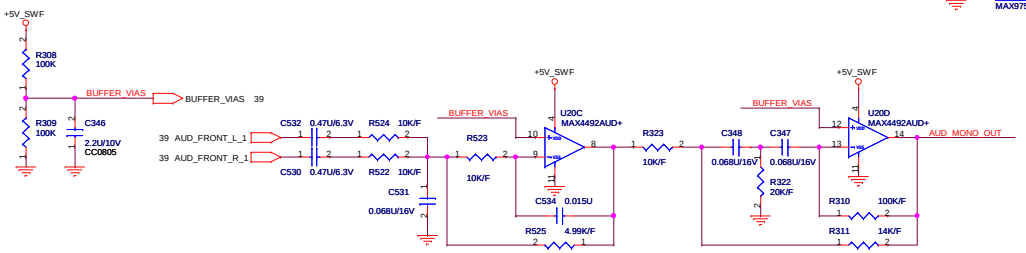
INTERNAL SUBWOOFER AMP

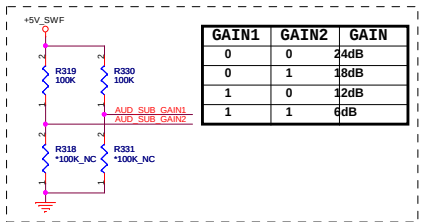
SYNC	Condition
VDD	Spread-spectrum mode with fS = 1200kHz ±70kHz.
GND	Fixed-frequency mode with fS = 1100kHz.
FLOAT	Fixed-frequency mode with fS = 1500kHz.
Clocked	Fixed-frequency mode with fS = external clock frequency.



Gur_0808: 0 ohm removal,
delete R304, R309







GAIN1	GAIN2	GAIN
0	0	24dB
0	1	18dB
1	0	12dB
1	1	6dB

QUANTA COMPUTER

Title	AUDIO CONN	
Size	Document Number FM9B	Rev 3A
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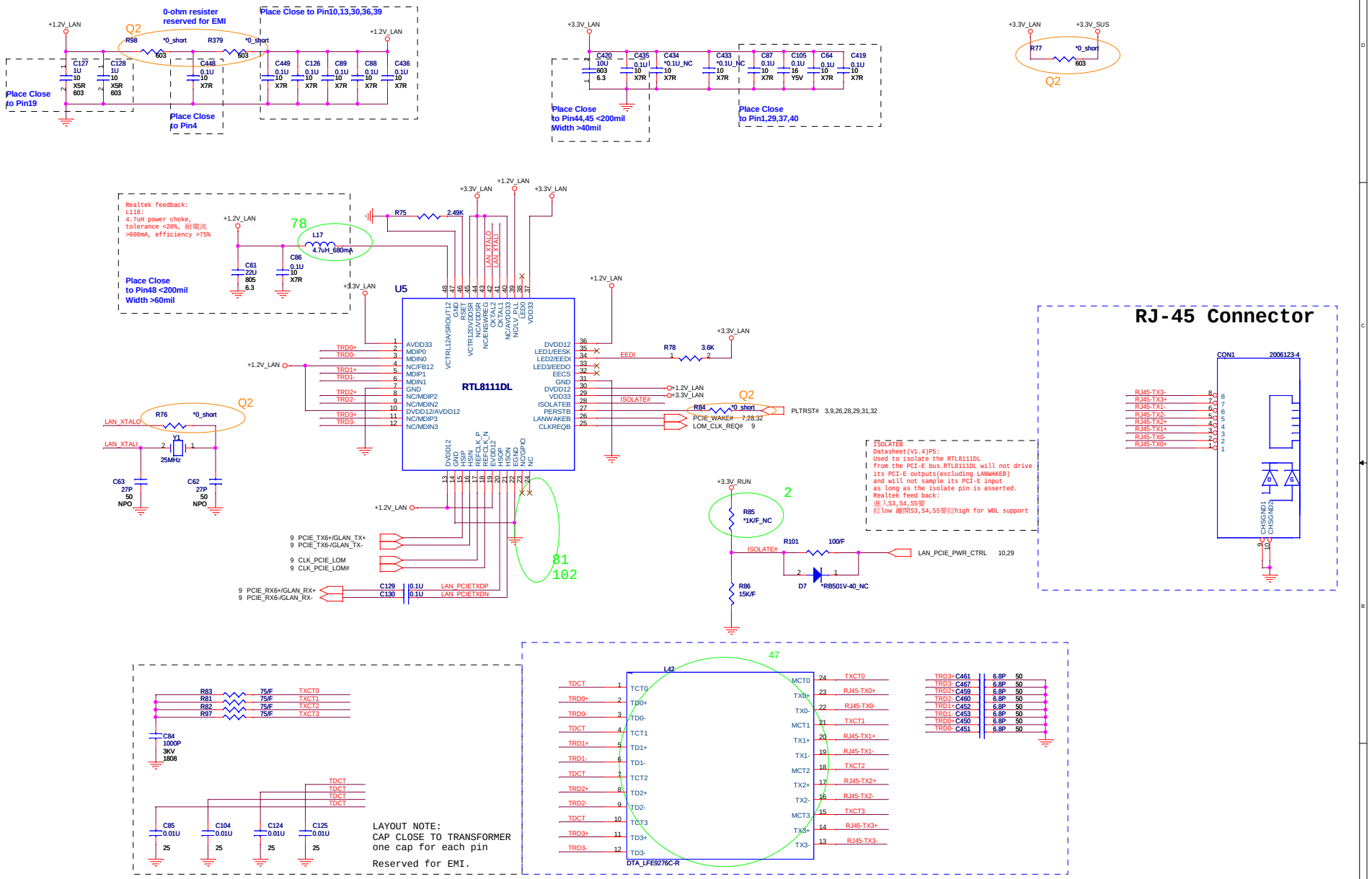
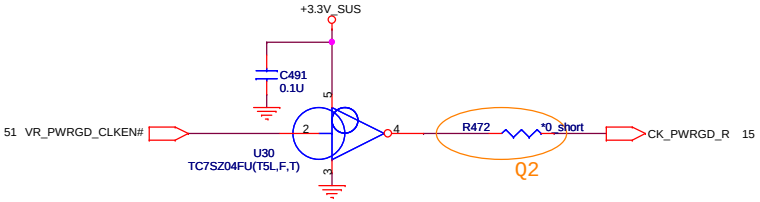
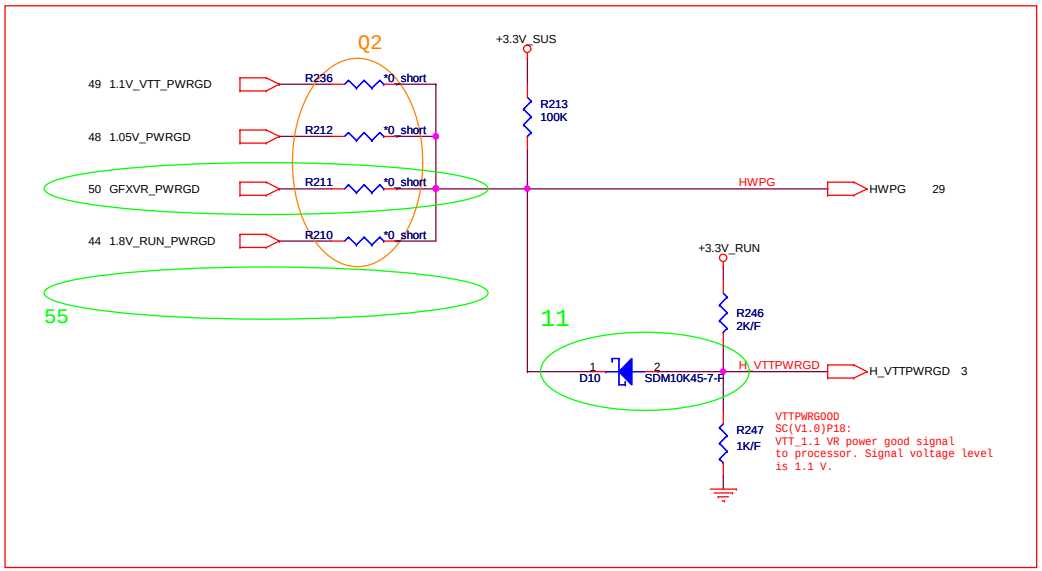
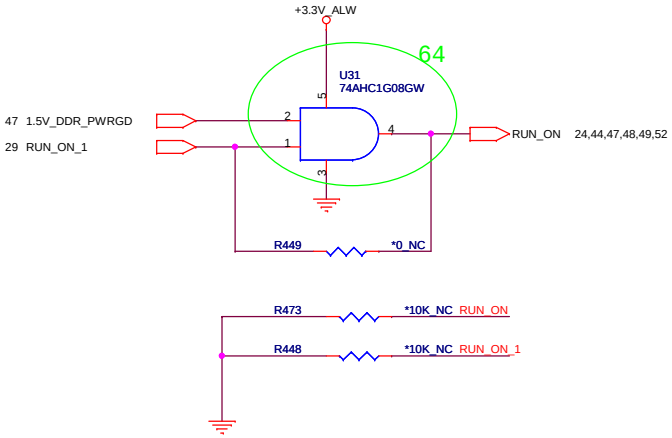

0-ohm resister reserved for EMI
Place Close to Pin10,13,30,36,39
Place Close to Pin19
Place Close to Pin4
Place Close to Pin44,45 <200mil Width >40mil
Place Close to Pin1,29,37,40
Realtek feedback: L118: 4.7uH power choke, tolerance <20%, 耐電流 >600mA, efficiency >75%
Place Close to Pin48 <200mil Width >60mil
RTL8111DL
U5
RJ-45 Connector
CON1 2006123-4
ISOLATEB Datasheet(V1.4)P5: Used to isolate the RTL8111DL from the PCI-E bus.RTL8111DL will not drive its PCI-E outputs(excluding LANWAKEB) and will not sample its PCI-E input as long as the isolate pin is asserted. Realtek feed back: 進入S3,S4,S5要拉low 離開S3,S4,S5要拉high for WOL support
LAYOUT NOTE: CAP CLOSE TO TRANSFORMER one cap for each pin
Reserved for EMI.
DTA_LFE9276C-R
QUANTA COMPUTER
Title LAN
Size Document Number FM9B Rev 3A
Date: Monday, October 05, 2009 Sheet 41 of 65





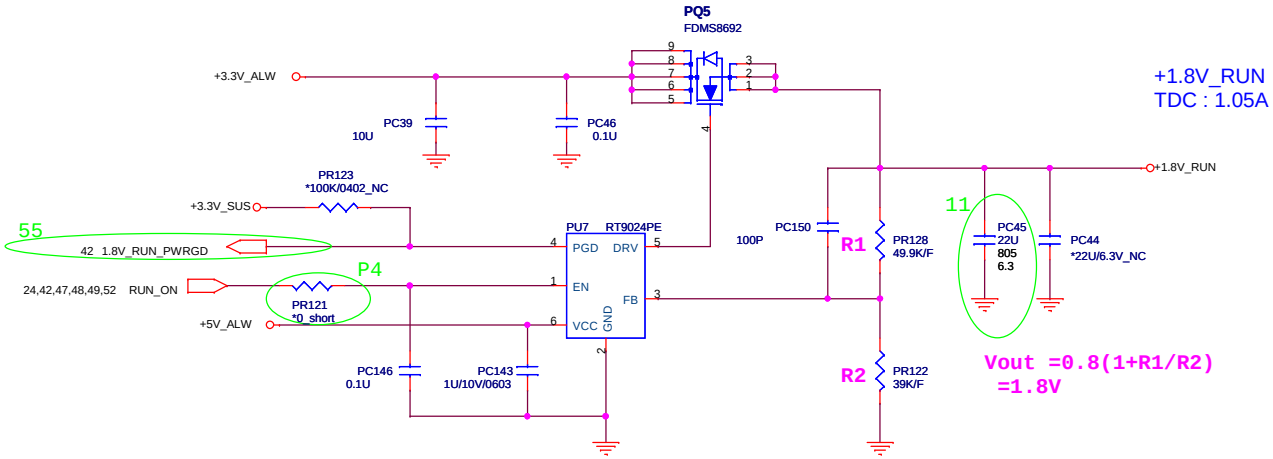


QUANTA COMPUTER

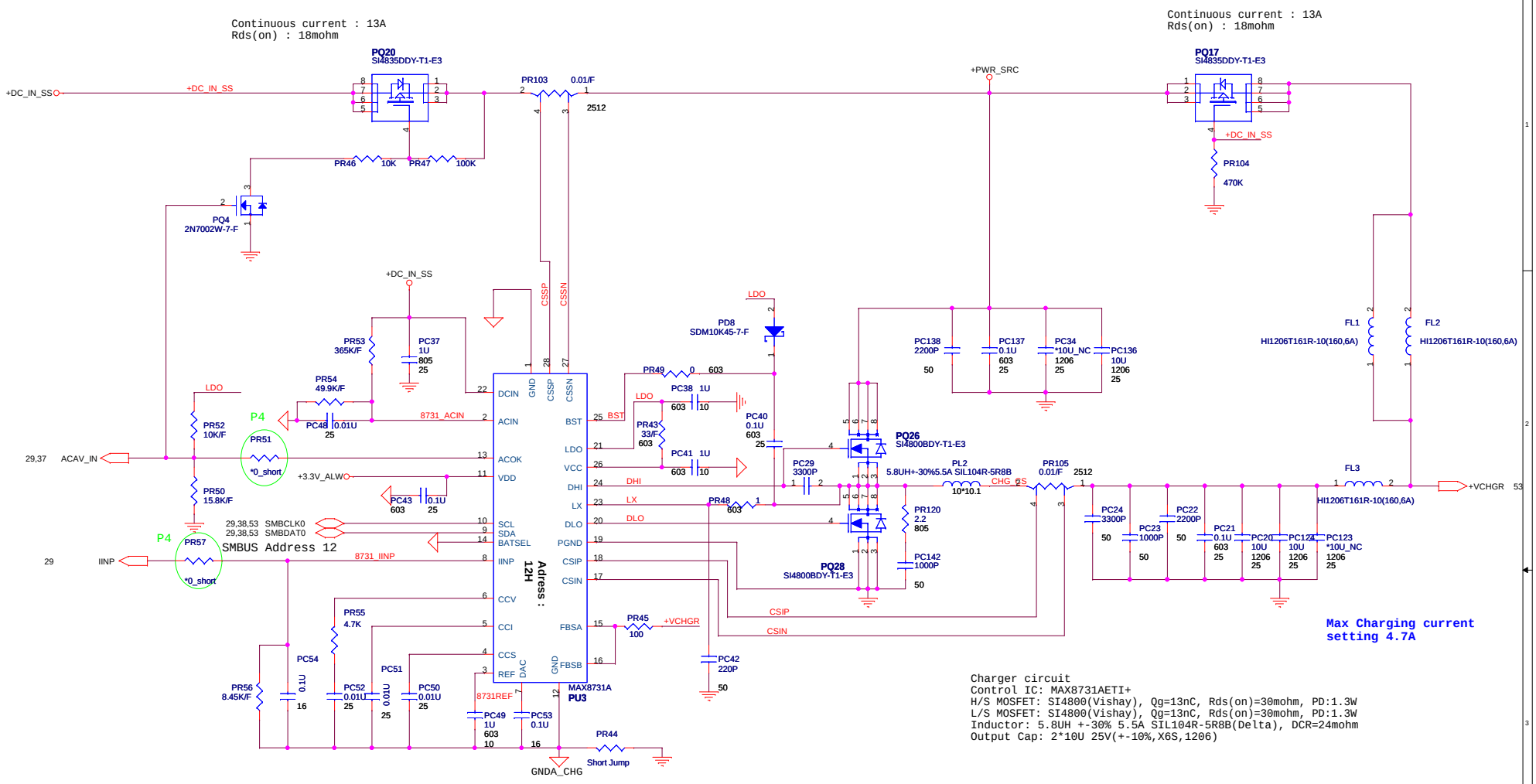
Title	System Reset Circuit	
Size	Document Number FM9B	Rev 3A
Date: Thursday, October 01, 2009	Sheet 42 of 65	

QUANTA COMPUTER

Title	Battery Selector	
Size	Document Number FM9B	Rev 3A
Date: Thursday, October 01, 2009	Sheet 43 of 65	



Title	+1.8V_RUN(RT9024)	
Size	Document Number FM9B	Rev 2B
Date: Thursday, October 01, 2009	Sheet 44 of 65	



QUANTA COMPUTER

Title	Charger (MAX8731)	
Size	Document Number FM9B	Rev 2B
Date: Thursday, October 01, 2009	Sheet 45 of 65	

+3.3V_ALW
Control IC: TPS51427A
H/S MOSFET: FDS6298(Fairchild), Qg=14nC, Rds(on)=12mohm, PD:3W
L/S MOSFET: FDS6676AS(Fairchild), Qg=35nC, Rds(on)=7.25mohm, PD:2.5W
Inductor: 1.5U20%17.1A(FDVE1040-H-1R5M=P3)(TOKO), DCR=4.6mohm
Output Cap: 1*150U 6.3V(20%,ESR15,7343,H=1.9),ripple current 2700mA

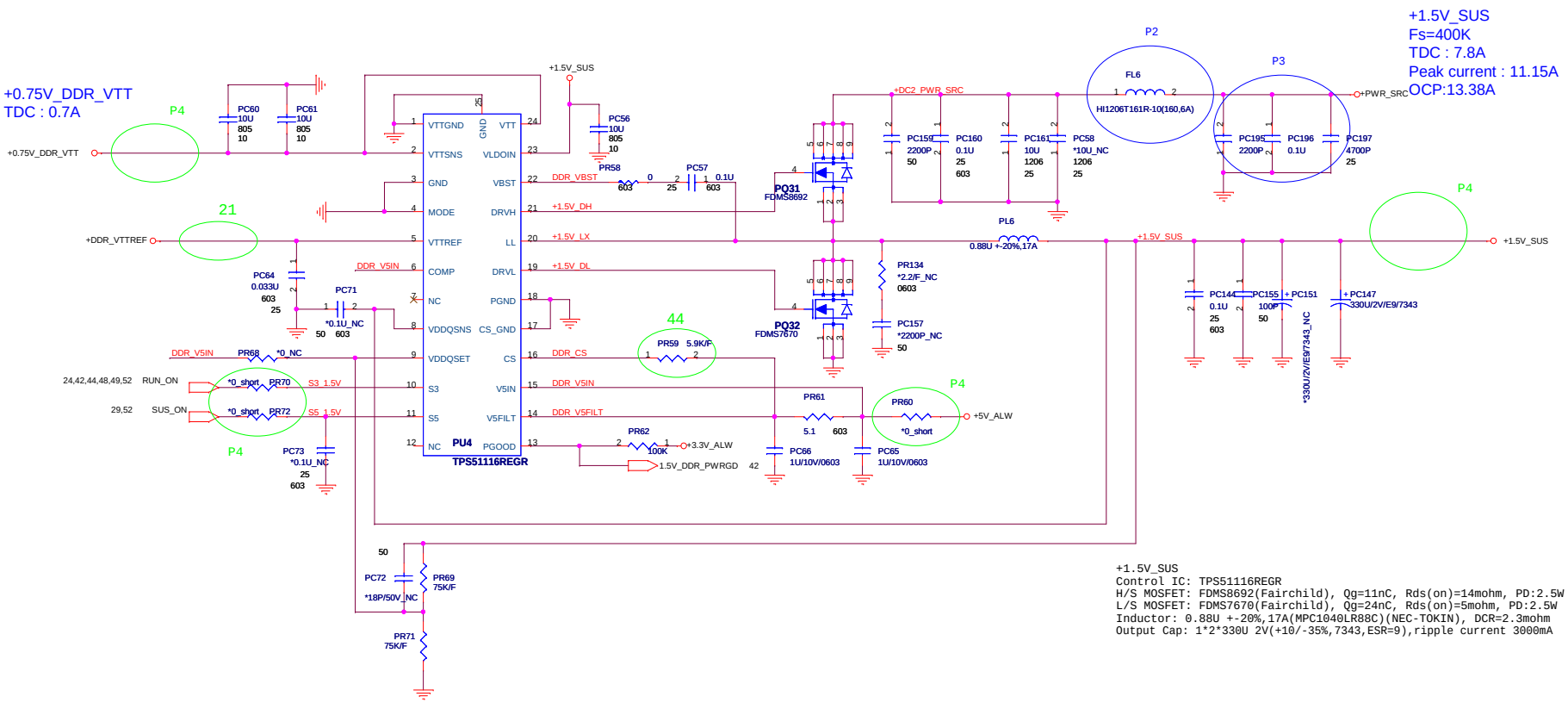
+5V_ALW
Fs=400K
TDC : 5.83A
Peak current : 8.33A
OCP:10A

+3.3V_ALW
Fs=300K
TDC : 8.23A
Peak : 11.77A
OCP:14A

+5V_ALW
Control IC: TPS51427A
H/S MOSFET: FDS8884(Fairchild), Qg=7nC, Rds(on)=30mohm, PD:2.5W
L/S MOSFET: FDS6690AS(Fairchild), Qg=13nC, Rds(on)=15mohm, PD:2.5W
Inductor: 3.3UH +-20% 12.3A FDVE1040-H-3R3M=P3(TOKO), DCR=10.1mohm
Output Cap: 1*150U 6.3V(20%,ESR15,7343,H=1.9),ripple current 2700mA

Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	400 kHz	200 kHz
Channel2 Fs	500 kHz	300 kHz	300 kHz

QUANTA COMPUTER			
Title: 3.3V_ALW / 5V_ALW(TPS51427A)			
Size	Document Number: FM9B		Rev: 2B
Date: Monday, October 05, 2009	Sheet 46 of 65		



+1.5V_SUS
Control IC: TPS51116REGR
H/S MOSFET: FDMS8692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS7670(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 0.88U +-20%,17A(MPC1040LR88C)(NEC-TOKIN), DCR=2.3mohm
Output Cap: 1*2*330U 2V(+10/-35%,7343,ESR=9),ripple current 3000mA

VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

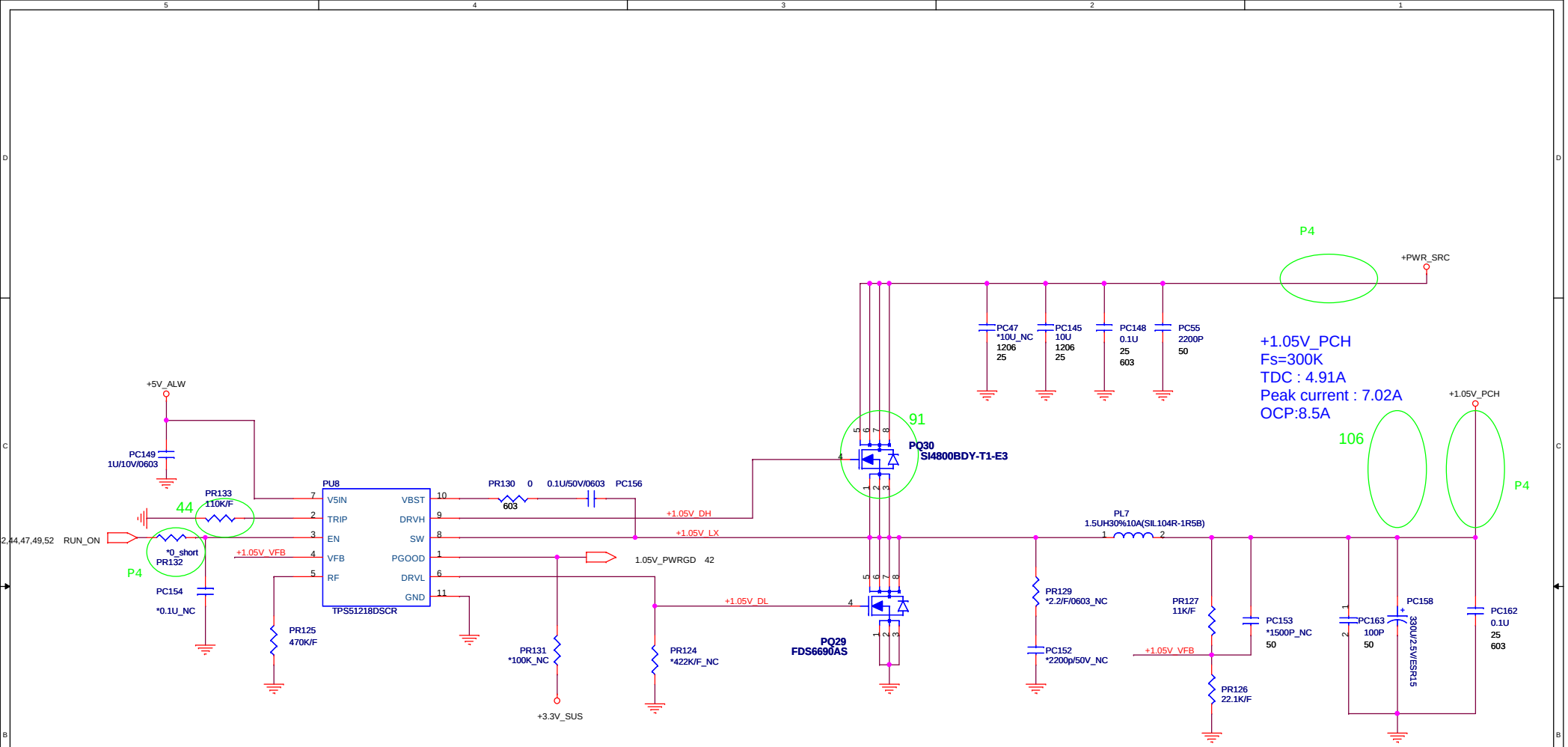
VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	2.5V	VDDQSNS/2	DDR
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

Title	DDR3 +1.5V_SUS(TPS51116)		
Size	Document Number FM9B		Rev 2B
Date:	Thursday, October 01, 2009	Sheet 47 of 65	

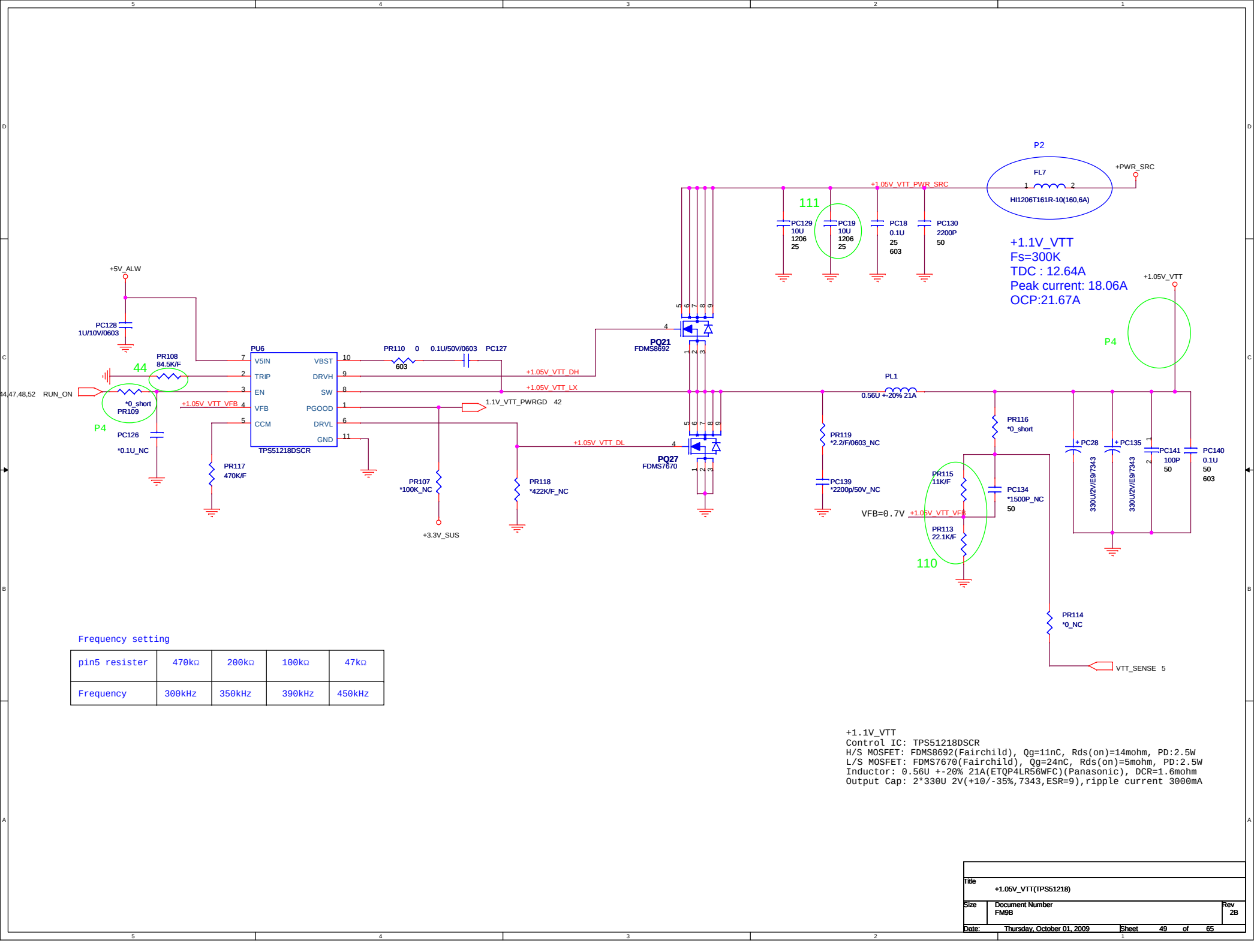


Frequency setting

pin5 resister	470kΩ	200kΩ	100kΩ	47kΩ
Frequency	300kHz	350kHz	390kHz	450kHz

+1.05V_PCH
Control IC: TPS51218DSCR
H/S MOSFET: FDS8884(Fairchild), Qg=7nC, Rds(on)=30mohm, PD:2.5W
L/S MOSFET: FDS6690AS(Fairchild), Qg=13nC, Rds(on)=15mohm, PD:2.5W
Inductor: 1.5UH +-30% 10A SIL104R-1R5B(Delta), DCR=8.1mohm
Output Cap: 1*330U 2.5V(20%,ESR15,7343,H1.9),ripple current 2700mA

Title	+1.05V_PCH(TPS51218)		
Size	Document Number FM9B		Rev 2B
Date:	Thursday, October 01, 2009	Sheet 48 of 65	

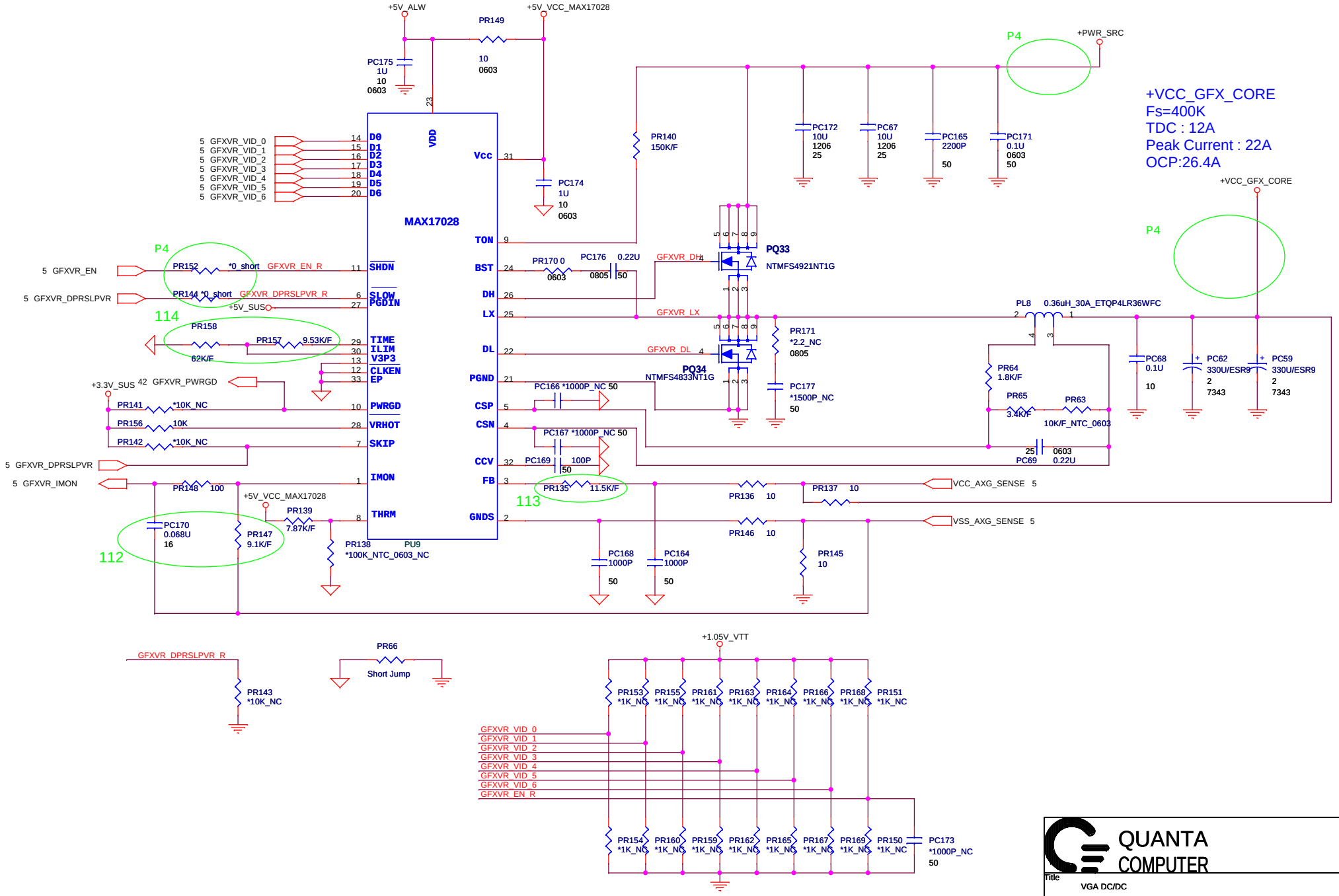


Frequency setting

pin5 resister	470kΩ	200kΩ	100kΩ	47kΩ
Frequency	300kHz	350kHz	390kHz	450kHz

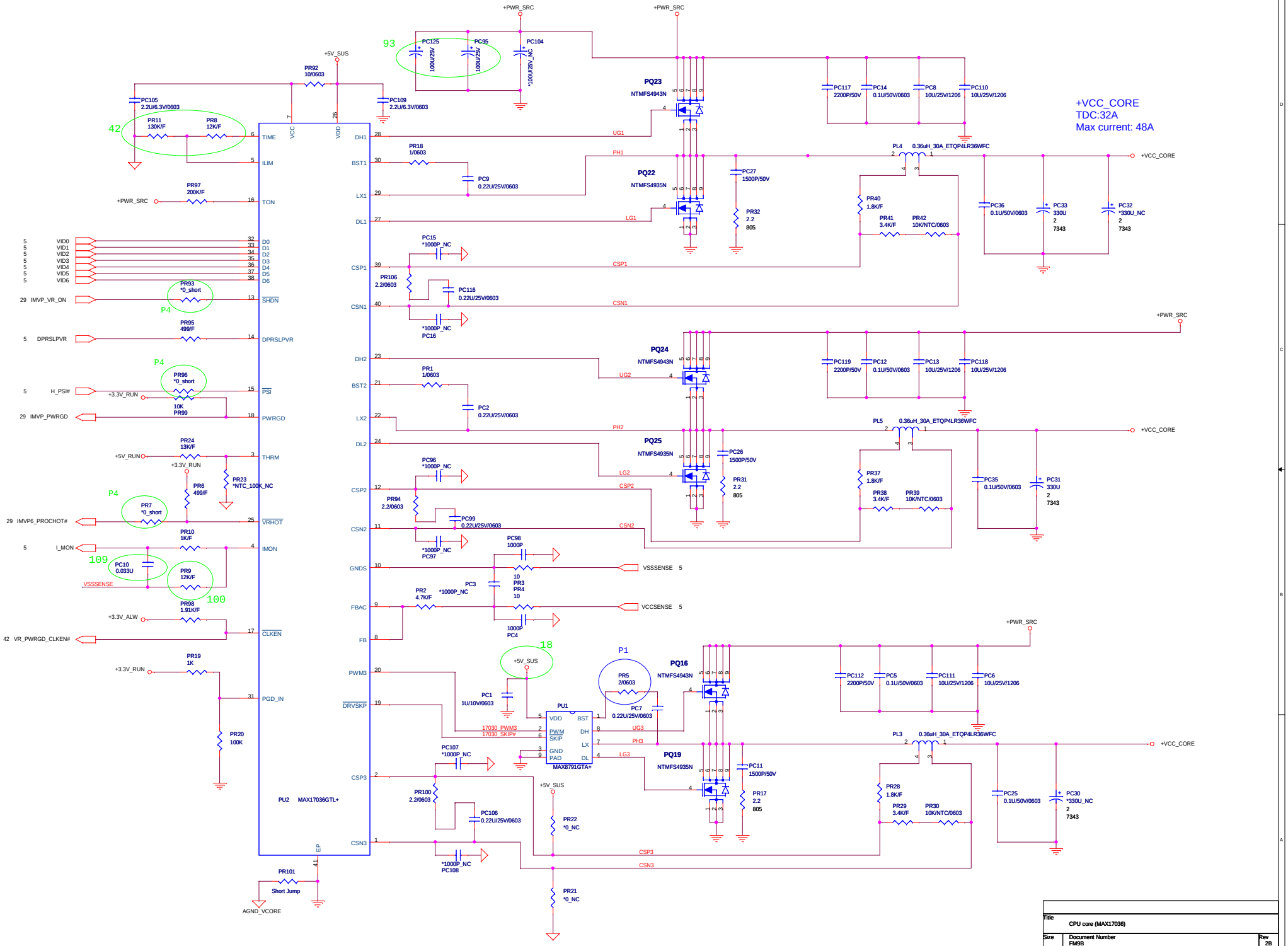
+1.1V_VTT
Control IC: TPS51218DSCR
H/S MOSFET: FDMS8692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS7670(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 0.56U +-20% 21A(ETQP4LR56WFC)(Panasonic), DCR=1.6mohm
Output Cap: 2*330U 2V(+10/-35%,7343,ESR=9),ripple current 3000mA

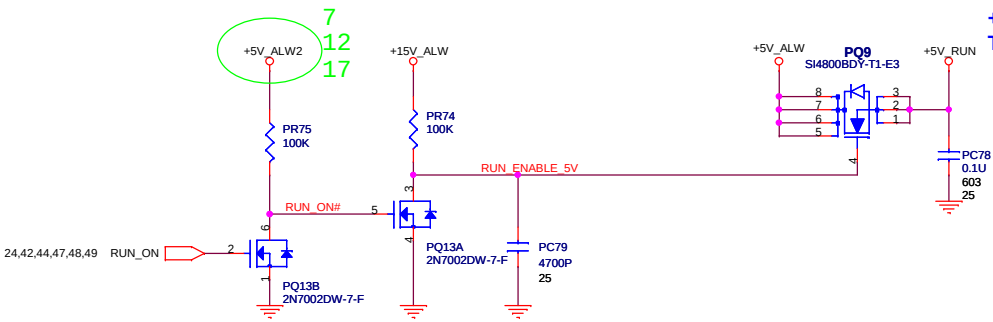
Title	+1.05V_VTT(TPS51218)	
Size	Document Number FM9B	Rev 2B
Date: Thursday, October 01, 2009	Sheet 49 of 65	

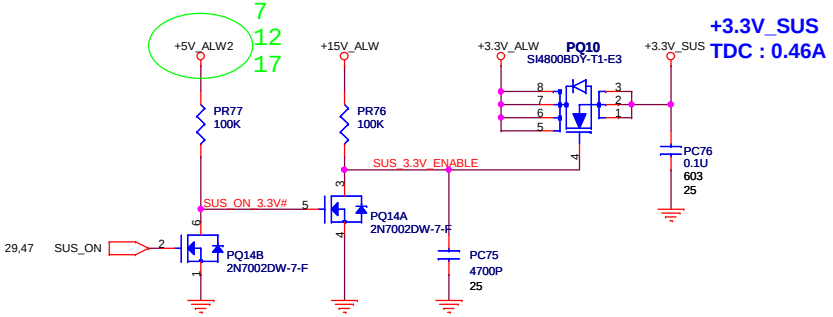


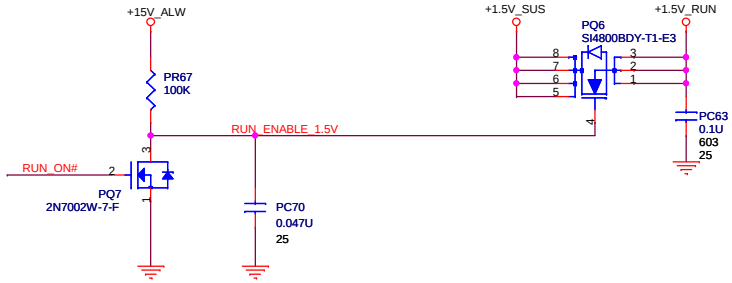
QUANTA COMPUTER

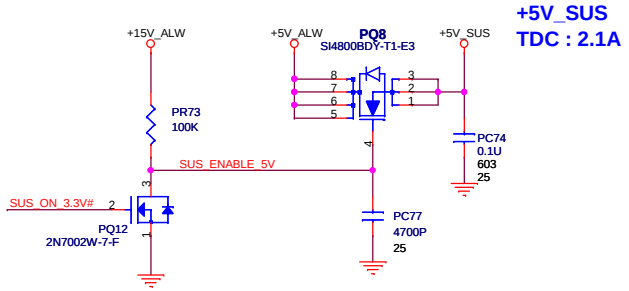
Title	VGA DC/DC	
Size	Document Number FM9B	Rev 2B
Date: Monday, October 05, 2009	Sheet 50 of 65	

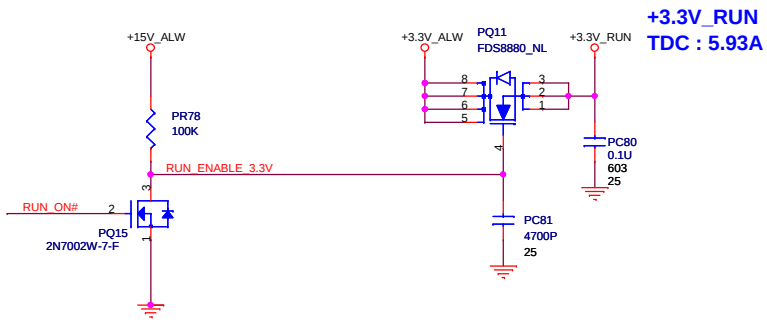

+VCC_CORE
TDC:32A
Max current: 48A
PU2 MAX17036GTL+
PU1 MAX8791GTA+
PQ23 NTMFS4943N
PQ22 NTMFS4935N
PQ24 NTMFS4943N
PQ25 NTMFS4935N
PQ16 NTMFS4943N
PQ19 NTMFS4935N
PL4 0.36uH_30A_ETQP4LR36WFC
PL5 0.36uH_30A_ETQP4LR36WFC
PL3 0.36uH_30A_ETQP4LR36WFC
+PWR_SRC
+5V_SUS
+3.3V_RUN
+3.3V_ALW
+VCC_CORE
AGND_VCORE
VSSSENSE
VCCSENSE
Short Jump
Title
CPU core (MAX17036)
Size
Document Number
FM9B
Rev
2B
Date: Friday, October 02, 2009
Sheet 51 of 65



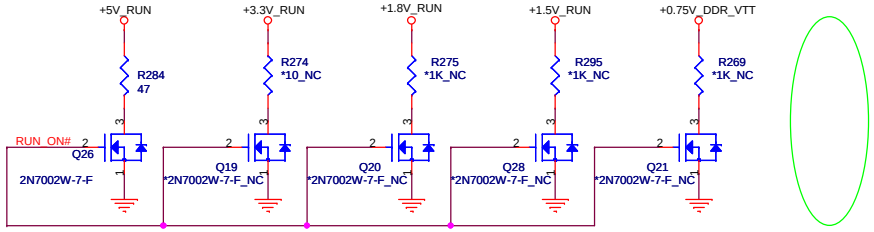


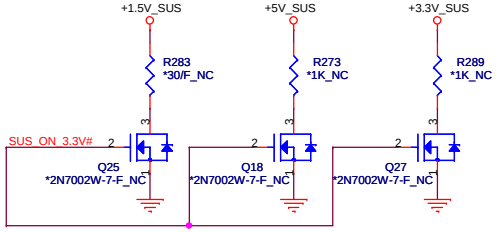






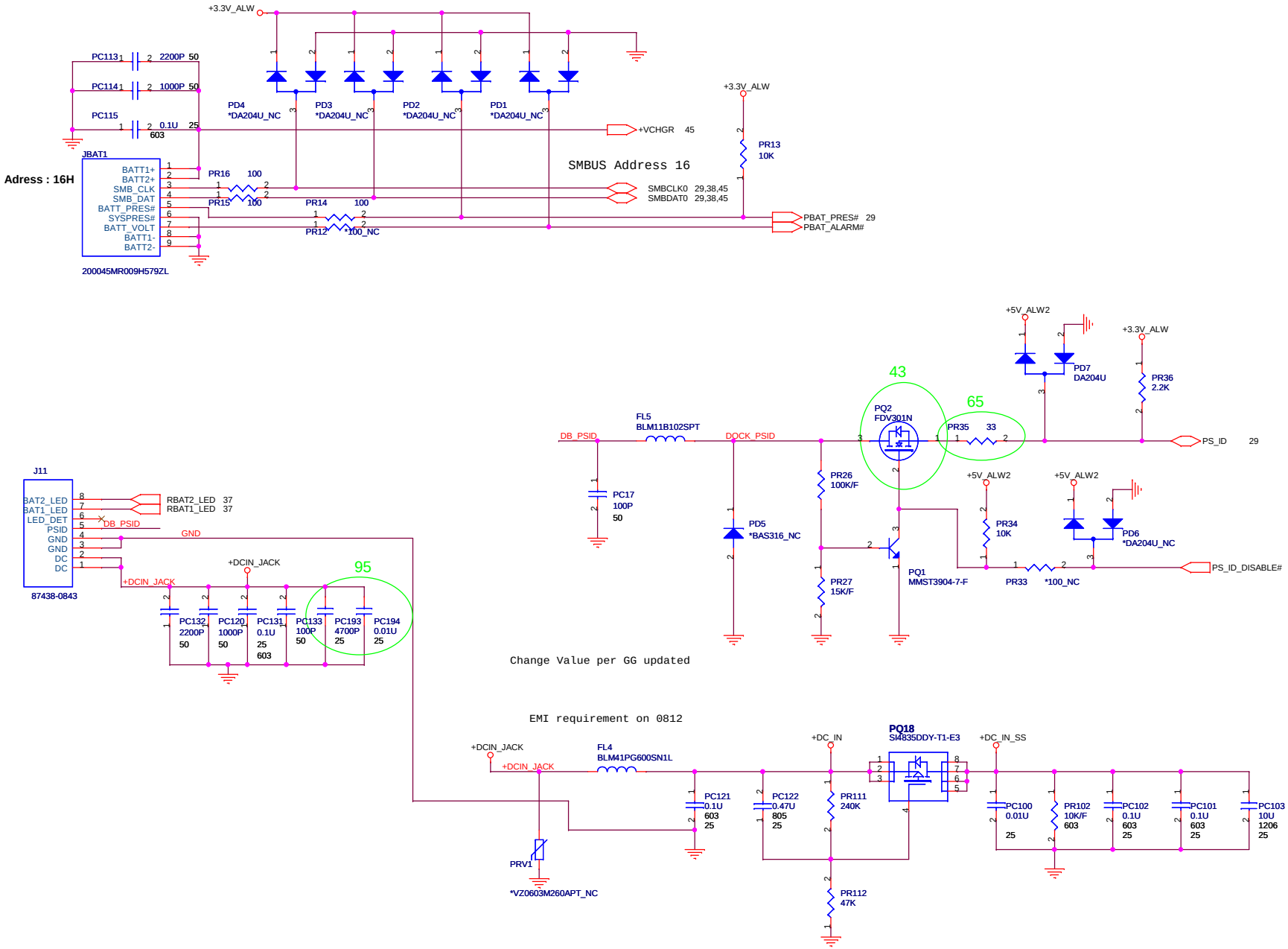
Reserve discharge path





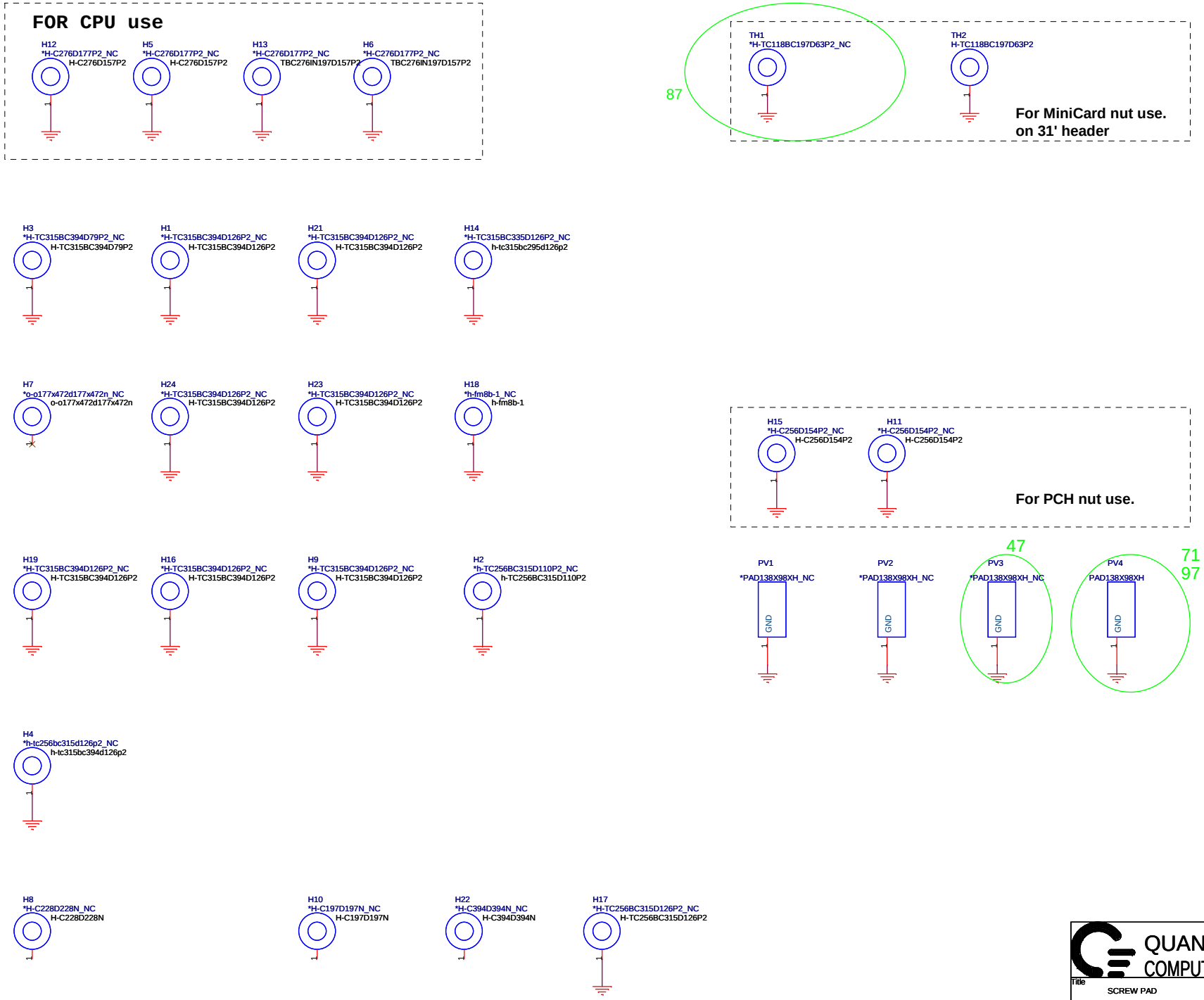
QUANTA COMPUTER

Title	RUN / SUS POWER SW	
Size	Document Number FM9B	Rev 3A
Date: Thursday, October 01, 2009	Sheet 52 of 65	



QUANTA COMPUTER

Title	DCIN,BATT CONNECTOR	
Size	Document Number FM9B	Rev 3A
Date: Thursday, October 01, 2009	Sheet 53 of 65	


FOR CPU use
H12
*H-C276D177P2_NC
H-C276D157P2
H5
*H-C276D177P2_NC
H-C276D157P2
H13
*H-C276D177P2_NC
TBC276IN197D157P2
H6
*H-C276D177P2_NC
TBC276IN197D157P2
87
TH1
*H-TC118BC197D63P2_NC
TH2
H-TC118BC197D63P2
For MiniCard nut use.
on 31' header
H3
*H-TC315BC394D79P2_NC
H-TC315BC394D79P2
H1
*H-TC315BC394D126P2_NC
H-TC315BC394D126P2
H21
*H-TC315BC394D126P2_NC
H-TC315BC394D126P2
H14
*H-TC315BC335D126P2_NC
h-tc315bc295d126p2
H7
*o-o177x472d177x472n_NC
o-o177x472d177x472n
H24
*H-TC315BC394D126P2_NC
H-TC315BC394D126P2
H23
*H-TC315BC394D126P2_NC
H-TC315BC394D126P2
H18
*h-fm8b-1_NC
h-fm8b-1
H15
*H-C256D154P2_NC
H-C256D154P2
H11
*H-C256D154P2_NC
H-C256D154P2
For PCH nut use.
47
71
97
PV1
*PAD138X98XH_NC
PV2
*PAD138X98XH_NC
PV3
*PAD138X98XH_NC
PV4
PAD138X98XH
GND
H19
*H-TC315BC394D126P2_NC
H-TC315BC394D126P2
H16
*H-TC315BC394D126P2_NC
H-TC315BC394D126P2
H9
*H-TC315BC394D126P2_NC
H-TC315BC394D126P2
H2
*h-TC256BC315D110P2_NC
h-TC256BC315D110P2
H4
*h-tc256bc315d126p2_NC
h-tc315bc394d126p2
H8
*H-C228D228N_NC
H-C228D228N
H10
*H-C197D197N_NC
H-C197D197N
H22
*H-C394D394N_NC
H-C394D394N
H17
*H-TC256BC315D126P2_NC
H-TC256BC315D126P2
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Reserved for EMI.

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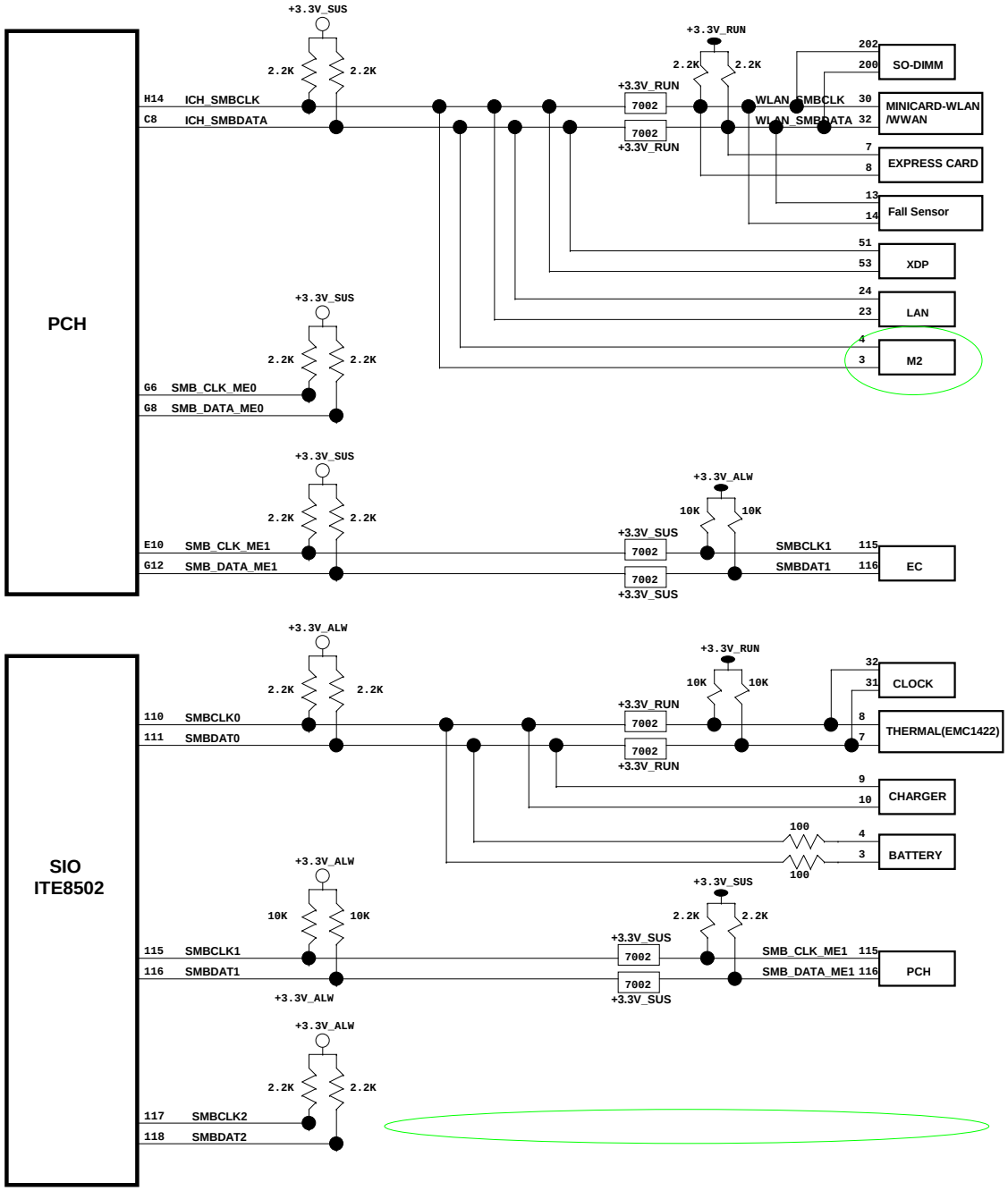

QUANTA COMPUTER			
Title: SMBUS BLOCK			
Size:	Document Number: FM05		Rev: 3A
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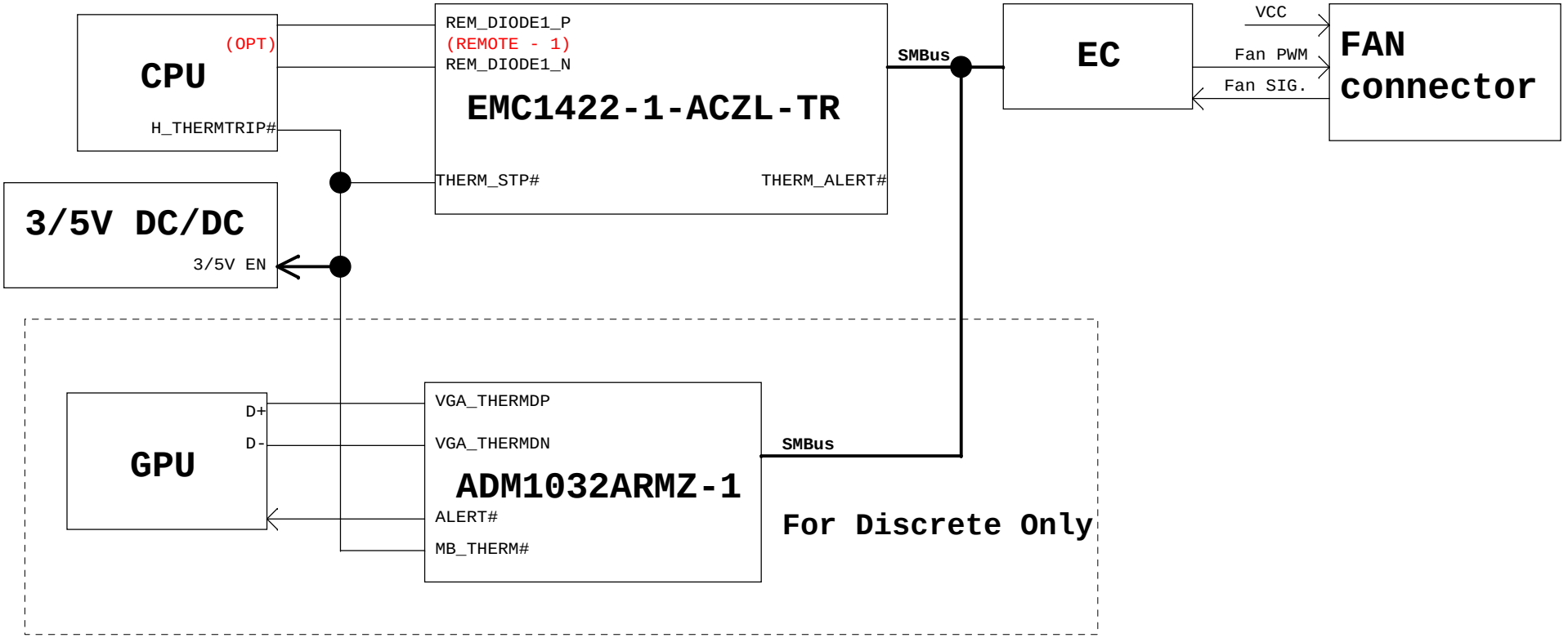

QUANTA COMPUTER

Title	Thermal Map	
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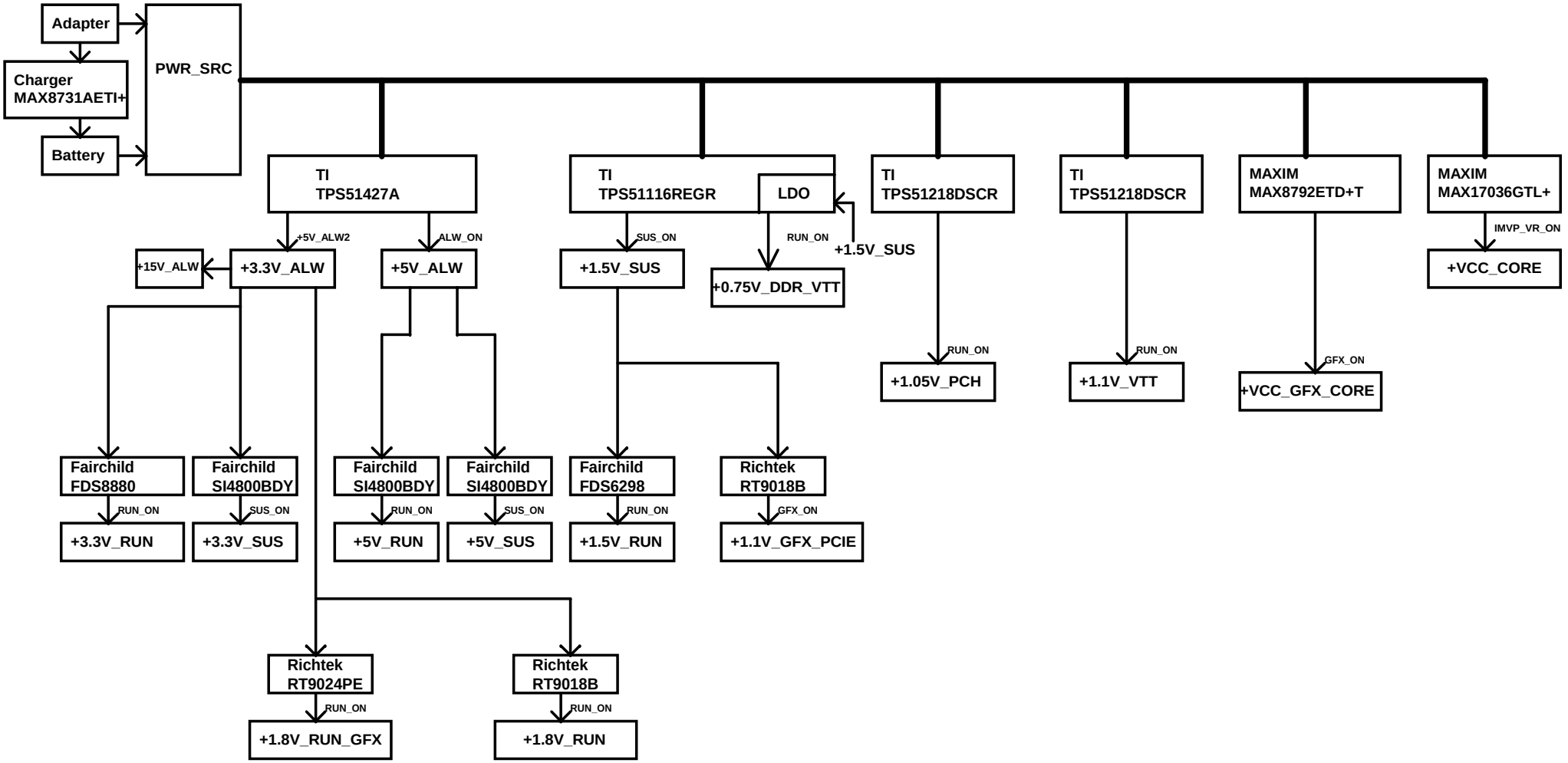
VER : 1A



QUANTA COMPUTER

Title	Schematic Block Diagram1	
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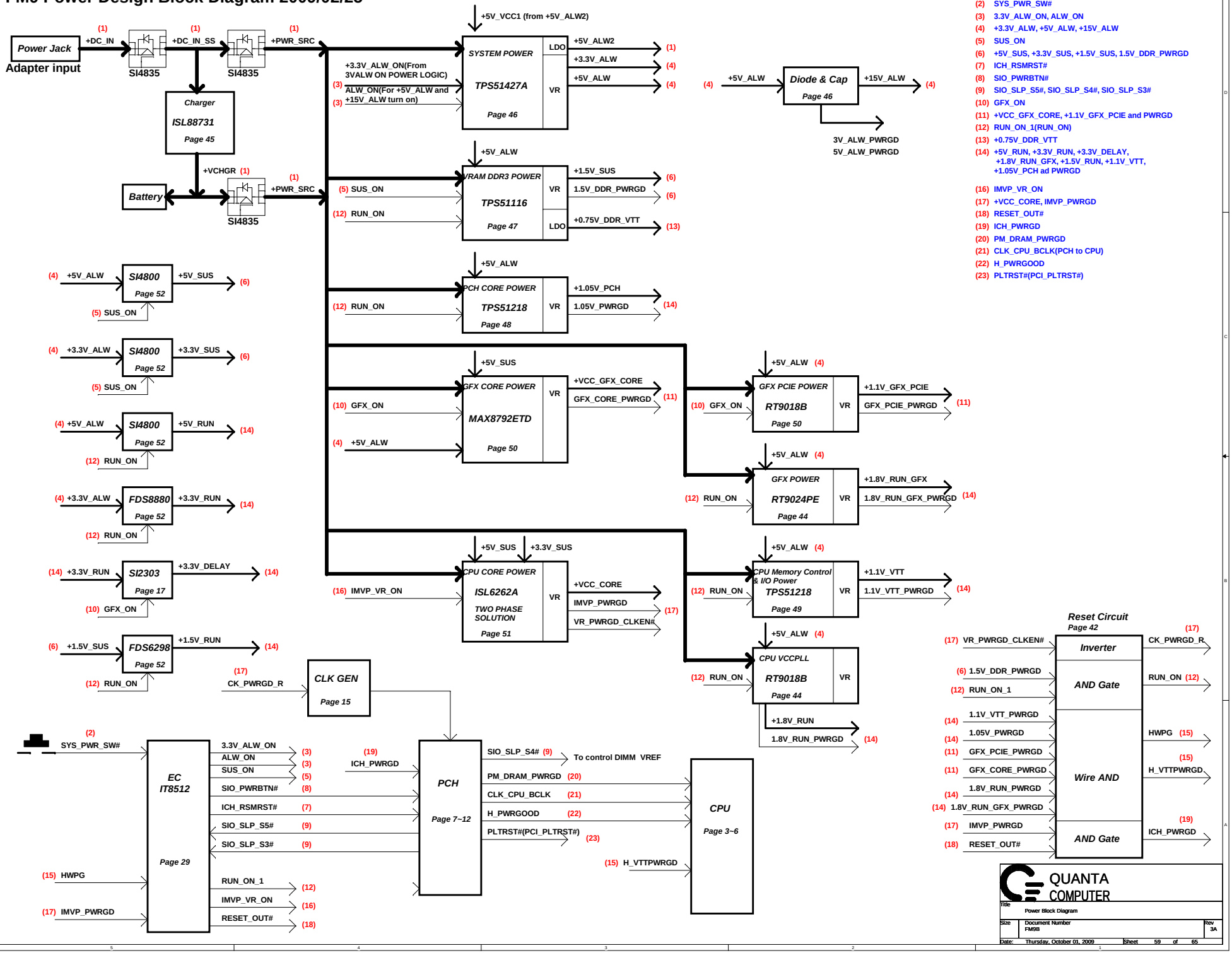
FM9 Power Design Block Diagram 2009/02/25



(1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
Bat : +VCHGR -> +PWR_SRC,+5V_ALW2,
(2) SYS_PWR_SW#
(3) 3.3V_ALW_ON, ALW_ON
(4) +3.3V_ALW, +5V_ALW, +15V_ALW
(5) SUS_ON
(6) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD
(7) ICH_RSMRST#
(8) SIO_PWRBTN#
(9) SIO_SLP_S5#, SIO_SLP_S4#, SIO_SLP_S3#
(10) GFX_ON
(11) +VCC_GFX_CORE, +1.1V_GFX_PCIE and PWRGD
(12) RUN_ON_1(RUN_ON)
(13) +0.75V_DDR_VTT
(14) +5V_RUN, +3.3V_RUN, +3.3V_DELAY, +1.8V_RUN_GFX, +1.5V_RUN, +1.1V_VTT, +1.05V_PCH ad PWRGD
(16) IMVP_VR_ON
(17) +VCC_CORE, IMVP_PWRGD
(18) RESET_OUT#
(19) ICH_PWRGD
(20) PM_DRAM_PWRGD
(21) CLK_CPU_BCLK(PCH to CPU)
(22) H_PWRGOOD
(23) PLTRST#(PCI_PLTRST#)

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Title	Power Block Diagram	
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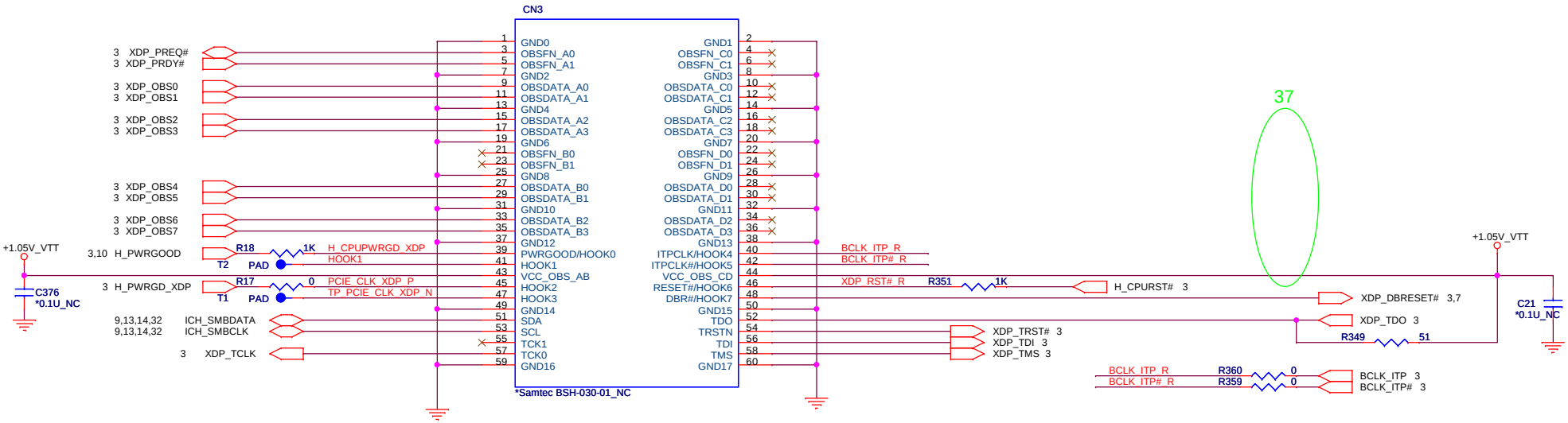

It is for debug. requesst vendeer provide 200 pcs sample.

QUANTA COMPUTER

Title	SMBUS BLOCK	
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