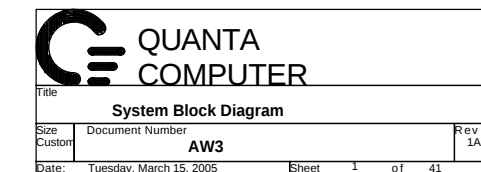


Dothan+Alviso (915PM)+ICH6-M



Voltage Rails

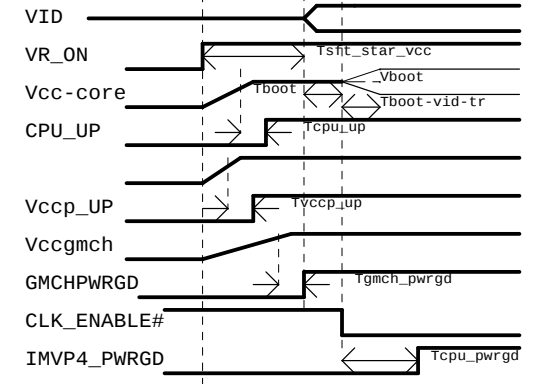
Board Stack up Description

Power On Sequencing Timing Diagram

2

PCB Layers

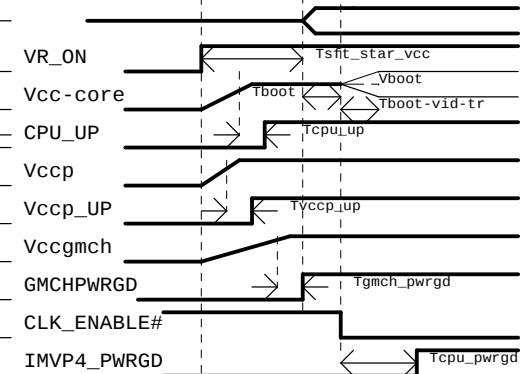
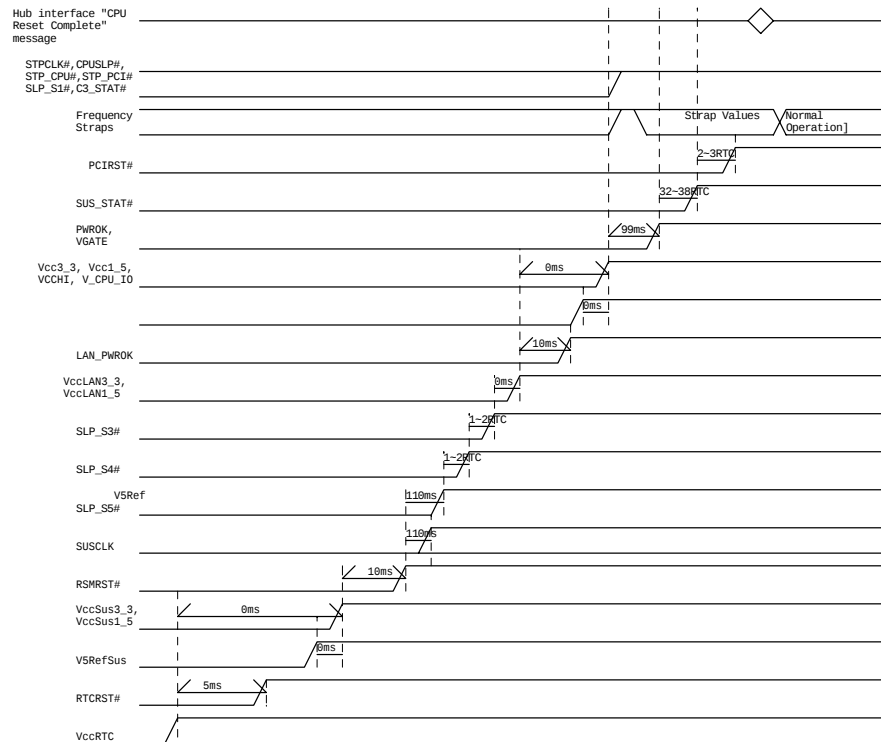
- Layer 1  TOP(FSB,DDR2,CLK,PCIE Component)
- Layer 2  Ground Plane
- Layer 3  IN1(FSB,CLOCK,DDR2,PEG,CLK)
- Layer 4  IN2(PCI,IDE,LPC)
- Layer 5  Power Plane
- Layer 6  BOTTOM, (Component,Other)



Power Sequencing and Reset Signal Timings

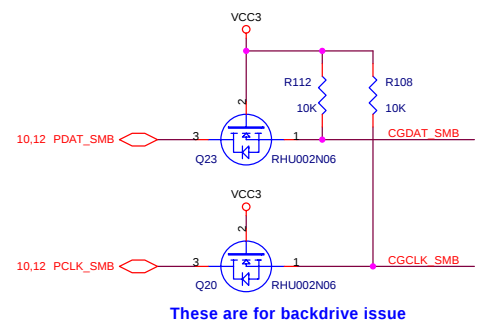
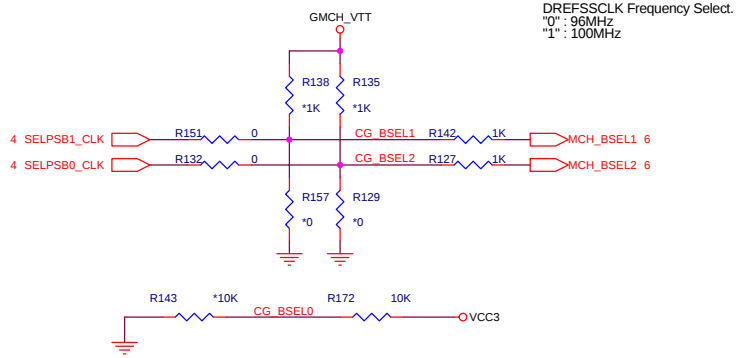
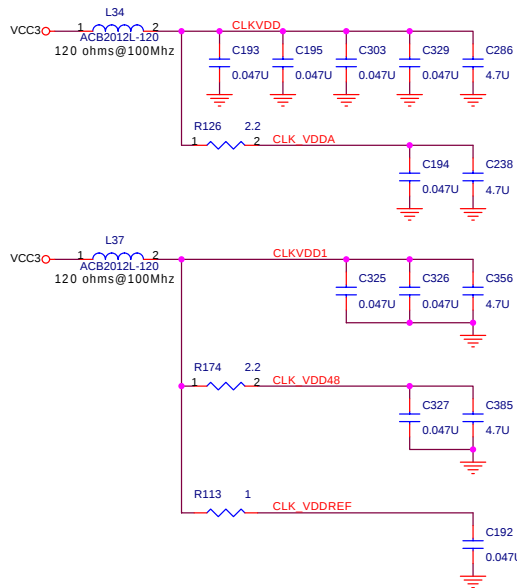
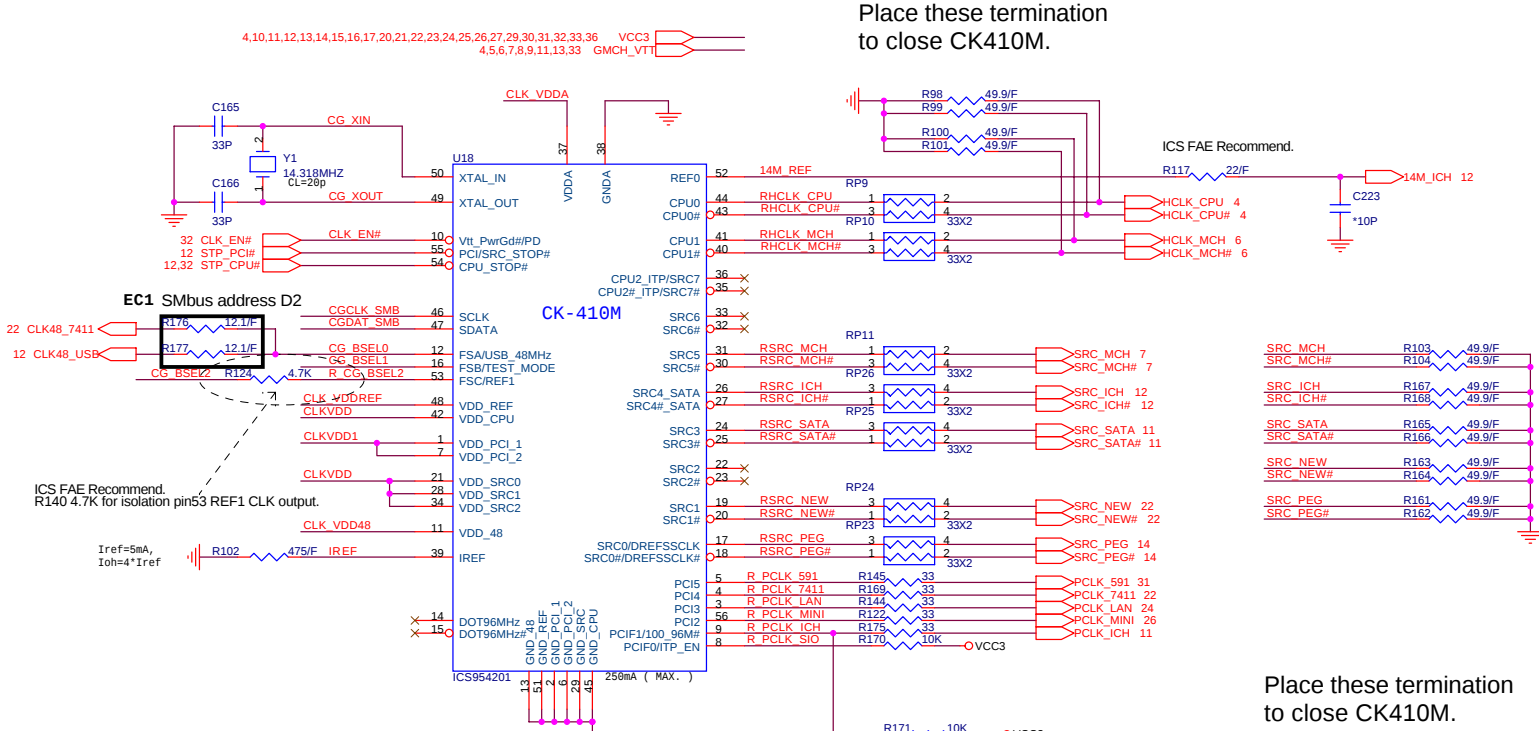
CPU Power On Sequence

ACIN POWER ON TIMING



			
QUANTA COMPUTER			
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FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33 Default
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RESERVED		



CPU Type	R132	R129	R151	R157
Dothan-A PSB400	×	×	×	✓
Dothan-A PSB533	×	✓	×	✓
Dothan-B (Default)	✓	×	✓	×
Pentium M 730-770				

QUANTA
COMPUTER

Title

System Block Diagram

Size

Custom

Document Number

AW3

Date

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Sheet

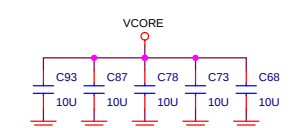
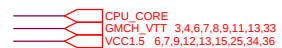
3

of

41

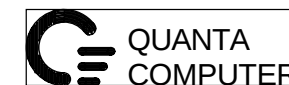
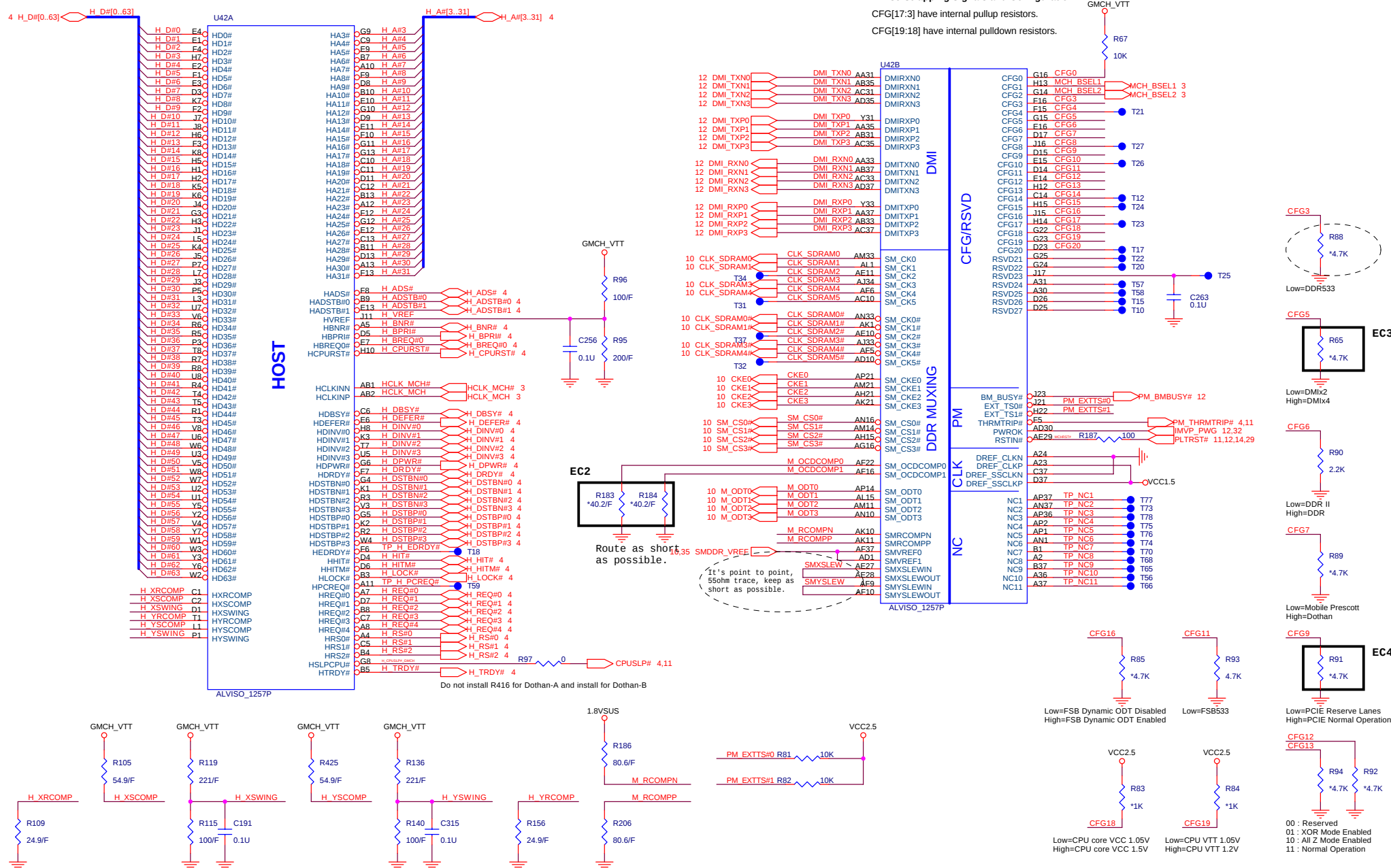
Rev

1A

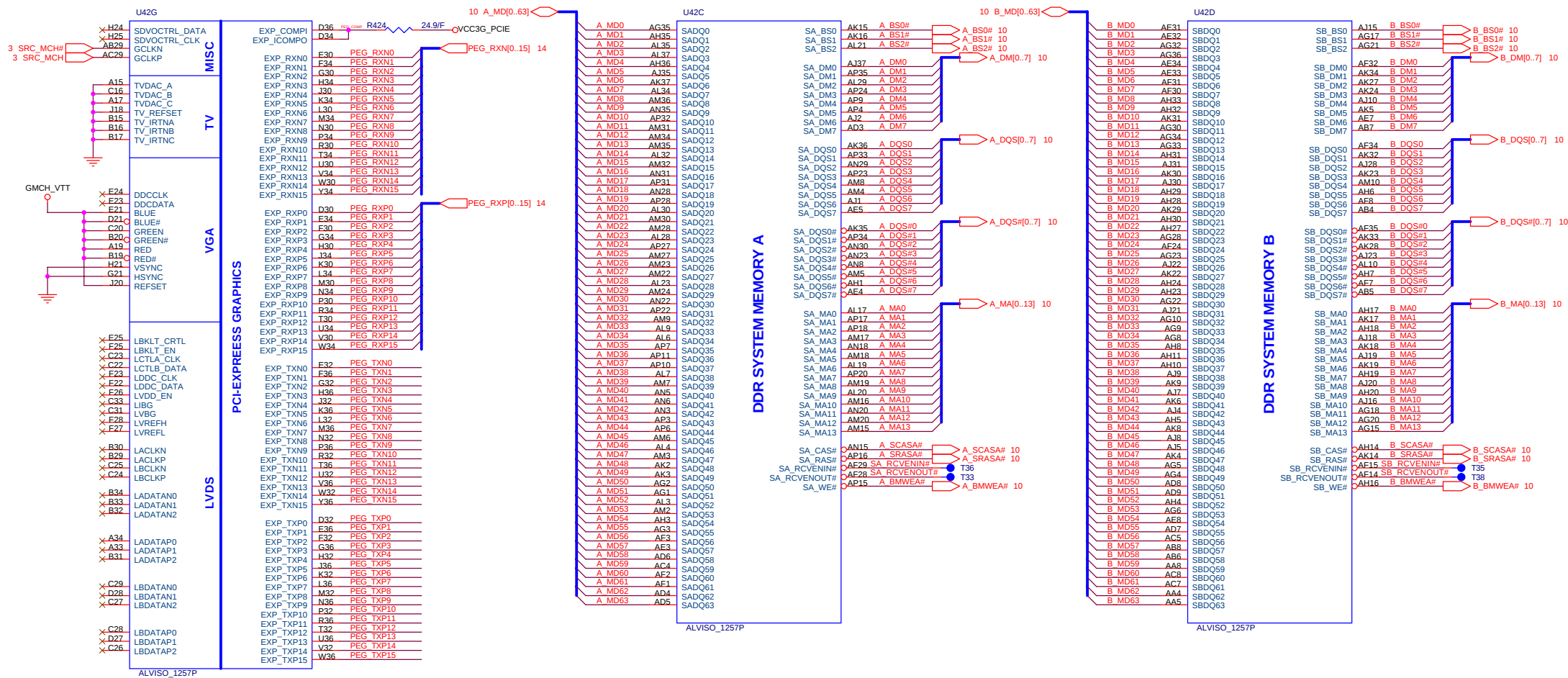


CFG[17:3] have internal pullup resistors.

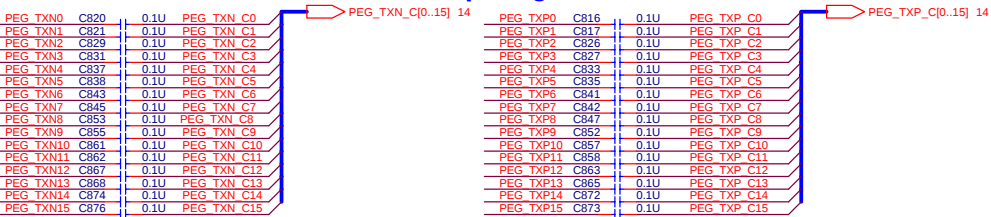
CFG[19:18] have internal pulldown resistors.

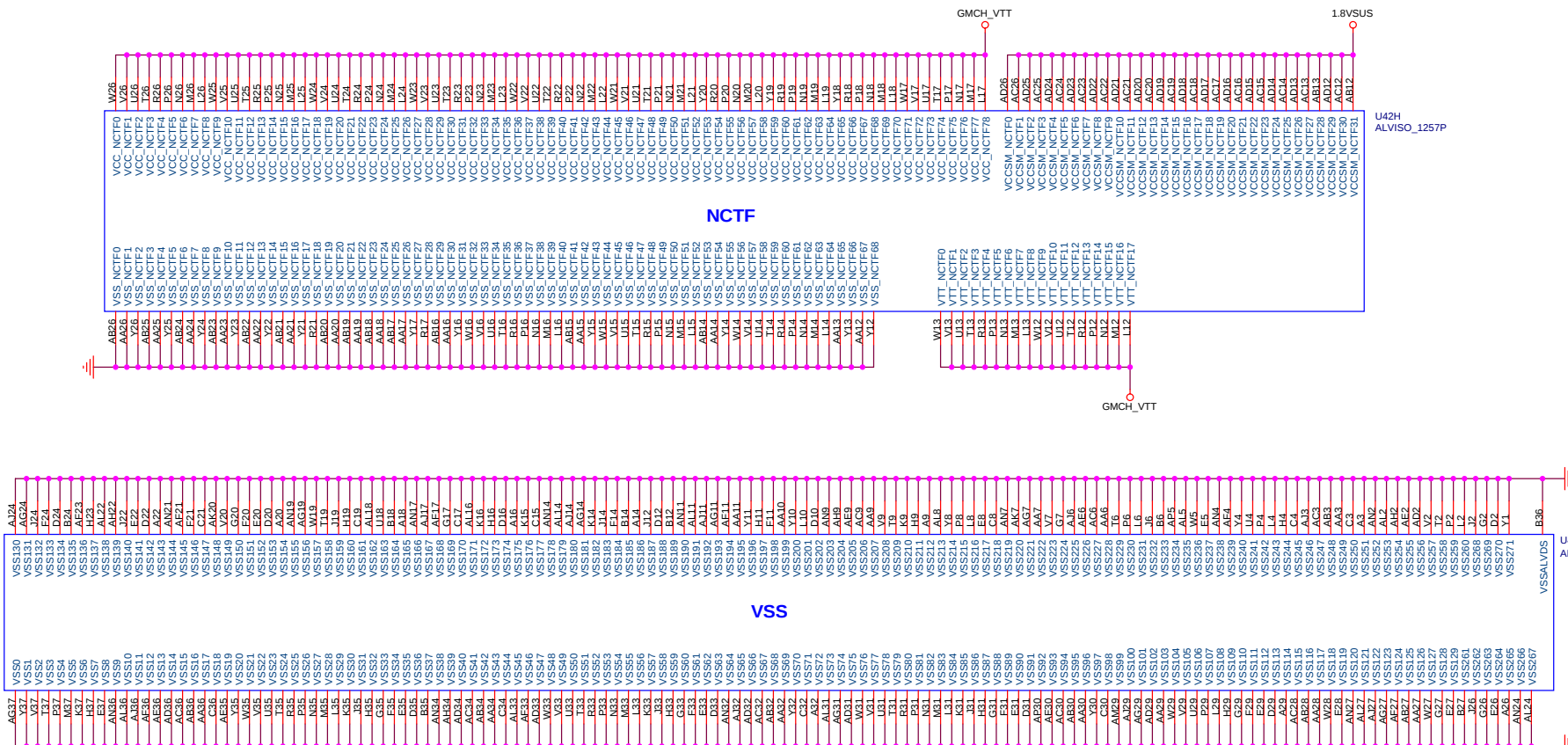


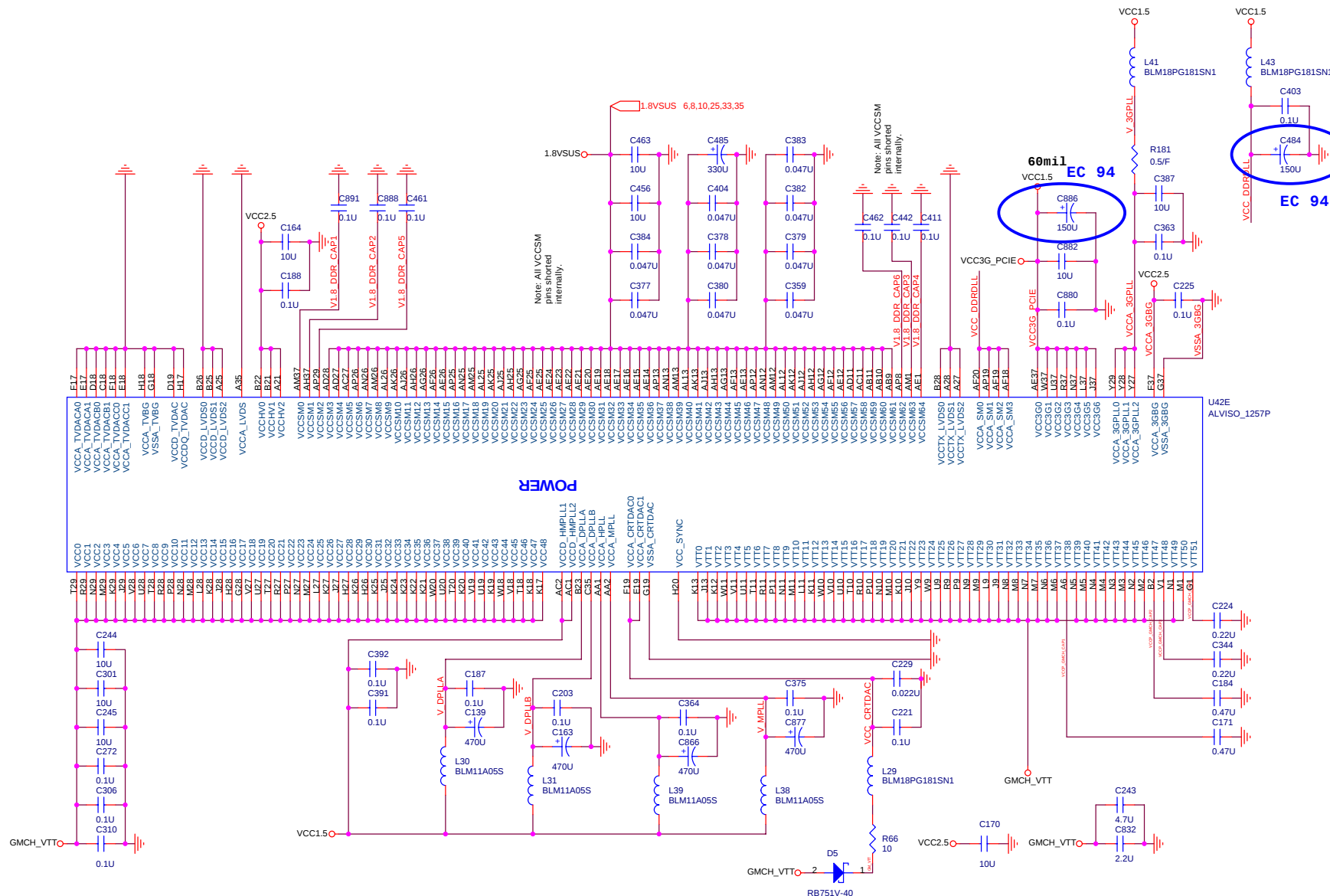
Title			
System Block Diagram			
Size Custom	Document Number AW3	Rev 1A	
Date: Tuesday, March 15, 2005	Sheet	6	of 41

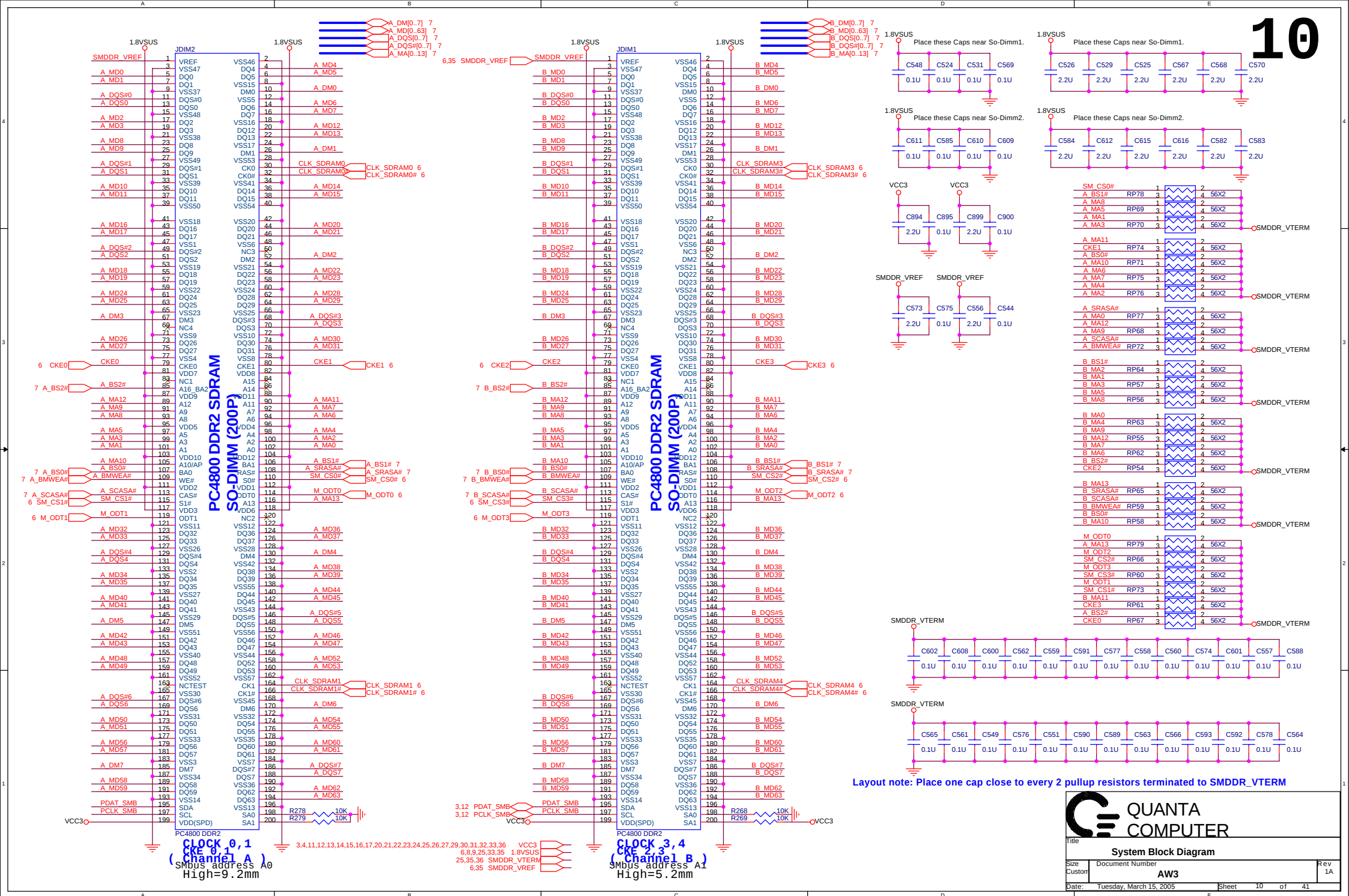


PCIE x16 AC Coupling CAP.







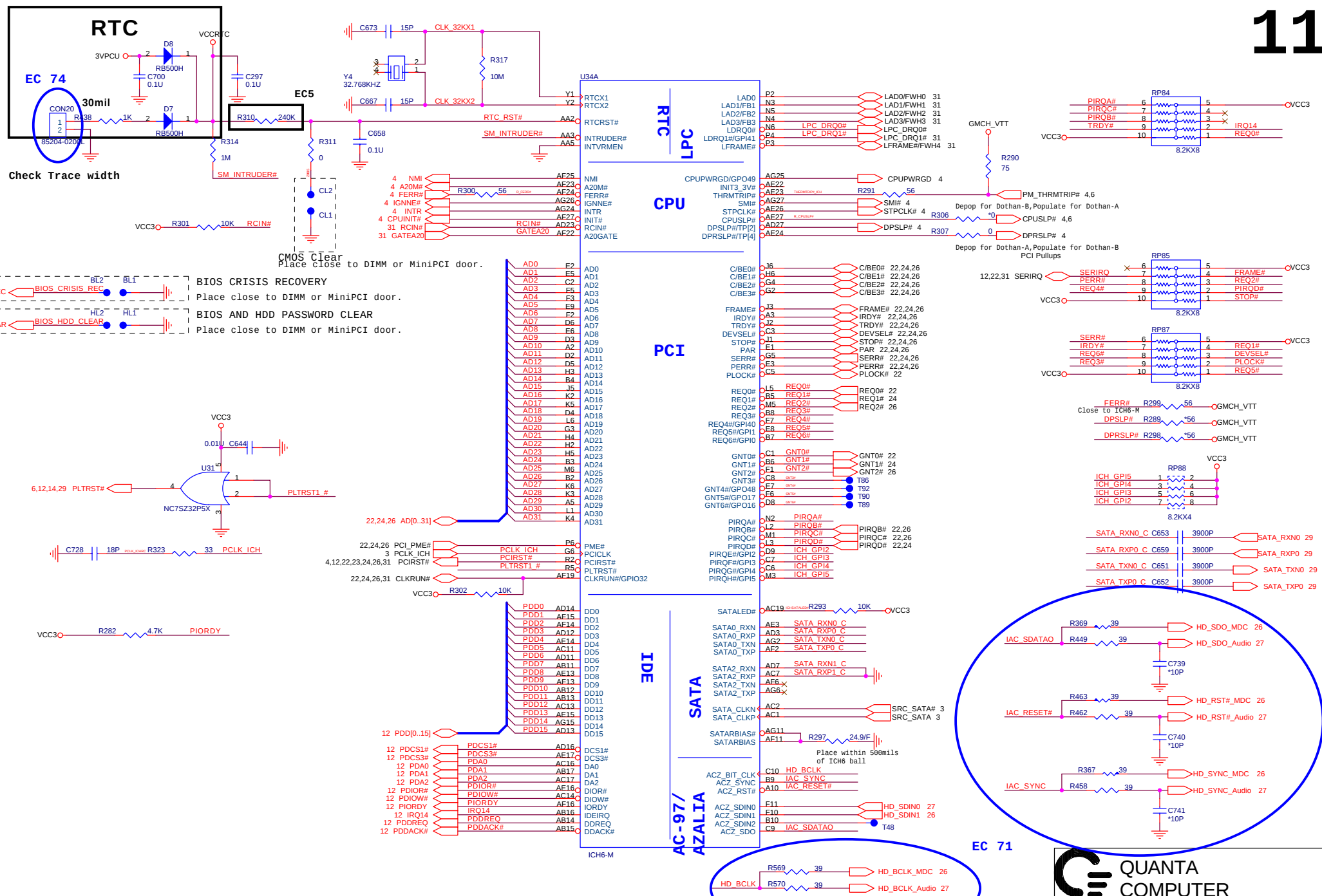


QUANTA COMPUTER

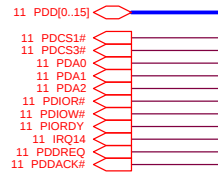
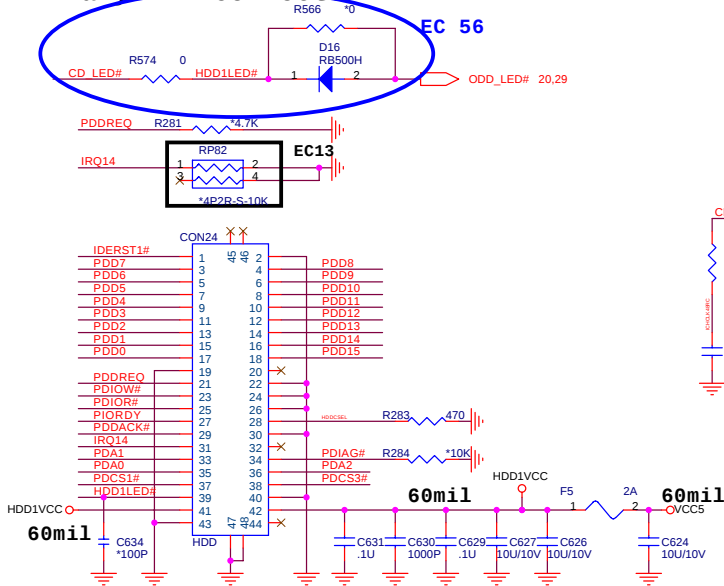
System Block Diagram

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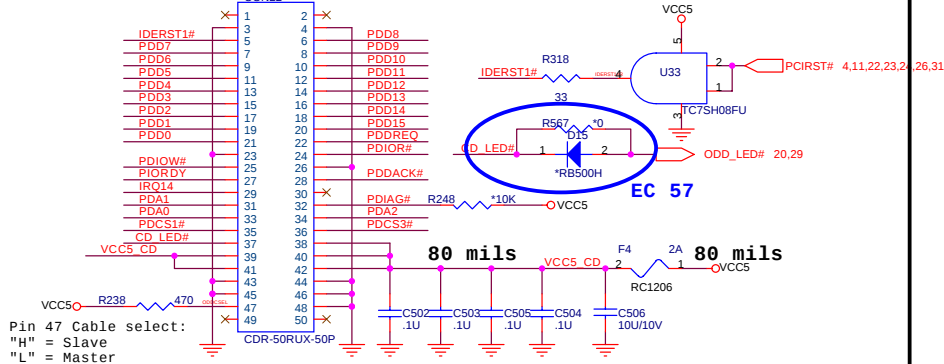
Date: Tuesday, March 15, 2005
Sheet: 10 of 41



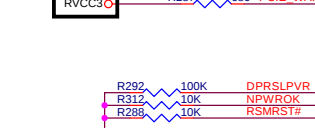
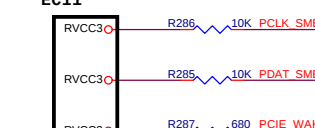
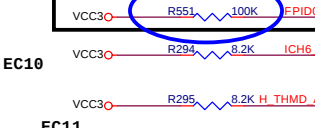
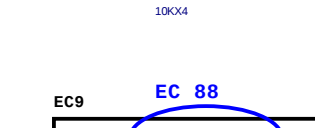
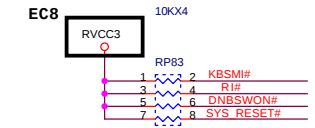
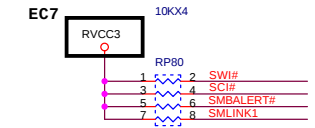
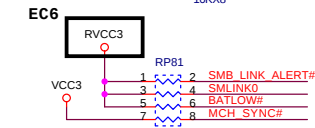
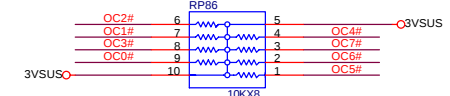
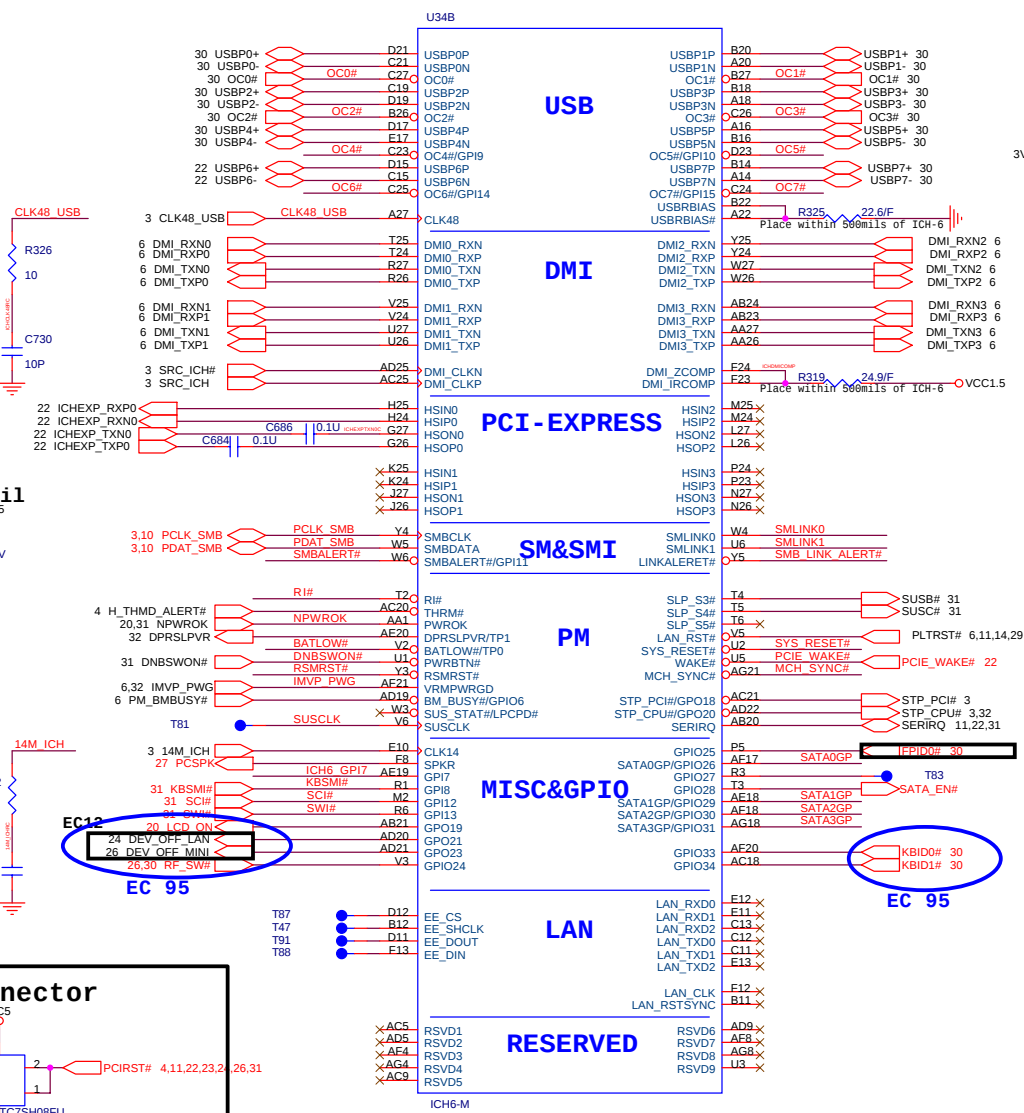
Primary HDD Connector



CD ROM Connector



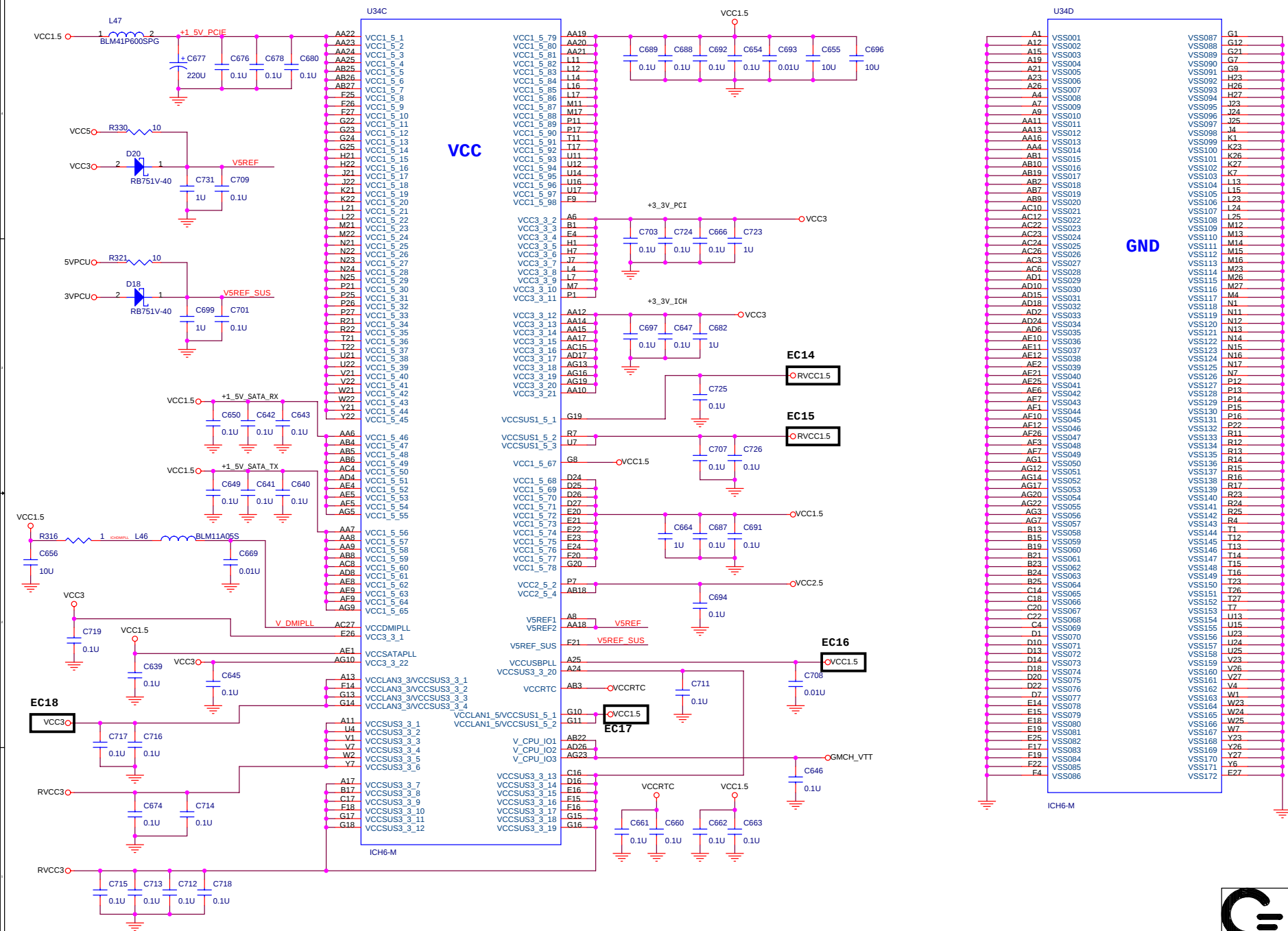
Pin 47 Cable select:
"H" = Slave
"L" = Master

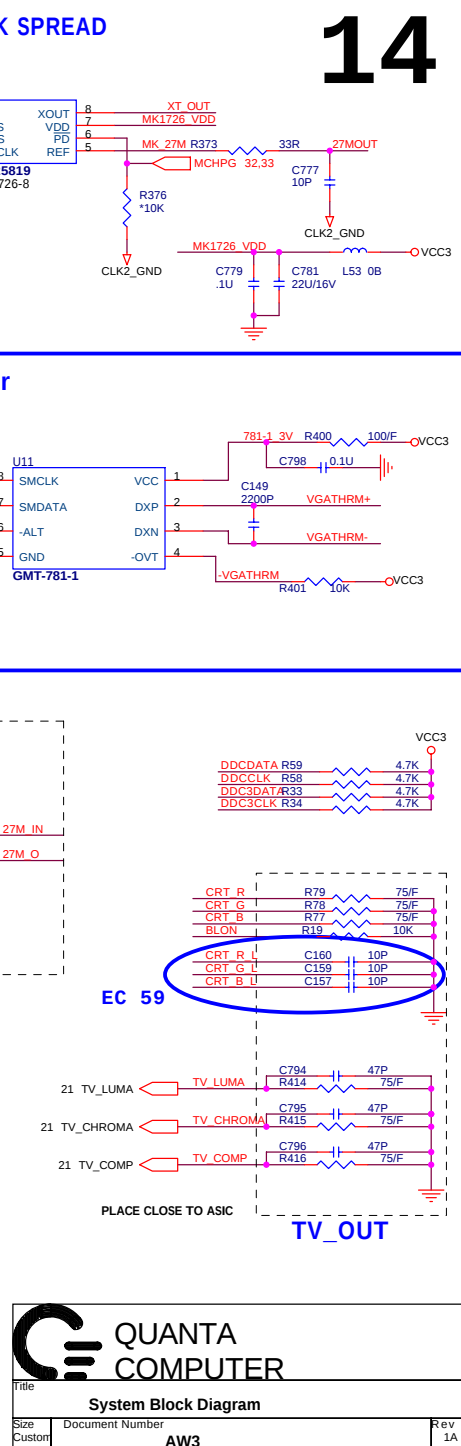
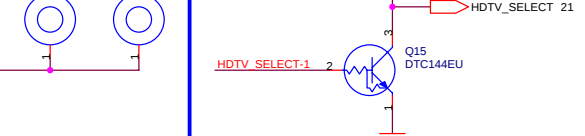
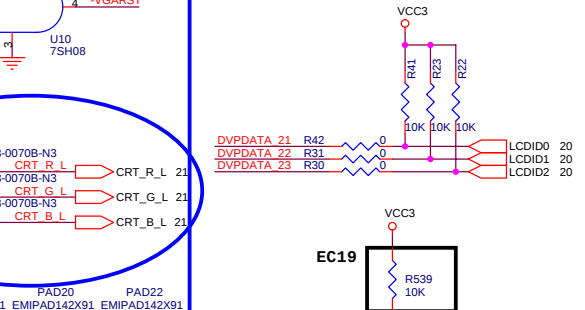
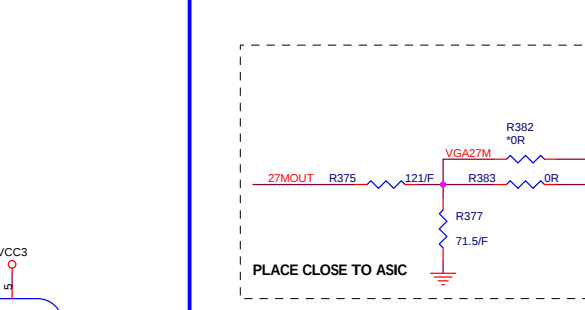
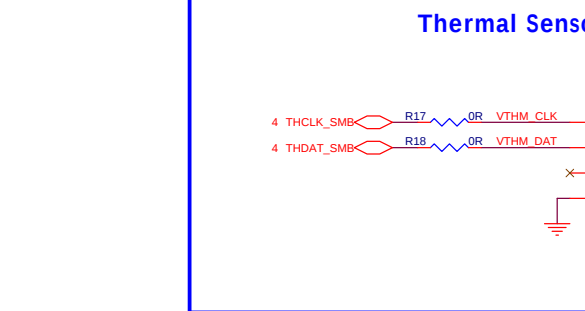
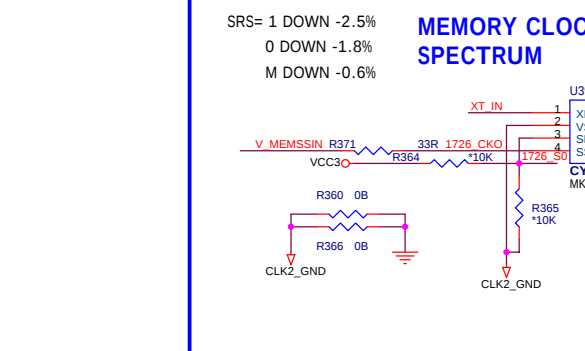
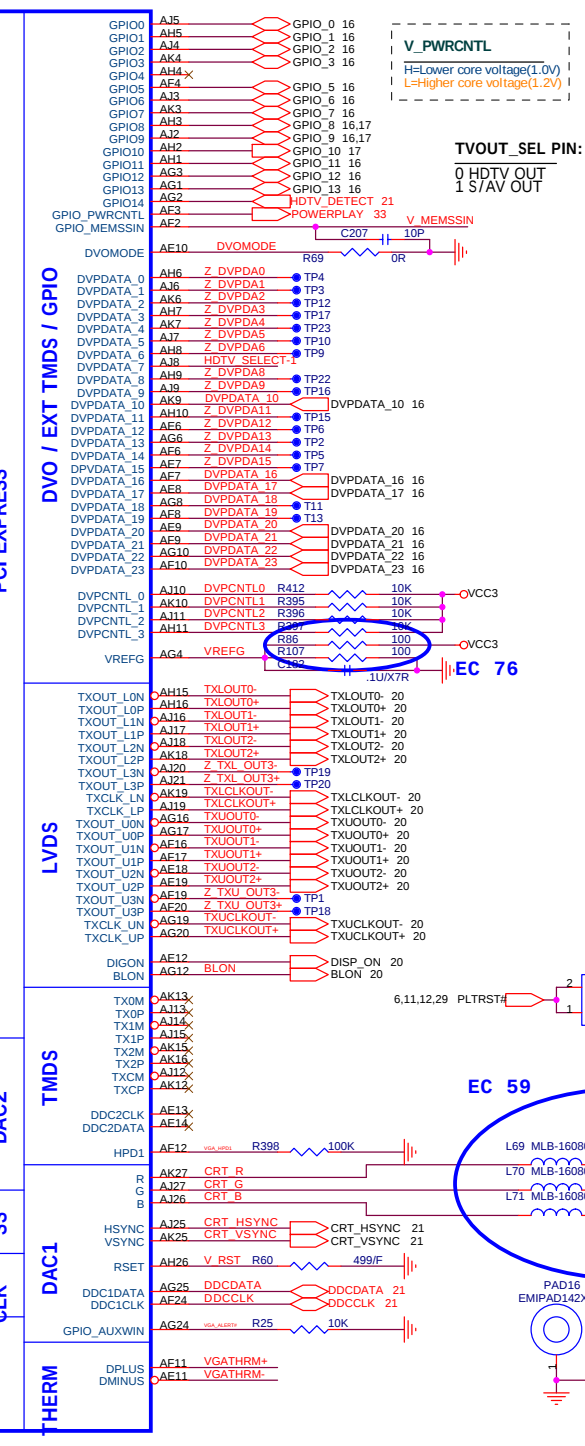
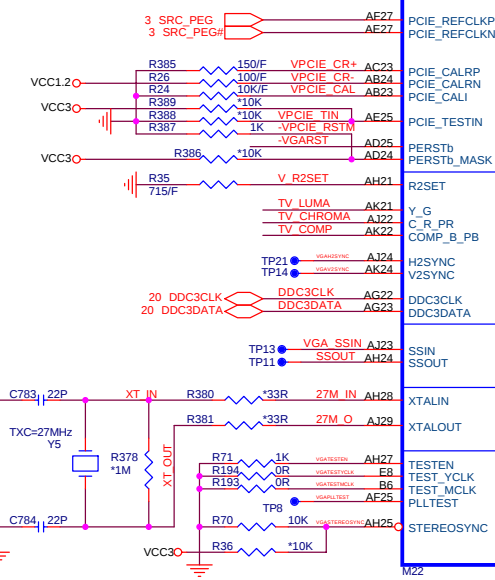
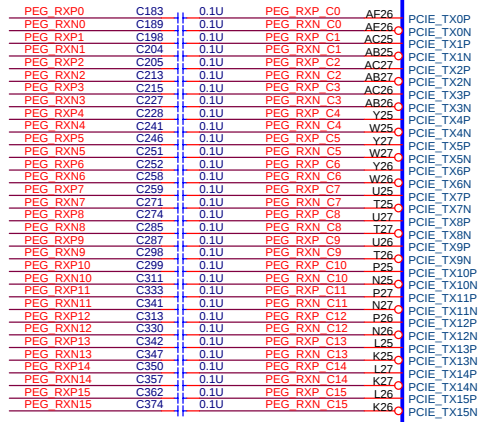
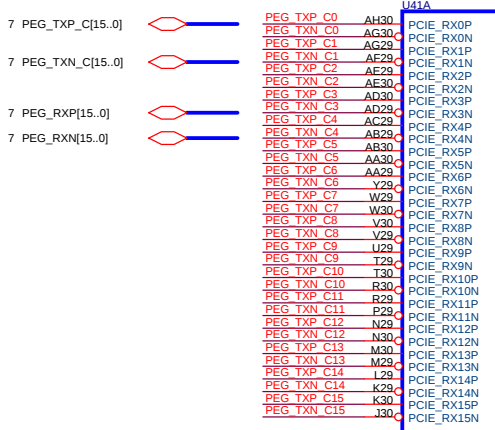


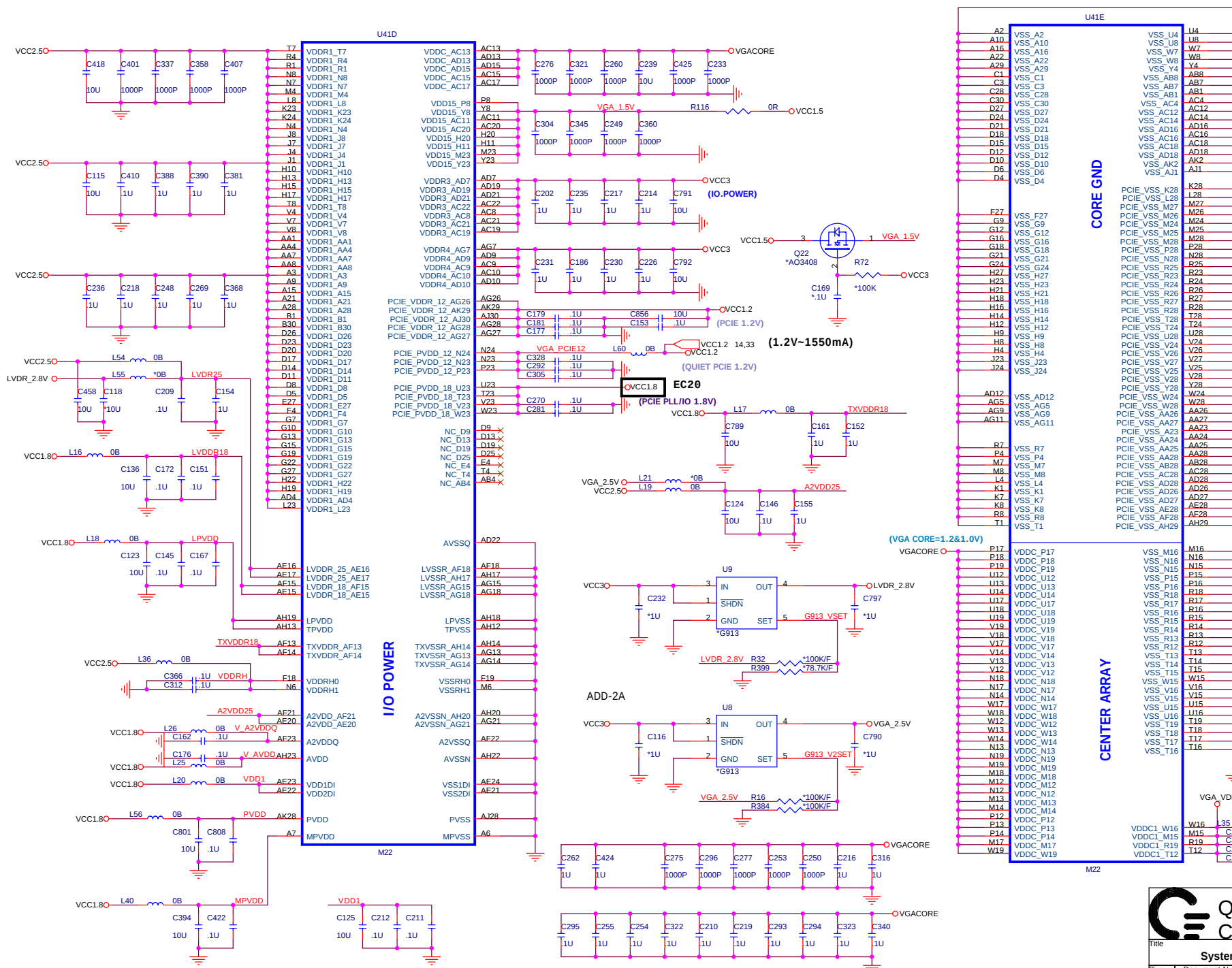
System Block Diagram

Size Custom Document Number AW3 Rev 1A

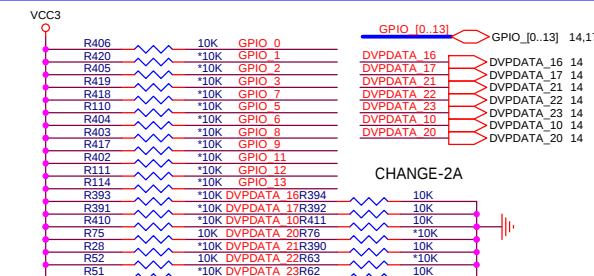
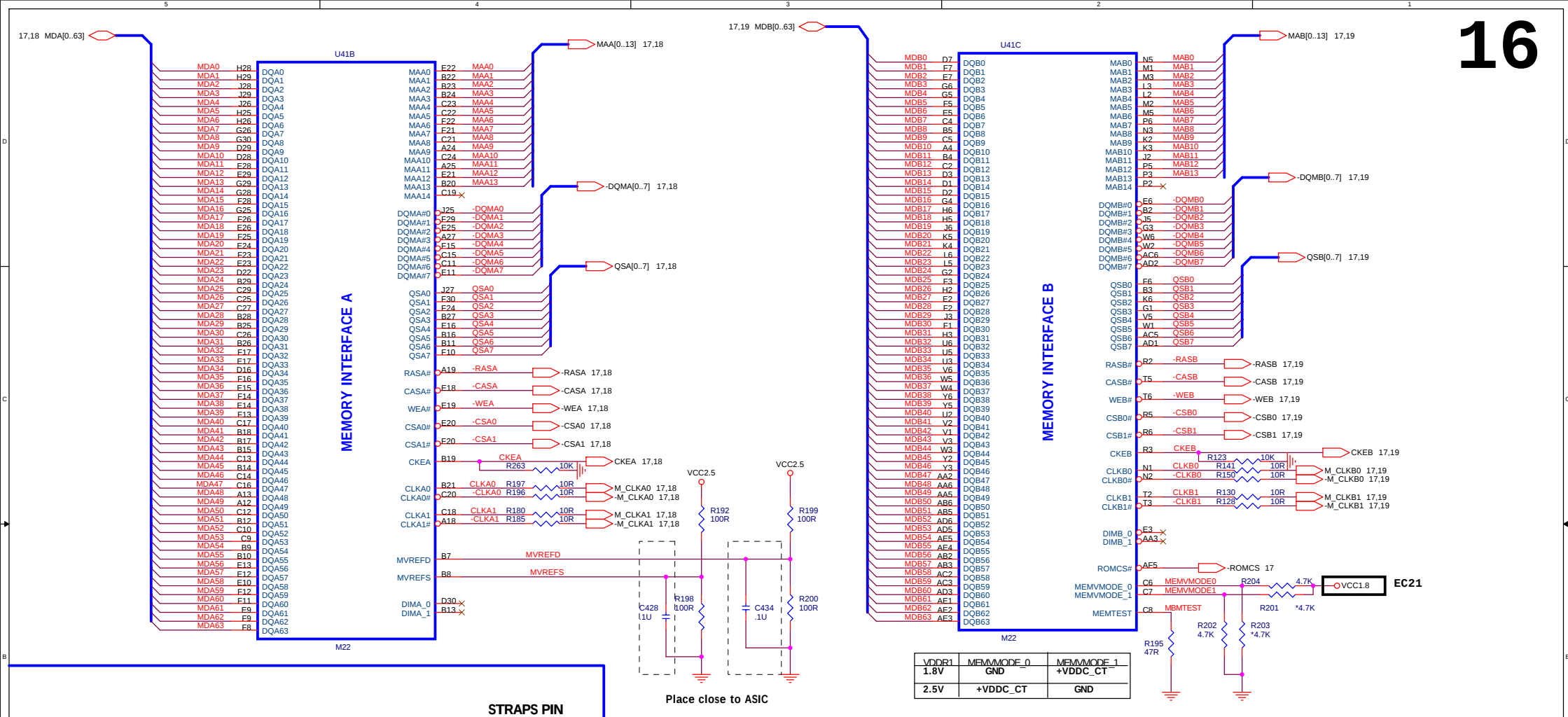
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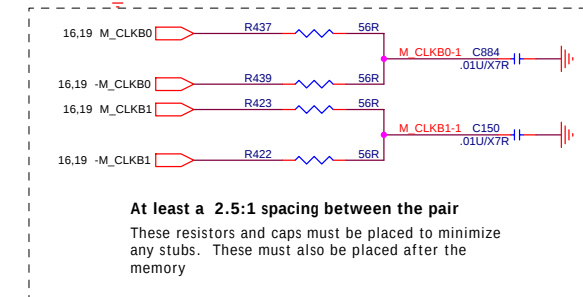
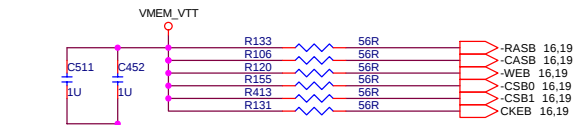
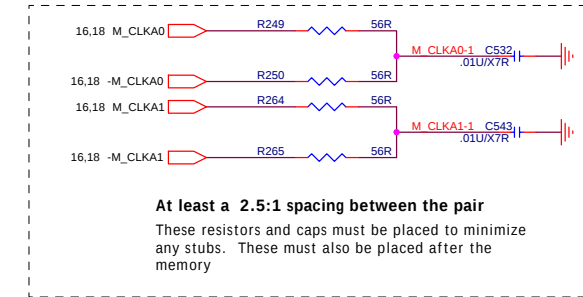
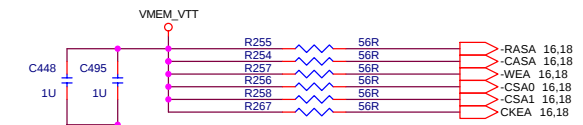
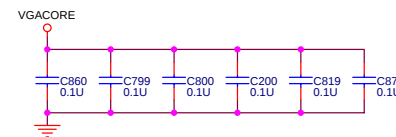
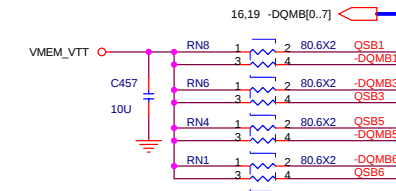
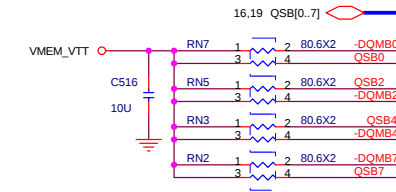
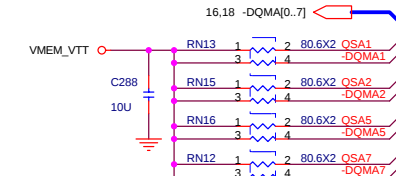
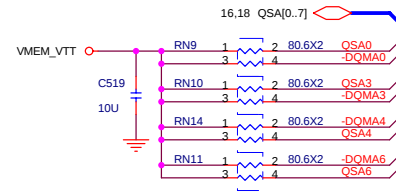
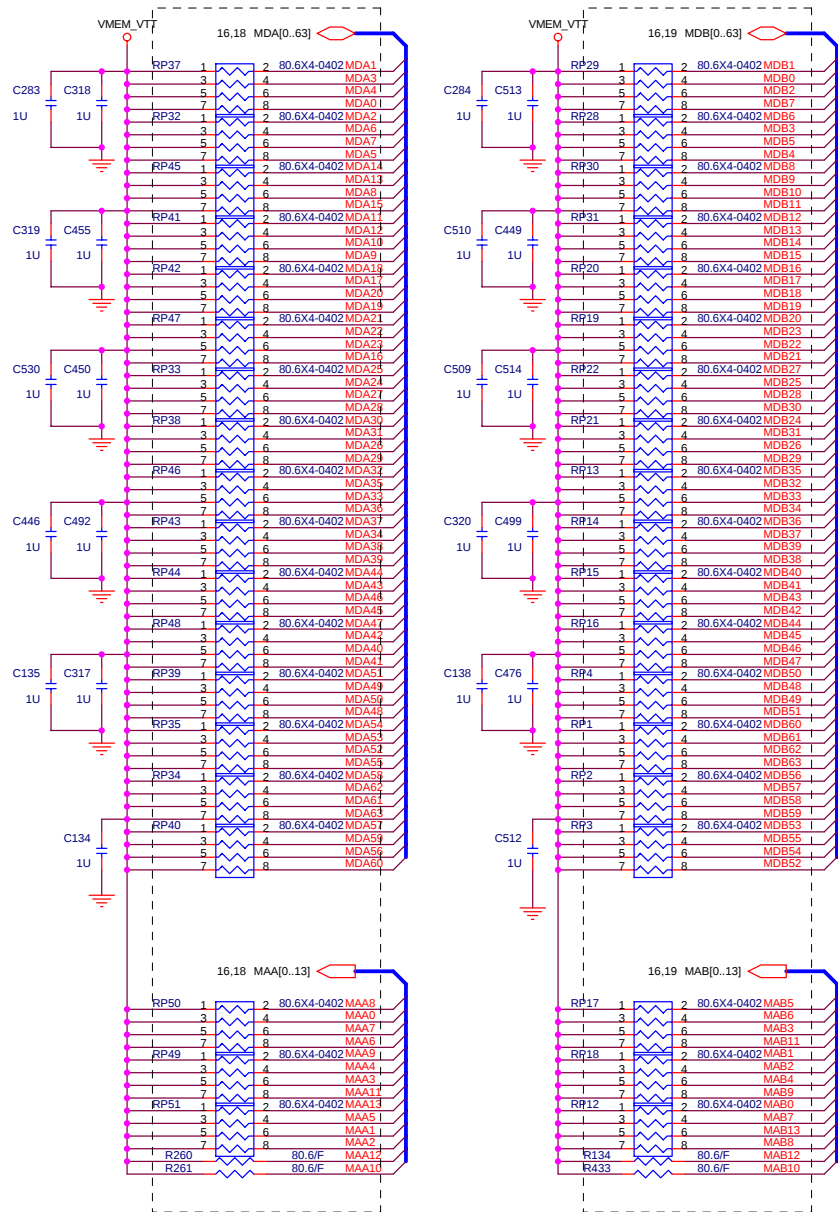
GPIO6, GPIO7 STRAPPING

1 : pop R418 -- Hynix 8M x 32 -- 128MB
0 : no-pop R418 -- Hynix 4M x 32 -- 64MB

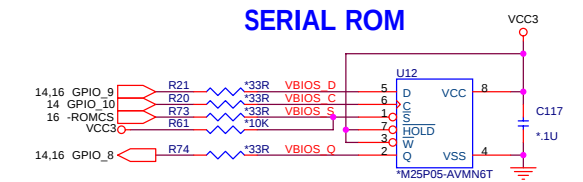
pop R418, R404 -- Hynix 8M x 32 -- 128M(NEW)



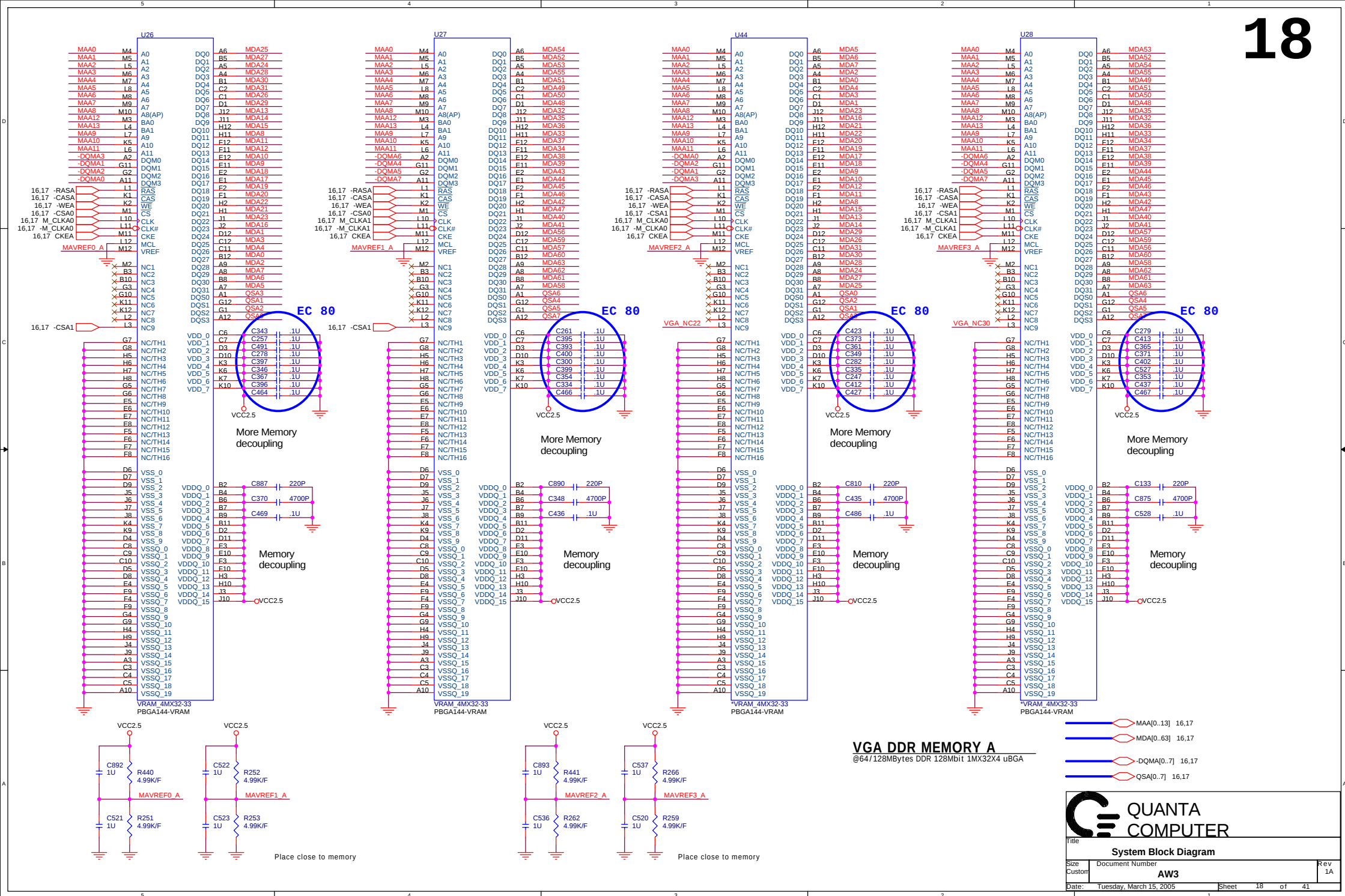
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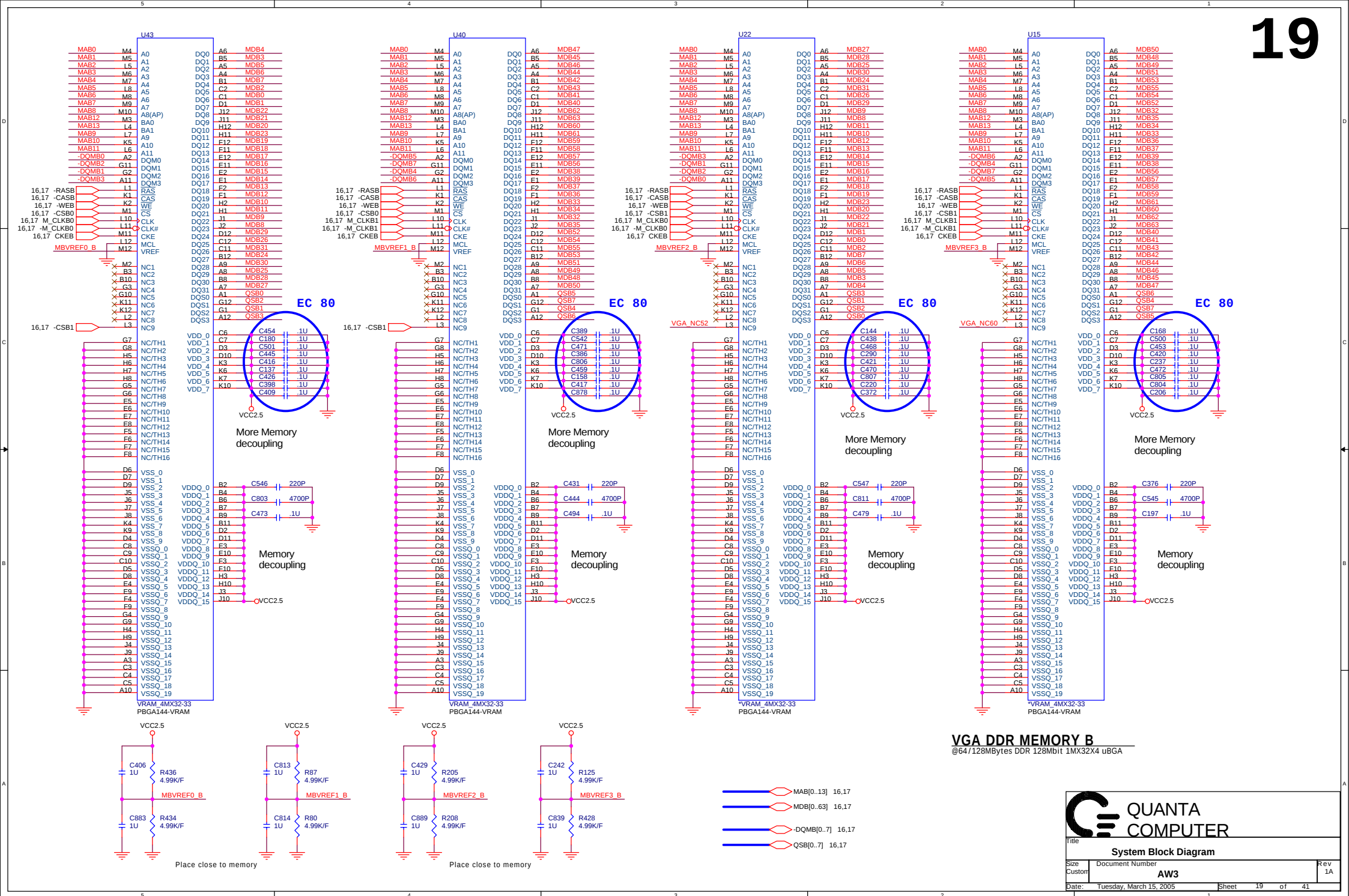


SERIAL ROM

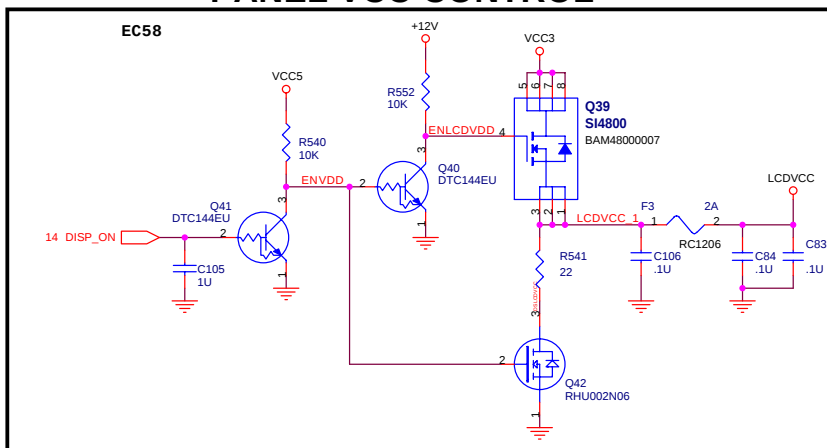


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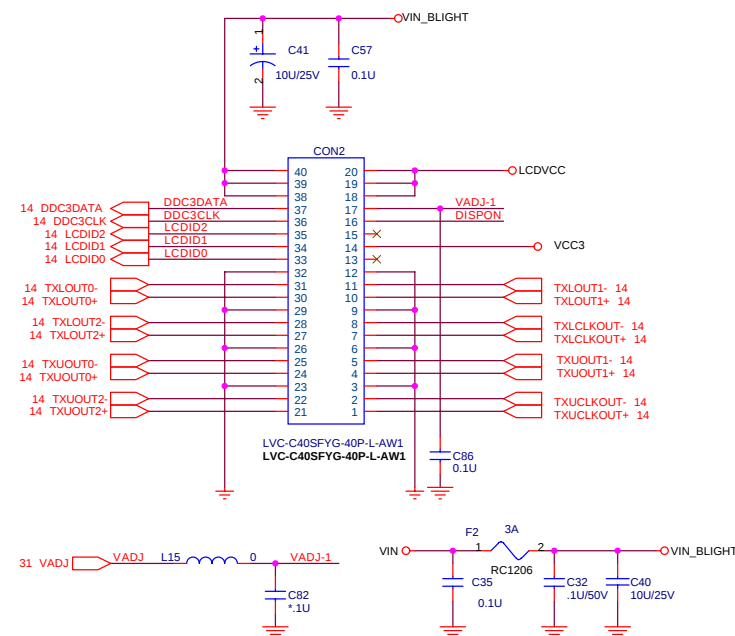
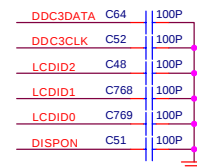
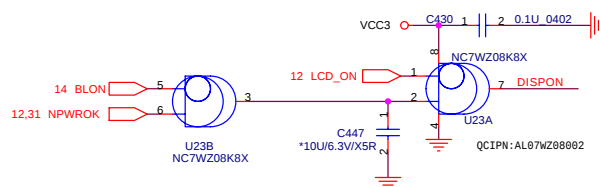




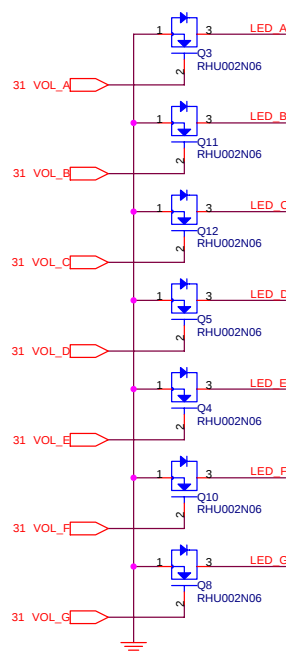
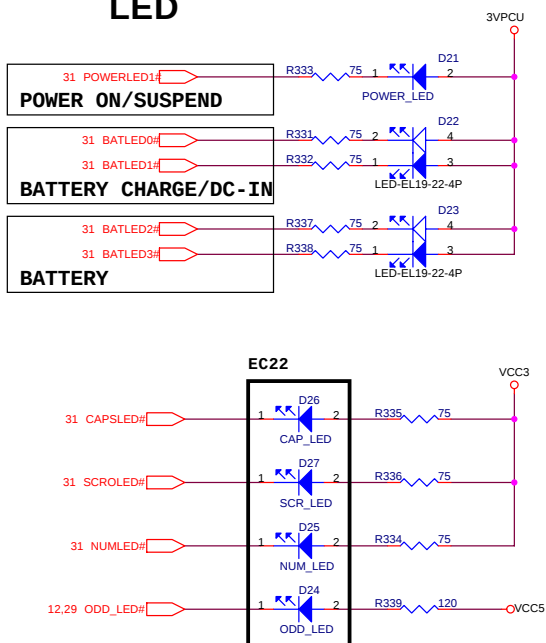
LCD CONNECTOR



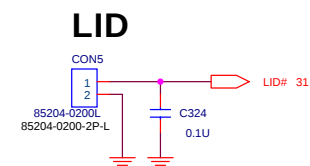
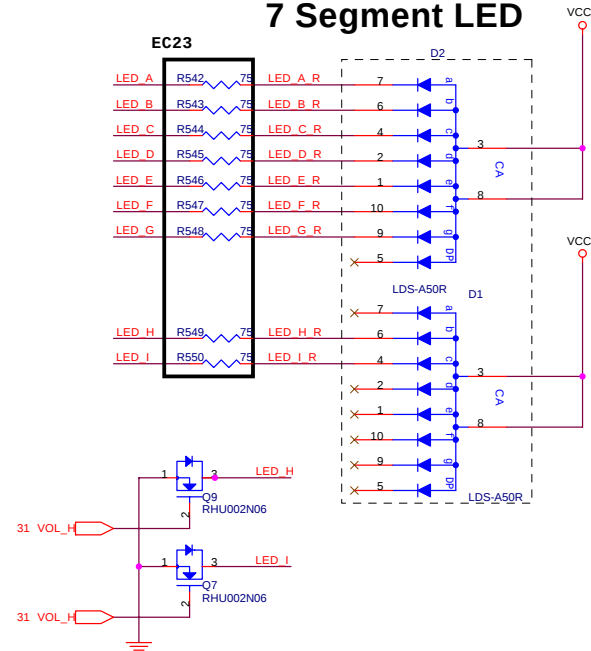
BACKLIGHT CONTROL



LED

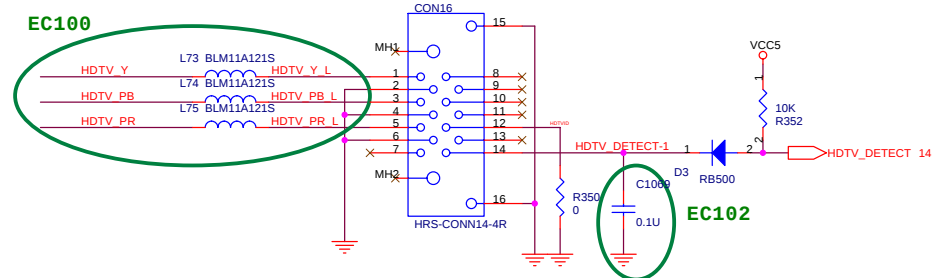


7 Segment LED



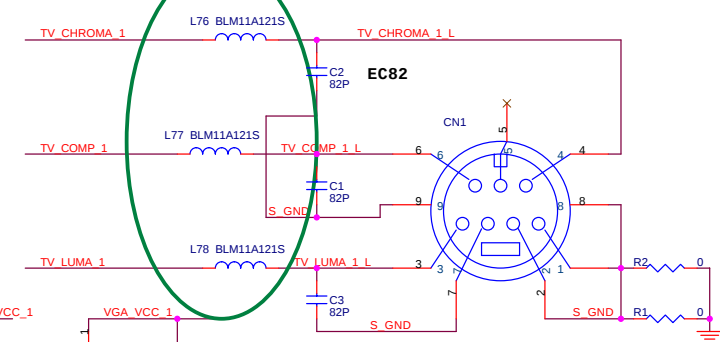
HDTV

EC100



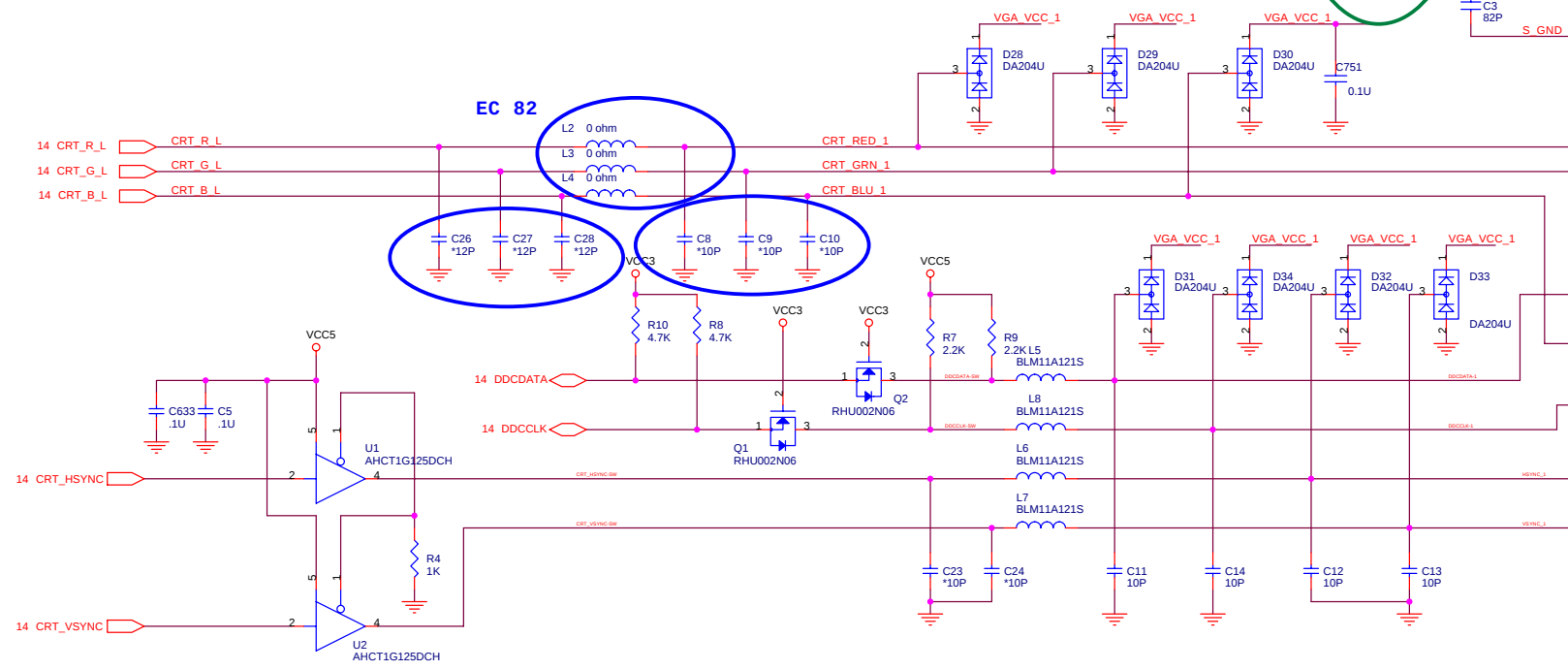
S-VIDEO

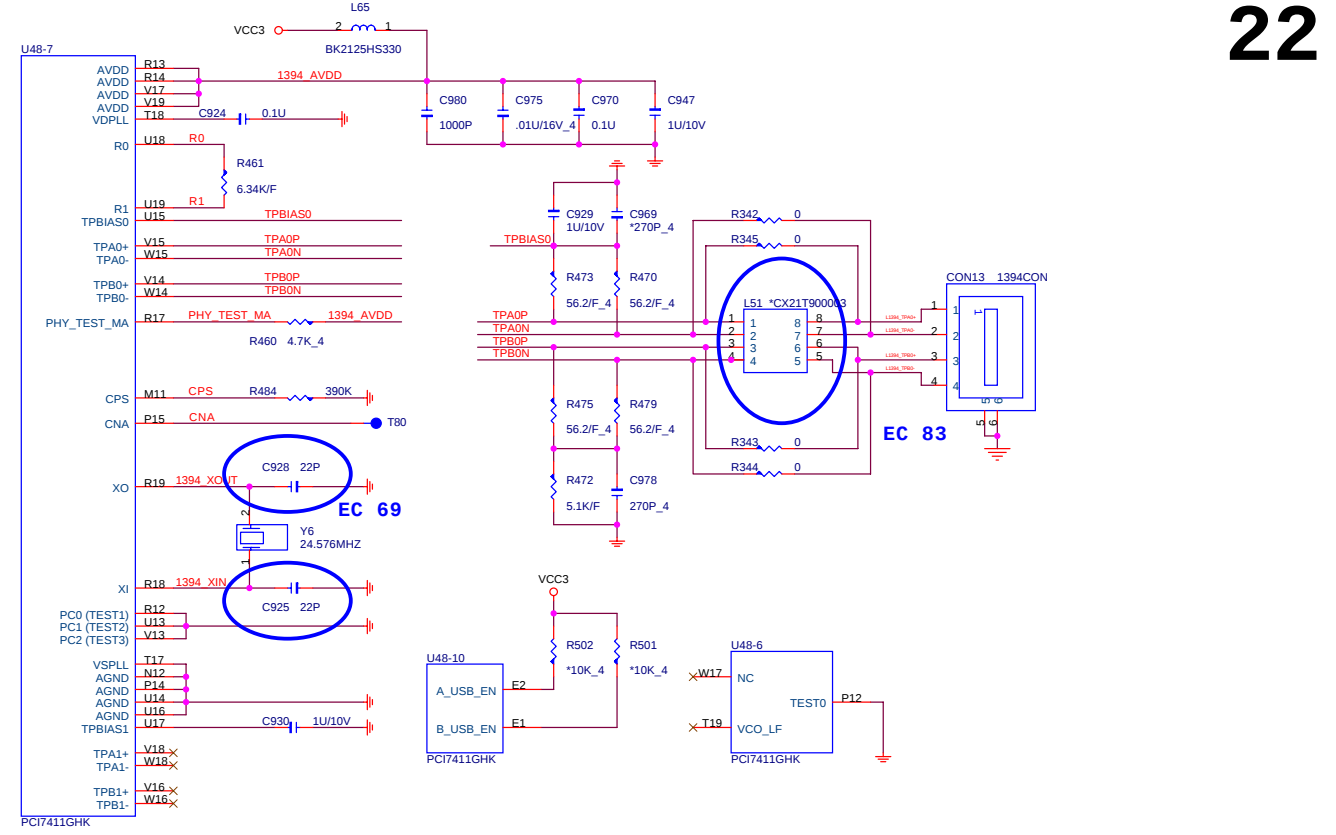
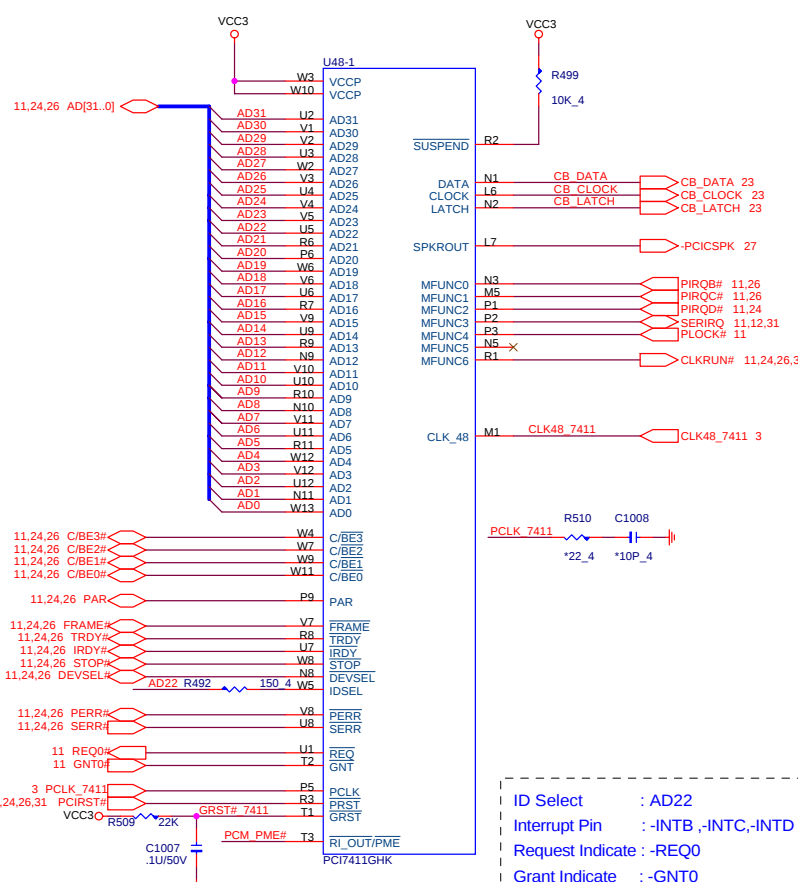
EC101



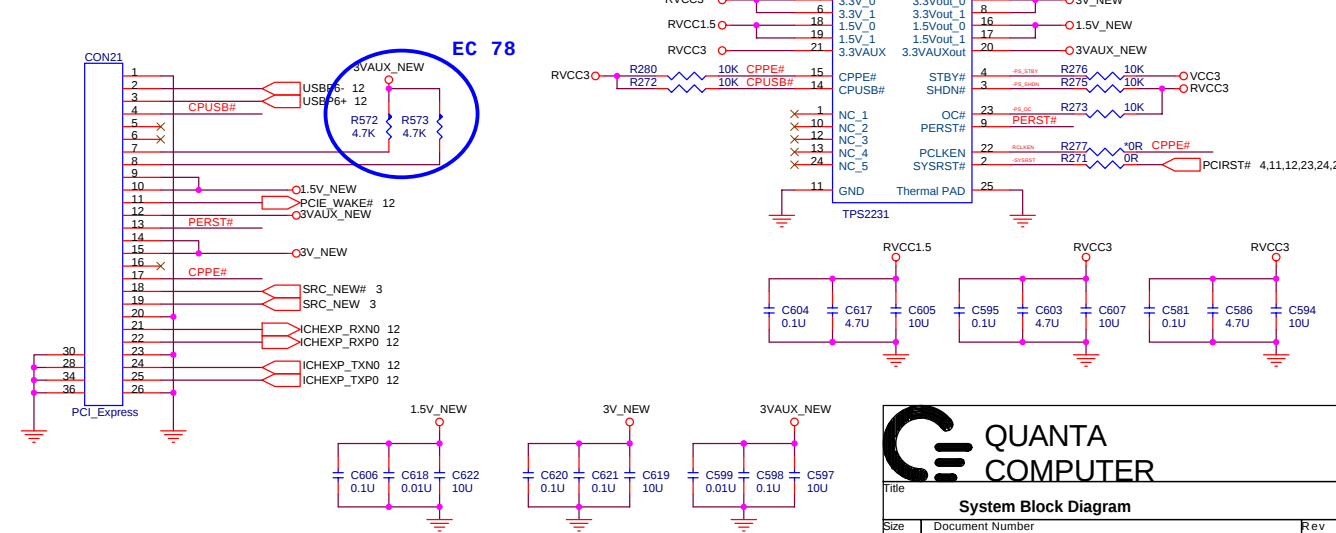
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L:A-B0

EC 82





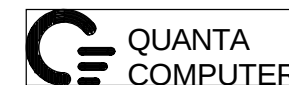
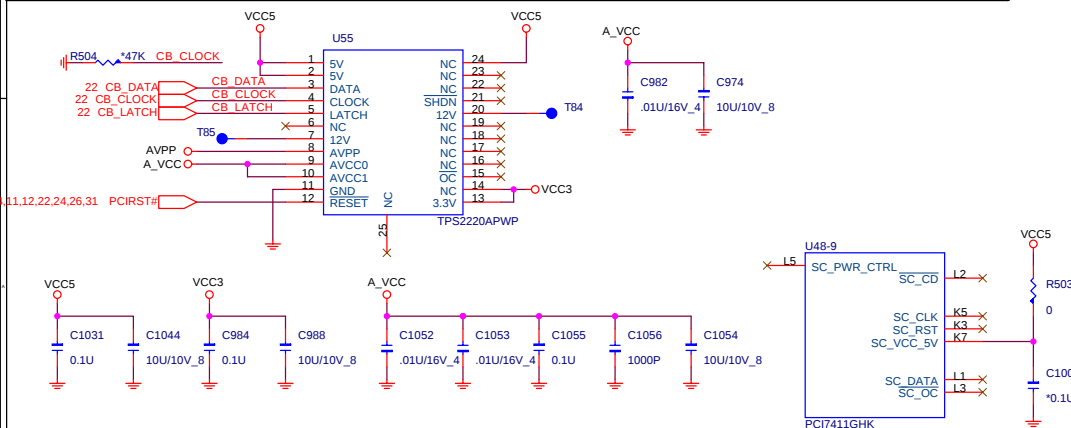
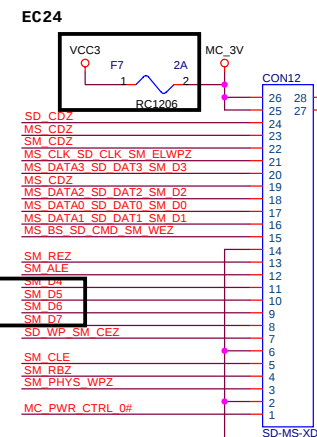
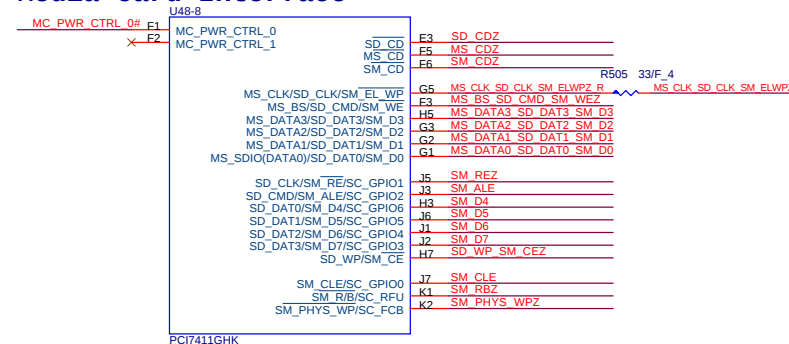
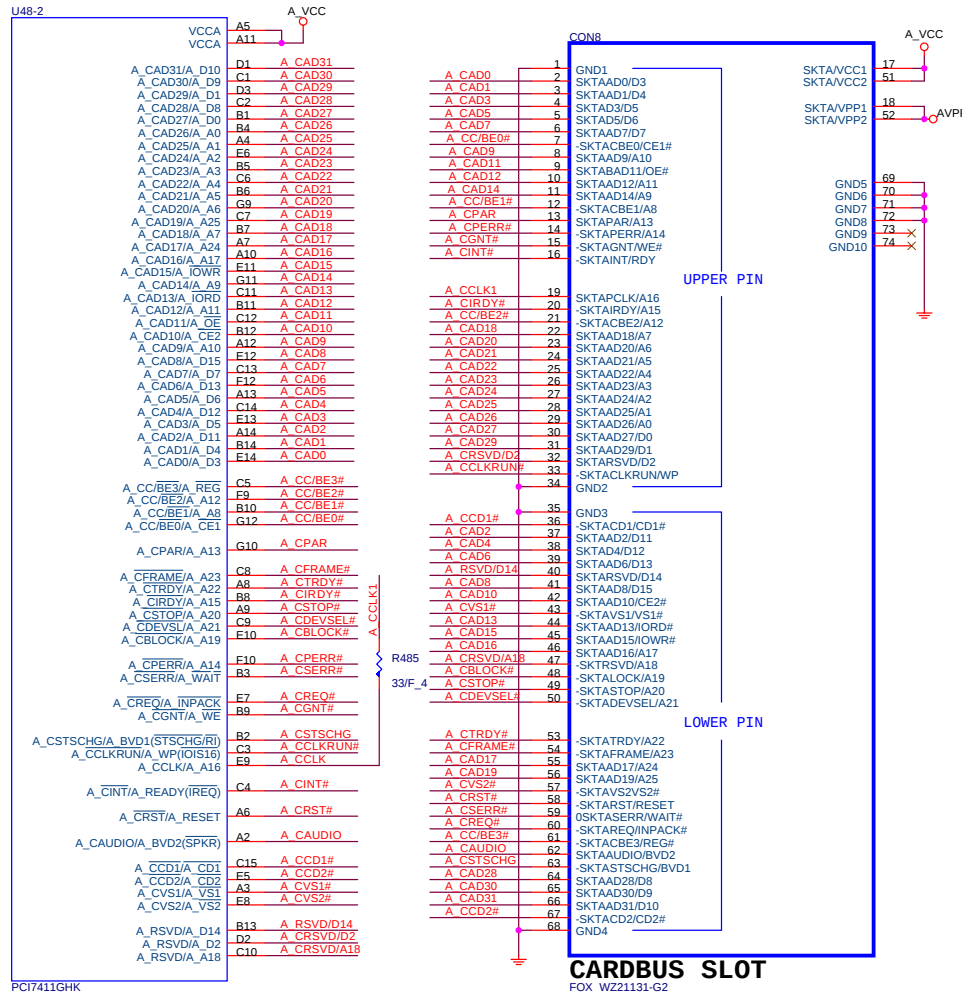
PCI-Express Card Power SW



QUANTA COMPUTER

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Media Card Interface

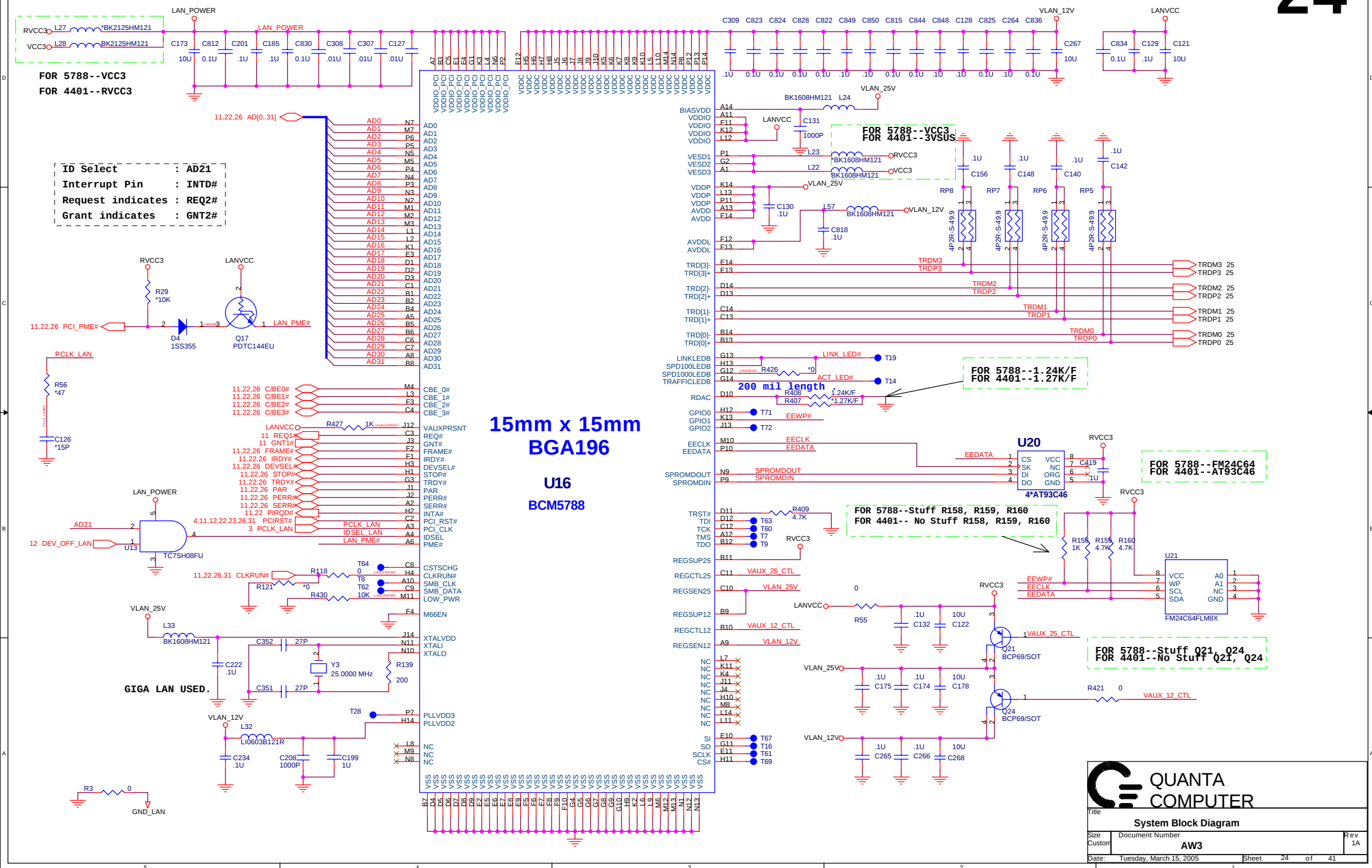


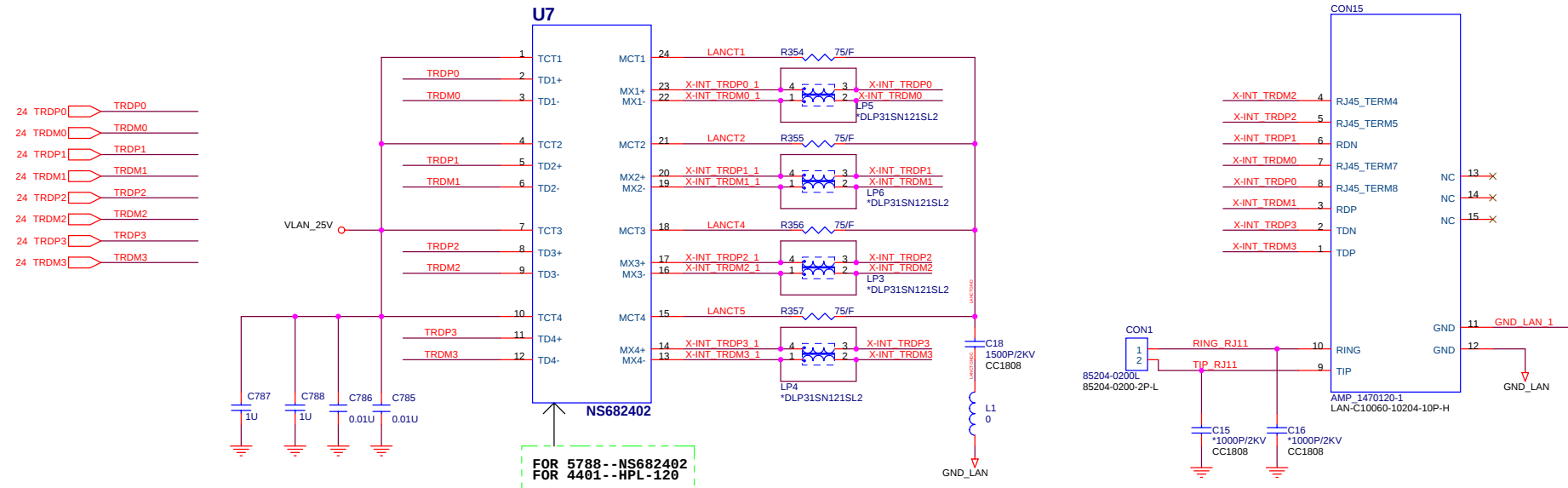
Title	System Block Diagram
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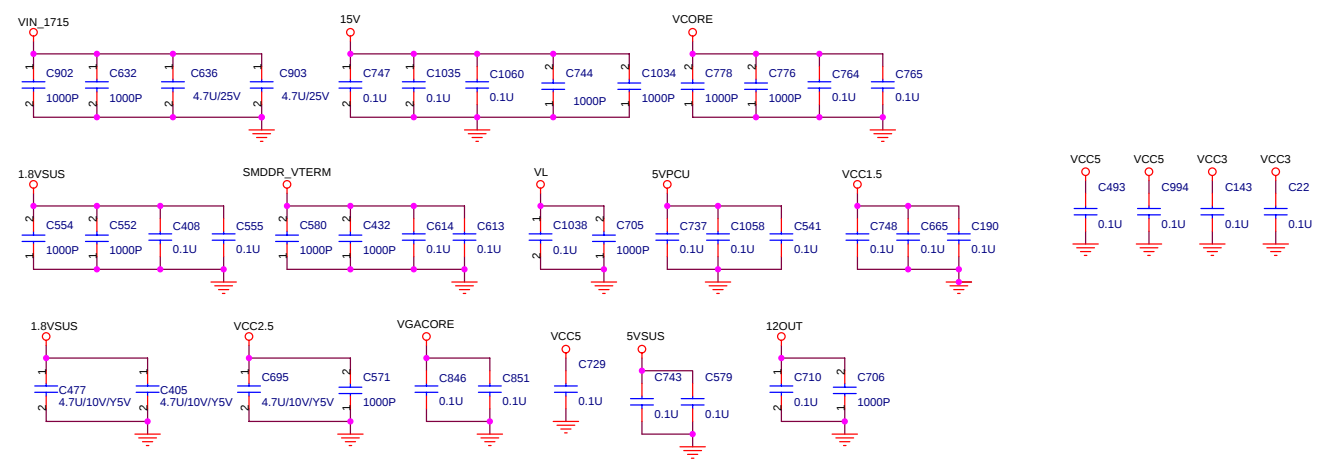
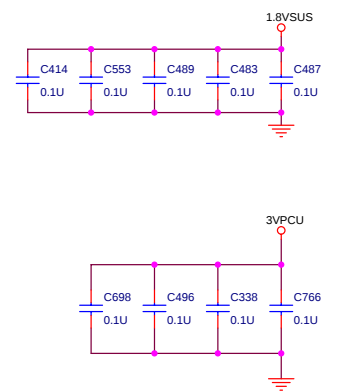
BCM4401 - -10/100
BCM5788 - -10/100/GIGA

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For EMI





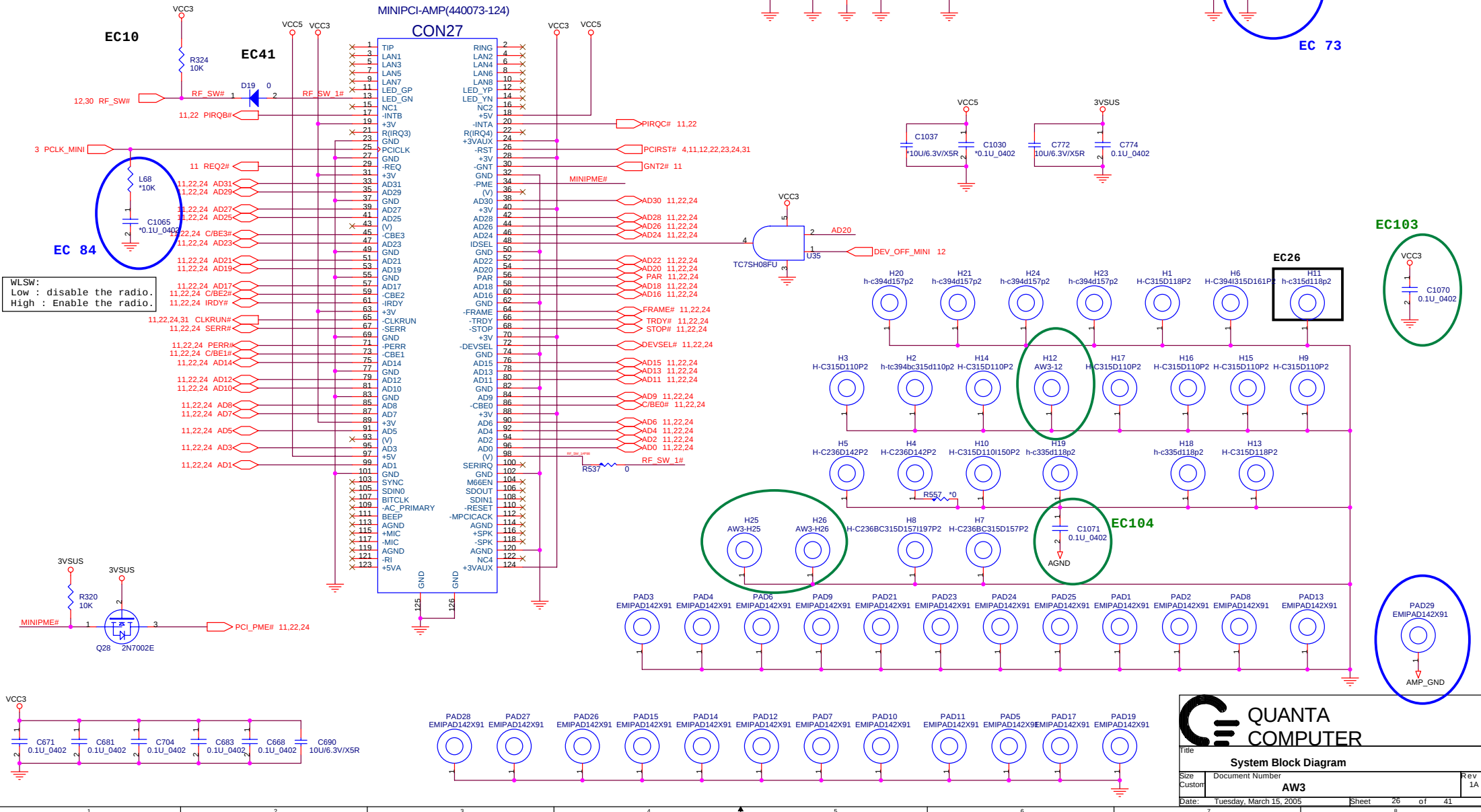
QUANTA
COMPUTER

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MDC V1.5 12Pin (Askey) Azalia MDC interface

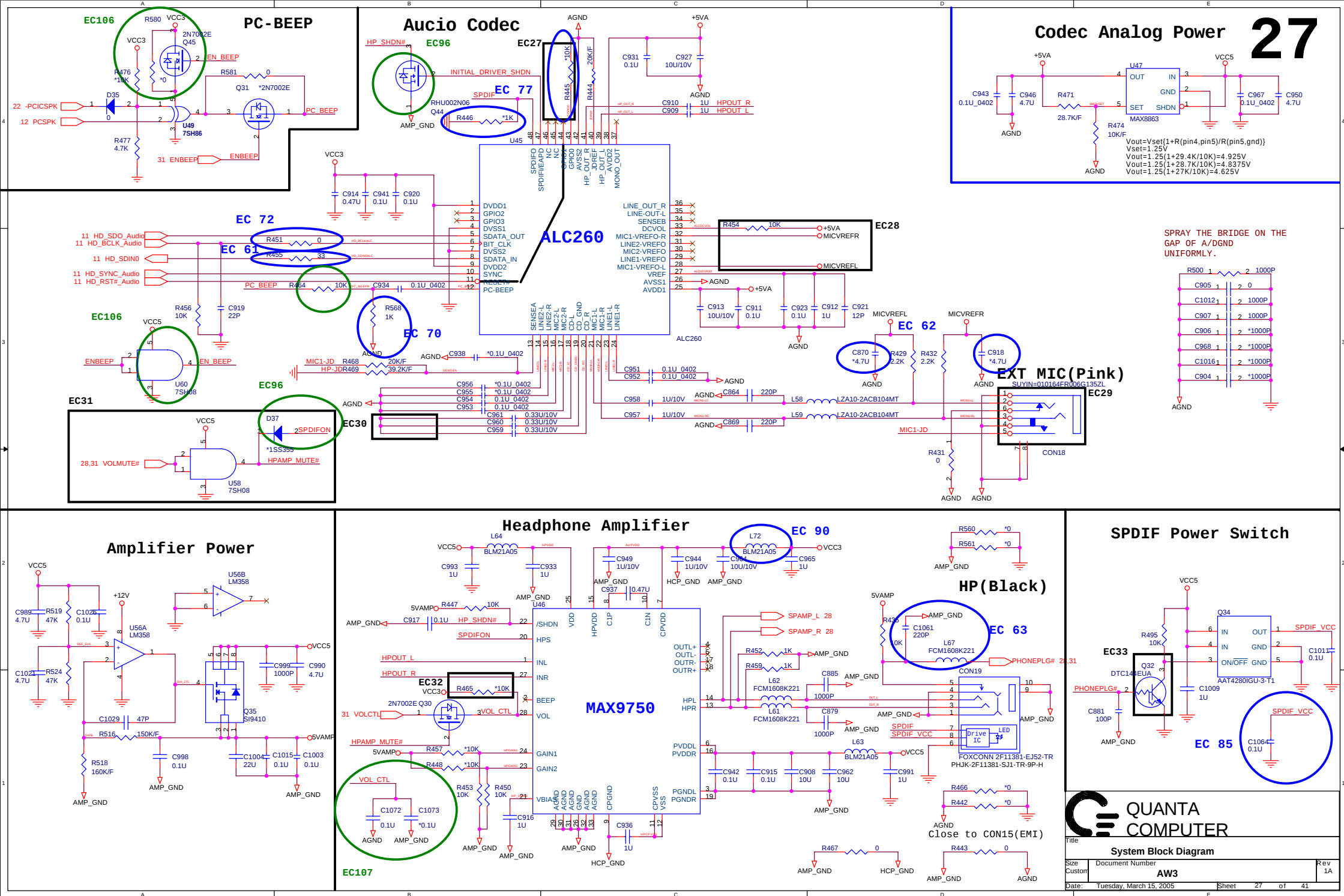
ID Select : AD20
Interrupt Pin : -INTB, -INTC
Request indicates : -REQ1
Grant indicates : -GNT1

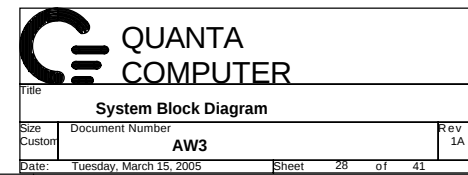
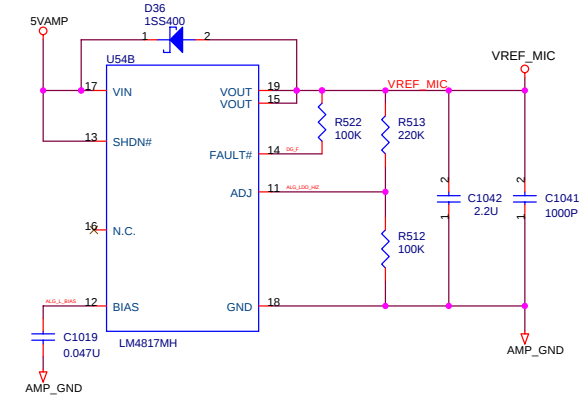
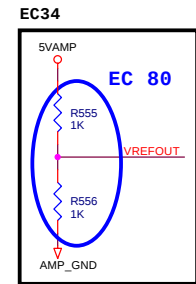
LED_GP : LED WLEN LINK
Output Current : 7mA
Blink rate : 1 flash per every 3 sec.



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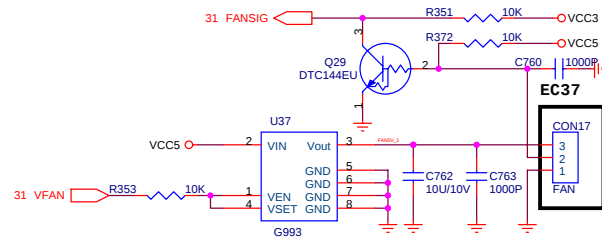




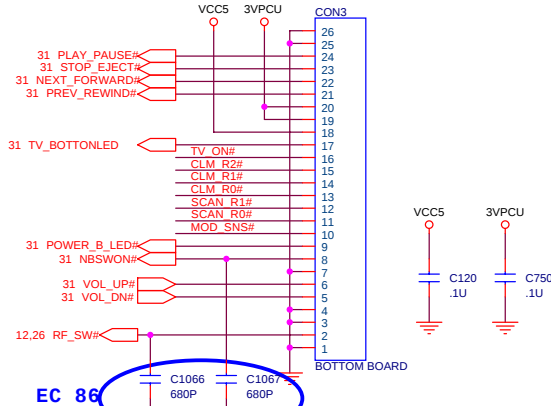
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MAIN FAN UNIT

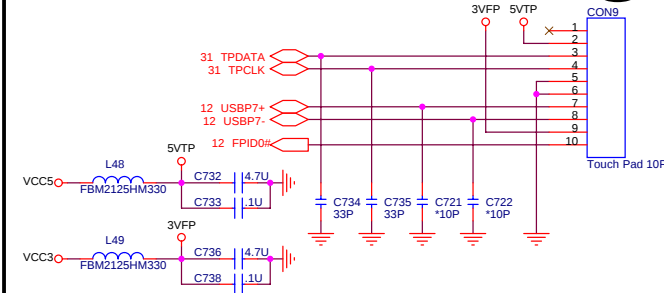


BUTTON BOARD

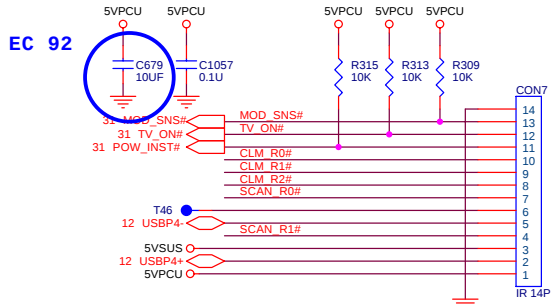


Touch Pad & Finger Print

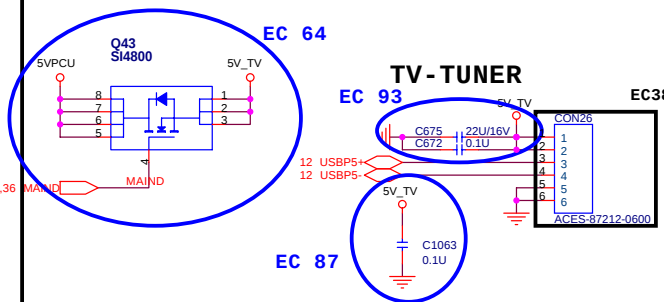
Power trace keep 12mil.



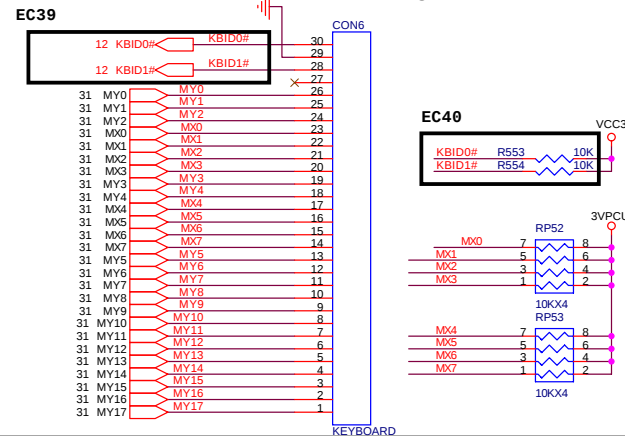
TO RECEIVER MODULE



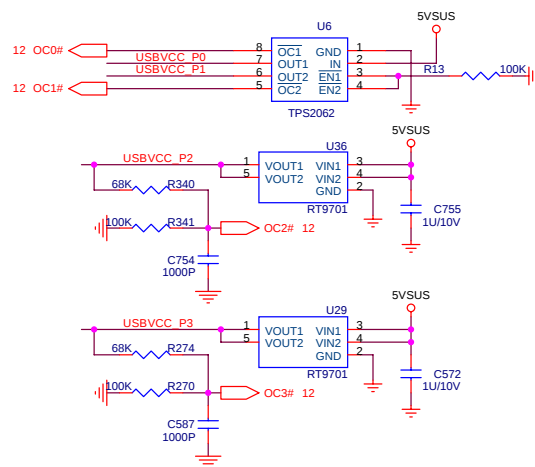
TV-TUNER



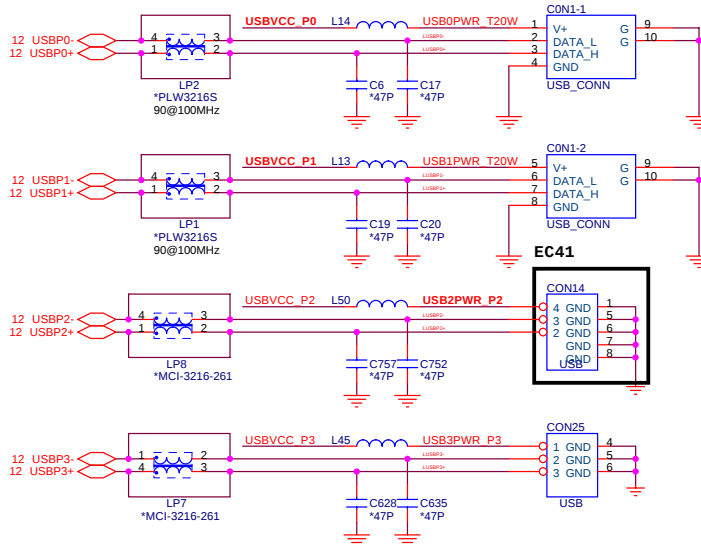
KEYBOARD



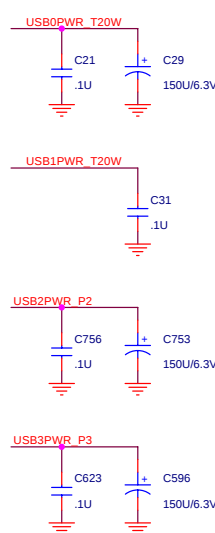
USB Power and Over current



USB Connector



Place near the USB connector



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3VPCU

ECHWPG# R237 10K

BA2# R179 2 1 *10K

BA3# R178 2 1 *10K

BA5# R173 2 1 10K

BA1# R189 2 1 *10K

NBSWON# R182 2 1 10K

BIOS_CRISIS_REC R241 2 1 10K

BIOS_HDD_CLEAR R240 2 1 10K

STOP_EJECT# R154 2 1 10K

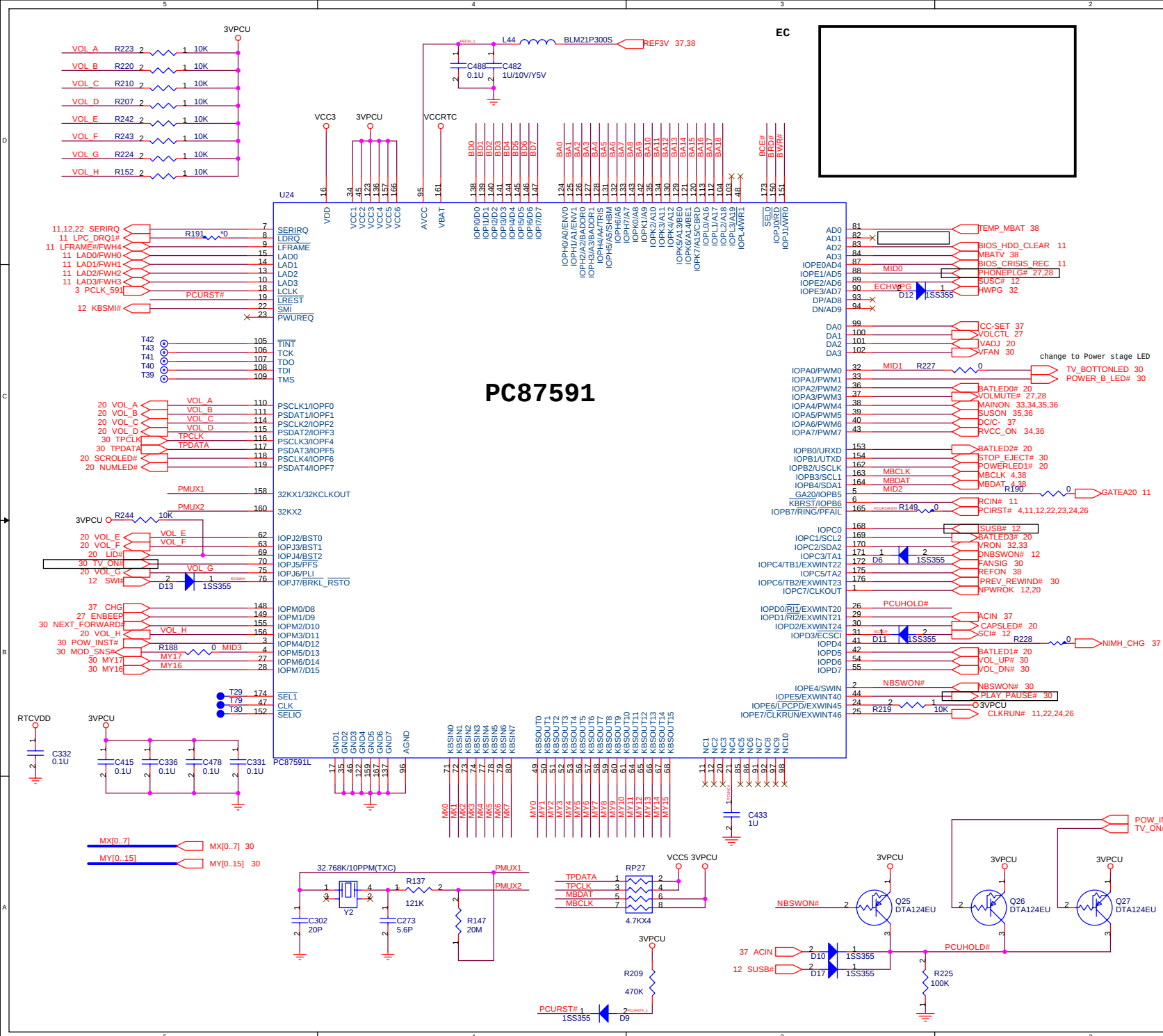
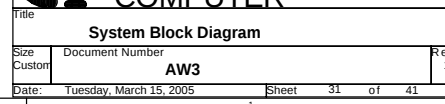
PREV_REWIND# R148 2 1 10K

PAUSE_PLAY# R231 2 1 10K

NEXT_FORWARD# R153 2 1 10K

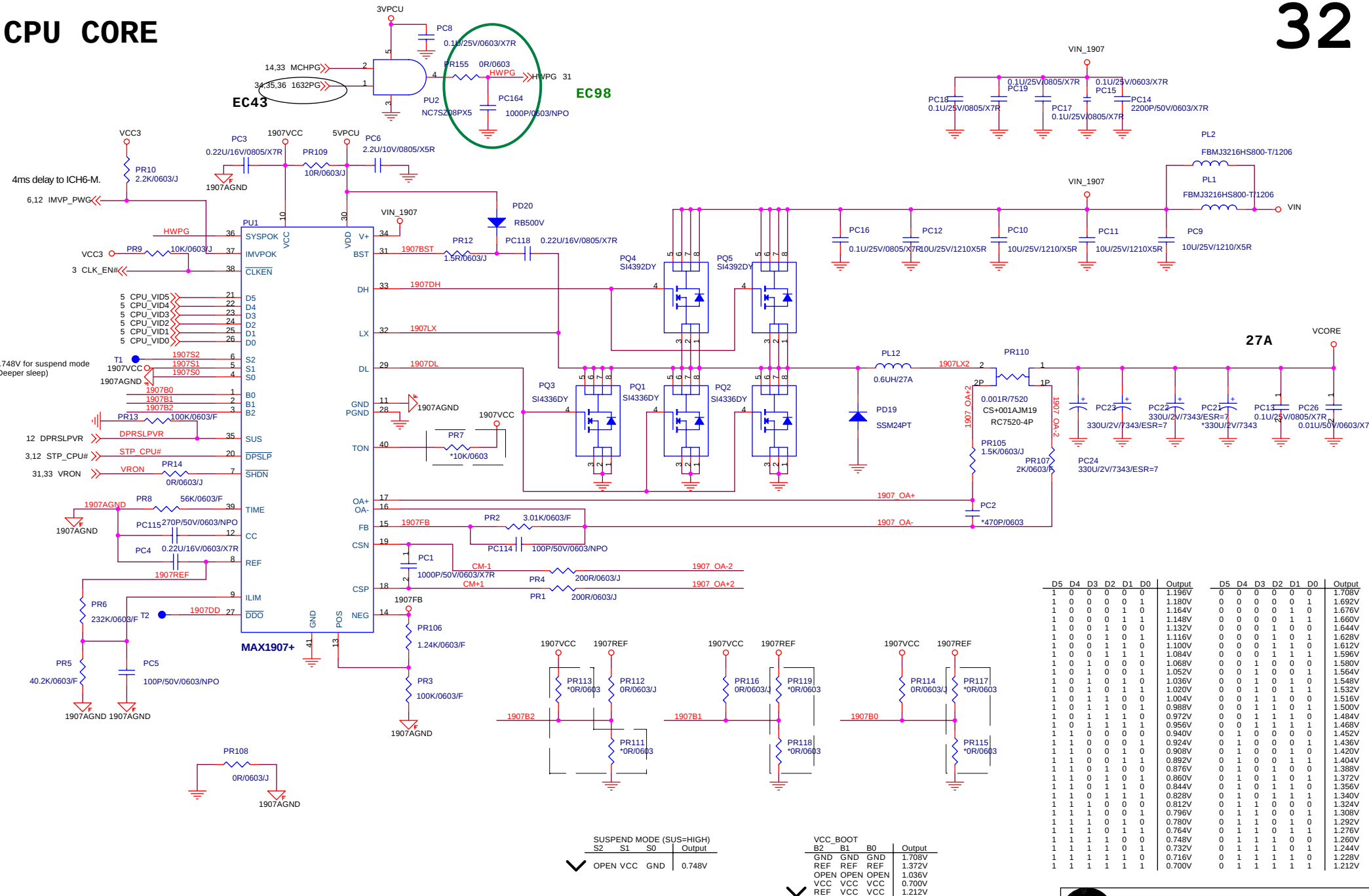
Enviroment	ENV0(BA0)	ENV1(BA1)	TRIS(BA4)
* IRE	0	0	0
0BD	0	1	0
DEV	1	0	0
PROG	1	1	0

```
BA0 : ENV0
BA1 : ENV1
BA4 : TRIS( If =1 will tristate all I/O pins)
BA5 : SHBM( If =1 Enable share host BIOS memory)
```



CPU CORE

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D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.196V	0	0	0	0	0	0	1.708V
1	0	0	0	0	1	1.180V	0	0	0	0	0	1	1.692V
1	0	0	0	1	0	1.164V	0	0	0	0	1	0	1.676V
1	0	0	0	1	1	1.148V	0	0	0	0	1	1	1.660V
1	0	0	1	0	0	1.132V	0	0	0	1	0	0	1.644V
1	0	0	1	0	1	1.116V	0	0	0	1	0	1	1.628V
1	0	1	0	0	0	1.100V	0	0	1	0	0	0	1.612V
1	0	1	0	1	0	1.084V	0	0	1	1	0	0	1.596V
1	0	1	0	0	0	1.068V	0	0	1	0	0	0	1.580V
1	0	1	0	0	1	1.052V	0	0	1	0	0	1	1.564V
1	0	1	0	1	0	1.036V	0	0	1	0	1	0	1.548V
1	0	1	0	1	1	1.020V	0	0	1	0	1	1	1.532V
1	0	1	1	0	0	1.004V	0	0	1	1	0	0	1.516V
1	0	1	1	0	1	0.988V	0	0	1	1	0	1	1.500V
1	0	1	1	1	0	0.972V	0	0	1	1	1	0	1.484V
1	0	1	1	1	1	0.956V	0	0	1	1	1	1	1.468V
1	1	0	0	0	0	0.940V	0	1	0	0	0	0	1.452V
1	1	0	0	0	1	0.924V	0	1	0	0	0	1	1.436V
1	1	0	0	1	0	0.908V	0	1	0	0	1	0	1.420V
1	1	0	0	1	1	0.892V	0	1	0	0	1	1	1.404V
1	1	0	1	0	0	0.876V	0	1	0	1	0	0	1.388V
1	1	0	1	0	1	0.860V	0	1	0	1	0	1	1.372V
1	1	0	1	1	0	0.844V	0	1	0	1	1	0	1.356V
1	1	0	1	1	1	0.828V	0	1	0	1	1	1	1.340V
1	1	1	0	0	0	0.812V	0	1	1	0	0	0	1.324V
1	1	1	0	0	1	0.796V	0	1	1	0	0	1	1.308V
1	1	1	0	1	0	0.780V	0	1	1	0	1	0	1.292V
1	1	1	0	1	1	0.764V	0	1	1	0	1	1	1.276V
1	1	1	1	0	0	0.748V	0	1	1	1	0	0	1.260V
1	1	1	1	0	1	0.732V	0	1	1	1	0	1	1.244V
1	1	1	1	1	0	0.716V	0	1	1	1	1	0	1.228V
1	1	1	1	1	1	0.700V	0	1	1	1	1	1	1.212V



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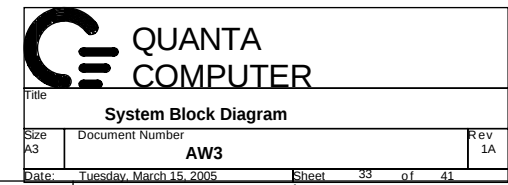
AW3

Date: Tuesday, March 15, 2005

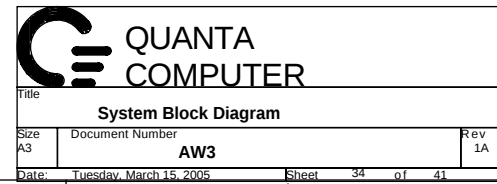
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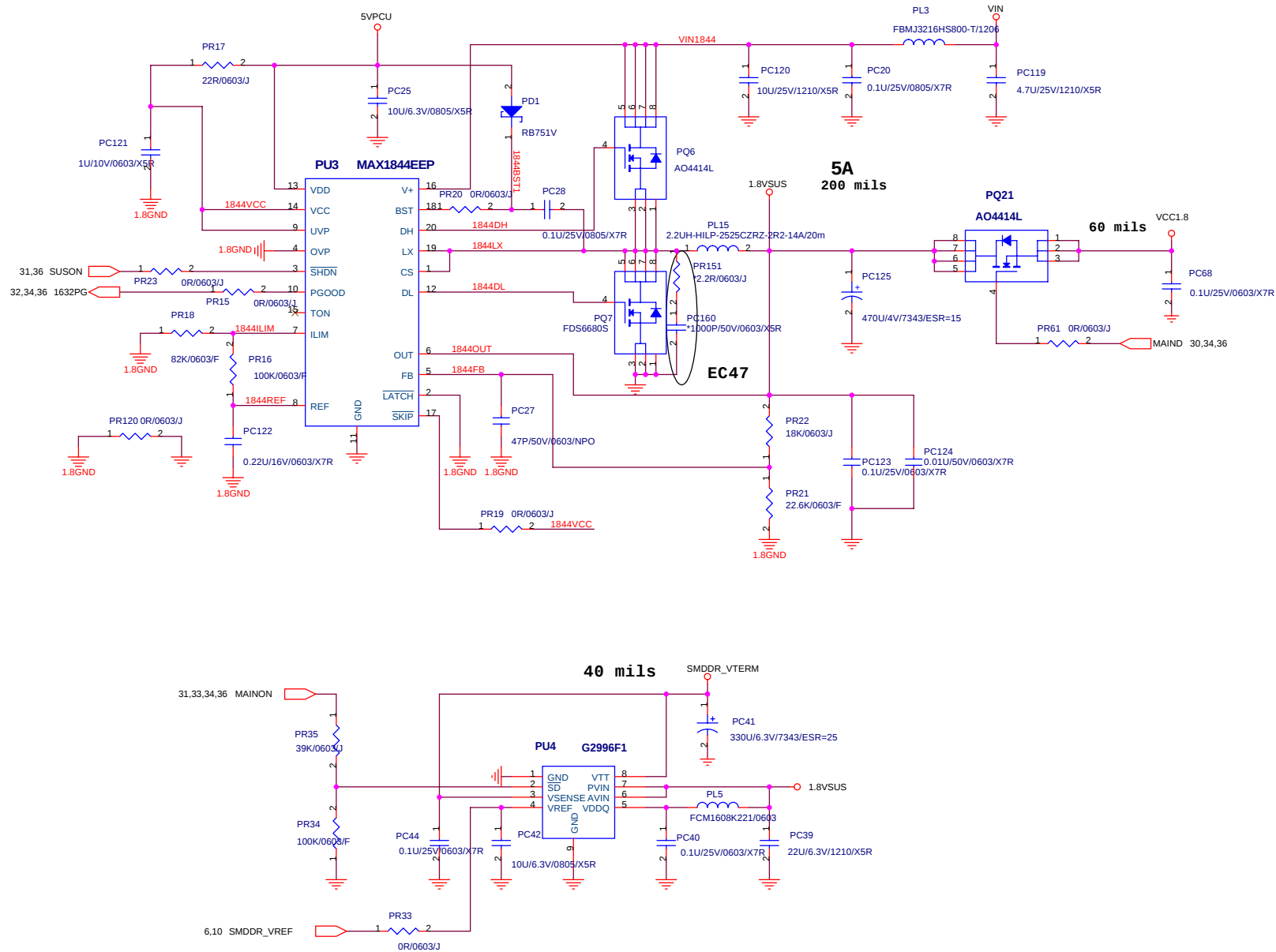
Rev 1A

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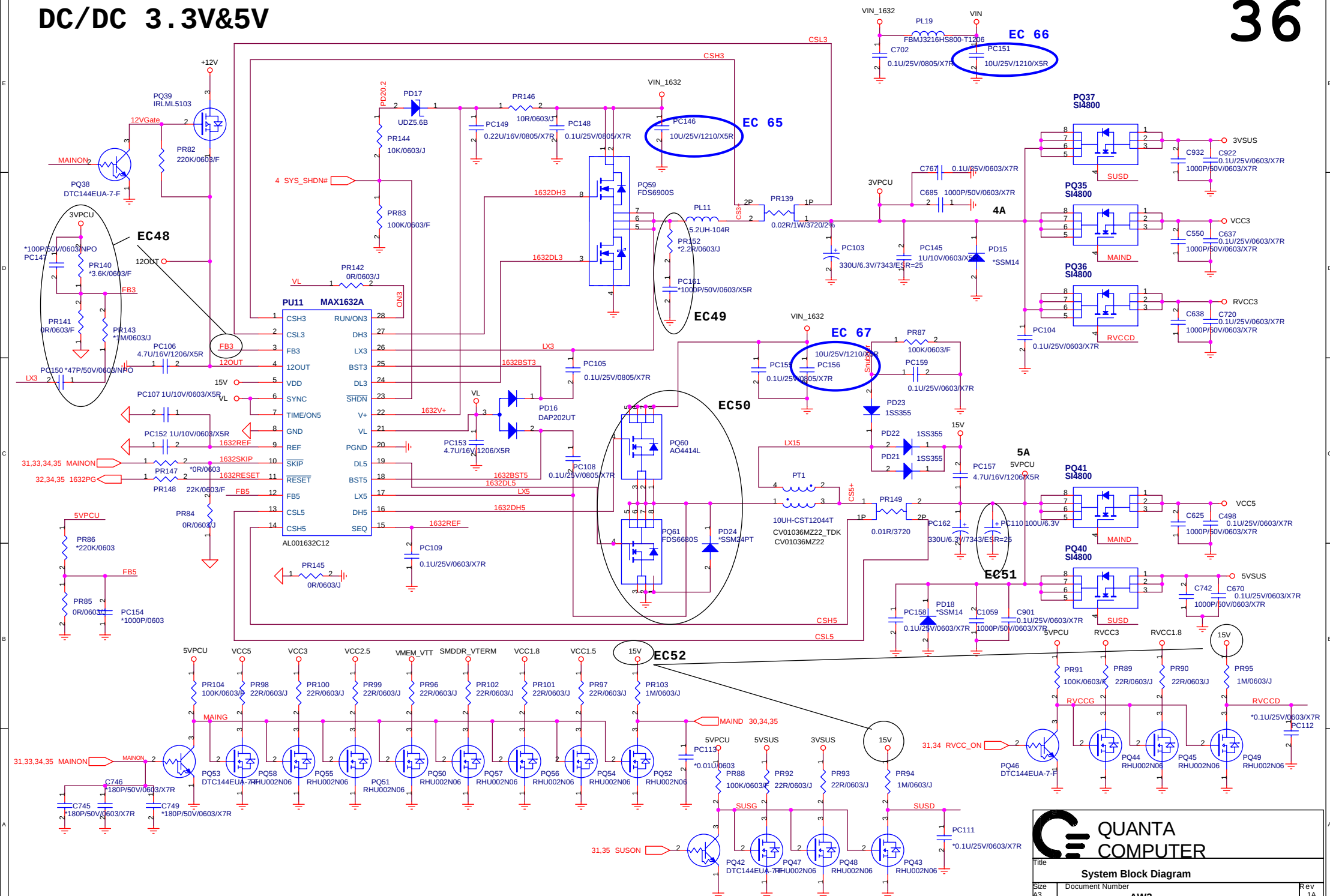
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DC/DC 3.3V&5V

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80W/ 19V/ 4.22A

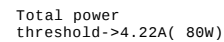


QUANTA
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System Block Diagram

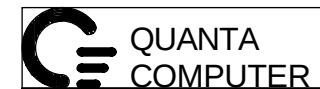
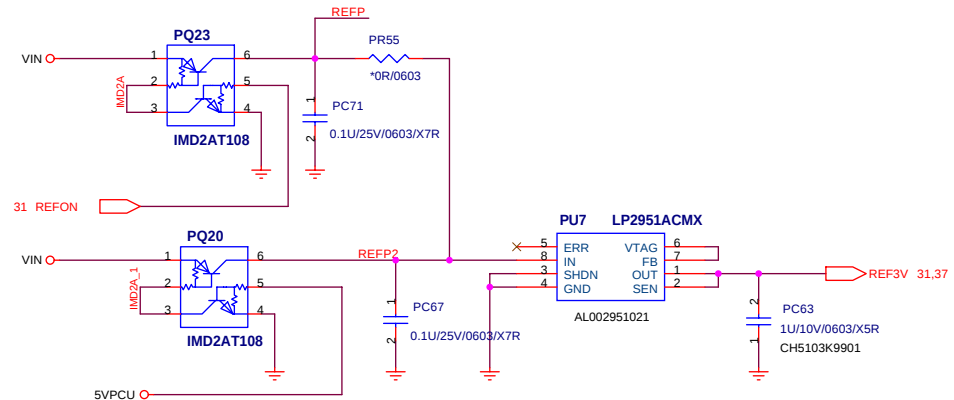
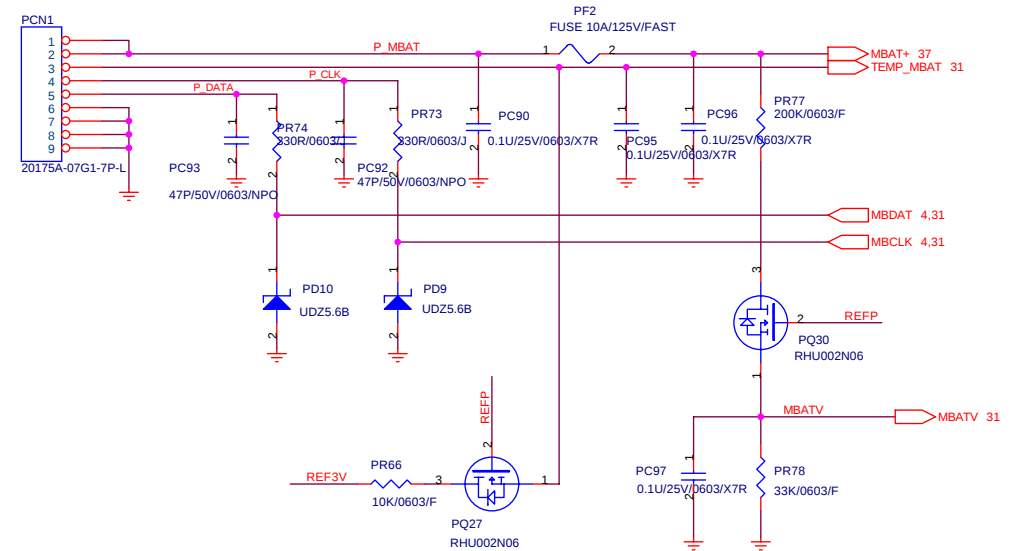
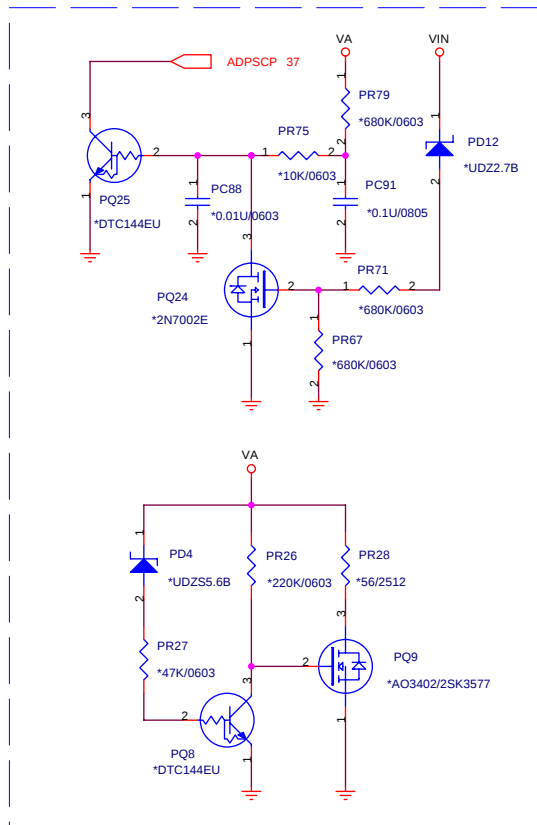
1A

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Battery Connector

SCP CKT



EC LIST -- A to B test :

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EC1-- Page 3 -- Change R176, R177 footprint to 0402 -- Fix footprint error in A PCBA
 EC2-- Page 6 -- R183,R184 change to no-pop -- Intel suggest to improve S3
 EC3-- Page 6 -- R65 change to no-pop to set DMI x 4-- A design error
 EC4-- Page 6 -- R91 change to no-pop -- Set PCIE to normal operation
 EC5-- Page 11 -- Change R310 to 240K -- Improve RTC reset timing
 EC6-- Page 12 -- Change RP81 pull high power rail to RVCC3 and VCC3 -- A circuit design error
 EC7-- Page 12 -- Change RP80 pul high power rail to RVCC3 -- A circuit design error
 EC8-- Page 12 -- Change RP83 pul high power rail to RVCC3 -- A circuit design error
 EC9-- Page 12 -- Add R551 and pull high to VCC3 -- For fingerprint detect high level supply
 EC10-- Page 12 -- Connect IFPID to SB GPIO25 -- For fingerprint detect
 EC11-- Page 12 -- Change R286,R285,R287 pull high power rail to RVCC3 -- A circuit design error
 EC12-- Page 12 -- Connect KBID0#,KBID1# to SB GPIO19,GPIO21 -- For Keyboard ID detection
 EC13-- Page 12 -- Change RP82 to no-pop -- IRQ14 should be pull high to VCC3
 EC14-- Page 13 -- U34 G19 change connection to from 1.5VSUS to RVCC1.5 -- A circuit design error
 EC15-- Page 13 -- U34 R7,U7 change connection from 1.5VSUS to RVCC1.5 --A circuit design error
 EC16-- Page 13 -- U34 A25 change connect from 1.5VSUS to VCC1.5 -- A circuit design error
 EC17-- Page 13 -- U34 G10,G11 change connection from 1.5VSUS to VCC1.5 -- A circuit design error
 EC18-- Page 18 -- U34 A13,F14,G13,G14 change connection from RVCC3 to VCC3 -- A circuit design error
 EC19-- Page 14 -- Add R539 pull high to VCC3 -- Fix S-Video can not be detected
 EC20-- page 15 -- Change U41 AG26,AK29,AJ30,AG28,AG27 connection from 1.8V to VCC1.8 -- A circuit typo
 EC21-- Page 16 -- Change R204,R201 connection from 1.8V to VCC1.8 -- A circuit typo
 EC22-- Page 20 -- Change D26,D27,D25,D24 footprint -- A footprint error
 EC23-- Page 20 -- Add R542 - R550 -- Seperate current limit resistor to one by one
 EC24-- Page 23 -- Add F7 -- Protect MC_3V overcurrent
 EC25-- Page 23 -- Change CON12 pin 9,10,11,12 connection to SM_D7,6,5,4 -- Fix XD card can not be detected
 EC26-- Page 26 -- H11 change footprint -- Mechanical requirement
 EC27-- Page 27 -- Add R445 --Fujitsu suggestion
 EC28-- Page 27 -- Remove VREFOUT from U45 pin30 -- Decrease noise from internal speaker
 EC29-- Page 27 -- Change CON18 footprint -- Fix footprint define error
 EC30-- Page 27 -- Connect C961,C960,C959 to AGND -- Fujitsu suggestion
 EC31-- Page 31 -- Add U58 -- Level up VOLMUTE# high voltage
 EC32-- Page 27 -- R465 change to no-pop -- Prevent voltage level divide by R465
 EC33-- Page 27 -- Change Q32 to DTC144EUA -- Fix PHONEPLG# be pull down by MMBT3904
 EC34-- Page 28 -- Change VREFOUT to 5VAMP/2 --Solve big noise from internal speaker
 EC35-- Page 28 -- Change U57 pin9 to AMP_SHDN
 EC36-- Page 29 -- Change CON23 footprint -- A footprint error
 EC37-- Page 30 -- Change CON17 pin define -- Pin define error
 EC38-- Page 30 -- Change CON26 pin define -- A pin define error
 EC39-- Page 30 -- Add ID pin on CON6 -- Add Keyboard ID detection
 EC40-- Page 30 -- Add R553,R554 -- Provide pull high to KBID0#,KBID1#
 EC41-- Page 30 -- Change CON41 footprint -- Change connector to short type
 EC42-- Page 31 -- Remove SW1 -- Change to Keyboard ID
 EC43-- Page 32 -- 1999PG change to 1632PG -- A circuit design error
 EC44-- Page 33 -- Change PR20,PR30,PR125 footprint to 0603 -- Fix footprint error in A PCBA
 EC45-- Page 33 -- Change PR150 connection to MCHPG -- A circuit design error
 EC46-- Page 33 -- Change PR121,PR122,PR123,PR124,PR126,PR128,PC30,PC127 footprint to 0603 -- Fix footprint error in A PCBA
 EC47-- Page 35 -- Backup PR151,PC160 -- Decrease ripple
 EC48-- Page 36 -- Change FB3 connection to GND -- A circuit design error
 EC49-- Page 36 -- Backup PR152,PC161 -- Decrease ripple
 EC50-- Page 36 -- Change PQ60 to PQ60&PQ61 -- A circuit design error
 EC51-- Page 36 -- Add PC162 -- Decrease ripple
 EC52-- Page 36 -- 12V change to 15V -- A circuit design error
 EC53-- Page 37 -- Add PR153&PR154 connection to CHG -- A circuit design error
 EC54-- Page 37 -- PR52 change to 17.4K and PR132 change to 20K -- Fix total power current

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EC LIST -- B to C test :

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EC55-- Page 04 -- Add thermaltrip circuit -- Solve system can not power on
 EC56-- Page 12 -- Add R566 location and R574 -- Solve HDD and ODD can not be detected issue
 EC57-- Page 12 -- Add R567 location-- Solve HDD and ODD can not be detected issue
 EC58-- Page 22 -- Add C1068 -- Prevent timing error on PCI_PME#
 EC59-- Page 14 -- Add L69, L70, L71 and pop C160,C159,C157 -- EMI request
 EC60-- Page 26 -- R363 change to 33 ohm -- Azalia spec.
 EC61-- Page 27 -- R455 change to 33 ohm -- Azalia spec.
 EC62-- Page 27 -- C870 and C918 change to NO-POP -- To meet impedance requirement
 EC63-- Page 27 -- Remove R559 and change to L67; change C1061location -- EMI request
 EC64-- Page 30 -- Add Q43 -- Change TV tuner power plane to 5V_TV
 EC65-- Page 36 -- PC146 change to 10U/25V -- Improve ripple noise
 EC66-- Page 36 -- PC151 change to 10U/25V -- Improve ripple noise
 EC67-- Page 36 -- PC156 change to 10U/25V -- Improve ripple noise
 EC68-- Page 37 -- PR57 change to NO-POP -- B design error
 EC69-- Page 22 -- C928, C925 change to 22pF -- Improve 24.576MHZ clock quality
 EC70-- Page 27 -- Add R568 -- Improve PC-Beep waveform
 EC71-- Page 11 -- Change R369,R449,R463,R462,R367,R458 location and add R569,R570 -- Correct Azalia layout
 EC72-- Page 27 -- Change R451 to 0 ohm -- For EMI debug use
 EC73-- Page 27 -- Change R362 to 0 ohm -- For EMI debug use
 EC74-- Page 11 -- Change CON20 footprint and location-- Improve assembly
 EC75-- Page 28 -- Add R571 0 ohm -- Solve Woofer sound no good
 EC76-- Page 14 -- R86 and R107 change to 100 ohm -- ATI suggestion
 EC77-- Page 27 -- R445, R446 change to no-pop -- Meet driver requirement
 EC78-- Page 22 -- Add R572,R573 -- Remove SMBUS and add pull high
 EC79-- Page 28 -- R555, R556 change to 1K ohm -- Fujitsu suggestion
 EC80-- Page 18 -- Change VRAM VDD bypass capacitor to 0.1uF -- ATI suggestion
 EC81-- Page 19 -- Change VRAM VDD bypass capacitor to 0.1uF -- ATI suggestion
 EC82-- Page 21 -- L2,L3,L4 change to 0 ohm; C26,C27,C28,C8,C9,C10 change to no pop -- EMI request
 EC83-- Page 22 -- remove L52 and change L51 footprint -- EMI request
 EC84-- Page 26 -- Add L68, C1065 location-- EMI request
 EC85-- Page 27 -- Add C1064 -- EMI request
 EC86-- Page 30 -- Add C1066, C1067 -- EMI request
 EC87-- Page 30 -- Add C1063 -- EMI request
 EC88-- Page 12 -- Change R551 to 100K -- Fujitsu suggestion
 EC89-- Page 29 -- Add R575, R576; R233 change to 5.6K -- Solve Toshiba HDD CRC error
 EC90-- Page 27 -- Add L72-- Improve U46 power quality
 EC91-- Page 33 -- Change PU12 power source to 5VPCU-- Improve PU12 power sequence
 EC92-- Page 30 -- Change C679 to 10UF -- Improve IR receiver power quality
 EC93-- Page 30 -- Change C672 to 0603 footprint and move C675,C672 location-- Improve TVtuner power quality
 EC94-- Page 09 -- Change C484 and C886 to 150uF -- Improve 1.5V power quality
 EC95-- Page 09 -- Change DEV_OFF_LAN and DEV_OFF_MINI to GP021,GP023; change KBID0#,KBID1# to GPIO33,GPIO34 -- Design error

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EC LIST -- C to C+ test :

- EC96-- Page 27 -- Add Q44 and D37 -- To solve Headphone POP noise.
EC97-- Page 28 -- Add R536 and R579 -- To solve Internal speaker and Woofer speaker sound unsynchronism when remove Headphone.
EC98-- Page 32 -- Add PC164 1000P -- Filter out noise on HWPG signal
EC99-- Page 33 -- Add PC163 180P -- Filter out noise on MCHPG signal
EC100-- Page 21 -- Add L73,L74,L75 -- EMI solution
EC101-- Page 21 -- Add L76,L77,L78 -- EMI solution
EC102-- Page 21 -- Add C1069 0.1uF 0402 -- EMI solution
EC103-- Page 26 -- Add C1070 0.1uF 0402 -- EMI solution
EC104-- Page 26 -- Add C1071 0.1uF 0402 -- EMI solution
EC105-- Page 33 -- PL16 change to 1.5UH/14A/20m -- solve VGA core over current issue(Already implement on C unit)
EC105-- Page 33 -- ADD PC165 2.2U 1206 and PC144 change to 2.2U 1206 -- machine height limited
EC106-- Page 27 -- Add U60,Q45,R581 and Del Q31--To solve leak the sound when mute PCBEEP .
EC107-- Page 27 -- Add C1072--To solve some volum level noise.

