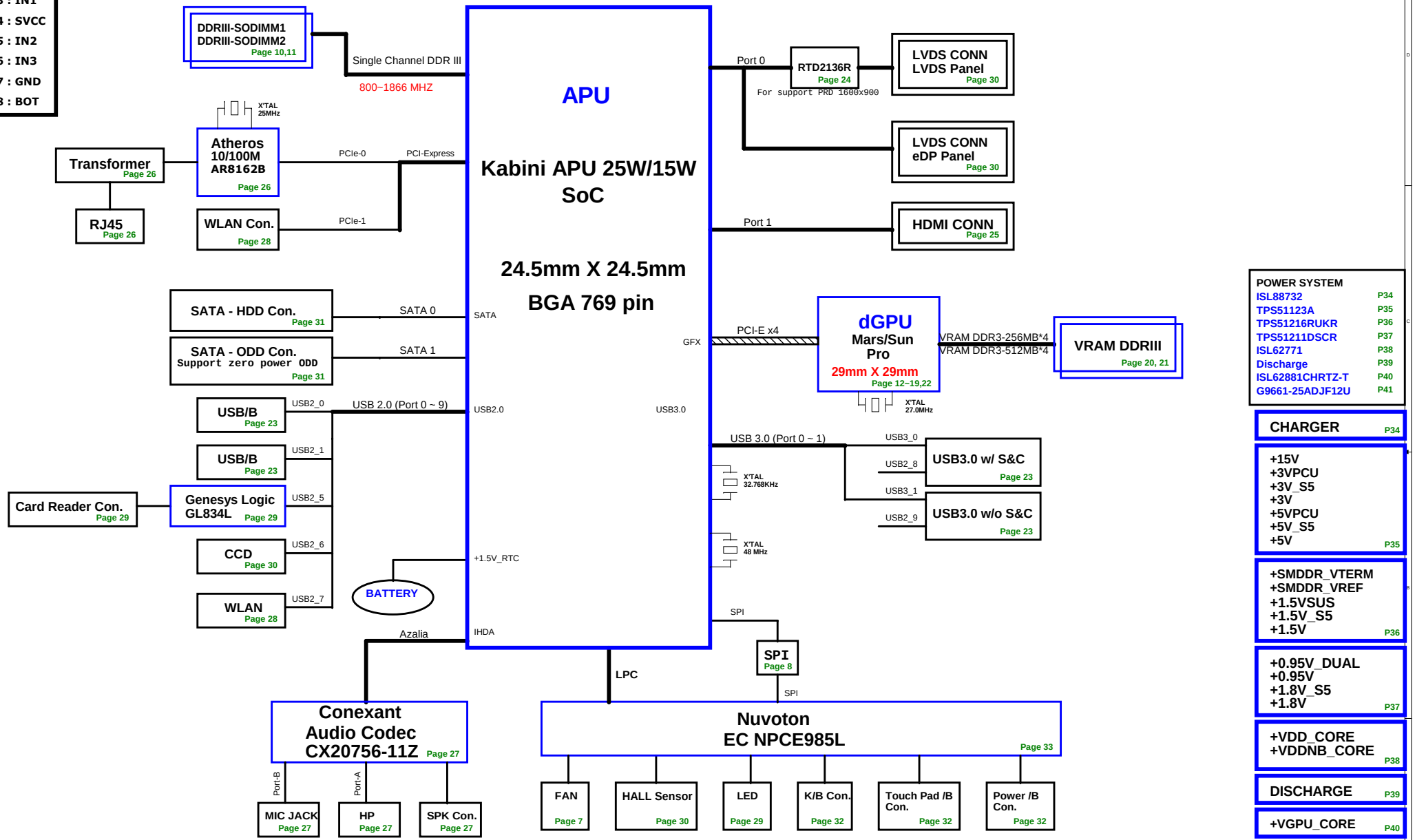
BD9 FT3 Kabini Block Diagram

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : SVCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : GND
- LAYER 8 : BOT



POWER SYSTEM

ISL88732	P34
TPS51123A	P35
TPS51216RUKR	P36
TPS51211DSCR	P37
ISL62771	P38
Discharge	P39
ISL62881CHRTZ-T	P40
G9661-25ADJF12U	P41

CHARGER P34

+15V
+3VPCU
+3V_S5
+3V
+5VPCU
+5V_S5
+5V
P35

+SMDDR_VTERM
+SMDDR_VREF
+1.5VSUS
+1.5V_S5
+1.5V
P36

+0.95V_DUAL
+0.95V
+1.8V_S5
+1.8V
P37

+VDD_CORE
+VDDNB_CORE
P38

DISCHARGE P39

+VGPU_CORE P40

+1.8V_GPU
+1.5V_GPU
+0.95V_GPU
P41

Quanta Computer Inc.
PROJECT : BD9

Size	Document Number	Rev
	Block Diagram	A1A

Date: Tuesday, December 25, 2012 Sheet 1 of 41

Table of Contents

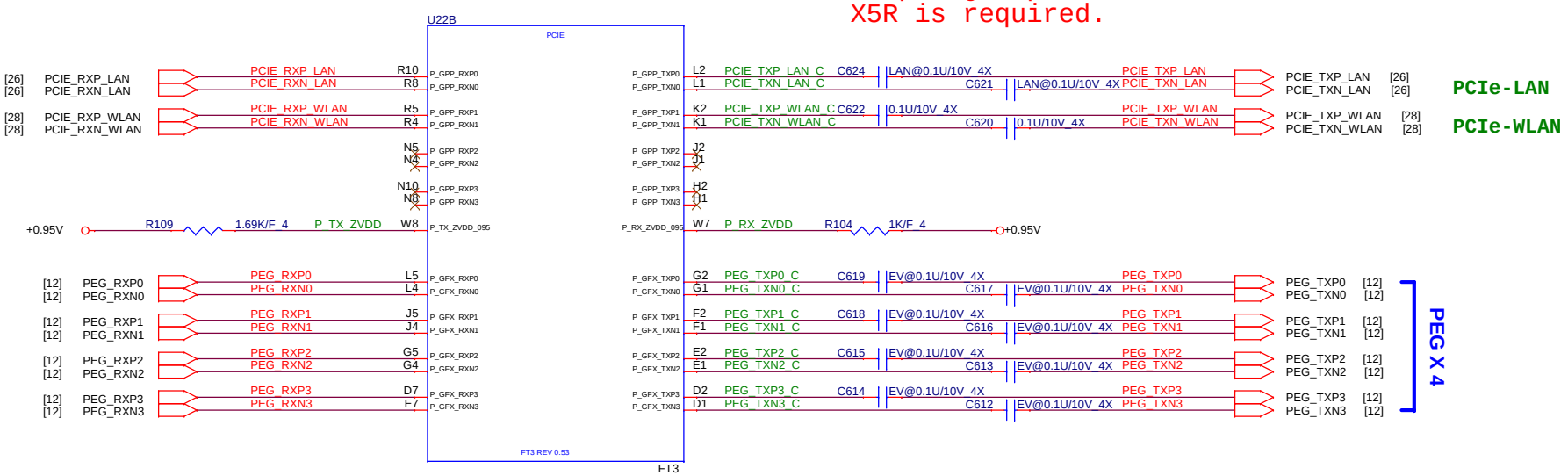
GND PLANE	PAGE
GND_SIGNAL	
8769GND	
GND	ALL
ADOGND	

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+1.5V		S0~S5
+3V	+3.3V	MAIND	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3VPCU	+3.3V	AC/DC Insert enable	S0~S5
+5V	+5V	MAIND	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
+WIMAX_P	+3.3V	IOAC_EN	S0
+1.5VSUS	+1.5V	SUSON	S0~S3
+1.5V	+1.5V	MAIND	S0
+1.8V_S5	+1.8V	PE_PWRGD ^ PE_GPIO1	S0~S5
+0.95V_DUAL	+0.95V	+0.95V_DUAL_EN	S0~S5
+0.95V	+0.95V	MAIND	S0
+VDD_CORE	~	VRON	S0
+VDDNB_CORE	~	VRON	S0
+VGPU_CORE		GPU_MAINON ^ PE_GPIO1	S0
+1.8V_GPU	+1.8V	GPU_MAIND	S0
+0.95V_GPU	+0.95V	GPU_MAINON ^ PE_GPIO1	S0
+3V_GPU	+3.3V	GPU_MAIND	S0
+1.5V_GPU	+1.5V	GPU_MAIND	S0

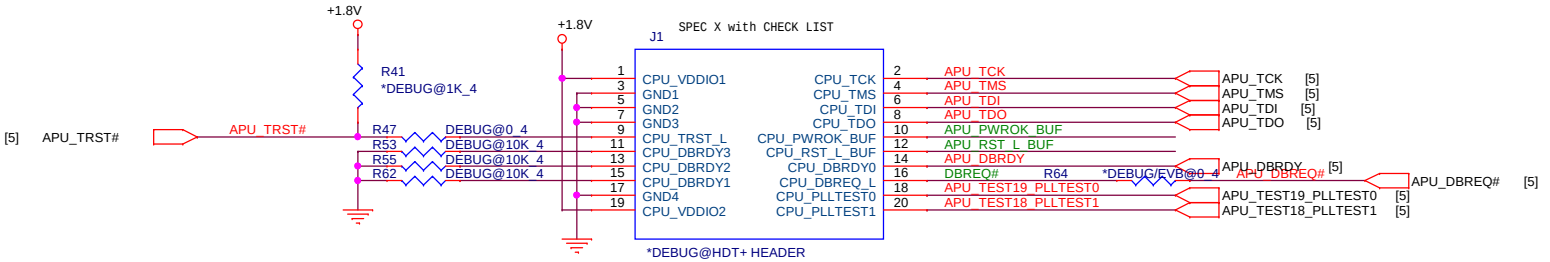
Coupling Caps Note:
X5R is required.

PCIe-LAN

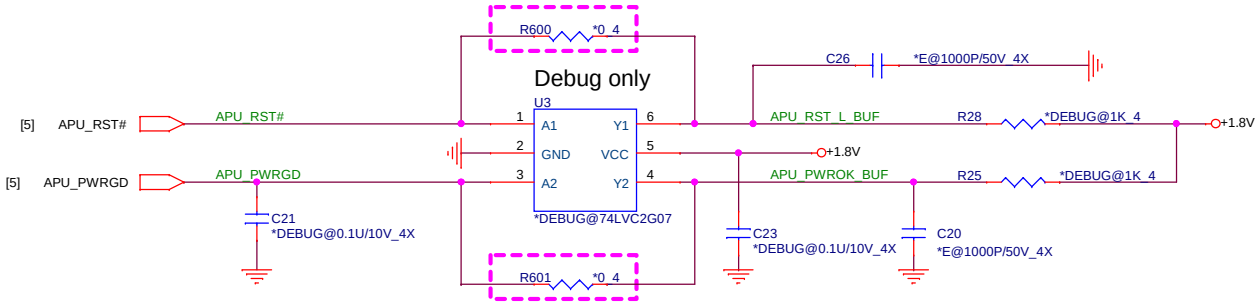
PCIe-WLAN



HDT+ Connector

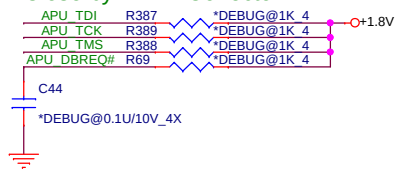


Debug only

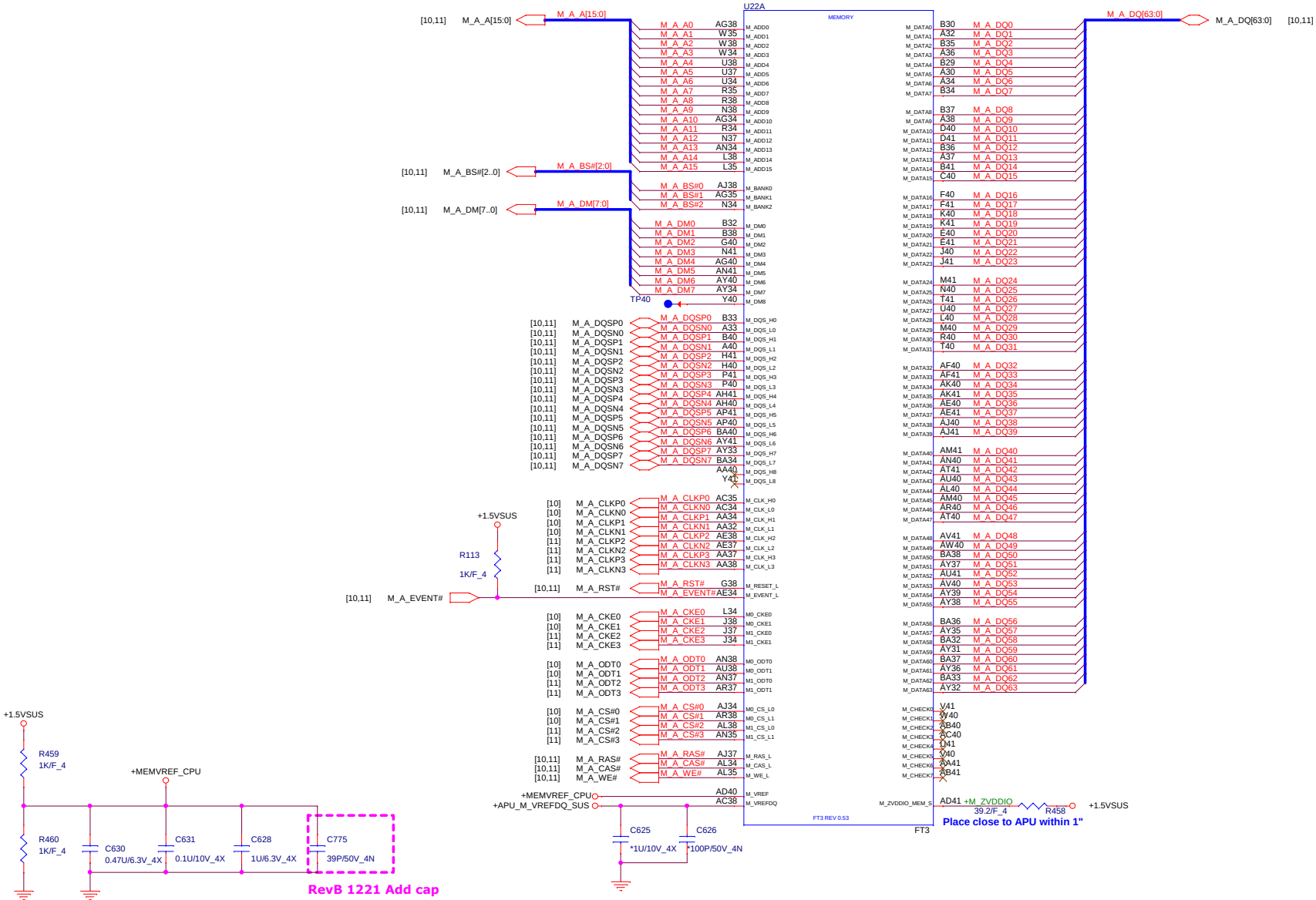


RevB 1221 Add 0 ohm for debug

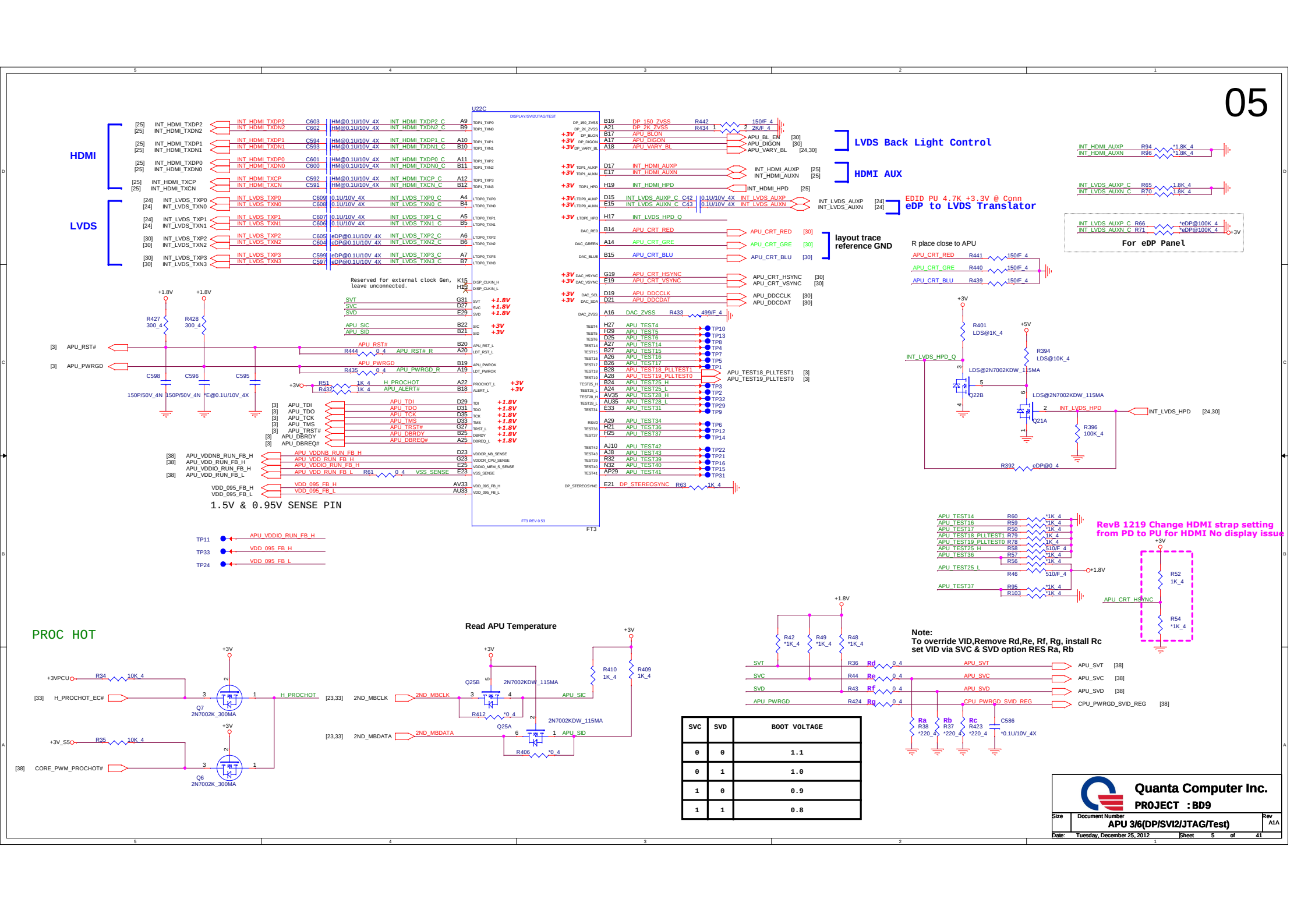
Close by HDT+ Conector



Quanta Computer Inc.		
PROJECT : BD9		
Size	Document Number: APU 1/6(PCIE/GPP)	Rev: A1A
Date: Tuesday, December 25, 2012	Sheet 3 of 41	



Quanta Computer Inc.	
PROJECT : BD9	
Size	Document Number: APU 2/6(DDR3 MEM) — Rev: A1A
Date: Tuesday, December 25, 2012	Sheet 4 of 41



SVC	SVD	BOOT VOLTAGE
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Quanta Computer Inc.
PROJECT : BD9

Size	Document Number	Rev
	APU 3/6(DP/SVI2/JTAG/Test)	A1A

Date: Tuesday, December 25, 2012 Sheet 5 of 41

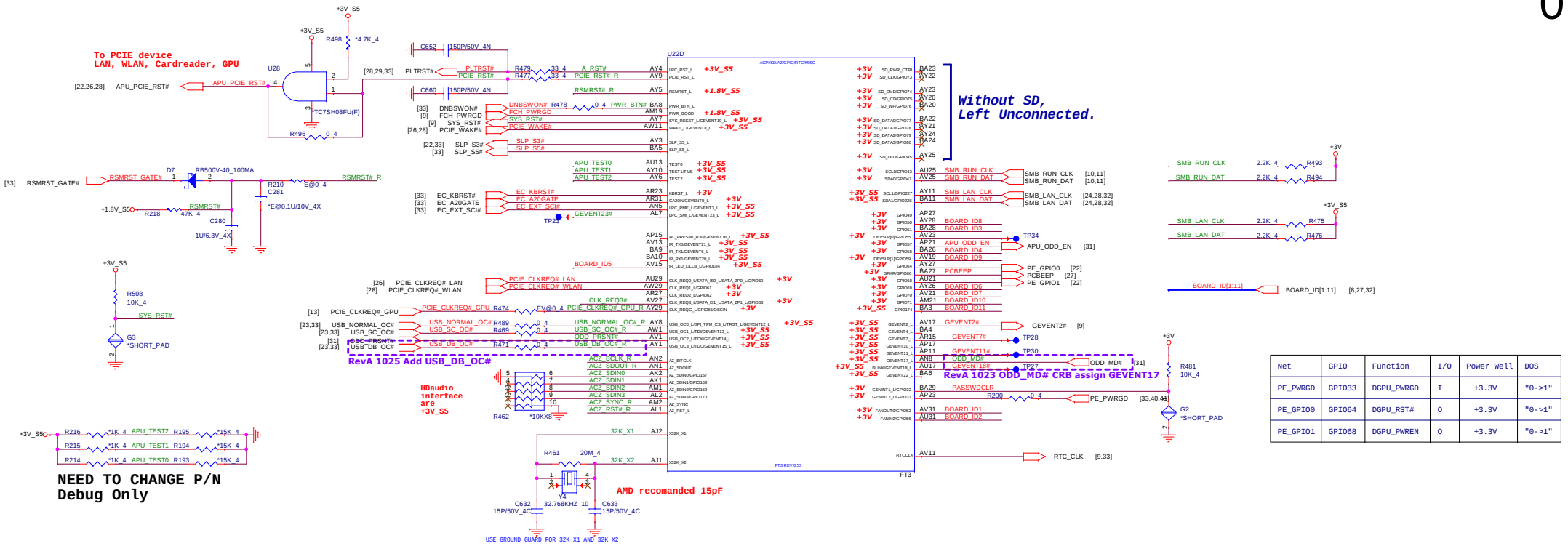
180pF: COG, NP0
Others: X5R

3 A
21 A
17 A
0.1 A
0.5 A
0.2 A
1 A
0.5 A
1.5 A
0.2 A
5 A
0.6 A

RevB 1219 Change from short pad to mount 0805
RevB 1219 Change from short pad to mount 0805
RevB 1219 Change from short pad to mount 0805
RevB 1219 Change from short pad to mount 0805
RevB 1221 Change EV@
RevB 1210 Change P/N to AL000698000
RevB 1219 Change for EOD
RevB 1219 Change for EOD

1.5V level
need a LDO from 3V to 1.5V

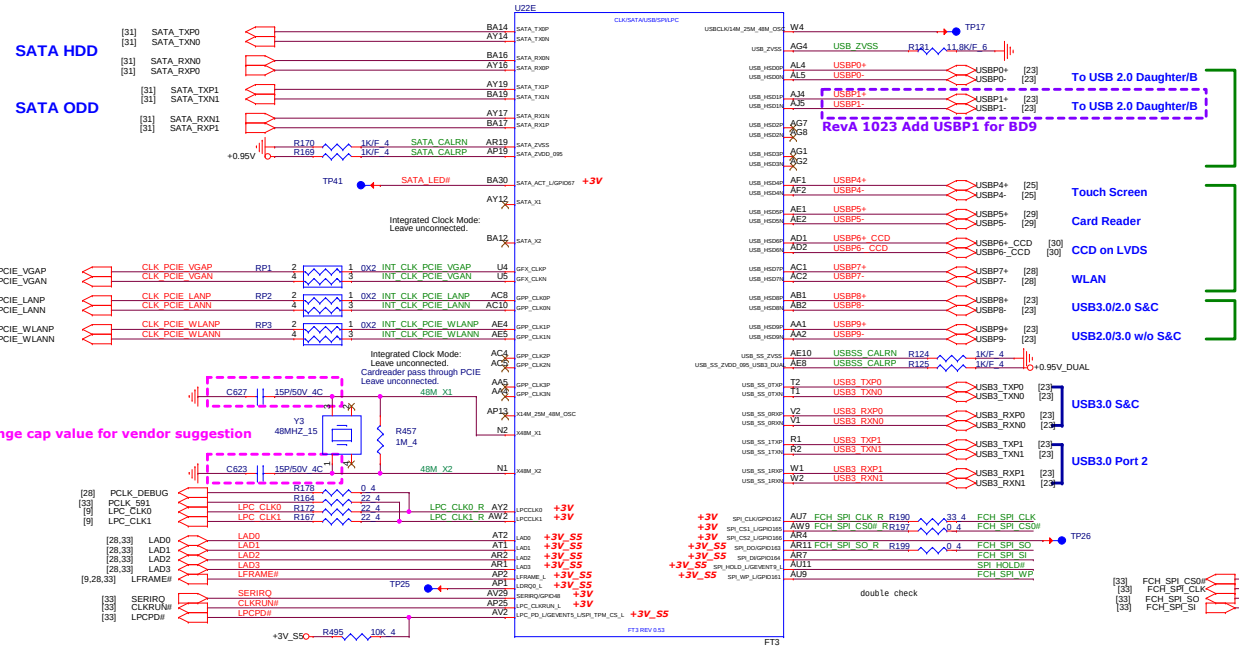
Quanta Computer Inc.			
PROJECT : BD9			
Size	Document Number		Rev
	APU 4/6(POWER/GND/GND)		A1A
Date: Thursday, December 27, 2012	Sheet 6 of 41		

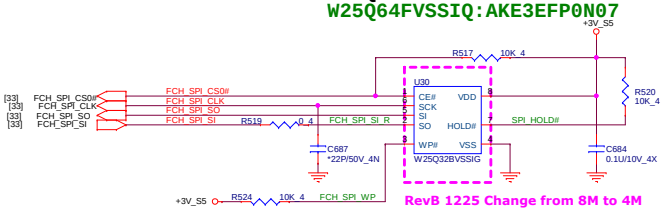


Net	GPIO	Function	I/O	Power Well	DOS
PE_PWRGD	GPIO33	DGPU_PWRGD	I	+3.3V	"0->1"
PE_GPIO0	GPIO64	DGPU_RST#	O	+3.3V	"0->1"
PE_GPIO1	GPIO68	DGPU_PWREN	O	+3.3V	"0->1"

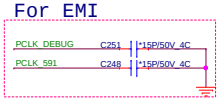
CLK Source	GPP_Clk	Clk_Req	GPIO
GFX	GFX_CLKP/N	Clk_Req6	GPIO65
Lan	GPP_CLK0P/N	Clk_Req0	GPIO60
WLan	GPP_CLK1P/N	Clk_Req1	GPIO61

Quanta Computer Inc.			
PROJECT : BD9			
Size	Document Number		Rev
	APU 5/6(ACPI/SD/AZ/GPIO/RTC/MISC)		A1A
Date: Tuesday, December 25, 2012	Sheet 7 of 41		





For EMI



BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9	ID10	ID11	ID12	ID13
UMA_SKU PX_SKU	H L												
VRAM 1Ghz VRAM 900M		H L											
USB3.0 USB2.0			H L										
14" MTN 17" BD9				H L									
W/O S&C W S&C					H L								
N-METAL (W/O KBLED) METAL (W/ KBLED)						H L							
N-Brand Brand (ONKYO)							H L						
W/O HDMI W HDMI								H L					
N-Brand Brand(Harman/Kardon)									H L				
Metal/IMR TEXTURE										H L			
RSVD RSVD											H L		

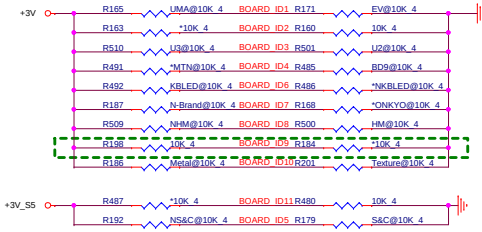
RevB 1221 Modify Board ID

Always PU

Always PU

RevC 0130 Change Board ID setting

Reserve PD

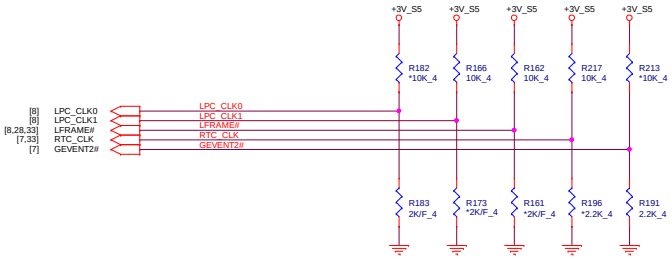


Quanta Computer Inc.
PROJECT : BD9

Size	Document Number	Rev
	APU 6/7(CLK/SATA/USB/SPI)	A1A

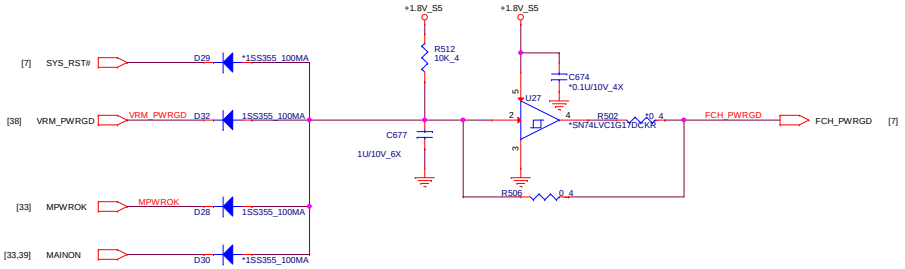
Date: Wednesday, January 30, 2013 Sheet 8 of 41

STRAPS PINS



REQUIRED STRAPS

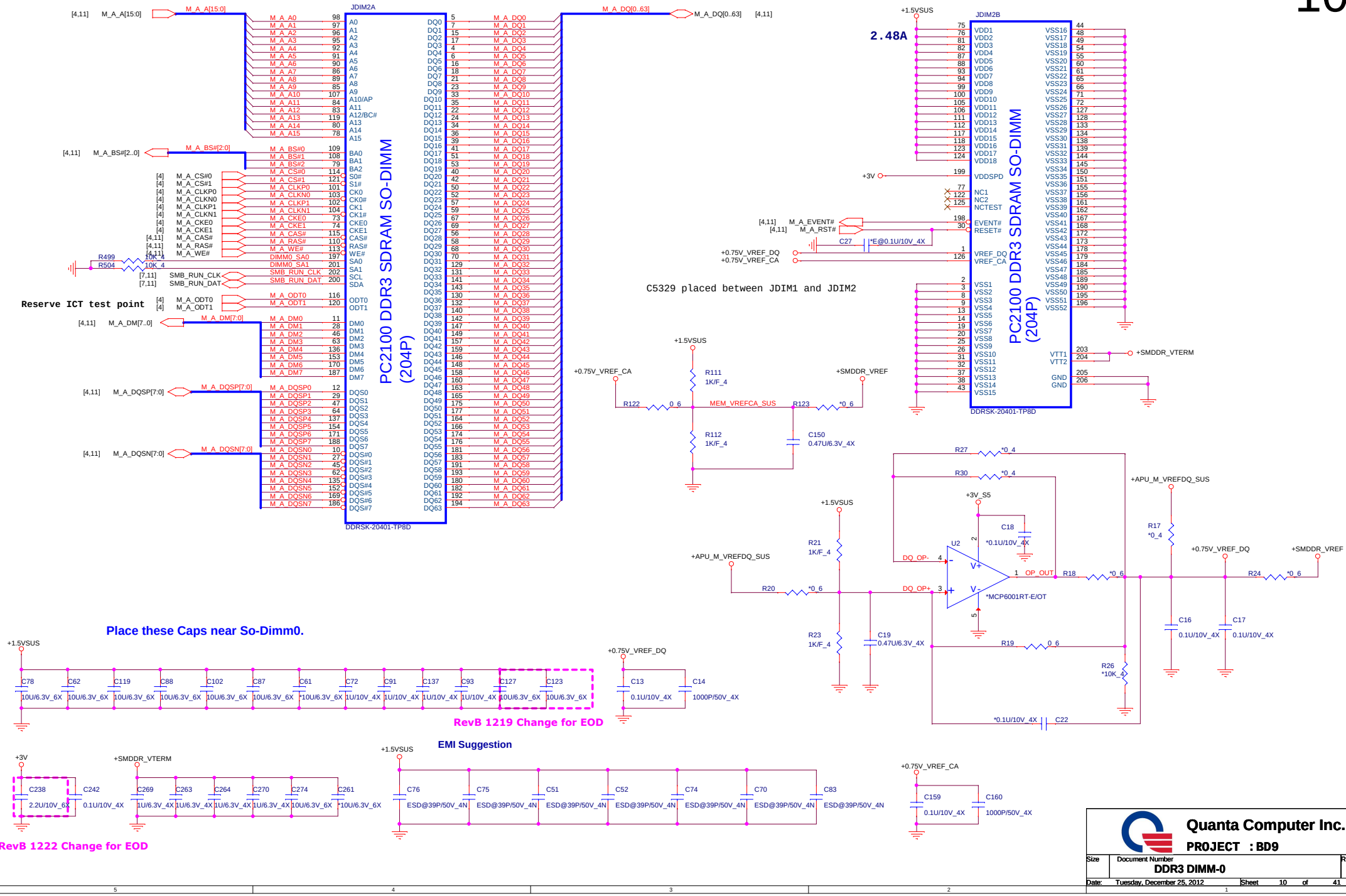
	LPC_CLK0	LPC_CLK1	LFRAME#	RTC_CLK	GEVENT2#
PULL HIGH	BOOT Fail Timer ENABLE	Internal CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT	Normal Power Timing ENABLE DEFAULT	SPI Voltage 1.8V
PULL LOW	BOOT Fail Timer DISABLE DEFAULT	Internal CLKGEN DISABLED	LPC ROM	Normal Power Timing DISABLE	SPI Voltage 3.3V DEFAULT



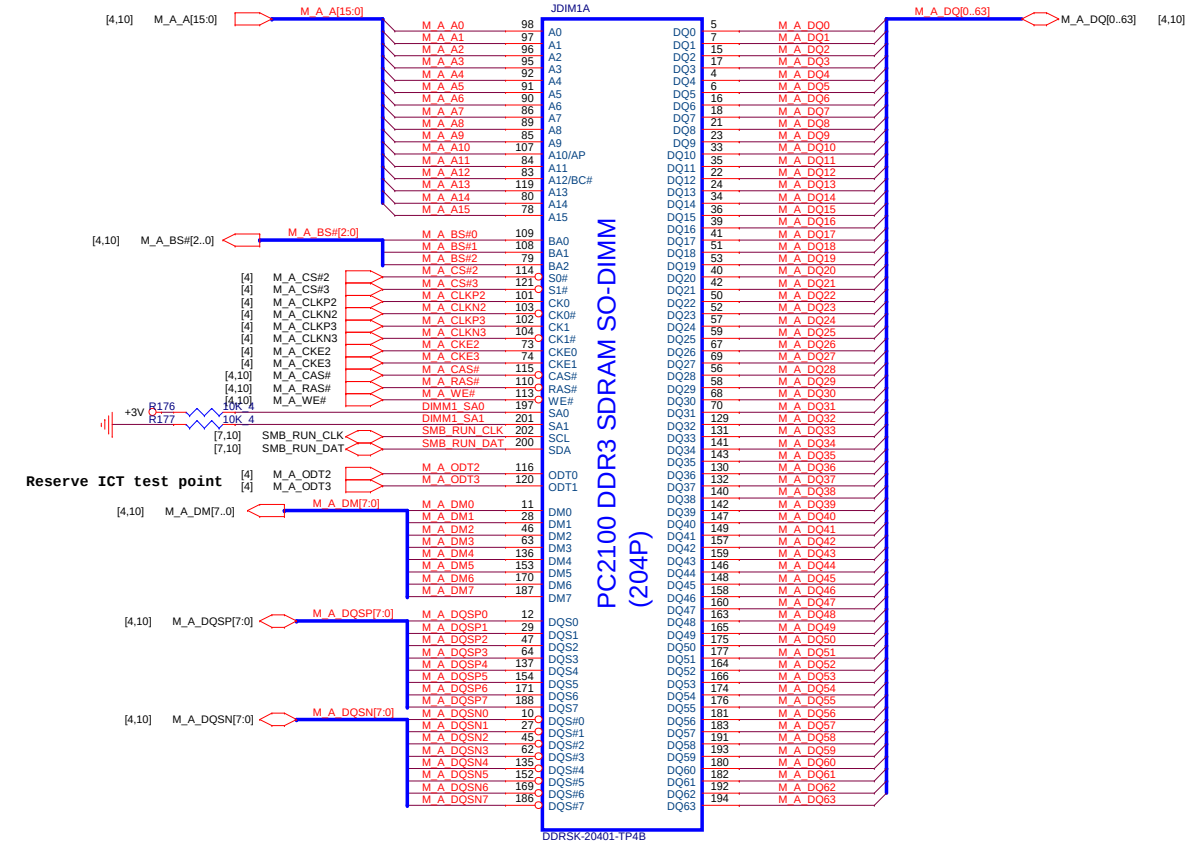
PWRGD CIRCUIT

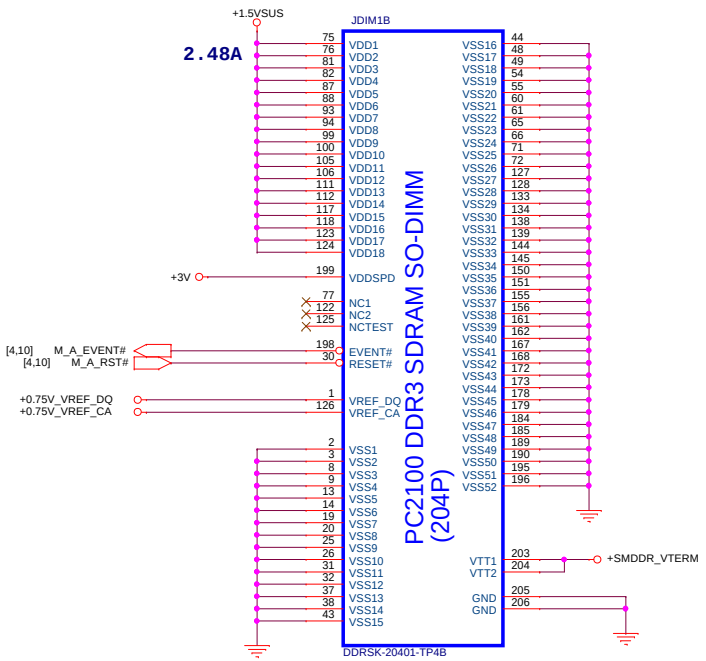
Quanta Computer Inc.	PROJECT : BD9	
Size	Document Number: APU 7/7(STRAP & PWRGD)	Rev: A1A
Date: Tuesday, December 25, 2012	Sheet 9 of 41	

DDR_STD(DDR)

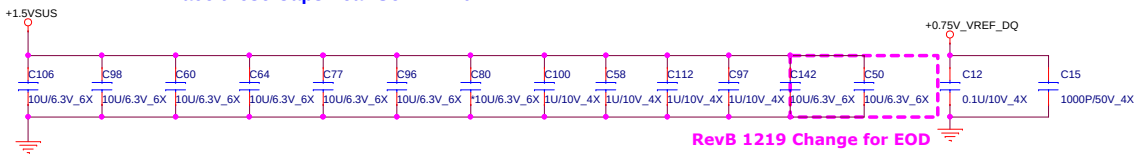

JDIM2A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDRSK-20401-TP8D
JDIM2B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDRSK-20401-TP8D
2.48A
C5329 placed between JDIM1 and JDIM2
Reserve ICT test point
Place these Caps near So-Dimm0.
RevB 1219 Change for EOD
RevB 1222 Change for EOD
EMI Suggestion
*MCP6001RT-E/OT
Quanta Computer Inc.
PROJECT : BD9
DDR3 DIMM-0
Tuesday, December 25, 2012

DDR_STD(DDR)





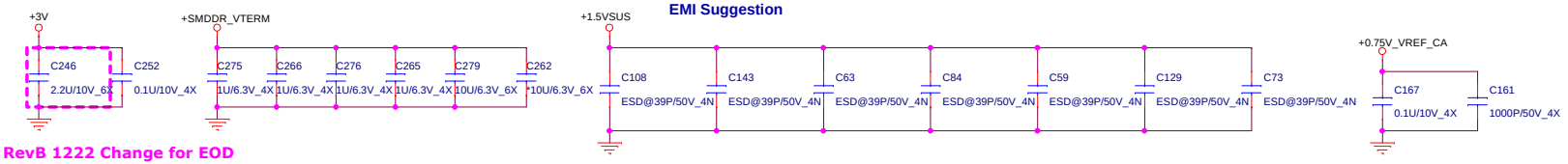
Place these Caps near So-Dimm0.



RevB 1219 Change for EOD

RevB 1219 Change for EOD

EMI Suggestion

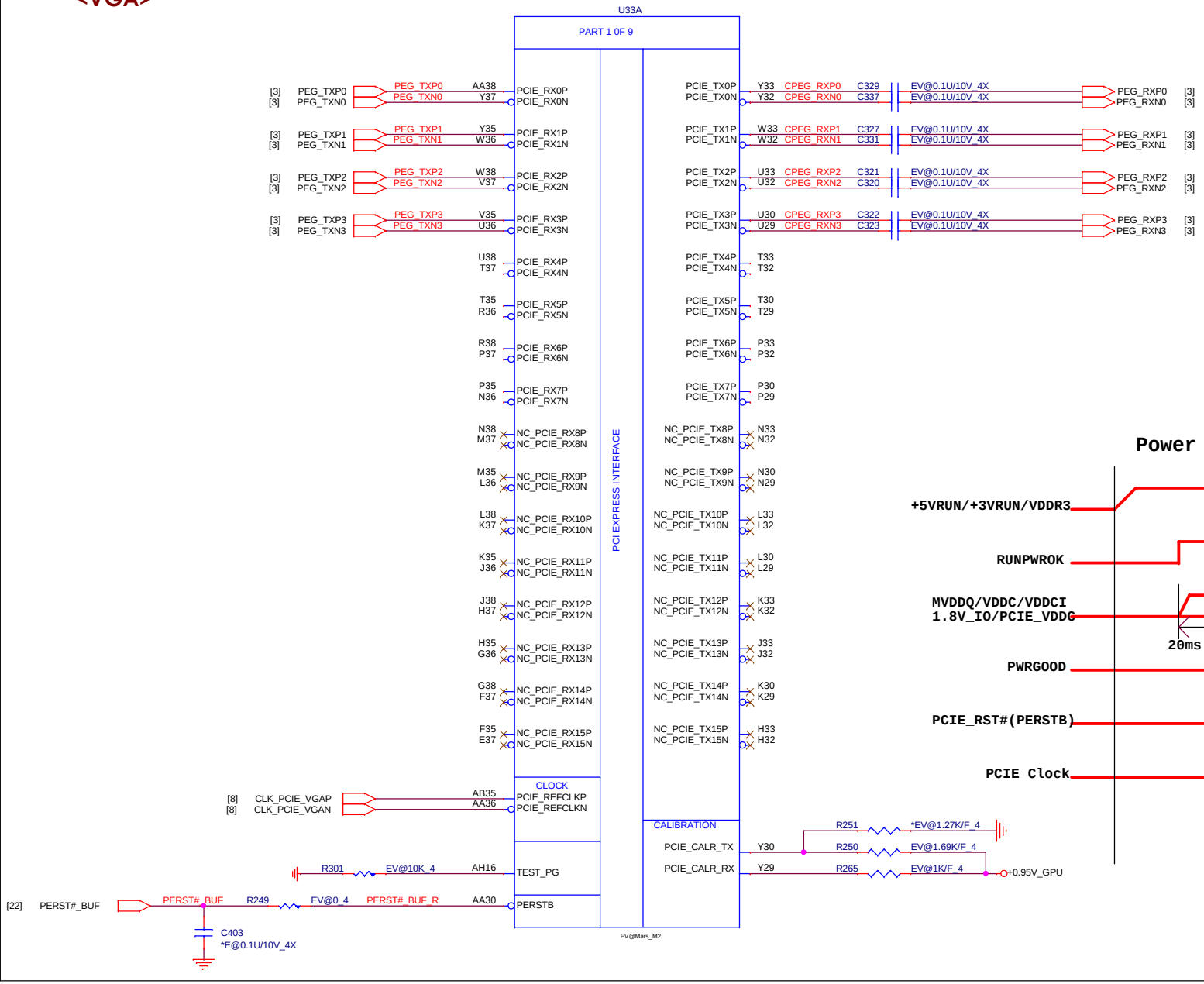


RevB 1222 Change for EOD

Quanta Computer Inc.

PROJECT : BD9

Size	Document Number	Rev
	DDR3 DIMM-1	A1A
Date: Tuesday, December 25, 2012	Sheet 11 of 41	

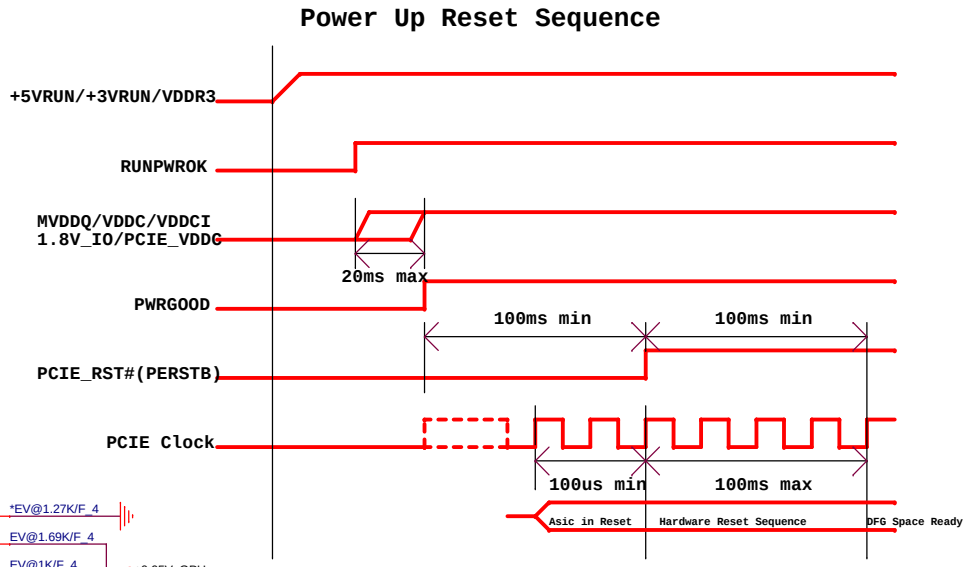


Mars Power-on sequence

1 => +3V_GPU
2 => +VDDC,+VDDCI,+1.5V_GPU,+0.95V_GPU
3 => +1.8V_GPU

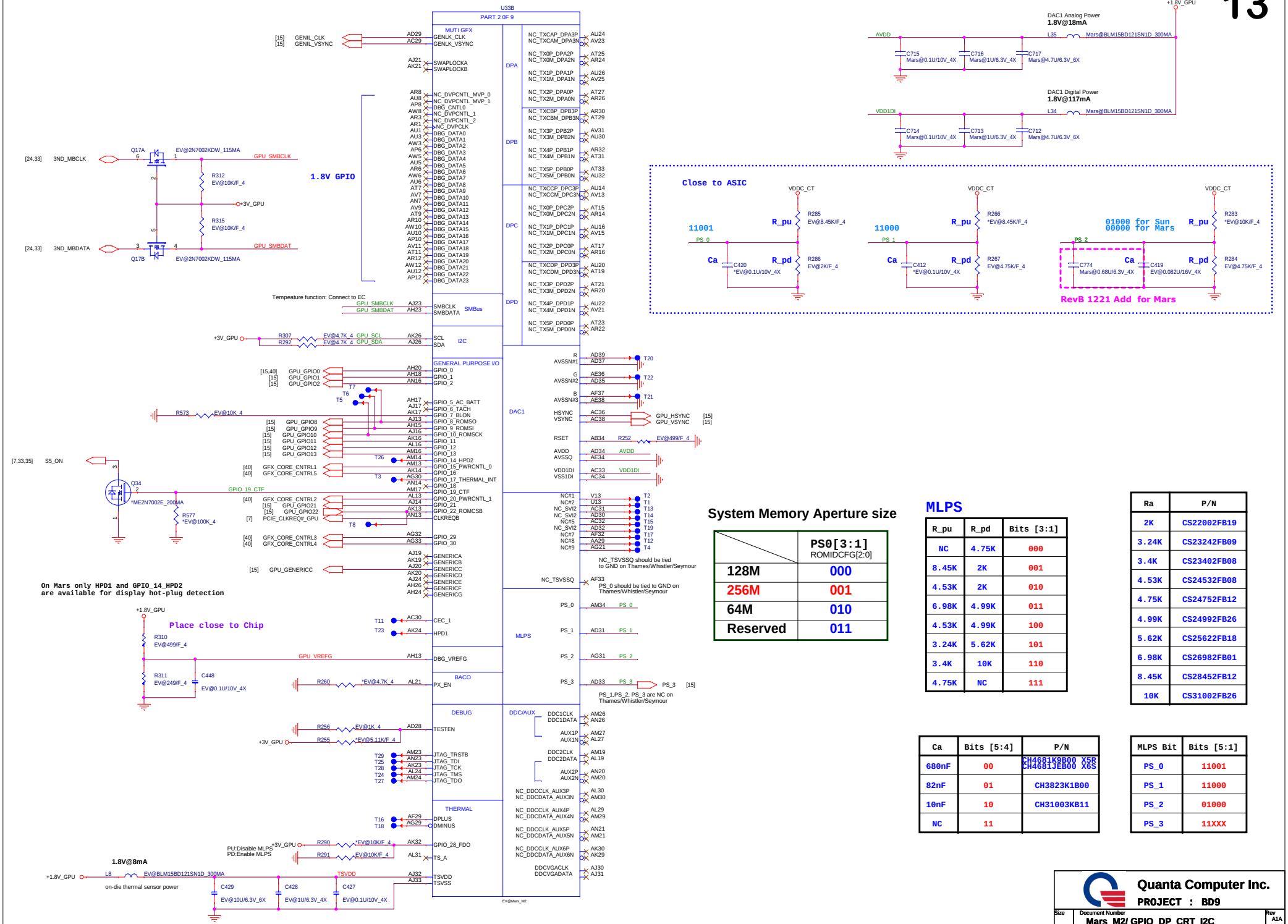
PEG

Intel platform: Lane0 ~ Lane15
Brazos platform: Lane12 ~ Lane15
Comal and Sabine platform: Lane8 ~Lane15
Richland and Kabini platform: Lane0 ~ Lane7



Quanta Computer Inc.
PROJECT : BD9

Size	Document Number	Rev
	Mars_M2/ PEG*8	A1A
Date: Tuesday, December 25, 2012	Sheet 12 of 41	



System Memory Aperture size

	PS0[3:1] ROMIDCFG[2:0]
128M	000
256M	001
64M	010
Reserved	011

MLPS

R_pu	R_pd	Bits [3:1]
NC	4.75K	000
8.45K	2K	001
4.53K	2K	010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	10K	110
4.75K	NC	111

Ra	P/N
2K	CS22002FB19
3.24K	CS23242FB09
3.4K	CS23402FB08
4.53K	CS24532FB08
4.75K	CS24752FB12
4.99K	CS24992FB26
5.62K	CS25622FB18
6.98K	CS26982FB01
8.45K	CS28452FB12
10K	CS31002FB26

Ca	Bits [5:4]	P/N
680nF	00	CH4681K9B00 X5R CH4681JEB00 X6S
82nF	01	CH3823K1B00
10nF	10	CH31003KB11
NC	11	

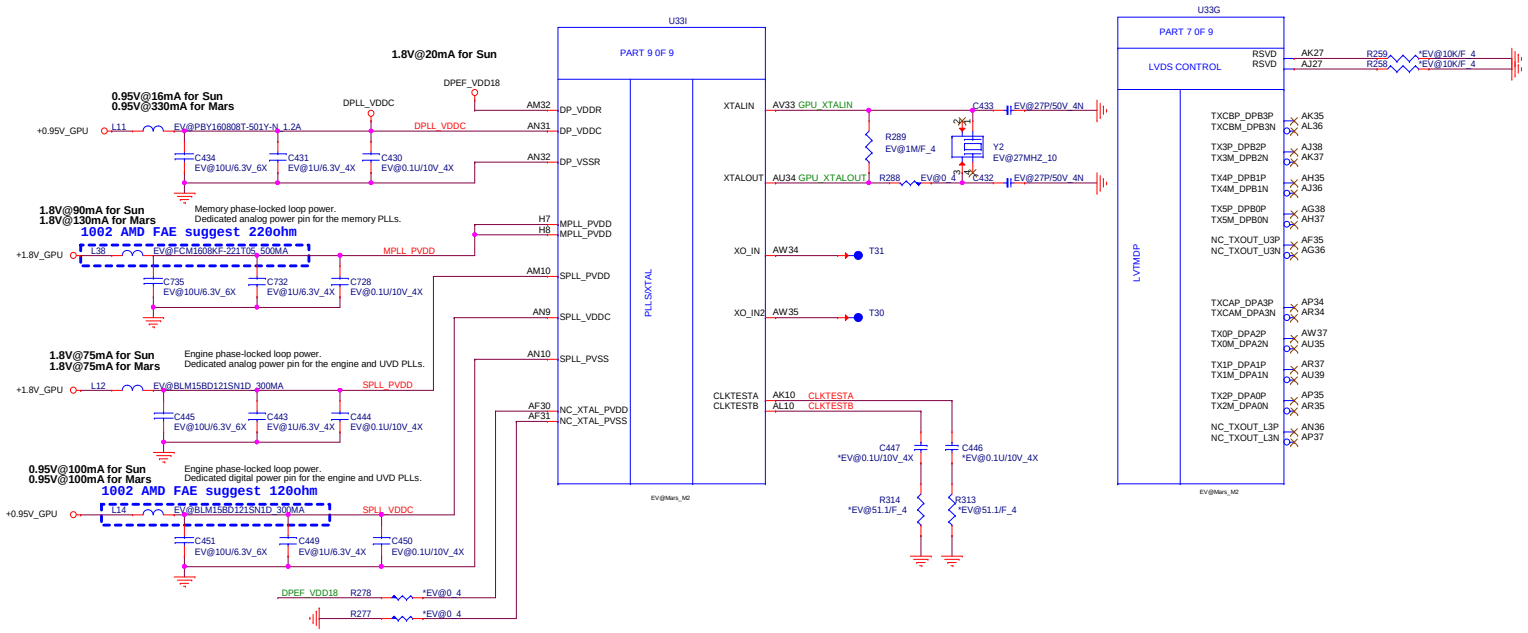
MLPS Bit	Bits [5:1]
PS_0	11001
PS_1	11000
PS_2	01000
PS_3	11XXX

Quanta Computer Inc.
PROJECT : BD9

Size	Document Number	Rev
	Mars_M2/ GPIO_DP_CRT_I2C	A1A

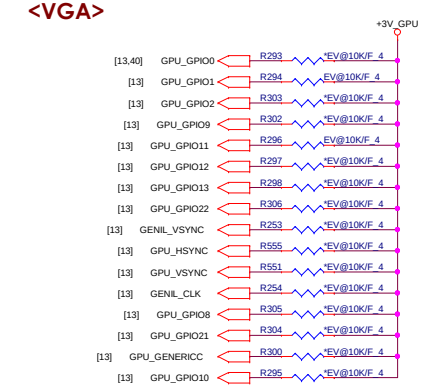
Date: Wednesday, January 30, 2013 Sheet 13 of 41

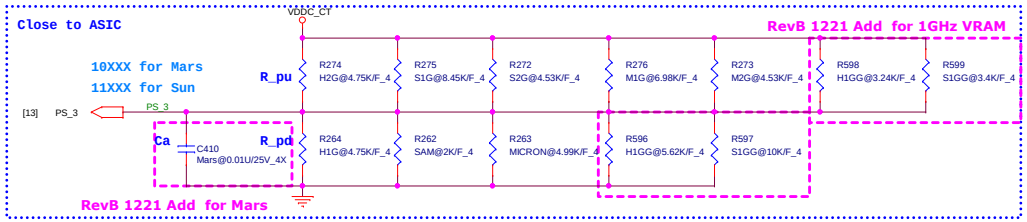
DPE/DPF/LVDS



Quanta Computer Inc.		
PROJECT : BD9		
Size	Document Number: Mars_M2/ XTAL_LVDS	Rev: A1A
Date: Tuesday, December 25, 2012	Sheet 14 of 41	

<VGA>





MLPS

R_pu	R_pd	Bits [3:1]
NC	4.75K	000
8.45K	2K	001
4.53K	2K	010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	10K	110
4.75K	NC	111

Ca	Bits [5:4]	P/N
680nF	00	CH4681K9B00
82nF	01	CH3823K1B00
10nF	10	CH31003KB11
NC	11	

Ra	P/N
2K	CS22002FB19
3.24K	CS23242FB09
3.4K	CS23402FB08
4.53K	CS24532FB08
4.75K	CS24752FB12
4.99K	CS24992FB26
5.62K	CS25622FB18
6.98K	CS26982FB01
8.45K	CS28452FB12
10K	CS31002FB26

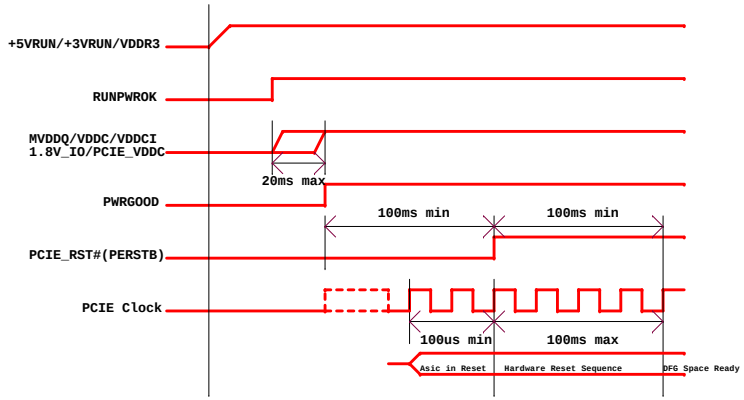
DDR3 Memory TYPE

Vendor	Vendor P/N	B/S P/N (QCI P/N)	Size	MLPS
Hynix	H5TQ2G63DFR-11C (128M*16)	AKD5MGWTW16 * 4	1GB	000
	H5TC4G63AFR-11C (256M*16)	AKD5PGWTW05 * 4	2GB	111
Micron	MT41J128M16JT-107G:K (128M*16)	AKD5DGSTL00 * 4	1GB	011
	MT41K256M16HA-107G:E (256M*16)	AKD5PGSTL00 * 4	2GB	100
Samsung	K4W2G1646E-BC11 (128M*16)		1GB	001
	K4W4G1646B-HC11 (256M*16)		2GB	010

CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED,
THEY MUST NOT CONFLICT DURING RESET

STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	0
STRAP_TX_CFG_DRV_FULL_SWING	PS_1[4]		Control the transmitter full-/half- swing mode 0: 50% Tx output swing 1: Full Tx output swing	1
STRAP_TX_DEEMPH_EN	PS_1[5]		PCIe transmitter, de-emphasis enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
STRAP_BIF_GEN3_EN_A	PS_1[1]		PCIe GEN3 Capability 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	0 for Kabini
STRAP_BIF_VGA_DIS	PS_2[4]		VGA disable determines whether or not the card will be recognized as the system's VGA controler (through the SUBCLASS field in the PCI configuration space) 0: VGA controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
ROM_CONFIG[2:0]	PS_0[3..1]		Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
STRAP_BIOS_ROM_EN	PS_2[3]		Enable external BIOS ROM device 0: Disabled 1: Enabled	0
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
N/A	PS_0[4]		Reserved for internal use only. Must be 1 at reset	1
N/A	PS_1[3]	GENLK_CLK	Reserved	0
STRAP_BIF_CLK_PM_EN	PS_1[2]	GPIO8	PCIe reference clock power management capability is reported in the PCI 0: The CLKREQB power management capability is disabled 1: The CLKREQB power management capability is enabled	0
RESERVED RESERVED	NA NA	GPIO21 GENERICC	Reserved Reserved (for Thames/Whistler/Seymour only)	0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

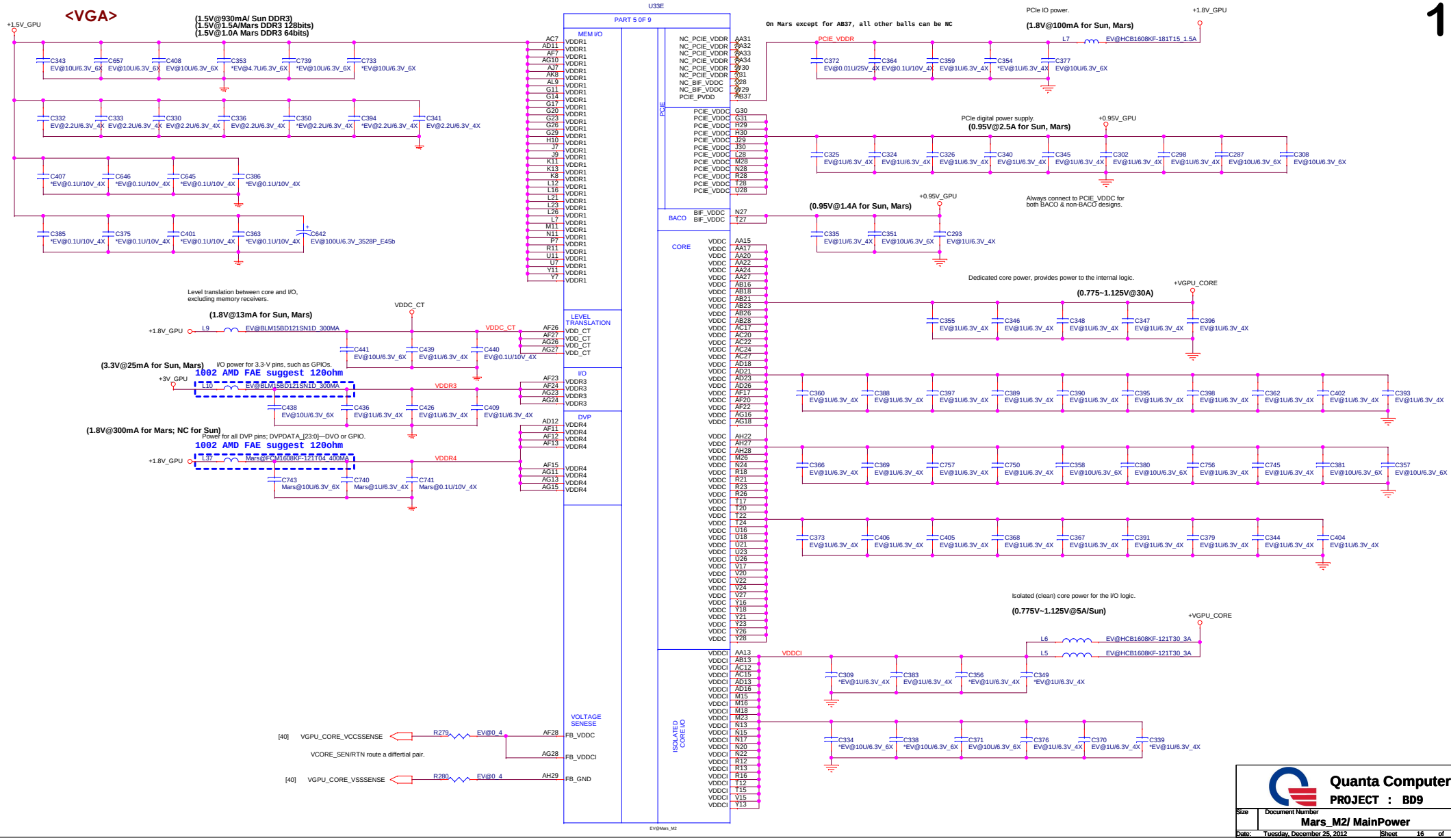
Power Up Reset Sequence

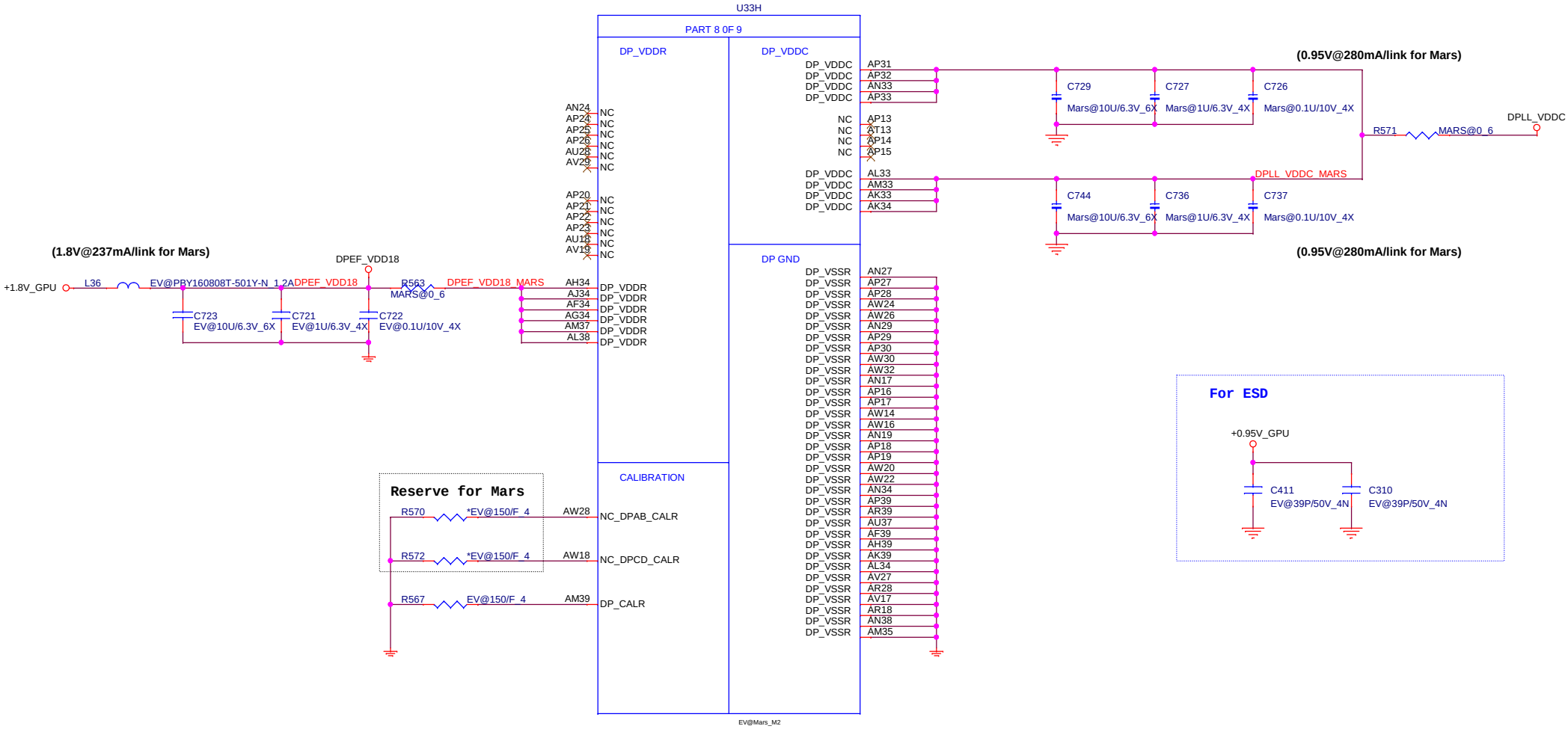


Quanta Computer Inc.
PROJECT : BD9

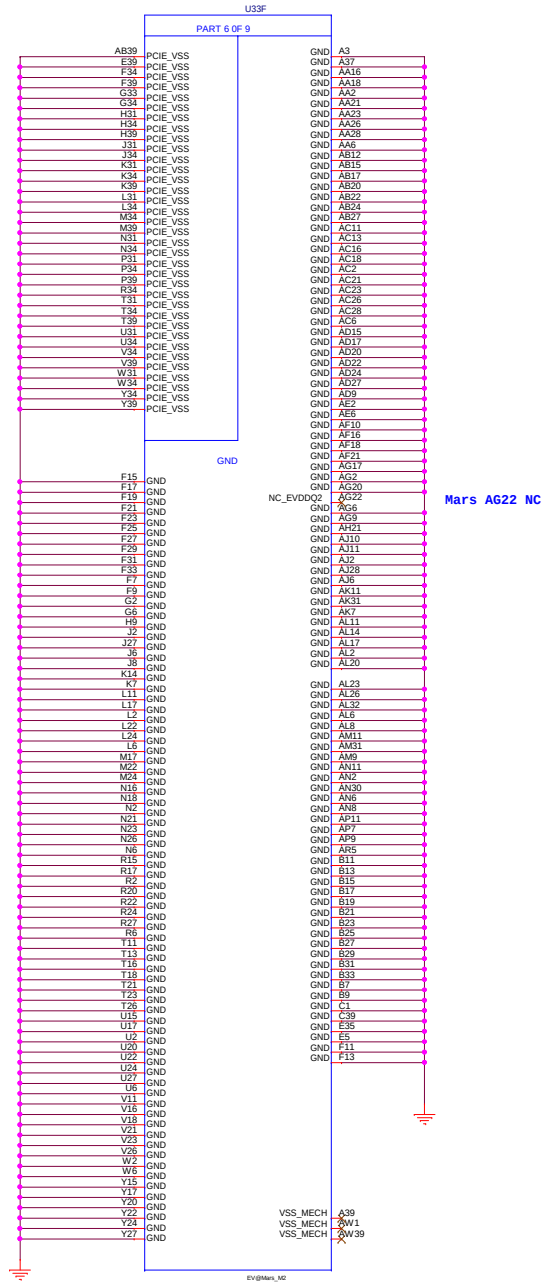
Size	Document Number	Rev
	Mars_M2/ STRAPS_Thermal	A1A

Date: Tuesday, December 25, 2012 Sheet 15 of 41


<VGA>
(1.5V@930mA/ Sun DDR3)
(1.5V@1.5A/Mars DDR3 128bits)
(1.5V@1.0A Mars DDR3 64bits)
+1.5V_GPU
U33E
PART 5 OF 9
MEM I/O
PCIE
BACO
CORE
LEVEL TRANSLATION
I/O
DVP
VOLTAGE SENESE
ISOLATED CORE I/O
On Mars except for AB37, all other balls can be NC
PCIe IO power.
(1.8V@100mA for Sun, Mars)
+1.8V_GPU
PCIE_VDDR
PCIe digital power supply.
(0.95V@2.5A for Sun, Mars)
+0.95V_GPU
Always connect to PCIE_VDDC for both BACO & non-BACO designs.
(0.95V@1.4A for Sun, Mars)
Dedicated core power, provides power to the internal logic.
(0.775~1.125V@30A)
+VGPU_CORE
Isolated (clean) core power for the I/O logic.
(0.775V~1.125V@5A/Sun)
Level translation between core and I/O, excluding memory receivers.
(1.8V@13mA for Sun, Mars)
VDDC_CT
(3.3V@25mA for Sun, Mars)
I/O power for 3.3-V pins, such as GPIOs.
1002 AMD FAE suggest 120ohm
+3V_GPU
(1.8V@300mA for Mars; NC for Sun)
Power for all DVP pins; DVPDATA_[23:0]—DVO or GPIO.
1002 AMD FAE suggest 120ohm
[40] VGPU_CORE_VCCSSENSE
[40] VGPU_CORE_VSSSENSE
VCORE_SEN/RTN route a differtial pair.
FB_VDDC
FB_VDDCI
FB_GND
Quanta Computer Inc.
PROJECT : BD9
Mars_M2/ MainPower
Rev A1A
Date: Tuesday, December 25, 2012
Sheet 16 of 41



Quanta Computer Inc.		
PROJECT : BD9		
Size	Document Number: Mars_M2/ DP_Powers	Rev: A1A
Date: Tuesday, December 25, 2012	Sheet 17 of 41	

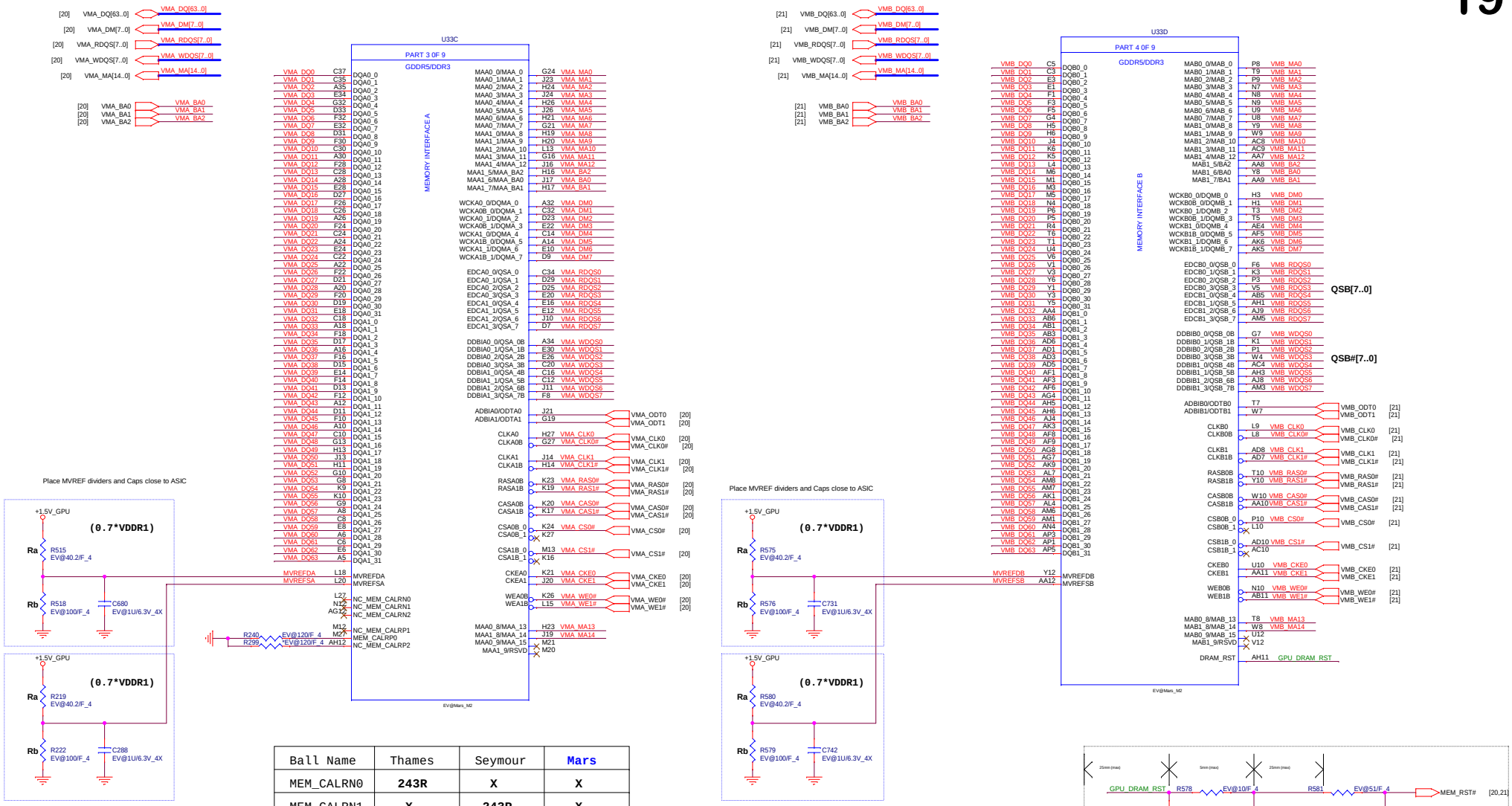


Quanta Computer Inc.

PROJECT : BD9

Size	Document Number	Rev
	Mars_M2/ GND	A1A

Date: Tuesday, December 25, 2012 Sheet 18 of 41



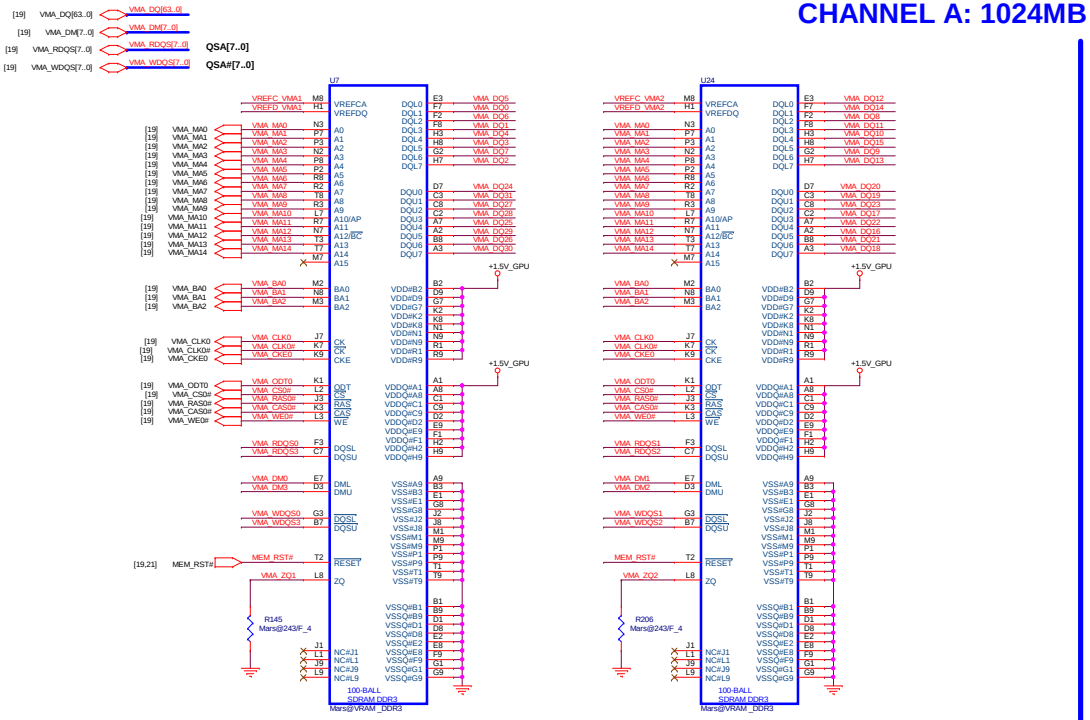
Ball Name	Thames	Seymour	Mars
MEM_CALRN0	243R	X	X
MEM_CALRN1	X	243R	X
MEM_CALRN2	243R	X	X
MEM_CALRP0	243R	X	120R
MEM_CALRP1	X	243R	X
MEM_CALRP2	243R	X	X

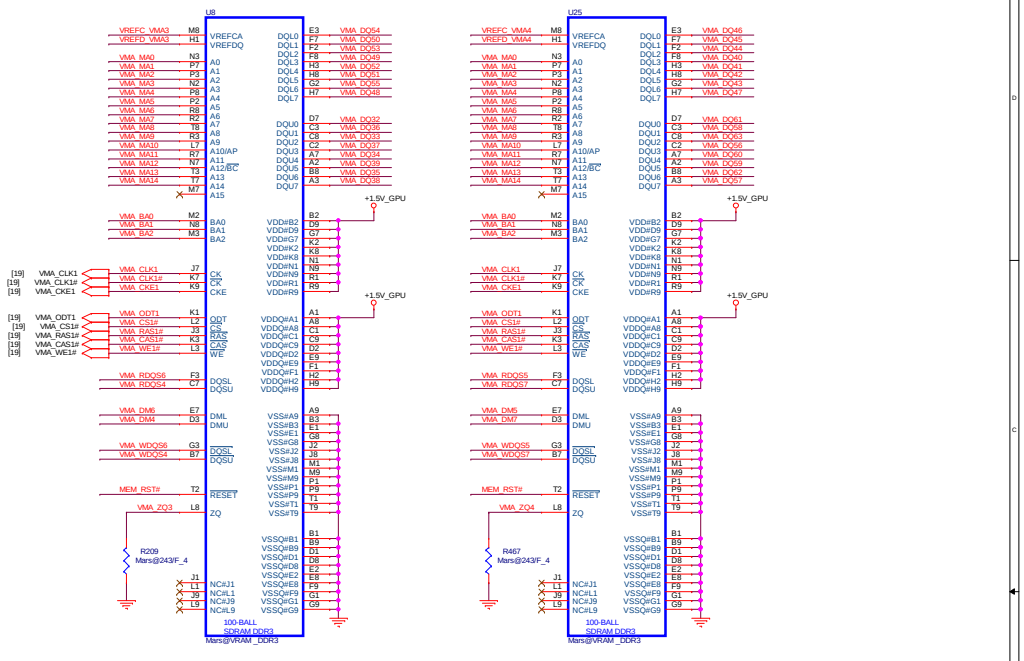
Quanta Computer Inc.
PROJECT : BD9

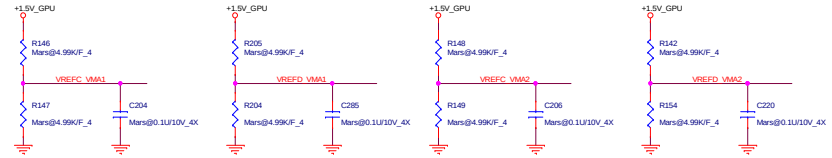
Size	Document Number	Rev
	Mars_M2/ MEM Interface	A1A

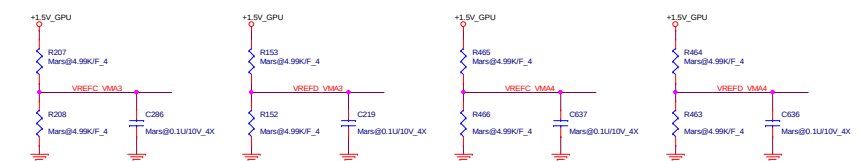
Date: Tuesday, December 25, 2012 Sheet 19 of 41

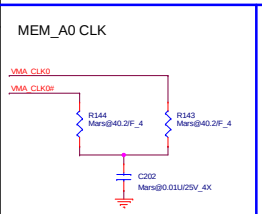
CHANNEL A: 1024MB DDR3 (128M*16*4pcs)<VGA>

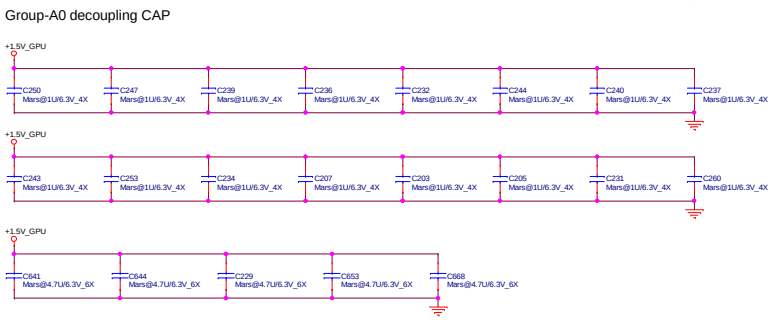


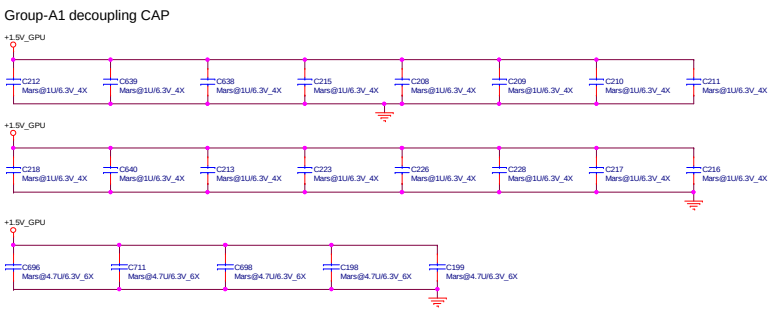


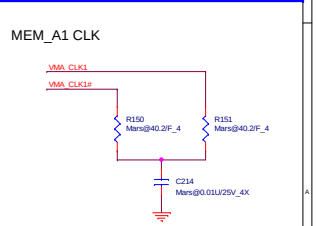










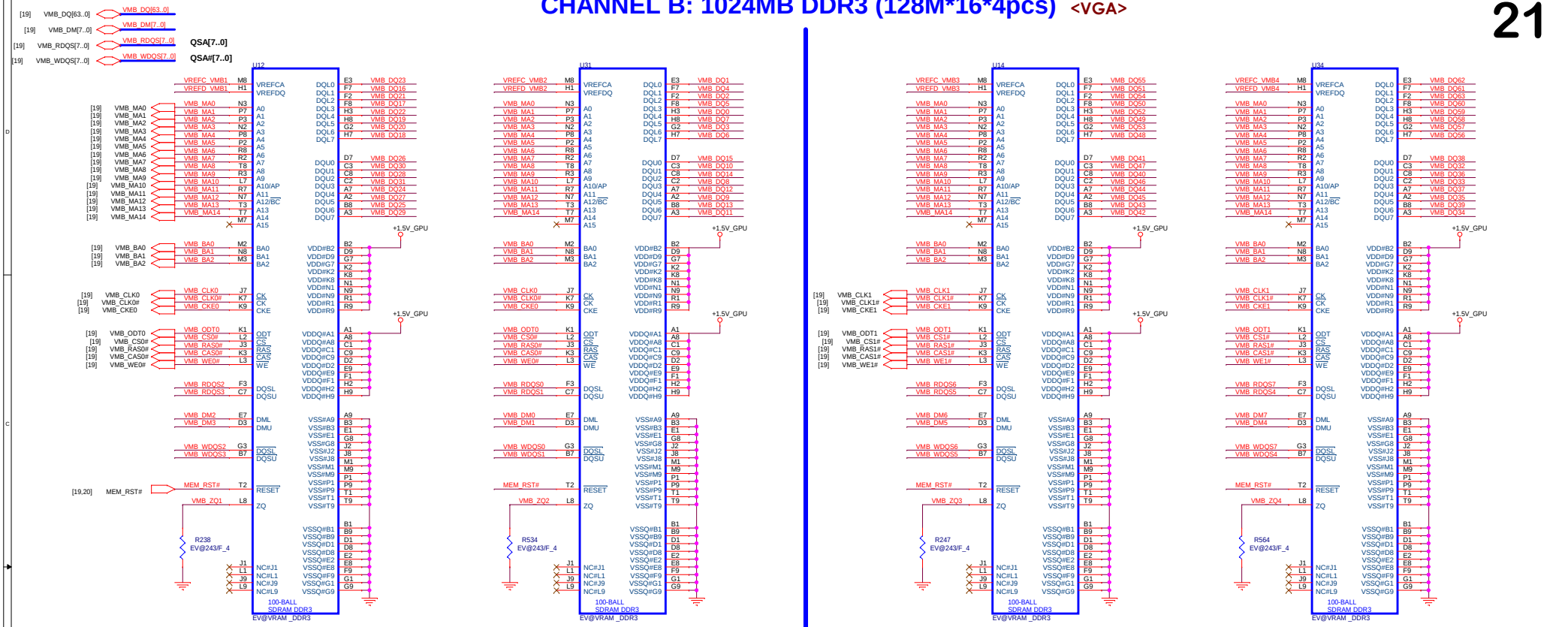


Quanta Computer Inc.
PROJECT : BD9

Size	Document Number	Rev
	VRAM_A: DDR3*4PCS	A1A

Date: Tuesday, December 25, 2012 Sheet 20 of 41

CHANNEL B: 1024MB DDR3 (128M*16*4pcs) <VGA>



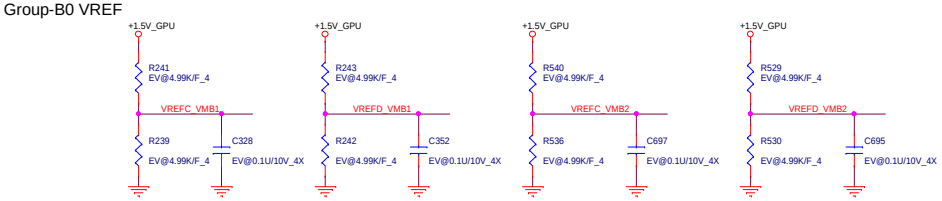
BOT Down

TOP Down

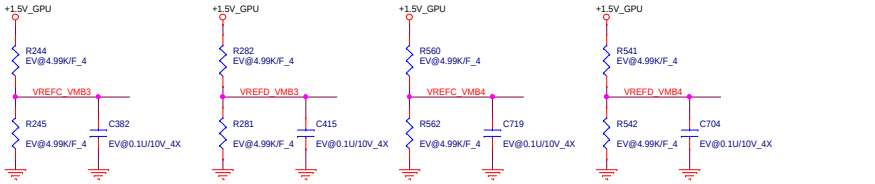
TOP Up

BOT Up

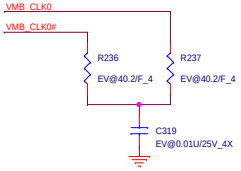
Group-B0 VREF



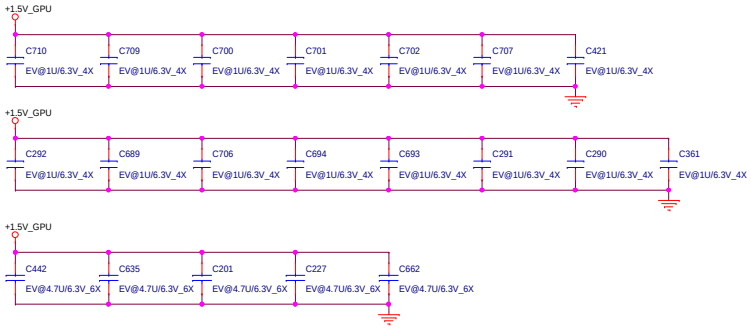
Group-B1 VREF



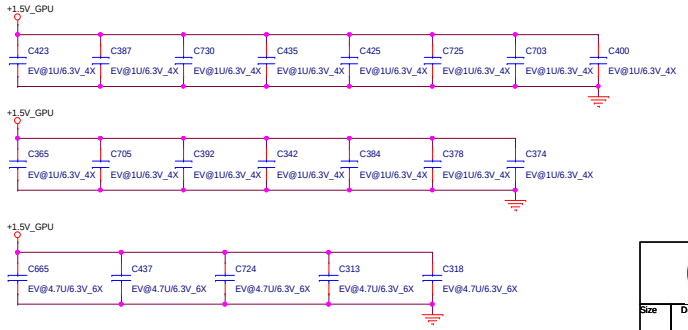
MEM_B0 CLK



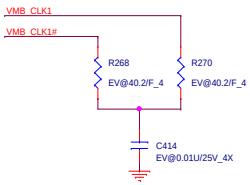
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK

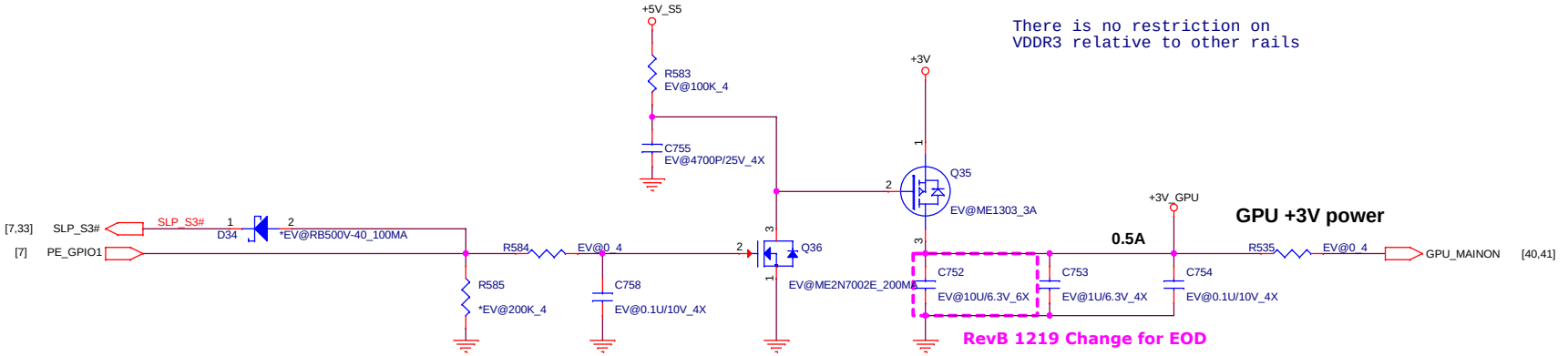


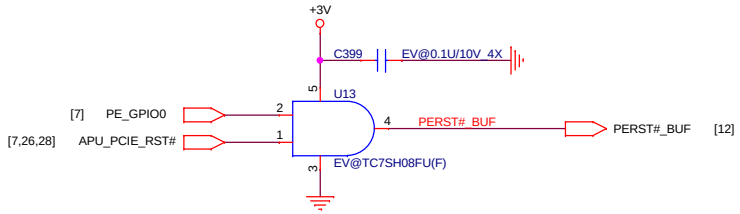
Quanta Computer Inc.

PROJECT : BD9

Size	Document Number	Rev
	VRAM_B: DDR3*4PCS	A1A
Date: Tuesday, December 25, 2012	Sheet 21 of 41	

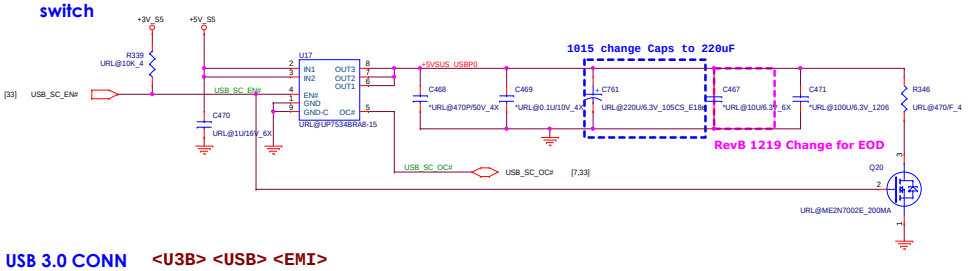
There is no restriction on
VDDR3 relative to other rails





Quanta Computer Inc.		
PROJECT : BD9		
Size	Document Number: Mars_M2/ PX5	Rev: A1A
Date: Tuesday, December 25, 2012	Sheet 22 of 41	

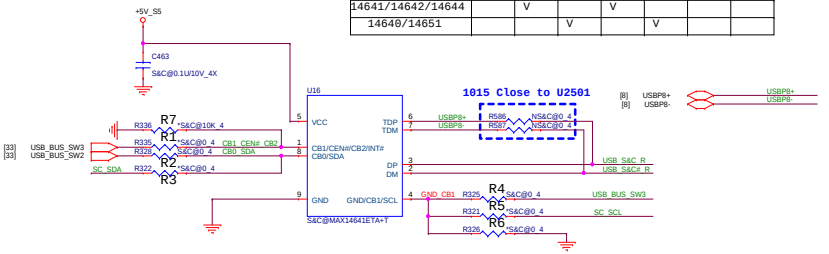
USB 3.0 Power switch <USB> <U3B>



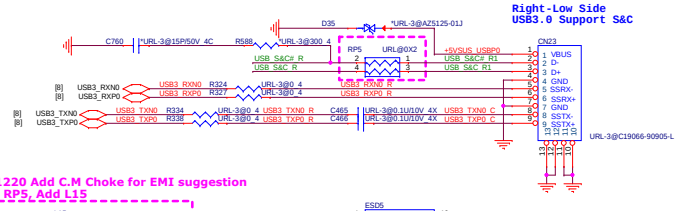
USB w S&C MAXIM solution <SLC>

14566/14600/14617

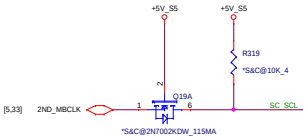
	R1	R2	R3	R4	R5	R6	R7
14566	V	V				V	
14600		V		V			
14617(no CB2)		V		V			V
14641/14642/14644		V		V			
14640/14651			V		V		

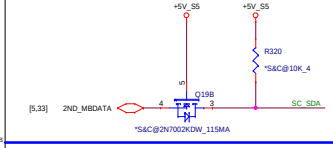


USB 3.0 CONN <U3B> <USB> <EMI>

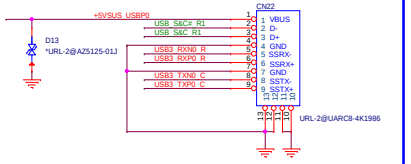


RevB 1220 Add C.M Choke for EMI suggestion
Delete RP5, Add L15





Co-Lay USB 2.0 CONN <USB> <EMI>



RevC 0130 update S&C table

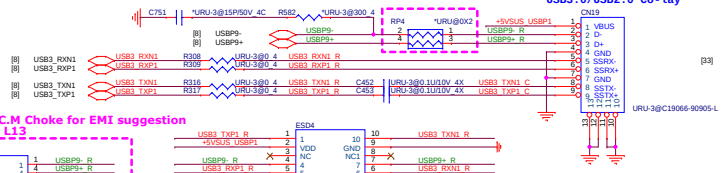
SW2	SW3	14600	
CB0	CB1	Status	
0	0	Auto mode	Charger , AM
0	1	Force dedicated charger mode	Charger , FM
1	0	Pass-Through(USB) mode	USB , PM
1	1	pass-through(USB) with CDP Emulation	USB , CM

SW2	SW3	14641	
CB0	CB1	Status	
0	0	2A Auto mode for Apple device	Charger , AM2
0	**1**	Force 1A for Apple device	Charger , AP1
1	**0**	Pass-Through(USB) mode	USB , PM
1	1	pass-through(USB) with CDP Emulation	USB , CM

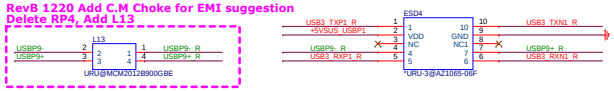
SW2	SW3	14644	
CB0	CB1	Status	
0	0	2A Auto mode for Apple device	Charger , AM2
0	**1**	Force dedicated charger mode	Charger , FM
1	**0**	Pass-Through(USB) mode	USB , PM
1	1	pass-through(USB) with CDP Emulation	USB , CM

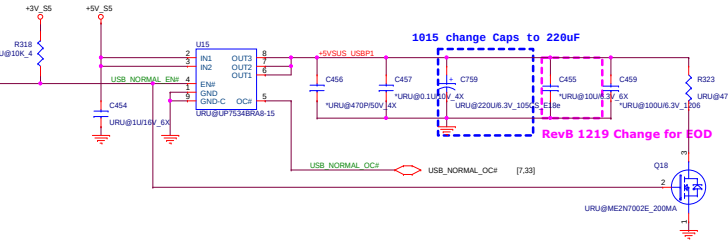
SW2	SW3	14642	
CB0	CB1	Status	
0	X	2A Auto mode for Apple device	Charger , AM2
1	**0**	Pass-Through(USB) mode	USB , PM
1	1	pass-through(USB) with CDP Emulation	USB , CM

USB 3.0 CONN <U3B> <U2B> <EMI>



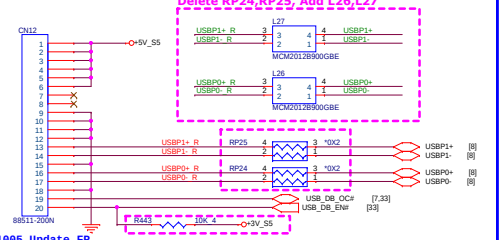
RevB 1220 Add C.M Choke for EMI suggestion
Delete RP4, Add L13





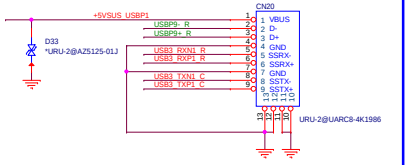
USB 2.0 CONN (USB/B) <U2B> <EMI>

RevB 1220 Add C.M Choke for EMI suggestion
Delete RP24,RP25, Add L26,L27



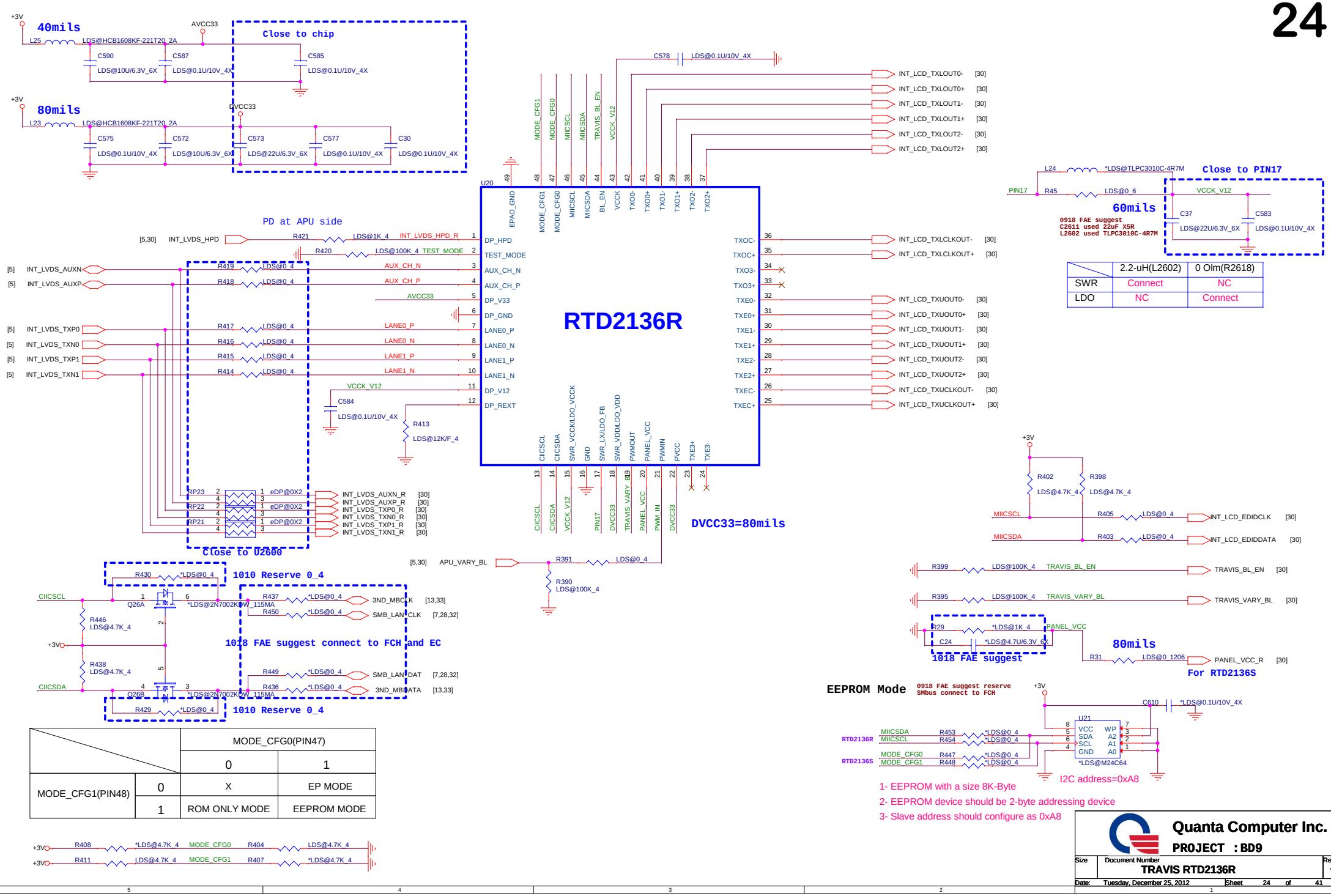
RevB 1130 Change R443 PU from USB_DB_OC# to USB_DB_EN#

Co-Lay USB 2.0 CONN <USB> <EMI>



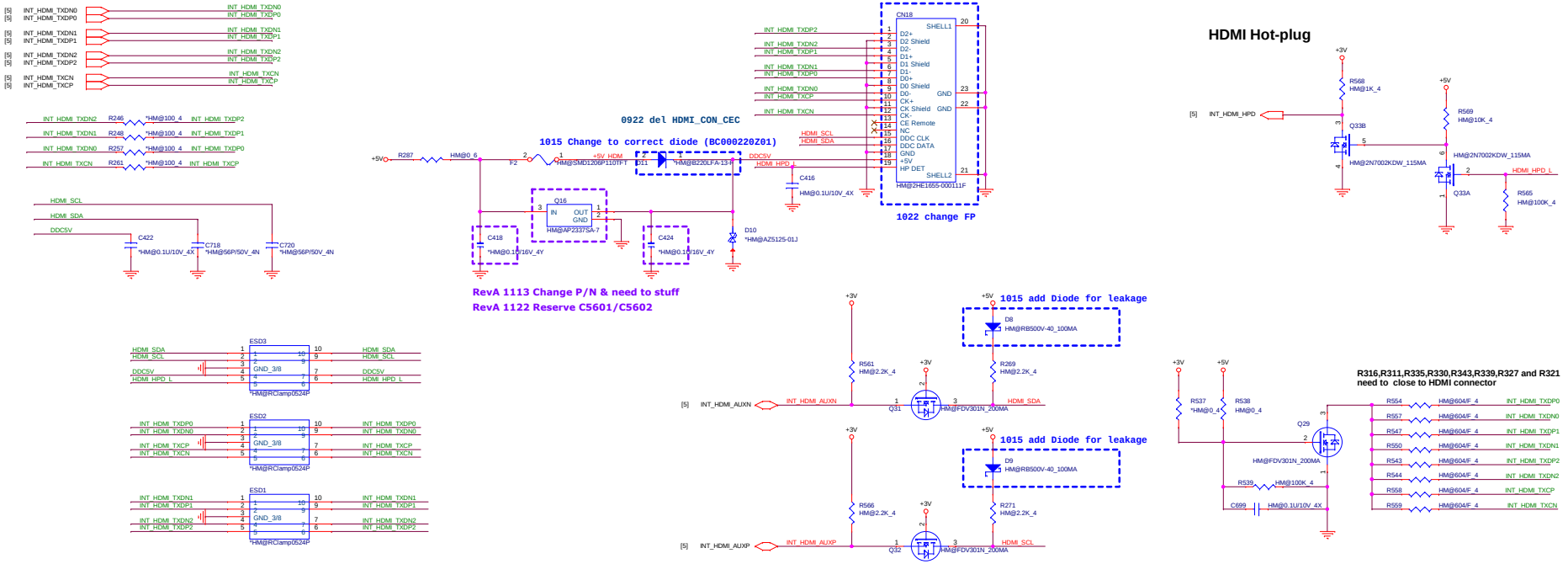
Quanta Computer Inc.
PROJECT :BD9

Size	Document Number	Rev
	USB2.0/USB3.0	A1A
Date: Wednesday, January 30, 2013	Sheet 23 of 41	

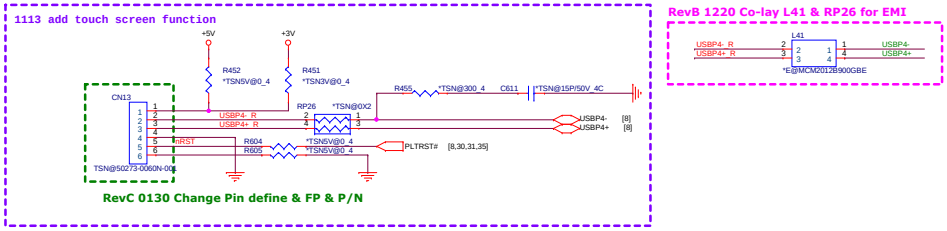


Quanta Computer Inc.		
PROJECT : BD9		
Size	Document Number: TRAVIS RTD2136R	Rev: A1A
Date: Tuesday, December 25, 2012	Sheet 24 of 41	

HDMI

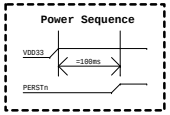


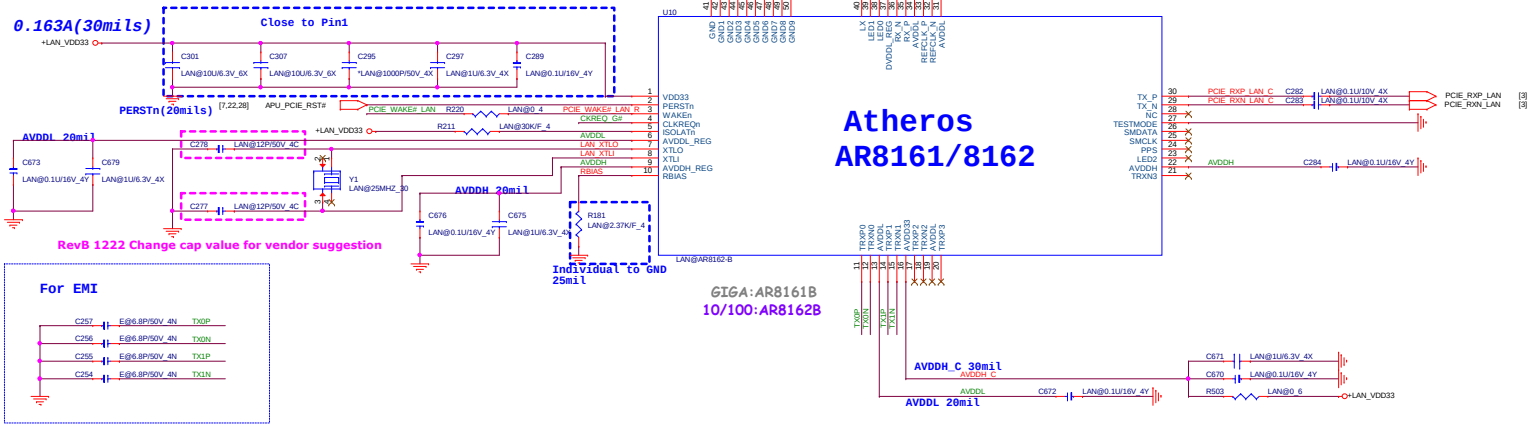
Touch Screen <TSN>



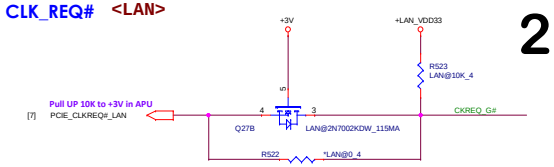
Quanta Computer Inc.			
PROJECT : BD9			
Size	Document Number		Rev
	HDMI/CEC		A1A
Date: Wednesday, January 30, 2013		Sheet 25 of 41	

Atheros Lan <LAN> <LNG>

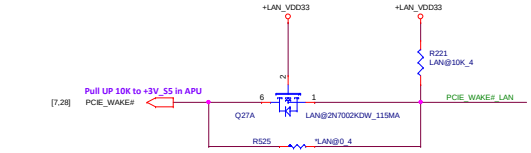




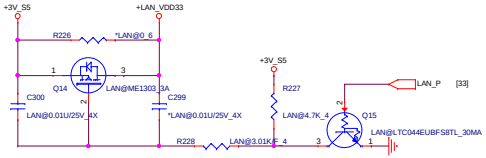
CLK_REQ# <LAN>



LAN-Wake up function <LAN>



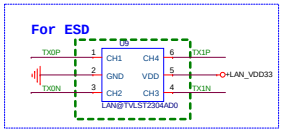
Wake on LAN function <LAN>



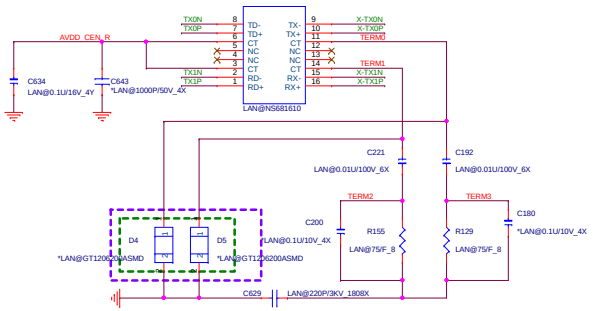
PLACE NEAR LAN IC SIDE <LAN> <LNG>

0920 FAE suggest remove 49.9K, 0.1u and 1000p

TRANSFORMER CONN <LAN> <LNG>

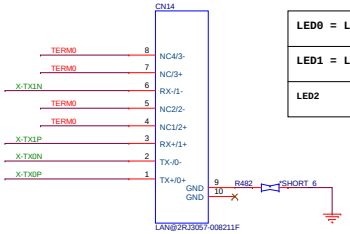


RevC 0130 Stuff U9



RevA 1114 Add Gas Tube for Surge issue
RevC 0130 Un-stuff D4,D5

RJ45 <LAN> <LNG> <LN1>



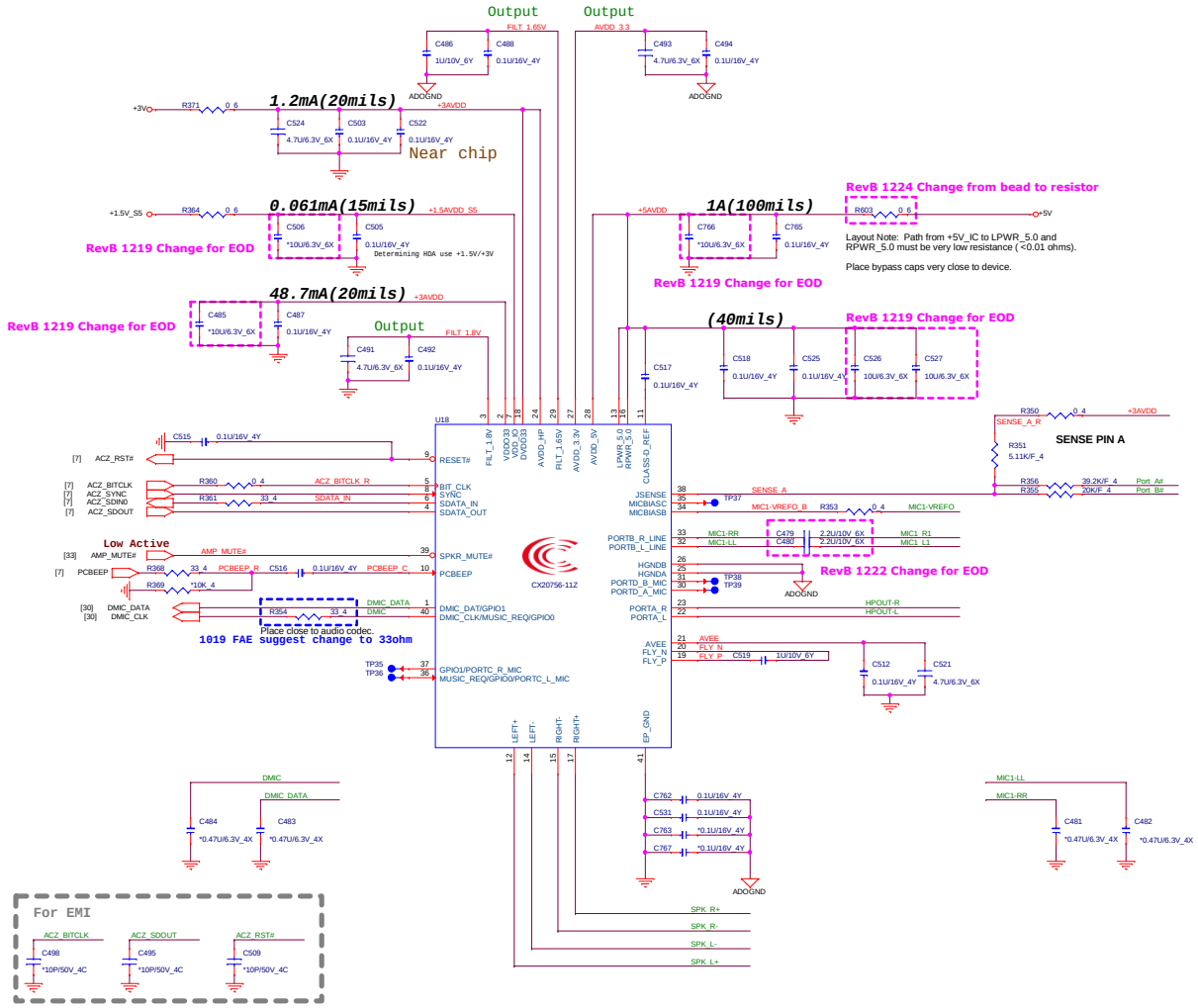
1005 Update FP

LED0 = LAN_ACTLED	1	High core voltage(default=1)
	0	Low core voltage
LED1 = LAN_LINKLED#	1	Switch mode regulator (SWR) select
	0	Linear regulator (LDO) select
LED2	1	25 MHz external clock input
	0	48 MHz external clock input

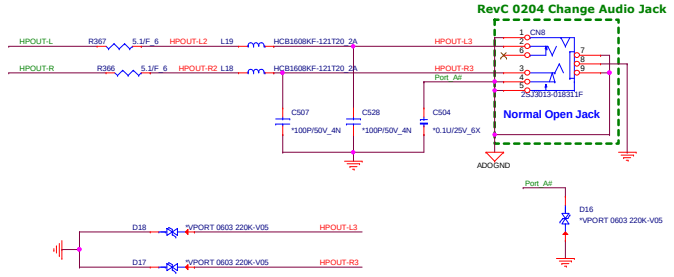
Power on Strapping pin

Quanta Computer Inc.
PROJECT : BD9
Size | Document Number: ATHEROS LAN (AR8152B) | Rev A1A
Date: Wednesday, January 30, 2013 | Sheet 26 of 41

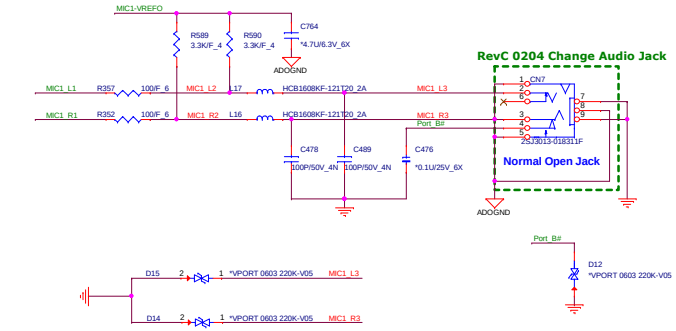
Codec (CX20756-11Z) <ADO> <EMI>



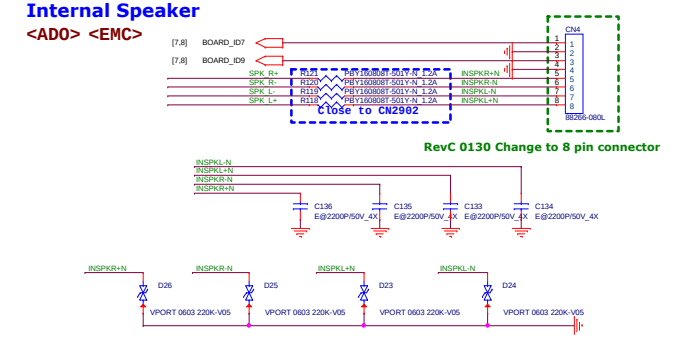
HP <ADO> <EMC>



External MIC <ADO> <EMC>



Internal Speaker <ADO> <EMC>



Quanta Computer Inc.		
PROJECT : BD9		
Size	Document Number: AUDIO CODEC (CX20756-11Z)	Rev: A1A
Date: Monday, February 04, 2013	Sheet 27 of 41	

MINI Card Slot#1 <MNW> (WiFi)

Before RAMP must to remove debug card component

RevB 1219 Change for EOD

RevB 1219 Change for EOD

C576 E@0.01U/25V_4X
C571 E@0.1U/16V_4Y
C582 *10U/6.3V_6X
C32 E@0.1U/16V_4Y
C10 0.1U/16V_4Y
C25 *C@0.1U/16V_4Y
C31 *C@0.1U/16V_4Y
C588 *C@10U/6.3V_6X

CN10
AAA-PCI-052-P01

1018 change to 7H

SMBus(WLAN)

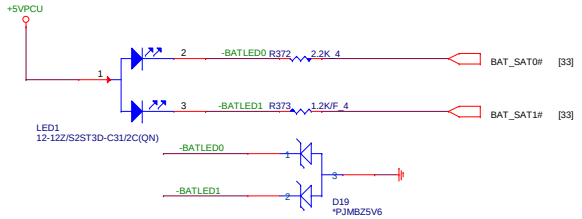
Pull UP 10K to +3V in APU
Pull UP 10K to +3V_S5 in APU

Quanta Computer Inc.
PROJECT : BD9

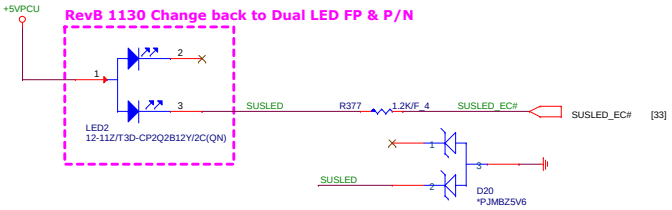
Size	Document Number	Rev
	MINI CARD	A1A

Date: Tuesday, December 25, 2012 Sheet 28 of 41

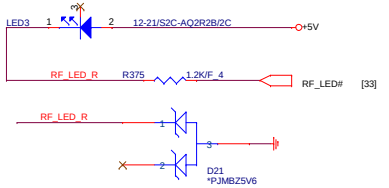
BATERRY



POWER



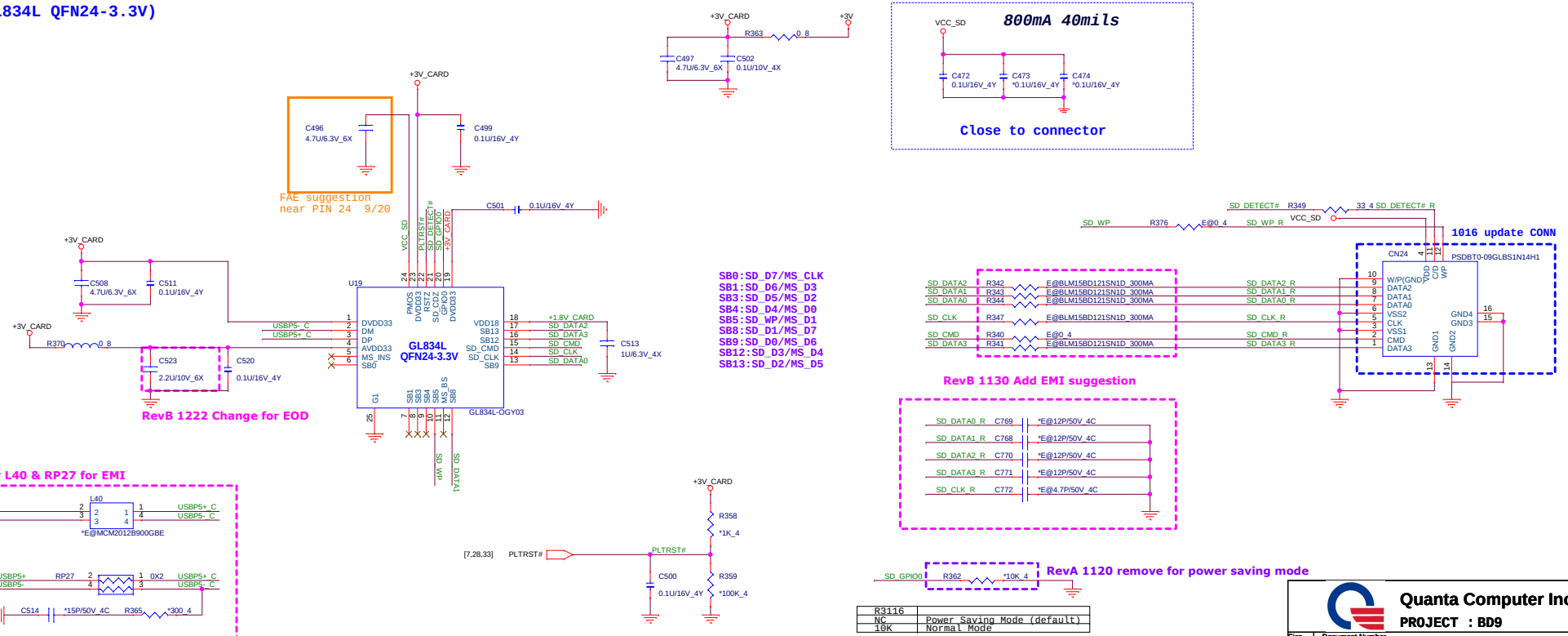
RF LED



29

2 IN 1 CARD READER (Type: MS/SD) <MMC>

Card Reader (GL834L QFN24-3.3V)



R3116	
NC	Power Saving Mode (default)
10K	Normal Mode

Quanta Computer Inc.

PROJECT : BD9

Size	Document Number	Rev
	CARD READER/LED	A1A

Date: Tuesday, December 25, 2012 Sheet 29 of 41

CCD [CCD]

RevB 1220 Add C.M Chock for EMI

L22 E@MCM2012B900GBE

Close LVDS Connector

USBP6+_CCD [8]
USBP6-_CCD [8]

R380 Hudson@330_4 C568 Hudson@15P/50V_4C

0924 Bolton without R+C

F1 SMD1206P110TF

R7 *0_8

1015 Exchange

CCD_POWER

C5 10U/6.3V_6X

RevB 1219 Change for EOD

C567 *4.7P/50V_4C USBP6+_CCD
C542 *4.7P/50V_4C USBP6-_CCD

LCD POWER SWITCH <LDS>

1017 3D eDP panel VDD=5V

+5V 2A +3V

C533 eDP@1U/10V_6X
R379 eDP@0_1206
R380 LDS@0_1206
C534 LDS@1U/10V_6X

U1 AP2821KTR-G1

LCDVCC

C1 0.1U/16V_4Y

[5] APU_DIGON R1 eDP@0_1206
[24] PANEL_VCC_R R2 LDS@0_1206
R3 100K_4

HALL SENSOR&BACK LIGHT SWITCH <HSR>

+3VPCU R378 100K_4

MR1 APX9132H AI-TRG

C532 0.1U/10V_4X

LID591# [33]

[33] DISPON_I R91 100K_4

R84 LDS@0_4 TRAVIS_BL_EN [24]
R87 eDP@0_4 APU_BL_EN [5]

DISPON R4 1.2K/F_4 EC_FPBACK# [33]

D1 LCP0G050M0R2R

LCD Panel Module [LDS]

VIN R381 0_8 LCD_BK_POWER

C536 1000P/50V_4X
C537 0.1U/25V_6X

LVDS Enable

+3VO R9 4.7K_4 LCD_EDIDCLK
R8 4.7K_4 LCD_EDIDDATA

[5,24] APU_VARY_BL R5 eDP@0_4 LVDS_VADJ
[24] TRAVIS_VARY_BL R6 LDS@0_4
C3 0.1U/10V_4X

LCD_EDIDDATA C7 E@2200P/50V_4X
LCD_EDIDCLK C6 E@2200P/50V_4X

+3VPCU C569 0.1U/10V_4X
+3VPCU C570 0.1U/10V_4X

Close to CN3200

[24] INT_LCD_TXLOUT0- RP8 LDS@0X2 LCD_TXLOUT0-
[24] INT_LCD_TXLOUT0+ LCD_TXLOUT0+
[24] INT_LCD_TXLOUT1- RP11 LDS@0X2 LCD_TXLOUT1-
[24] INT_LCD_TXLOUT1+ LCD_TXLOUT1+
[24] INT_LCD_TXLOUT2- RP13 LDS@0X2 LCD_TXLOUT2-
[24] INT_LCD_TXLOUT2+ LCD_TXLOUT2+
[24] INT_LCD_TXLCLKOUT- RP15 LDS@0X2 LCD_TXLCLKOUT-
[24] INT_LCD_TXLCLKOUT+ LCD_TXLCLKOUT+
[24] INT_LCD_TXUOUT0- RP17 LDS@0X2 LCD_TXUOUT0-
[24] INT_LCD_TXUOUT0+ LCD_TXUOUT0+

[24] INT_LVDS_TXN0_R RP7 eDP@0X2
[24] INT_LVDS_TXP0_R RP9 eDP@0X2
[24] INT_LVDS_TXN1_R RP12 eDP@0X2
[24] INT_LVDS_TXP1_R RP14 eDP@0X2
[5] INT_LVDS_TXN2
[5] INT_LVDS_TXP2
[5] INT_LVDS_TXN3
[5] INT_LVDS_TXP3
[24] INT_LVDS_AUXN_R RP16 eDP@0X2
[24] INT_LVDS_AUXP_R

[5,24] INT_LVDS_HPD +3VO R383 eDP@0_4 R382 LDS@0_4 LCDVCC

C538 *10U/6.3V_4X LCDVCC
C539 *47P/50V_4N
C540 22P/50V_4N
L20 FCM1005KF-221T03_300MA
L21 FCM1005KF-221T03_300MA
C541 22P/50V_4N

[27] DMIC_DATA
[27] DMIC_CLK

[24] INT_LCD_EDIDCLK
[24] INT_LCD_EDIDDATA
RP6 LDS@0X2

CN9

LCD_BK_POWER
CCD_POWER
DMIC_DATA_R
DMIC_CLK_R
LVDS_VADJ
DISPON
LCD_EDIDCLK
LCD_EDIDDATA
USBP6-_CCD_C
USBP6+_CCD_C
LCD_TXLOUT0-
LCD_TXLOUT0+
LCD_TXLOUT1-
LCD_TXLOUT1+
LCD_TXLOUT2-
LCD_TXLOUT2+
LCD_TXLCLKOUT-
LCD_TXLCLKOUT+
LCD_TXUOUT0-
LCD_TXUOUT0+
LCD_TXUOUT1-
LCD_TXUOUT1+
LCD_TXUOUT2-
LCD_TXUOUT2+
LCD_TXUCLKOUT-
LCD_TXUCLKOUT+

[24] INT_LCD_TXUOUT1- RP18 LDS@0X2
[24] INT_LCD_TXUOUT1+
[24] INT_LCD_TXUOUT2- RP19 LDS@0X2
[24] INT_LCD_TXUOUT2+
[24] INT_LCD_TXUCLKOUT- RP20 LDS@0X2
[24] INT_LCD_TXUCLKOUT+

Close to CN3200

7300L40-000000-G4

RevB 1224 Change FP & P/N

CRT [CRT]

[5] APU_CRT_RED
[5] APU_CRT_GRE
[5] APU_CRT_BLU
[5] APU_CRT_HSYNC
[5] APU_CRT_VSYNC
[5] APU_DDCDAT
[5] APU_DDCCLK

APU_CRT_RED L33 CRT@BLM18BA470SN1D_300MA CRT_RED_L
APU_CRT_GRE L32 CRT@BLM18BA470SN1D_300MA CRT_GRE_L
APU_CRT_BLU L31 CRT@BLM18BA470SN1D_300MA CRT_BLU_L

R528 CRT@150/F_4
R527 CRT@150/F_4
R526 CRT@150/F_4

C692 CRT@10P/50V_4C
C691 CRT@10P/50V_4C
C690 CRT@10P/50V_4C
C683 CRT@10P/50V_4C
C681 CRT@10P/50V_4C
C682 CRT@10P/50V_4C

RevB 1220 Change from 6.8P to 10P for EMI suggestion

+5V C272 CRT@0.1U/16V_4Y
+3V C273 CRT@0.1U/16V_4Y

+3V R234 CRT@4.7K_4 APU_DDCDAT
R231 CRT@4.7K_4 APU_DDCCLK

+5V D27 CRT@SS14L_1A F3 CRT@SMD1206P110TF

C688 CRT@0.1U/16V_4Y
5V_CRT2

CRT_RED_L
CRT_GRE_L
CRT_BLU_L

CN17 CRT@10256-00011

CRTDDAT
CRTHSYNC
CRTVSYNC
CRTDCLK

1020 Update CRT CONN

RevA 1115 Change P/N & FP

+5V C267 CRT@0.1U/25V_6X
+3V C268 CRT@0.1U/25V_6X

U11 CRT@CM2009-02QR

5V_CRT2
+5V
+3V
C271 CRT@0.22U/10V_4X

VCC_SYNC SYNC_OUT2
SYNC_OUT1
VCC_DDC
BYP
VCC_VIDEO
SYNC_IN2
SYNC_IN1
VIDEO_1
VIDEO_2
VIDEO_3
DDC_IN1
DDC_IN2
DDC_OUT1
DDC_OUT2
GND

CRT_RED_L
CRT_GRE_L
CRT_BLU_L

VSYNC1
HSYNC1
APU_CRT_VSYNC
APU_CRT_HSYNC
APU_DDCCLK
APU_DDCDAT
CRTDCLK
CRTDDAT

R232 CRT@39/F_4
R229 CRT@39/F_4

CRTVSYNC
CRTHSYNC

C316 CRT@10P/50V_4C
C317 CRT@10P/50V_4C

5V_CRT2
R230 CRT@2.7K_4
R235 CRT@2.7K_4

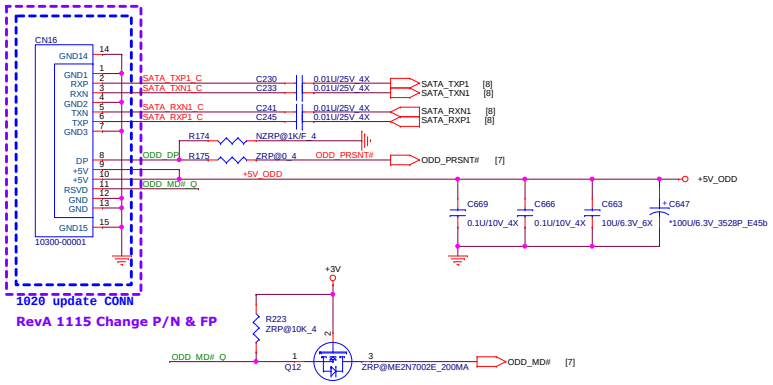
C311 CRT@10P/50V_4C
C312 CRT@10P/50V_4C

Quanta Computer Inc.
PROJECT : BD9

Size	Document Number	Rev
	LVDS/CCD/DRT	A1A

Date: Wednesday, December 26, 2012 Sheet 30 of 41

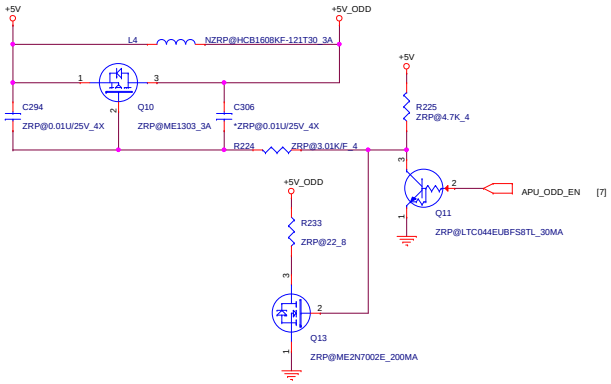
SATA ODD [ODD]



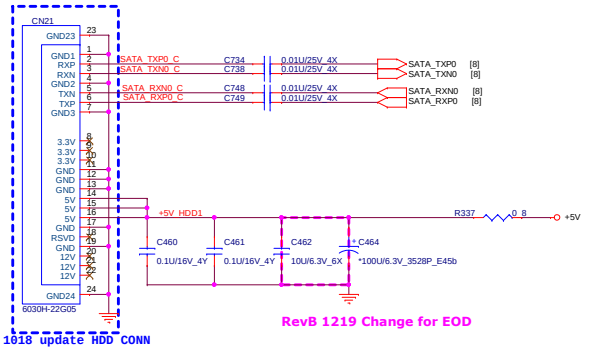
1020 update CONN

RevA 1115 Change P/N & FP

ODD Zero power <OZP>



SATA HDD [HDD]



1018 update HDD CONN

RevA 1115 Need to update correct FP

RevB 1219 Change for EOD

3D-LDO Power <GSR>

3D-u-micro P <GSR>

3D-SMBus <GSR>

3D-Sensor IC <GSR>

Quanta Computer Inc.

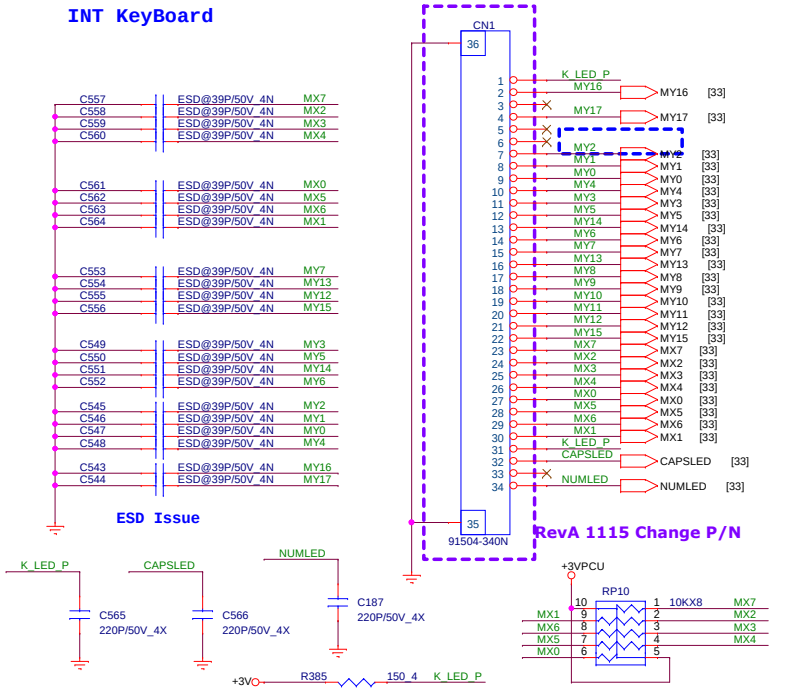
PROJECT : BD9

Size	Document Number	Rev
	HDD/ODD	A1A

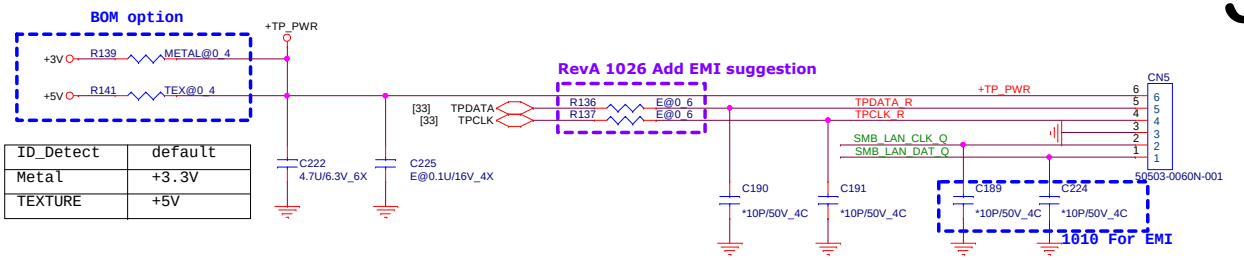
Date: Thursday, December 27, 2012 Sheet 31 of 41

KEY BOARD Connector <KBC> <EMI>

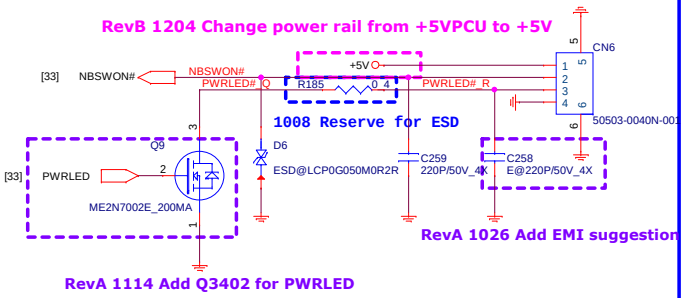
INT KeyBoard



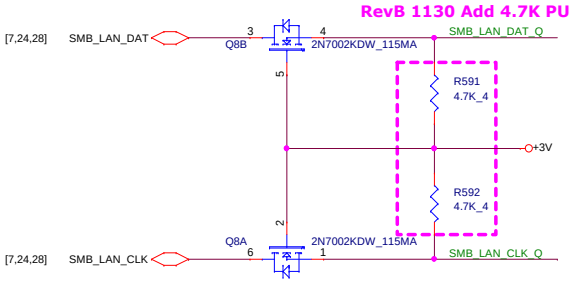
TOUCH PAD BOARD <TPD> <EMI>



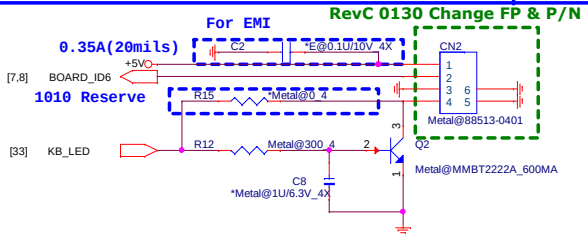
Power Board (UIF) <PSW>



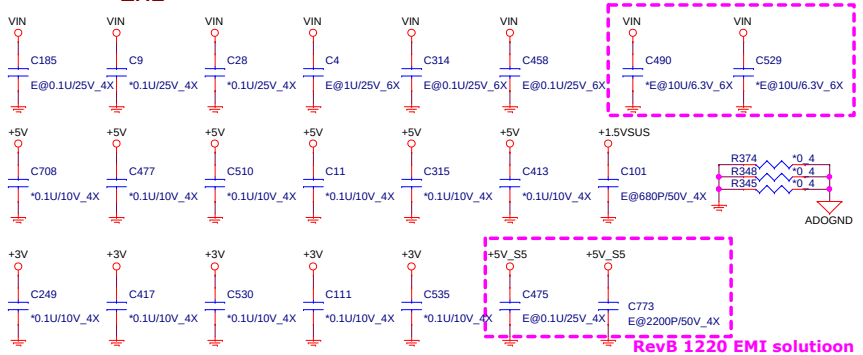
TP board <TPD>



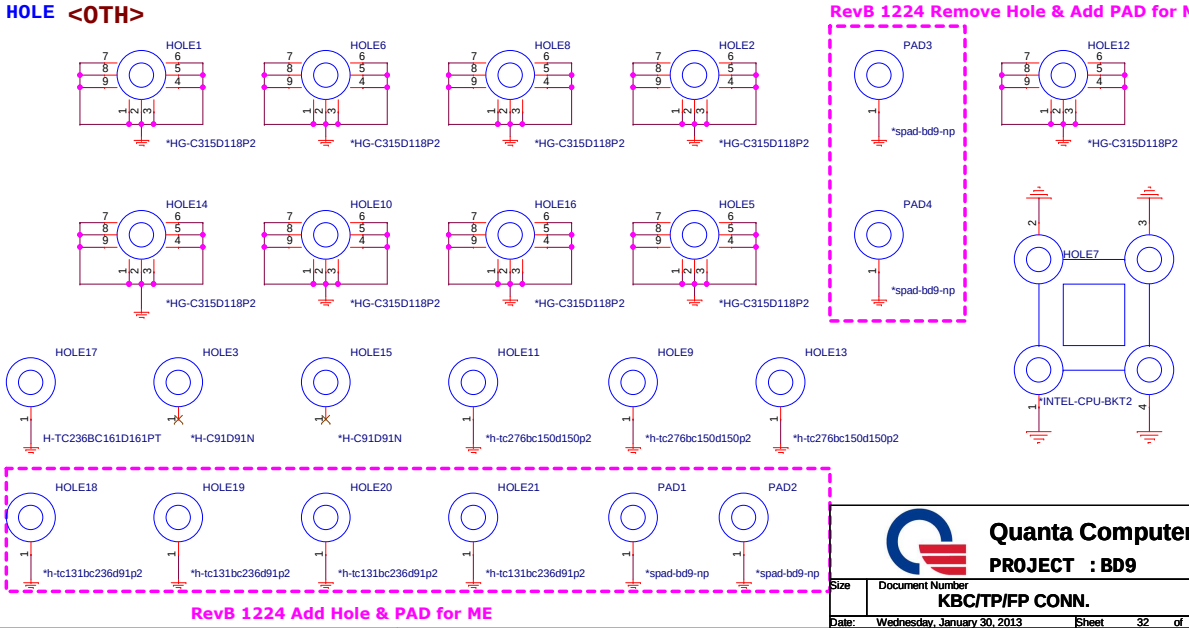
KEY BOARD LED <KBP> <EMI>



EMI PAD <EMI>



HOLE <OTH>



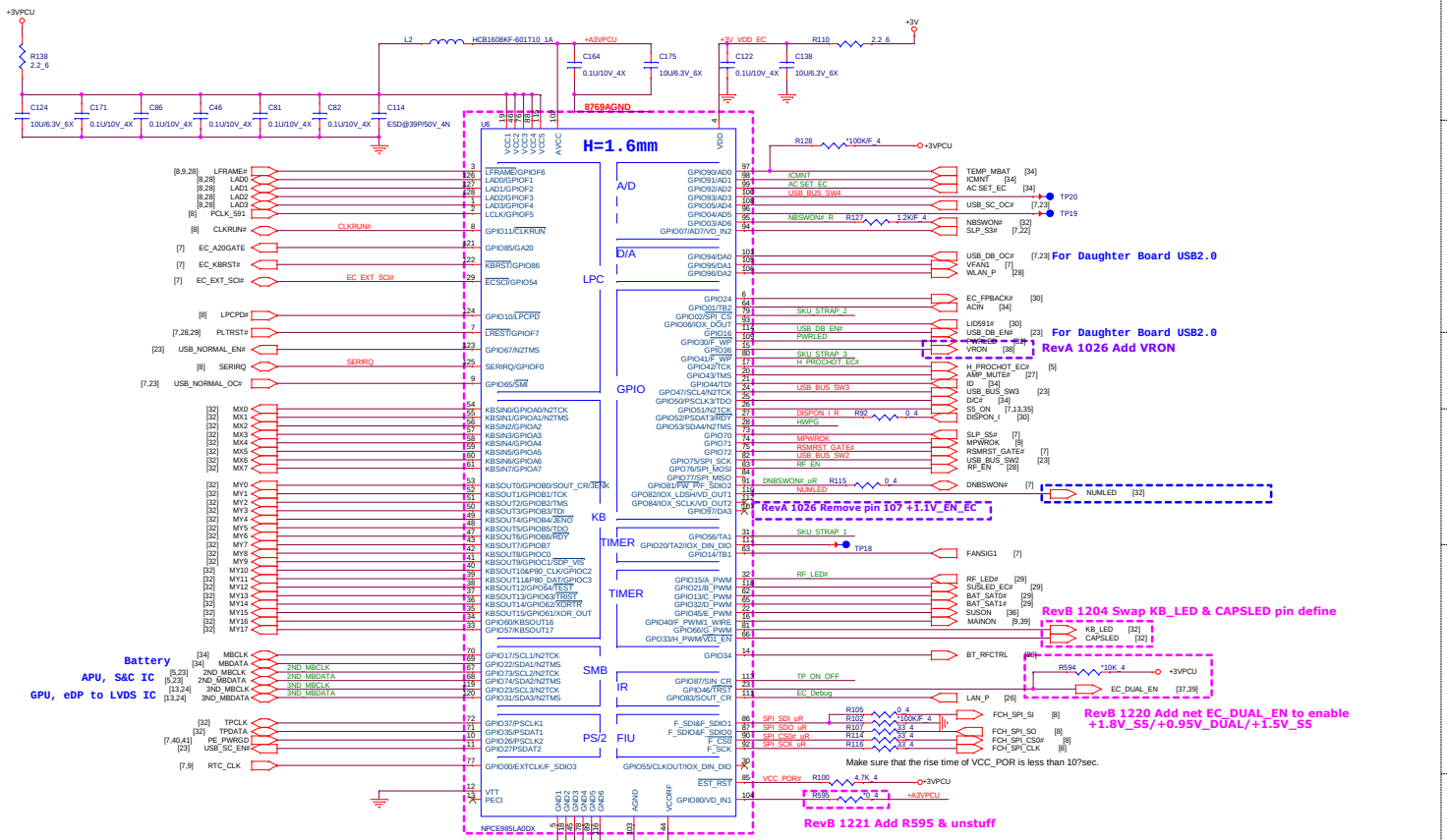
Quanta Computer Inc.

PROJECT : BD9

Size	Document Number	Rev
	KBC/TP/FP CONN.	A1A

Date: Wednesday, January 30, 2013 Sheet 32 of 41

EC <KBC>



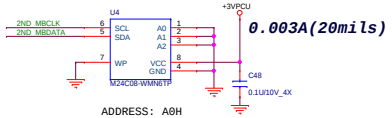
SM BUS PU <KBC>

SMBUS Table

SMBUS	Devices	Address
1	Battery	
2	PCH SML1	
	3D Sensor	32H
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H
	Touch Sensor	58H
	HDMI CEC	34H
	Light Sensor	52H

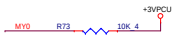
Strap <KBC> SHBM

ID EEPROM <KBC>

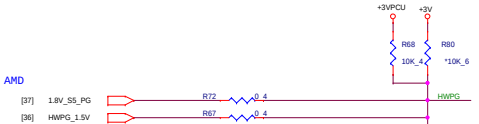


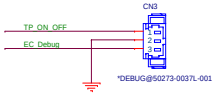
SPI FLASH <KBC>

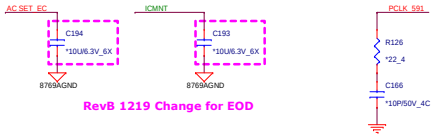
INTERNAL KEYBOARD STRIP SET <KBC>

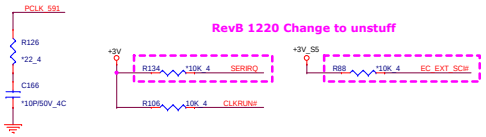


HWPG circuit <KBC>







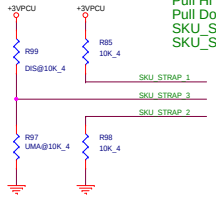


TP interface PU <KBC>

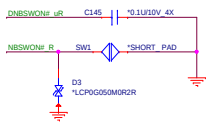
SKU_STRAP_1(GPIO56)	SKU_STRAP_2(GPIO02)	SKU_STRAP_3(GPIO41)	SKU
0	0	0	14" Kabini UMA
0	0	1	14" Kabini DIS
0	1	0	Richland UMA
0	1	1	Richland DIS
1	0	0	17" Kabini UMA
1	0	1	17" Kabini DIS

SKU strap pin <KBC>

For BD9 Strap pin setting:
Pull Hi SKU_STRAP_3 For Disctete
Pull Down SKU_STRAP_3 For UMA
SKU_STRAP_1=Hi
SKU_STRAP_2=Low

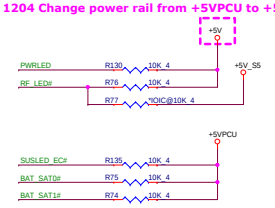


Power Button <KBC>

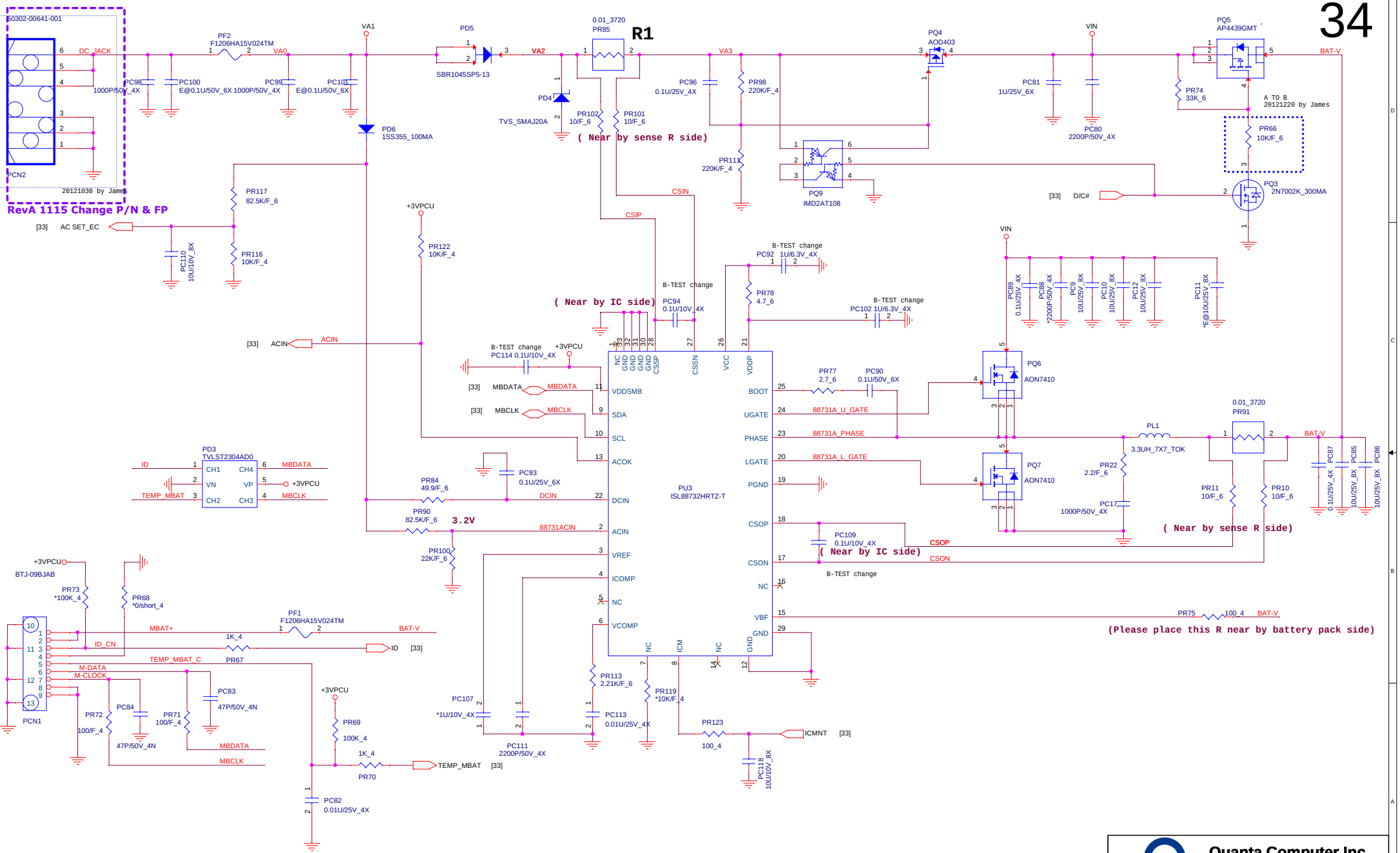


LED PU/PD <LED>

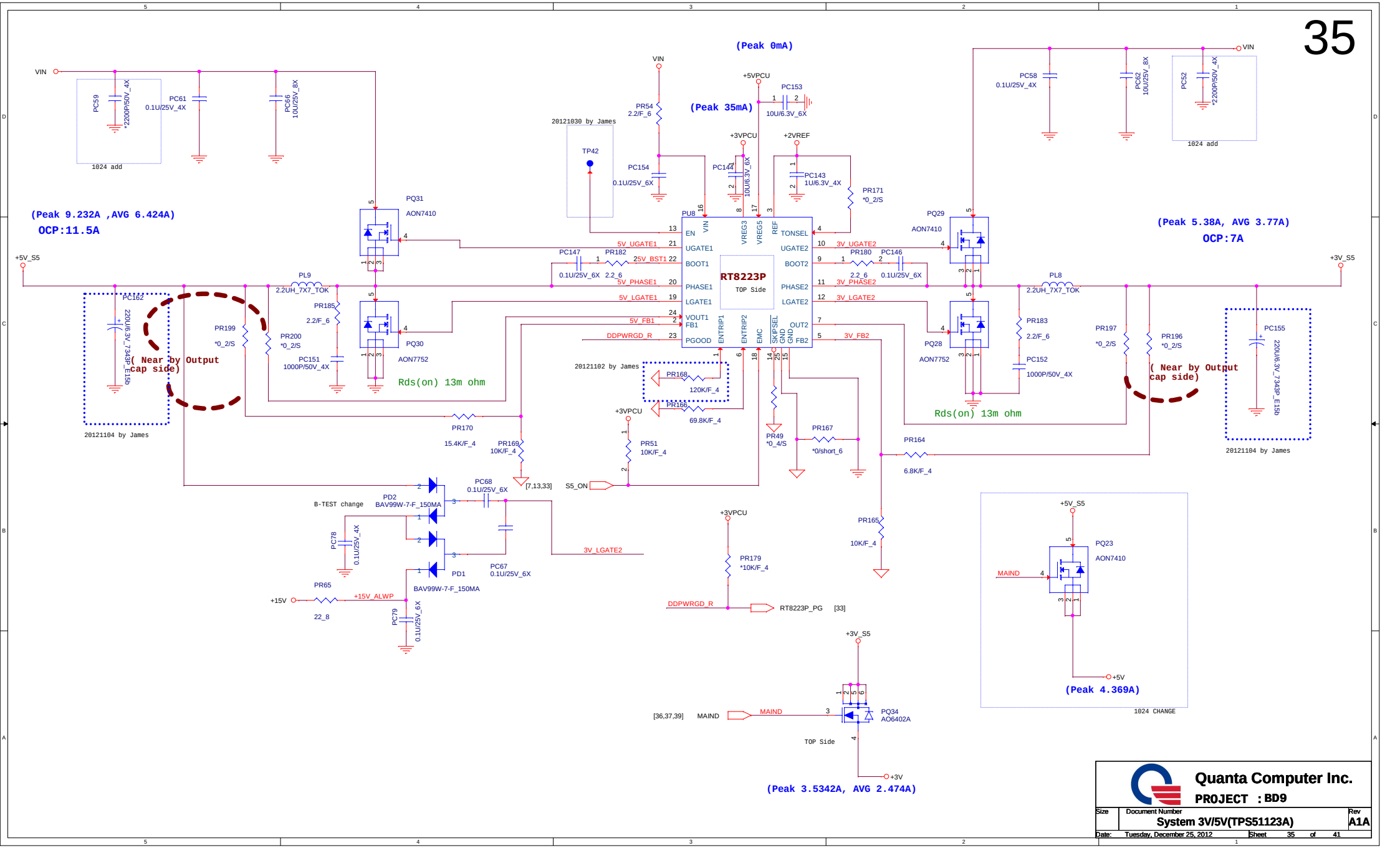
RevB 1204 Change power rail from +5VPCU to +5V

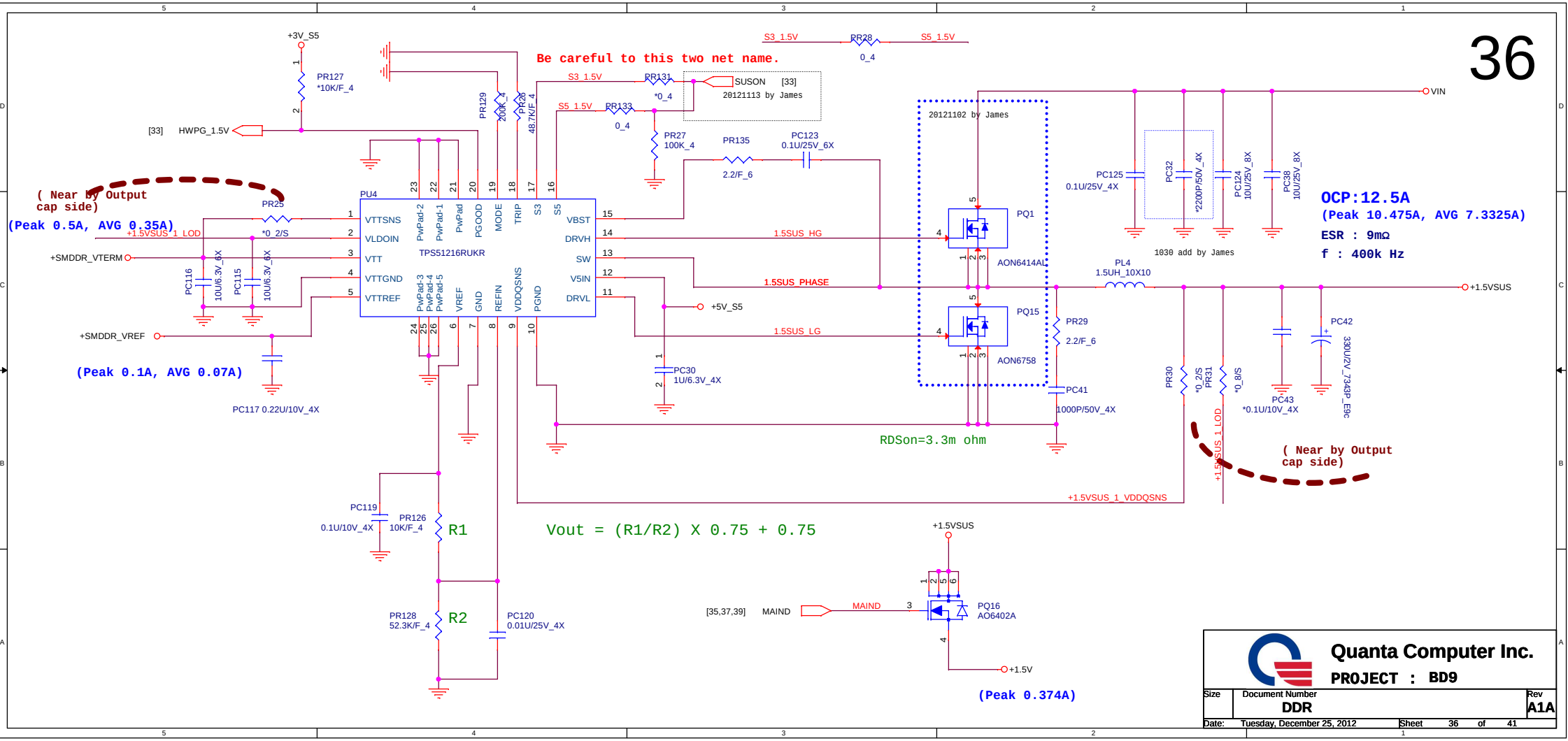


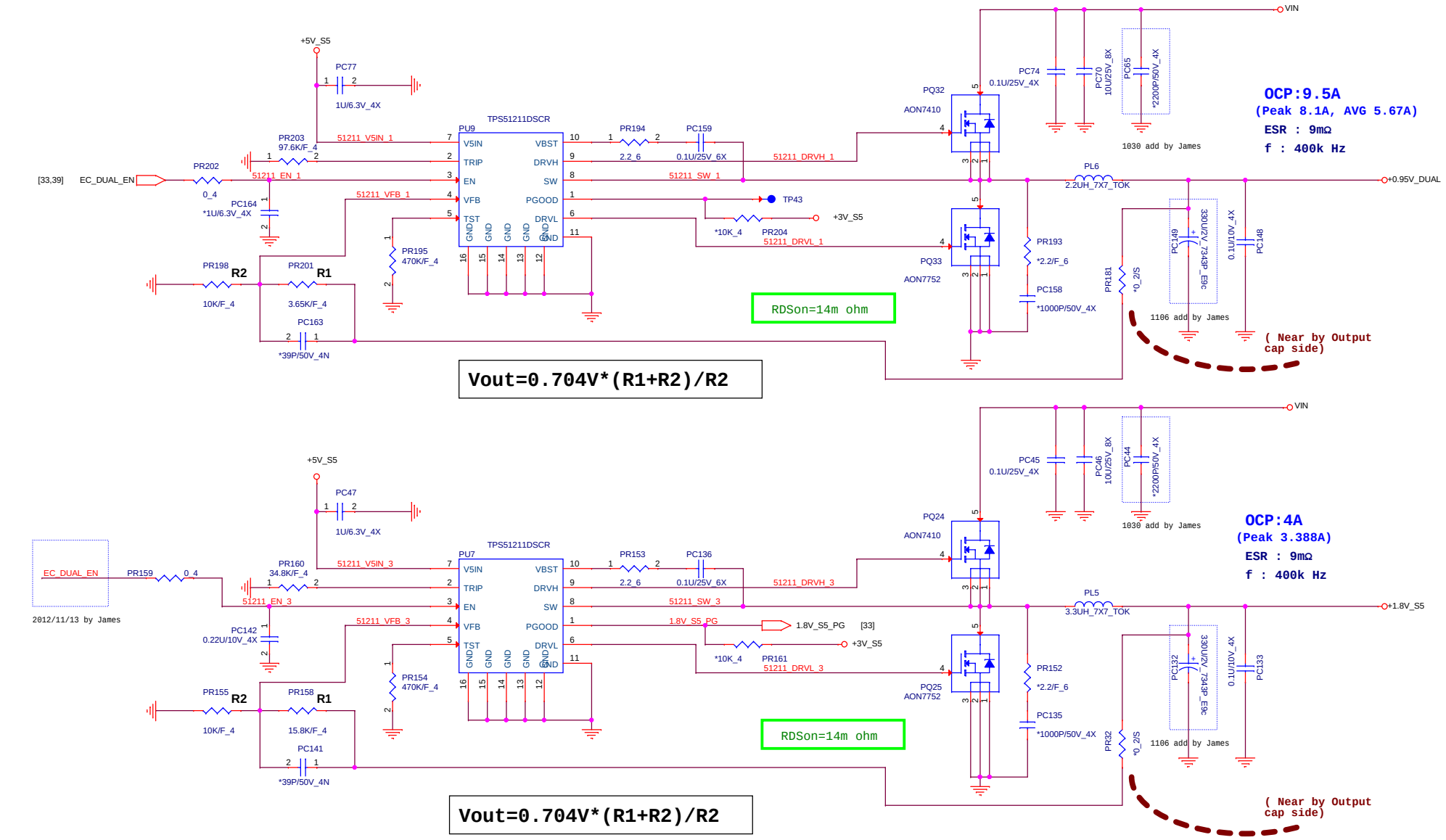
Quanta Computer Inc.
PROJECT : BD9
Size: Document Number: EC NPCE795CA0DX Rev: A1A
Date: Tuesday, December 25, 2012 Sheet 33 of 41

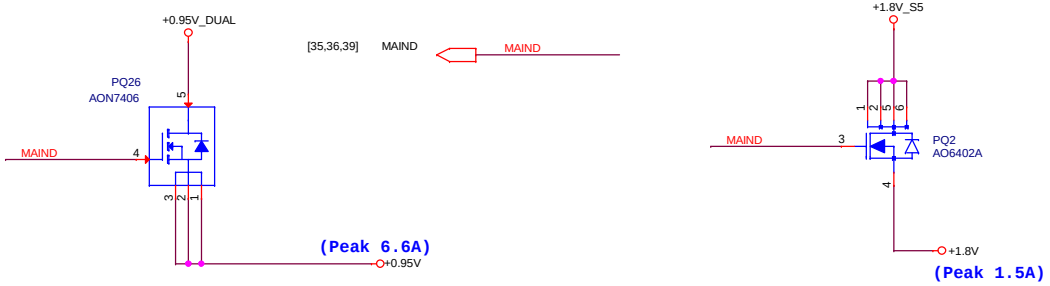


Quanta Computer Inc.		
PROJECT : BD9		
Size	Document Number	Rev
	CHARGER-ISL88731C	A1A
Date: Thursday, December 27, 2012	Sheet 34 of 41	


(Peak 0mA)
(Peak 35mA)
(Peak 9.232A ,AVG 6.424A)
OCP:11.5A
(Peak 5.38A, AVG 3.77A)
OCP:7A
RT8223P
TOP Side
Rds(on) 13m ohm
Rds(on) 13m ohm
(Near by Output cap side)
(Near by Output cap side)
(Peak 4.369A)
(Peak 3.5342A, AVG 2.474A)
1024 add
1024 add
1024 CHANGE
20121104 by James
20121104 by James
20121102 by James
20121030 by James
B-TEST change
VIN
+5VPCU
+3VPCU
+2VREF
+5V_S5
+3V_S5
+15V
+5V
PQ31 AON7410
PQ30 AON7752
PQ29 AON7410
PQ28 AON7752
PQ23 AON7410
PQ34 AO6402A
PD1 BAV99W-7-F_150MA
PD2 BAV99W-7-F_150MA
PL9 2.2UH_7X7_TOK
PL8 2.2UH_7X7_TOK
PC59 *2200P/50V_4X
PC61 0.1U/25V_4X
PC66 10U/25V_8X
PC58 0.1U/25V_4X
PC62 10U/25V_8X
PC52 *2200P/50V_4X
PC153 10U/6.3V_6X
PC154 0.1U/25V_6X
PC144 10U/6.3V_6X
PC143 1U/6.3V_4X
PC147 0.1U/25V_6X
PC146 0.1U/25V_6X
PC162 220U/6.3V_7343P_E15b
PC155 220U/6.3V_7343P_E15b
PC151 1000P/50V_4X
PC152 1000P/50V_4X
PC68 0.1U/25V_6X
PC67 0.1U/25V_6X
PC78 0.1U/25V_4X
PC79 0.1U/25V_6X
PR54 2.2/F_6
PR182 25V_BST1 2.2_6
PR180 2.2_6
PR171 *0_2/S
PR185 2.2/F_6
PR183 2.2/F_6
PR199 *0_2/S
PR200 *0_2/S
PR197 *0_2/S
PR196 *0_2/S
PR170 15.4K/F_4
PR169 10K/F_4
PR168 120K/F_4
PR186 69.8K/F_4
PR51 10K/F_4
PR49 *0_4/S
PR167 *0/short_6
PR164 6.8K/F_4
PR165 10K/F_4
PR179 *10K/F_4
PR65 22_8
TP42
5V_UGATE1
5V_BST1
5V_PHASE1
5V_LGATE1
5V_FB1
DDPWRGD_R
3V_UGATE2
3V_PHASE2
3V_LGATE2
3V_FB2
S5_ON
MAIND
+15V_ALWP
RT8223P_PG
[7,13,33]
[36,37,39]
Quanta Computer Inc.
PROJECT : BD9
System 3V/5V(TPS51123A)
Size
Document Number
Rev
A1A
Date: Tuesday, December 25, 2012
Sheet 35 of 41

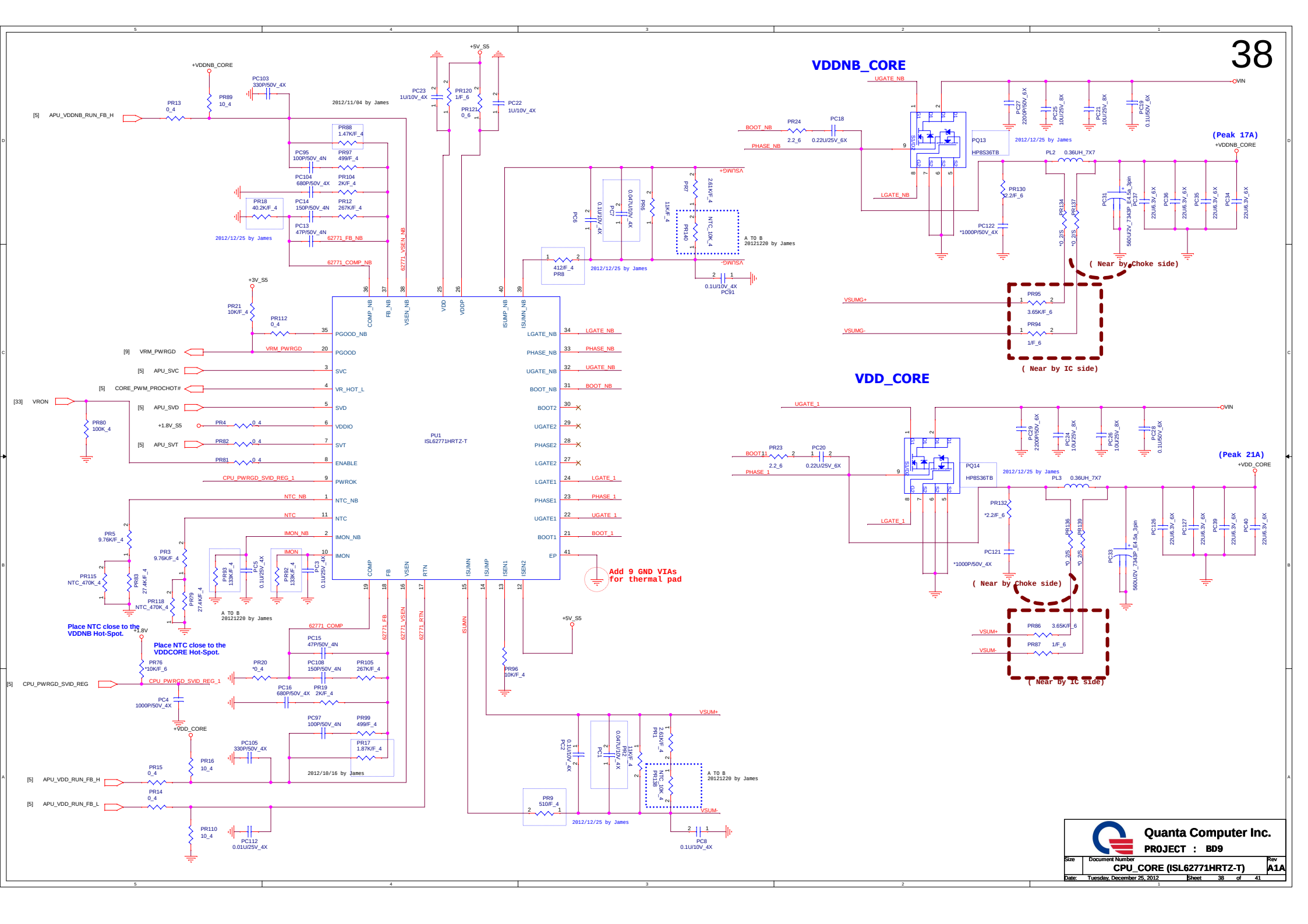

36
Be careful to this two net name.
(Near by Output cap side)
(Peak 0.5A, AVG 0.35A)
(Peak 0.1A, AVG 0.07A)
OCP:12.5A
(Peak 10.475A, AVG 7.3325A)
ESR : 9mΩ
f : 400k Hz
RDSon=3.3m ohm
Vout = (R1/R2) X 0.75 + 0.75
(Peak 0.374A)
TPS51216RUKR
AON6414AL
AON6758
AO6402A
20121113 by James
20121102 by James
1030 add by James
Quanta Computer Inc.
PROJECT : BD9
Document Number
DDR
Rev
A1A
Date: Tuesday, December 25, 2012
Sheet 36 of 41

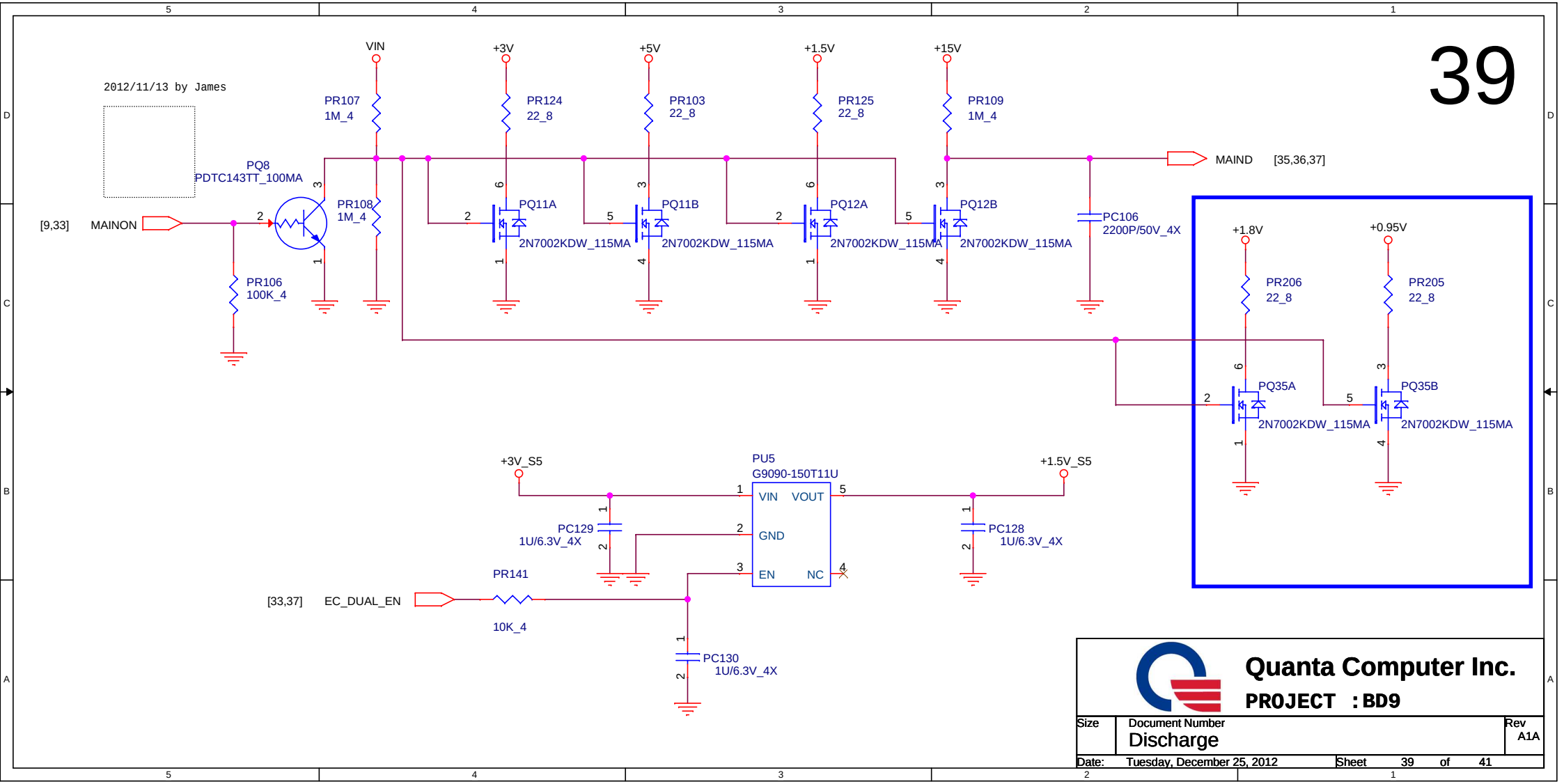




Quanta Computer Inc.
PROJECT : BD9

Size	Document Number	Rev
	+0.95V/+1.8V	A1A
Date: Tuesday, December 25, 2012	Sheet 37 of 41	

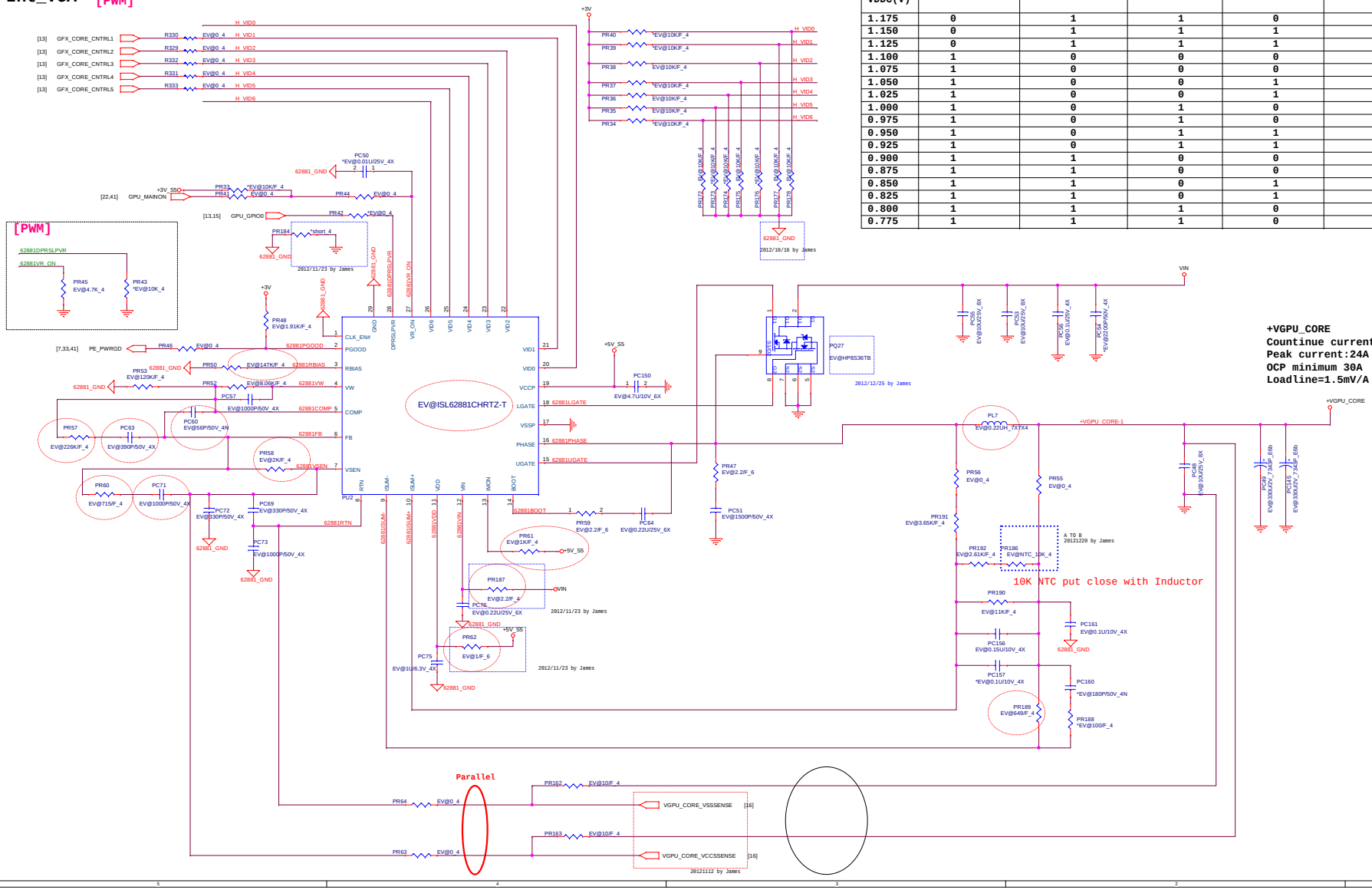

VDDNB_CORE
VDD_CORE
PU1
ISL62771HRTZ-T
Add 9 GND VIAs for thermal pad
Place NTC close to the VDDNB Hot-Spot.
Place NTC close to the VDDCORE Hot-Spot.
(Near by Choke side)
(Near by IC side)
(Peak 17A)
(Peak 21A)
2012/11/04 by James
2012/12/25 by James
2012/10/16 by James
A TO B 20121220 by James
Quanta Computer Inc.
PROJECT : BD9
CPU_CORE (ISL62771HRTZ-T)
A1A
Tuesday, December 25, 2012


39
2012/11/13 by James
VIN
+3V
+5V
+1.5V
+15V
PR107
1M_4
PR124
22_8
PR103
22_8
PR125
22_8
PR109
1M_4
MAIND
[35,36,37]
PQ8
PDTC143TT_100MA
[9,33]
MAINON
PR108
1M_4
PR106
100K_4
PQ11A
PQ11B
PQ12A
PQ12B
2N7002KDW_115MA
PC106
2200P/50V_4X
+1.8V
+0.95V
PR206
22_8
PR205
22_8
PQ35A
PQ35B
2N7002KDW_115MA
+3V_S5
PU5
G9090-150T11U
VIN
VOUT
GND
EN
NC
+1.5V_S5
PC129
1U/6.3V_4X
PC128
1U/6.3V_4X
PR141
[33,37]
EC_DUAL_EN
10K_4
PC130
1U/6.3V_4X
Quanta Computer Inc.
PROJECT : BD9
Size
Document Number
Discharge
Rev
A1A
Date: Tuesday, December 25, 2012
Sheet 39 of 41

Int_VGA [PWM]

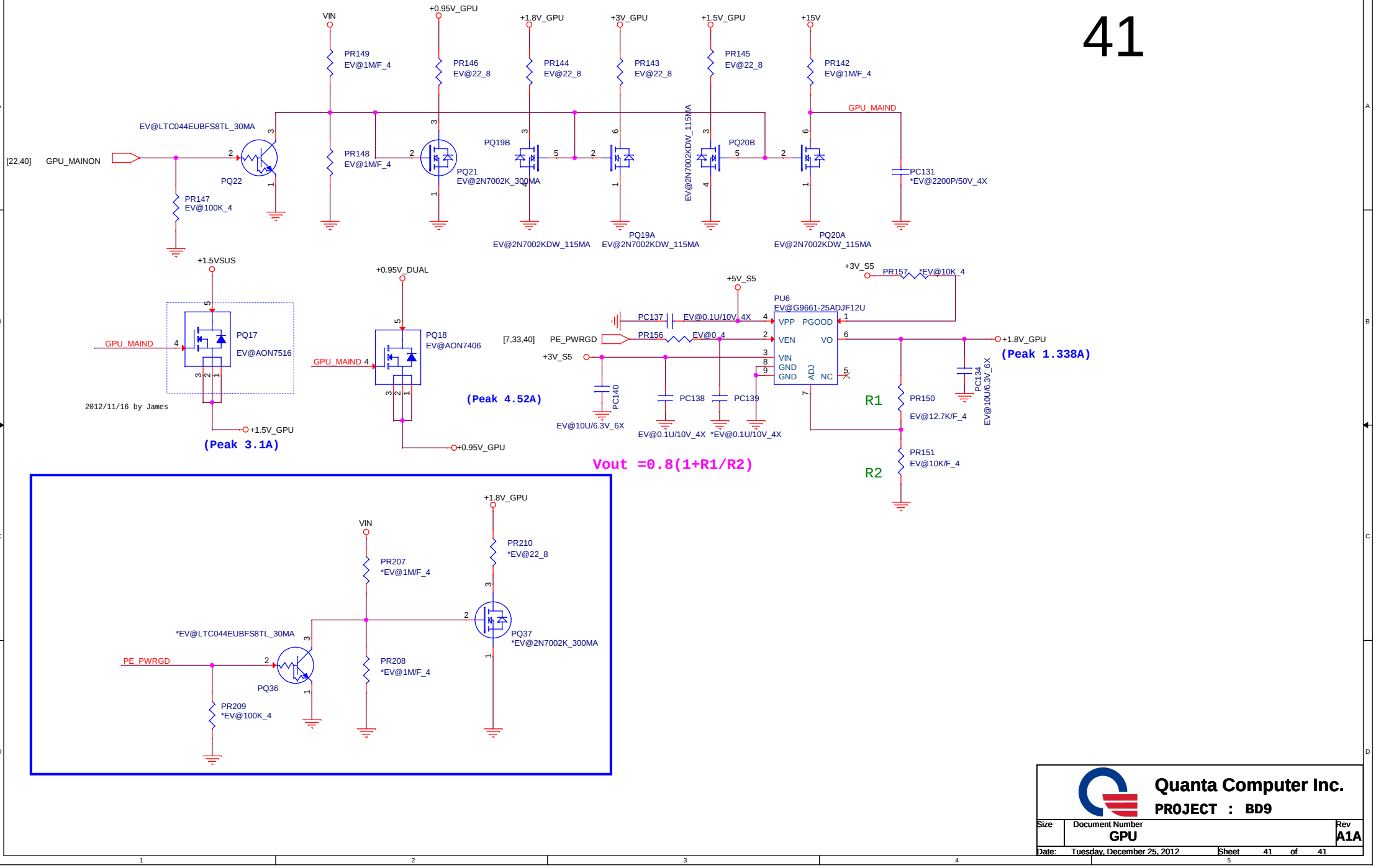
Mars VDDC VID TABLE

VDDC(V)	GFX_CORE_CNTRL5 (VID5)	GFX_CORE_CNTRL4 (VID4)	GFX_CORE_CNTRL3 (VID3)	GFX_CORE_CNTRL2 (VID2)	GFX_CORE_CNTRL1 (VID1)
1.175	0	1	1	0	1
1.150	0	1	1	1	0
1.125	0	1	1	1	1
1.100	1	0	0	0	0
1.075	1	0	0	0	1
1.050	1	0	0	1	0
1.025	1	0	0	1	1
1.000	1	0	1	0	0
0.975	1	0	1	0	1
0.950	1	0	1	1	0
0.925	1	0	1	1	1
0.900	1	1	0	0	0
0.875	1	1	0	0	1
0.850	1	1	0	1	0
0.825	1	1	0	1	1
0.800	1	1	1	0	0
0.775	1	1	1	0	1



Quanta Computer Inc.
PROJECT : BD9

Size	Document Number	Rev
	+VGPU_CORE (TPS51728RHAR)	A1A
Date: Wednesday, January 30, 2013	Sheet 40 of 41	



Quanta Computer Inc.		
PROJECT : BD9		
Size	Document Number: GPU	Rev: A1A
Date: Tuesday, December 25, 2012	Sheet 41 of 41	