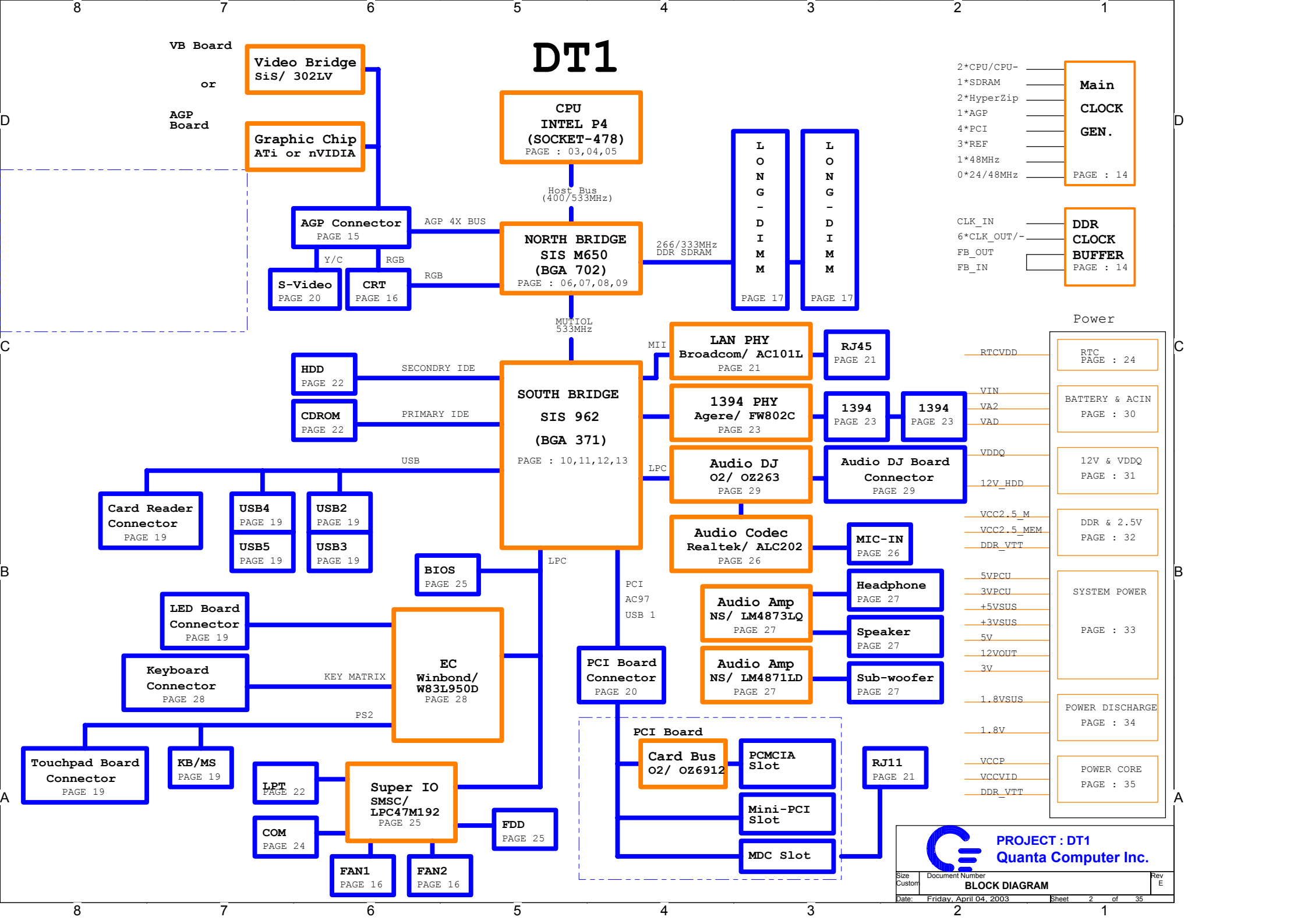
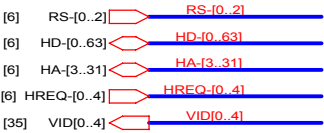


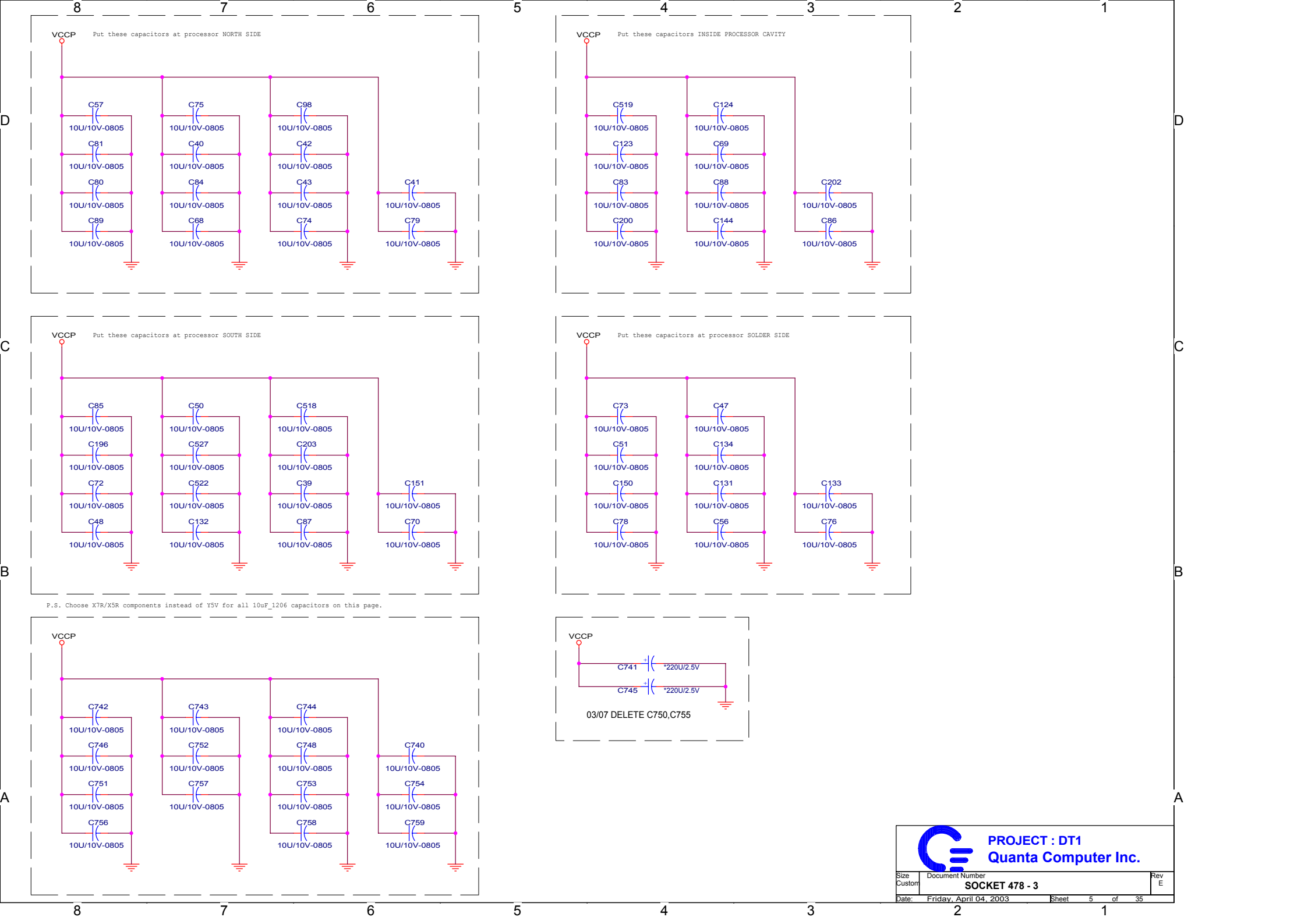
QUANTA COMPUTER INC.

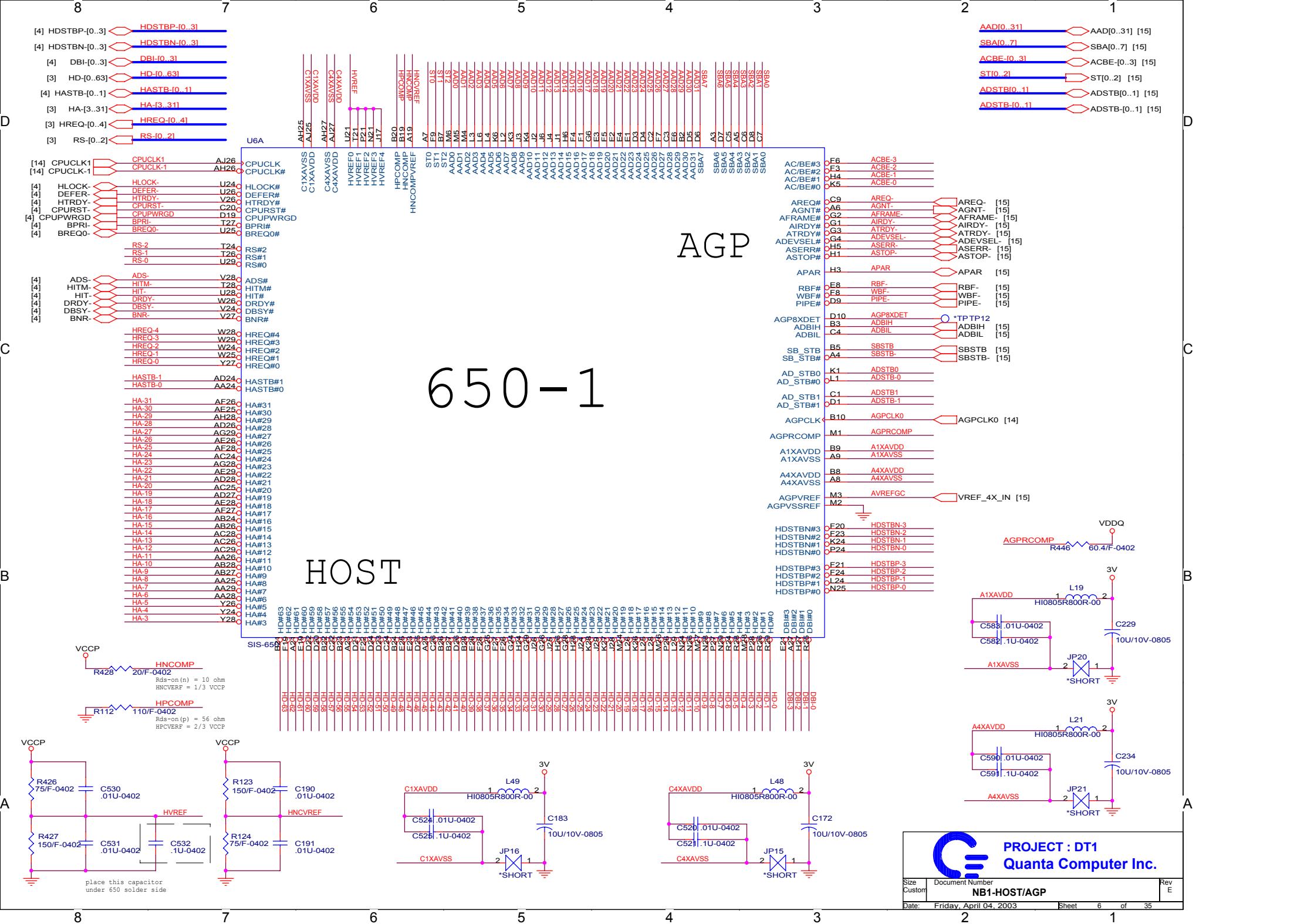
(March/31/2003) Rev : E

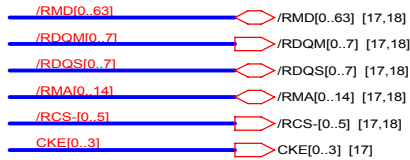
PAG	Content	PAG	Content
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2	650 System Block Diagram	32	POWER - DDR & 2.5V
3	SOCKET 478 - 1	33	SYSTEM POWER
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5	SOCKET 478 - 3	35	POWER CORE
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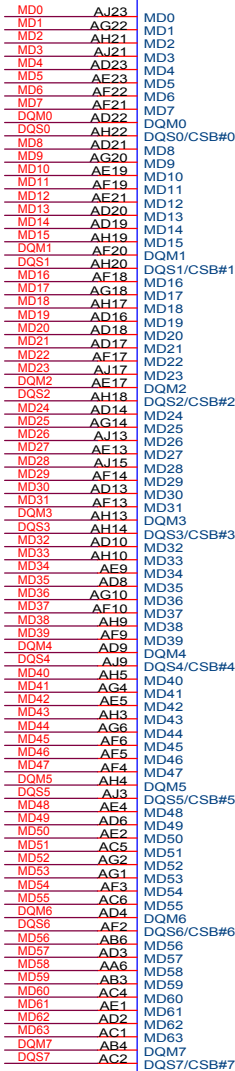
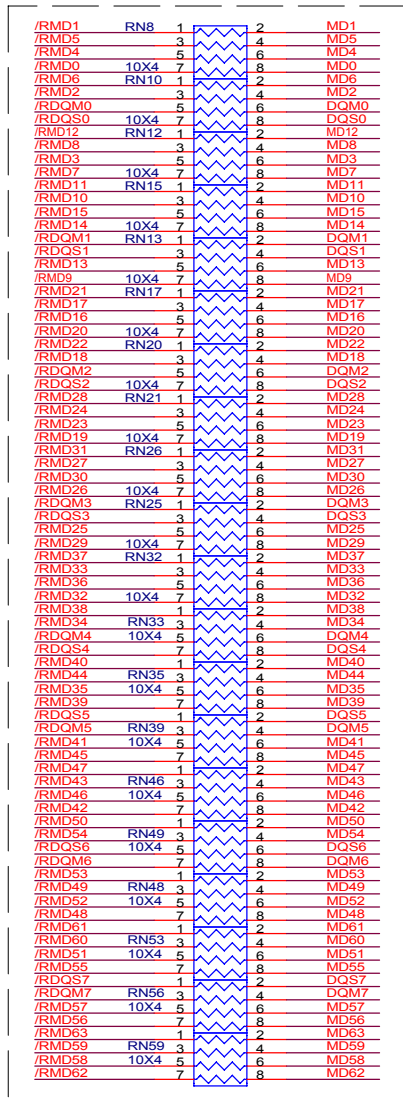








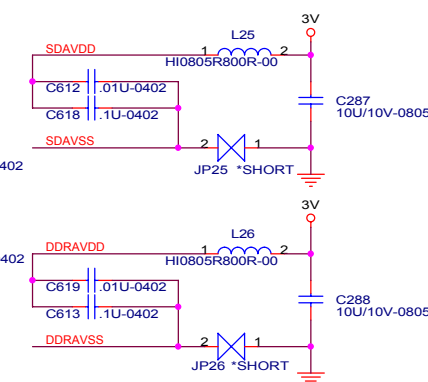
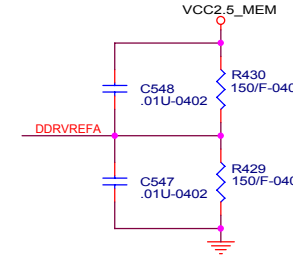
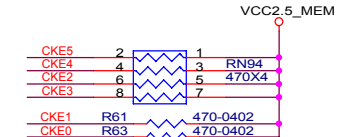
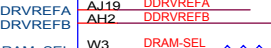
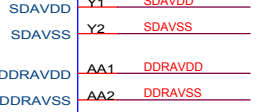
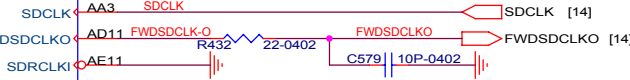
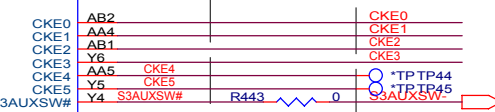
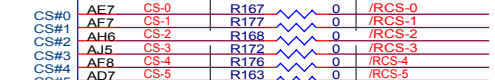
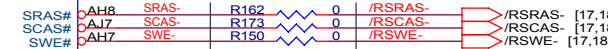
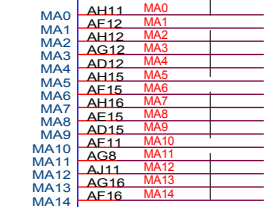
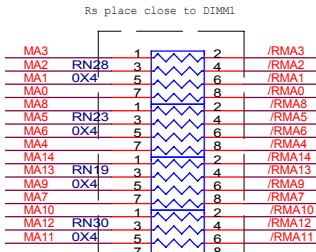
Rs place close to DIMM1



U6B

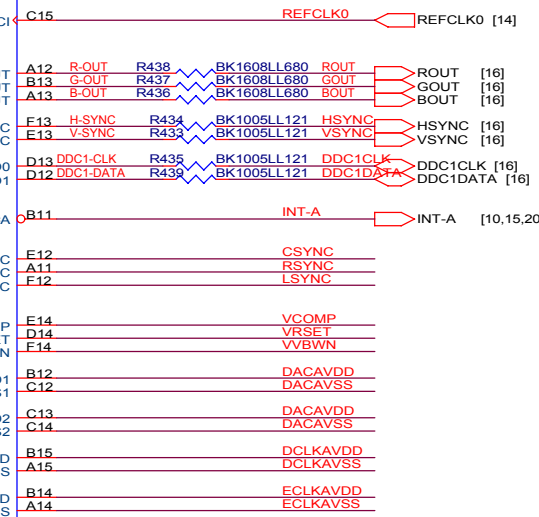
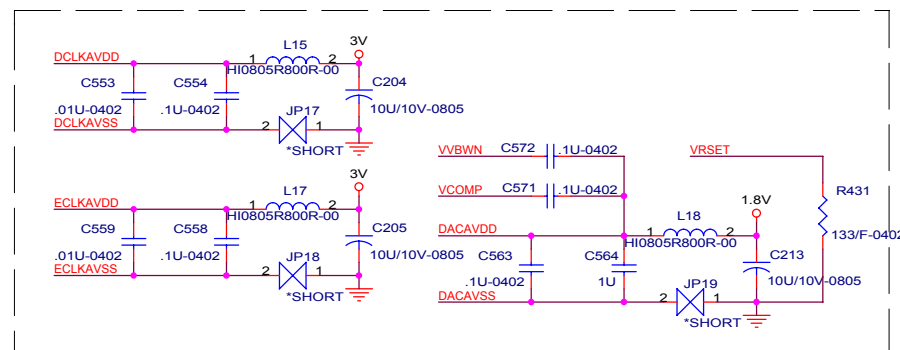
650-2

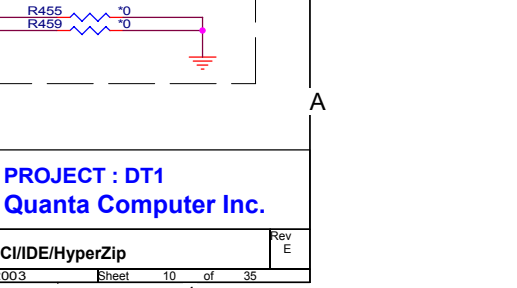
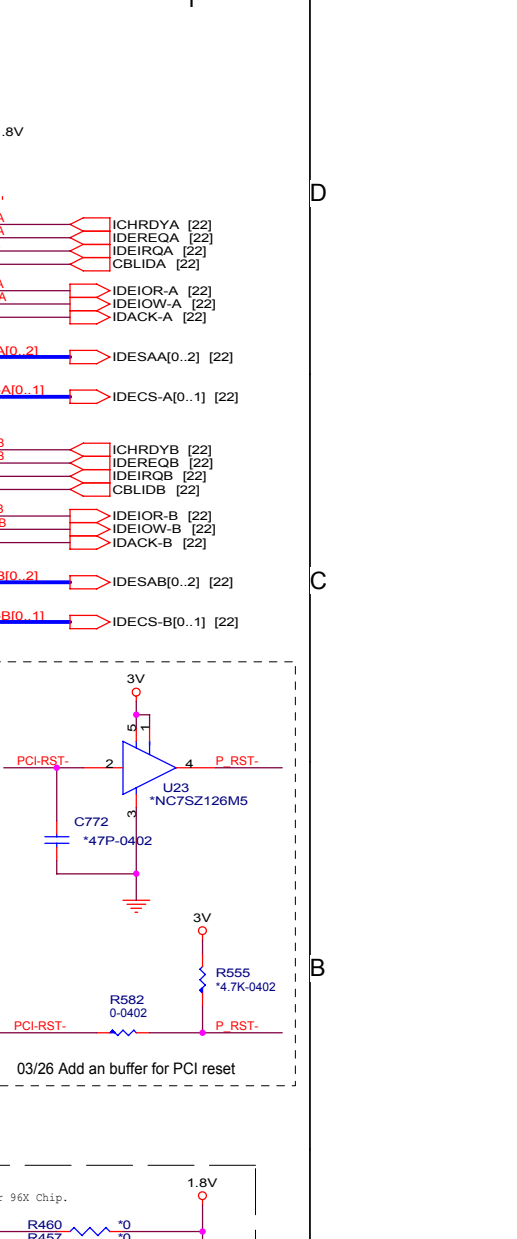
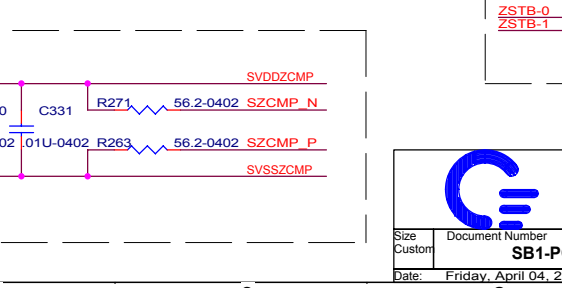
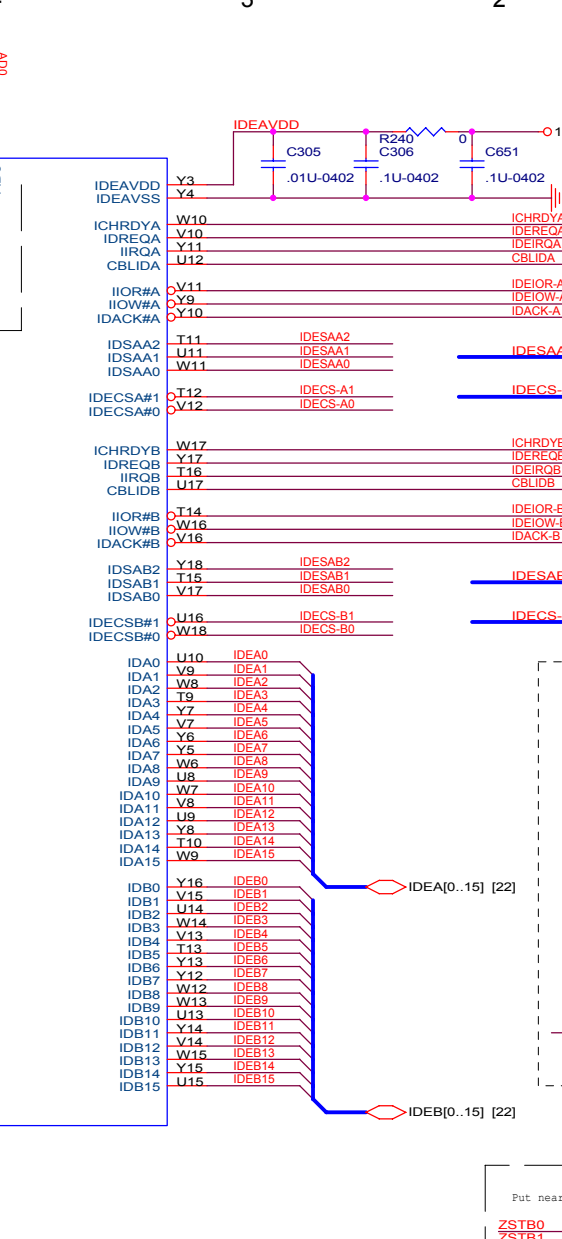
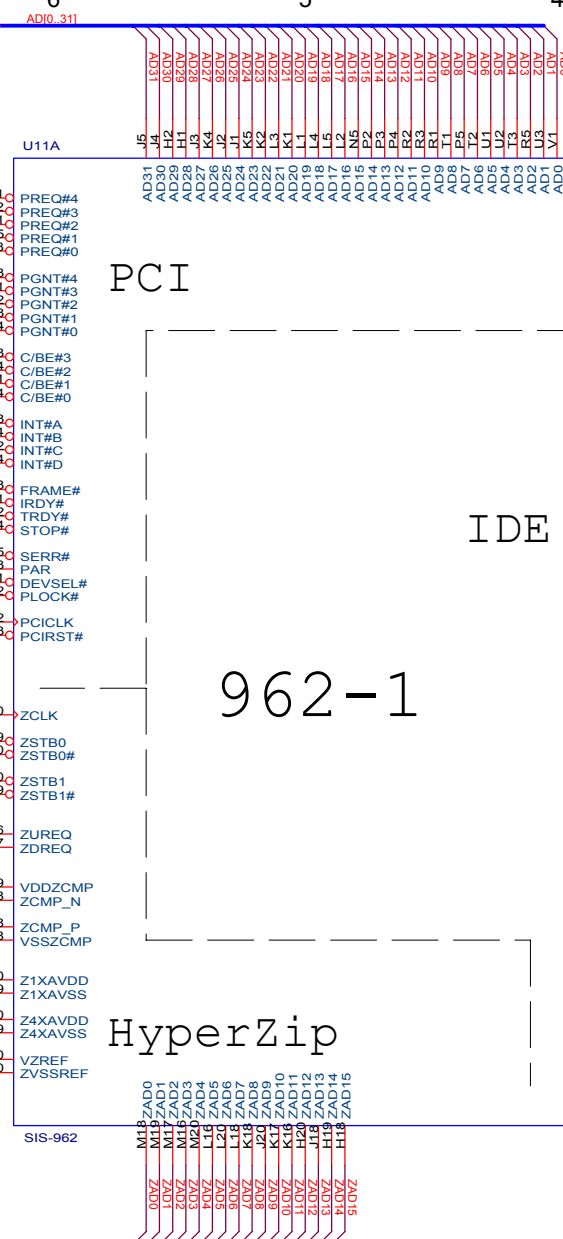
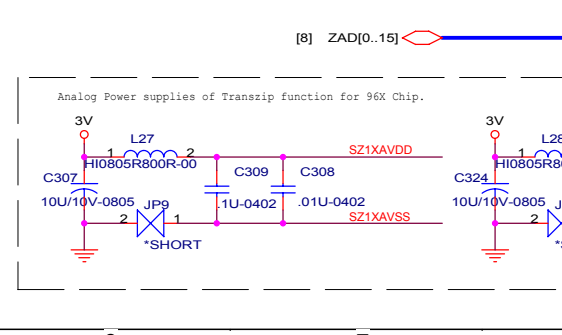
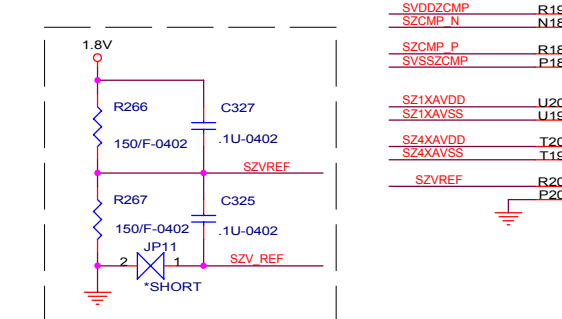
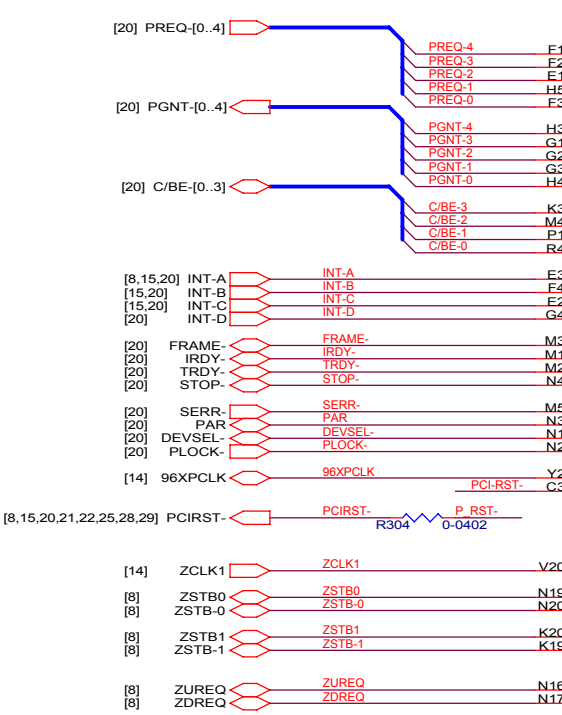
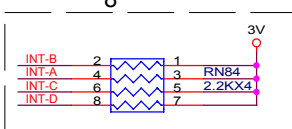
SIS-650



PROJECT : DT1
Quanta Computer Inc.

NB Hardware Trap Table				
	0	1	Default	embedded pull-low (30~50K Ohm)
DILEN#	enable PLL	disable PLL	0	yes
DRAM SEL	SDR	DDR	1 (DDR)	yes
TRAP0	normal	NB debug mode	0	yes
TRAP1	TV selection, NTSC/PAL(0/1)			0
CSYNC	enable VS			0
RSYNC	enable VGA interrupt			1
LSYNC	enable panel link			0





D

C

B

A

8

7

7

6

6

5

5

4

4

3

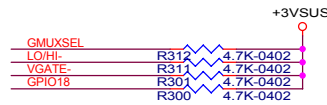
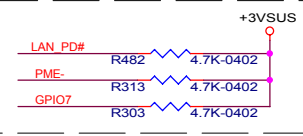
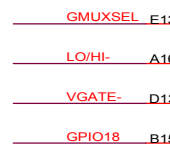
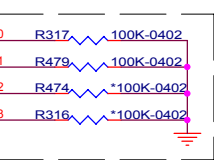
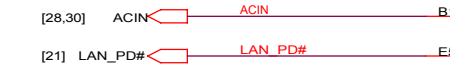
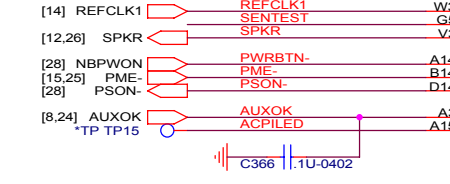
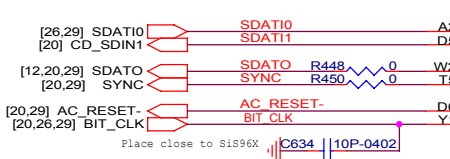
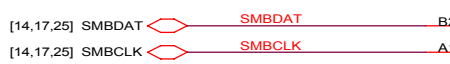
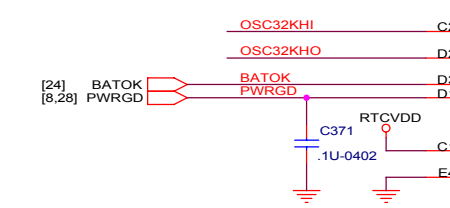
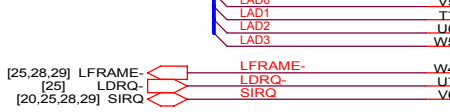
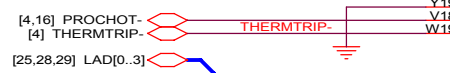
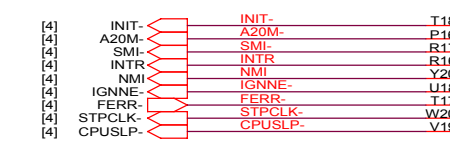
3

2

2

1

1



CPU_S

APIC

LPC

RTC

GPIO

AC97

ACPI
/others

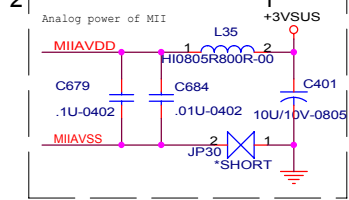
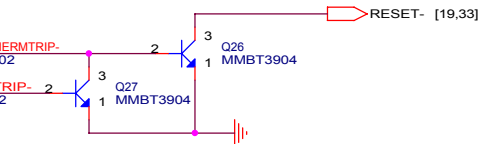
KBC

/geyserville

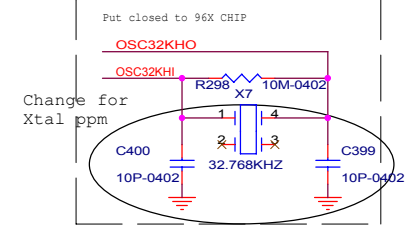
SIS-962

MII

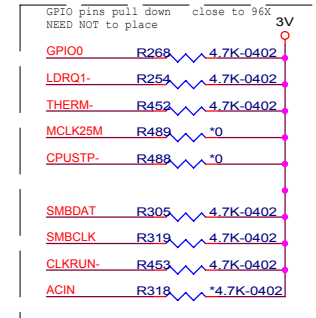
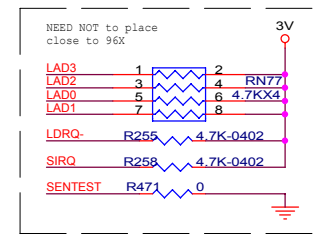
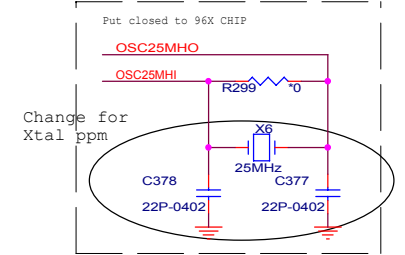
GPIO



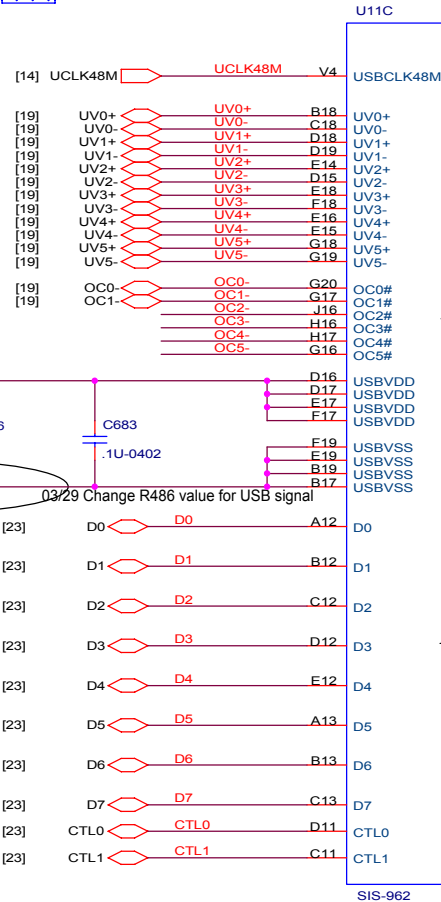
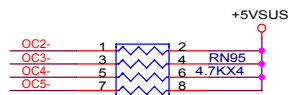
02/28 X7 COMPONENT FROM BG332768721 TO BG33768216



02/28 C399 FROM 20P TO 10P, C400 FROM 15P TO 10P



PROJECT : DT1
Quanta Computer Inc.



OTHERS

USB

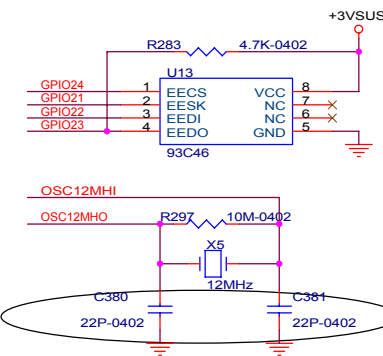
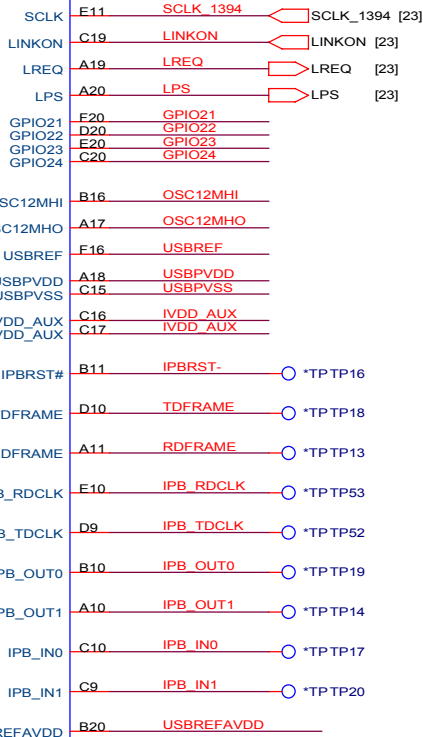
962-3

ACR-IPB
/ADSL
(For 962,963)

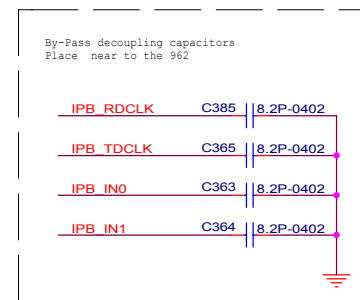
ACR-WIRELESS
/BLUETOOTH
(ONLY FOR 963)

USBREFAVDD

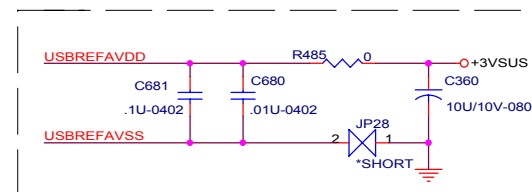
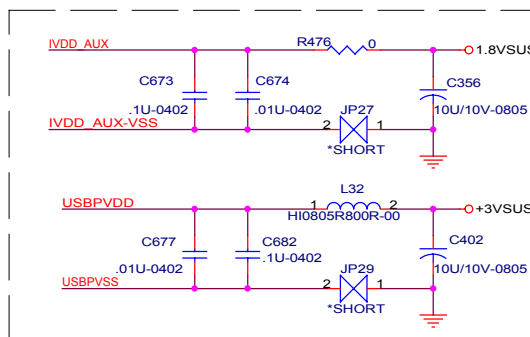
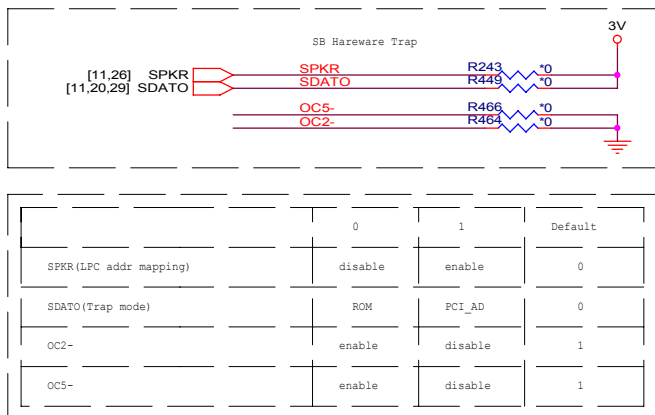
SIS-962



3/29 Modify for Xtal

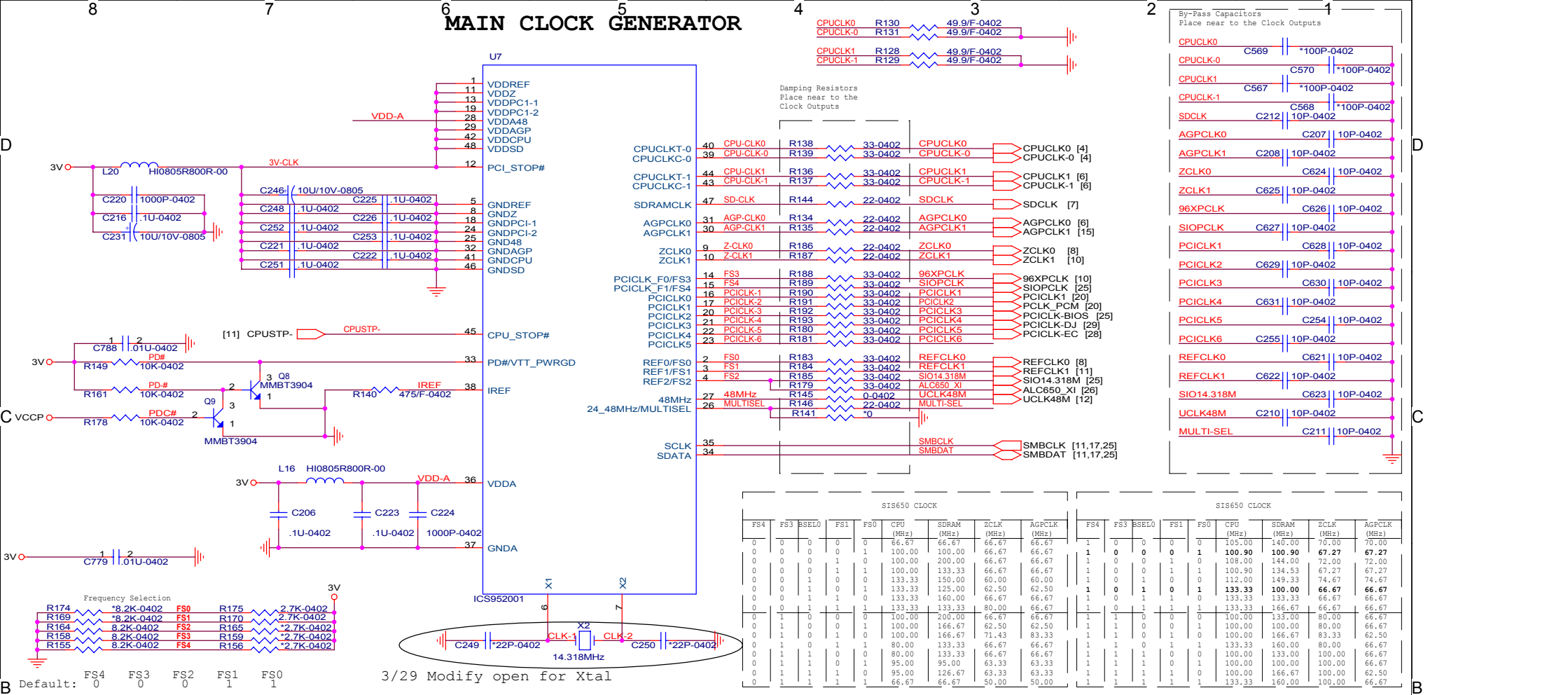


By-Pass decoupling capacitors
Place near to the 962

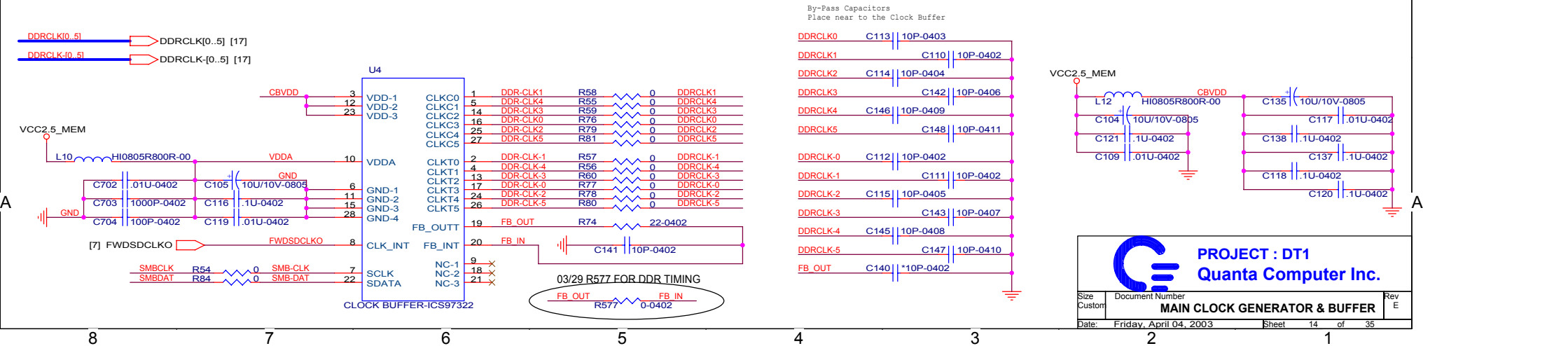


PROJECT : DT1
Quanta Computer Inc.

MAIN CLOCK GENERATOR

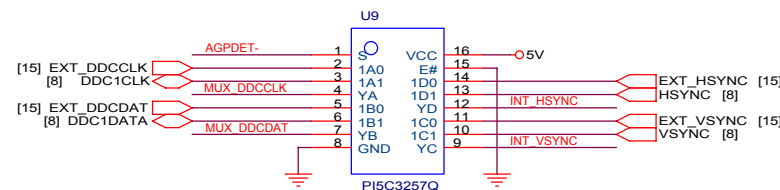
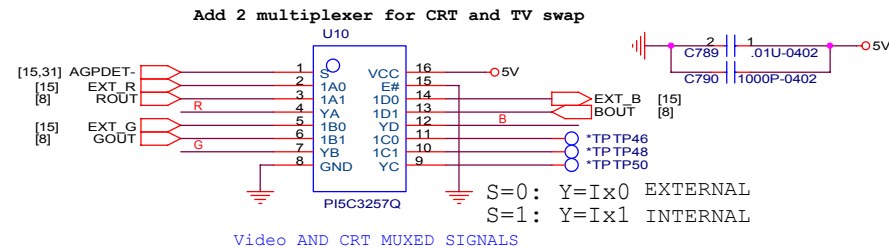
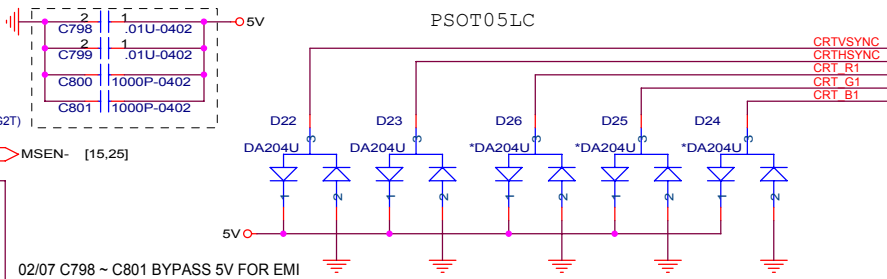
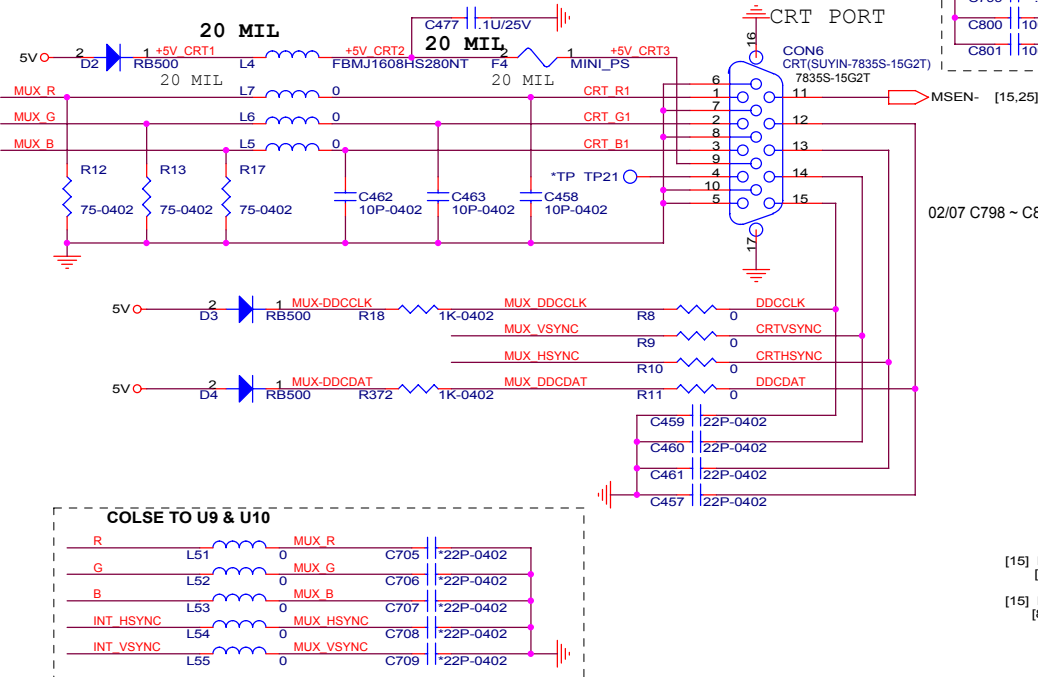


CLOCK BUFFER

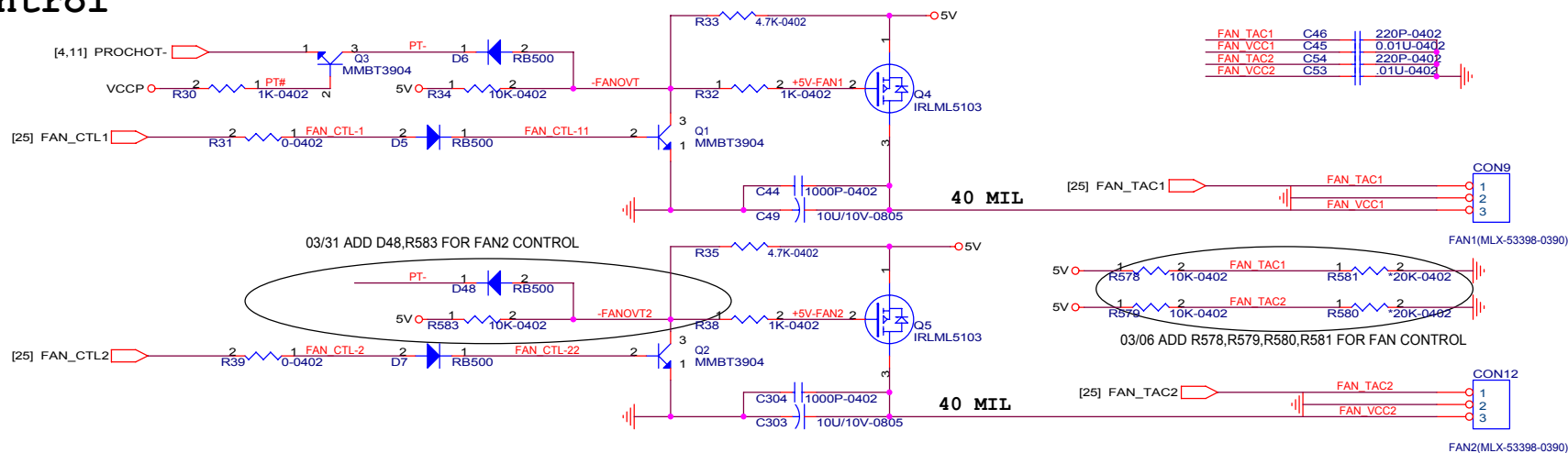


PROJECT : DT1
Quanta Computer Inc.

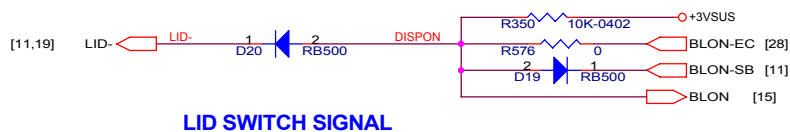
CRT



FAN Control

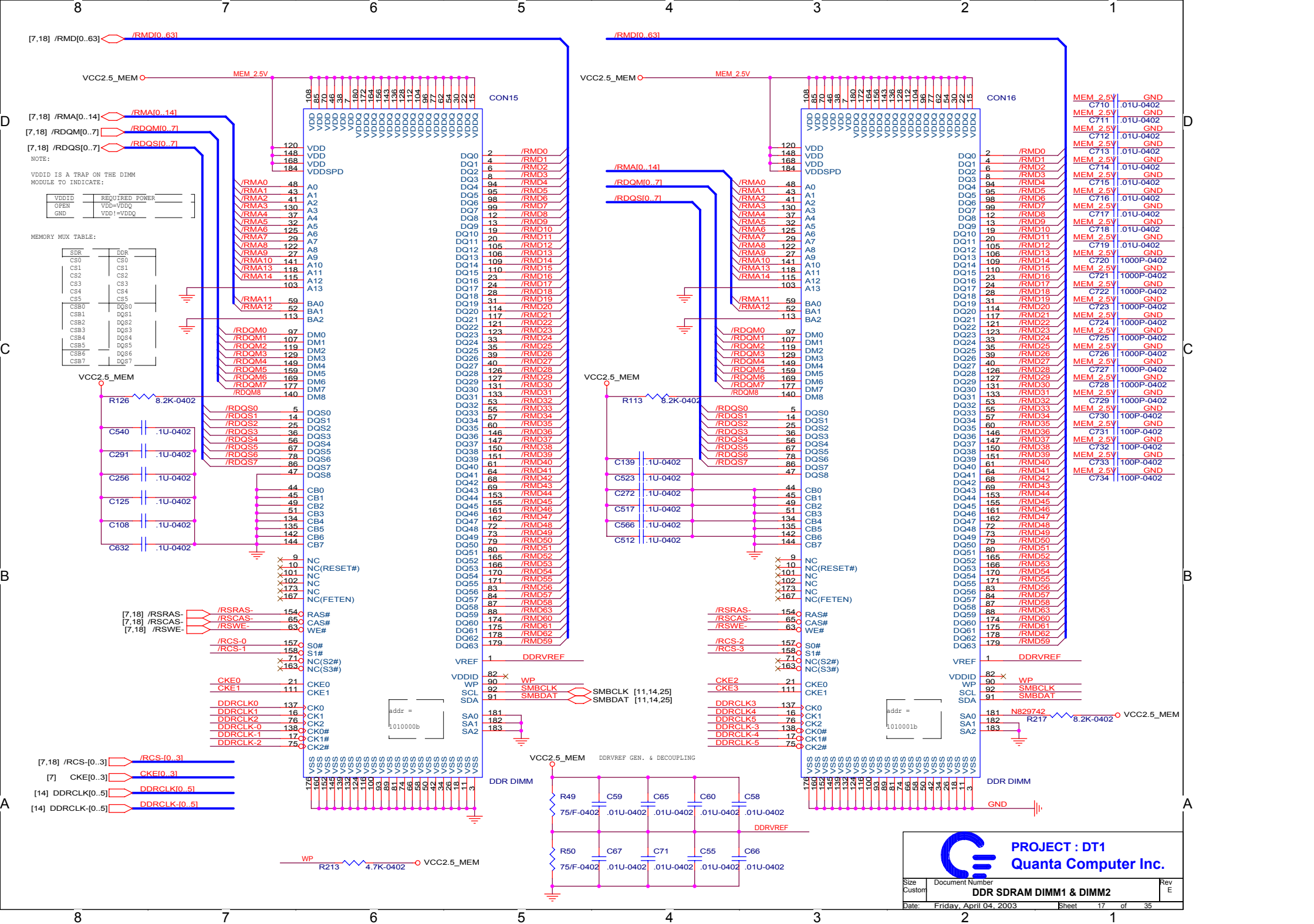


LCD-LID



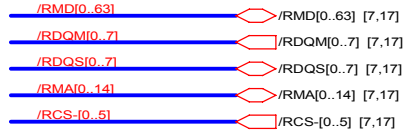
PROJECT : DT1
Quanta Computer Inc.

Size: Custom
Document Number: CRT,LCD LID,BLON & FAN CONTROL
Date: Friday, April 04, 2003
Sheet: 16 of 35
Rev: E

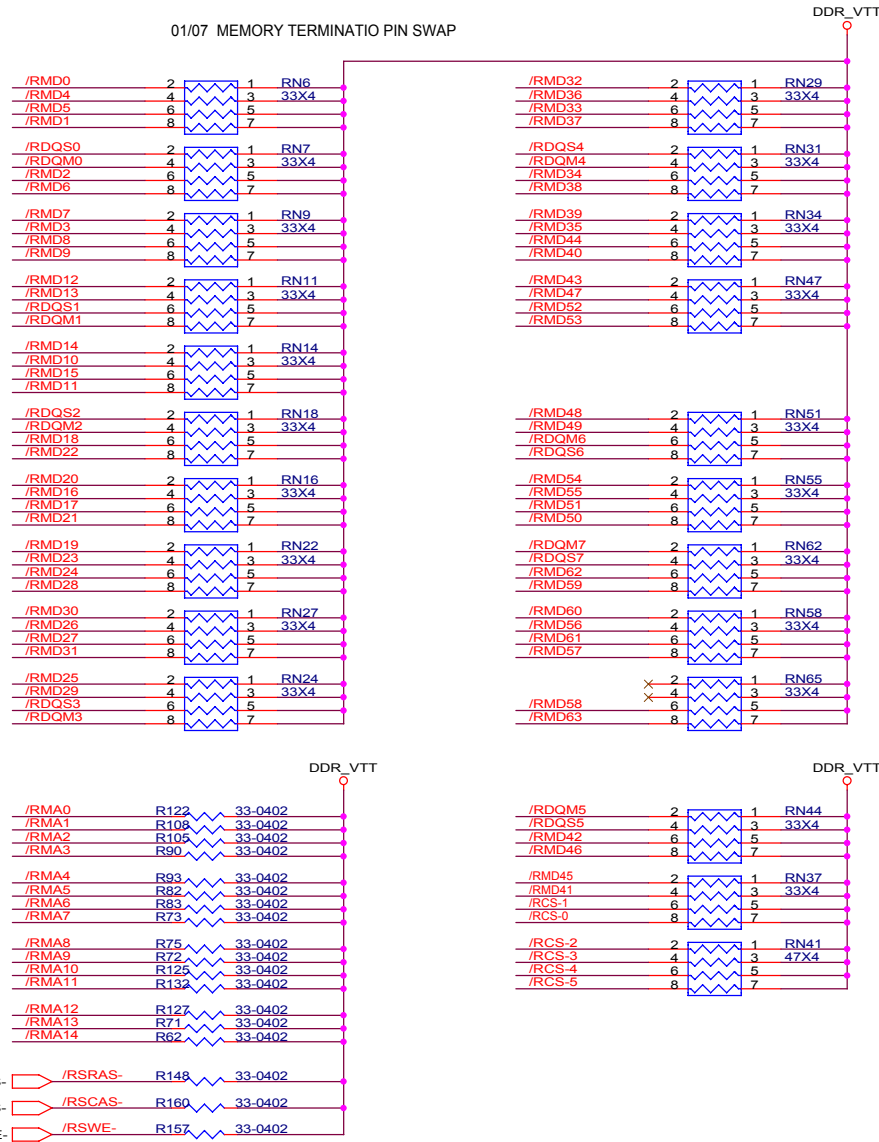


SSTL-2 Termination Resistors

	SDR		DDR		
MD/DQM (/DQS)	LV-CMOS	Rs	SSTL-2	Rs	Rtt
MA/Control	LV-CMOS	0/10/-	SSTL-2	10	33
CS	LV-CMOS	10	SSTL-2	0	33
CKE	OD 3.3V	0	SSTL-2	0	47
			OD 2.5V		

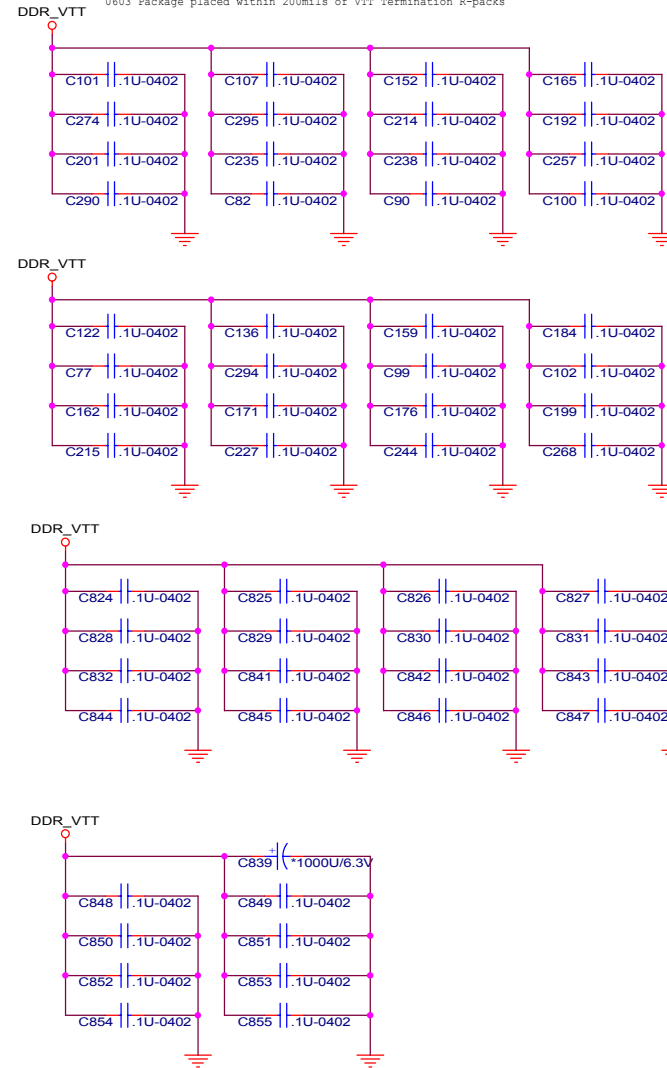


01/07 MEMORY TERMINATIO PIN SWAP



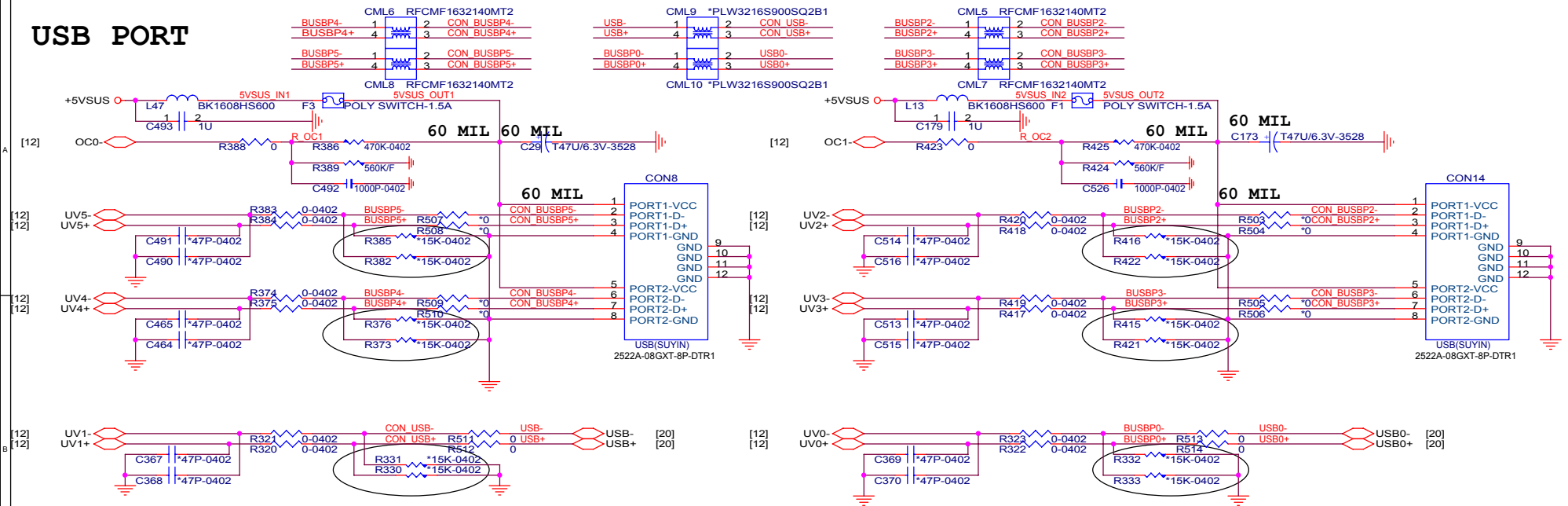
DECOUPLING CAPACITOR FOR SSTL-2 END TERMINATION VTT ISLAND

0603 Package placed within 200mils of VTT Termination R-packs



PROJECT : DT1
Quanta Computer Inc.

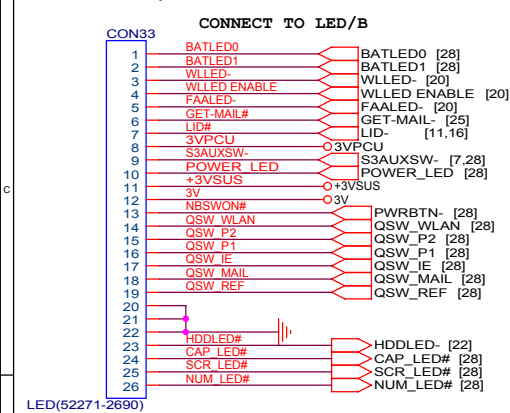
USB PORT



LED/B CONNECTOR

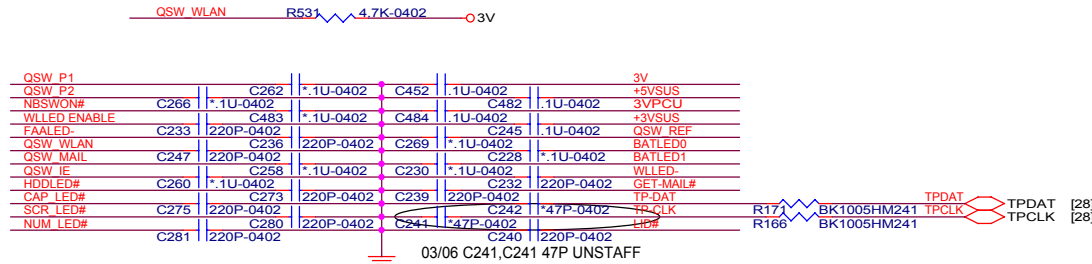
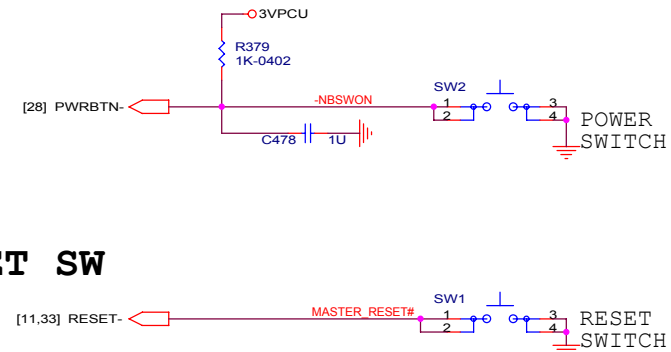
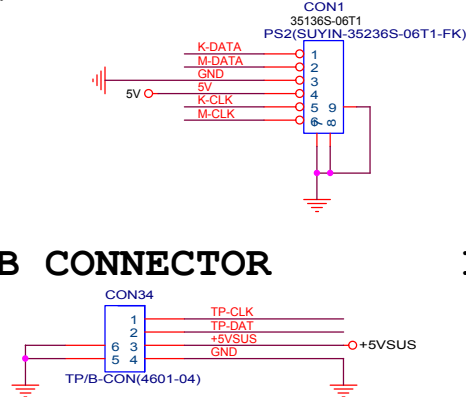
PS/2

POWER SW



TP/B CONNECTOR

RESET SW



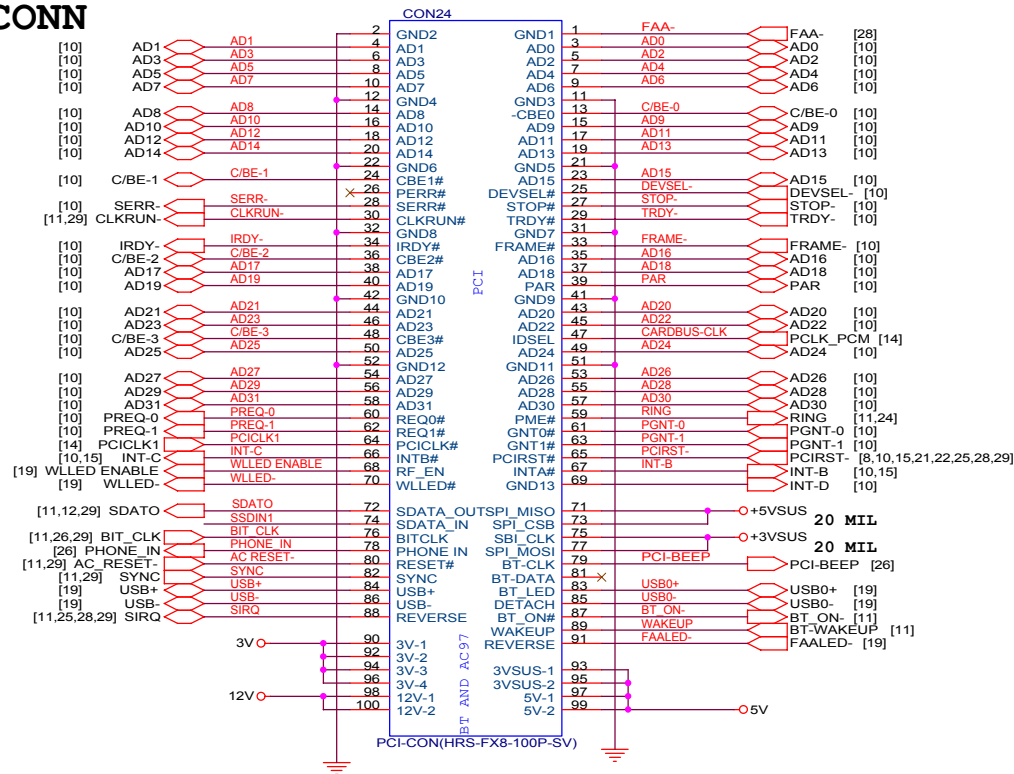
02/28 C45,C455,C456,C457 FROM 100P CHANGE TO 270P FOR EMI



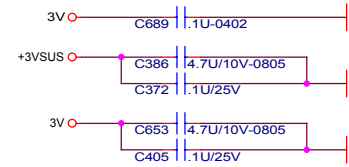
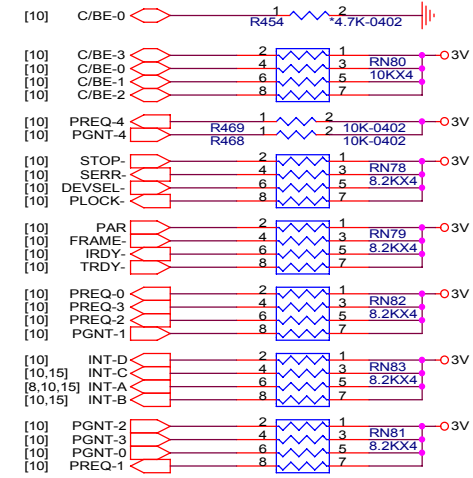
PROJECT : DT1
Quanta Computer Inc.

Size: Custom Document Number: **USB,LED/B,PS2,PW & RST CONN** Rev: E
Date: Friday, April 04, 2003 Sheet: 19 of 35

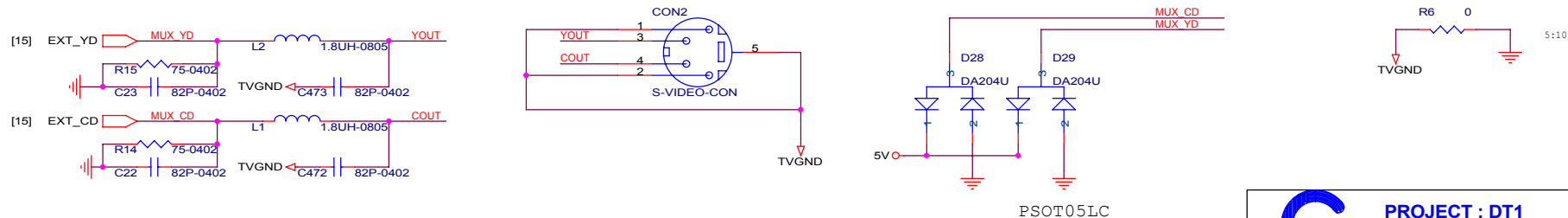
PCI-CONN

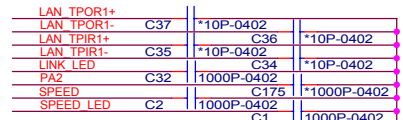
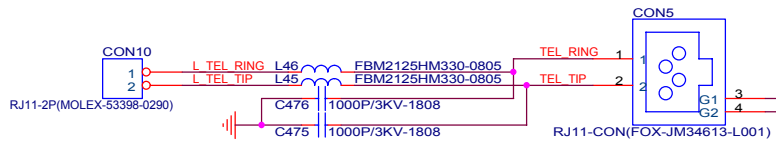
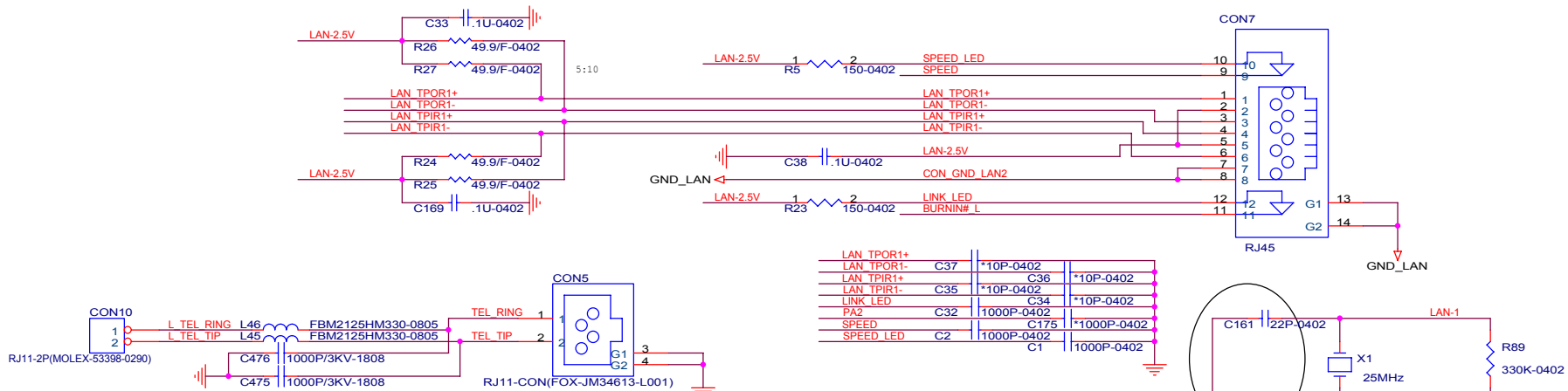


PCI PULL UP



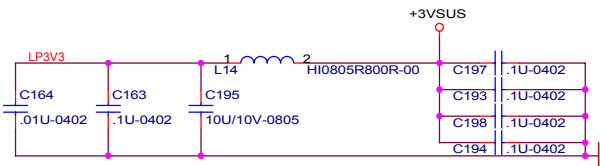
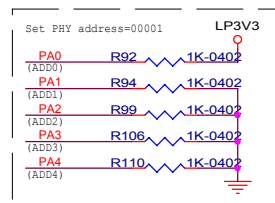
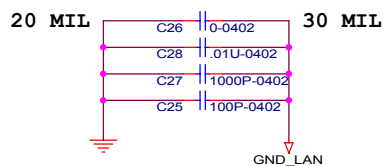
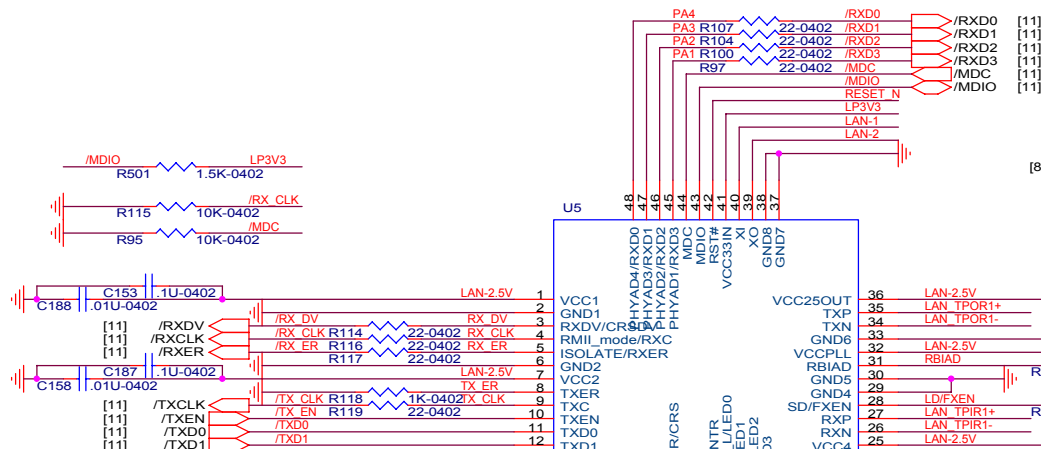
S-VIDEO (TV OUT)





3/29 Modify for Xtal

03/26 Open C52 for PCI reset

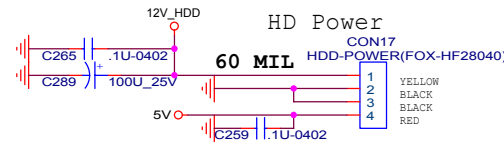


PROJECT : DT1
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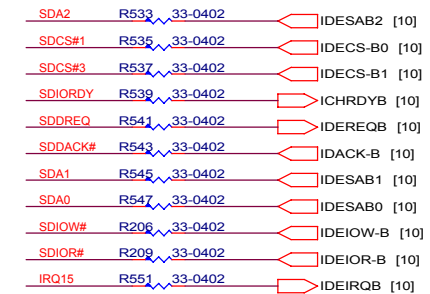
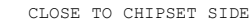
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Document Number: LAN PHY (AC101L) & RJ45,RJ11
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Sheet: 21 of 35
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HDD POWER CONNECTOR

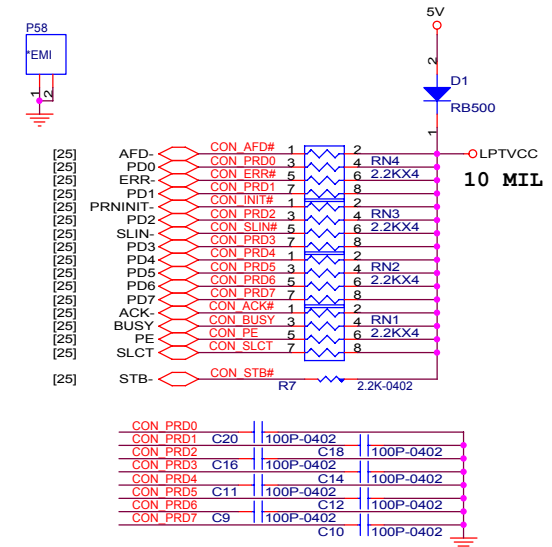
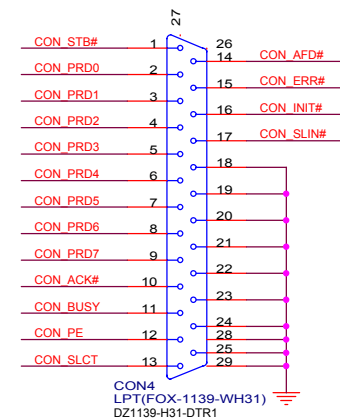
HD Power



CLOSE TO CHIPSET SIDE



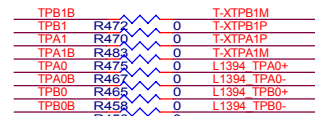
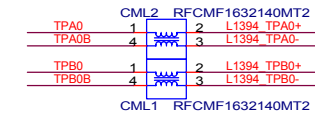
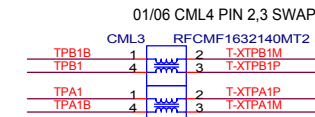
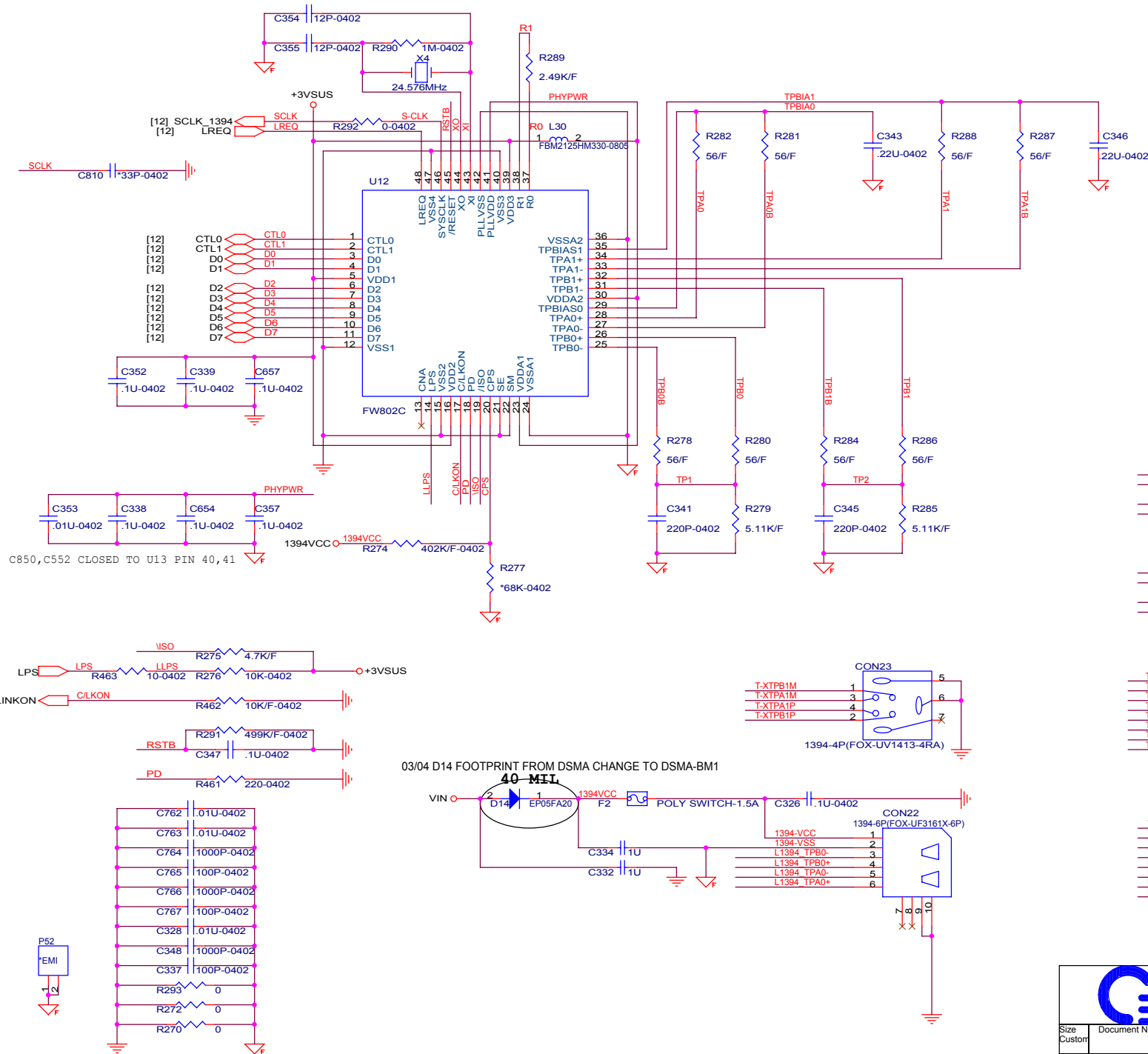
LPT CONN.

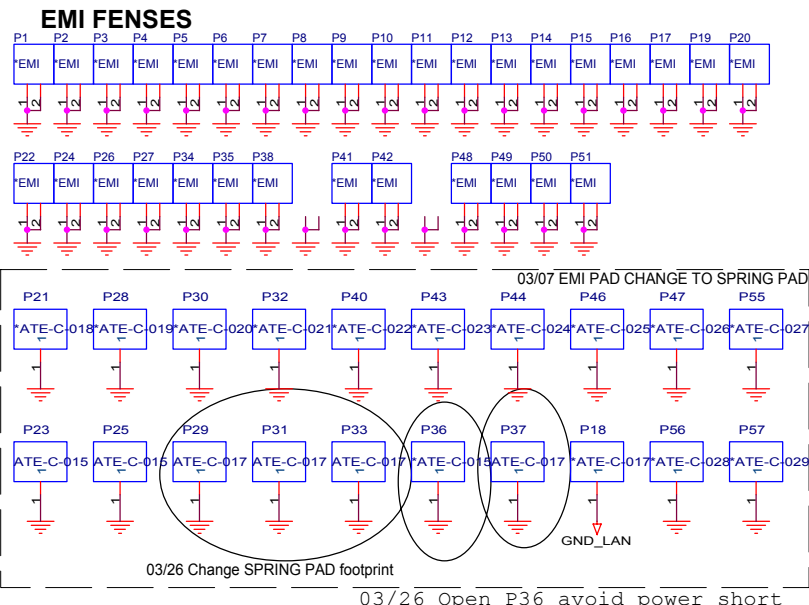
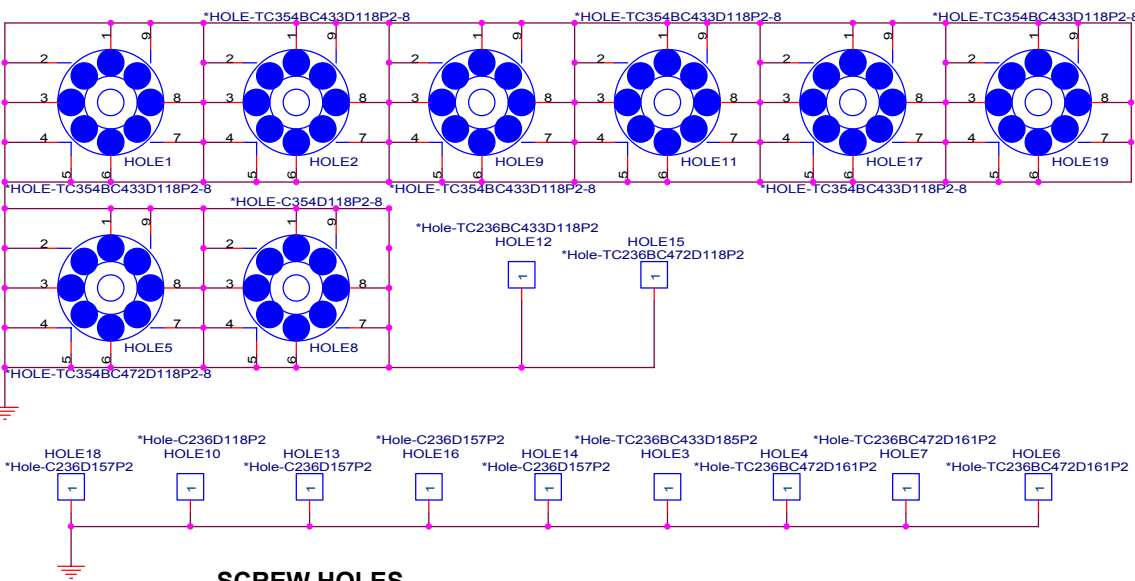


CON STB#			
CON ACK#	C21	100P-0402	
CON BUSY		C7	100P-0402
CON PE	C8	100P-0402	
CON SLCT		C5	100P-0402
CON AFD#	C6	100P-0402	
CON ERR#		C19	100P-0402
CON INIT#	C17	100P-0402	
CON SLIN#		C15	100P-0402
	C13	100P-0402	

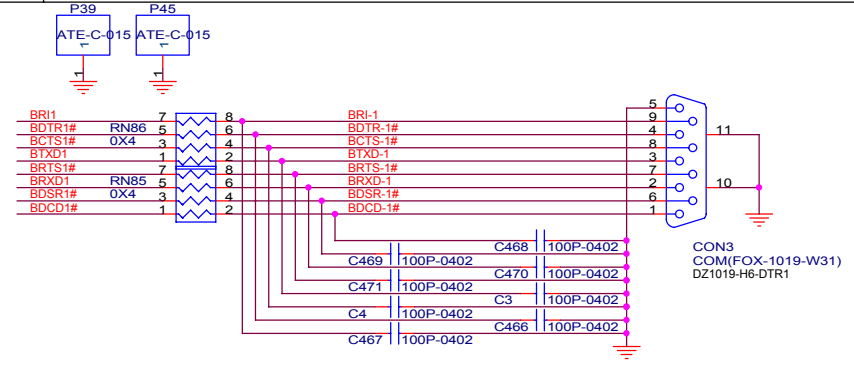
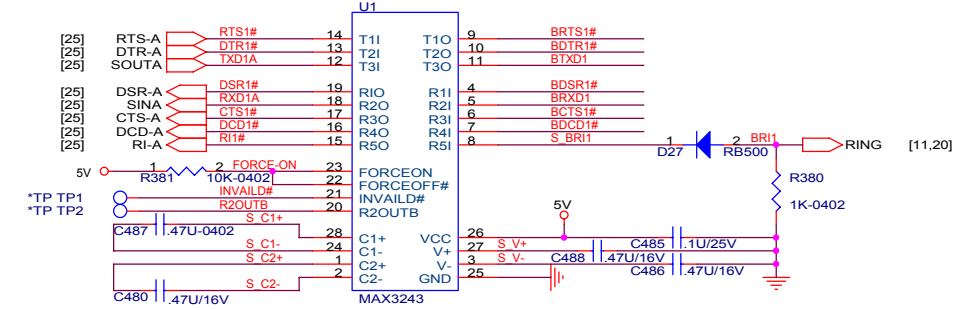
 PROJECT : DT1
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Size Custom	Document Number IDE (HDD & CDROM) & LPT
Date: Friday, April 04, 2003	Sheet 22 of 35





Serial Port

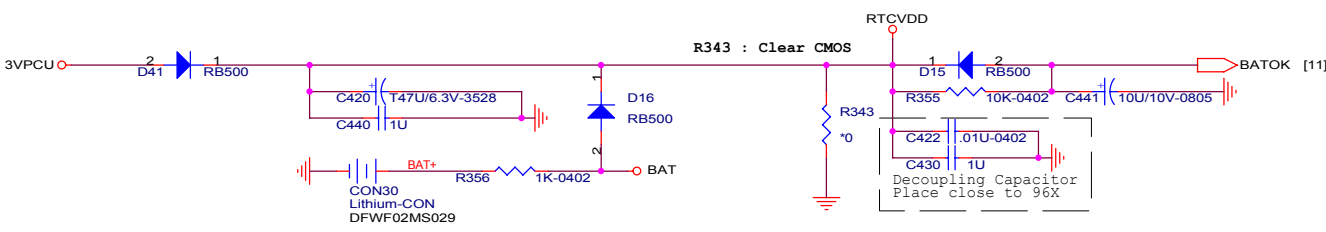
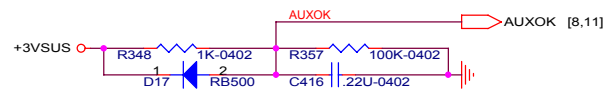
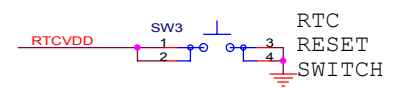


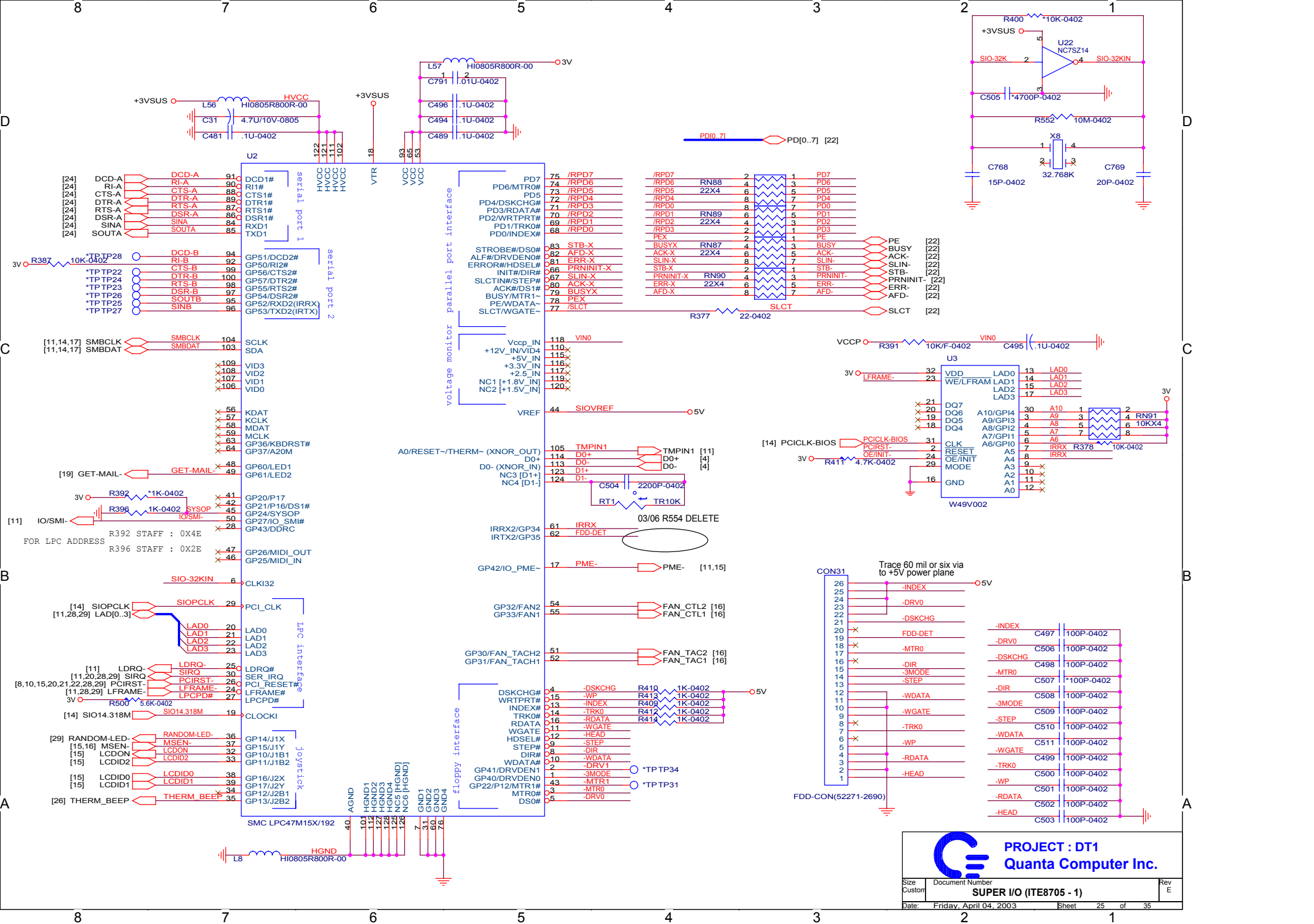
RTC

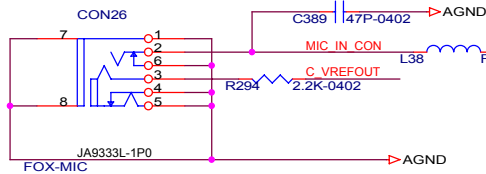
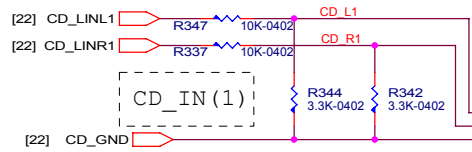
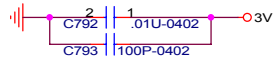
NOTE!

- 1.The RTCVDD is 3V
- 2.Decoupling capacitor must be close to 650 RTCVDD pin.
- 3.RTC circuit must strictly follow SiS's recommended design

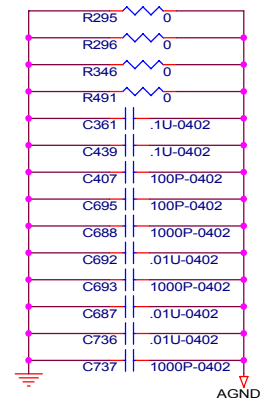
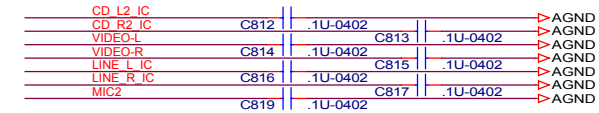
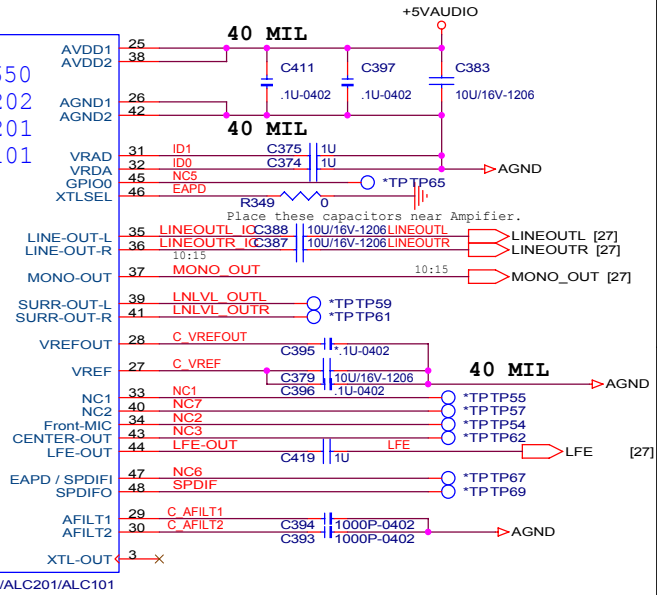
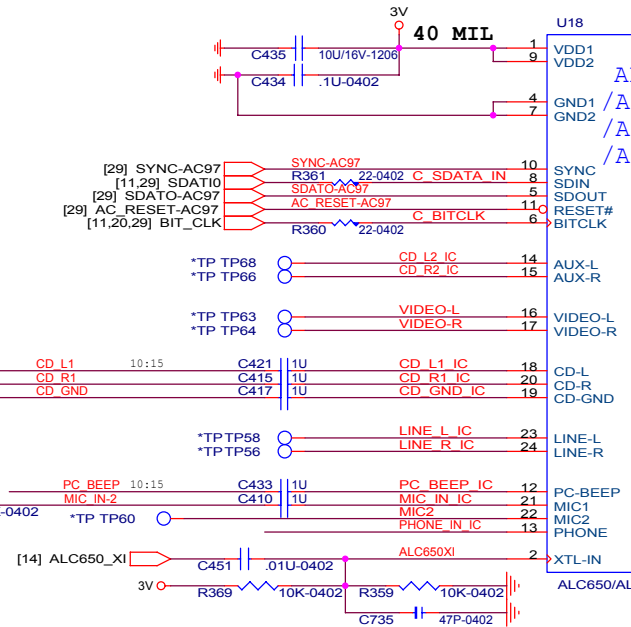
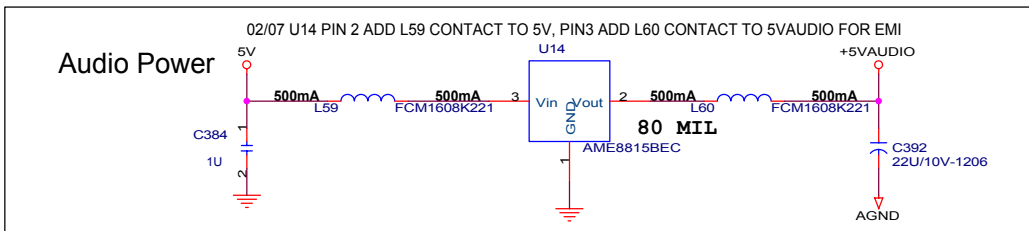
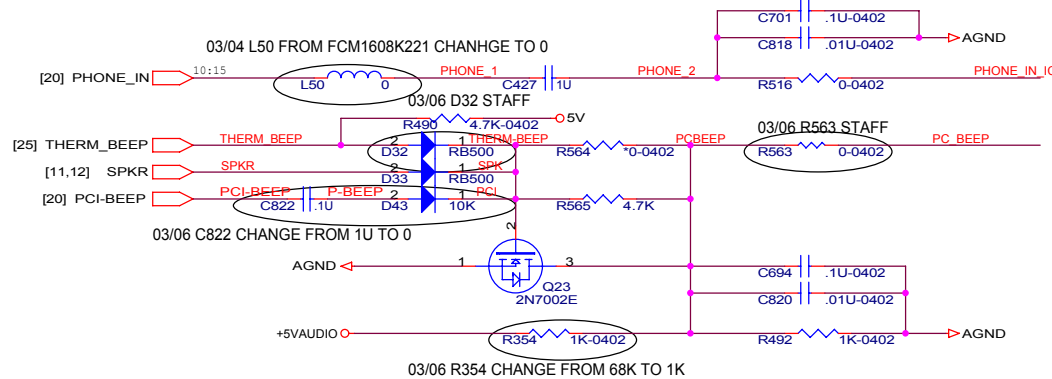
SiS is not responsible for RTC problems from foreign designs.





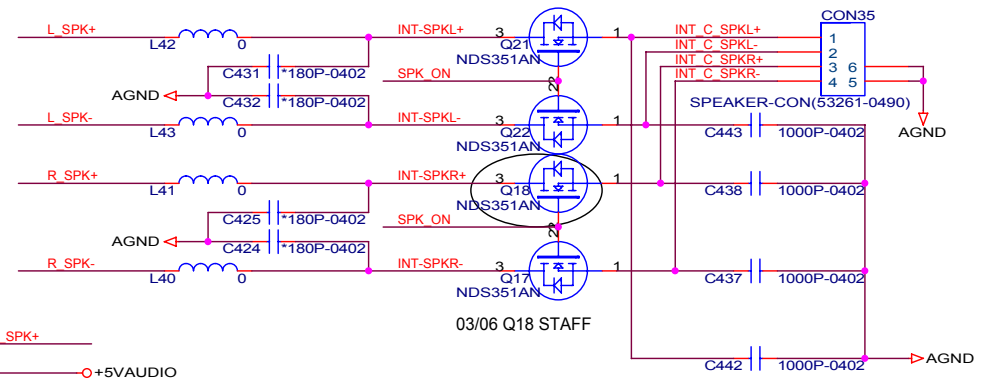
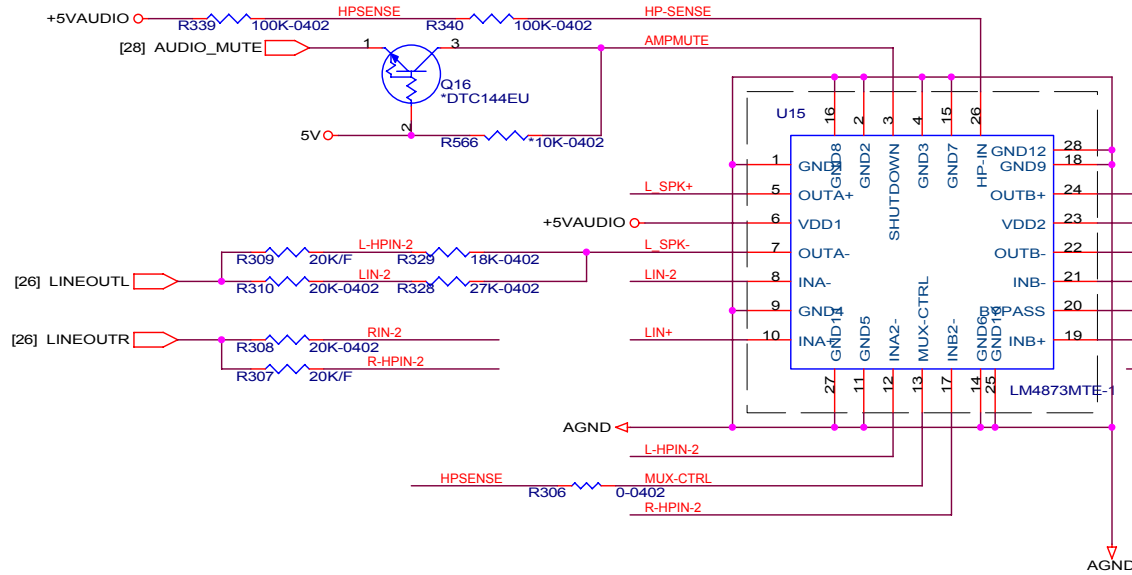


MIC_IN (PINK)

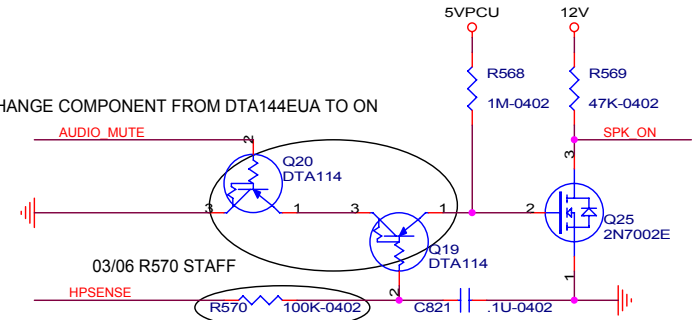


Audio amplifier

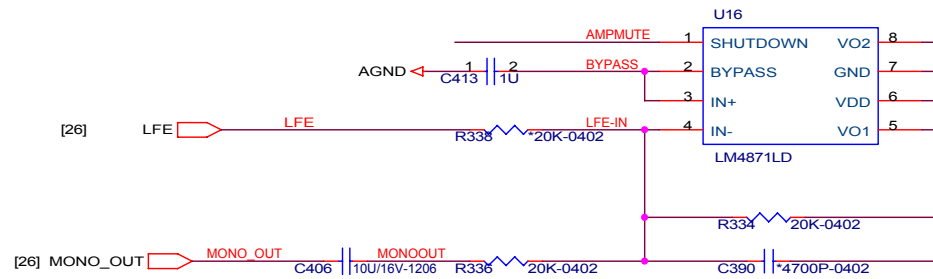
03/06 U15 CHANGE COMPONENT FROM LM4873LQ TO LM4873MTE-1



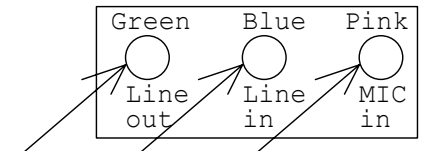
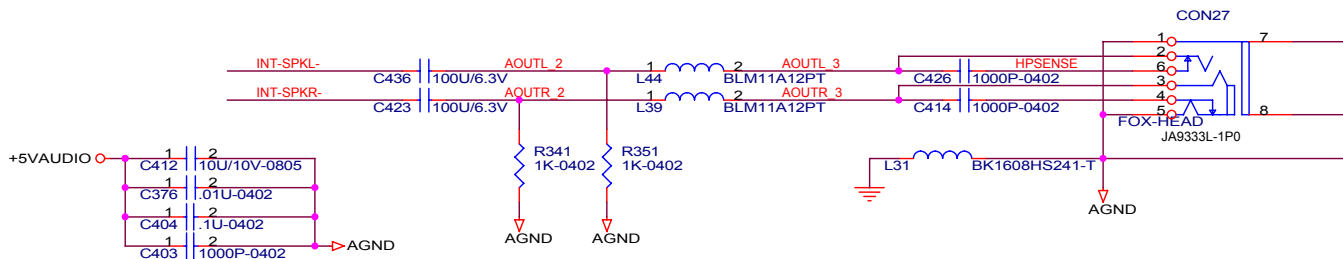
03/06 Q19, Q20 CHANGE COMPONENT FROM DTA144EUA TO ON

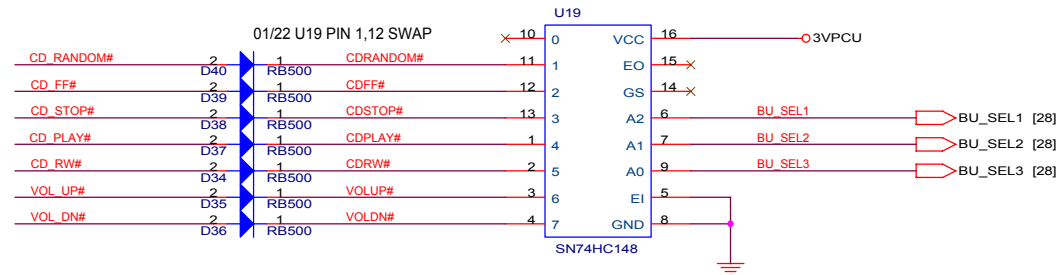
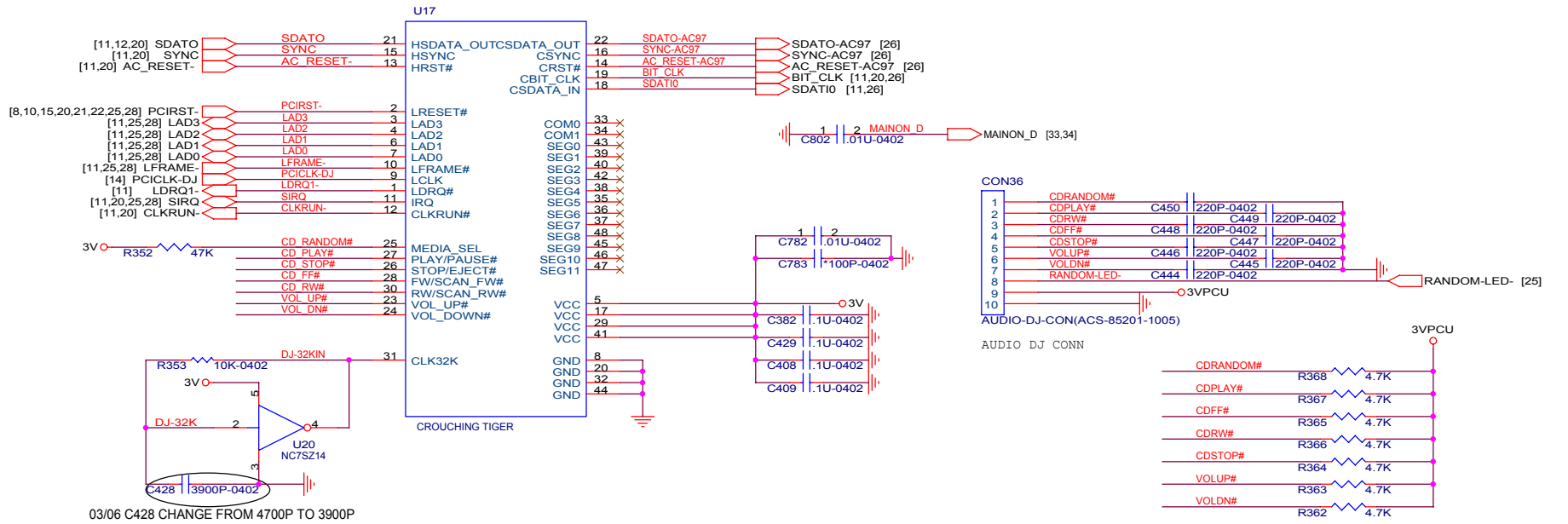


03/06 R570 STAFF

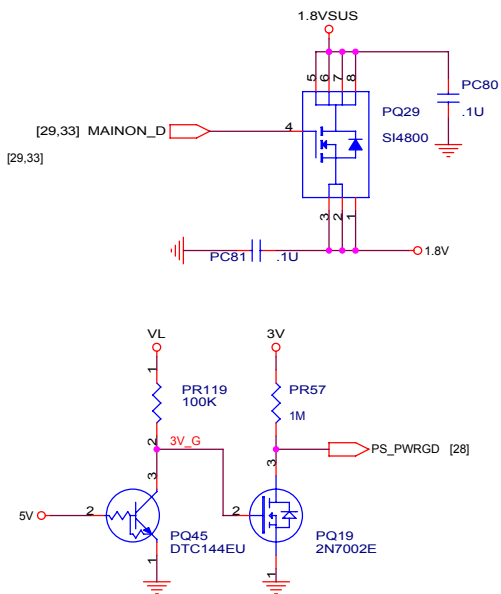
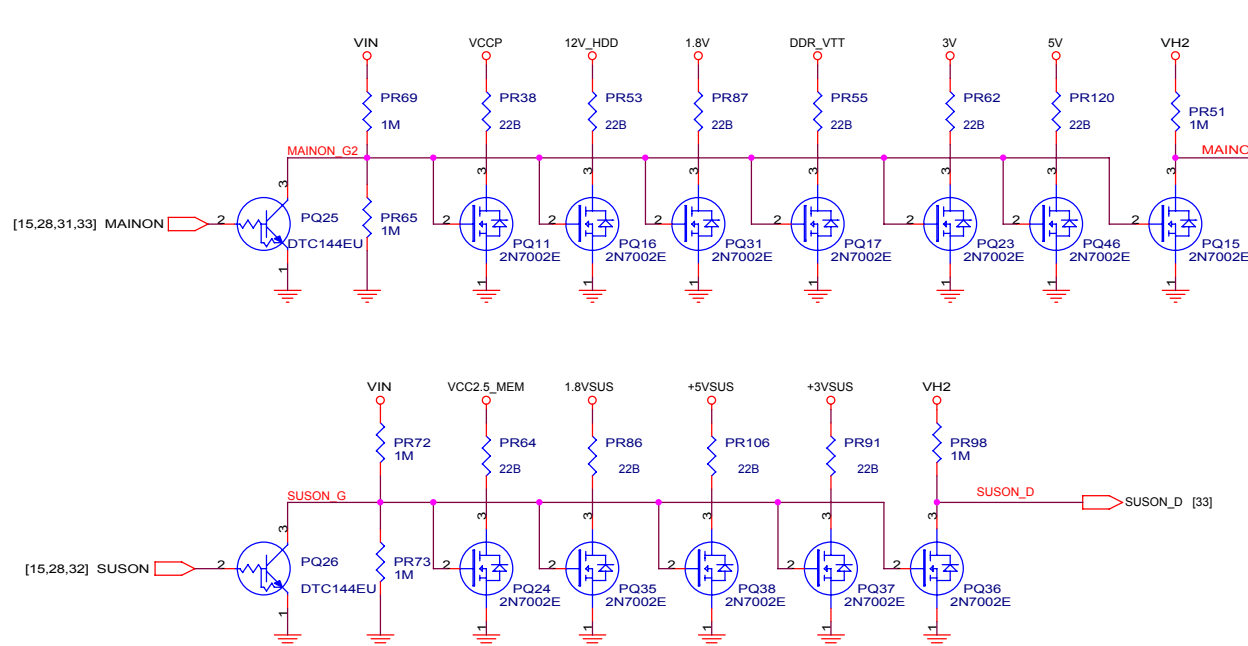
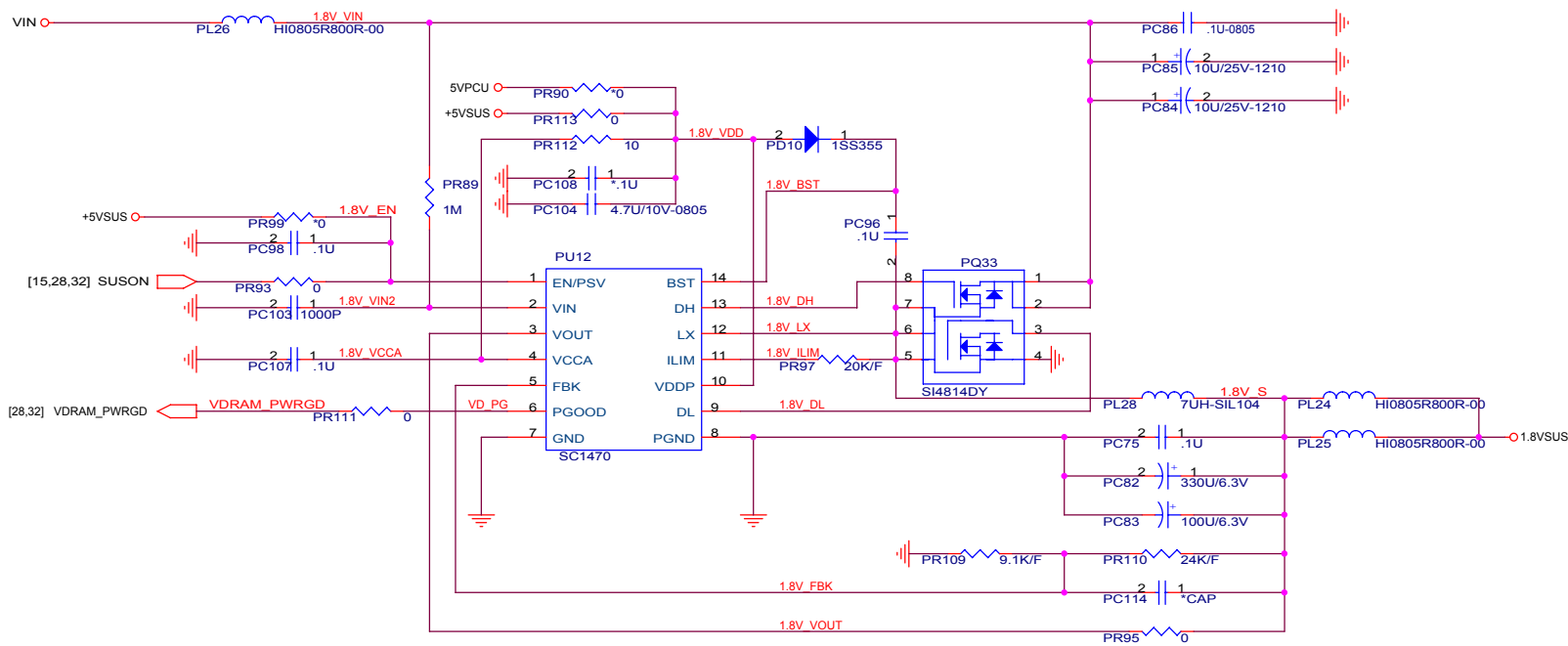


HEADPHONE OUT





SN74HC148 TABLE												
EI	INPUTS							OUTPUTS				
	0	1	2	3	4	5	6	7	A2	A1	A0	GS EO
H	X	X	X	X	X	X	X	X	H	H	H	H H
L	H	H	H	H	H	H	H	H	H	H	H	H L
L	X	X	X	X	X	X	X	L	L	L	L	L H
L	X	X	X	X	X	X	L	H	L	L	H	L H
L	X	X	X	X	L	H	H	H	L	H	H	L H
L	X	X	X	L	H	H	H	H	H	L	L	L H
L	X	X	L	H	H	H	H	H	H	L	H	L H
L	X	L	H	H	H	H	H	H	H	H	L	L H
L	L	H	H	H	H	H	H	H	H	H	H	L H



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HIP6301 FOR INTEL Brookdale POWER CKT-DDR

