

[illegible]

CLK-GEN
ICS 952801

Page 2

HOST 200MHz
ZCLK 133MHz
AGP 66MHz
PCI 33MHz
USB 48MHz
REF 14.318MHz

3V/5V

Page 22

3V_ALWAYS
5VPCU
3V_S5
1.8V_S5
3VSUS
5VSUS
+3V
+5V
15V

2.5V/1.25V

Page 23

2.5VSUS
1.25VREF
+2.5V
DDR_VTT

**1.2V/1.5V
1.8V**

Page 24

+1.2V_HT
+1.5V
+1.8V

CPU CORE

Page 25

VCC_CORE

**BATTERY
CHARGER**

Page 26

DDR SO-DIMM

Page 5

DDR 333

CPU
AMD Athlon64
SMT uPGA754

Page 3,4

HyperTransport
16x16
1600MT/s

NB
SIS M760GX
(698 PIN BGA)

Page 6,7,8

MuTIOL(1GB/s)

HDD
Primary Master

Page 19

ATA 66/100

ODD
Secondary Master

Page 19

ATA 66/100

USB
3x connector

Page 15

USB 2.0

MINI USB
(BLUETOOTH)

Page 15

SB
SIS 963L
(371 PIN BGA)

Page 11,12,13

Int. Keyboard
87-Key

Page 21

Touch Pad
6-Button

Page 21

EC
NS PC97551

Page 20

LPC

Thermal
Thermal sensor & Fan

ZL5
Block Diagram

RGB

CRT
1x D-SUB 15-Pin

Page 10

LVDS

LVDS Transmitter
SIS302ELV

Page 9

LCD
15" XGA/WXGA

Page 10

REQ0#, GNT0#
INTB#, INTC# IDSEL : AD22

Mini PCI
WLAN 802.11A/G

Page 15

Antenna

REQ1#, GNT1#
INTD# IDSEL : AD17

CardBus
TI PCI1410

Page 14

PC Card
1x type-I/II

MII

LAN PHY
RTL8201CP

Page 16

Transformer

Page 16

RJ-45

Page 16

AC'97 2.1

MDC1.5
56K MODEM

Page 17

RJ-11

Page 16

AC97 Codec
ALC203

Page 17

MIC-In Jack

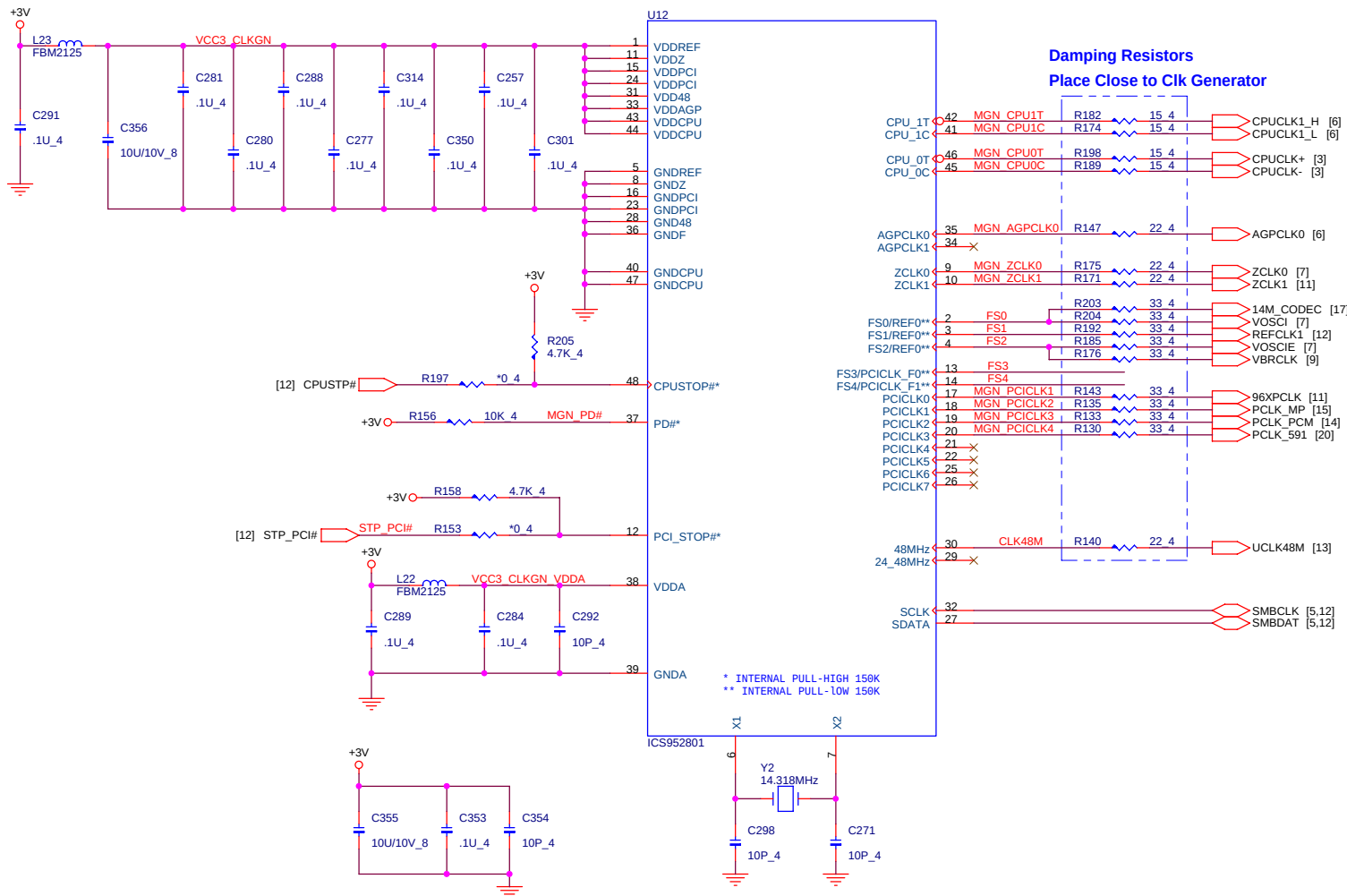
Line-In Jack

AMP
MAX9755

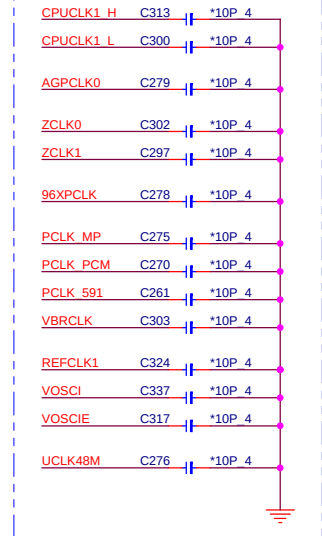
Page 18

HP-Out Jack

Int. Speaker



By-Pass Capacitors Place Close to Clock Generator



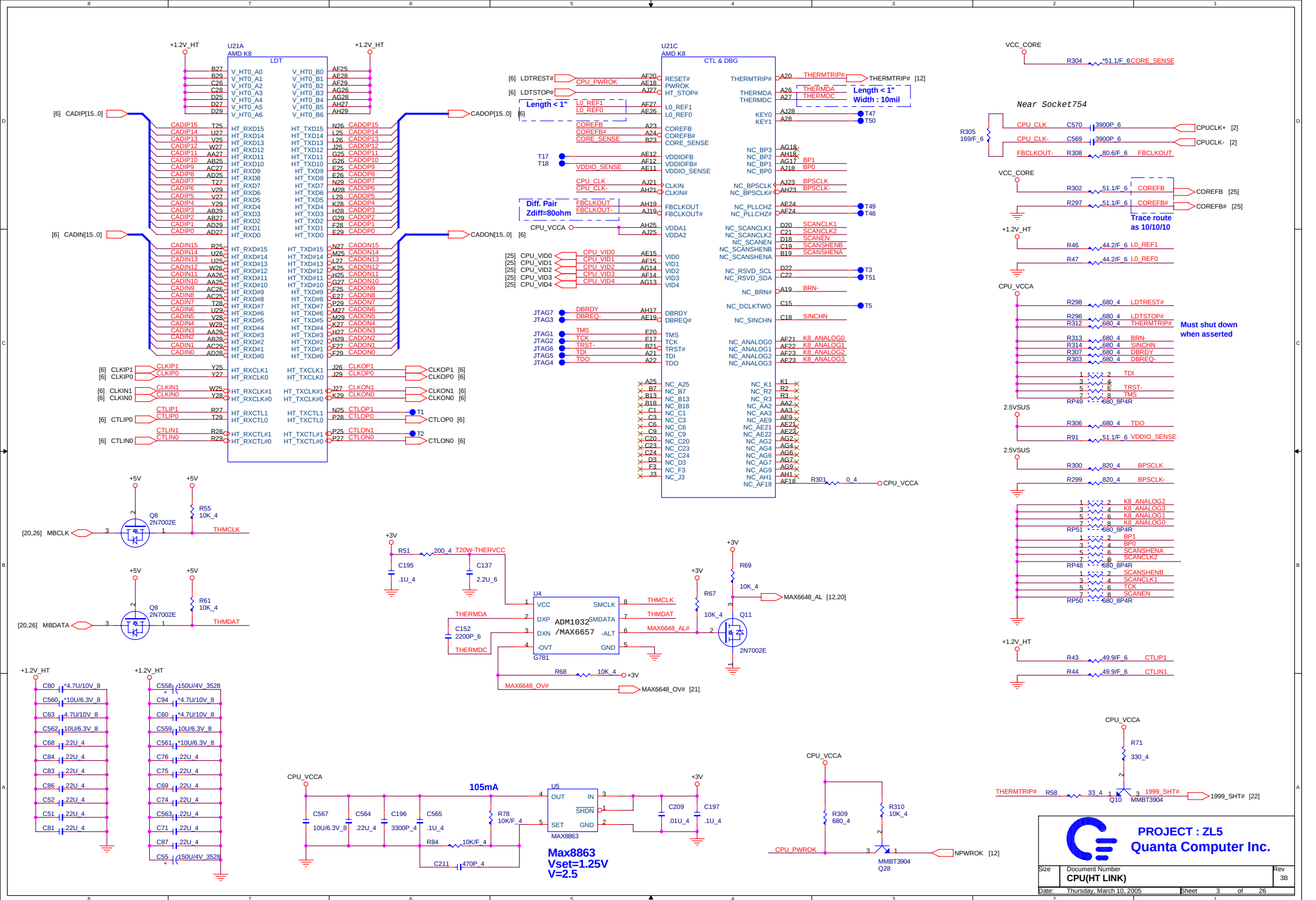
Frequency Selection



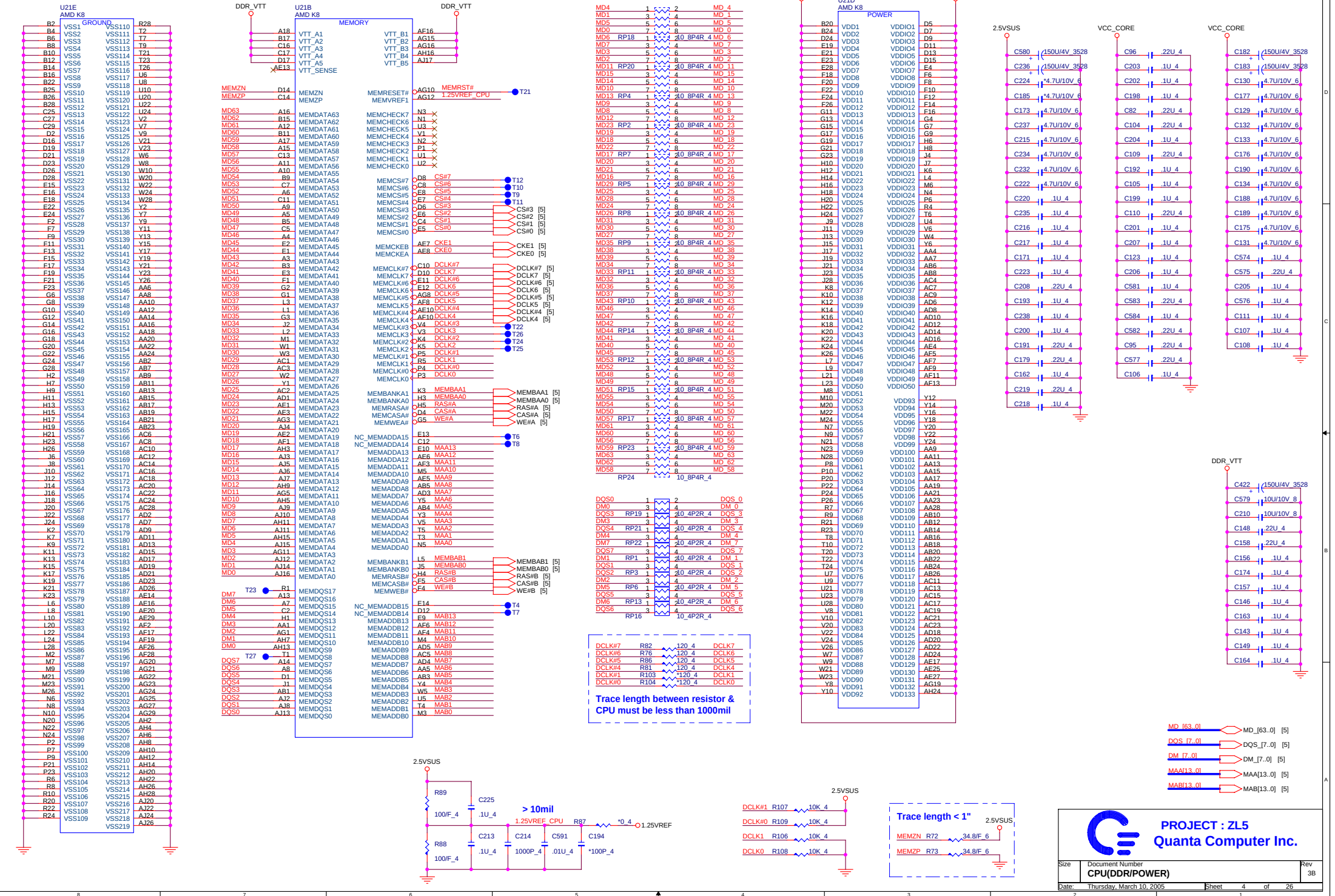
CLK Table for SiS M760 (Not For ICS ICS-952801)

SiS 755/M760 CLOCK									
(FS4)	(FS3)	(FS2)	(FS1)	(FS0)	CPU (MHz)	ZCLK (MHz)	AGPCLK (MHz)	PCI (MHz)	VCO (MHz)
0	0	0	0	0	200	66.66	66.66	33.33	400
0	0	0	0	1	200	100	66.66	33.33	400
0	0	0	1	0	200	133.33	66.66	33.33	400
0	0	0	1	1	200	166.66	66.66	33.33	1000
0	0	1	0	0	233	66.66	66.66	33.33	466
0	0	1	0	1	233	93.2	66.66	33.33	466
0	0	1	1	0	233	133.28	66.66	33.33	933
0	0	1	1	1	233	139.8	69.9	33.33	699
0	1	0	0	0	266	66.66	66.66	33.33	266
0	1	0	0	1	266	106.4	66.5	33.33	532
0	1	0	1	0	266	133	66.5	33.33	532
0	1	0	1	1	266	159.6	66.5	33.33	798
0	1	1	0	0	200	133	50	33.33	400
0	1	1	0	1	200	114	66.66	33.33	800
0	1	1	1	0	200	142	66.66	33.33	1000
0	1	1	1	1	200	160	66.66	33.33	800

SiS 755/M760 CLOCK									
(FS4)	(FS3)	(FS2)	(FS1)	(FS0)	CPU (MHz)	ZCLK (MHz)	AGPCLK (MHz)	PCI (MHz)	VCO (MHz)
1	0	0	0	0	180	135	67.5	33.75	
1	0	0	0	1	185	132.14	66.07	33.04	
1	0	0	1	0	190	135.71	67.08	33.93	
1	0	0	1	1	195	130	65	32.5	
1	0	1	0	0	205	136.66	68.33	34.17	
1	0	1	0	1	210	140	70	35	
1	0	1	1	0	215	129	64.5	32.25	
1	0	1	1	1	220	132	66	33	
1	1	0	0	0	66.66	66.66	66.66	33.33	
1	1	0	0	1	66.66	100	66.66	33.33	
1	1	0	1	0	100	100	66.66	33.33	
1	1	0	1	1	100	133.33	66.66	33.33	
1	1	1	0	0	133	100	66.66	33.33	
1	1	1	0	1	133	133.33	66.66	33.33	
1	1	1	1	0	166	100	66.66	33.33	
1	1	1	1	1	166	133.33	66.66	33.33	



CPU DDR/POWER I/F

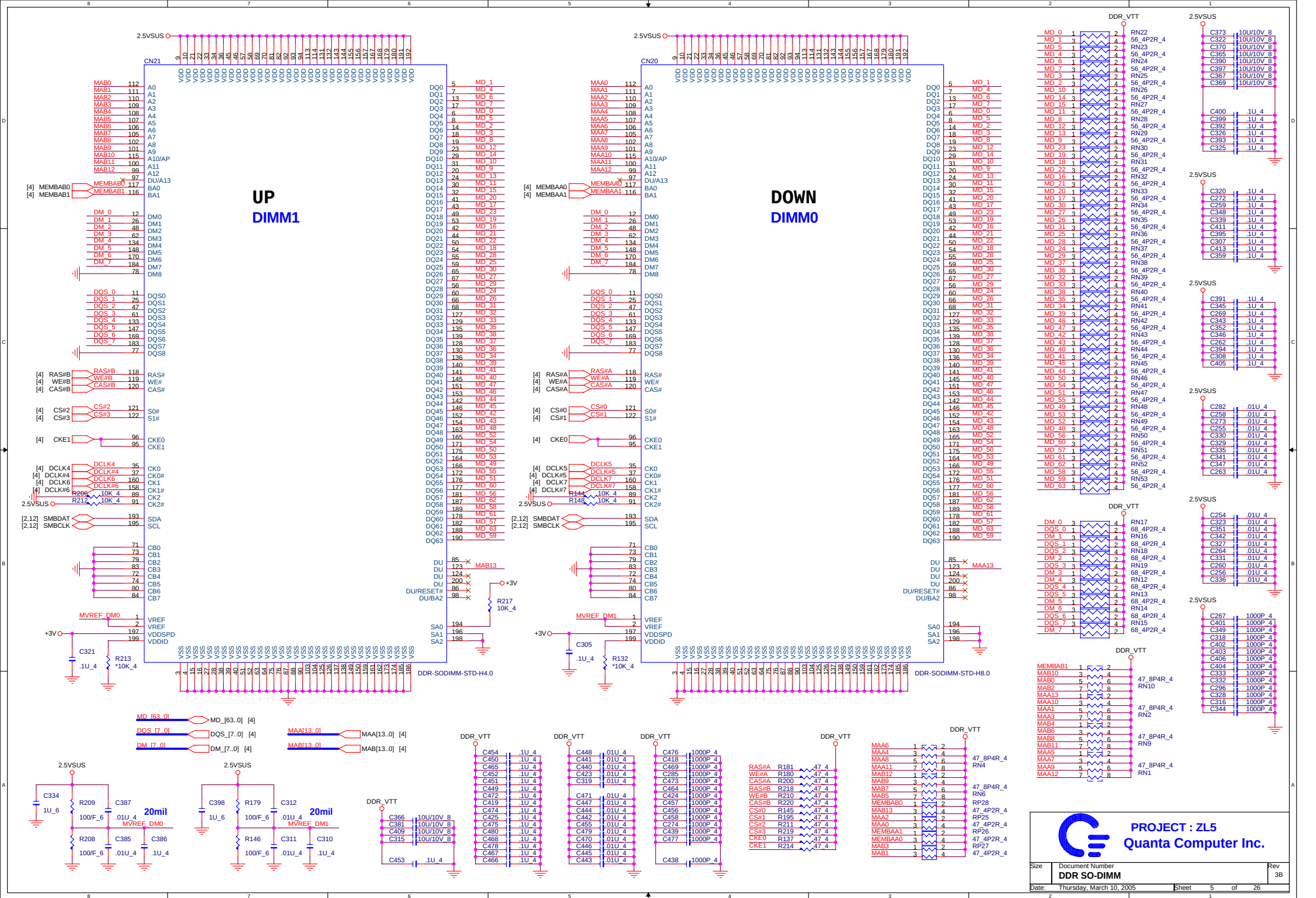


Trace length between resistor & CPU must be less than 1000mil

Trace length < 1"

Size Document Number
CPU(DDR/POWER)

Date: Thursday, March 10, 2005 Sheet 4 of 26 Rev 3B



[3] CADIP[15..0] CADIP[15..0]
[3] CADIN[15..0] CADIN[15..0]
[3] CADOP[15..0] CADOP[15..0]
[3] CADON[15..0] CADON[15..0]

CADIP15
CADIP14
CADIP13
CADIP12
CADIP11
CADIP10
CADIP9
CADIP8
CADIP7
CADIP6
CADIP5
CADIP4
CADIP3
CADIP2
CADIP1
CADIP0
CADIN15
CADIN14
CADIN13
CADIN12
CADIN11
CADIN10
CADIN9
CADIN8
CADIN7
CADIN6
CADIN5
CADIN4
CADIN3
CADIN2
CADIN1
CADIN0
CADOP15
CADOP14
CADOP13
CADOP12
CADOP11
CADOP10
CADOP9
CADOP8
CADOP7
CADOP6
CADOP5
CADOP4
CADOP3
CADOP2
CADOP1
CADOP0
CADON15
CADON14
CADON13
CADON12
CADON11
CADON10
CADON9
CADON8
CADON7
CADON6
CADON5
CADON4
CADON3
CADON2
CADON1
CADON0

L27 LRCAD_N0
P27 LRCAD_P0
M29 LRCAD_N1
L29 LRCAD_P1
M27 LRCAD_N2
K29 LRCAD_P2
L29 LRCAD_N3
H29 LRCAD_P3
J29 LRCAD_N4
G27 LRCAD_P4
H27 LRCAD_N5
F29 LRCAD_P5
G29 LRCAD_N6
E27 LRCAD_P6
E27 LRCAD_N7
N24 LRCAD_P7
P24 LRCAD_N8
M25 LRCAD_P8
N25 LRCAD_N9
L26 LRCAD_P9
M26 LRCAD_N10
K24 LRCAD_P10
L24 LRCAD_N11
H26 LRCAD_P11
J26 LRCAD_N12
G24 LRCAD_P12
H24 LRCAD_N13
F25 LRCAD_P13
G25 LRCAD_N14
E26 LRCAD_P14
F26 LRCAD_N15
C28 LRCOMP

J25 LRLCK_N1
K25 LRLCK_P1
J27 LRLCK_N0
K27 LRLCK_P0
D29 LRLCTLN
E29 LRLCTLP
A11 HTCLKN
A12 HTCLKP
C11 HTAVDD
B11 HTAVSS
C12 HTPHYAVDD
B12 HTPHYAVSS
E11 LDTSTOP#
D12 LDTREQ#
D11 LDTREST#

M760GX
SBA7
SBA6
SBA5
SBA4
SBA3
SBA2
SBA1
SBA0
ST0
ST1
ST2
AA00
AA01
AA02
AA03
AA04
AA05
AA06
AA07
AA08
AA09
AA10
AA11
AA12
AA13
AA14
AA15
AA16
AA17
AA18
AA19
AA20
AA21
AA22
AA23
AA24
AA25
AA26
AA27
AA28
AA29
AA30
AA31

HOST_RX

HOST_TX

M760-1

LVDS/AGP

CLKINO [3]
CLKIPO [3]
CLKIN1 [3]
CLKIP1 [3]
CTLINO [3]
CTLIPO [3]

[9] VAD[11..0]
[9] VAGCLK
[9] VAHSYNC
[9] VAVSYNC
[9] VADE
[9] VBD[11..0]

[9] VBGCLK
[9] VBHSYNC
[9] VBVSYSN
[9] VBDE
[9] VBCTL1
[9] VBCTL0

H3 AC/BE#3
L4 AC/BE#2
N5 AC/BE#1
R4 AC/BE#0
A6 AREQ#
B6 AGNT#
L6 AFRAME#
L1 AIRDY#
M4 ATRDY#
M5 ADEVSEL#
M1 ASERR#
M2 ASTOP#

N6 APAR
C4 RBF#
A3 WBF#
D6 GC_DET#
G6 PIPE#/ADBIH
E6 ADBIL

C1 SB_STB
C2 SB_STB#
T2 AD_STB0
R1 AD_STB0#
J2 AD_STB1
H1 AD_STB1#

AA1 AGPCLK
V2 AGPRCOMP
V3 AGPRCOMP_N
AA4 A1XAVDD
AA5 A1XAVSS
AA2 A4XAVDD
AA3 A4XAVSS
V1 AVREFGC
V4 AGPVSSREF

20mil
+1.8V
R318 124/F_6
R323 124/F_6
R320 *33_4
C606 *22P_4
Near 200mil

A1XAVDD
R62 0 6
C230 .1U_4
C181 .01U_4
A1XAVSS

A4XAVDD
L48 WB201209B121QNT03
C597 .1U_4
C601 .01U_4
C59 10U/10V_8
A4XAVSS

HTAVDD
L16 WB201209B121QNT03
C145 .1U_4
C153 .01U_4
C56 10U/10V_8
HTAVSS

HTPHYAVDD
L40 WB201209B121QNT03
C566 .1U_4
C568 .01U_4
C47 10U/10V_8
HTPHYAVSS

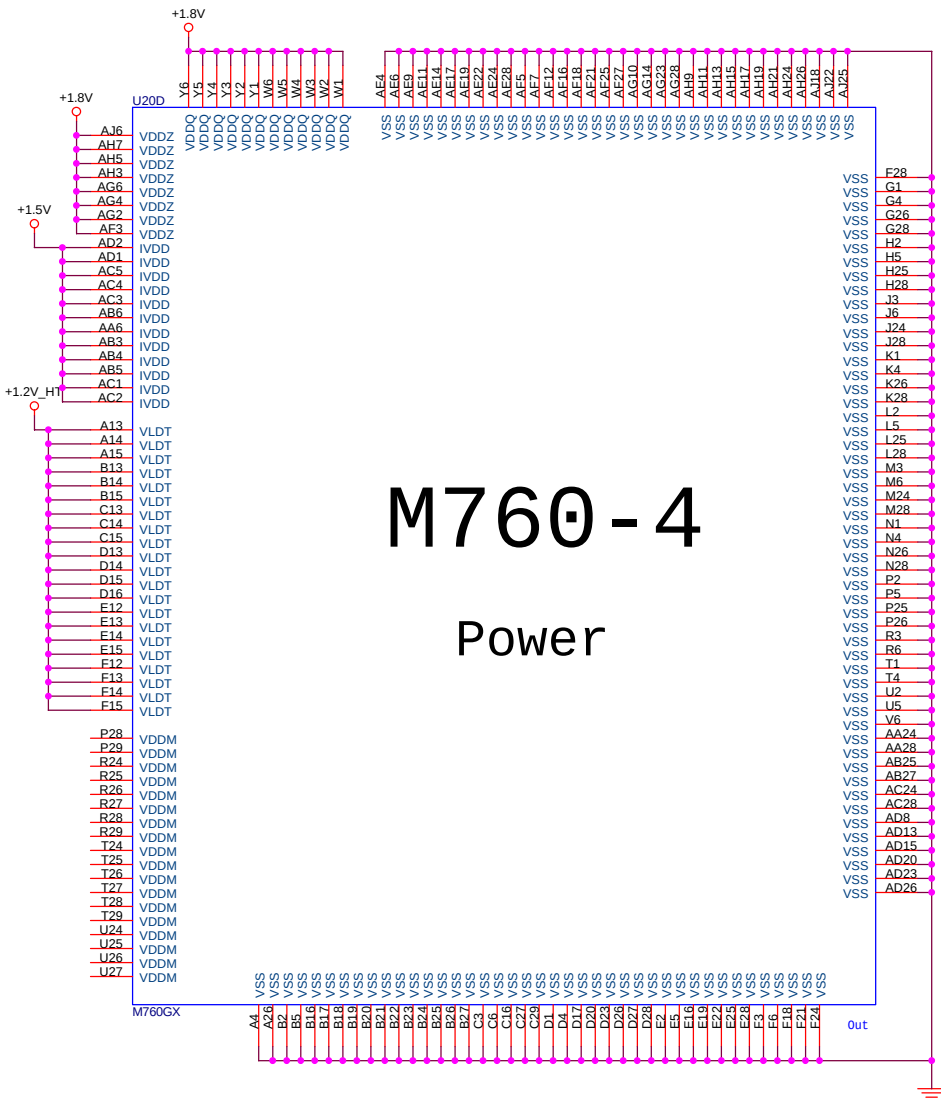
Place close to chip
+1.8V
AGPRCOMP R90 49.9/F 6
CPU_VCCA
+1.2V_HT
LDTREQ# R52 1K 4
LRCOMP R29 100/F 6
LTCOMP R30 49.9/F 6
LTCOMPP R36 49.9/F 6
AGPRCOMP R322 43.2/F 6
VAGCLK C604 *10P 4
VBGCLK C227 *10P 4
MVBCLK C212 *10P 4

+1.2V_HT
R49 75 4
R50 75 4
C136 3900P 6 755CLK-
C122 3900P 6 755CLK+
R53 169/F_6

PROJECT : ZL5
Quanta Computer Inc.

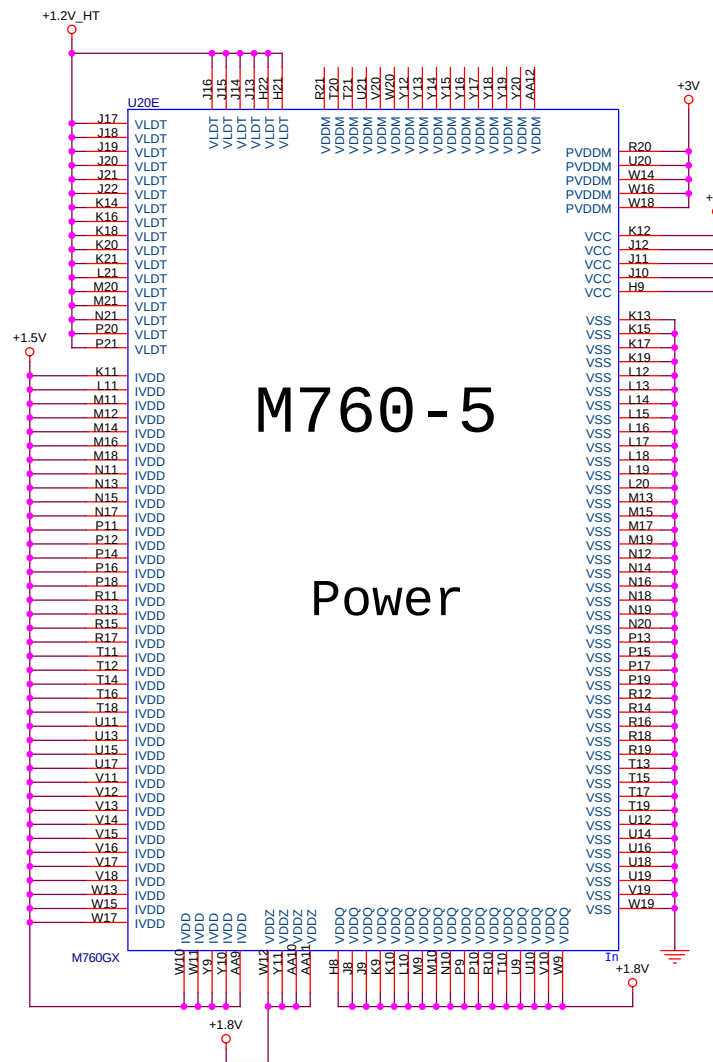
Size Document Number
M760GX(HT LINK/AGP)
Date: Thursday, March 10, 2005 Sheet 6 of 26 Rev 3B

If Support SiS M760LV IVDD=1.5V



M760-4

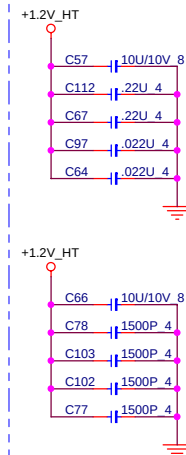
Power



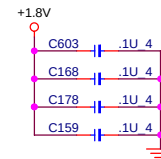
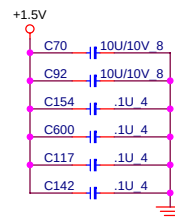
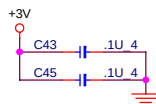
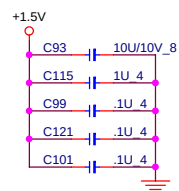
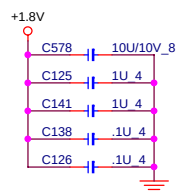
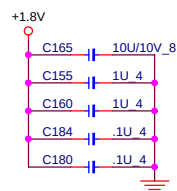
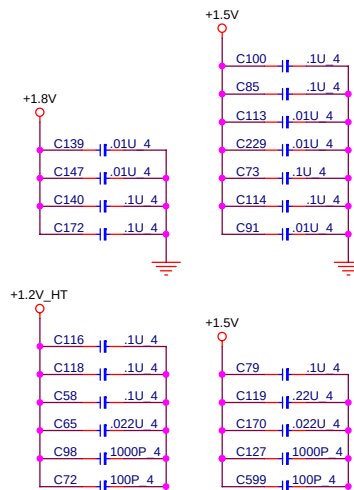
M760-5

Power

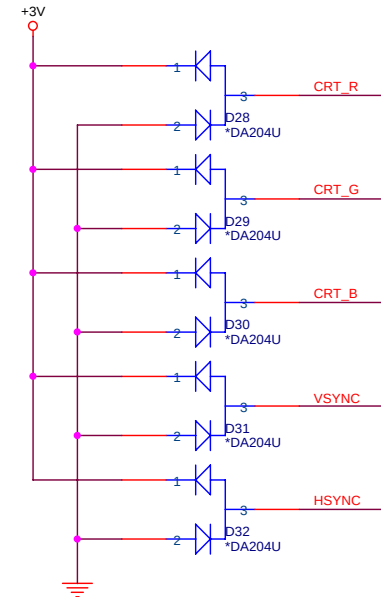
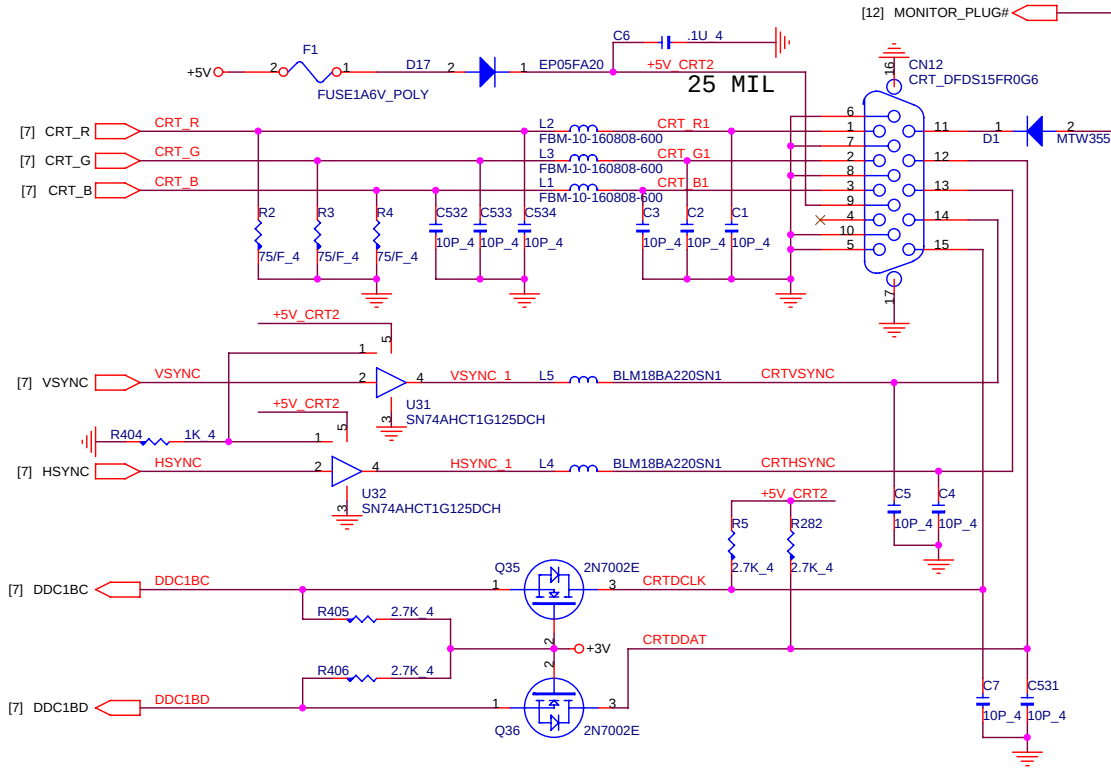
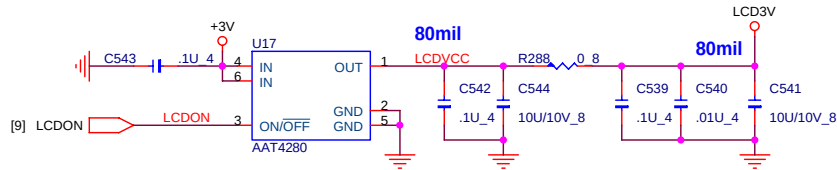
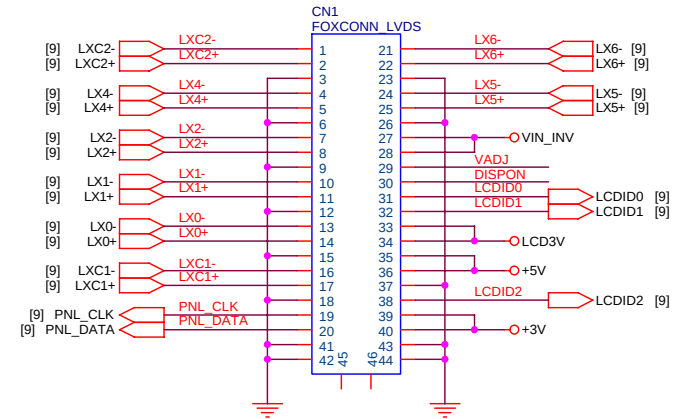
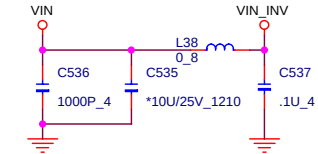
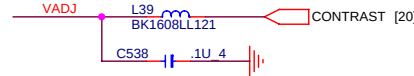
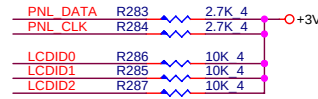
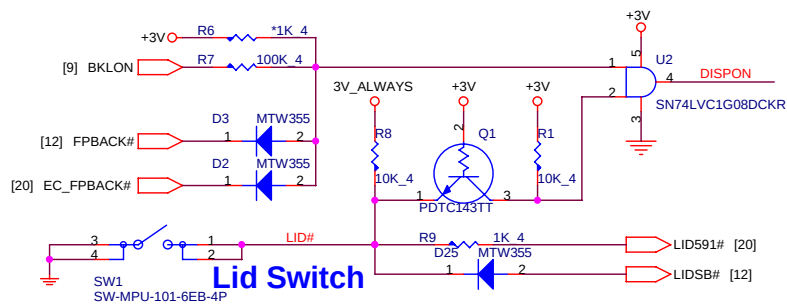
LAYOUT: Place HT bypass caps on topside near connected Lokar HT link.

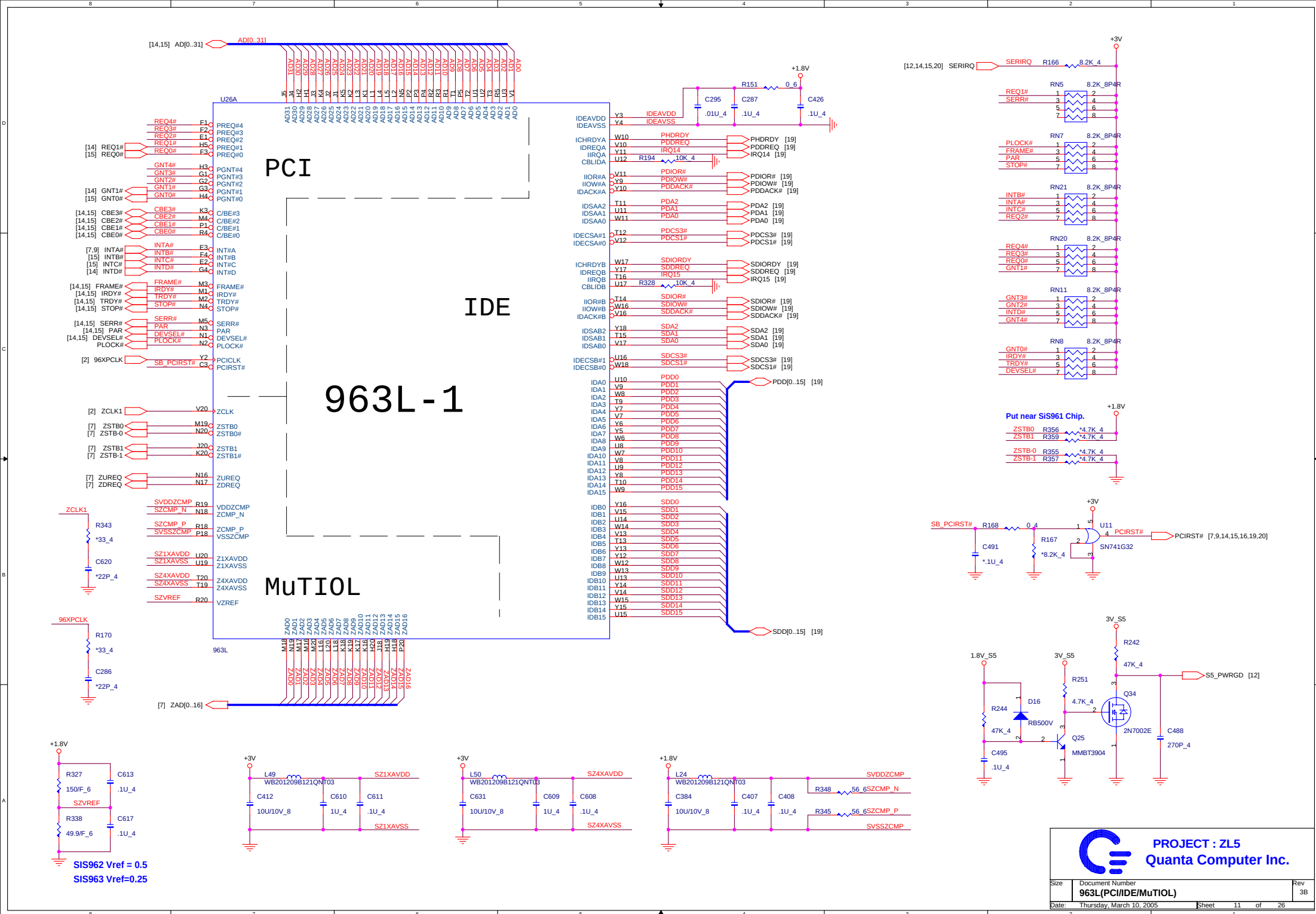


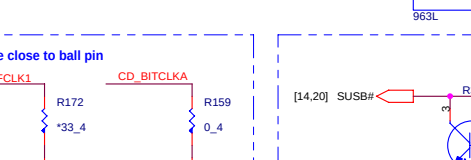
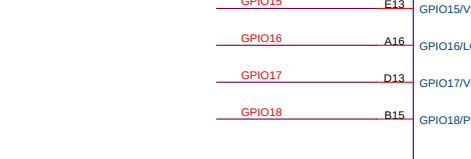
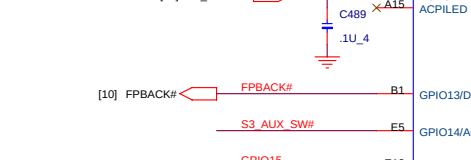
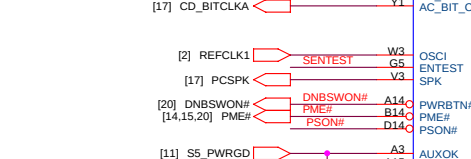
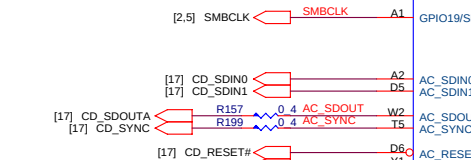
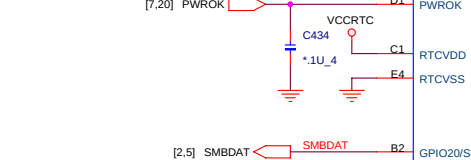
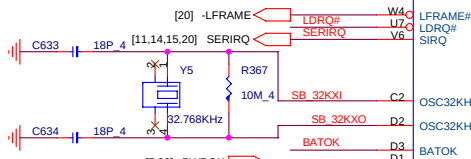
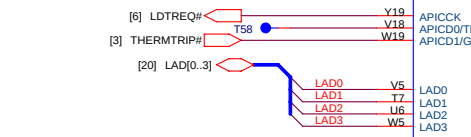
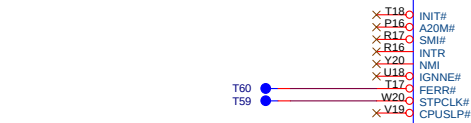
Place these capacitors under 760 solder side.



PROJECT : ZL5
Quanta Computer Inc.







CPU_S

APIC

LPC

RTC

GPIO

AC97

GPIO

ACPI

others

GPIO

KBC

SPEEDSTEP

MII

GPIO

GPIO

GPIO

GPIO

GPIO

GPIO

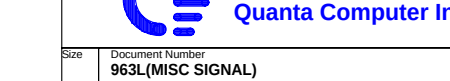
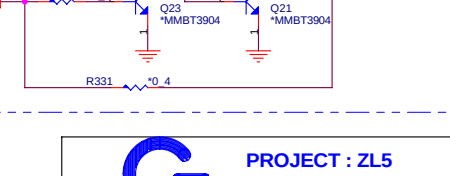
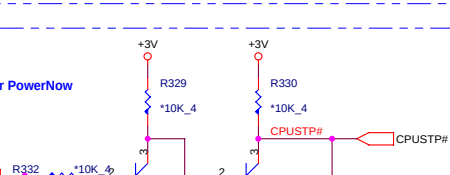
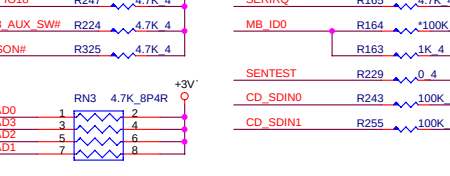
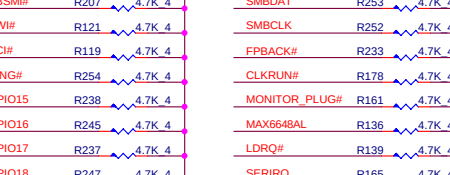
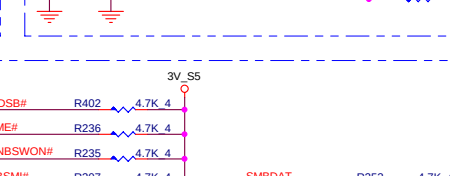
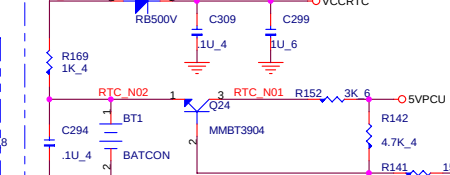
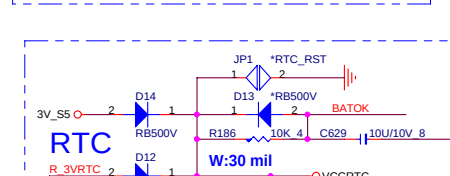
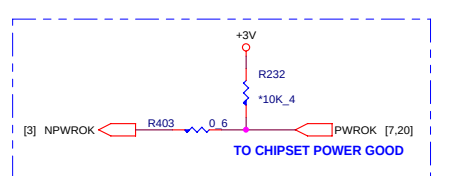
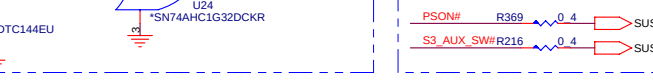
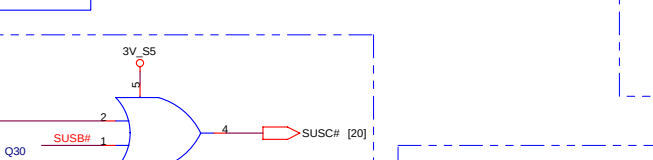
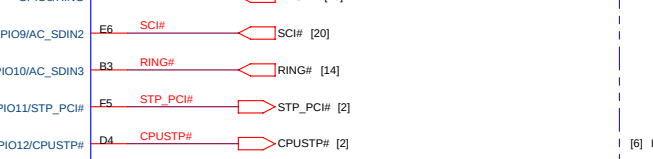
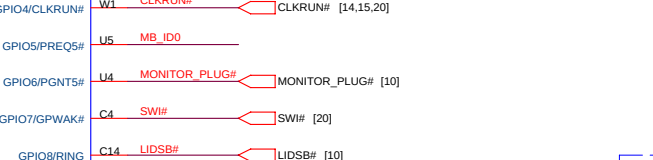
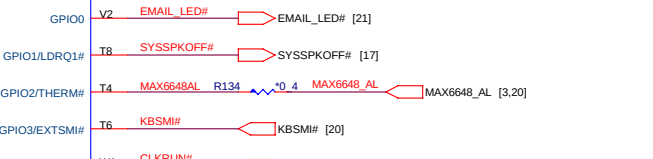
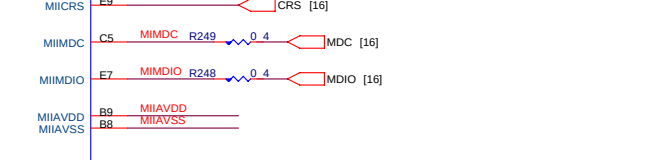
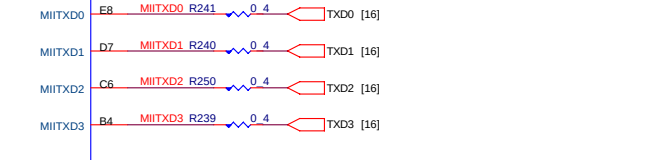
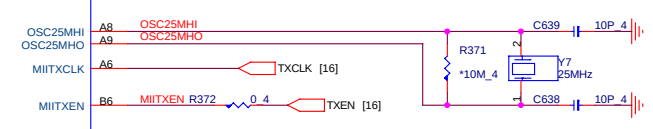
GPIO

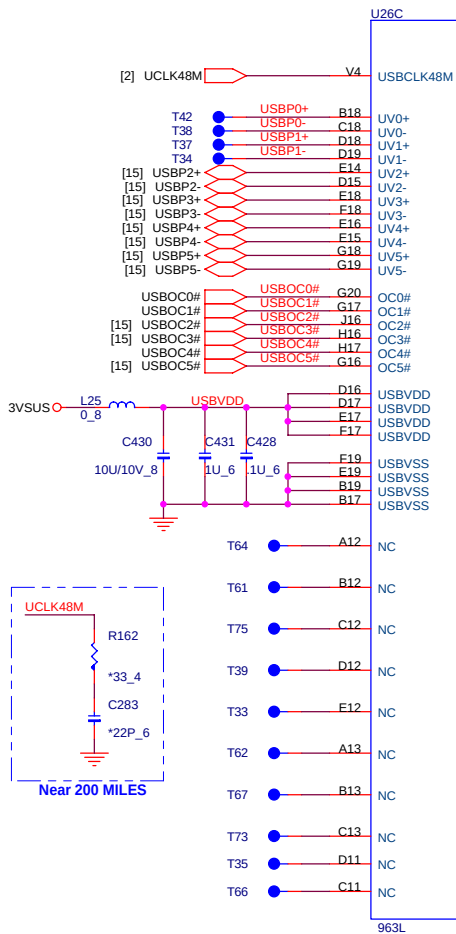
GPIO

GPIO

GPIO

GPIO

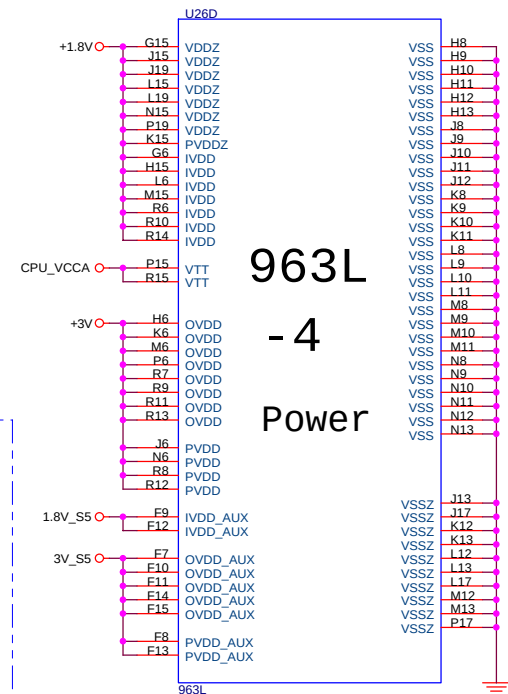
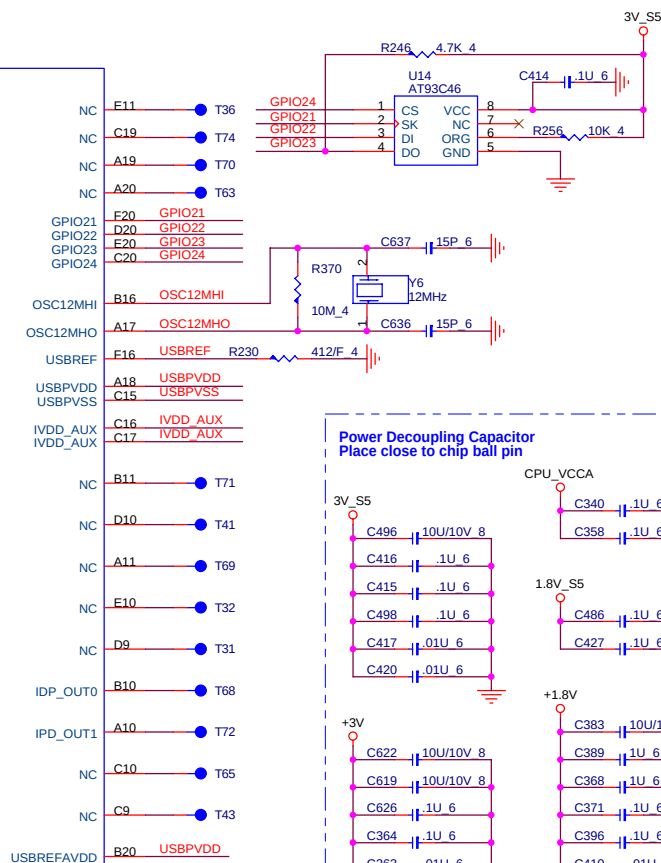
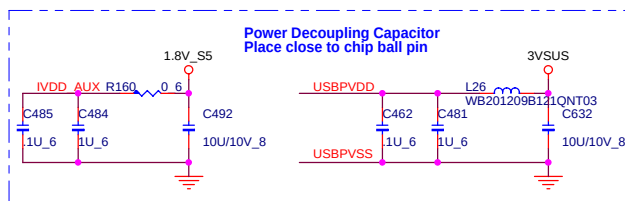
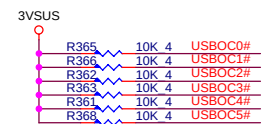




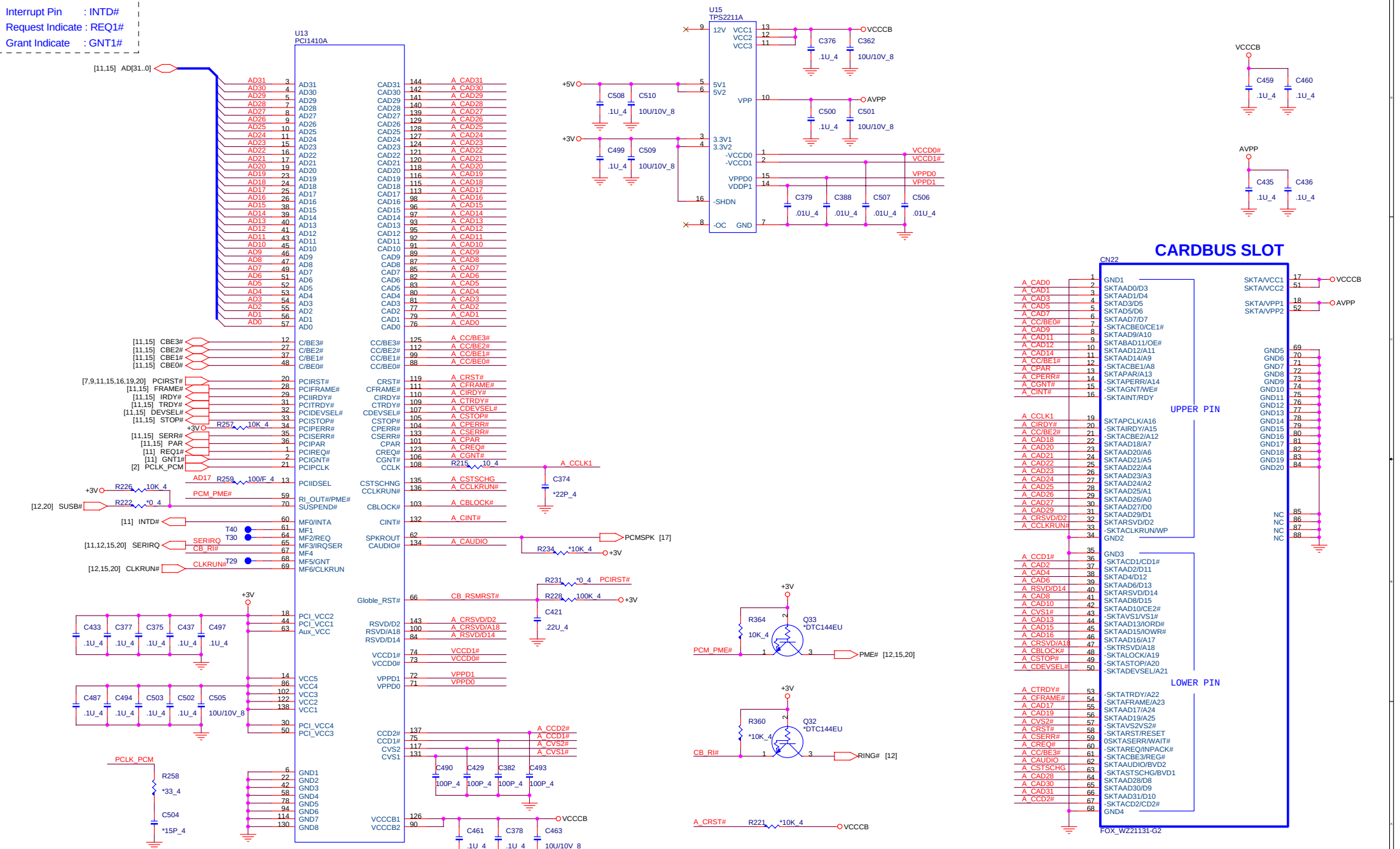
OTHERS

USB

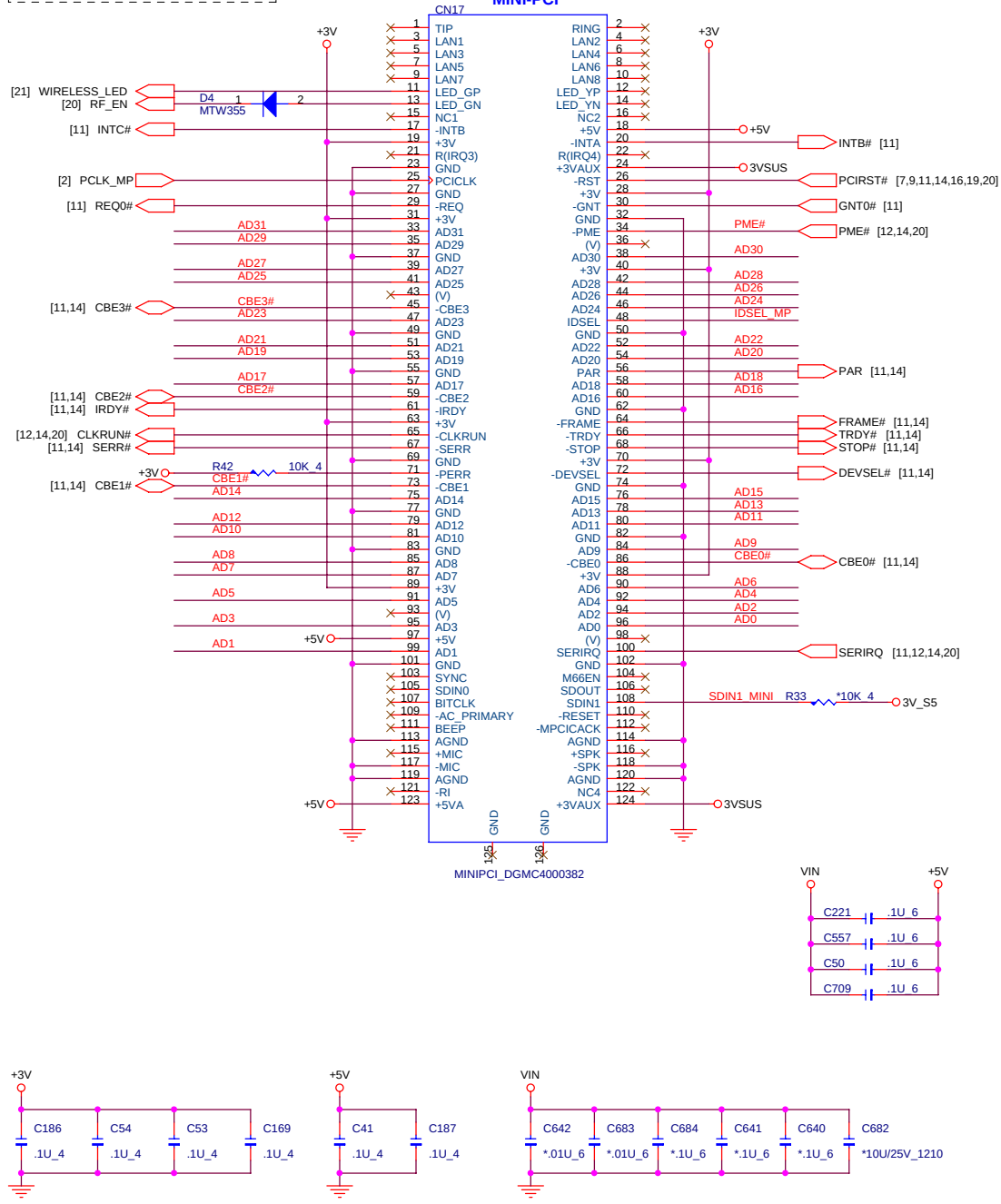
963L - 3

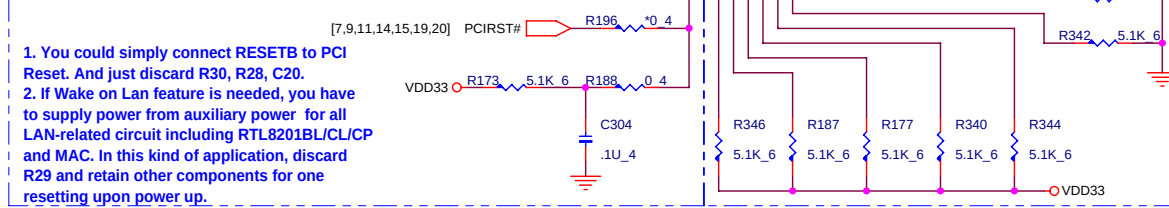
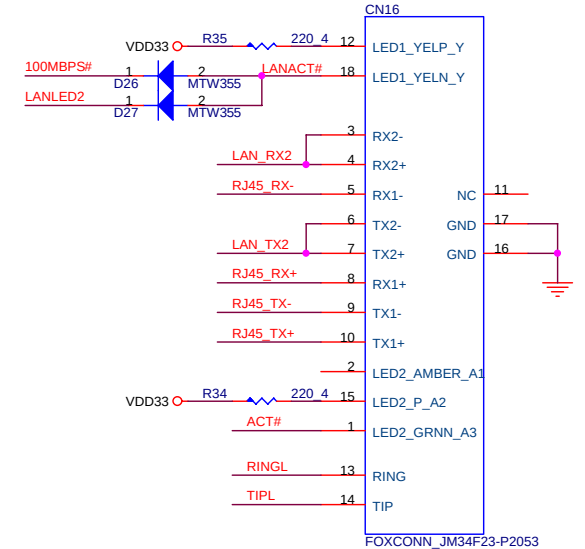
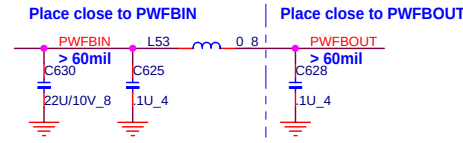
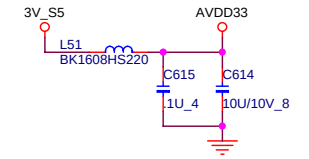
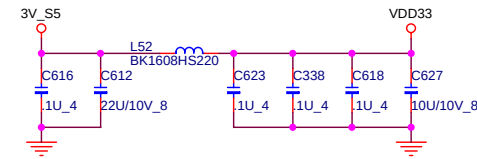
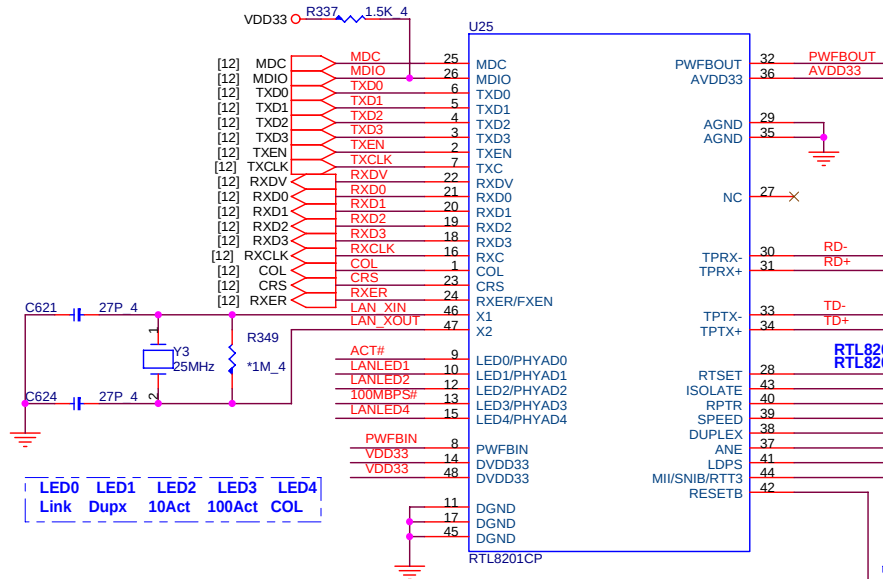


ID Select : AD17
Interrupt Pin : INTD#
Request Indicate : REQ1#
Grant Indicate : GNT1#



ID Select : AD22
Interrupt Pin : INTB# , INTC#
Request Indicate : REQ0#
Grant Indicate : GNT0#





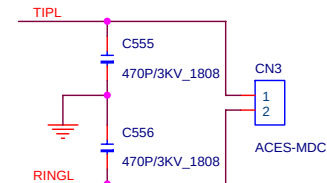
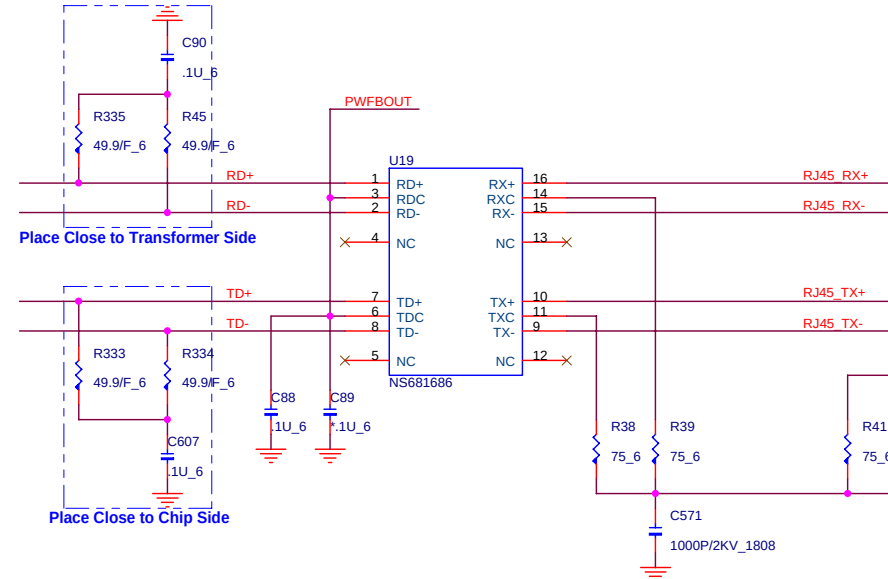
1. You could simply connect RESETB to PCI Reset. And just discard R30, R28, C20.
2. If Wake on Lan feature is needed, you have to supply power from auxiliary power for all LAN-related circuit including RTL8201BL/CL/CP and MAC. In this kind of application, discard R29 and retain other components for one resetting upon power up.

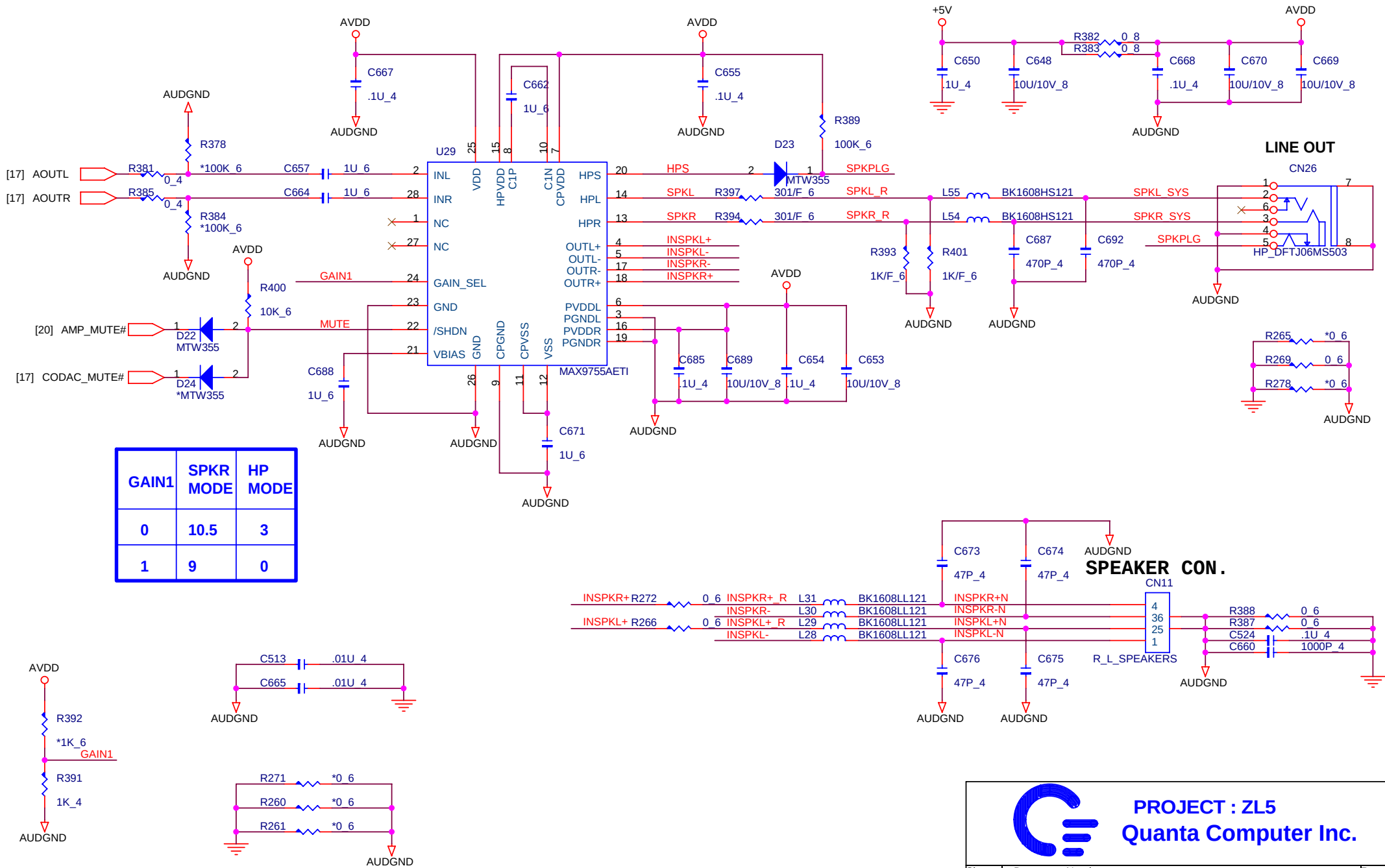
Reserved for 8201CL/CP LED Mode Change to compatible with BL
COL R354 5.1K 4 VDD33

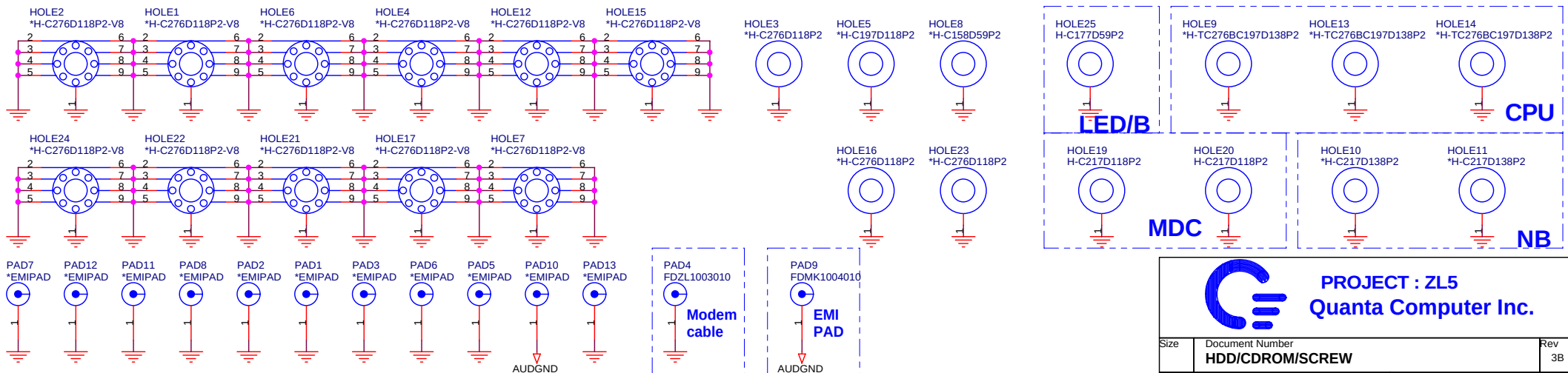
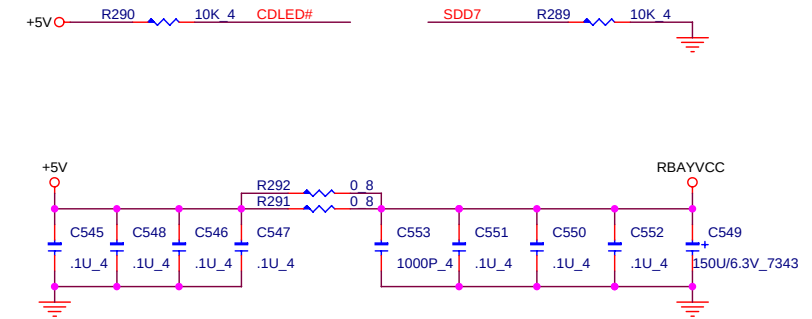
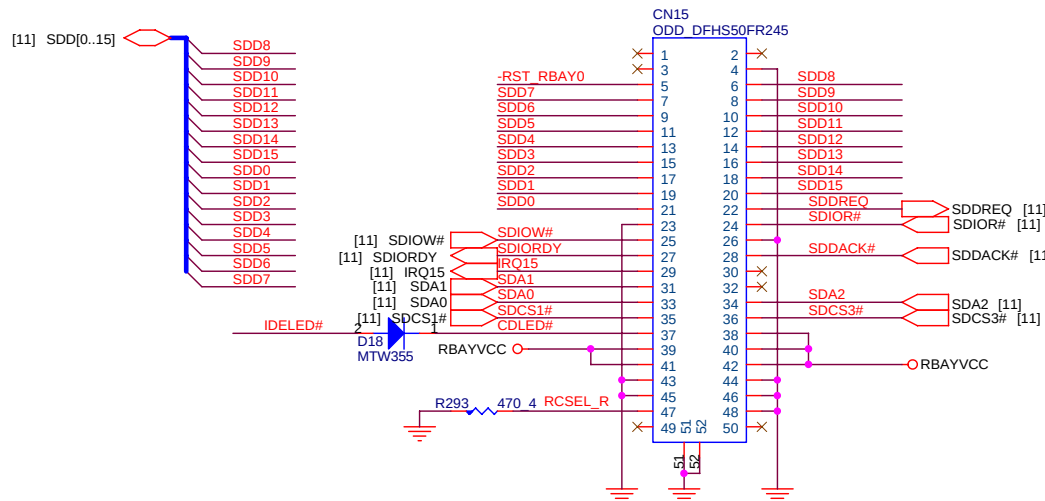
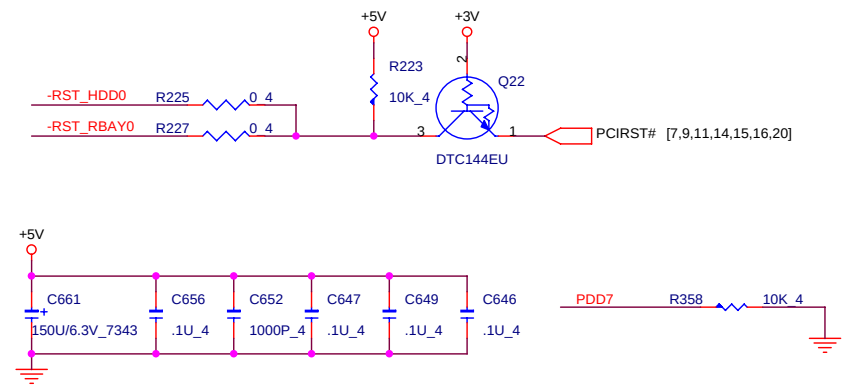
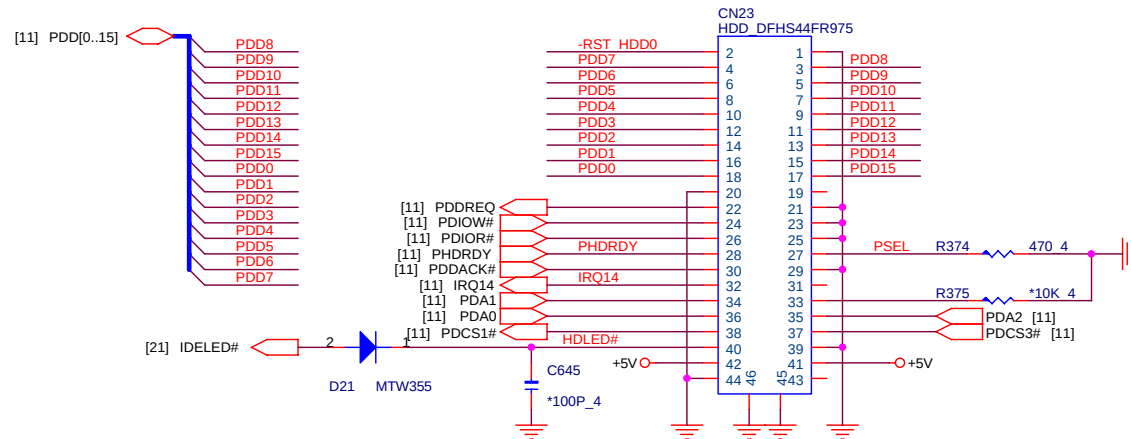
Reserved for ensuring 8201BL/CL/CP latch to UTP Mode.
RXER R339 5.1K 4

Reserved for ensuring 8201CL/CP latch to normal operation mode.
CRS R341 5.1K 4

ACT# R351 5.1K 4 VDD33
100MBPS# R350 5.1K 4
LANLED2 R353 5.1K 4
LANLED1 R352 5.1K 4
LANLED4 R347 5.1K 4

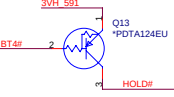
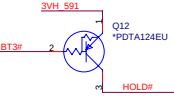
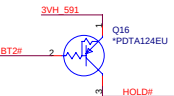
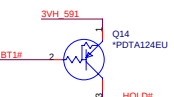
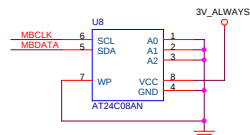




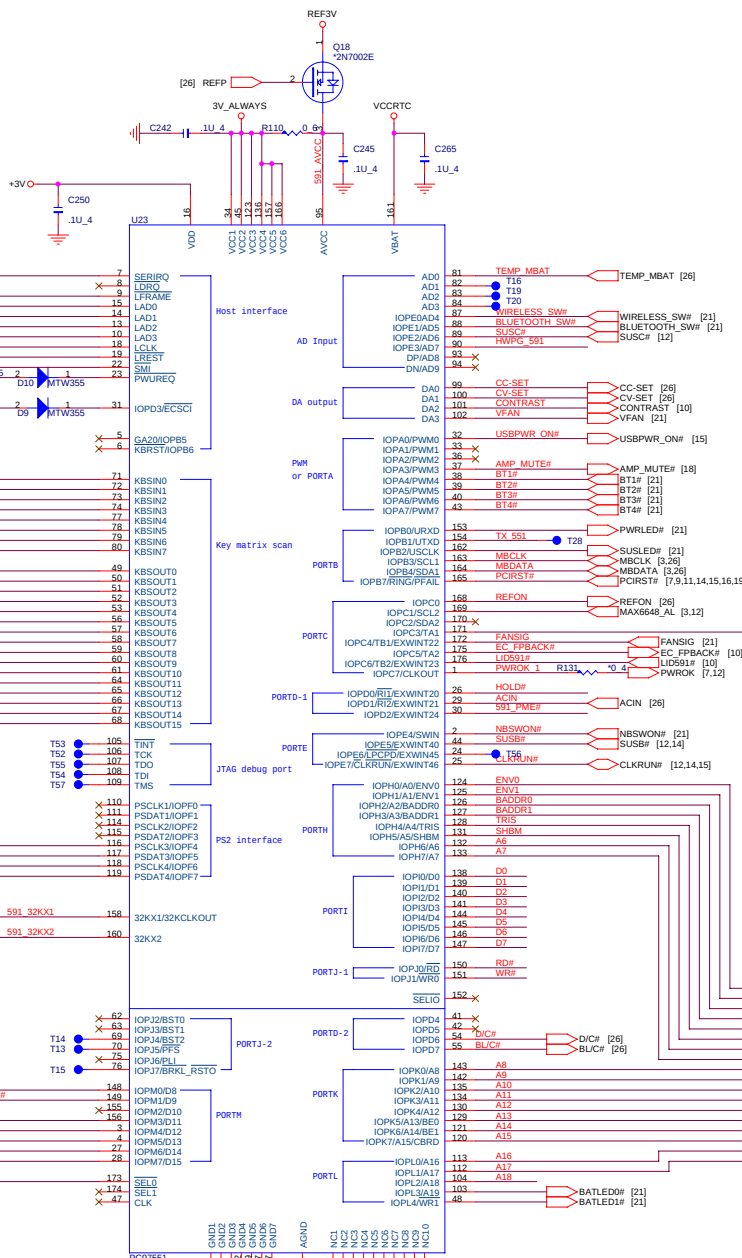
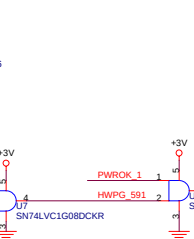
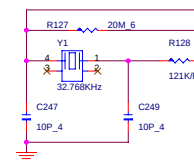


LDRQ#(pin 8) internal is no use

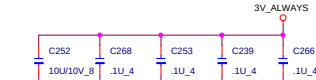
PCLK_591 R117 *22_4 C248 10P_4



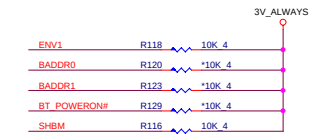
[21] TBCLK
[21] TBDATA
[21] CAPSLD#
[21] NUMLED#



FOR 97551 ONLY

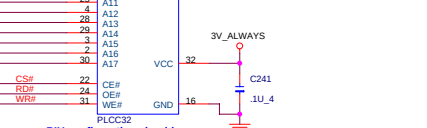
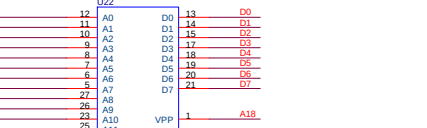
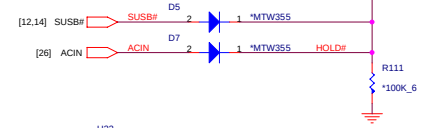
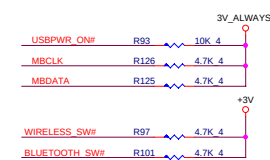


Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.



SHBM=1: Enable shared memory with host BIOS

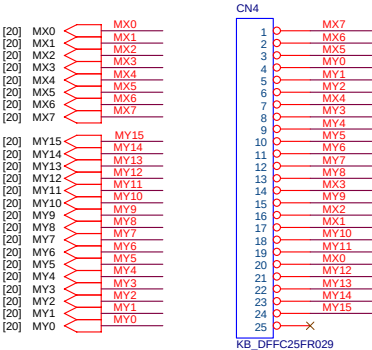
I/O Address		
BADDR0-1	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	



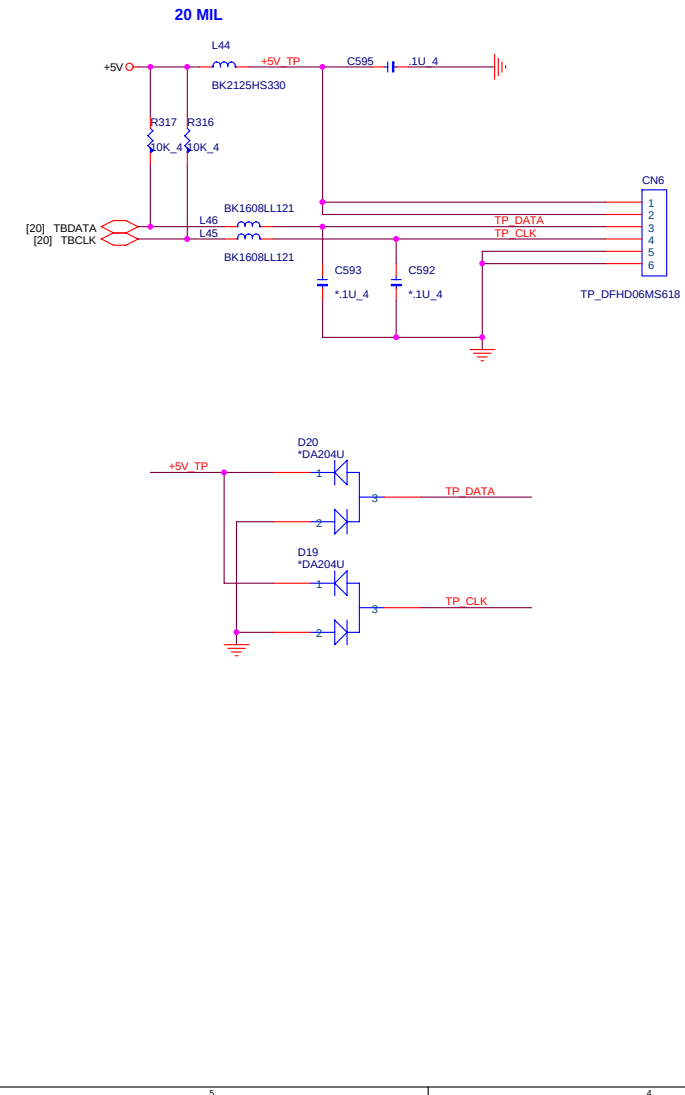
BIU configuration should match flash speed used

PROJECT : ZL5
Quanta Computer Inc.

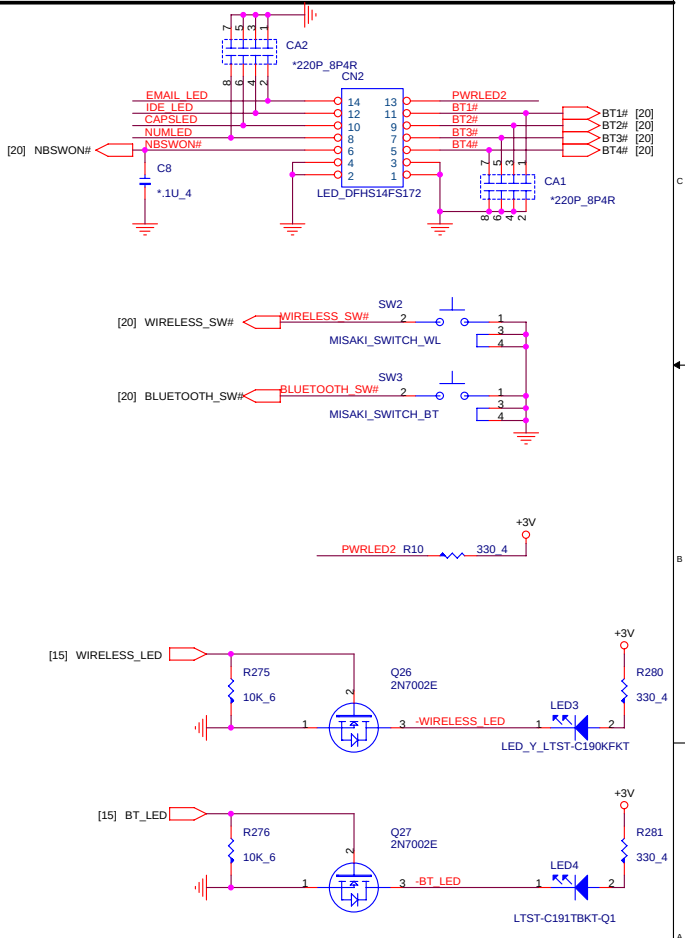
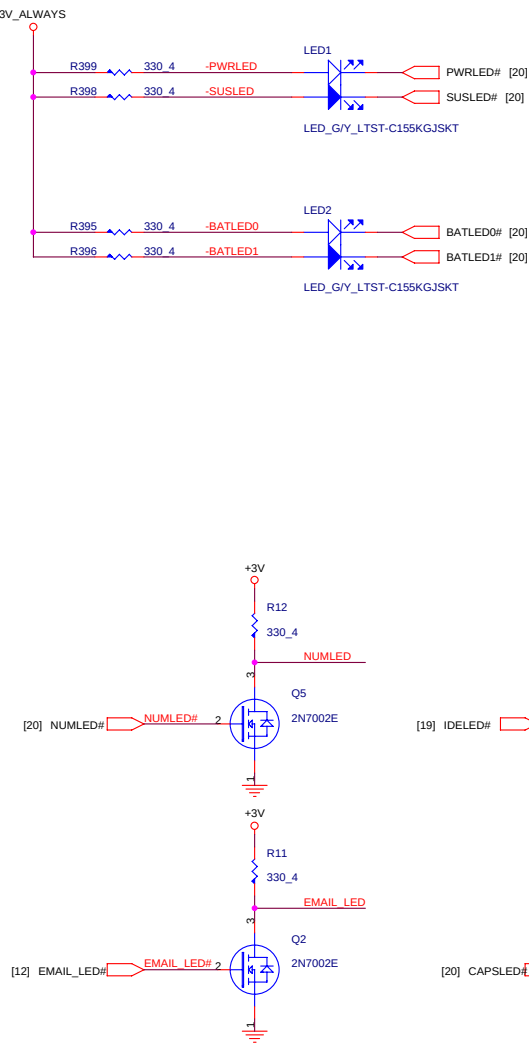
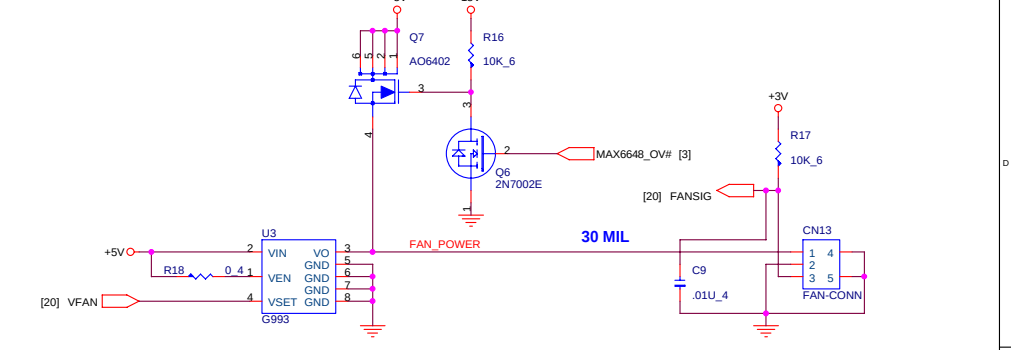
INT K/B

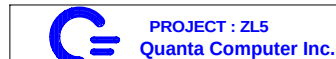


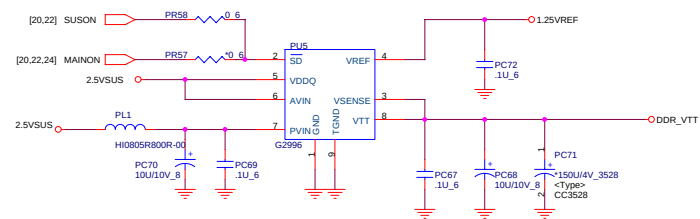
TOUCH PAD

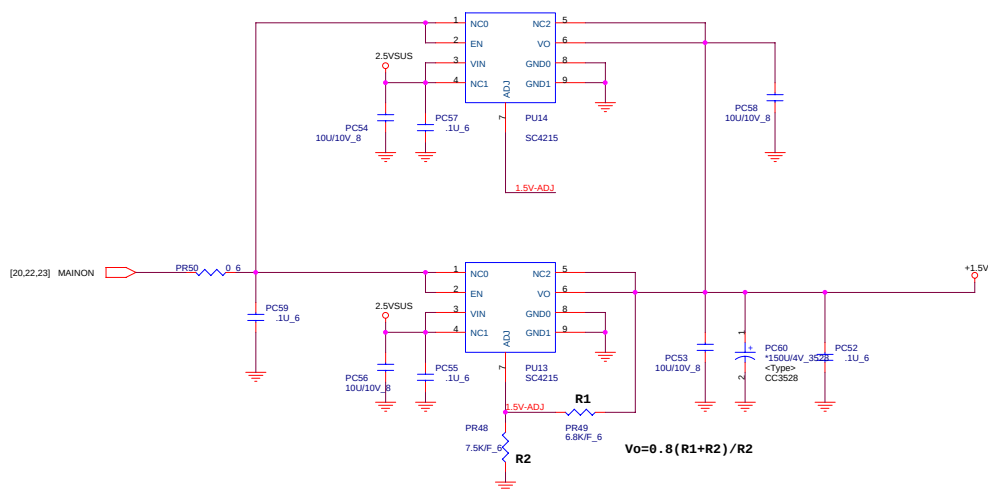
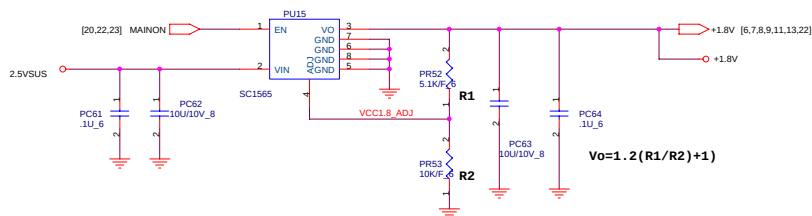
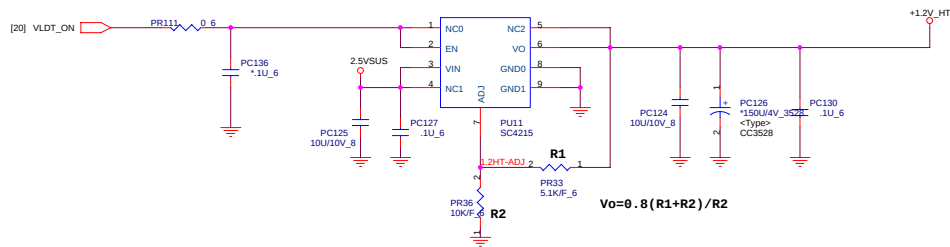


FAN CONTROL





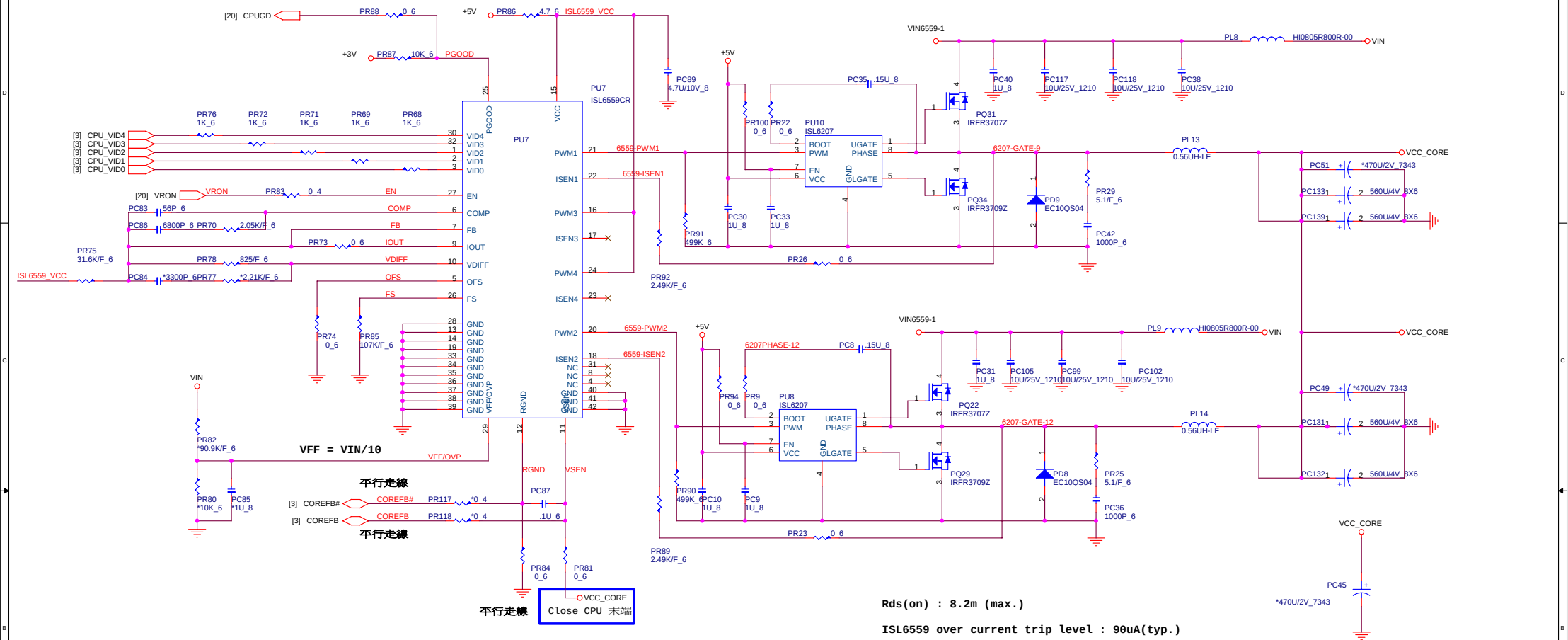




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Size	Document Number	Rev
	+1.5V/+1.8V/+1.2V	3B
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Vcore



Rds(on) : 8.2m (max.)

ISL6559 over current trip level : 90uA(typ.)

Full load Isen current : 90uA/1.5 ~ 60uA

AMD LPM 35W current 28A

$$R_{ds(on)} * I_o(\text{phase}) = R_{sen} * I_{sen}$$
$$8.2\text{m} \cdot 1.3 \cdot (28\text{A}/2) = R_{\text{sen}} \cdot 60\mu\text{A}$$

Rsen = 2.48K ~ 2.49K

OCP : $28A \cdot 1.5 = 42A$

