

Voltage Rails

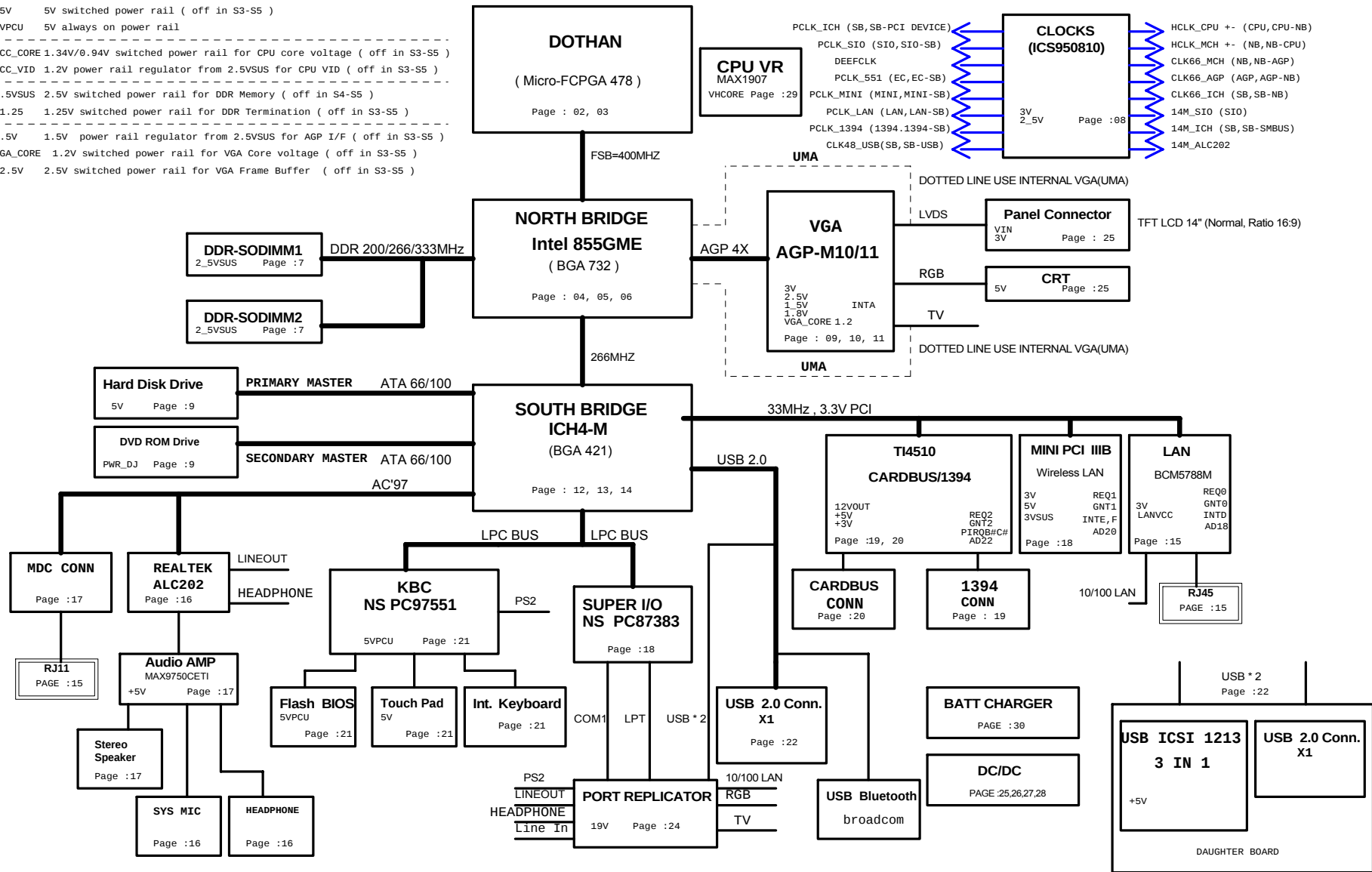
PWR_SRC Primary DC system power supply
 3VSUS 3.3V switched power rail (off in S4-S5)
 +3V 3.3V switched power rail (off in S3-S5)
 3VPCU 3V always on power rail
 5VSUS 5V switched power rail (off in S4-S5)
 +5V 5V switched power rail (off in S3-S5)
 5VPCU 5V always on power rail

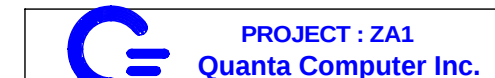
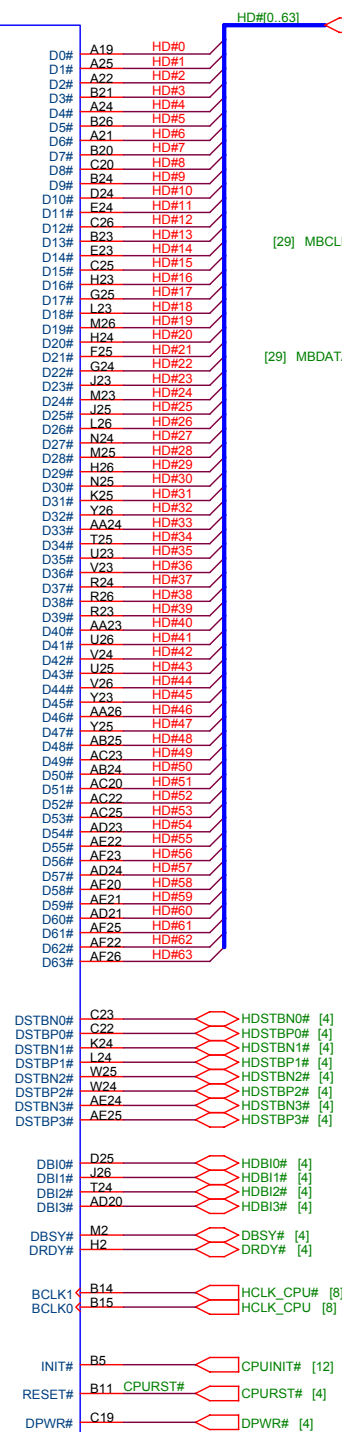
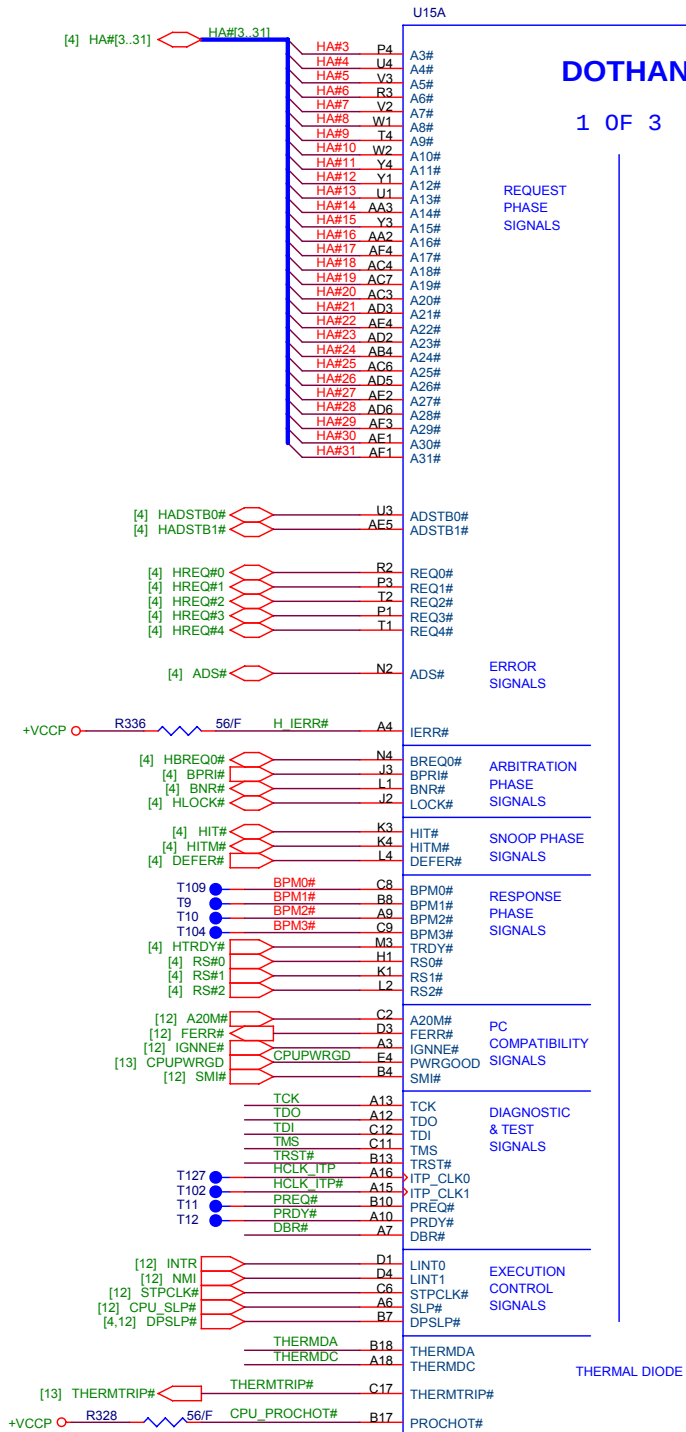
VCC_CORE 1.34V/0.94V switched power rail for CPU core voltage (off in S3-S5)
 VCC_VID 1.2V power rail regulator from 2.5VSUS for CPU VID (off in S3-S5)

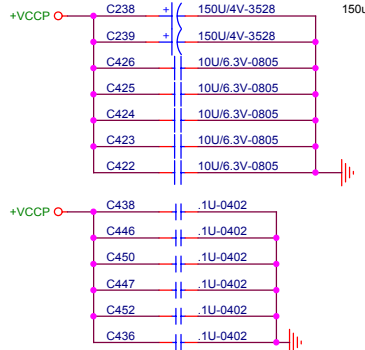
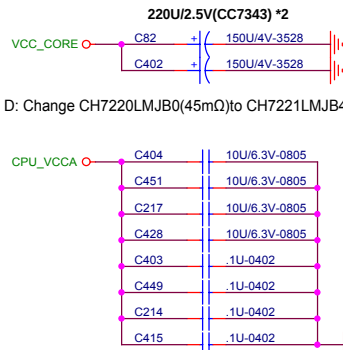
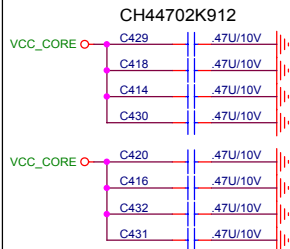
2.5VSUS 2.5V switched power rail for DDR Memory (off in S4-S5)
 +1.25 1.25V switched power rail for DDR Termination (off in S3-S5)

1.5V 1.5V power rail regulator from 2.5VSUS for AGP I/F (off in S3-S5)
 VGA_CORE 1.2V switched power rail for VGA Core voltage (off in S3-S5)
 +2.5V 2.5V switched power rail for VGA Frame Buffer (off in S3-S5)

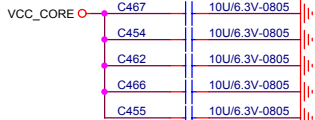
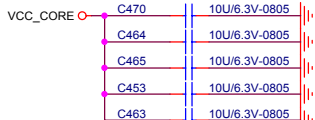
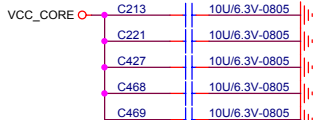
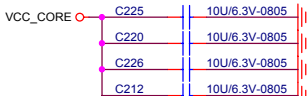
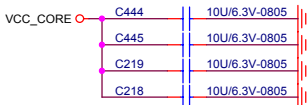
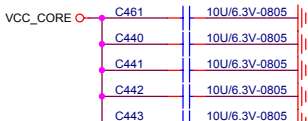
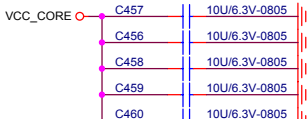
ZA1 SYSTEM BLOCK DIAGRAM



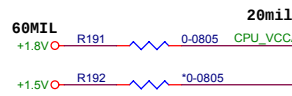
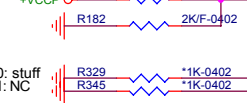
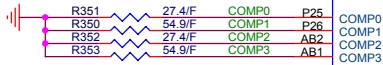




10U/6.3V/X5R(CC0805) *38



4/10 change P/N to CS02743F907

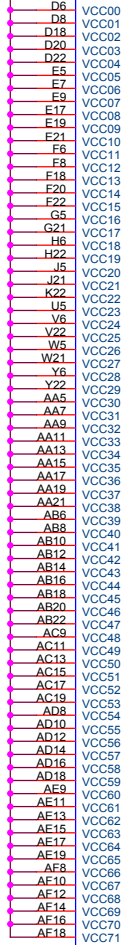


U15B

DOTHAN

2 OF 3

POWER, GROUND, RESERVED SIGNALS



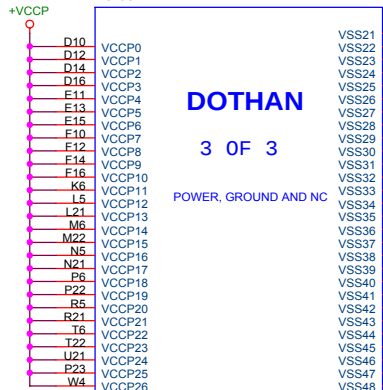
DOTHAN PROCESSOR

U15C

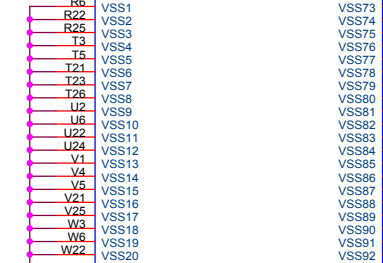
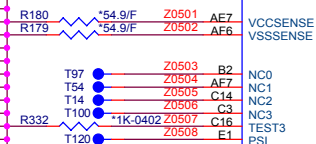
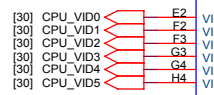
DOTHAN

3 OF 3

POWER, GROUND AND NC



VID



DOTHAN PROCESSOR

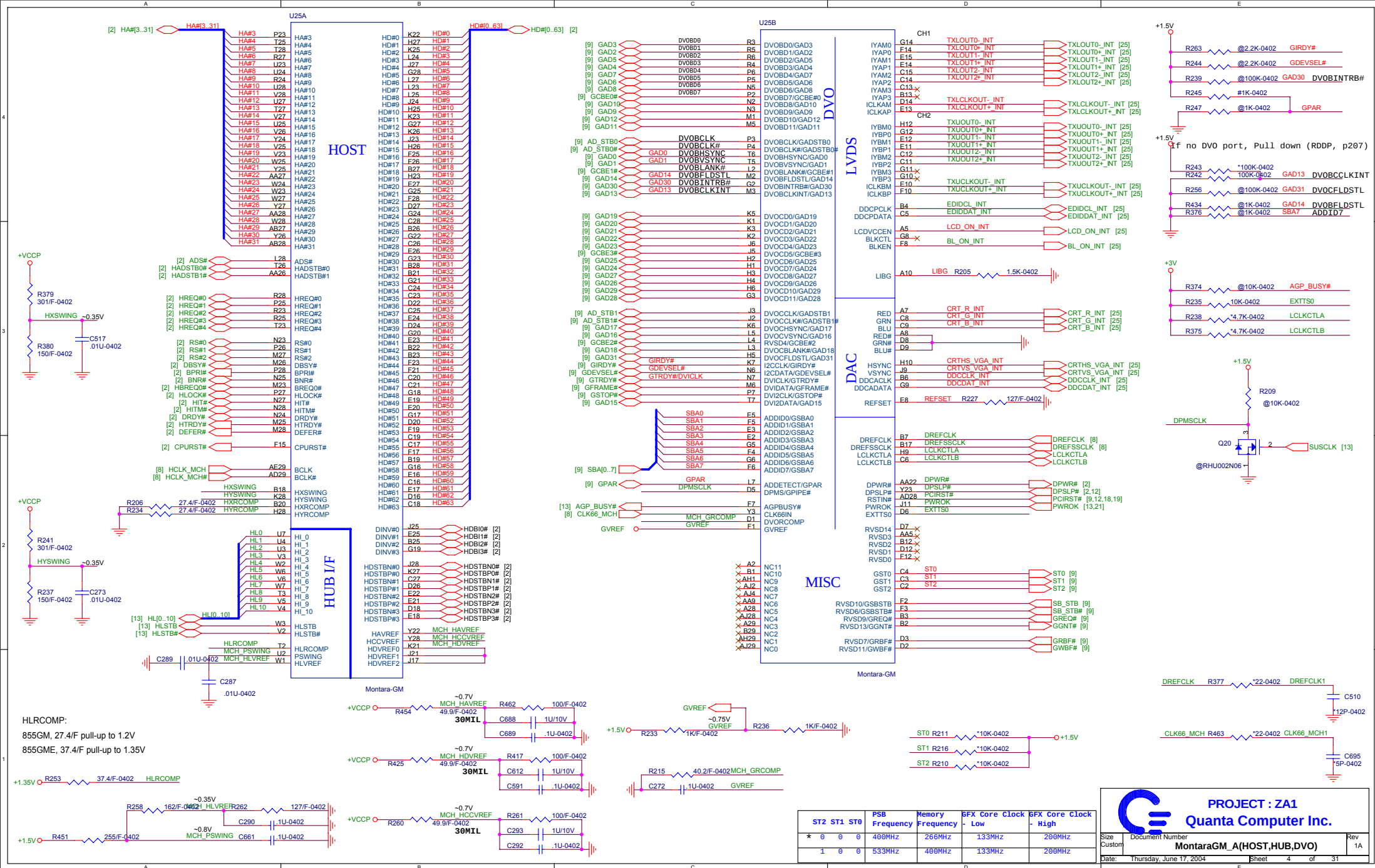
VCC_CORE: 1.356V-0.844V , 0.748V(Deeper sleep)

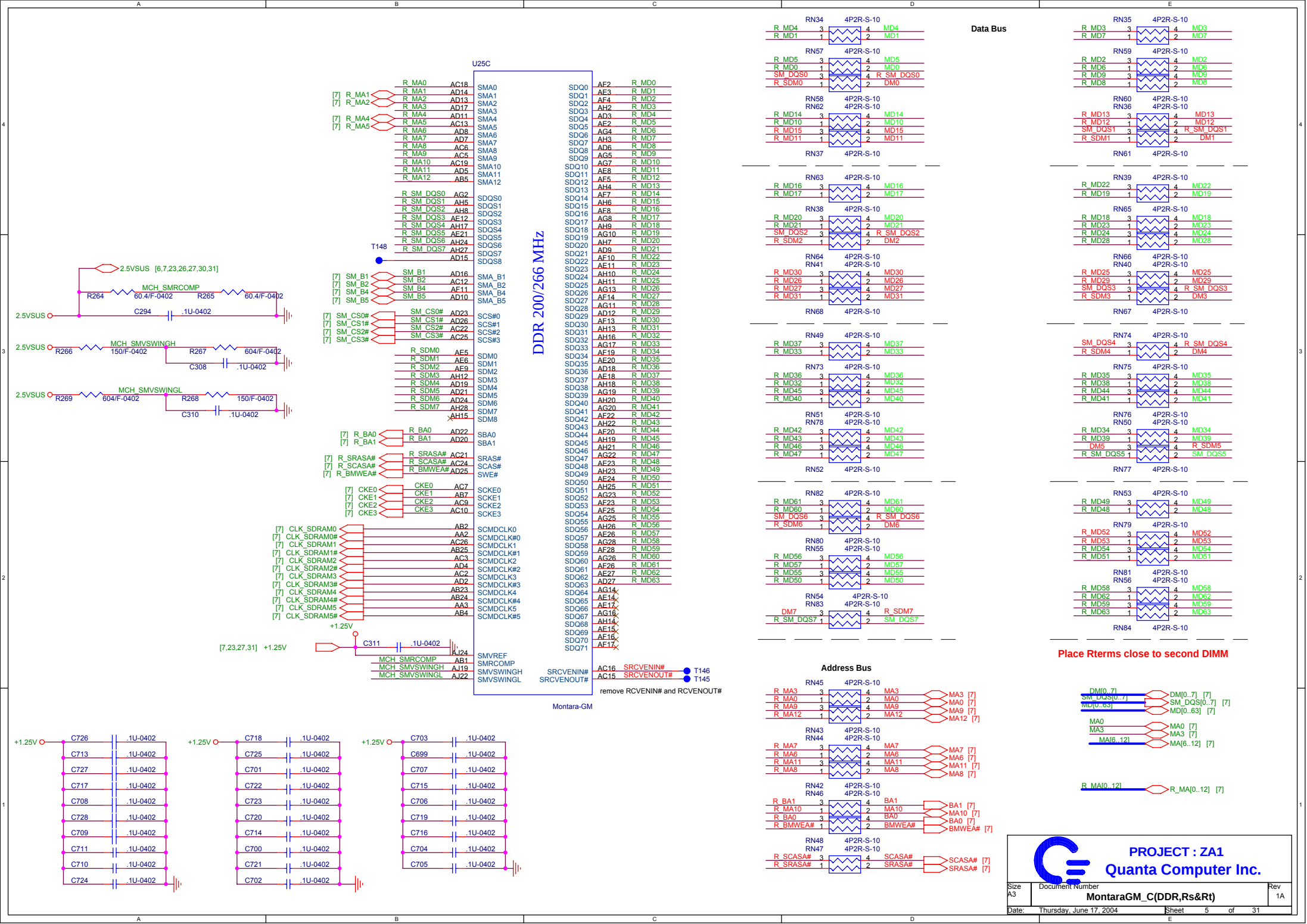
VCCP : 1.05V

VCCA : 1.8V

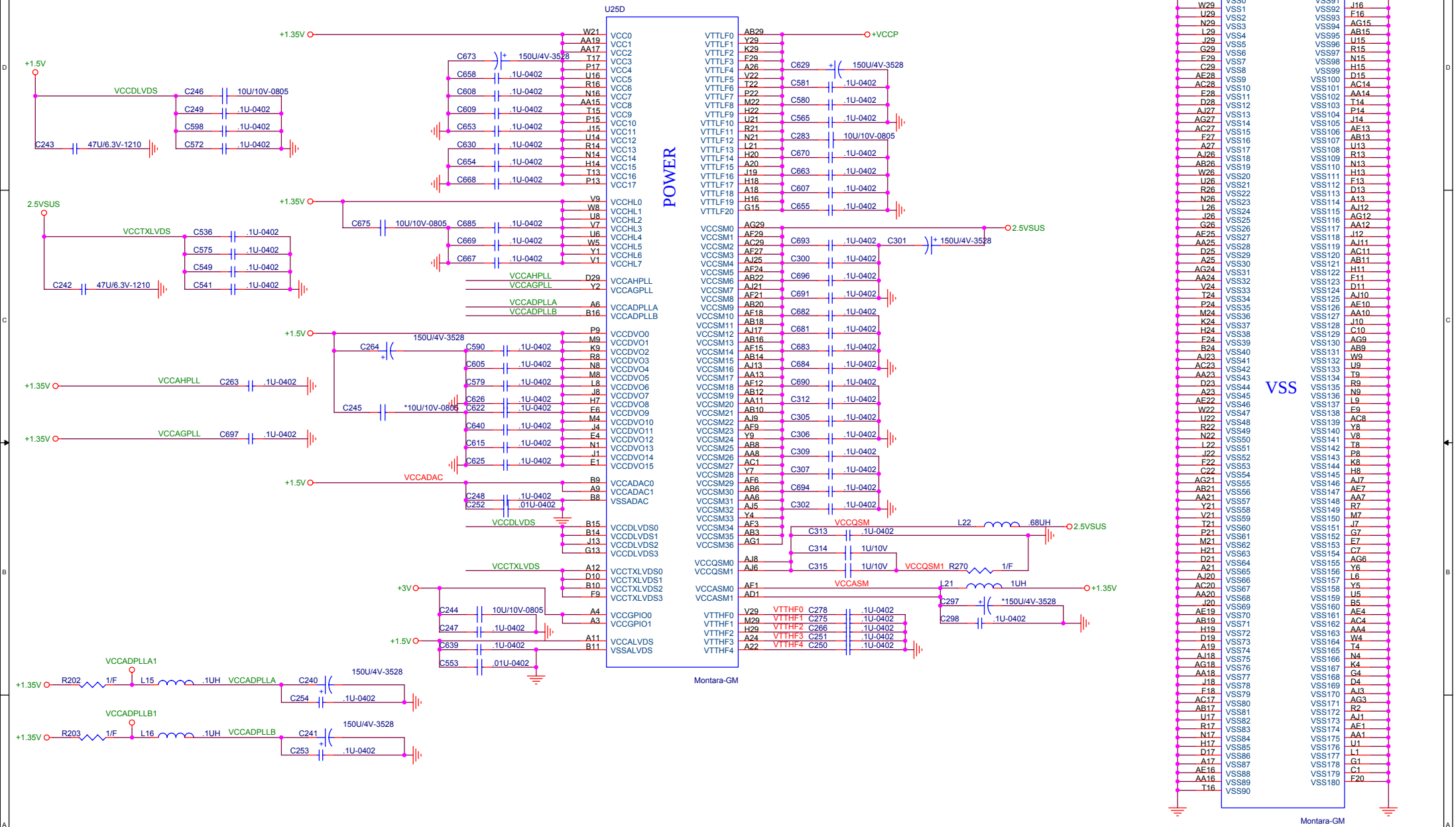
 **PROJECT : ZA1**
Quanta Computer Inc.

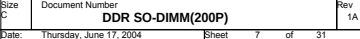
Size B	Doc Number	Rev 1A
CPU DOTHAN (POWER/NC)-B		
Date: Tuesday, July 06, 2004	Sheet 3 of 31	



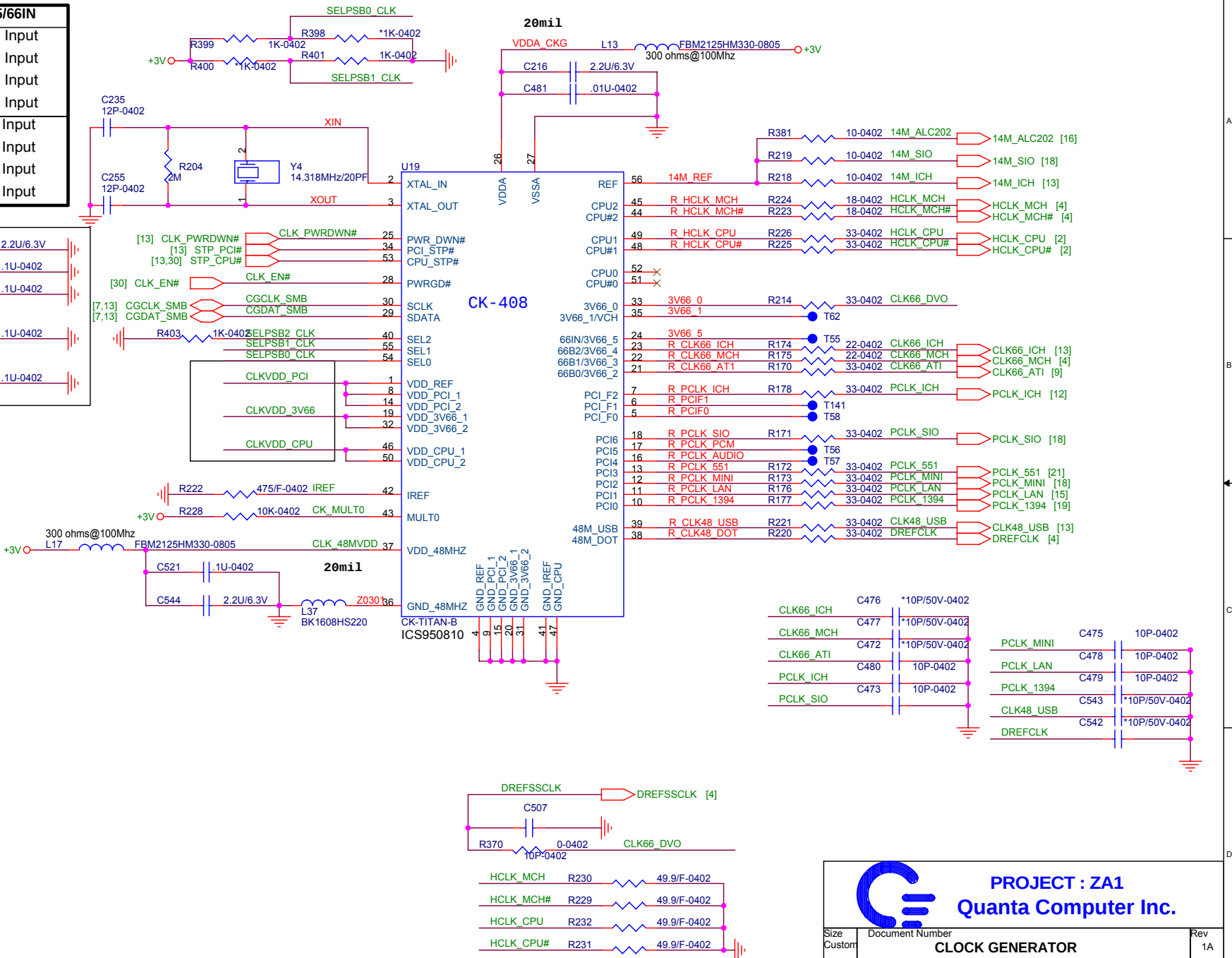
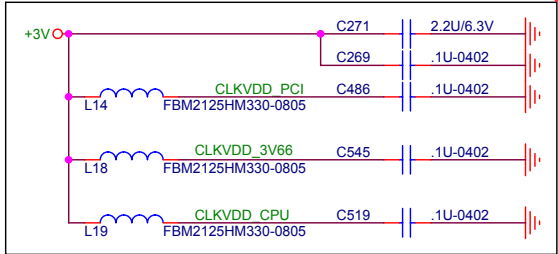


NB: +1.5V 60MIL
NB: +1.35V 60MIL





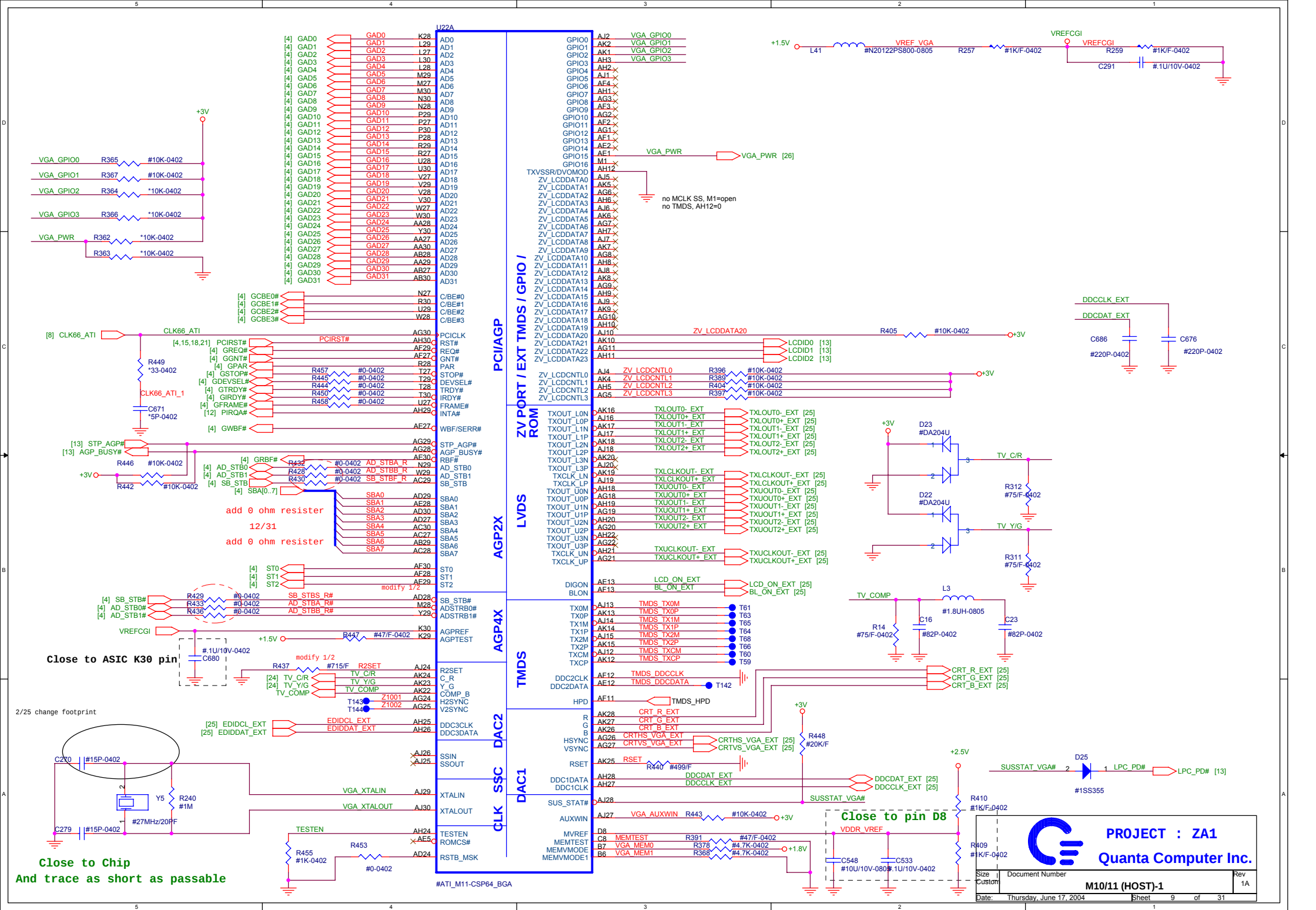
S2	S1	S0	CPU	3V66[0..4]	3V66_5/66IN
1	0	0	66	66IN	66 Input
1	0	1	100	66IN	66 Input
1	1	0	200	66IN	66 Input
1	1	1	133	66IN	66 Input
0	0	0	66	66	66 Input
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0	1	0	200	66	66 Input
0	1	1	133	66	66 Input

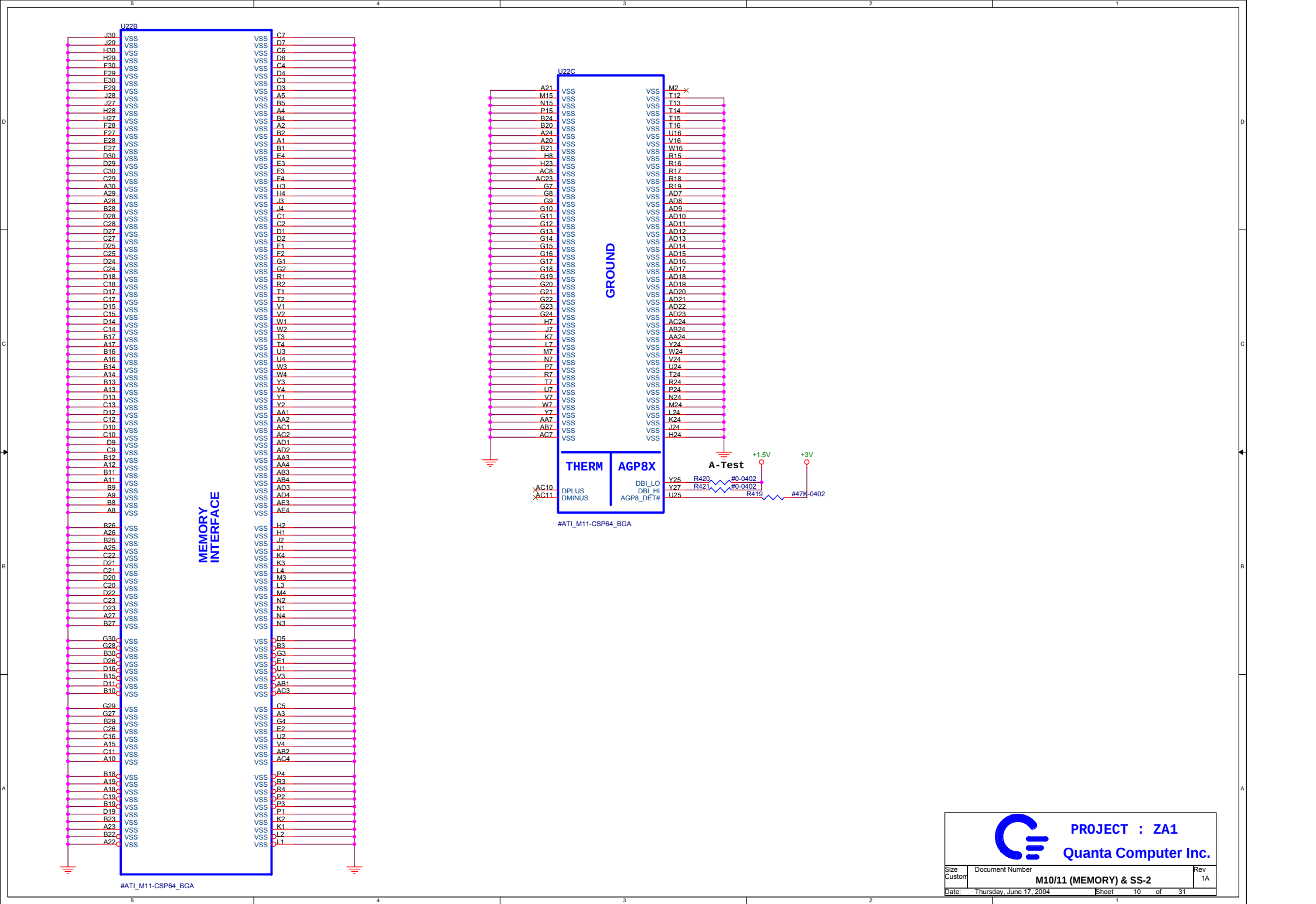


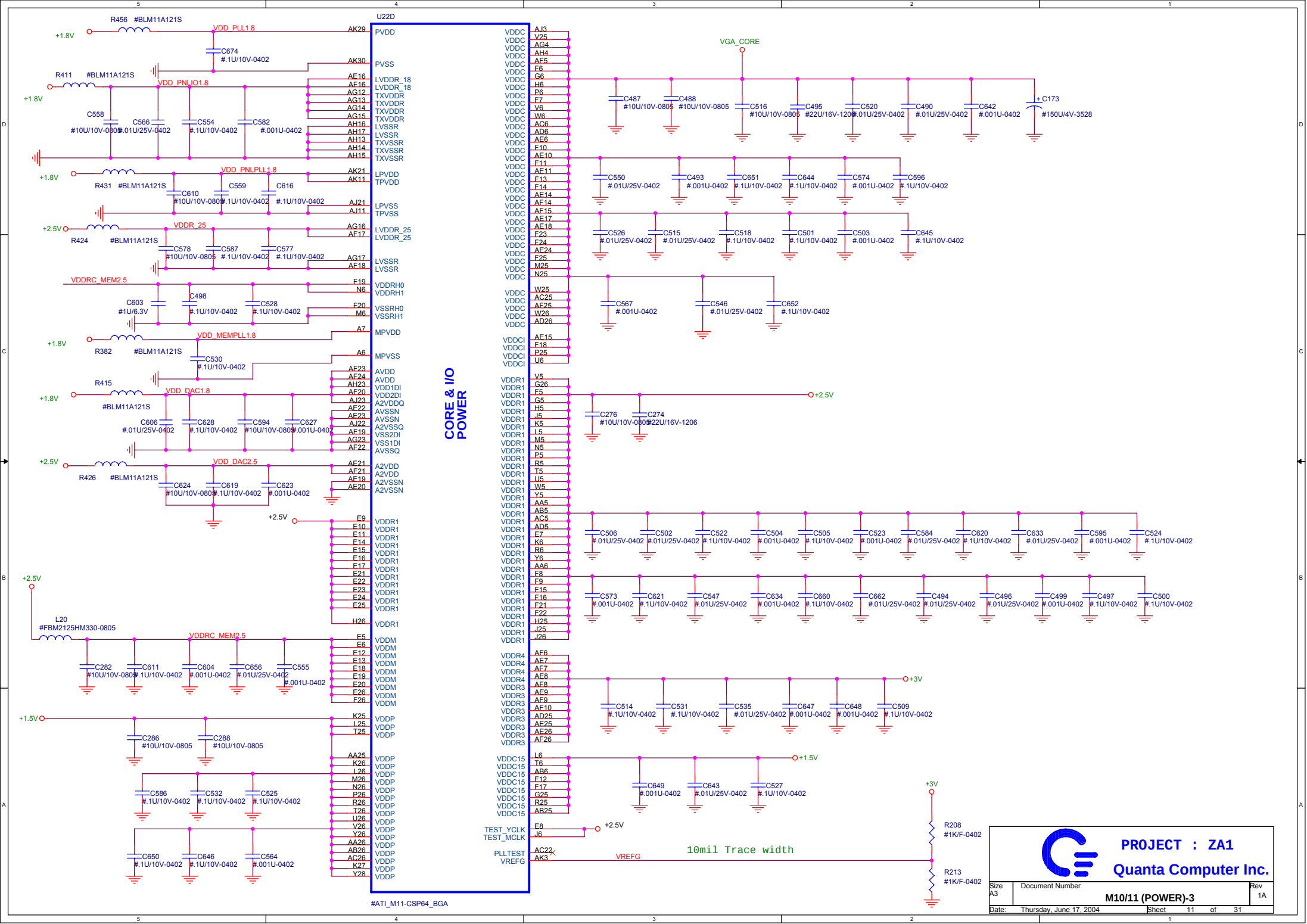


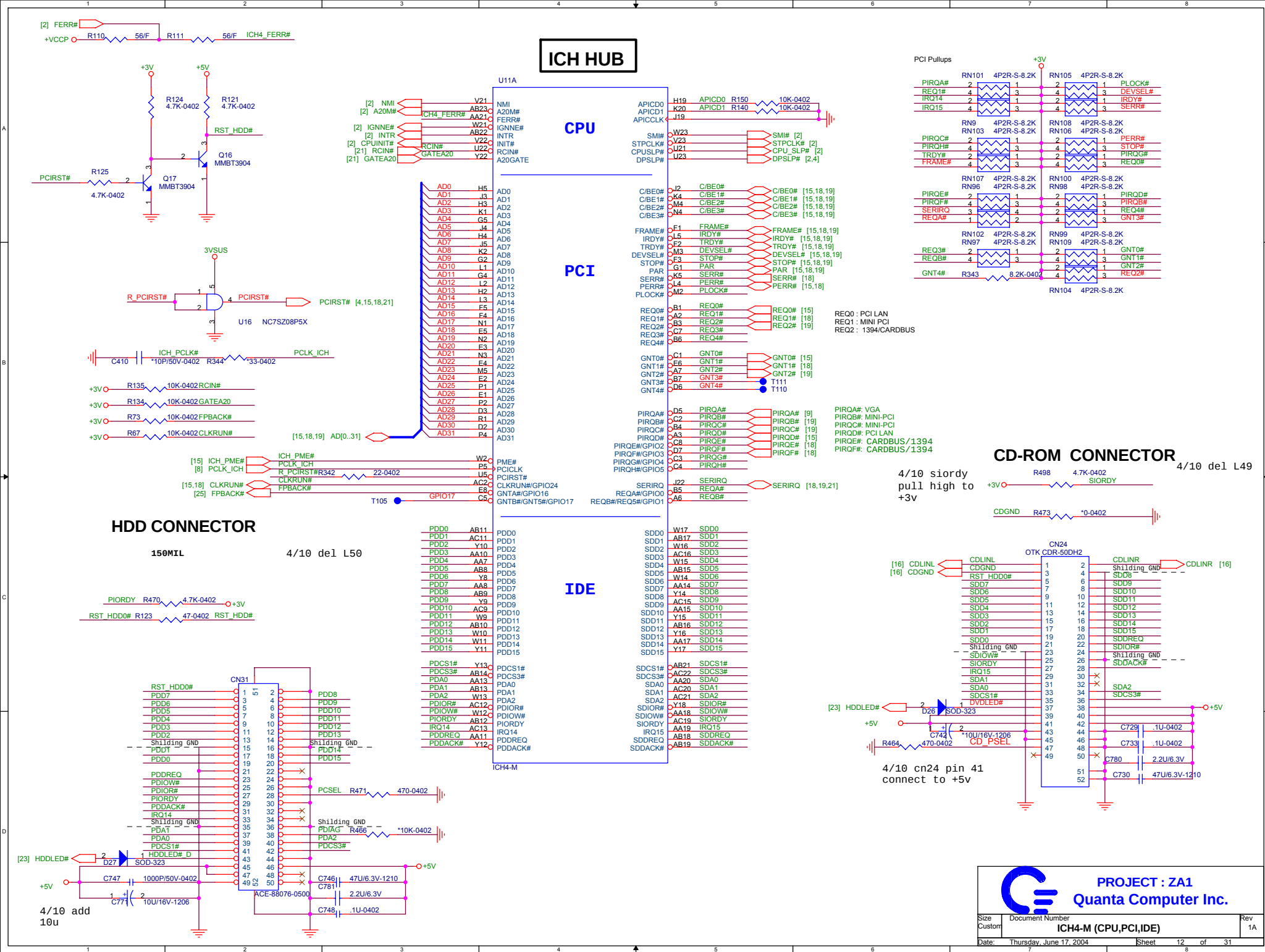
PROJECT : ZA1
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
CLOCK GENERATOR		
Date: Thursday, June 17, 2004	Sheet 8	of 31

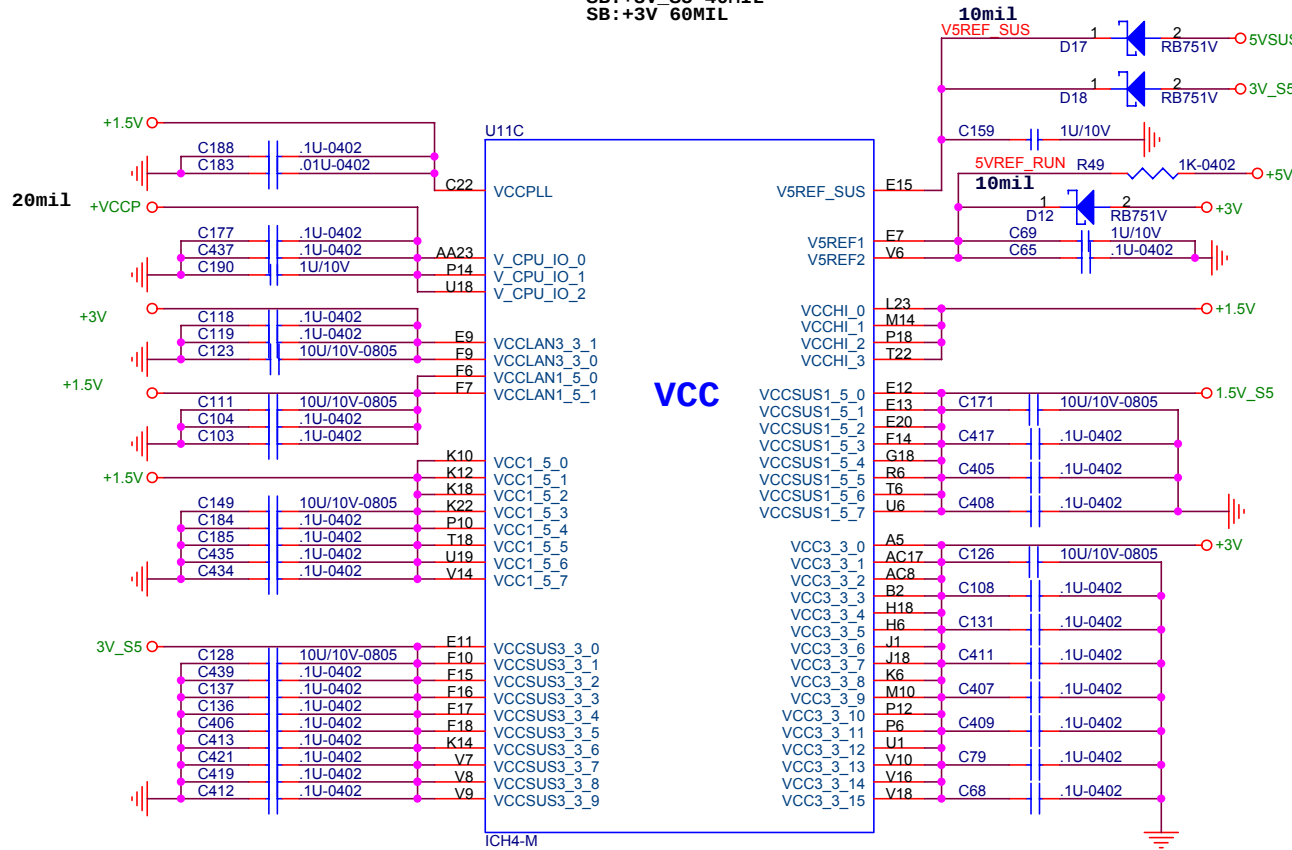




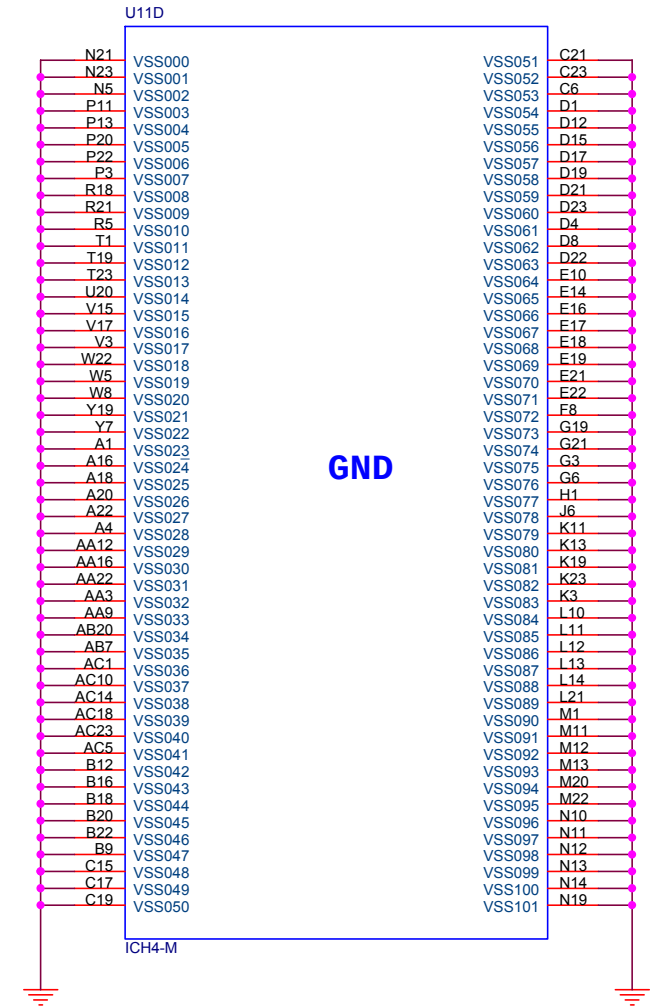




SB:+1.5V 40MIL
SB:+1.5V_S5 40MIL
SB:+3V_S5 40MIL
SB:+3V 60MIL



- +5V [12,17,18,20,21,22,24,25,26,27,28,31]
- +3V [2,4,6,7,8,9,10,11,12,13,15,16,17,18,19,20,21,22,23,24,25,27,28,30]
- 3V_S5 [2,13,27,28]
- 1.5V_S5 [26,27]
- +1.5V [3,4,6,9,10,11,13,26,27]
- +VCCP [2,4,6,12,27,30]





PROJECT : ZA1

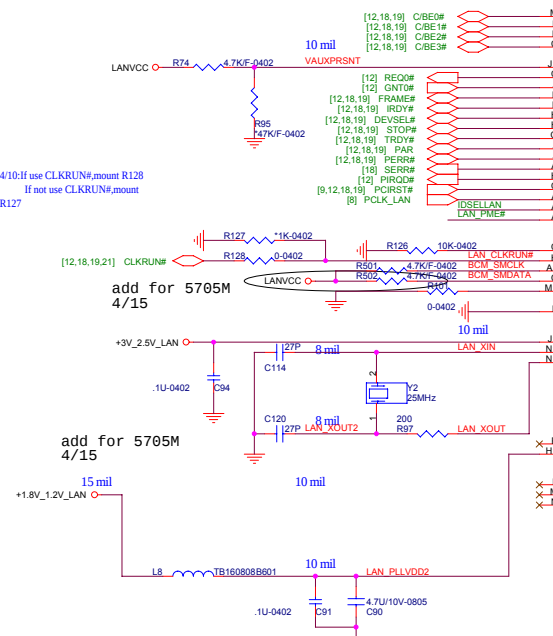
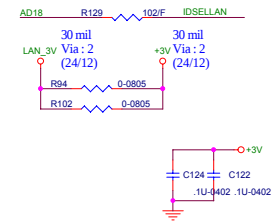
Quanta Computer Inc.

Size Custom	Document Number ICH4-M (POWER&GND)	Rev 1A
Date:	Thursday, June 17, 2004	Sheet 14 of 31

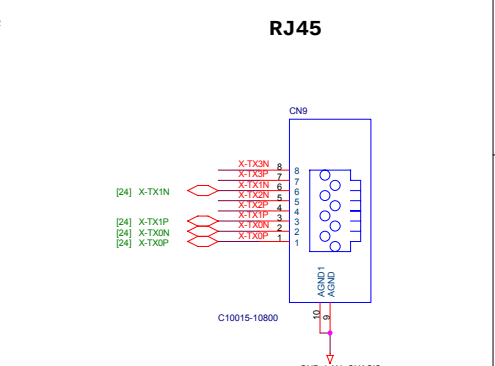
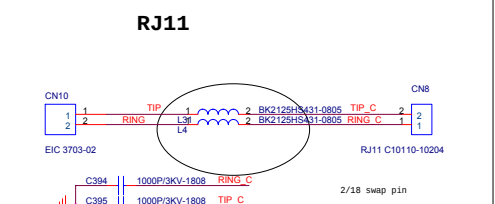
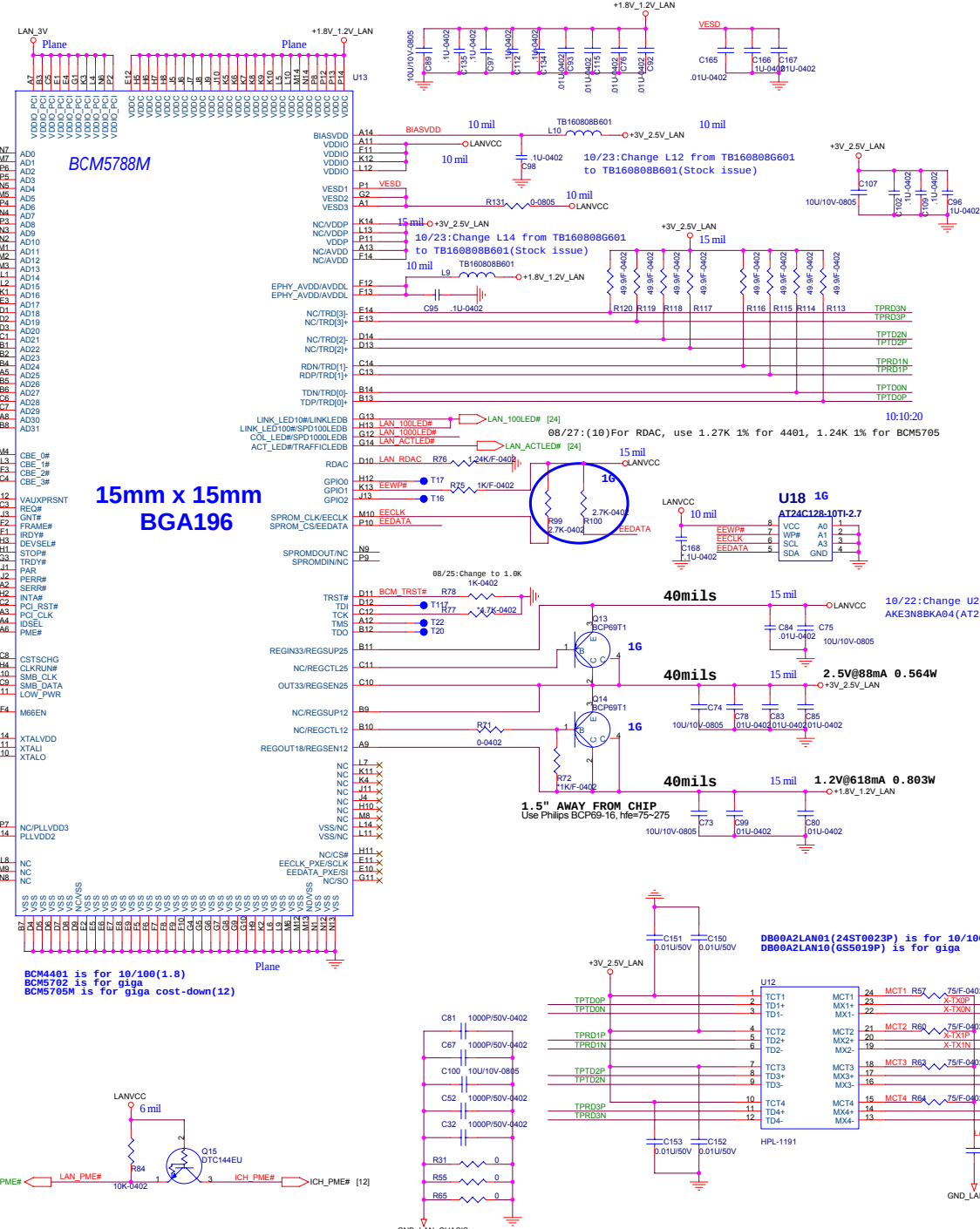
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| ID Select      : AD18 |
| Interrupt Pin  : PIRQB# |
| Request indicates : REQ0# |
| Grant indicates  : GNT0# |

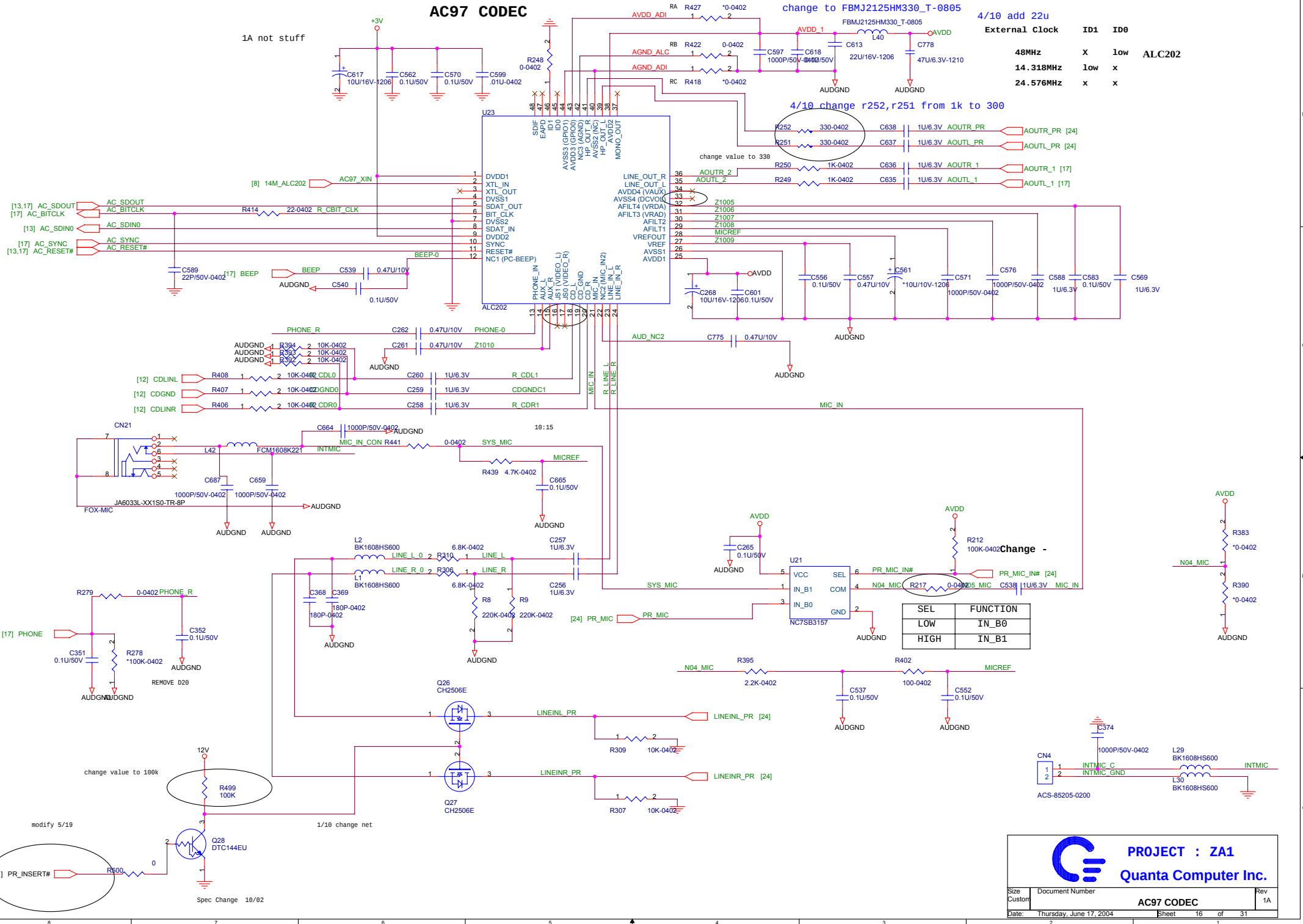
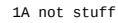
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10/23:Change L13 from TB160808G601 to
TB160808B601(Stock issue)

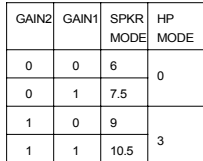


AC97 CODEC



4/10 add 22u			
External Clock	ID1	ID0	
48MHz	X	low	ALC202
14.318MHz	low	x	
24.576MHz	x	x	

SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1



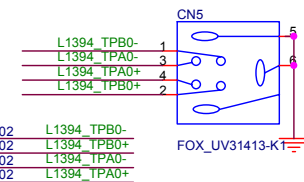
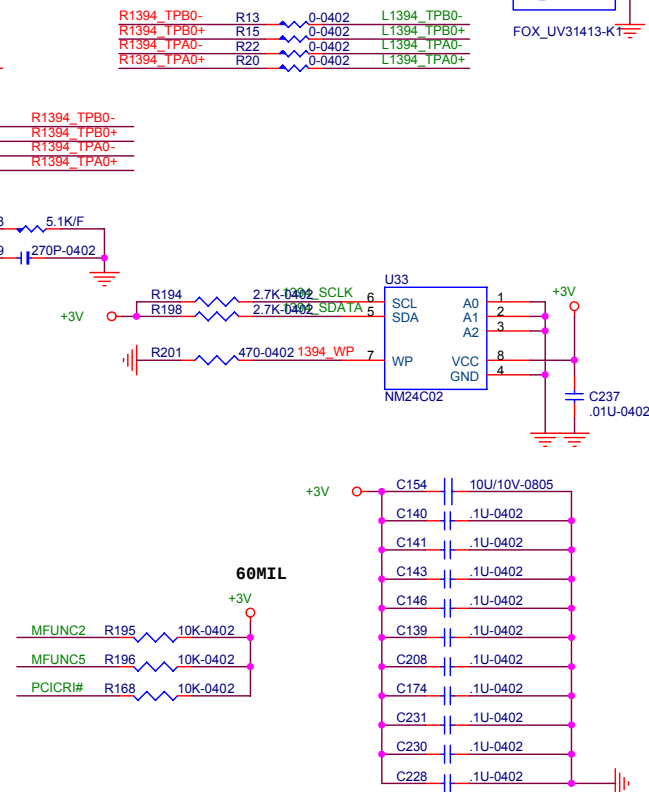
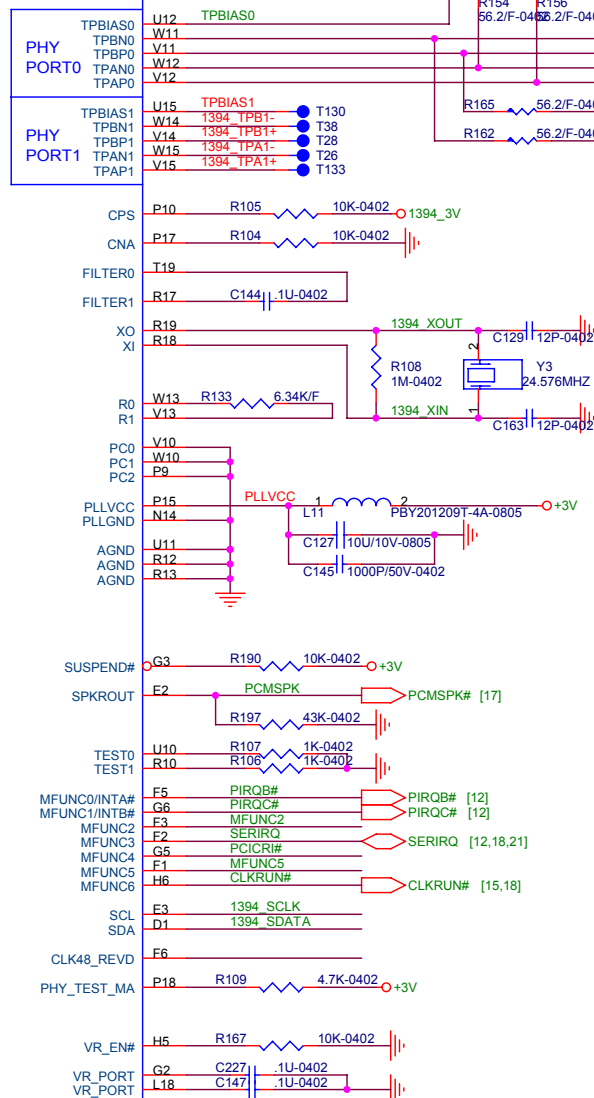
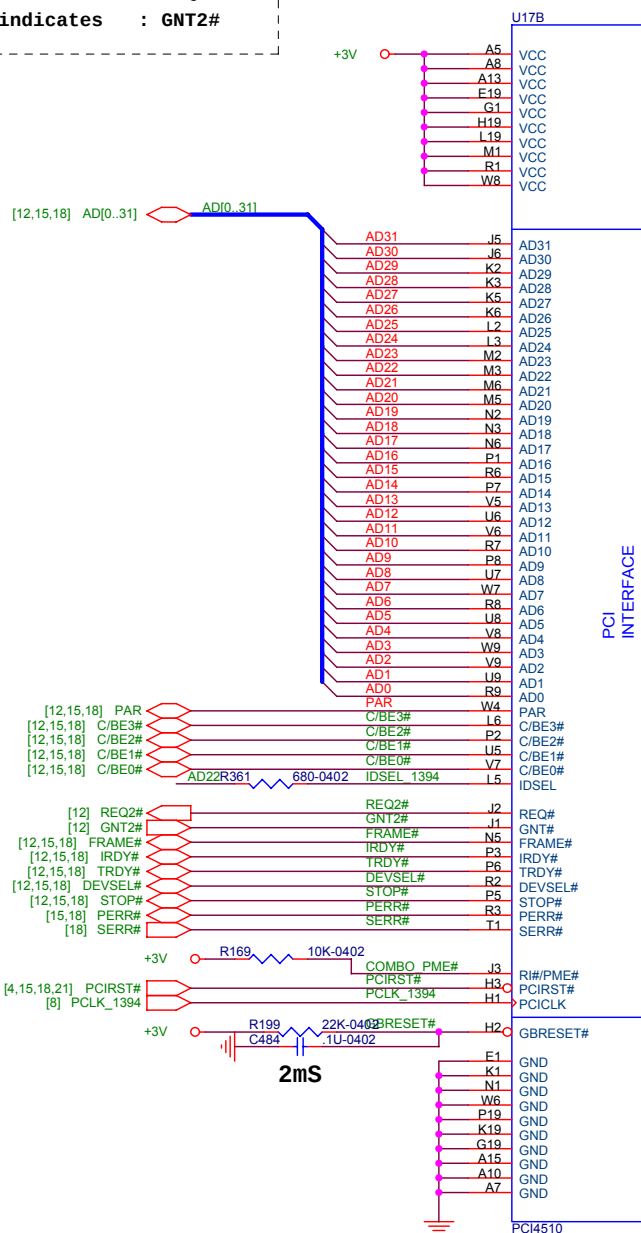
BT CONNECTOR



Size

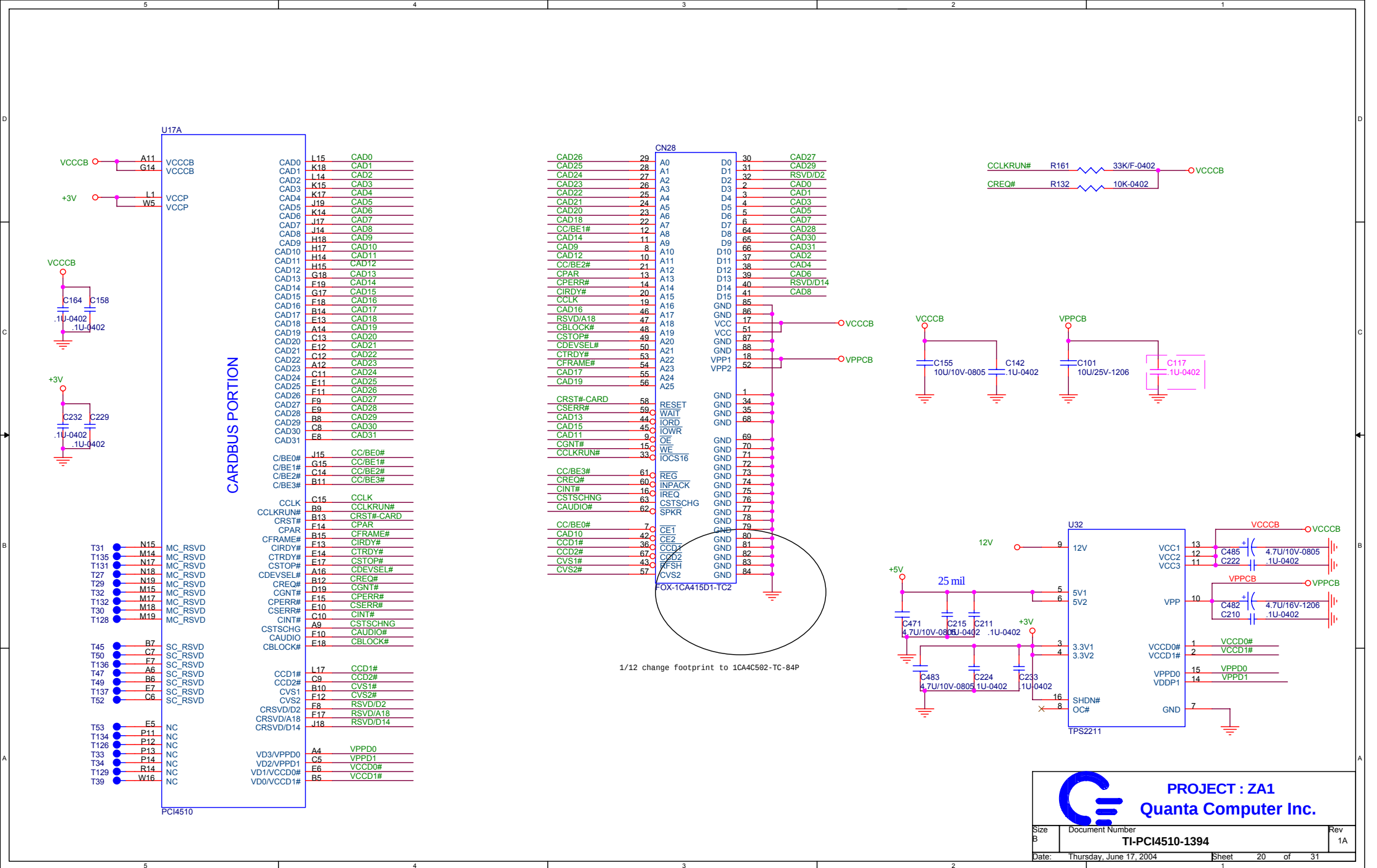

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ID Select      : AD22
Interrupt Pin  : PIRQ
Request indicates : REQ2#
Grant indicates  : GNT2#
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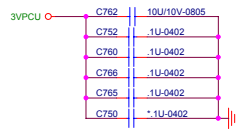
CARDBUS/1394



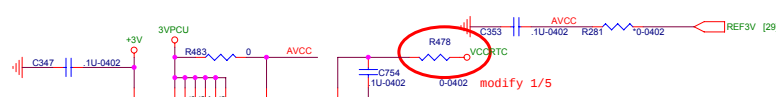
PROJECT : ZA1
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Size B	Document Number TI-PCI4510-1394	Rev 1A
Date:	Thursday, June 17, 2004	Sheet 19 of 31



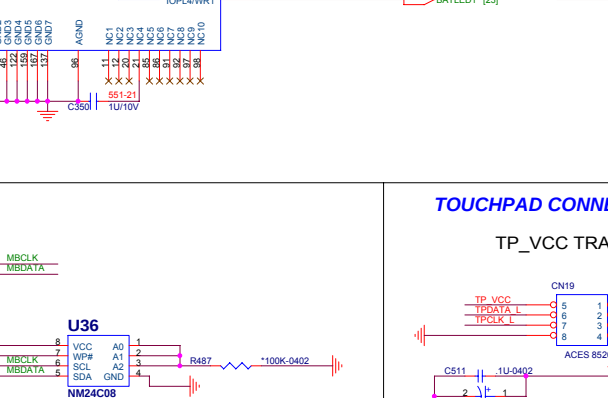
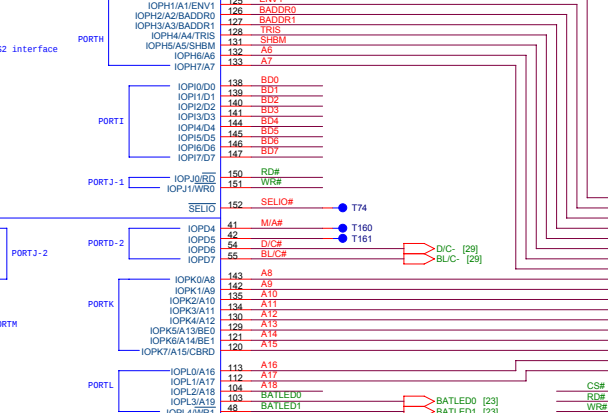
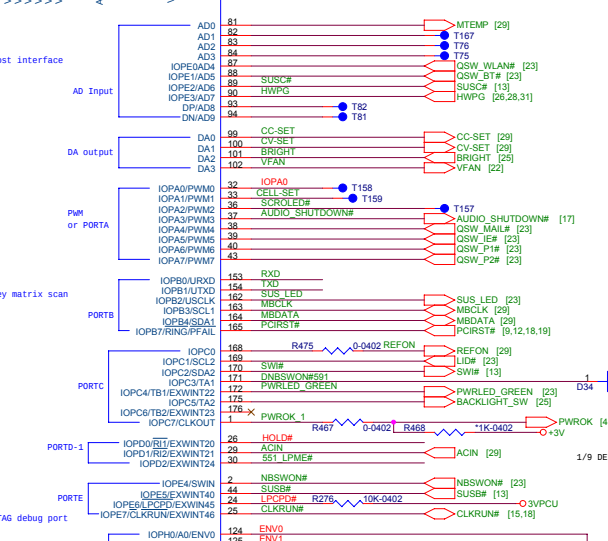
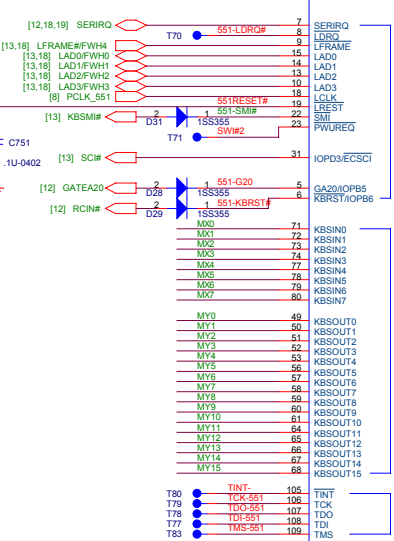


3VPCU : 20MIL

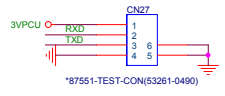


CN18

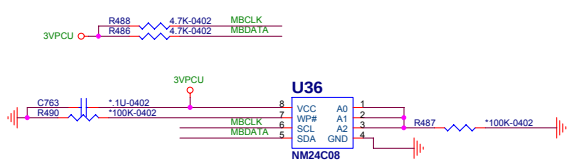
MX1	25	1	MX1
MX2	26	2	MX2
MX3	27	3	MX3
MX4	28	4	MX4
MX5	29	5	MX5
MX6	30	6	MX6
MX7	31	7	MX7
MX8	32	8	MX8
MX9	33	9	MX9
MX10	34	10	MX10
MX11	35	11	MX11
MX12	36	12	MX12
MX13	37	13	MX13
MX14	38	14	MX14
MX15	39	15	MX15
MX16	40	16	MX16
MX17	41	17	MX17
MX18	42	18	MX18
MX19	43	19	MX19
MX20	44	20	MX20
MX21	45	21	MX21
MX22	46	22	MX22
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MX24	48	24	MX24
MX25	49	25	MX25



DEBUG PORT

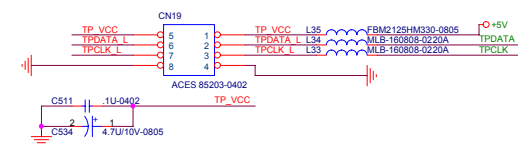


551 EEPROM



TOUCHPAD CONNECTOR

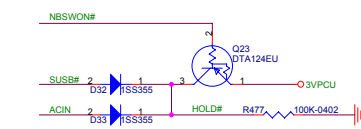
TP_VCC TRACE : 12 mil



LAN WAKE UP



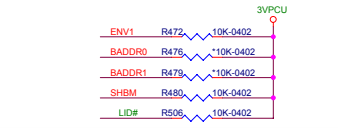
WAKE UP EC



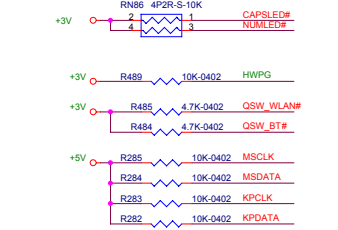
STRAP

SHBM=1: Enable shared memory with host BIOS

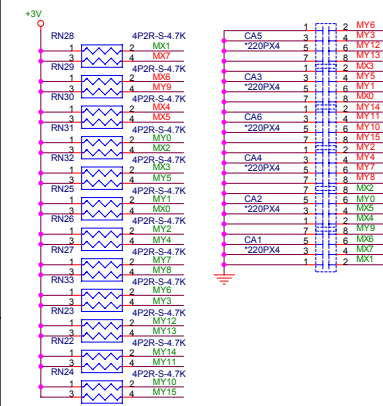
BADDR1-0	Index	I/O Address	Data
0 0	2E	2E	2E
0 1	4E	4E	4E
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1	
1 1		Reserved	

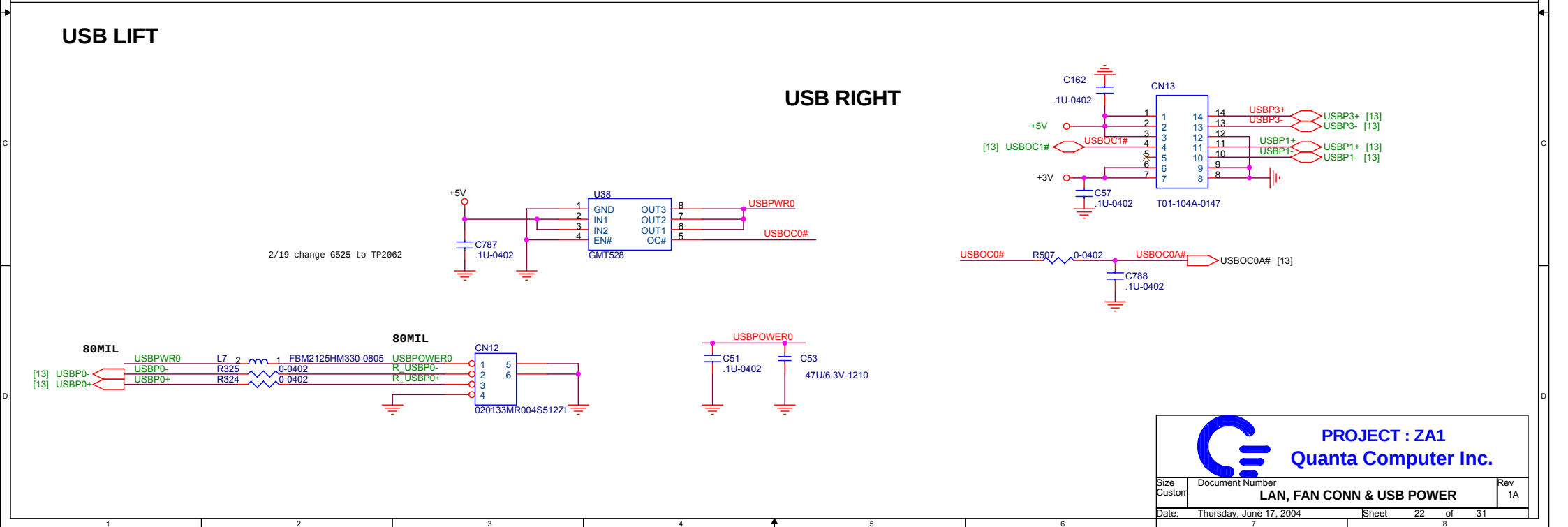
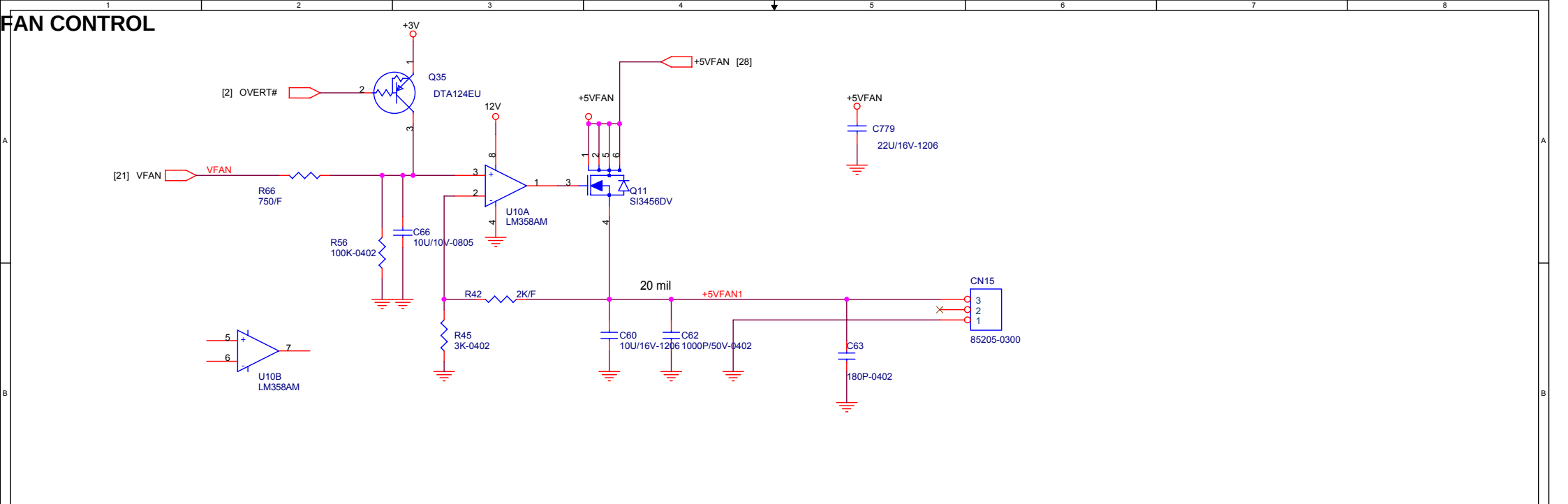


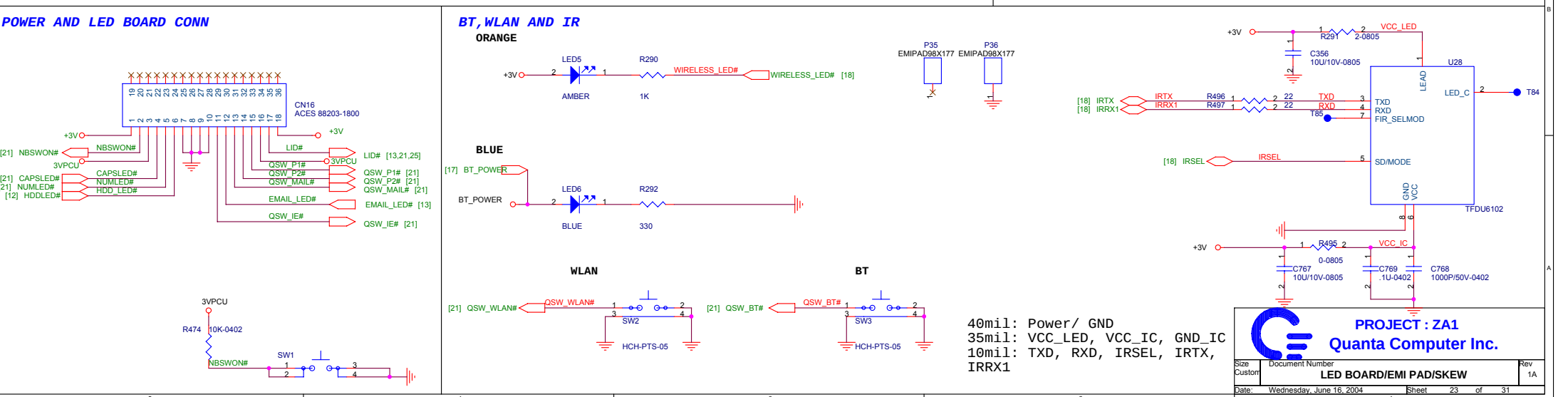
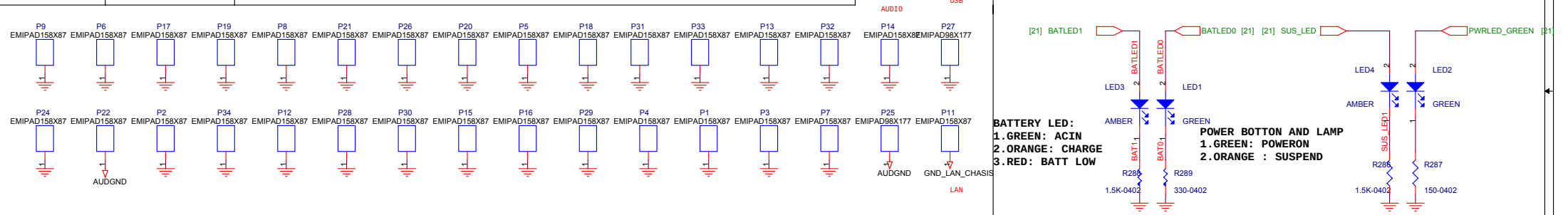
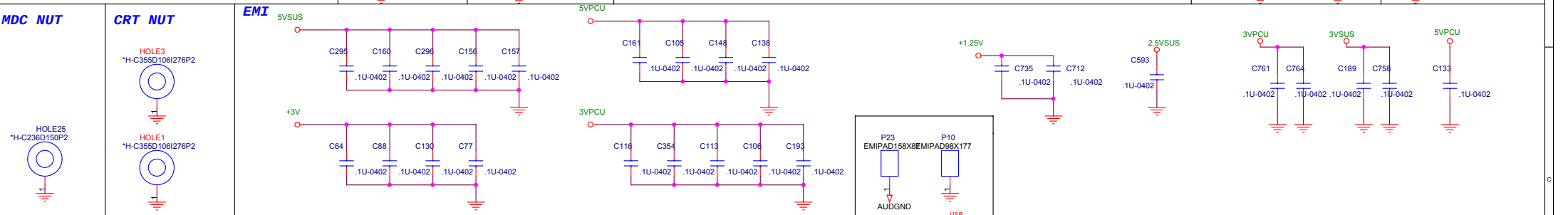
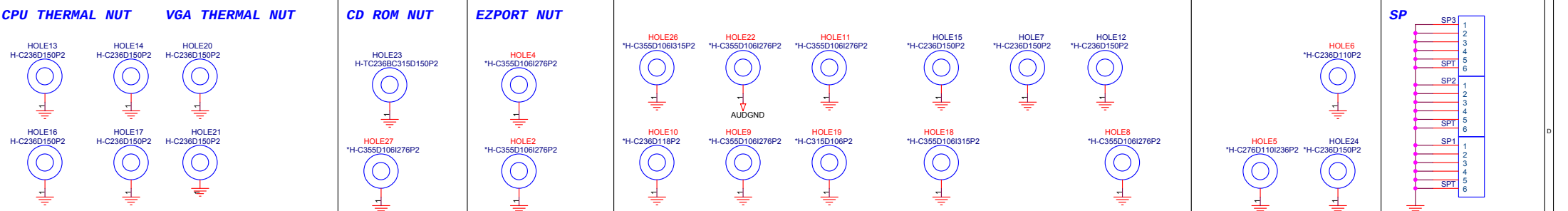
PULL UP

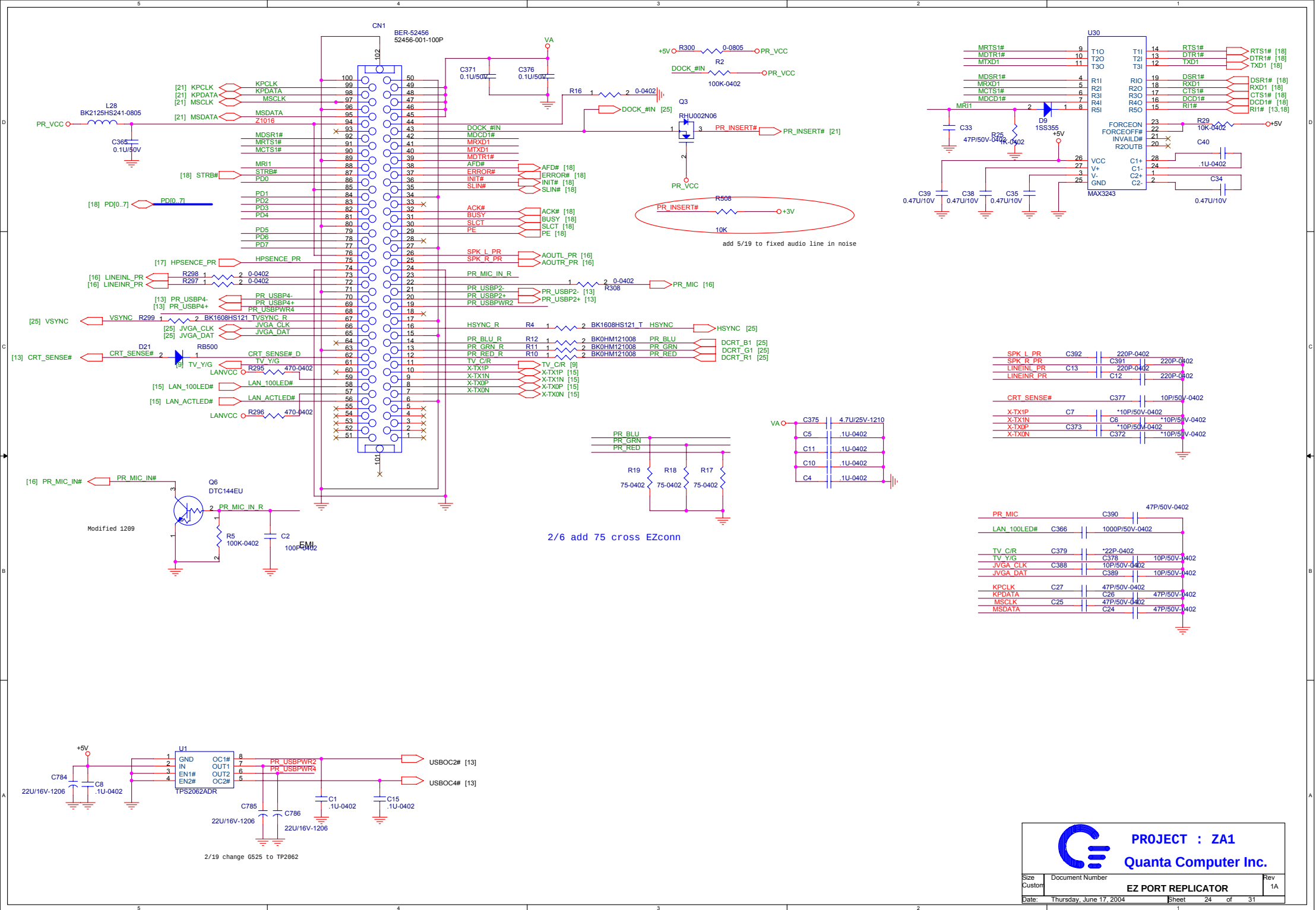


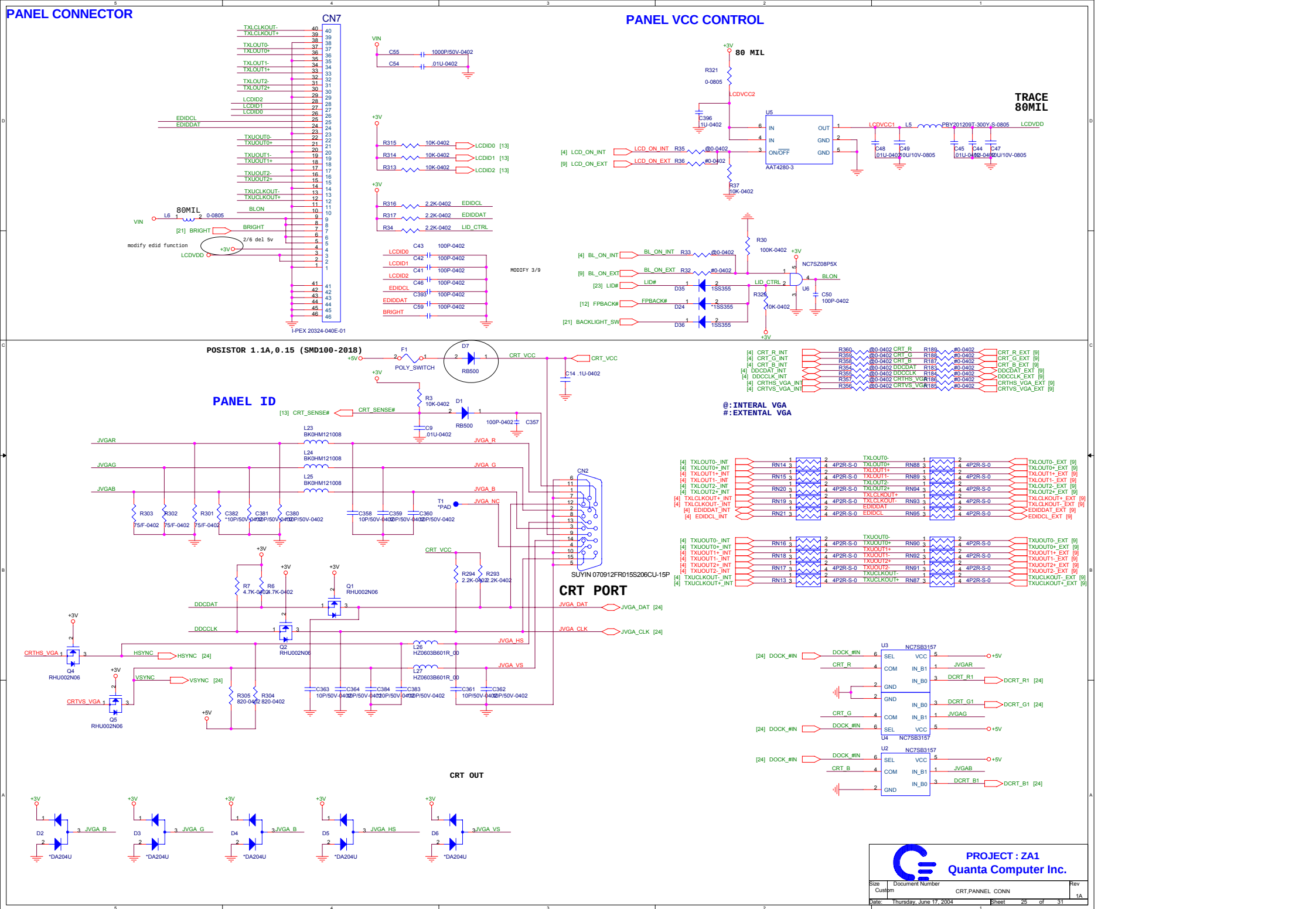
KEYBOARD CONNECTOR

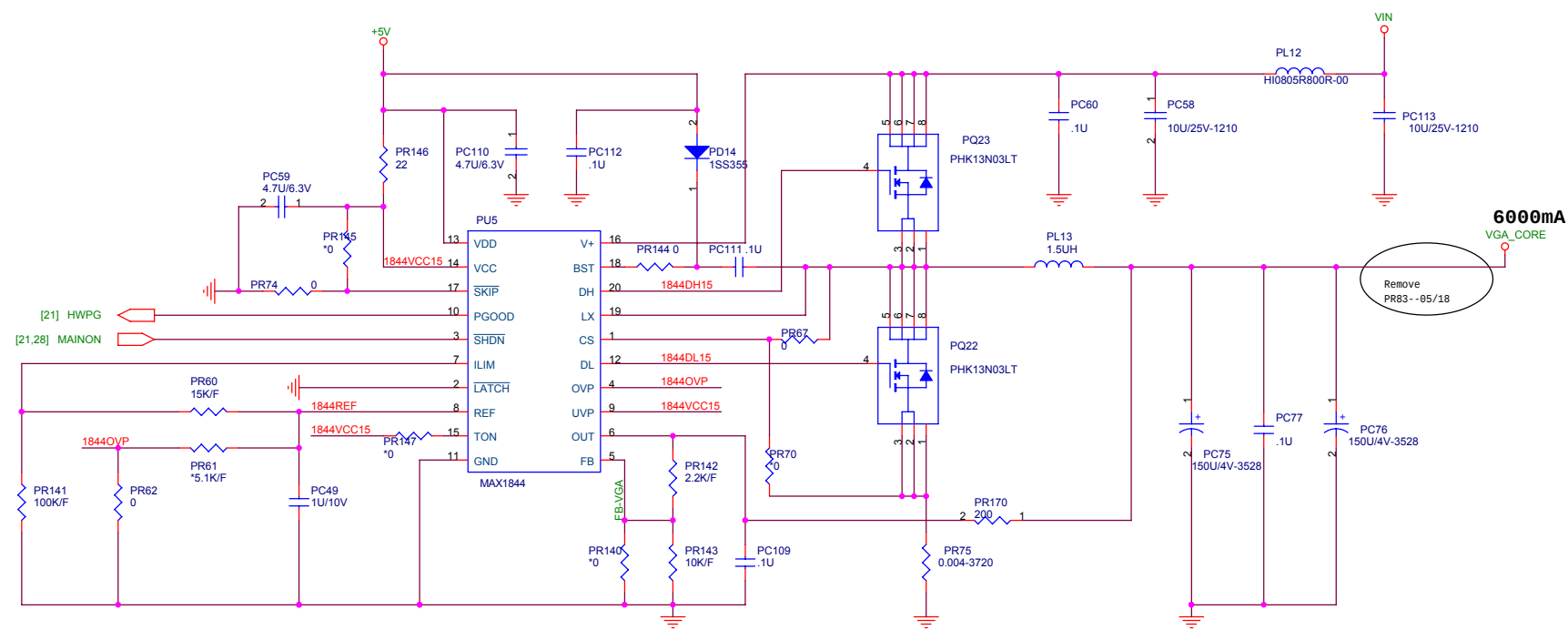






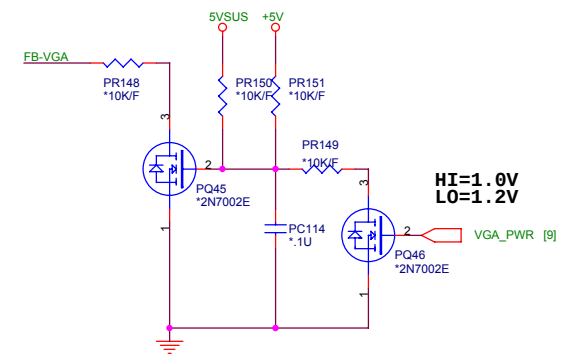
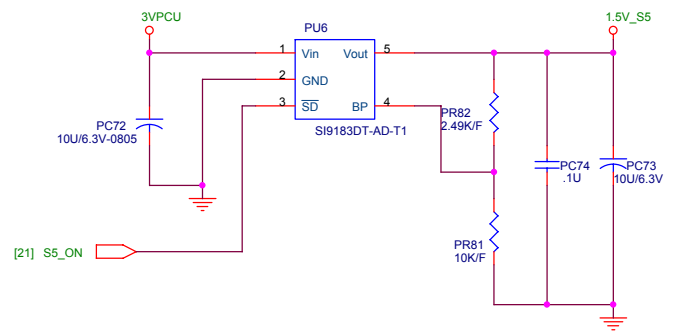
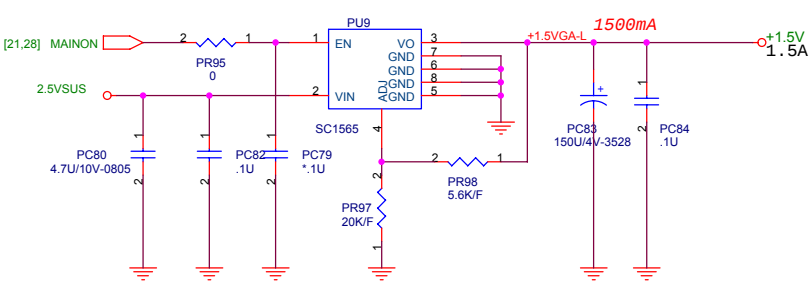






6000mA

Remove
PR83 - 05/18



HI=1.0V
LO=1.2V



PROJECT : ZA1
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