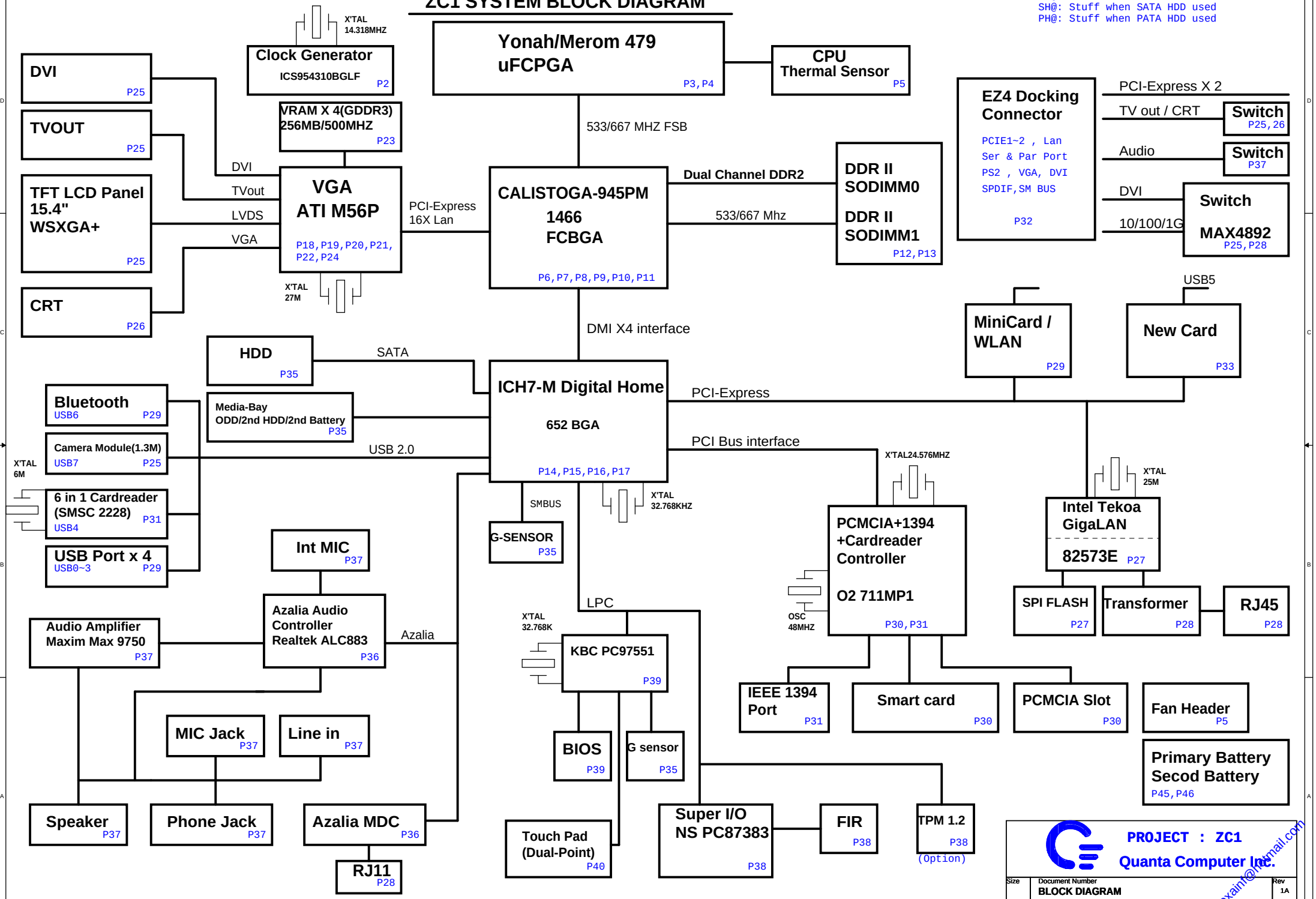
ZC1 SYSTEM BLOCK DIAGRAM

EV@: Stuff when external VGA used
SH@: Stuff when SATA HDD used
PH@: Stuff when PATA HDD used



PROJECT : ZC1		
Quanta Computer Inc.		
Size	Document Number: BLOCK DIAGRAM	Rev 1A
Date: Monday, November 07, 2005	Sheet 1 of 46	

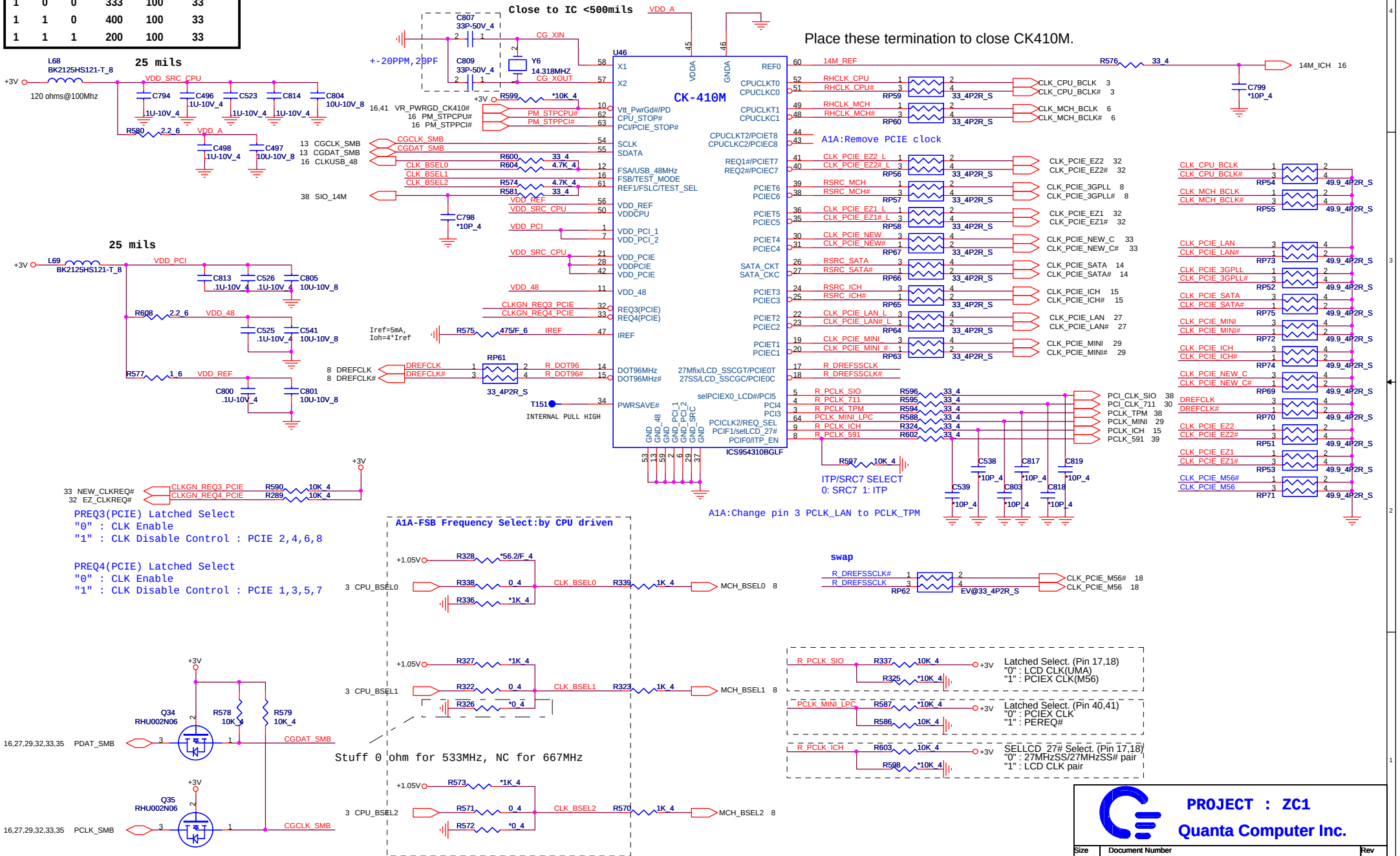
nexaint@hotmail.com

FSC	FSB	FSA	CPU	SRC	PCI	
1	0	1	100	100	33	
0	0	1	133	100	33	Default
0	1	1	166	100	33	
0	1	0	200	100	33	
0	0	0	266	100	33	
1	0	0	333	100	33	
1	1	0	400	100	33	
1	1	1	200	100	33	

A1A-change X1,X2 capacitor from 27pf to 33pf(CL=20pf)

Close to IC <500mils

Place these termination to close CK410M.

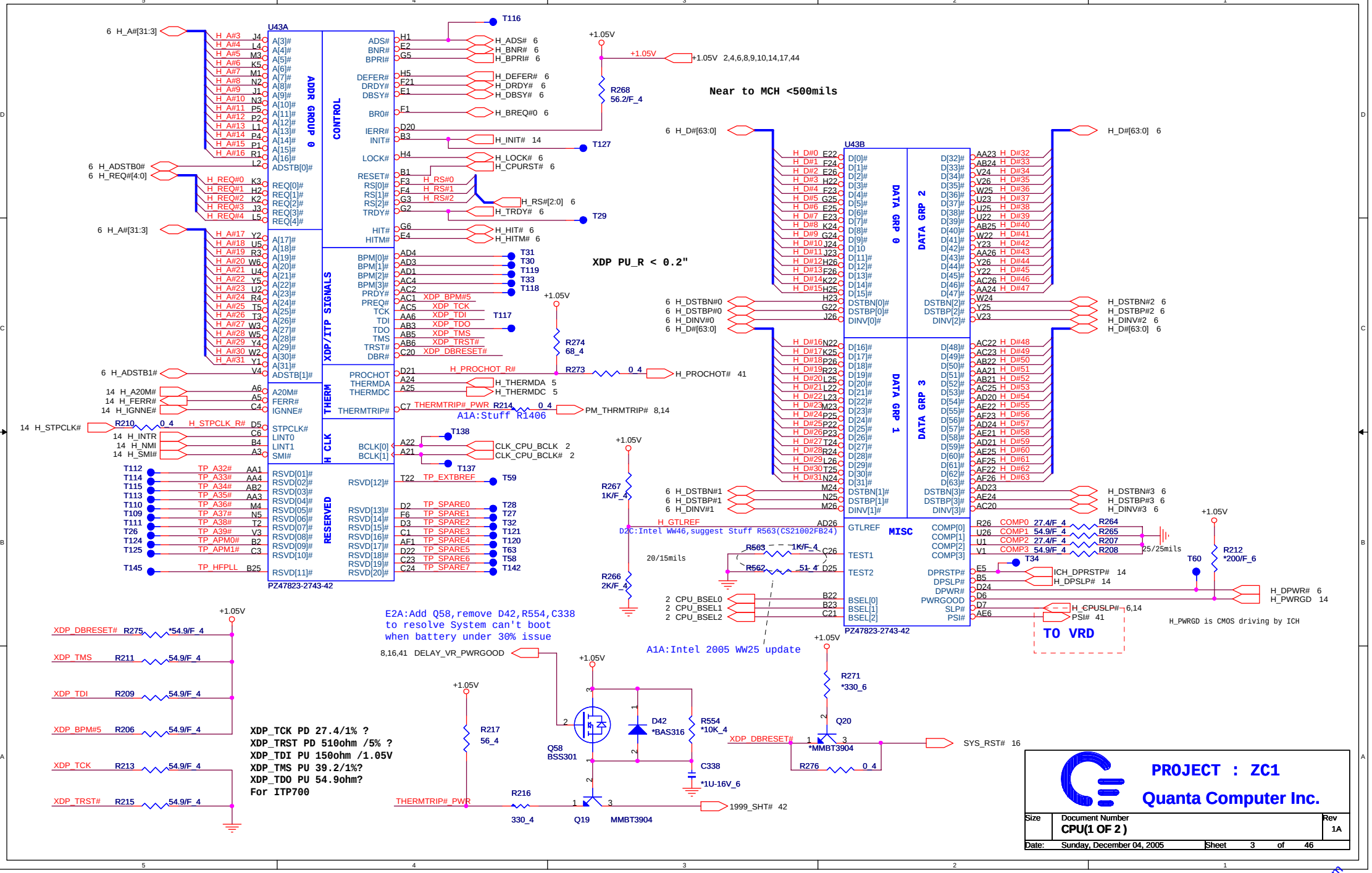


PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	CLOCK GENERATOR	1A

Date: Friday, December 09, 2005 Sheet 2 of 46



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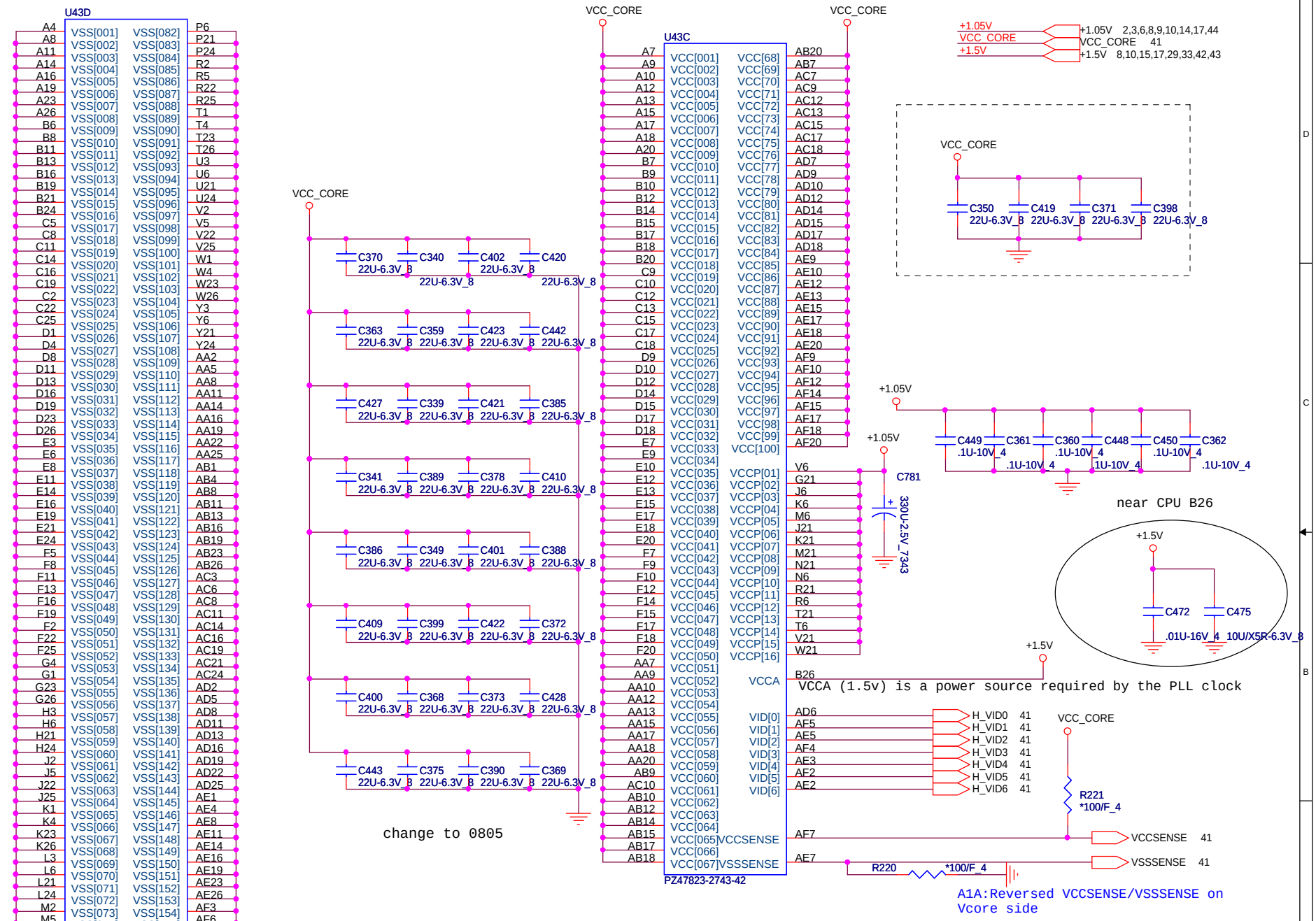
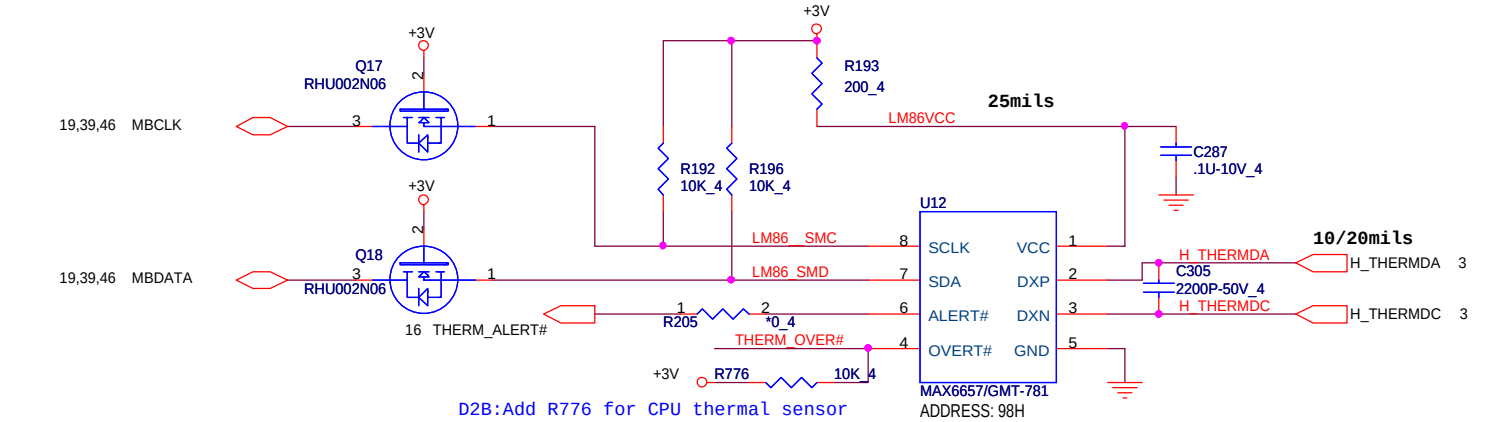
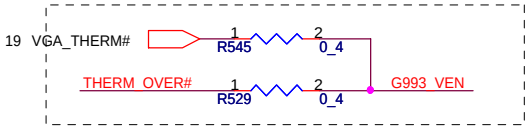

U43D
PZ47823-2743-42
U43C
PZ47823-2743-42
VCC_CORE
+1.05V
+1.5V
C350 22U-6.3V_8
C419 22U-6.3V_8
C371 22U-6.3V_8
C398 22U-6.3V_8
C449 .1U-10V_4
C361 .1U-10V_4
C360 .1U-10V_4
C448 .1U-10V_4
C450 .1U-10V_4
C362 .1U-10V_4
C781 330U-2.5V_7343
near CPU B26
C472 .01U-16V_4
C475 10U/X5R-6.3V_8
VCCA (1.5v) is a power source required by the PLL clock
R221 *100/F_4
R220 *100/F_4
VCCSENSE 41
VSSSENSE 41
A1A:Reversed VCCSENSE/VSSSENSE on Vcore side
change to 0805
PROJECT : ZC1
Quanta Computer Inc.
Size
Document Number
CPU(2 OF 2)
Rev
1A
Date: Monday, November 28, 2005
Sheet 4 of 46

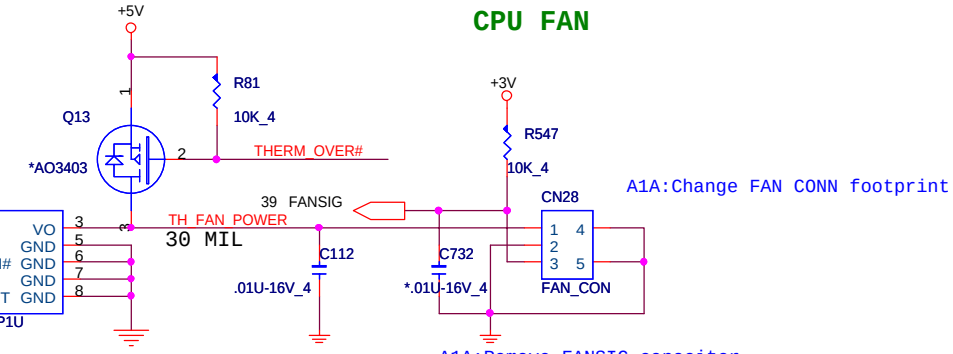


D2B:Add R776 for CPU thermal sensor

D2B:Add R545 for VGA thermal sensor



CPU FAN



A1A:Change FAN CONN footprint

A1A:Change FAN driver to G995

F3B:Add R793,C974 to prevent FAN noise

A1A:Remove FANSIG capacitor

PROJECT : ZC1		
Quanta Computer Inc.		
Size	Document Number: Thermal Sensor,FAN	Rev 1A
Date: Friday, December 02, 2005	Sheet 5 of 46	

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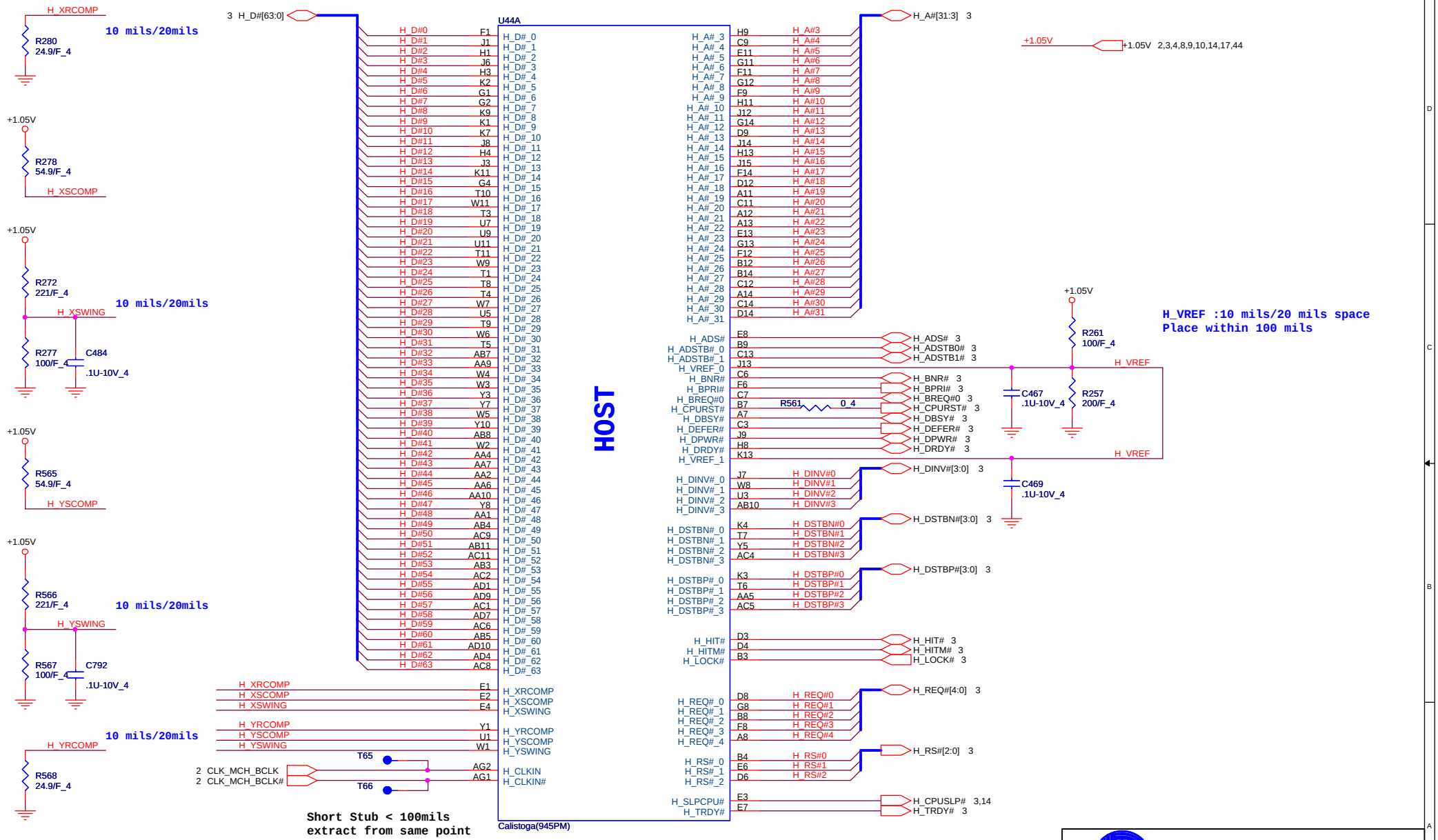
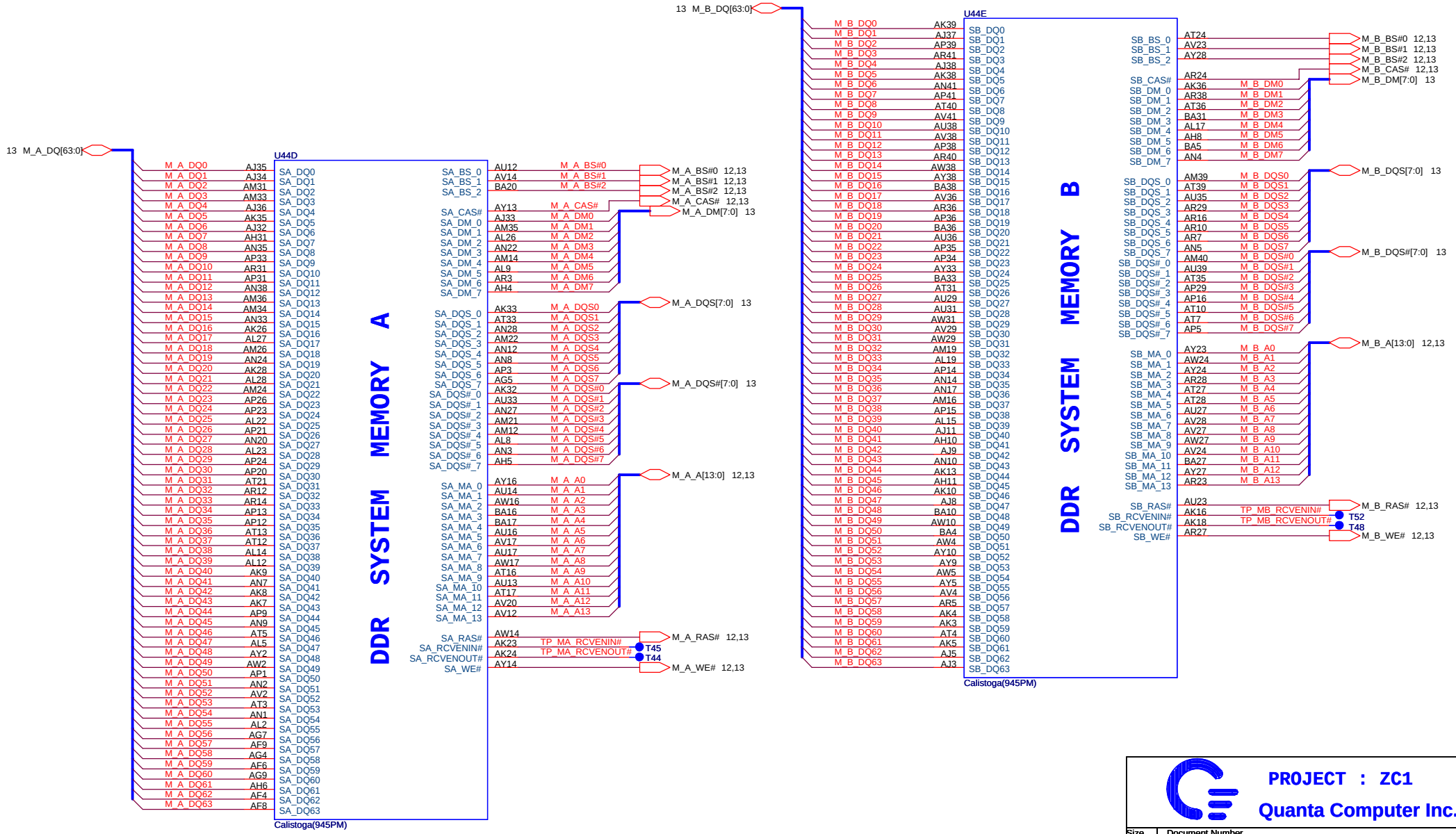


PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	GMCH HOST(1 OF 6)	1A

Date: Friday, December 02, 2005 Sheet 6 of 46



PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	GMCH DDR(2 OF 6)	1A

Date: Friday, December 02, 2005 Sheet 7 of 46

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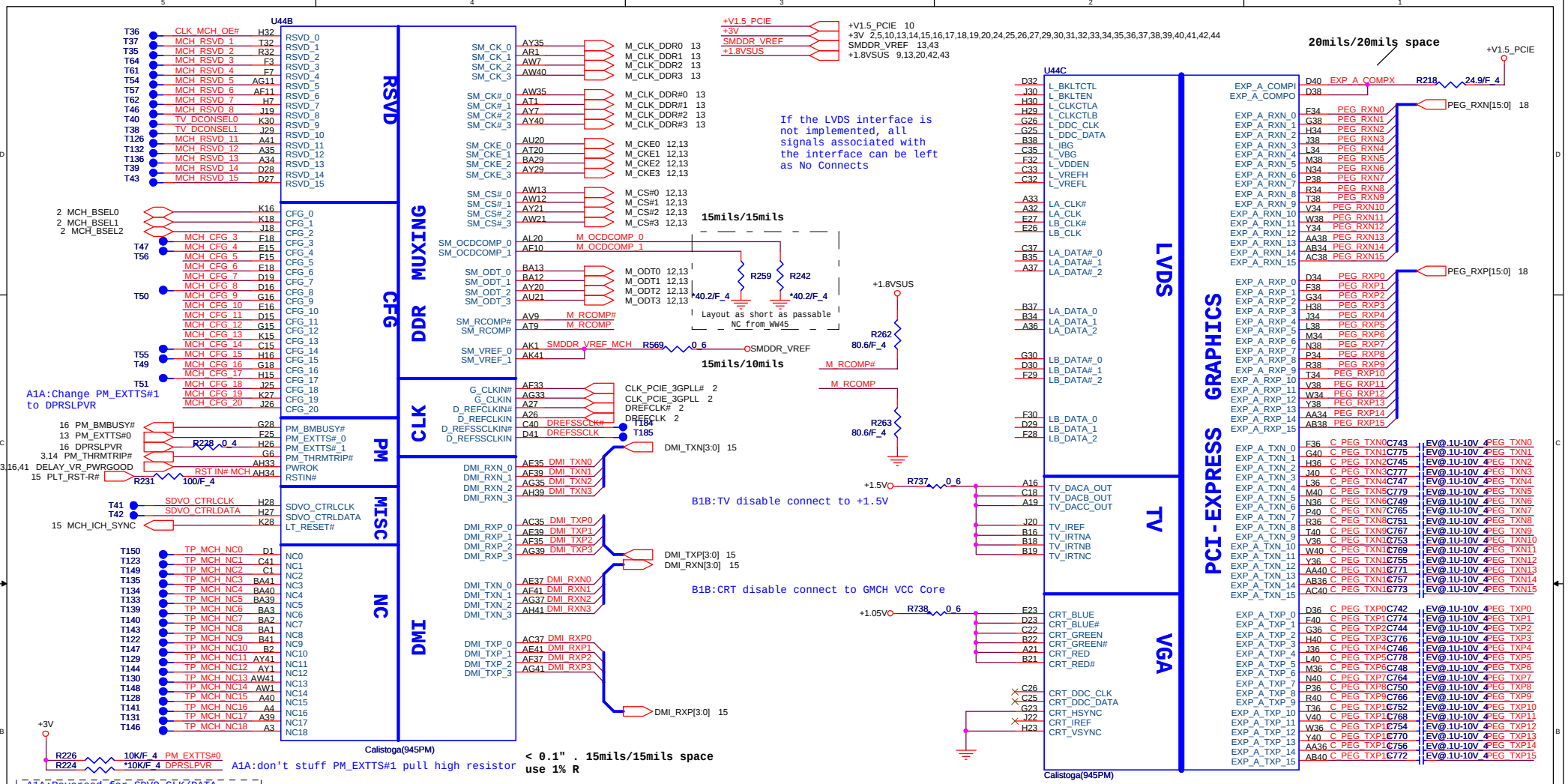
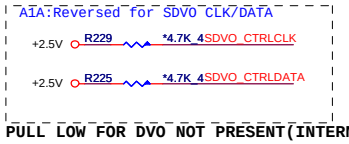


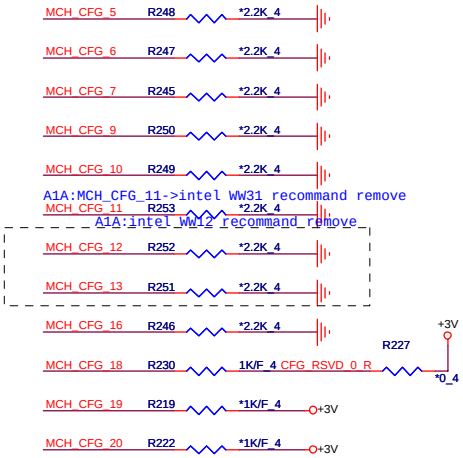
A1A:Reversed for SDVO CLK/DATA



PULL LOW FOR DVO NOT PRESENT(INTERNAL PULLLOW IN 915GM)

1. MCH_CFG_5 Low = DMI X2, High=DMIX4
2. MCH_CFG_6 DDR : Low =Moby Dick, High= Calistoga (Default)
3. MCH_CFG_7 CPU Strap Low=RSVD, High=Mobile CPU
4. MCH_CFG_9 PCI Exp Graphics Lane: Low =Reserved,High=Mobility
5. MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility
6. **MCH_CFG_11: PSB 4x CLK ENABLE Low=Reserved, High=Calistoga**
7. MCH_CFG_16 FSB Dynmic ODT: Low=Dynamic ODT Disabled, High=Dynamic ODT Enabled.
8. MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V
9. MCH_CFG_19 DMI LANE Reversal: Low=Normal,High=LANES Reversed.
10. MCH_CFG_20 PCIE Backward interpoerability mode: Low= only SDVO or PCIE x1 is operational (defaults) ,High=SDVO and PCIE x1 are operation simultaneously via the PEG port.

GMCH Strap pin

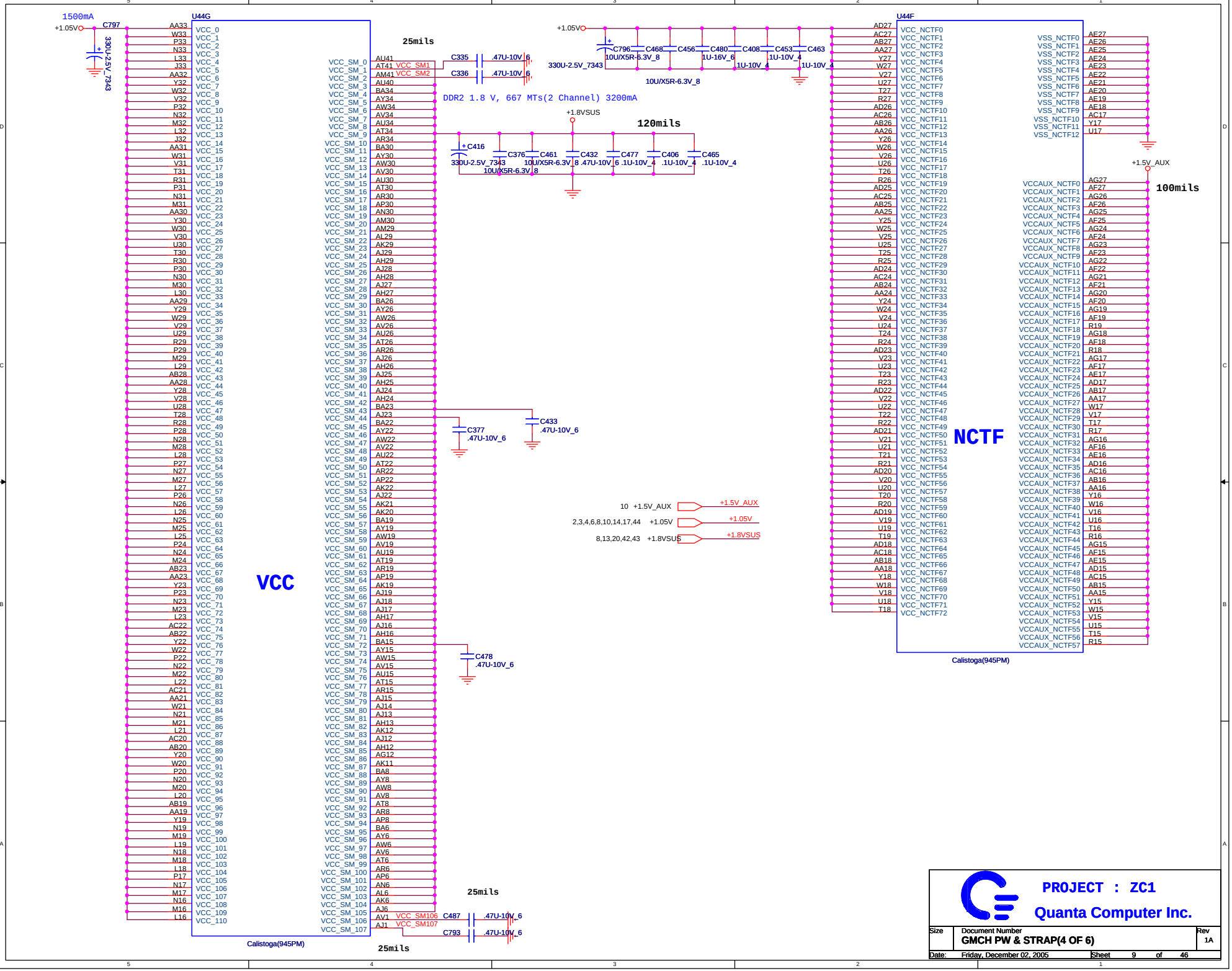


PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	GMCH DMI/VEDIO(3 OF 6)	1A

Date: Tuesday, December 06, 2005 Sheet 8 of 46



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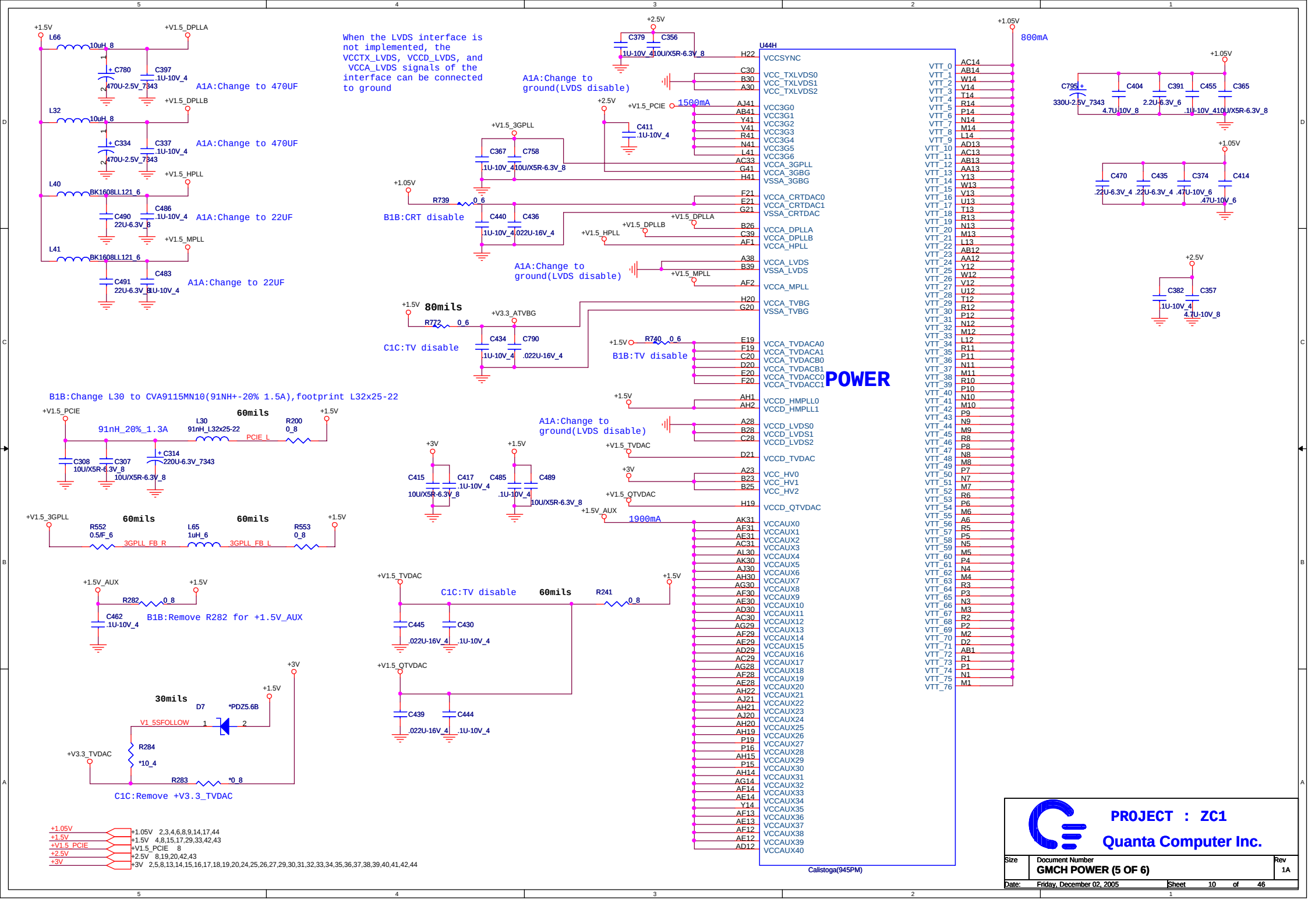
U44H
POWER
Calistoga(945PM)
VCCSYNC
VCC_TXLVDS0
VCC_TXLVDS1
VCC_TXLVDS2
VCC3G0
VCC3G1
VCC3G2
VCC3G3
VCC3G4
VCC3G5
VCC3G6
VCCA_3GPLL
VCCA_3GBG
VSSA_3GBG
VCCA_CRTDAC0
VCCA_CRTDAC1
VSSA_CRTDAC
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_LVDS
VSSA_LVDS
VCCA_MPLL
VCCA_TVBG
VSSA_TVBG
VCCA_TVDACA0
VCCA_TVDACA1
VCCA_TVDACB0
VCCA_TVDACB1
VCCA_TVDACC0
VCCA_TVDACC1
VCCD_HMPLL0
VCCD_HMPLL1
VCCD_LVDS0
VCCD_LVDS1
VCCD_LVDS2
VCCD_TVDAC
VCC_HV0
VCC_HV1
VCC_HV2
VCCD_QTVDAC
VCCAUX0
VCCAUX1
VCCAUX2
VCCAUX3
VCCAUX4
VCCAUX5
VCCAUX6
VCCAUX7
VCCAUX8
VCCAUX9
VCCAUX10
VCCAUX11
VCCAUX12
VCCAUX13
VCCAUX14
VCCAUX15
VCCAUX16
VCCAUX17
VCCAUX18
VCCAUX19
VCCAUX20
VCCAUX21
VCCAUX22
VCCAUX23
VCCAUX24
VCCAUX25
VCCAUX26
VCCAUX27
VCCAUX28
VCCAUX29
VCCAUX30
VCCAUX31
VCCAUX32
VCCAUX33
VCCAUX34
VCCAUX35
VCCAUX36
VCCAUX37
VCCAUX38
VCCAUX39
VCCAUX40
VTT_0
VTT_1
VTT_2
VTT_3
VTT_4
VTT_5
VTT_6
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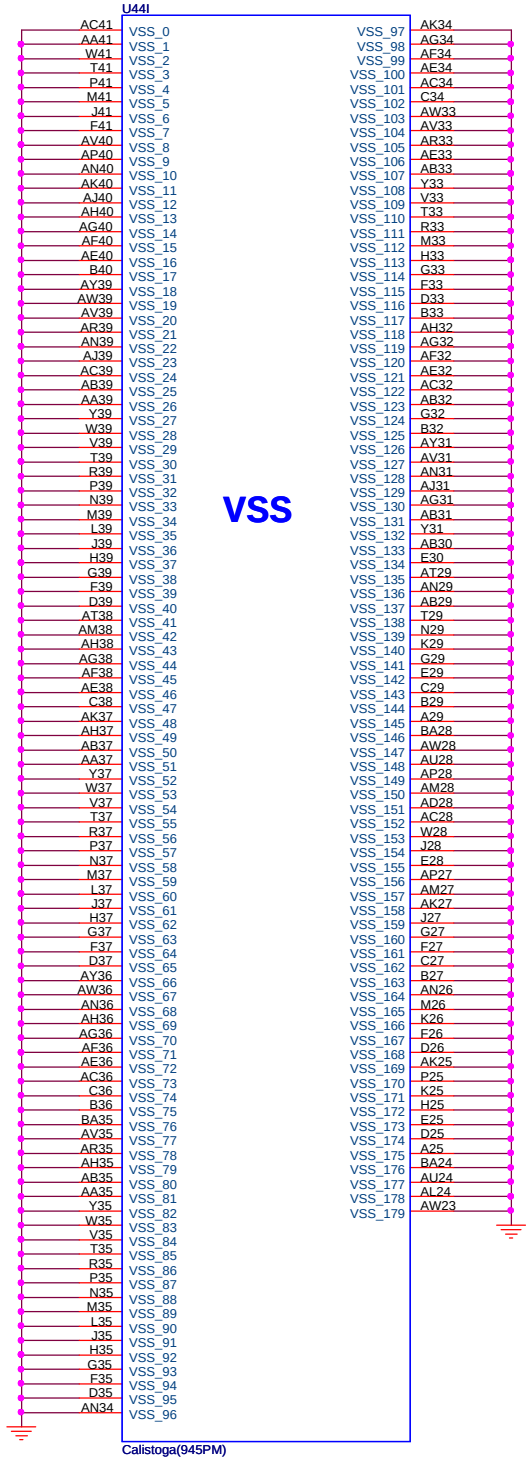
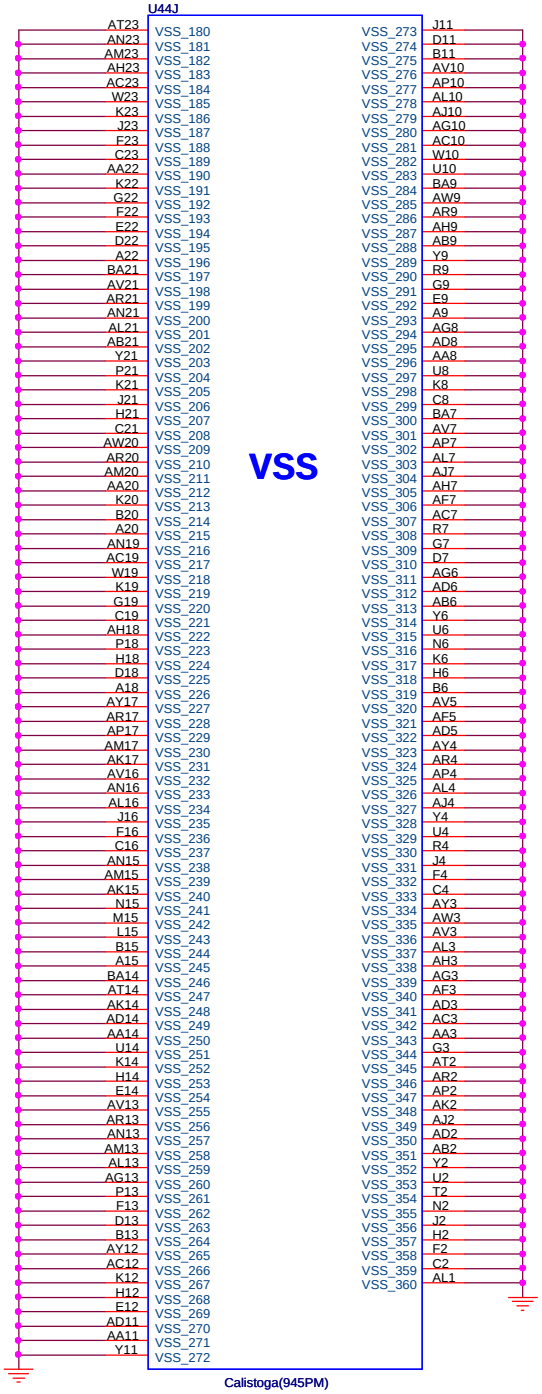
VTT_68
VTT_69
VTT_70
VTT_71
VTT_72
VTT_73
VTT_74
VTT_75
VTT_76
+1.05V
800mA
+1.5V
+V1.5_DPLLA
+V1.5_DPLLB
+V1.5_HPLL
+V1.5_MPLL
+V1.5_3GPLL
+V1.5_PCIE
1500mA
+2.5V
+V3.3_ATVBG
+V3.3_TVDAC
+V1.5_TVDAC
+V1.5_QTVDAC
+1.5V_AUX
1900mA
+3V
L66 10uH_8
L32 10uH_8
L40 BK1608LL121_6
L41 BK1608LL121_6
C780 470U-2.5V_7343
C397 .1U-10V_4
C334 470U-2.5V_7343
C337 .1U-10V_4
C490 22U-6.3V_8
C486 .1U-10V_4
C491 22U-6.3V_8
C483 .1U-10V_4
A1A:Change to 470UF
A1A:Change to 470UF
A1A:Change to 22UF
A1A:Change to 22UF
When the LVDS interface is not implemented, the VCCTX_LVDS, VCCD_LVDS, and VCCA_LVDS signals of the interface can be connected to ground
A1A:Change to ground(LVDS disable)
A1A:Change to ground(LVDS disable)
A1A:Change to ground(LVDS disable)
C379 1U-10V_4
C356 10U/X5R-6.3V_8
C411 .1U-10V_4
C367 .1U-10V_4
C758 10U/X5R-6.3V_8
R739 0_6
B1B:CRT disable
C440 .1U-10V_4
C436 .022U-16V_4
80mils
R772 0_6
C434 .1U-10V_4
C790 .022U-16V_4
C1C:TV disable
R740 0_6
B1B:TV disable
B1B:Change L30 to CVA9115MN10(91NH+-20% 1.5A),footprint L32x25-22
60mils
91nH_20%_1.3A
L30 91nH_L32x25-22
PCIE_L
R200 0_8
C308 10U/X5R-6.3V_8
C307 10U/X5R-6.3V_8
C314 220U-6.3V_7343
C415 10U/X5R-6.3V_8
C417 .1U-10V_4
C485 .1U-10V_4
C489 10U/X5R-6.3V_8
60mils
R552 0.5/F_6
3GPLL_FB_R
L65 1uH_6
3GPLL_FB_L
R553 0_8
R282 0_8
C462 .1U-10V_4
B1B:Remove R282 for +1.5V_AUX
C1C:TV disable
60mils
R241 0_8
C445 .022U-16V_4
C430 .1U-10V_4
C439 .022U-16V_4
C444 .1U-10V_4
30mils
D7 *PDZ5.6B
V1_5SFOLLOW
R284 *10_4
R283 *0_8
C1C:Remove +V3.3_TVDAC
C795 330U-2.5V_7343
C404 4.7U-10V_8
C391 2.2U-6.3V_6
C455 .1U-10V_4
C365 10U/X5R-6.3V_8
C470 .22U-6.3V_4
C435 .22U-6.3V_4
C374 .47U-10V_6
C414 .47U-10V_6
C382 .1U-10V_4
C357 4.7U-10V_8
+1.05V 2,3,4,6,8,9,14,17,44
+1.5V 4,8,15,17,29,33,42,43
+V1.5_PCIE 8
+2.5V 8,19,20,42,43
+3V 2,5,8,13,14,15,16,17,18,19,20,24,25,26,27,29,30,31,32,33,34,35,36,37,38,39,40,41,42,44
PROJECT : ZC1
Quanta Computer Inc.
Size
Document Number
GMCH POWER (5 OF 6)
Rev
1A
Date: Friday, December 02, 2005
Sheet 10 of 46





PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	GMCH GND(6 OF 6)	1A

Date: Friday, December 02, 2005 Sheet 11 of 46

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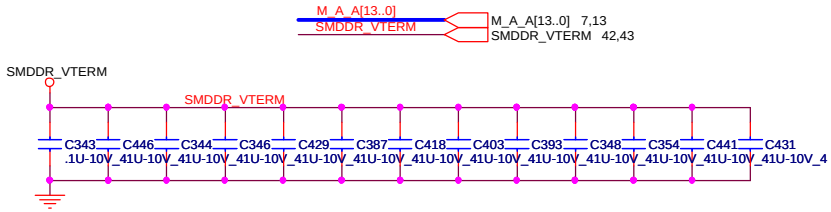
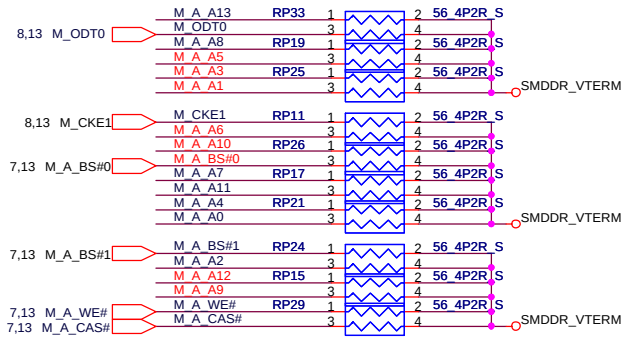
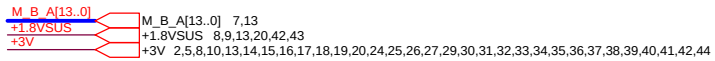
DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL

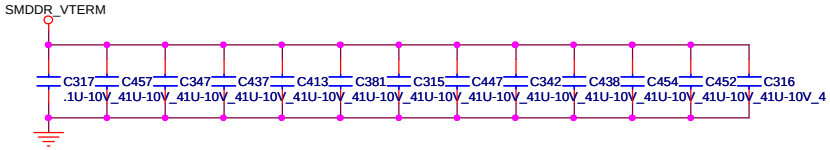


A1A:Swap net



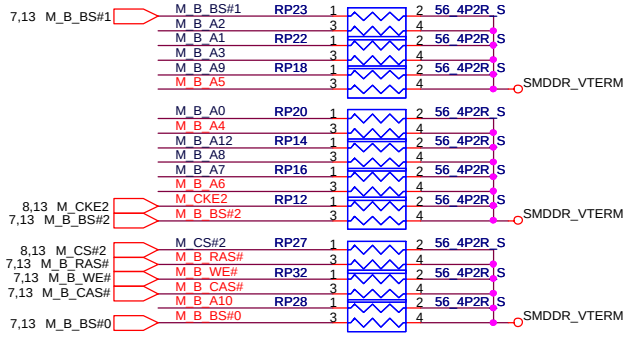


DDRII B CHANNEL

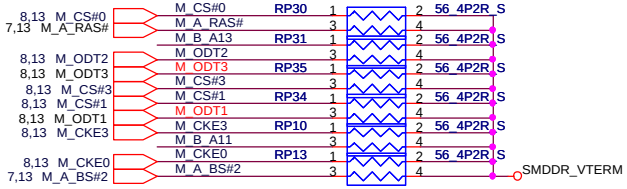


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

A1A:Swap net



A1A:Swap net

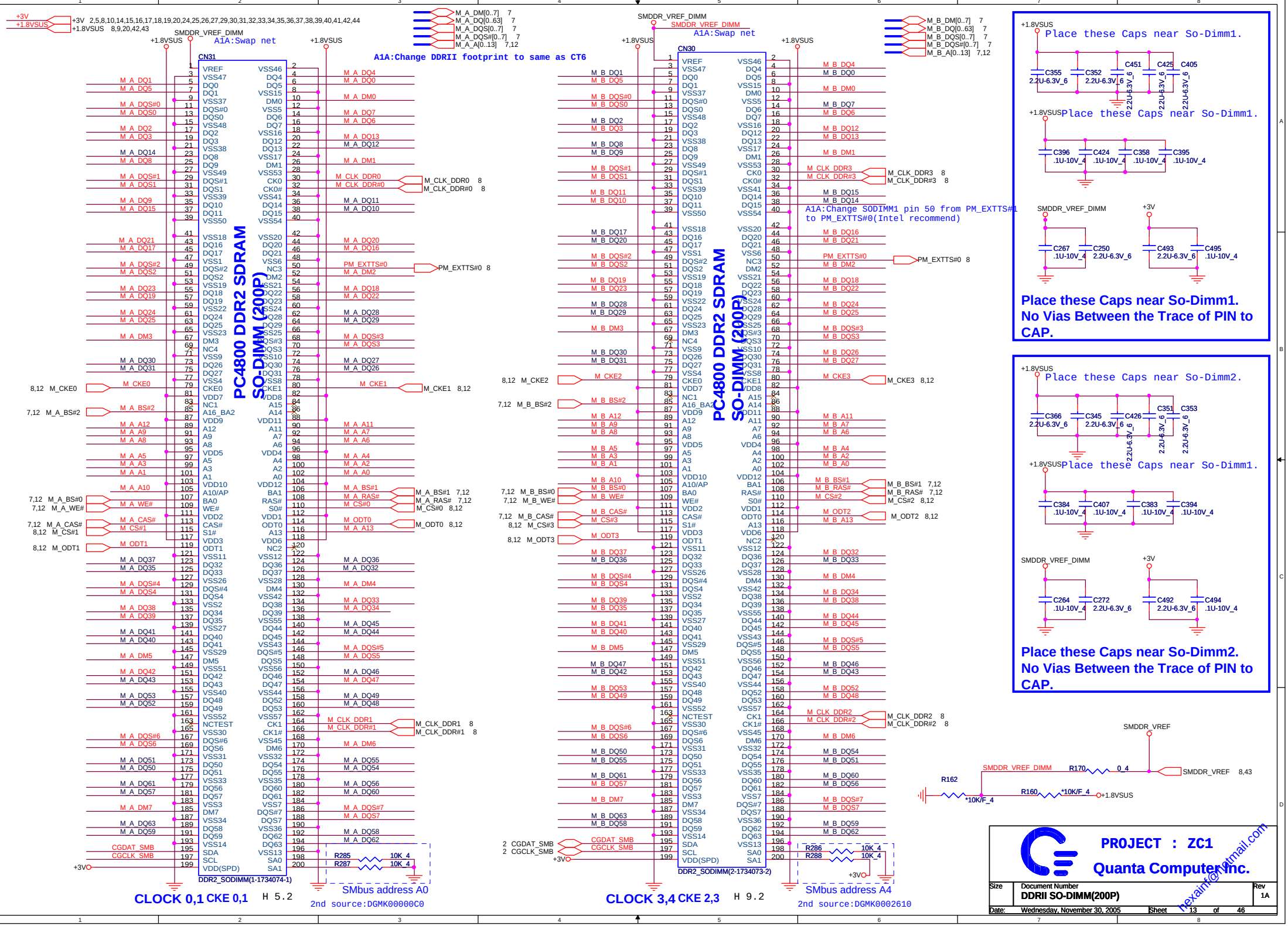


PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	DDR RES. ARRAY	1A

Date: Monday, November 28, 2005 Sheet 12 of 46


CN31
PC4800 DDR2 SDRAM
SO-DIMM (200P)
DDR2_SODIMM(1-1734074-1)
A1A:Swap net
A1A:Change DDRII footprint to same as CT6
SMDDR_VREF_DIMM
CN30
DDR2_SODIMM(2-1734073-2)
A1A:Change SODIMM1 pin 50 from PM_EXTTS#1 to PM_EXTTS#0(Intel recommend)
Place these Caps near So-Dimm1.
Place these Caps near So-Dimm1.
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.
Place these Caps near So-Dimm2.
Place these Caps near So-Dimm1.
Place these Caps near So-Dimm2.
No Vias Between the Trace of PIN to CAP.
SMDDR_VREF
R162 *10K/F_4
R170 0_4
R160 *10K/F_4
SMbus address A0
2nd source:DGMK00000C0
SMbus address A4
2nd source:DGMK0002610
CLOCK 0,1 CKE 0,1 H 5.2
CLOCK 3,4 CKE 2,3 H 9.2
PROJECT : ZC1
Quanta Computer Inc.
Size
Document Number
DDRII SO-DIMM(200P)
Rev
1A
Date: Wednesday, November 30, 2005
Sheet 13 of 46
hexaim@hotmail.com

RTC

CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF
A1A:Change RTXC1/RTXC2 from 10pf to 18pf

A1A:Change RTC Connector footprint

B1B:Per Intel comment,don't stuff R307 for CPUSLP#

Should be 2" close ICH7

A series termination resistor is required for the PRIMARY CODEC

B1B:Add R719 for BIT_CLK_MODEM

ICH7 internal VR enable strap

	INTVRMEN
Enable (default)	1
Disable	0

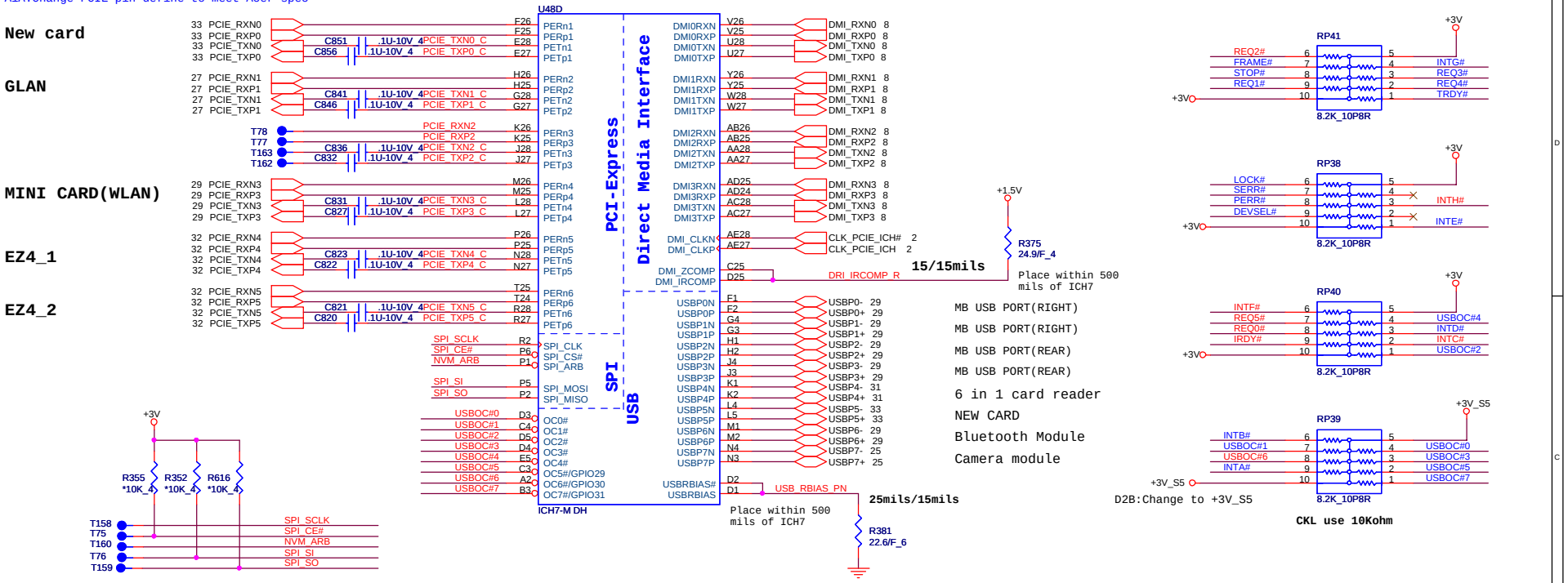
PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M HOST (1 OF 4)	1A

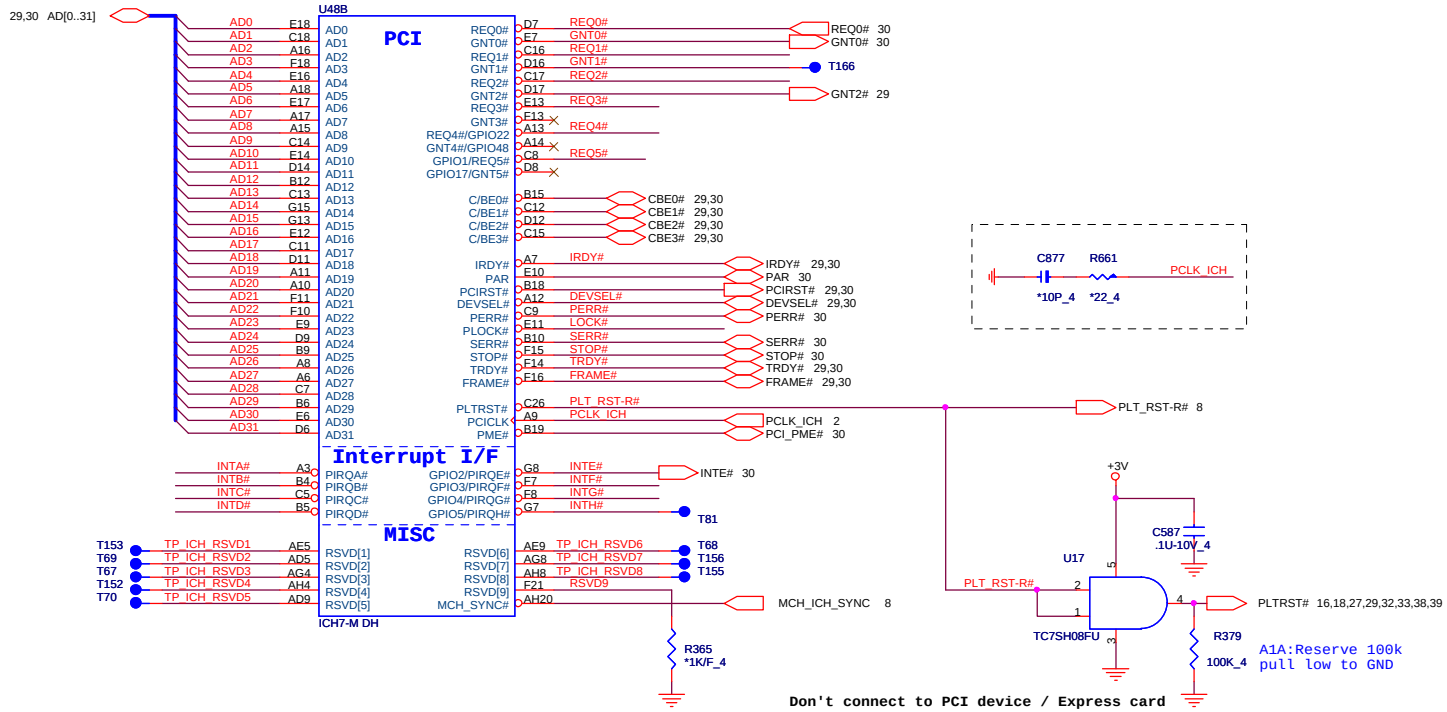
Date: Friday, December 02, 2005 Sheet 14 of 46

A1A:Change PCIE pin define to meet Acer spec



ICH7 Boot BIOS select

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF



PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
OZ711MP1	AD25	REQ0# / GNT0#	INTE#

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M PCI E (2 OF 4)	1A

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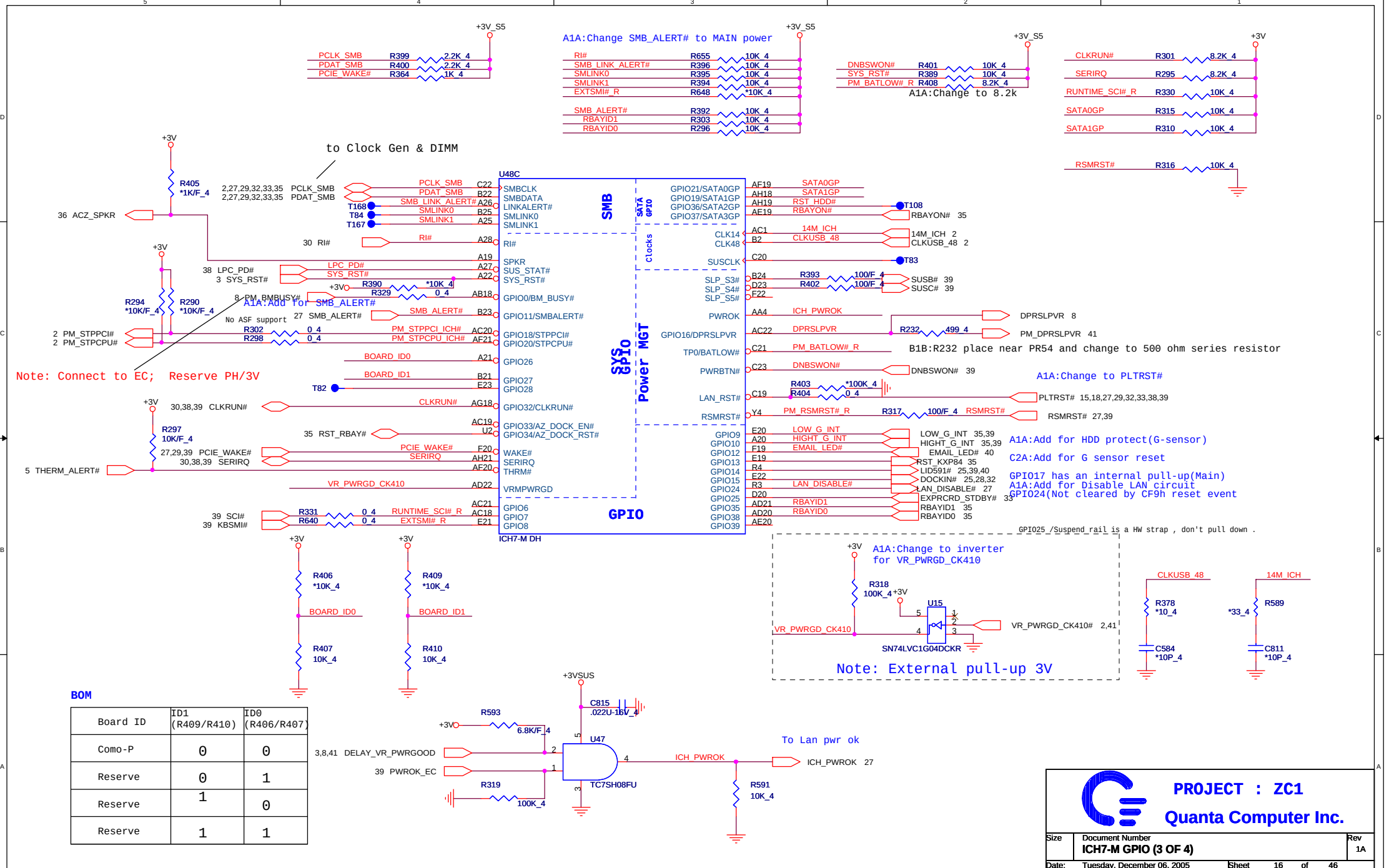
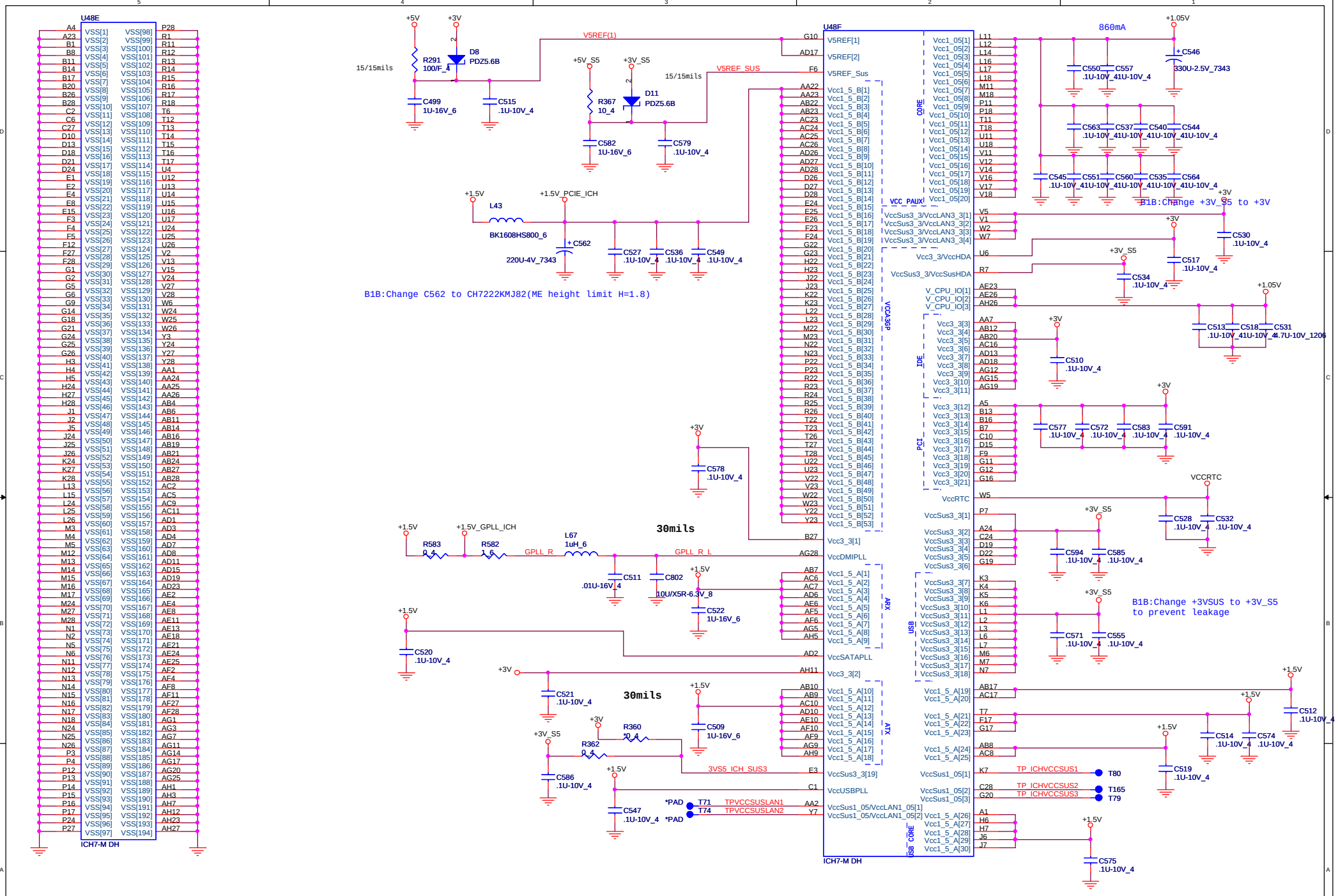


BOM

Board ID	ID1 (R409/R410)	ID0 (R406/R407)
Como-P	0	0
Reserve	0	1
Reserve	1	0
Reserve	1	1



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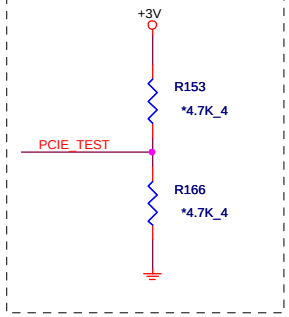
PCIE TEST PADS
PCIE TEST POINTS MUST BE WITHIN 250 MILS
OF THE ASIC BALL WITH POSITIVE AND NEGATIVE
SIGNALS THE SAME DISTANCE

8 PEG_RXP[15:0]
8 PEG_RXN[15:0]
8 PEG_TXP[15:0]
8 PEG_TXN[15:0]

ATI FEATURE NOT ENABLED (M52P,M54P,M56P)
B1B:Don't stuff R153,R166 for PCIE_TEST



U41A

PART 1 OF 7

PCI-EXPRESS INTERFACE

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
PEG_TXP0	AJ31	PCIE_RX0P		PCIE_TX0P	AK27	V_GMCHEXP_RXP0	C304	EV@.1U-10V_4	PEG_RXP0		
PEG_TXN0	AH31	PCIE_RX0N		PCIE_TX0N	AJ27	V_GMCHEXP_RXN0	C303	EV@.1U-10V_4	PEG_RXN0		
PEG_TXP1	AH30	PCIE_RX1P		PCIE_TX1P	AJ25	V_GMCHEXP_RXP1	C333	EV@.1U-10V_4	PEG_RXP1		
PEG_TXN1	AG30	PCIE_RX1N		PCIE_TX1N	AH25	V_GMCHEXP_RXN1	C332	EV@.1U-10V_4	PEG_RXN1		
PEG_TXP2	AG32	PCIE_RX2P		PCIE_TX2P	AH28	V_GMCHEXP_RXP2	C302	EV@.1U-10V_4	PEG_RXP2		
PEG_TXN2	AF32	PCIE_RX2N		PCIE_TX2N	AG28	V_GMCHEXP_RXN2	C301	EV@.1U-10V_4	PEG_RXN2		
PEG_TXP3	AF31	PCIE_RX3P		PCIE_TX3P	AG27	V_GMCHEXP_RXP3	C331	EV@.1U-10V_4	PEG_RXP3		
PEG_TXN3	AE31	PCIE_RX3N		PCIE_TX3N	AF27	V_GMCHEXP_RXN3	C330	EV@.1U-10V_4	PEG_RXN3		
PEG_TXP4	AE30	PCIE_RX4P		PCIE_TX4P	AF25	V_GMCHEXP_RXP4	C300	EV@.1U-10V_4	PEG_RXP4		
PEG_TXN4	AD30	PCIE_RX4N		PCIE_TX4N	AE25	V_GMCHEXP_RXN4	C299	EV@.1U-10V_4	PEG_RXN4		
PEG_TXP5	AD32	PCIE_RX5P		PCIE_TX5P	AE28	V_GMCHEXP_RXP5	C329	EV@.1U-10V_4	PEG_RXP5		
PEG_TXN5	AC32	PCIE_RX5N		PCIE_TX5N	AD28	V_GMCHEXP_RXN5	C328	EV@.1U-10V_4	PEG_RXN5		
PEG_TXP6	AC31	PCIE_RX6P		PCIE_TX6P	AD27	V_GMCHEXP_RXP6	C298	EV@.1U-10V_4	PEG_RXP6		
PEG_TXN6	AB31	PCIE_RX6N		PCIE_TX6N	AC27	V_GMCHEXP_RXN6	C297	EV@.1U-10V_4	PEG_RXN6		
PEG_TXP7	AB30	PCIE_RX7P		PCIE_TX7P	AC25	V_GMCHEXP_RXP7	C327	EV@.1U-10V_4	PEG_RXP7		
PEG_TXN7	AA30	PCIE_RX7N		PCIE_TX7N	AB25	V_GMCHEXP_RXN7	C326	EV@.1U-10V_4	PEG_RXN7		
PEG_TXP8	AA32	PCIE_RX8P		PCIE_TX8P	AB28	V_GMCHEXP_RXP8	C296	EV@.1U-10V_4	PEG_RXP8		
PEG_TXN8	Y32	PCIE_RX8N		PCIE_TX8N	AA28	V_GMCHEXP_RXN8	C295	EV@.1U-10V_4	PEG_RXN8		
PEG_TXP9	Y31	PCIE_RX9P		PCIE_TX9P	AA27	V_GMCHEXP_RXP9	C325	EV@.1U-10V_4	PEG_RXP9		
PEG_TXN9	W31	PCIE_RX9N		PCIE_TX9N	Y27	V_GMCHEXP_RXN9	C324	EV@.1U-10V_4	PEG_RXN9		
PEG_TXP10	W30	PCIE_RX10P		PCIE_TX10P	Y25	V_GMCHEXP_RXP10	C294	EV@.1U-10V_4	PEG_RXP10		
PEG_TXN10	V30	PCIE_RX10N		PCIE_TX10N	W25	V_GMCHEXP_RXN10	C293	EV@.1U-10V_4	PEG_RXN10		
PEG_TXP11	V32	PCIE_RX11P		PCIE_TX11P	W28	V_GMCHEXP_RXP11	C323	EV@.1U-10V_4	PEG_RXP11		
PEG_TXN11	U32	PCIE_RX11N		PCIE_TX11N	V28	V_GMCHEXP_RXN11	C322	EV@.1U-10V_4	PEG_RXN11		
PEG_TXP12	U31	PCIE_RX12P		PCIE_TX12P	V27	V_GMCHEXP_RXP12	C292	EV@.1U-10V_4	PEG_RXP12		
PEG_TXN12	T31	PCIE_RX12N		PCIE_TX12N	U27	V_GMCHEXP_RXN12	C291	EV@.1U-10V_4	PEG_RXN12		
PEG_TXP13	T30	PCIE_RX13P		PCIE_TX13P	U25	V_GMCHEXP_RXP13	C321	EV@.1U-10V_4	PEG_RXP13		
PEG_TXN13	R30	PCIE_RX13N		PCIE_TX13N	T25	V_GMCHEXP_RXN13	C320	EV@.1U-10V_4	PEG_RXN13		
PEG_TXP14	R32	PCIE_RX14P		PCIE_TX14P	T28	V_GMCHEXP_RXP14	C290	EV@.1U-10V_4	PEG_RXP14		
PEG_TXN14	P32	PCIE_RX14N		PCIE_TX14N	R28	V_GMCHEXP_RXN14	C289	EV@.1U-10V_4	PEG_RXN14		
PEG_TXP15	P31	PCIE_RX15P		PCIE_TX15P	R27	V_GMCHEXP_RXP15	C319	EV@.1U-10V_4	PEG_RXP15		
PEG_TXN15	N31	PCIE_RX15N		PCIE_TX15N	P27	V_GMCHEXP_RXN15	C318	EV@.1U-10V_4	PEG_RXN15		

Clock

Signal	Pin	Signal
AL28	PCIE_REFCLKP	
AK28	PCIE_REFCLKN	
AG24	PERSTB	
AA24	PCIE_TEST	
AF24	PERSTB_MASK	

Tie To VSS

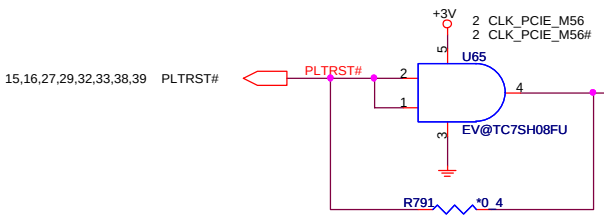
Calibration

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
AE24	PCIE_CALRN	R156	EV@2K/F_4	+1.2V_VPCIE			
AD24	PCIE_CALRP	R172	EV@562/F_4				
AB24	PCIE_CALI	R167	EV@1.47K/F_4				

EV@M56-P B13

B1B:PCIE_CALRN(ball AE24) need change to +1.2V_VPCIE

FOR M52P,M54P,M56P
PCIE_CALRN = 2K
PCIE CALRP = 562R
PCIE CALI = 1.47K



E3A:Add U65 for M56 PLTRST#

PROJECT : ZC1

Quanta Computer Inc.

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	M56P 1 OF 7	1A

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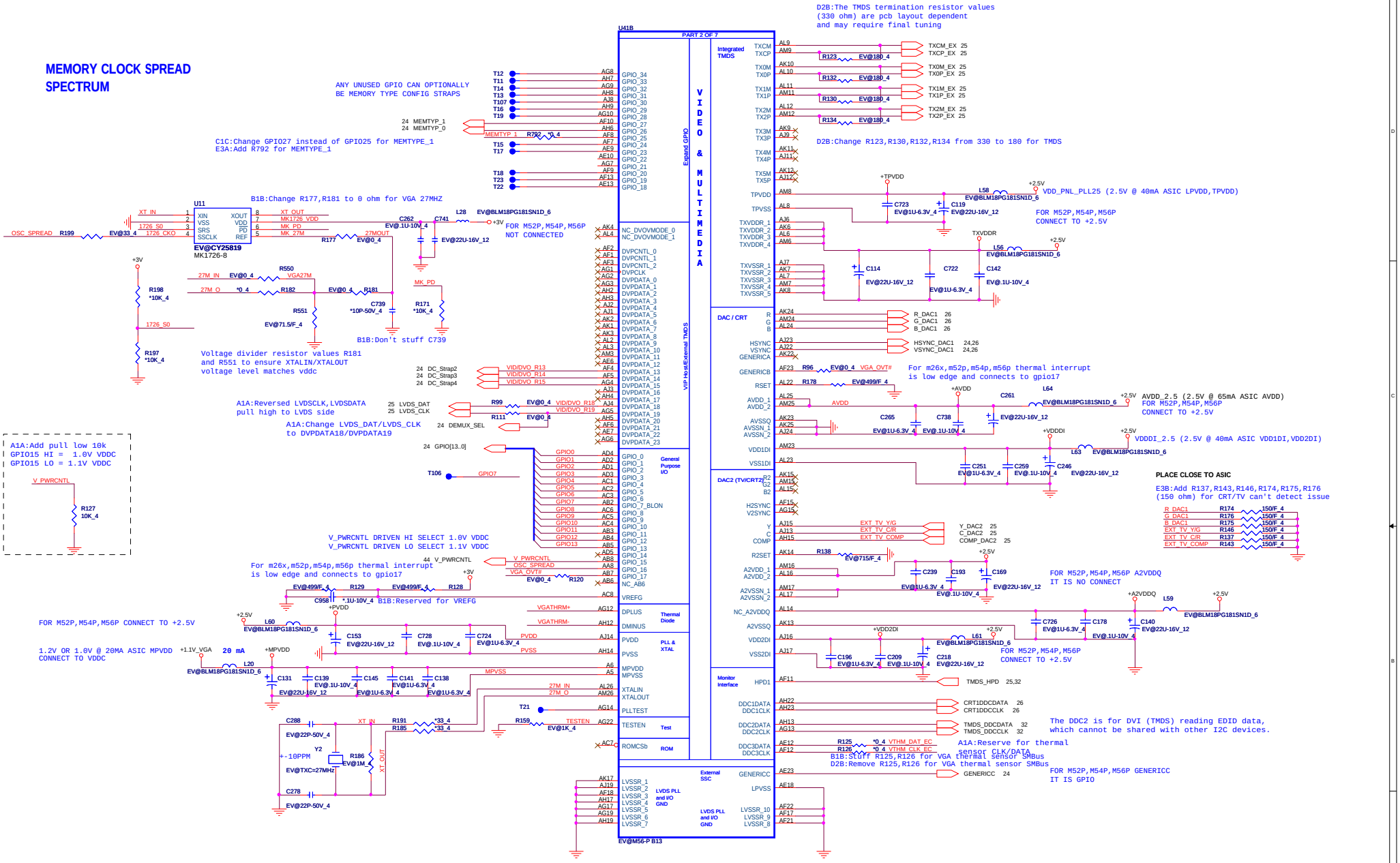
MEMORY CLOCK SPREAD SPECTRUM



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Quanta Computer Inc.

Size	Document Number	Rev
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If memory interface has to be up to 600Mhz or above, the GPU core voltage and memory I/O voltage may need to be increased to 1.2~1.3V and 2.0V

A1A:Change to VGA_MEM_IO

U41E

PART 5 OF 7

POWER

Memory I/O

I/O

Core

PCI-Express

I/O Internal

LVDS PLL, I/O

Memory I/O Clock

EV@M56-P B13

1.2V ASIC PCIE_PVDD_12 @ 100mA, PCIE_VDDR_12 @ 2000mA

FOR M52P,M54P,M56P CONNECT TO +1.2V

1.2V OR 1.0V @ 18A ASIC VDDC,VDDCI

D2B:Add R778,Q56,Q57 for VGA +3V power sequence

VDD_PNL_PLL25 (2.5V @ 40mA ASIC LPVDD,TPVDD)

GENERICD : FOR M56P IT IS A BACK BIAS REGULATOR CONTROL

U41G

PART 7 OF 7

Forward Compatibility

Control and External SSC

LVDS channel

EV@M56-P B13

Panel power(LCDVCC) control

GENERICD->FOR M56P IT IS A BACK BIAS REGULATOR CONTROL

E3A:Add R789 for G966_VIN,change source to +1.8VSUS

D2B:Add R778,R780 for +1.2V_VPCIE

PROJECT :	ZC1
Quanta Computer Inc.	
Size	
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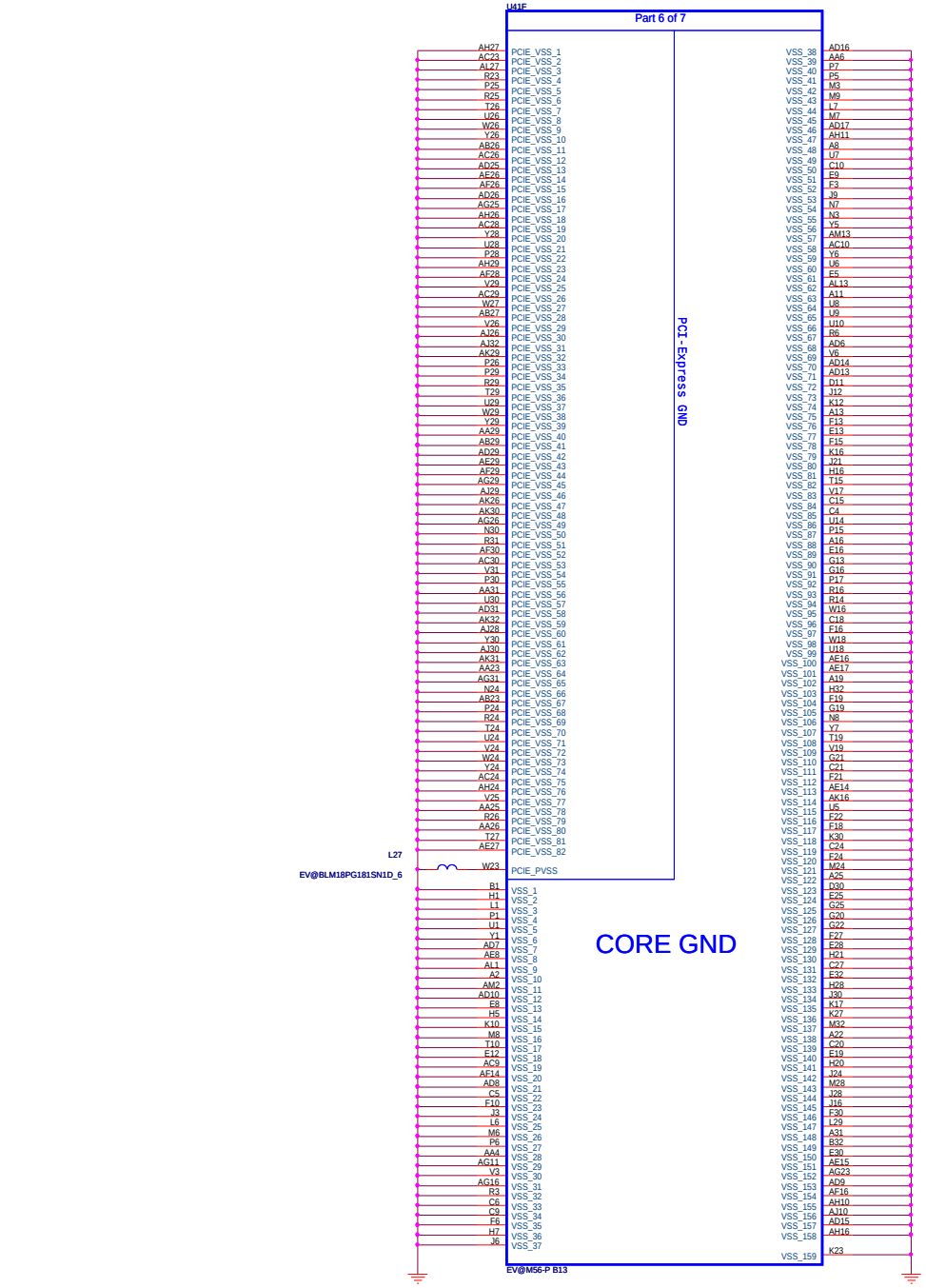

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	M56P 6 OF 7	1A

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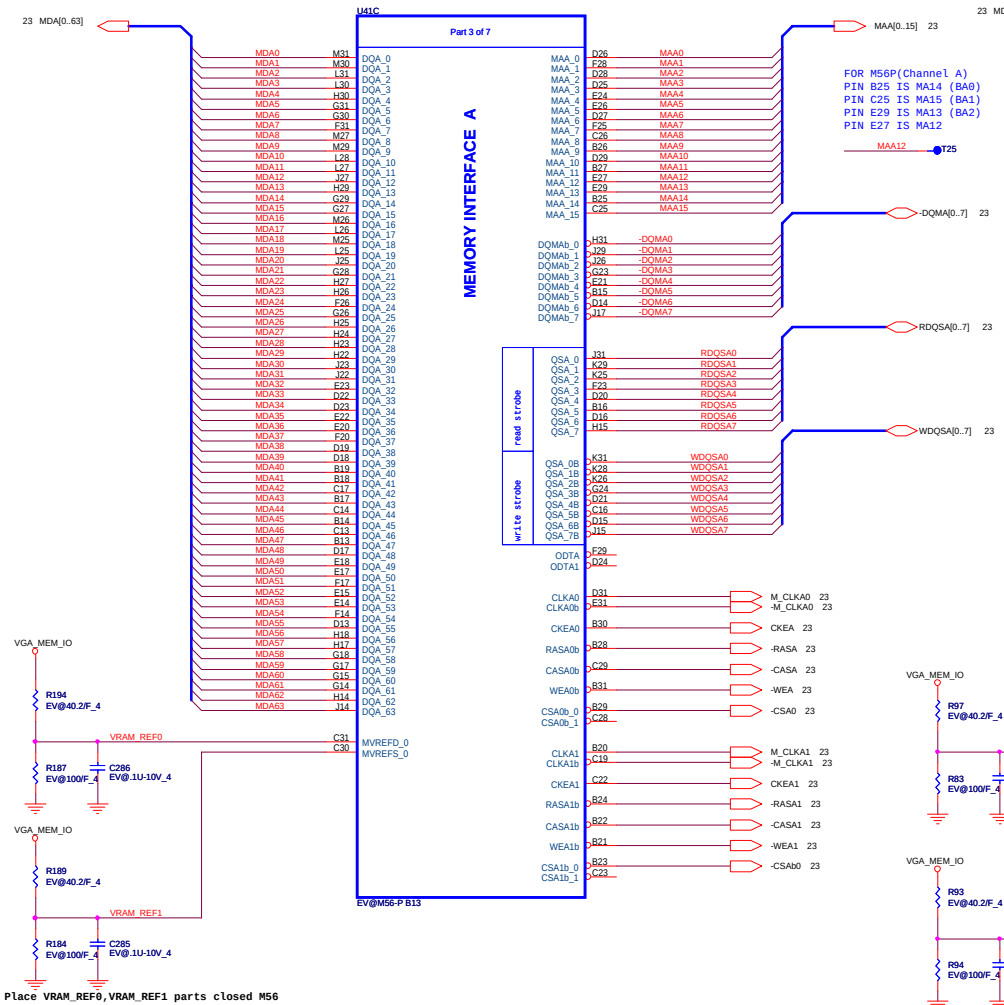
RV410 MEMORY CHANNELS A and B

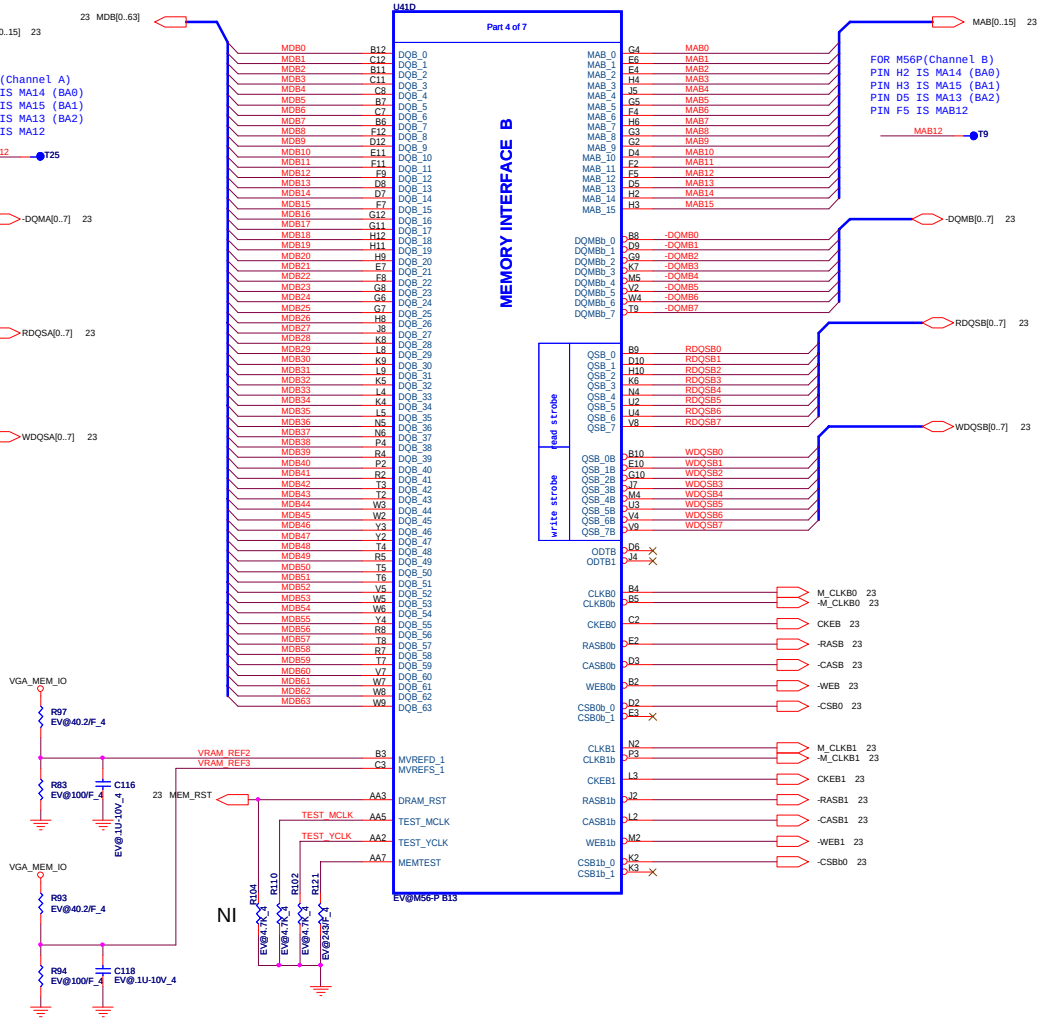
Channel A



Place VRAM_REF0,VRAM_REF1 parts closed M56

Reference voltage per channel (memory data/strobe)
MVREFD_[0:1] (0.7 * VDDR1) (for GDDR3)
MVREFS_[0:1] (0.7 * VDDR1) (for GDDR3)

Channel B



Reference voltage per channel (memory data/strobe)
MVREFD_[0:1] (0.7 * VDDR1) (for GDDR3)
MVREFS_[0:1] (0.7 * VDDR1) (for GDDR3)

PROJECT : ZC1

Quanta Computer Inc.

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	M56P 3/4 OF 7	1A

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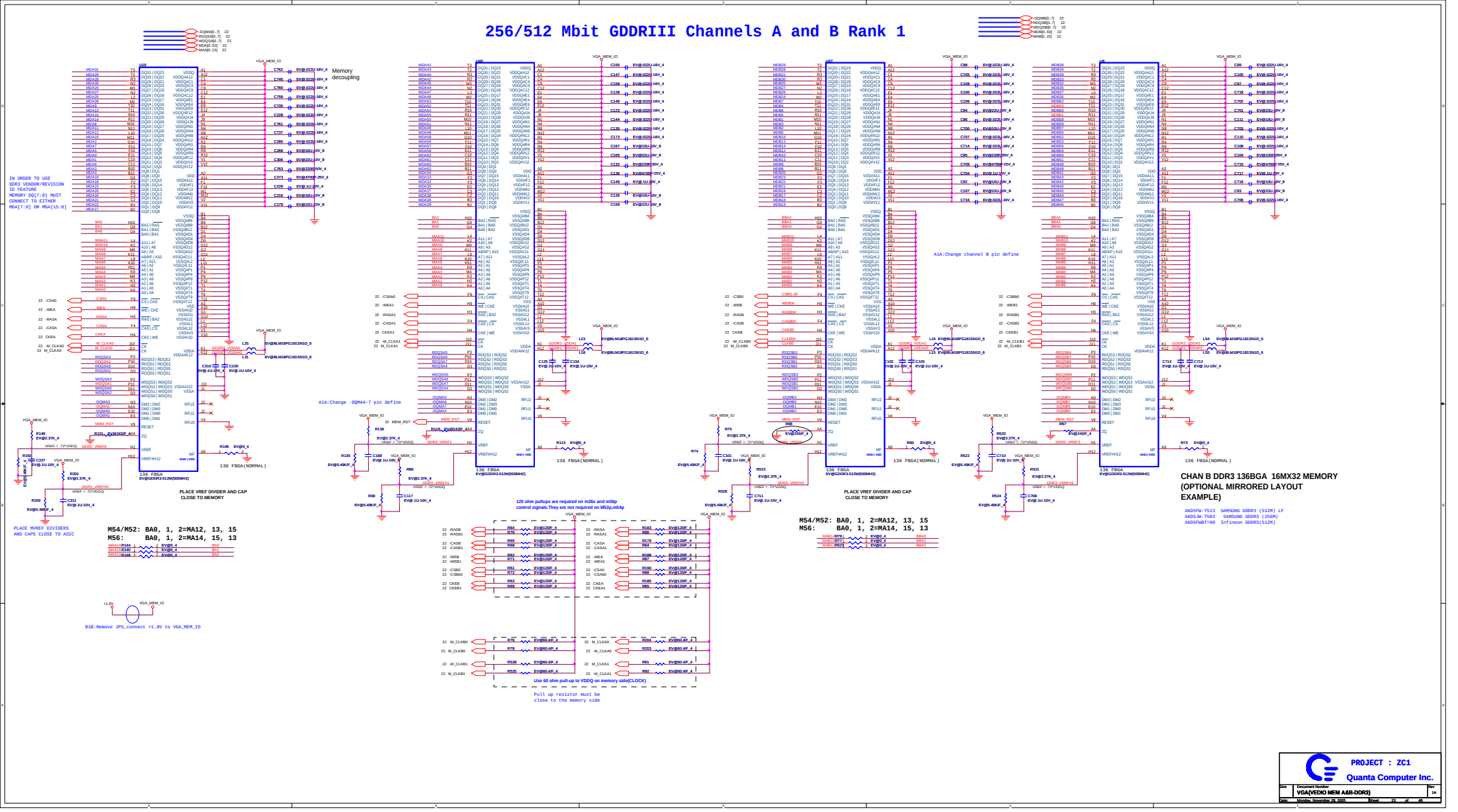
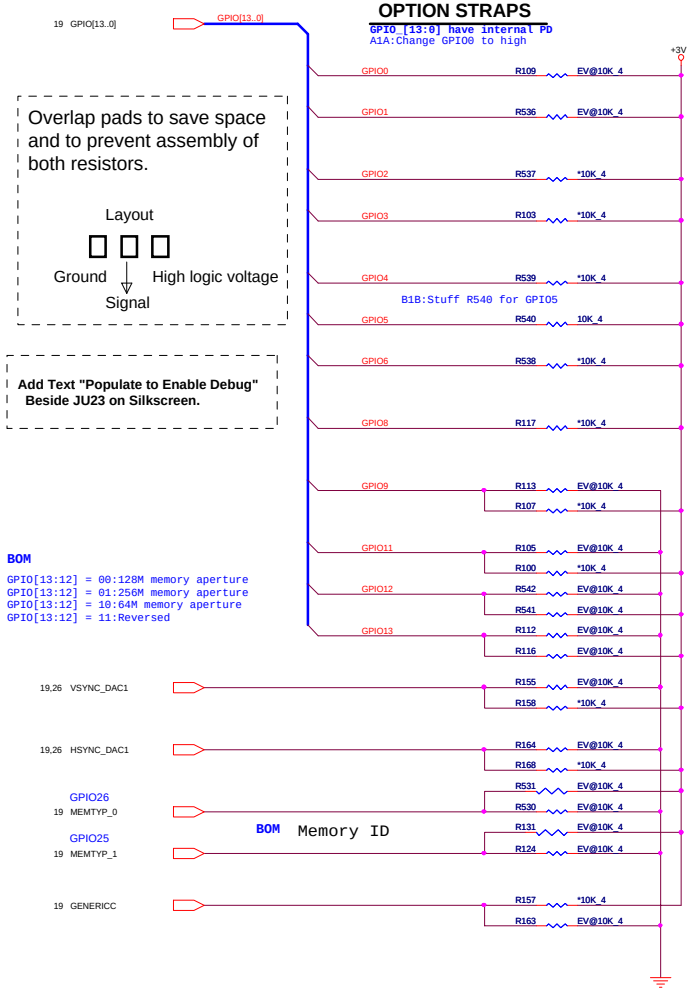
256/512 Mbit GDDRIII Channels A and B Rank 1



OPTION STRAPS

GPIO_[13:0] have internal Pd
A1A:Change GPIO0 to high



Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground → Signal

High logic voltage

Add Text "Populate to Enable Debug" Beside JU23 on Silkscreen.

BOM

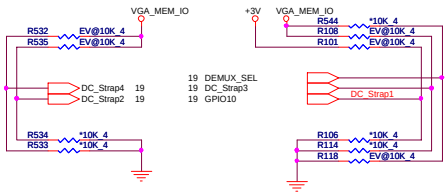
GPIO[13:12] = 00:128M memory aperture
GPIO[13:12] = 01:256M memory aperture
GPIO[13:12] = 10:64M memory aperture
GPIO[13:12] = 11:Reversed

BOM Memory ID

M56-P Strap

STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
STRAP_B_PTX_PWRS_ENB	GPIO0	TRANSMITTER POWER SAVINGS ENABLE - FULL TX OUTPUT SWING	INSTALL 10K RESISTOR
STRAP_B_PTX_DEEMPH_EN	GPIO1	TRANSMITTER DE-EMPHASIS ENABLE FOR M26X,M56P: INSTALL WITH ATI RS480,RS400,RX480, RC410,RS482 CHIPSETS DO NOT INSTALL WITH INTEL 915PM CHIPSET FOR M5X - INSTALL	TBD
RSVD	GPIO(3:2)	NO ATI FEATURE ENABLED	DO NOT INSTALL 10K RESISTORS
REVERSE LANES DEBUG ACCESS	GPIO4	NO DEBUG ACCESS (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
STRAP_FORCE_COMPLIANCE RSVD	GPIO5	sets the desired PCIE PLL bandwidth for M5x parts	DO NOT INSTALL 10K RESISTOR
COMMON MODE RANGE	GPIO6	NO ATI FEATURE ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
DEBUG ACCESS FORCE_COMPLIANCE	GPIO8	DON'T FORCE COMPLIANCE STATE(M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
ROMIDCFG(3:0) MEMORY APERTURE SIZE	GPIO(9,13:11)	IF NO ROM GPIO11(M26X) AND GPIO12,13(M52,M54,M56) SET MEMORY APERTURE SIZE 000x - No ROM, MEM_AP_SIZE=00(128MB) 001x - No ROM,MEM_AP_SIZE=01(256MB) 010x - No Rom, MEM_AP_SIZE=10(64MB) 011x - No ROM,MEM_AP_SIZE=11(Reserved) 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port deviced present. 1-No slave VIP port devices reporting presence during reset	No default
NO STRAP FUNCTION	H2SYNC, V2SYNC,GENERICC	ATI FEATURE NOT ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
	VSYNC	RSVD	
	HSYNC	RSVD	
	PCIE_TEST	RSVD	

A1A:change ROMIDCFG(3:0) to 0010



A1A:change video capture enable setting

Board Straps REV_0.3

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE(1:0)	GPIO25,26	MEMORY TYPE AND SPEED SELECT Memory connected to R420 identification for BIOS 00 - Samsung GDDR 3 memory(256Mb) 136 Ball BGA package 01 - Samsung GDDR 3 memory(512Mb) 136 Ball BGA package 10 - Infineon GDDR 3 memory(256Mb) 136 Ball BGA package 11 - Infineon GDDR 3 memory(512Mb) 136 Ball BGA package	00
DC_Strap1	GPIO(10)	Internal TMDS Enabled 0 - Disabled **1 - Enabled**	1
DC_Strap2	LCDDATA(13)	Video Capture Enabled **0 - Disabled** 1 - Enabled	1
DC_Strap3	LCDDATA(14)	HDTV out detect 0 - Detected **1 - Not detected**	1
DC_Strap4, DEMUX_SEL	LCDDATA(15,19)	Video capture enable 00 - DAC2 Off 01 - DAC2 On as CRT **10 - DAC2 On as TVOUT** 11 - DAC2 On as TVOUT and CRT	10
PAL/NTSC	LCDDATA(18)	TVO Standard Default (Resistor pull-up and switch short to GND) **0 - PAL (on board resistor pull-down and switch closed)** **1 -NTSC (on board resistor pull-up)**	1

MEMORY TYPE AND SPEED SELECT

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Quanta Computer Inc.

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	M56P OPTION STRAPS	1A

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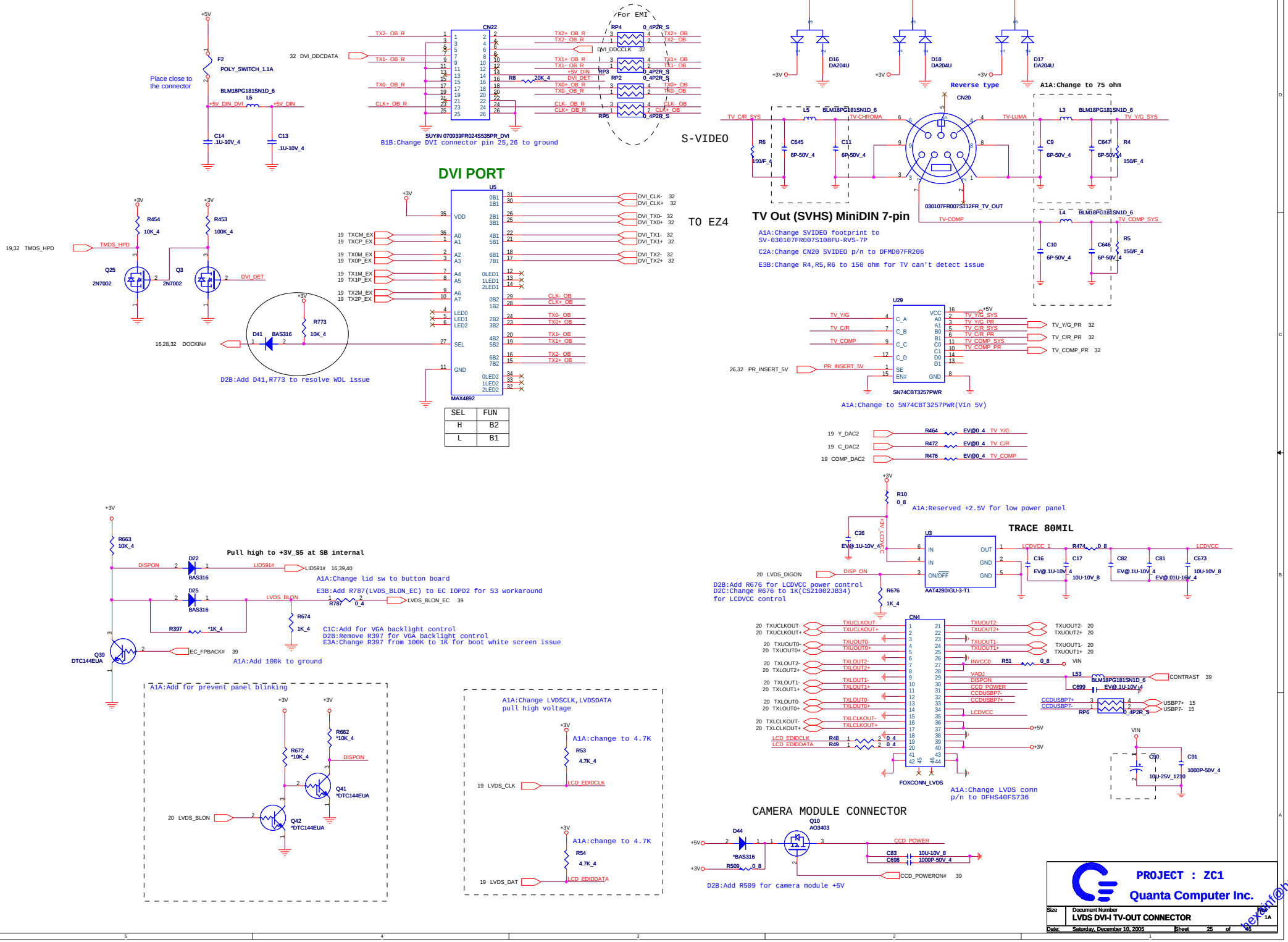
DVI-I CONNECTOR (DVI-D)



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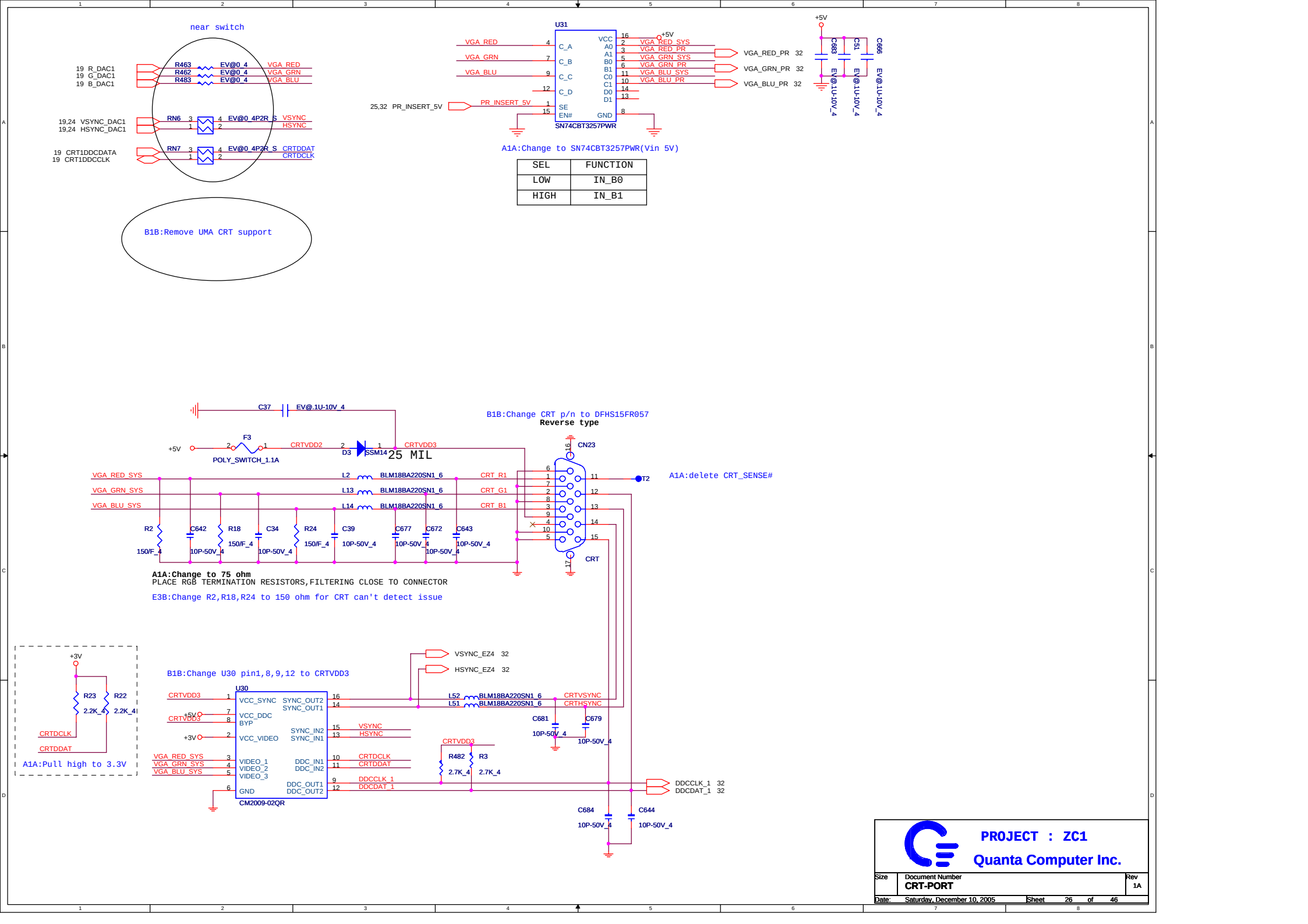

PROJECT : ZC1

Quanta Computer Inc.

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	CRT-PORT	1A

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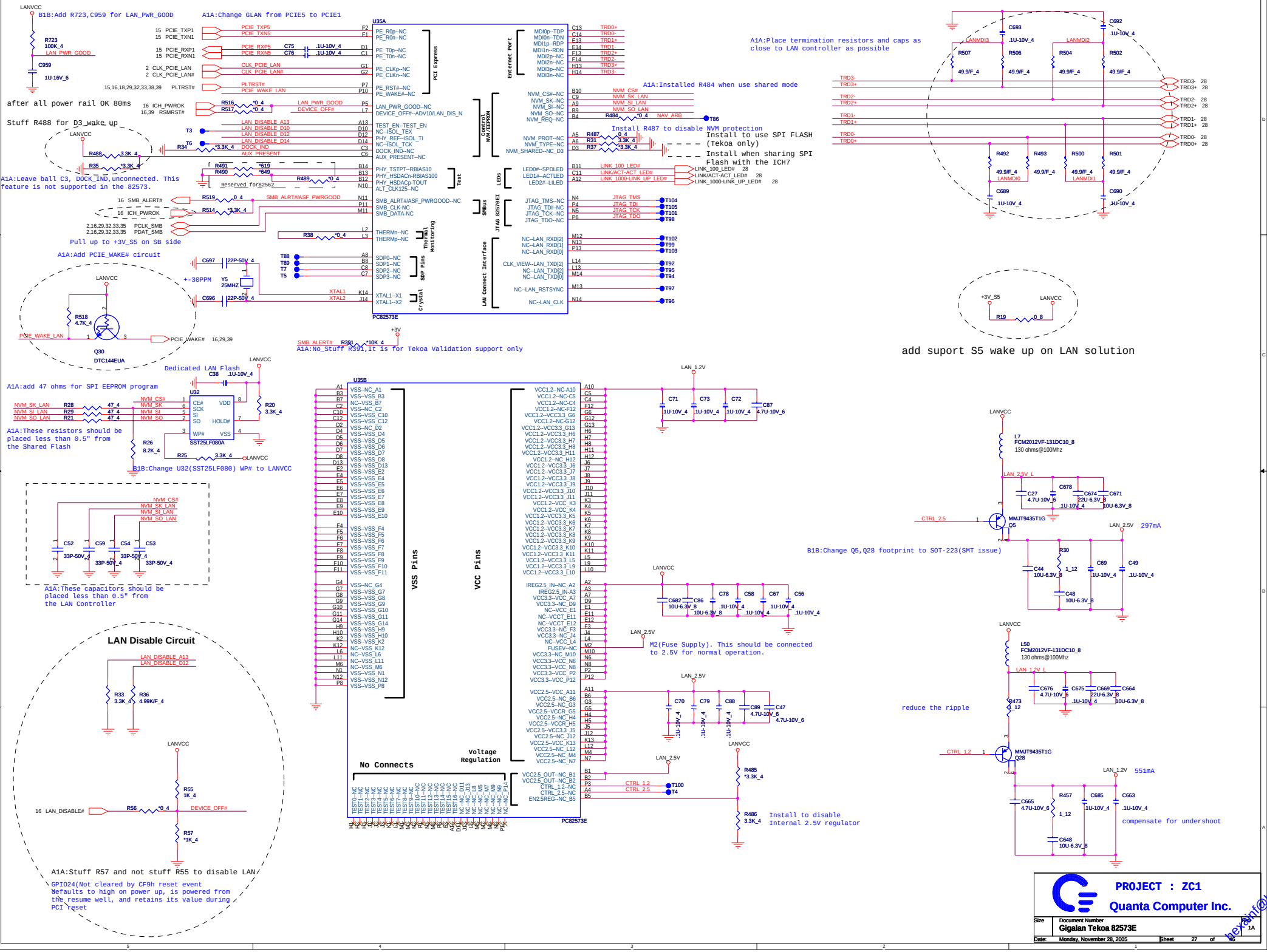
B1B:Add R723,C959 for LAN_PWR_GOOD
A1A:Change GLAN from PCIE5 to PCIE1
U35A
PCI Express
Enternet Port
Control NVM/EEPROM
Test
LEDs
SMBus
JTAG 82576EI
Thermal Monitoring
SDP Pins
Crystal
LAN Connect Interface
PC82573E
after all power rail OK 80ms
Stuff R488 for D3_wake up
A1A:Leave ball C3, DOCK_IND,unconnected. This feature is not supported in the 82573.
Pull up to +3V_S5 on SB side
A1A:Add PCIE_WAKE# circuit
Q30
DTC144EUA
A1A:No_Stuff R391,It is for Tekoa Validation support only
A1A:Installed R484 when use shared mode
Install R487 to disable NVM protection
Install to use SPI FLASH (Tekoa only)
Install when sharing SPI Flash with the ICH7
A1A:Place termination resistors and caps as close to LAN controller as possible
add suport S5 wake up on LAN solution
Dedicated LAN Flash
A1A:add 47 ohms for SPI EEPROM program
A1A:These resistors should be placed less than 0.5" from the Shared Flash
B1B:Change U32(SST25LF080) WP# to LANVCC
A1A:These capacitors should be placed less than 0.5" from the LAN Controller
LAN Disable Circuit
A1A:Stuff R57 and not stuff R55 to disable LAN
GPIO24(Not cleared by CF9h reset event Defaults to high on power up, is powered from the resume well, and retains its value during PCI reset
U35B
VSS Pins
VCC Pins
Voltage Regulation
No Connects
PC82573E
M2(Fuse Supply). This should be connected to 2.5V for normal operation.
Install to disable Internal 2.5V regulator
B1B:Change Q5,Q28 footprint to SOT-223(SMT issue)
reduce the ripple
compensate for undershoot
PROJECT : ZC1
Quanta Computer Inc.
Gigalan Tekoa 82573E
Monday, November 28, 2005
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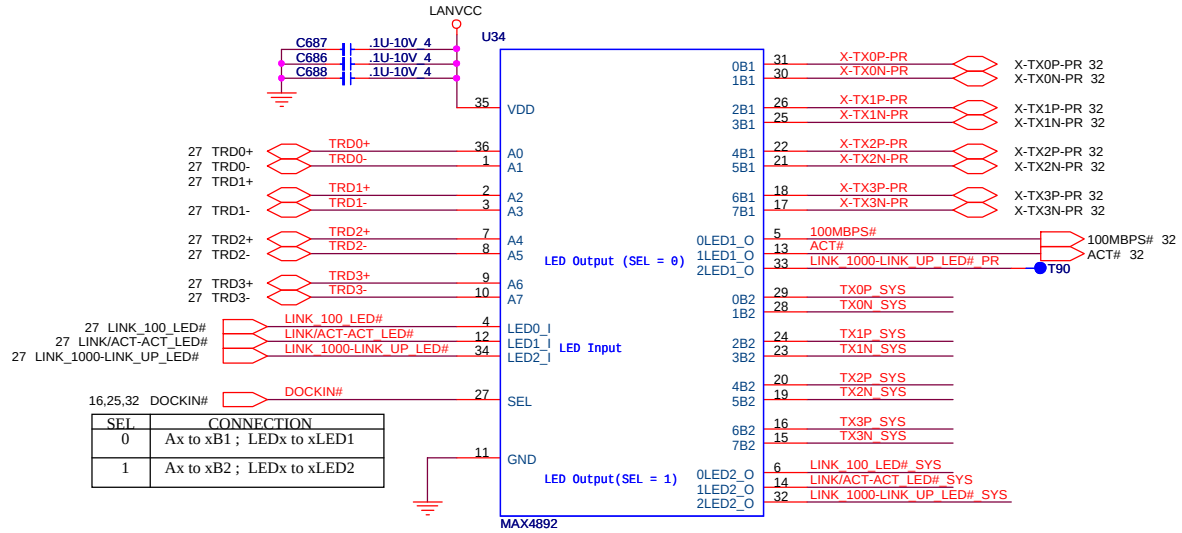
bekenf@hotmail.com

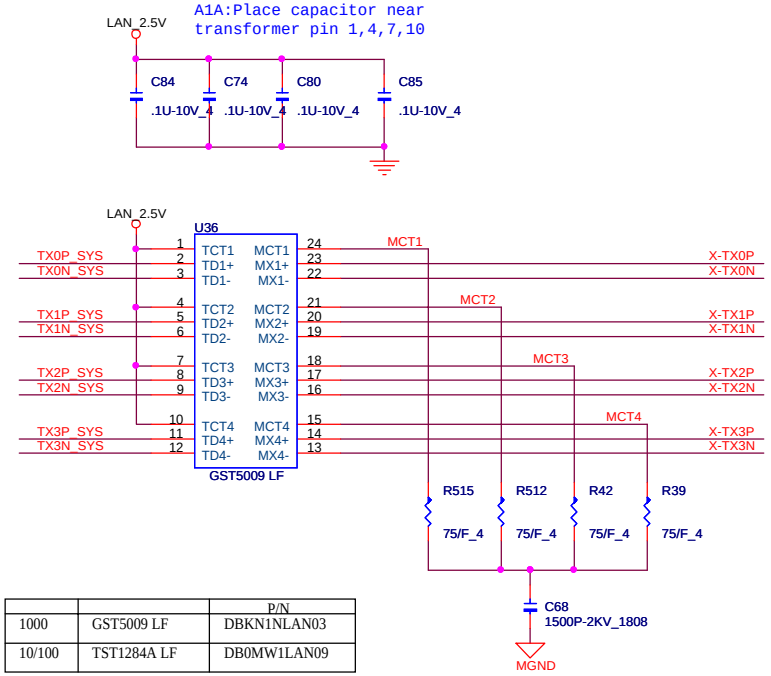


SEL	CONNECTION
0	Ax to xB1 ; LEDx to xLED1
1	Ax to xB2 ; LEDx to xLED2

LED0 Input
0LED1 Output. Connects LED0 to 0LED1 when SEL = 0.
0LED2 Output. Connects LED0 to 0LED2 when SEL = 1.

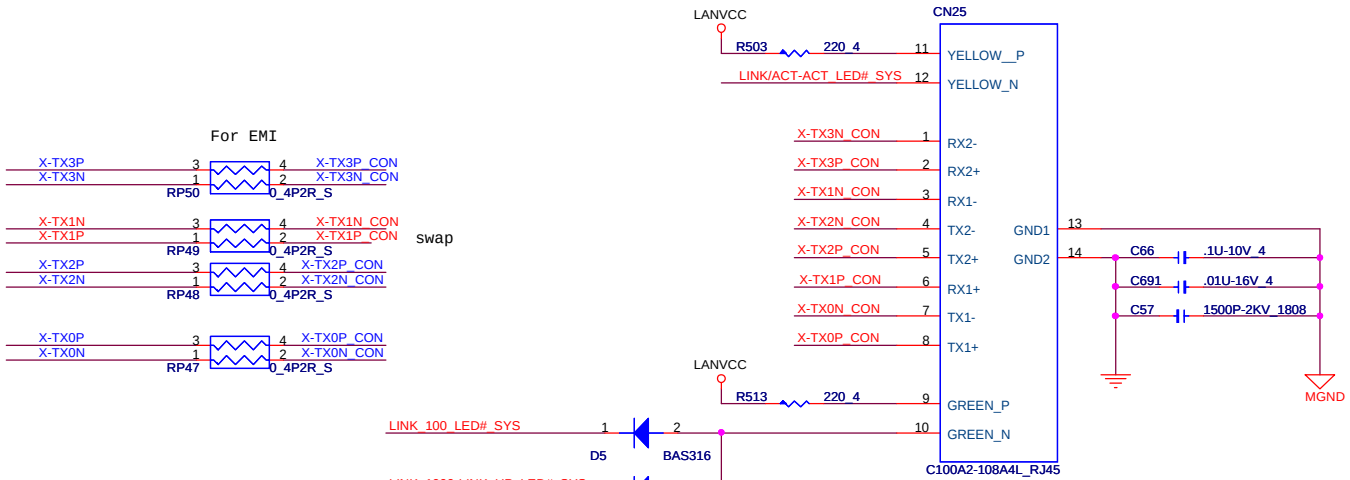
B1B:Change MAX4892 pin define

A1A:Place capacitor near transformer pin 1,4,7,10



		P/N
1000	GST5009 LF	DBKN1NLAN03
10/100	TST1284A LF	DB0MW1LAN09

A1A:Change RJ45 CONN to C100A2-108A4L
A1A:Change RJ45 TX,RX pin define



A1A:Add diode for 10/100M
& 1000M led control

LED1	A1(+) A2(-)	ACT (Tx/Rx)	YELLOW BLINKING
LED2	B1(+) B2(-)	LINK 10/100/1000	GREEN

PROJECT : ZC1

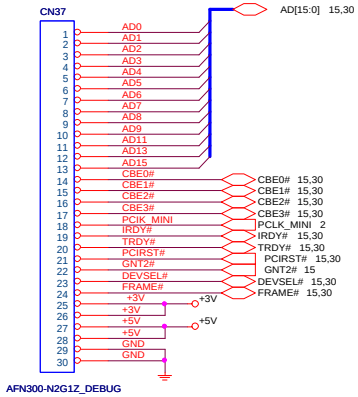
Quanta Computer Inc.

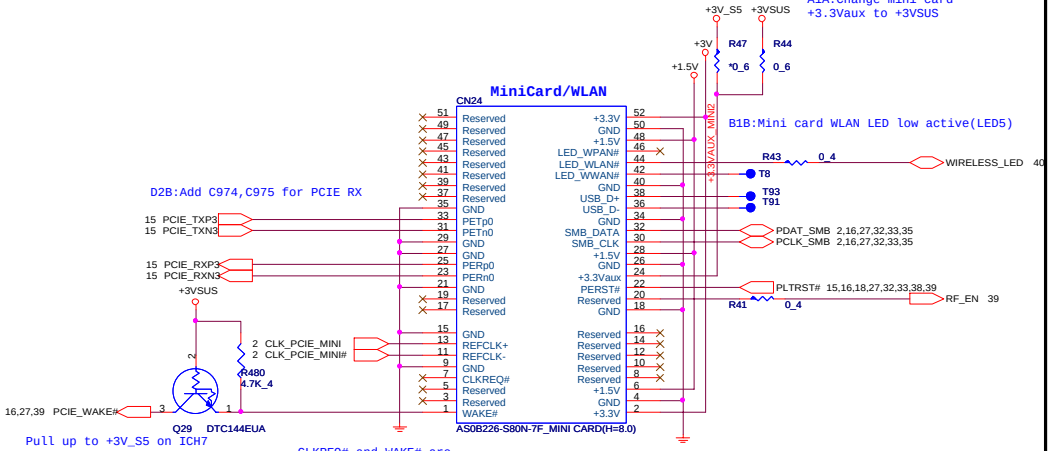
Size	Document Number	Rev
	TRANSFORMER/RJ45	A

Date: Monday, November 28, 2005 Sheet 28 of 46

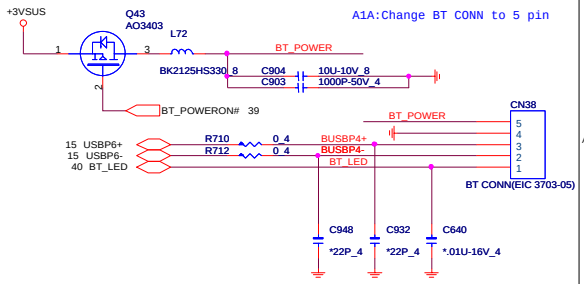
Debug card interface

BOT contact

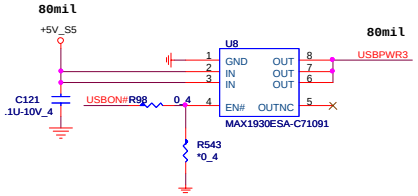


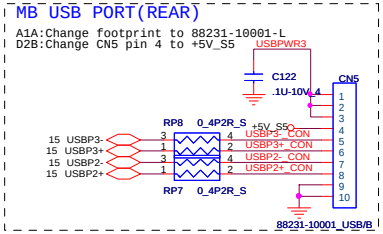


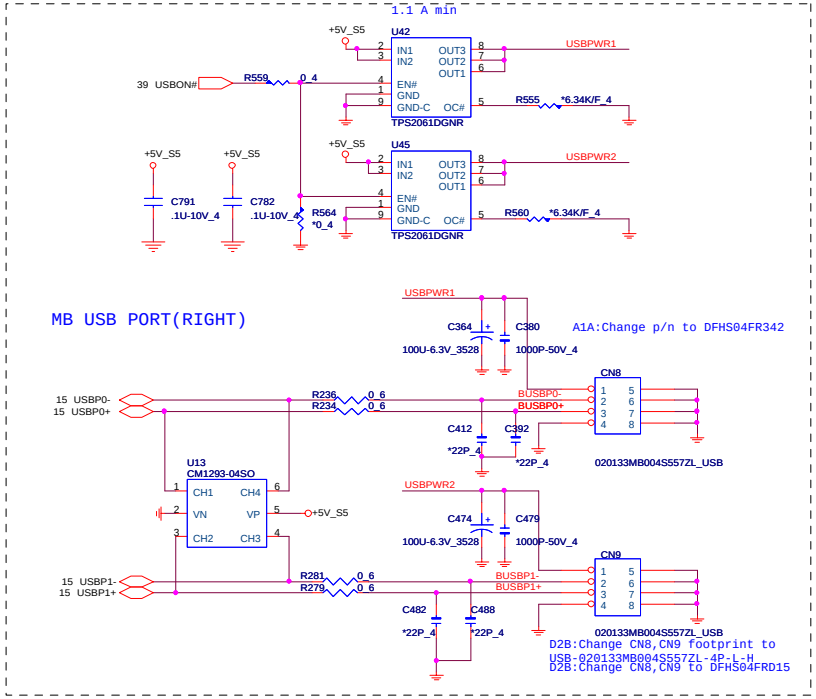
BLUETOOTH MODULE CONNECTOR



A1A:In adapter mode, should be powered during S0~S5.
In battery only mode, should be powered during S0 and S3, and not powered during S5





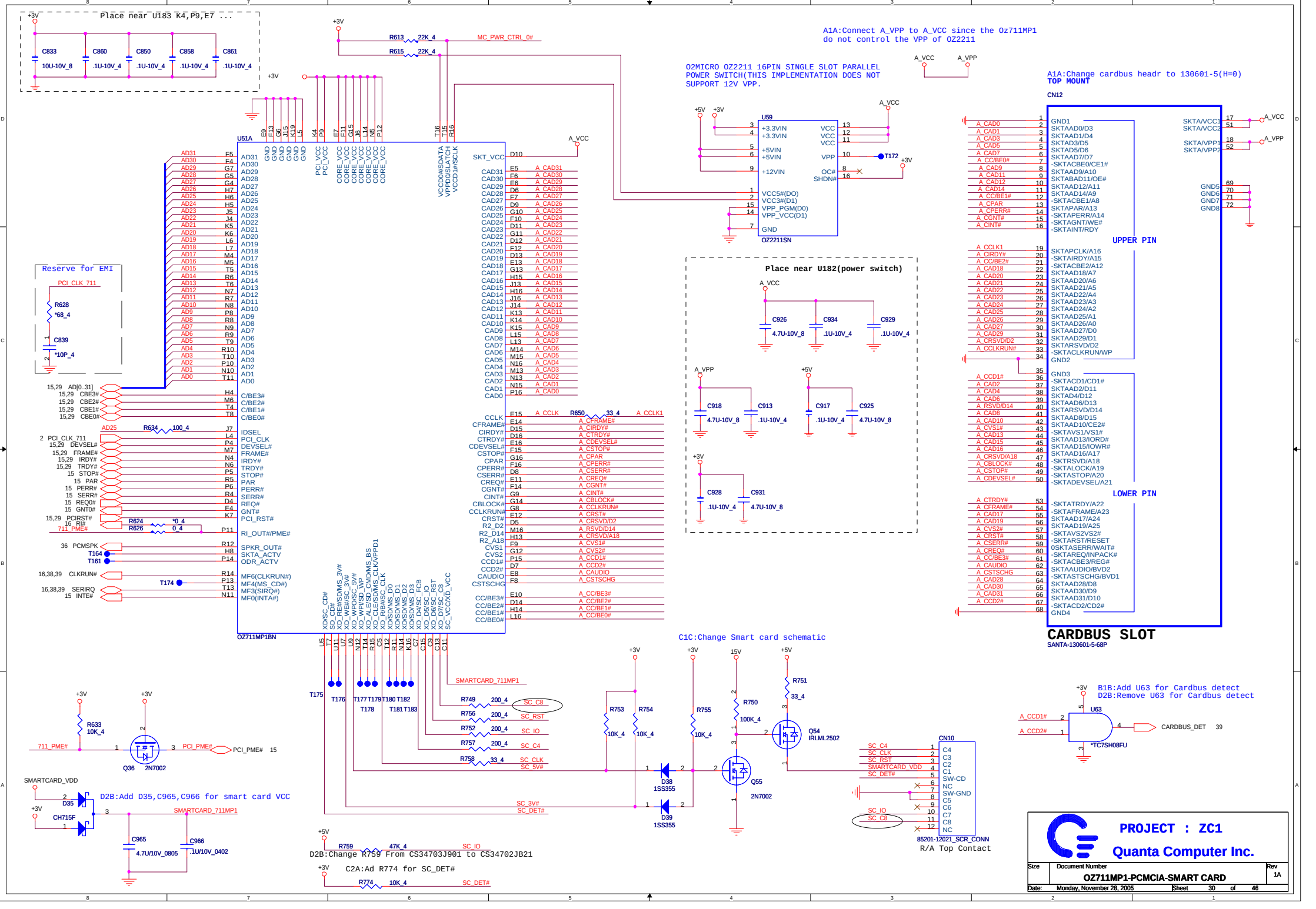


PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	DEBUG CARD&PCI-E card&USB	1A
Date: Monday, November 28, 2005	Sheet 29 of 46	

hexaint@hotmail.com


Place near U183 K4,P9,E7 ...
C833 10U-10V_8
C860 .1U-10V_4
C850 .1U-10V_4
C858 .1U-10V_4
C861 .1U-10V_4
R613 22K_4
R615 22K_4
MC_PWR_CTRL_0#
A1A:Connect A_VPP to A_VCC since the Oz711MP1 do not control the VPP of OZ2211
O2MICRO OZ2211 16PIN SINGLE SLOT PARALLEL POWER SWITCH(THIS IMPLEMENTATION DOES NOT SUPPORT 12V VPP.
U59
OZ2211SN
A1A:Change cardbus headr to 130601-5(H=0)
TOP MOUNT
CN12
UPPER PIN
LOWER PIN
CARDBUS SLOT
SANTA-130601-5-68P
U51A
OZ711MP1BN
Reserve for EMI
PCI_CLK_711
R628 *68_4
C839 *10P_4
Place near U182(power switch)
C926 4.7U-10V_8
C934 .1U-10V_4
C929 .1U-10V_4
C918 4.7U-10V_8
C913 .1U-10V_4
C917 .1U-10V_4
C925 4.7U-10V_8
C928 .1U-10V_4
C931 4.7U-10V_8
R634 100_4
R624 *0_4
R626 0_4
R650 33_4
C1C:Change Smart card schematic
SMARTCARD_711MP1
R633 10K_4
Q36 2N7002
D2B:Add D35,C965,C966 for smart card VCC
D35 CH715F
C965 4.7U/10V_0805
C966 .1U/10V_0402
D38 1SS355
D39 1SS355
Q55 2N7002
Q54 IRLML2502
R751 33_4
CN10
85201-12021_SCR_CONN
R/A Top Contact
B1B:Add U63 for Cardbus detect
D2B:Remove U63 for Cardbus detect
U63 *TC7SH08FU
CARDBUS_DET
D2B:Change R759 From CS34703J901 to CS34702JB21
C2A:Ad R774 from SC_DET#
R759 47K_4
R774 10K_4
PROJECT : ZC1
Quanta Computer Inc.
Size
Document Number
OZ711MP1-PCMCIA-SMART CARD
Rev 1A
Date: Monday, November 28, 2005
Sheet 30 of 46

A1A:1394 function of OZ711MP1 do not used the EEPROM , and Oz711MP1 put the GUID in PCI register , So , 24LC02BT can be remove

A1A:Change the C1885 filter Cap value from 270 pf to 820 pf

A1A:Change1394 footprint to 1394-020204fr004s502zx-c-4p-v

B1B:Change pin 7,8 to GND

B1B:Change 1394 p/n to DFHS04FS578

E3A:Change 1394 footprint to 1394-020204fr004s109zl-4p-v8

5pF attached to SD_D0 and GND for 48M compatibility issue

External xD resistors

Group 1 and 2 not populated:
Firmware in Internal ROM
No unique serial number

Group 2 populated:
Firmware in External FLASH
Unique serial number and configuration in FLASH

Check GPIO Pin & Det

D2B:Connect CN14 pin 4,12,22,23 to GND

6 IN1 CARD READER (MS,MS pro,SD, MMC,xD,SDIO)

Group 1 populated:
Firmware in Internal ROM
Unique serial number and configuration in EEPROM

C2B:Remove U49,C867,R361

D2B:Change C641 to 1M_4(CS51002JB21)

D2B:Change C845 to 1M_4(CS51002JB21)

C2B:Stuff U16,R368

E3A:Change U16 to AR0ZC1C1009

Check USB2.0 Power

Place C567 at pin 100, C542 at pin 108, and C524 at pin 89.

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	OZ711MP1-IEEE1394-SMART CARD	1A

Date: Wednesday, November 30, 2005 Sheet 31 of 46

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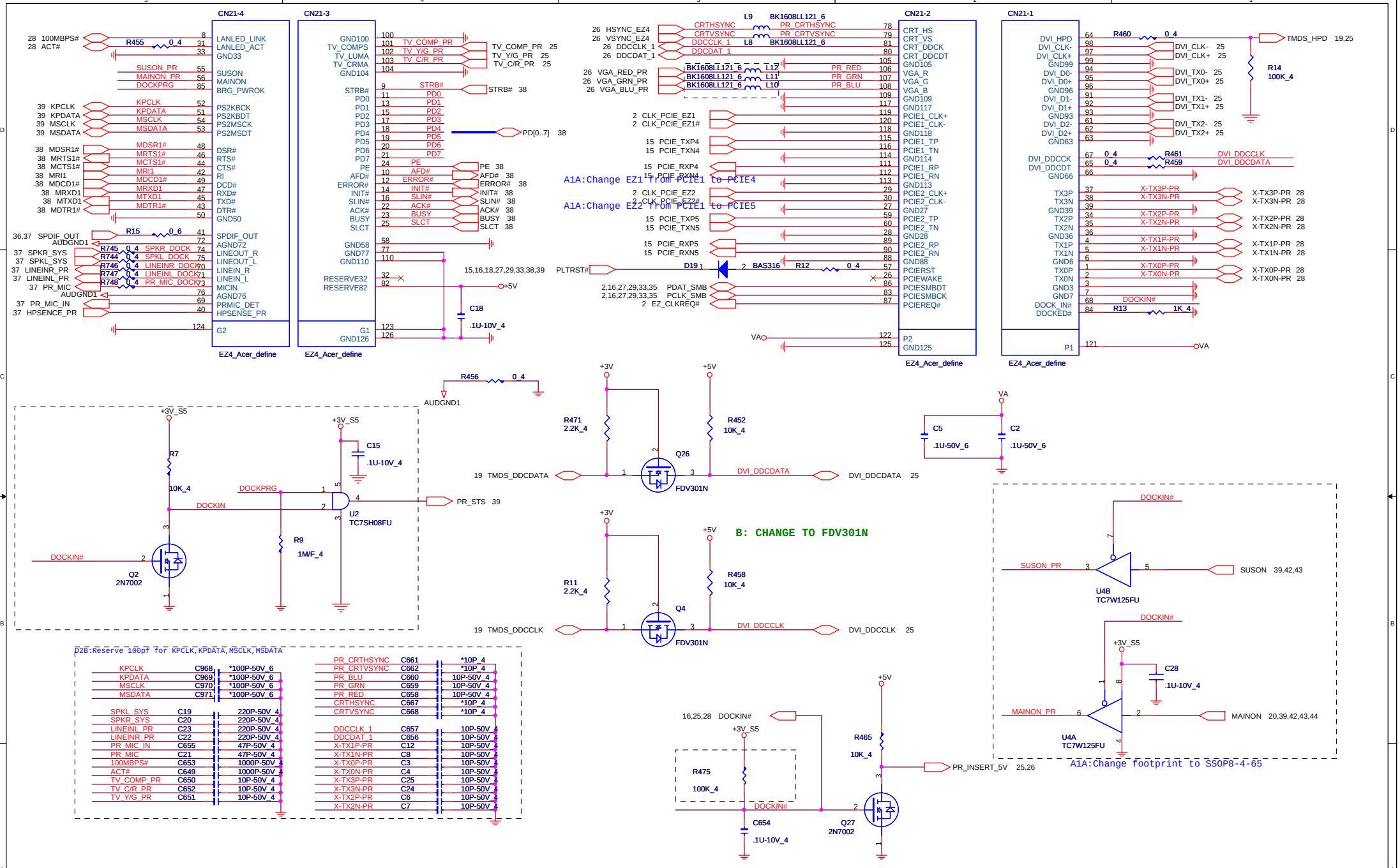
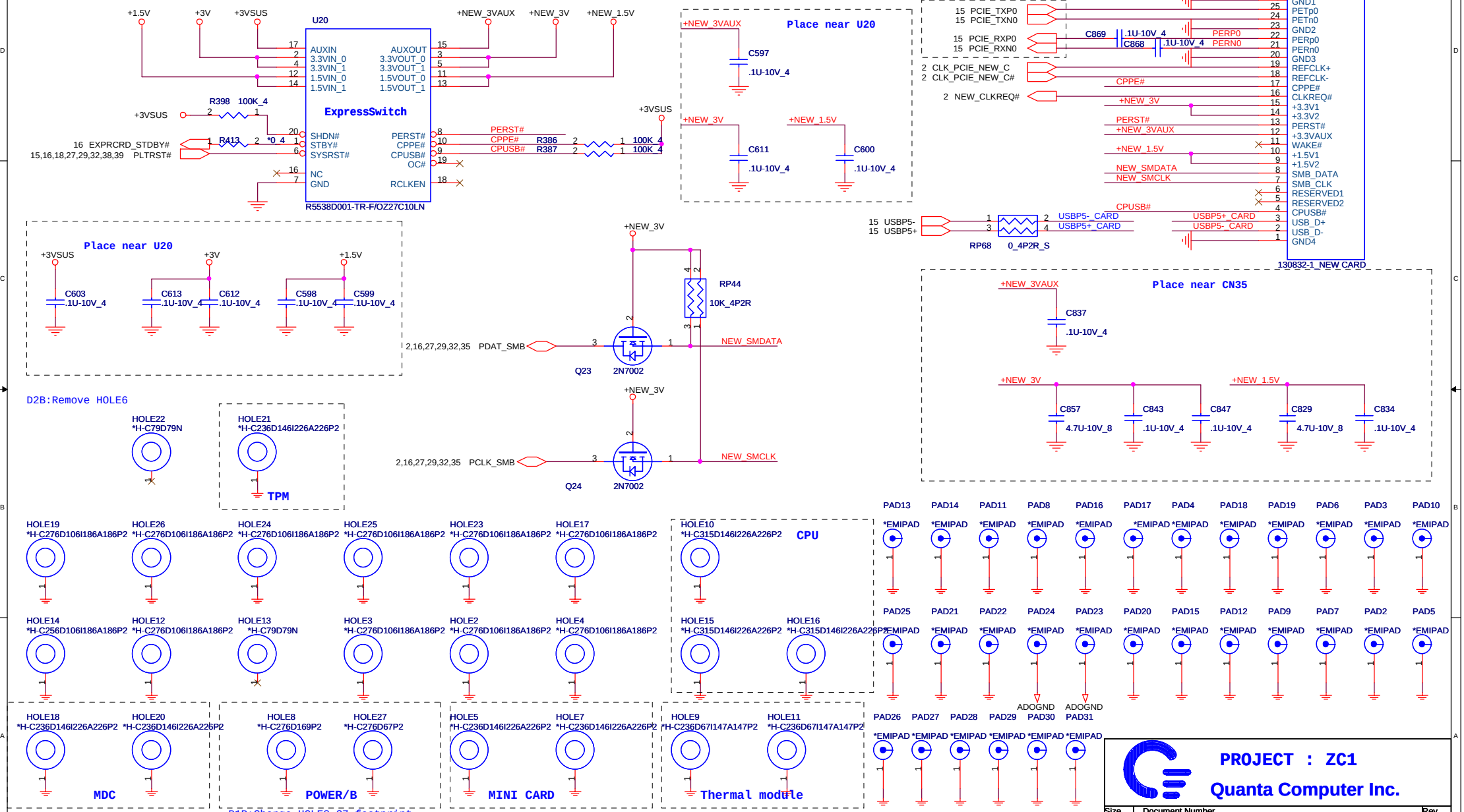

CN21-4
CN21-3
CN21-2
CN21-1
EZ4_Acer_define
A1A:Change EZ1 from PCIE1 to PCIE4
A1A:Change EZ2 from PCIE1 to PCIE5
B: CHANGE TO FDV301N
D26:Reserve 100pf for KPCLK,KPDATA,MSCLK,MSDATA
A1A:Change footprint to SSOP8-4-65
PROJECT : ZC1
Quanta Computer Inc.
Size
Document Number
EZ4 CONN
Rev
1A
Date: Tuesday, December 06, 2005
Sheet 32 of 46

+NEW_1.5V Max. 650mA, Average 500mA.
+NEW_3V Max. 1300mA, Average 1000mA.

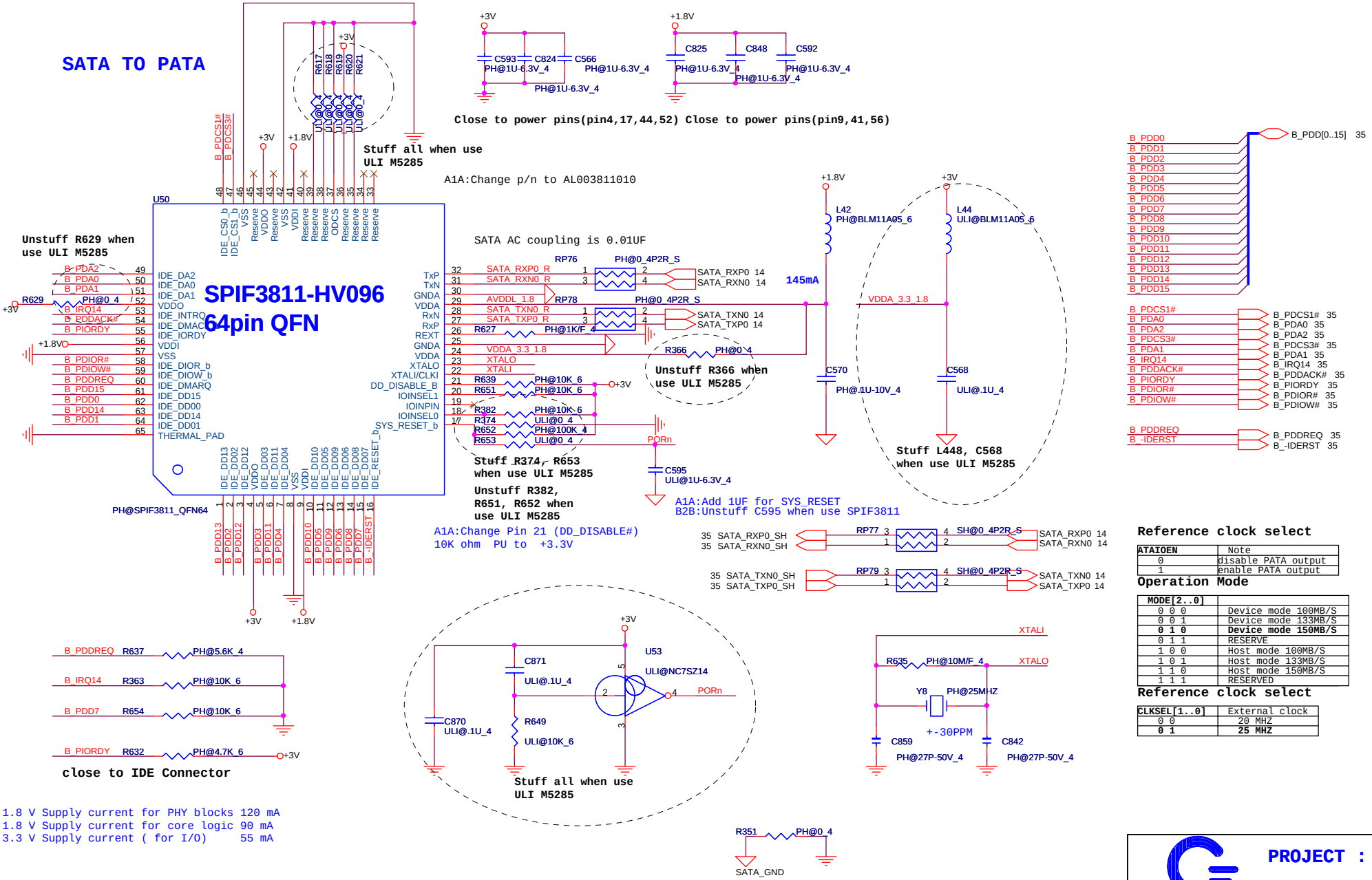
A1A:Change New card power sw to Oz27c10

A1A:Change New card to small type(130832-1)



hexainf@hotmail.com

SATA TO PATA



Reference clock select

ATAIOEN	Note
0	disable PATA output
1	enable PATA output

Operation Mode

MODE[2..0]	
0 0 0	Device mode 100MB/S
0 0 1	Device mode 133MB/S
0 1 0	**Device mode 150MB/S**
0 1 1	RESERVE
1 0 0	Host mode 100MB/S
1 0 1	Host mode 133MB/S
1 1 0	Host mode 150MB/S
1 1 1	RESERVED

Reference clock select

CLKSEL[1..0]	External clock
0 0	20 MHZ
0 1	**25 MHZ**

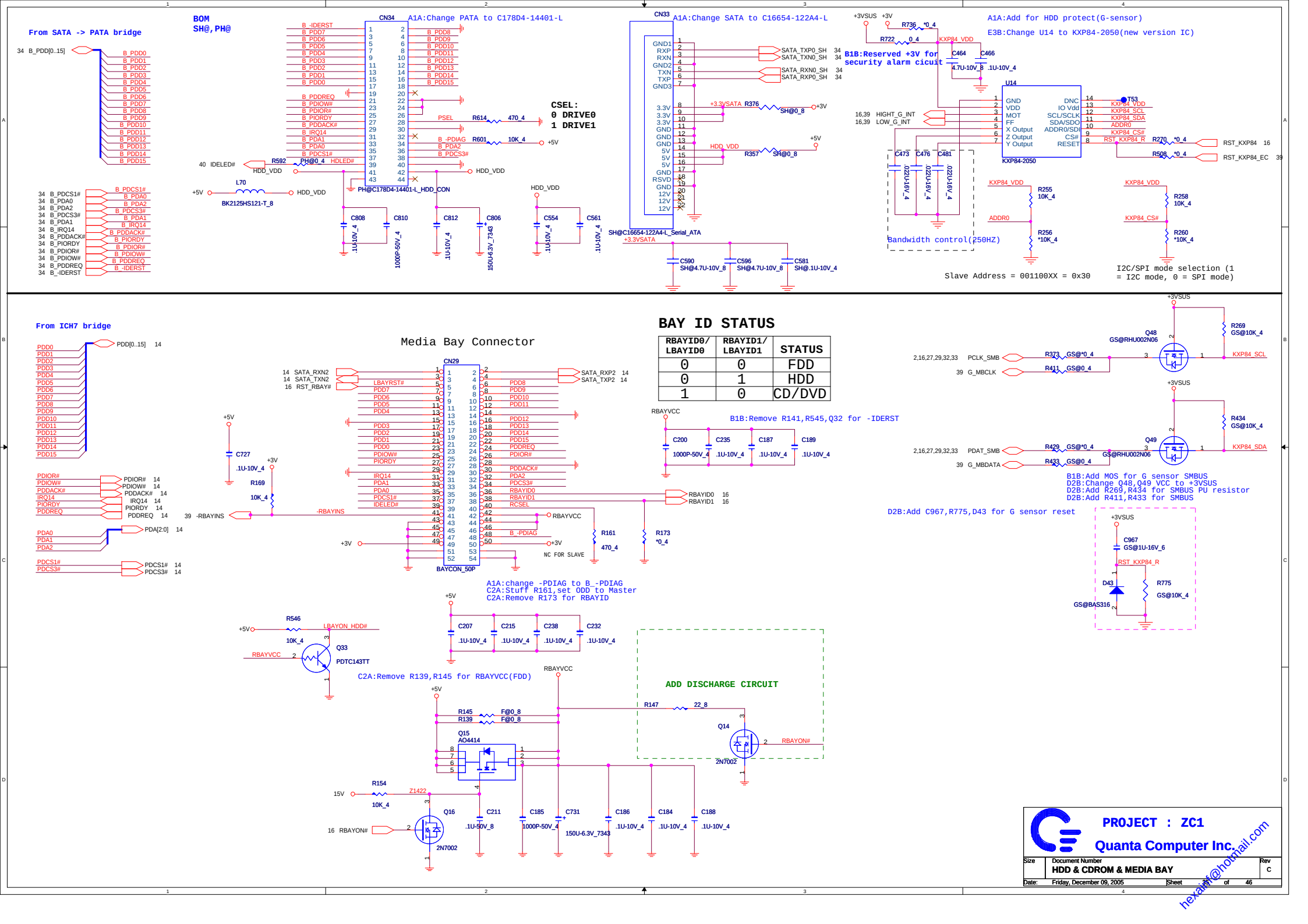
1.8 V Supply current for PHY blocks 120 mA
1.8 V Supply current for core logic 90 mA
3.3 V Supply current (for I/O) 55 mA

PROJECT : ZC1

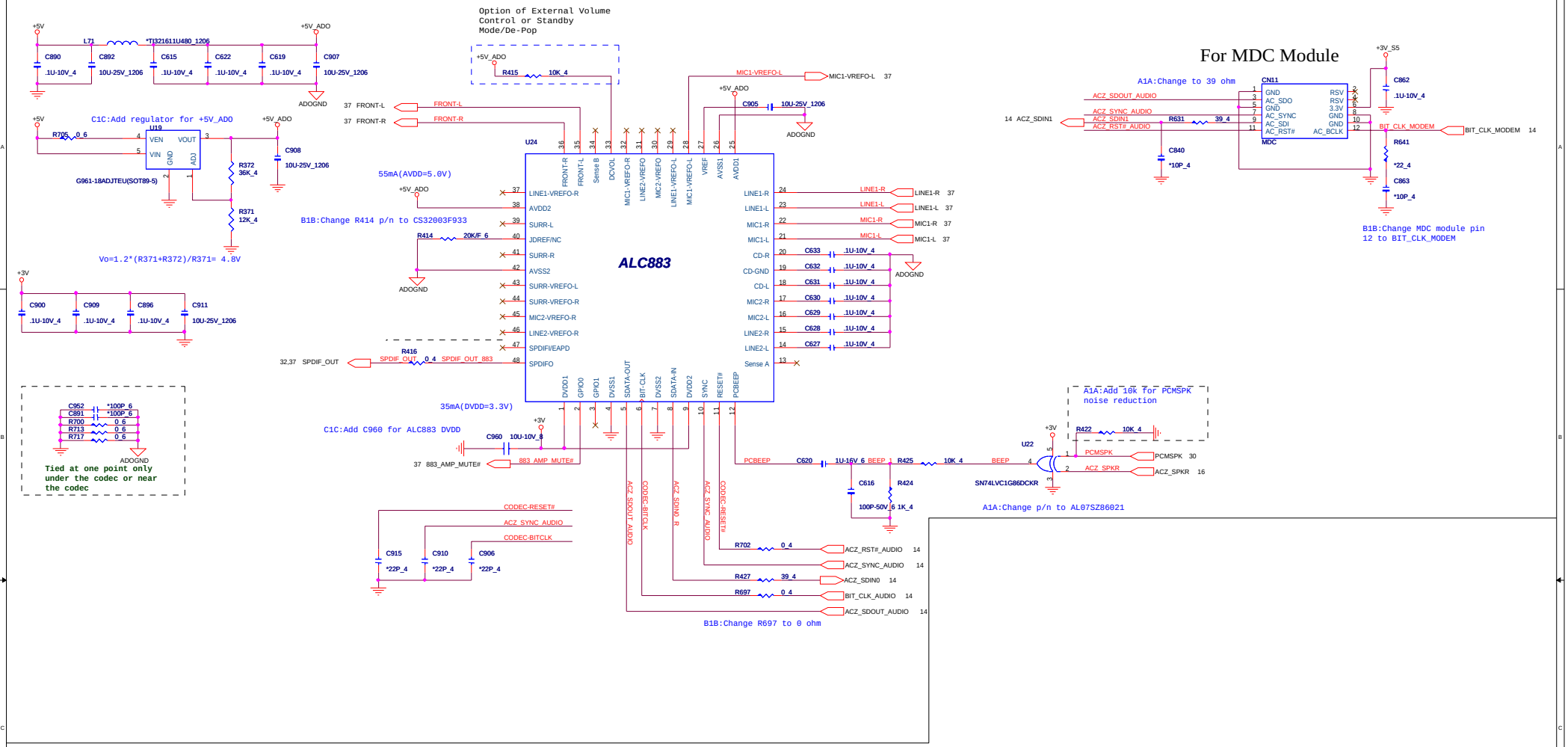
Quanta Computer Inc.

Size	Document Number	Rev
	SATA/PATA	A

Date: Monday, November 28, 2005 Sheet 34 of 46



RBAYID0/ LBAYID0	RBAYID1/ LBAYID1	STATUS
0	0	FDD
0	1	HDD
1	0	CD/DVD



PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	ALC883 & MDC	1A

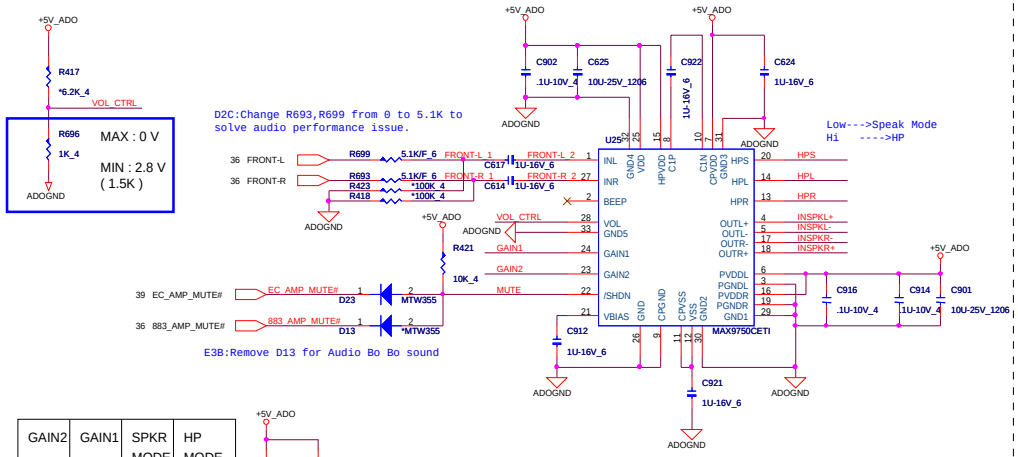
Date: Tuesday, December 06, 2005 Sheet 36 of 46

Audio amplifier

A1A:Change audio amplifier to MAX9750
A1A:Change footprint to tqfn28-5x5-5-33p

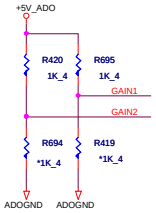
D2C:Change R693,R699 from 0 to 5.1K to solve audio performance issue.

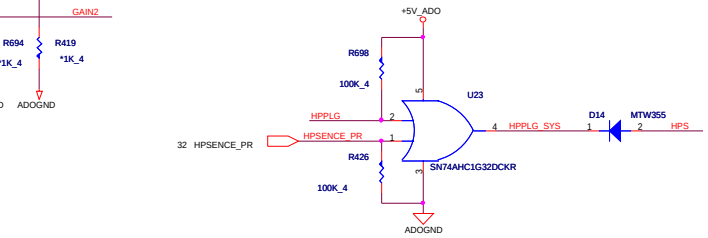
Low--->Speak Mode
Hi ---->HP



E3B:Remove D13 for Audio Bo Bo sound

GAIN2	GAIN1	SPKR MODE	HP MODE
0	0	6	0
0	1	7.5	
1	0	9	3
1	1	10.5	



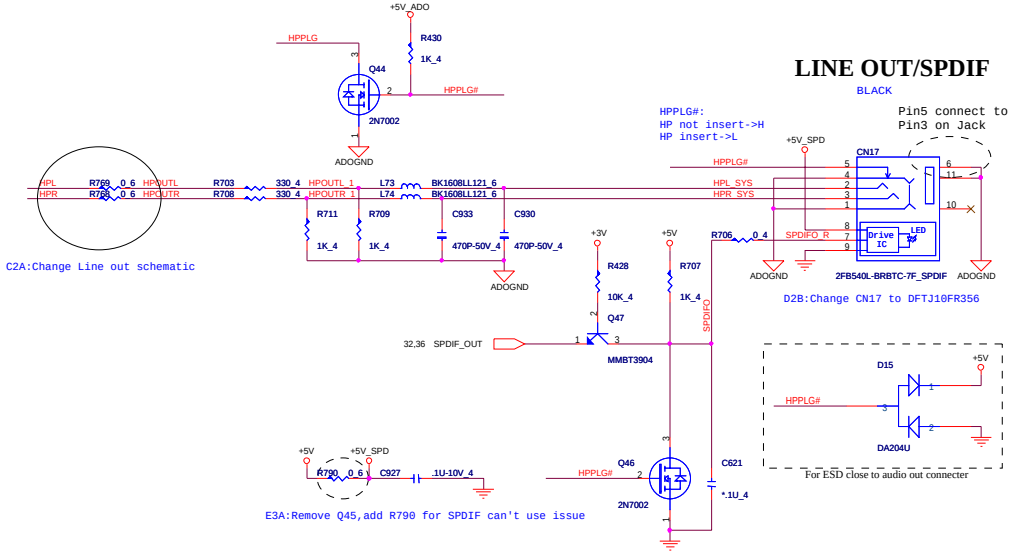


LINE OUT/SPDIF

BLACK

HPPLG#:
HP not insert->H
HP insert->L

Pin5 connect to Pin3 on Jack



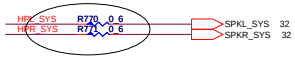
C2A:Change Line out schematic

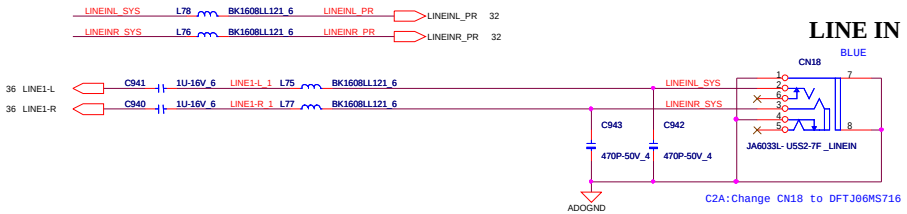
D2B:Change CN17 to DFTJ10FR356

E3A:Remove Q45,add R790 for SPDIF can't use issue

For ESD close to audio out connecter

C2A:Change Line out schematic





LINE IN

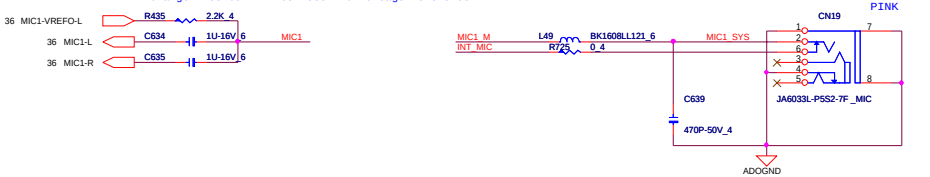
BLUE

C2A:Change CN18 to DFTJ06MS716

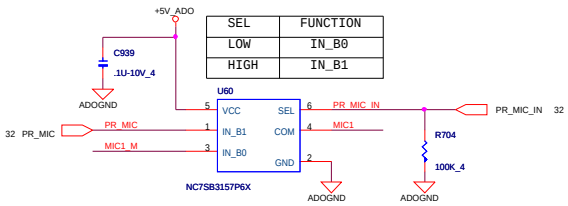
MIC

PINK

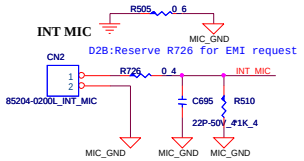
D2B:Change R435 to 2.2K to meet MIC voltage reference



C2A:Change CN19 to DFTJ06MS724

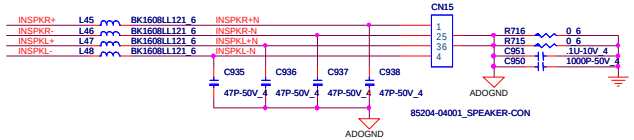


SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1



D2B:Reserve R726 for EMI request

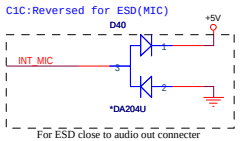
SPEAKER CONNECTOR



A1A:Change Speaker conn footprint

B1B:Change speaker p/n to DFHD04MR701

C1C:Reversed for ESD(MIC)



For ESD close to audio out connecter

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	AUDIO AMP(MAX9750) / JACK	1A

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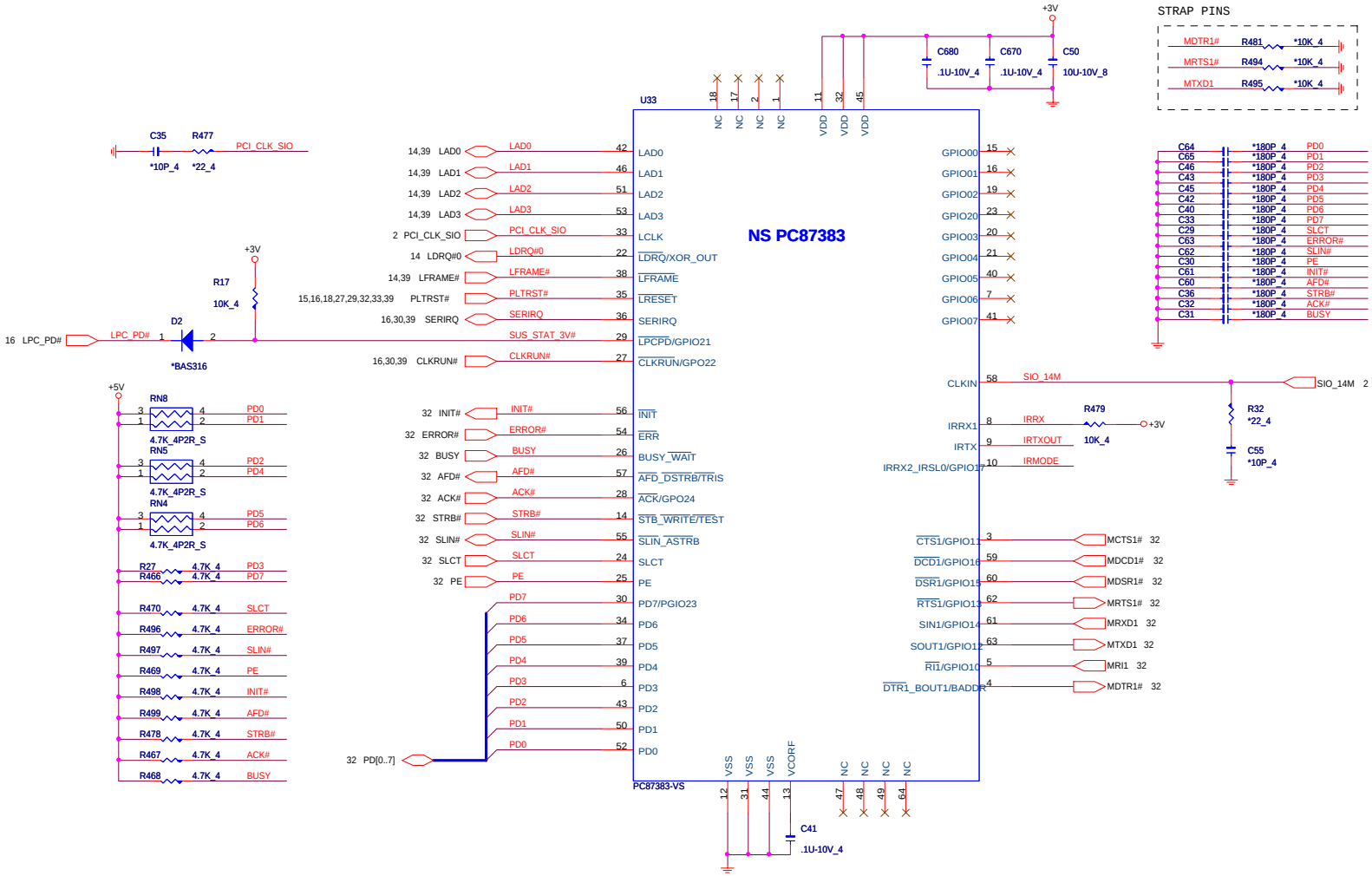
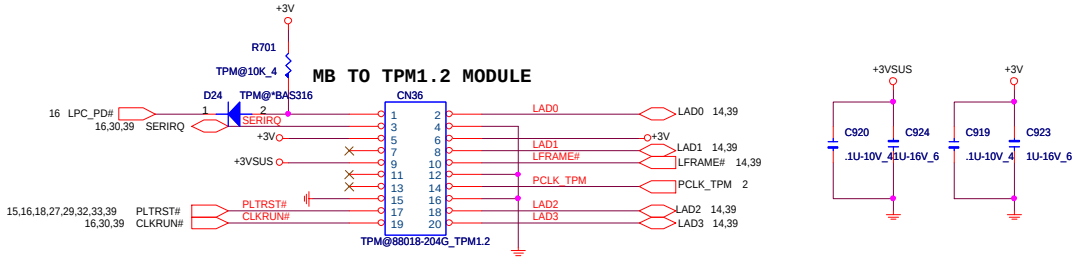
hetant@hotmail.com

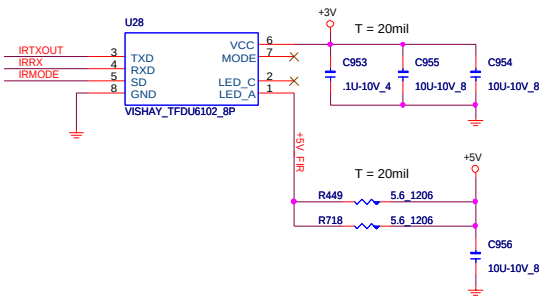




A1A:Change TPM CONN to 88018-204G(Pitch=0.8,H=2.65)

B1B:Change TPM pin define to same as ZH2

FIR



PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	SIO (87383),TPM 1.2	1A

Date: Monday, November 28, 2005 Sheet 38 of 46

Adapter ID	
Watt	Voltage
65W	0.66 +/- 0.1V
90W	1.32 +/- 0.1V
135W	1.98 +/- 0.1V
150W	2.64 +/- 0.1V
Un-define	3.3 +/- 0.1V

Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

LDRQ#(pin 8) internal is no use

A1A:Reserved GSENSOR-X/Y/Z for security alarm cicuit

A1A:Remove REFON pin (DA3 pin 102)

D2B:Add RST_KXP84_EC for G sensor reset(IOPA6)

D2B:Add G-Sensor SMBUS to EC(SCL2,SDA2)

D2B:Change EC_FPBACK# to IOPC6

D2B:Change Cardbus detect to IOPD0

SHBM=1: Enable shared memory with host BIOS

SST 1MB BIOS (AKE35ZAKK17)

ST Micro M29W008AB/AMD-29LV081B/SST39VF080

B1B:Reversed for G sensor buzzer

D2B:Change buzzer power to +5V,increase volume

BIU configuration should match flash speed used

CHANGED FROM PR_INSERT#

FOR 97551 ONLY

A1A:Reserved for debug use

B1B:Change SW4 p/n to DHP00BB1J03

INTERNAL PULLUP IN SB

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	97551 & FLASH	1A

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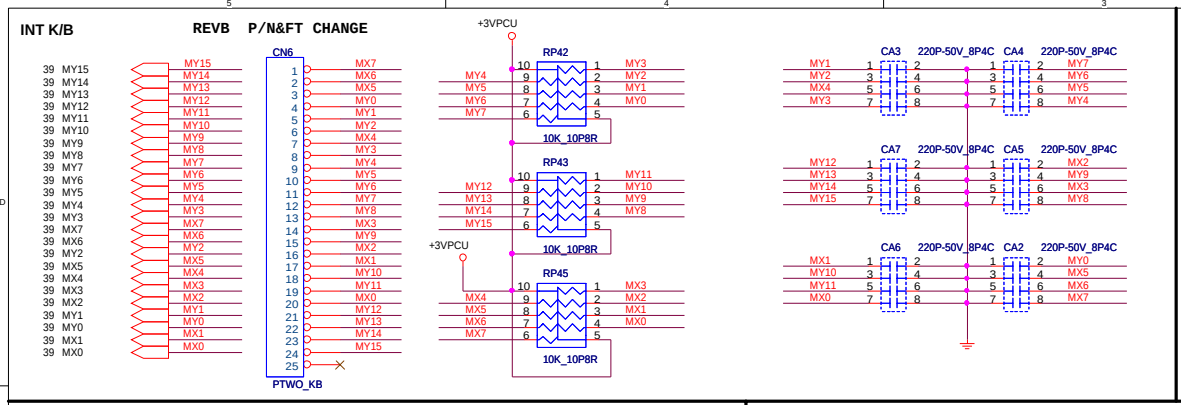
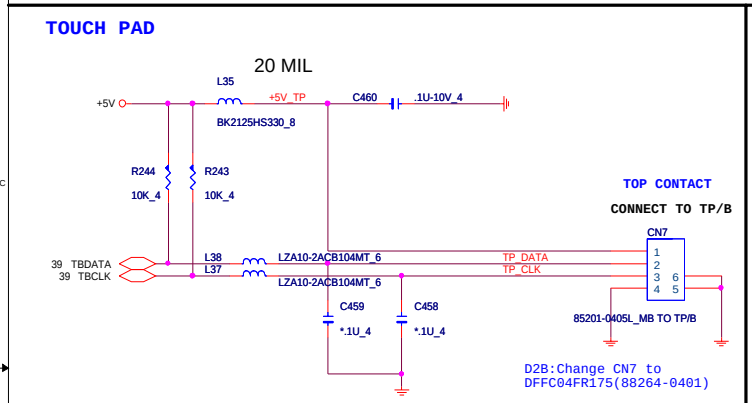
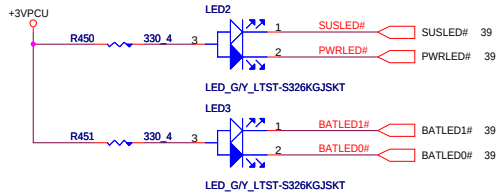
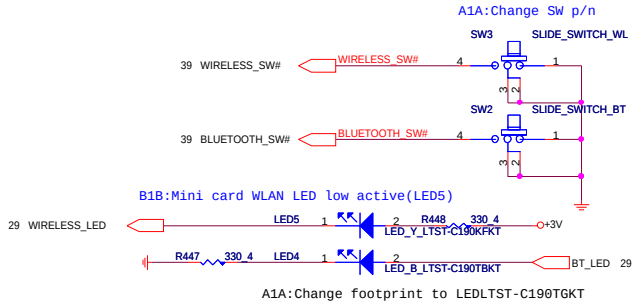
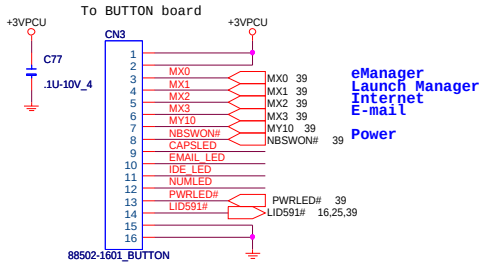








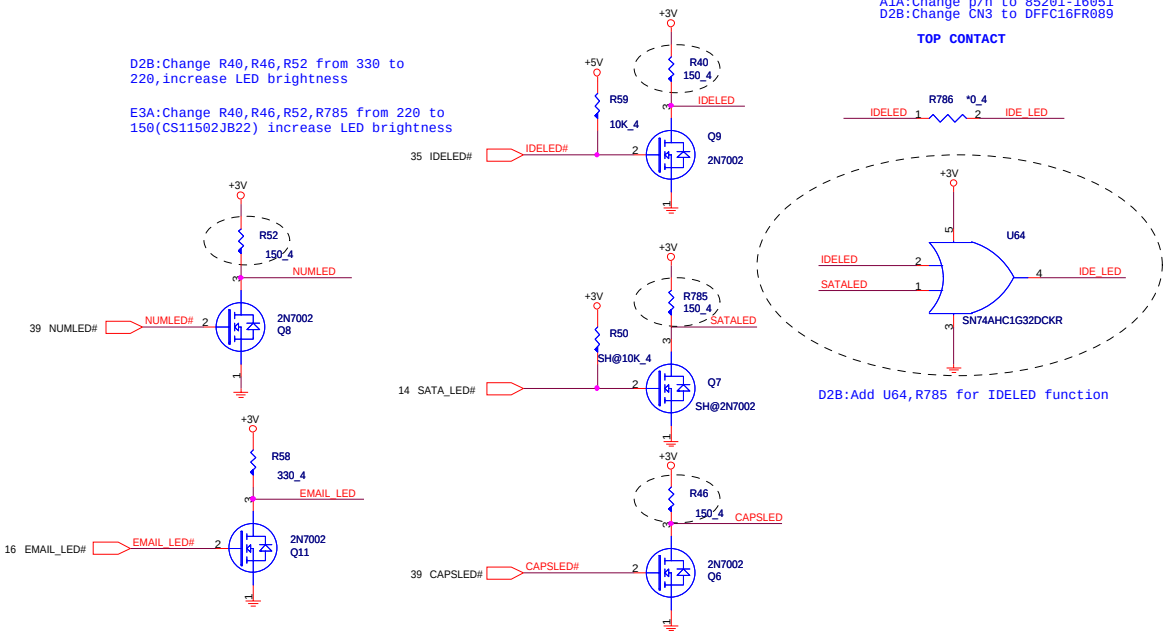


A1A:Change p/n to 85201-16051
D2B:Change CN3 to DFFC16FR089

TOP CONTACT

D2B:Change R40,R46,R52 from 330 to 220,increase LED brightness

E3A:Change R40,R46,R52,R785 from 220 to 150(CS11502JB22) increase LED brightness



D2B:Add U64,R785 for IDELED function

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	SWITCH,LED,K/B,TP	1A

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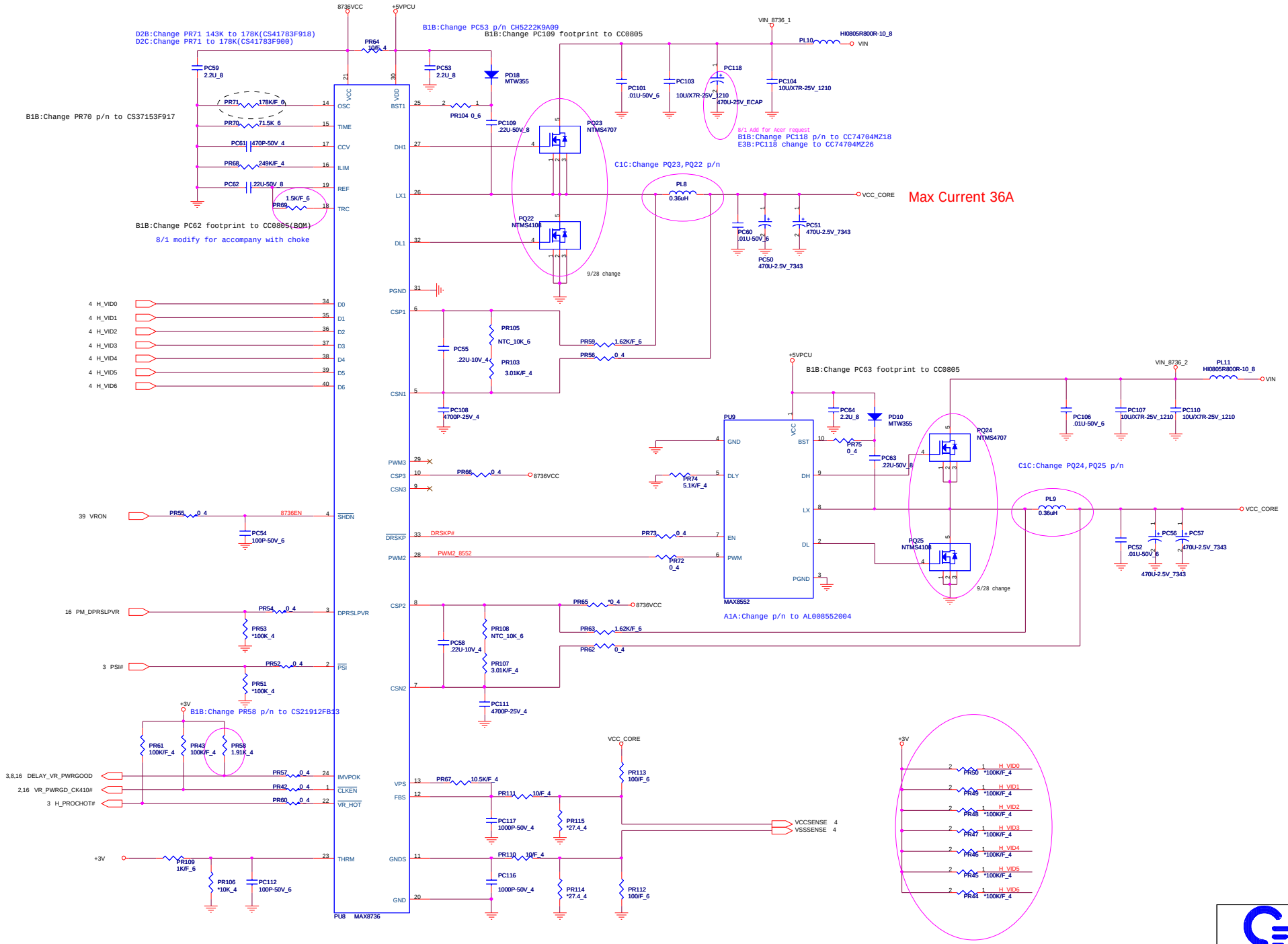
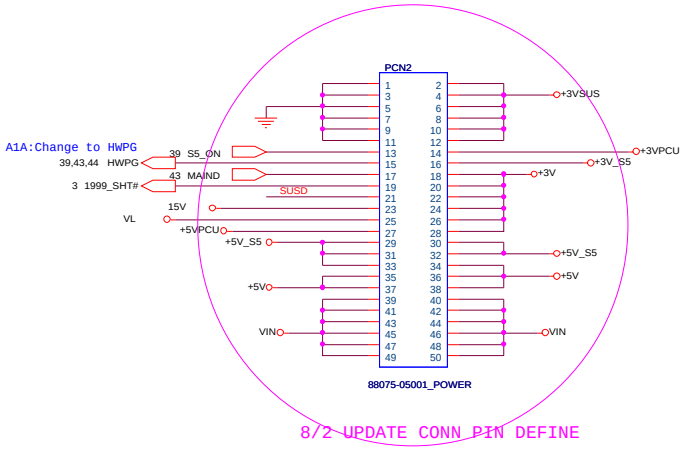
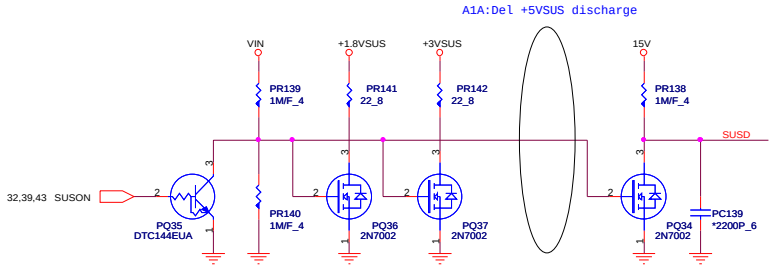
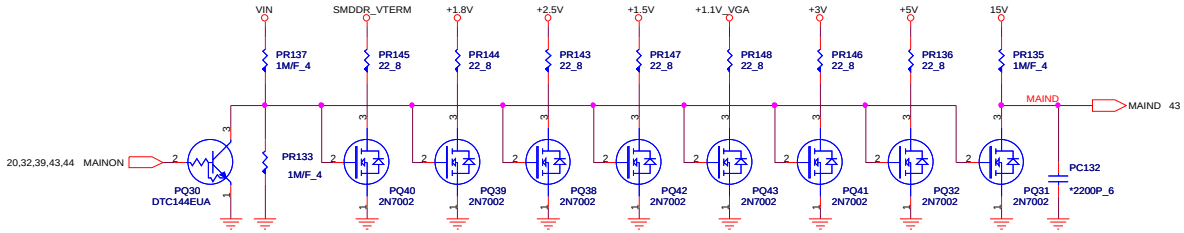


hexaline@hotmail.com







PROJECT : ZC1

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	DISCHARGE/CONNECTOR	1A

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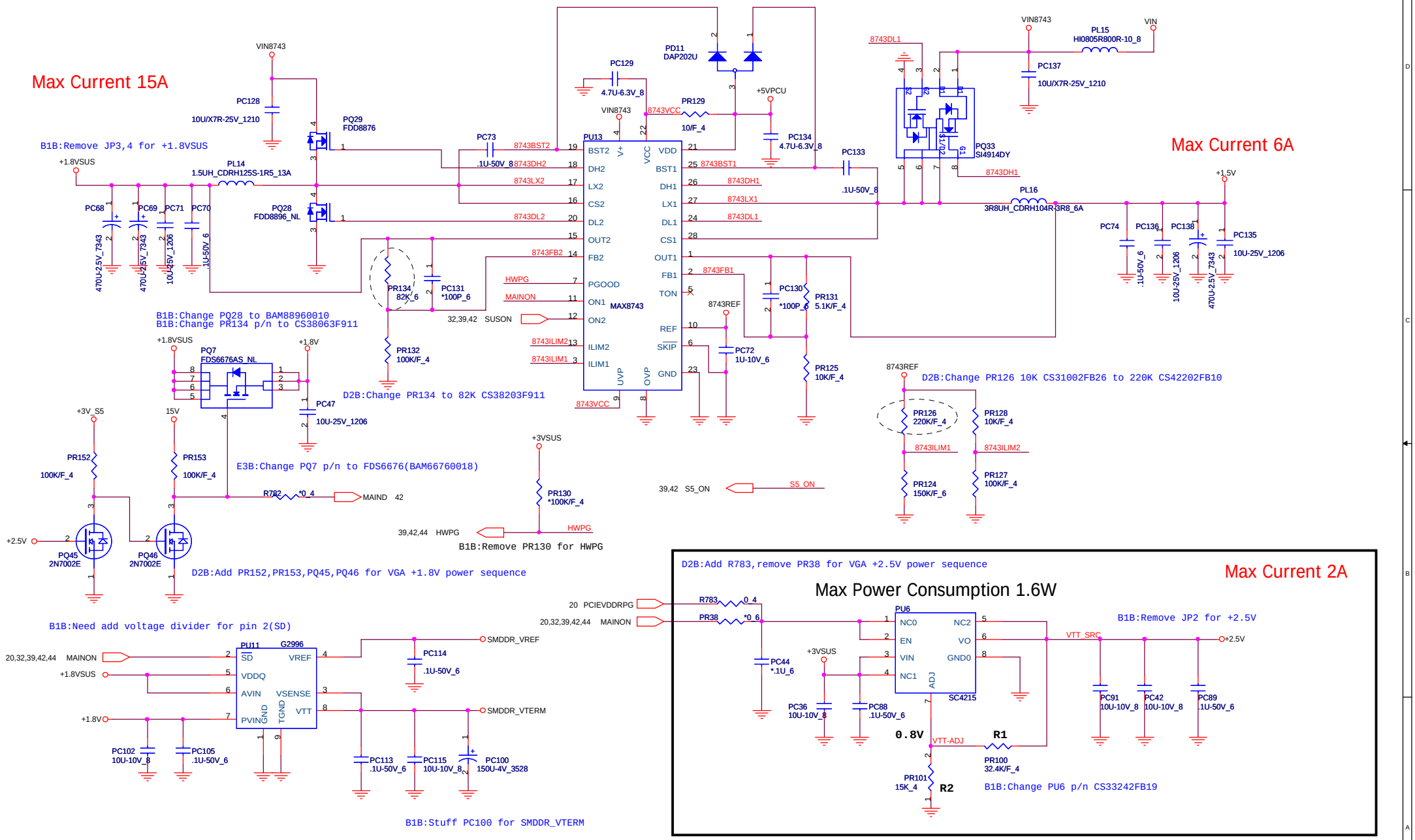
Max Current 15A
Max Current 6A
Max Current 2A
Max Power Consumption 1.6W
B1B:Remove JP3,4 for +1.8VSUS
B1B:Change PQ28 to BAM88960010
B1B:Change PR134 p/n to CS38063F911
D2B:Change PR134 to 82K CS38203F911
E3B:Change PQ7 p/n to FDS6676(BAM66760018)
D2B:Add PR152,PR153,PQ45,PQ46 for VGA +1.8V power sequence
B1B:Need add voltage divider for pin 2(SD)
B1B:Stuff PC100 for SMDDR_VTERM
B1B:Remove PR130 for HWPG
D2B:Change PR126 10K CS31002FB26 to 220K CS42202FB10
D2B:Add R783,remove PR38 for VGA +2.5V power sequence
B1B:Remove JP2 for +2.5V
B1B:Change PU6 p/n CS33242FB19
MAX8743
SC4215
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Quanta Computer Inc.
Size
Document Number
+2.5V/+1.8VSUS / +1.5V
Rev
A
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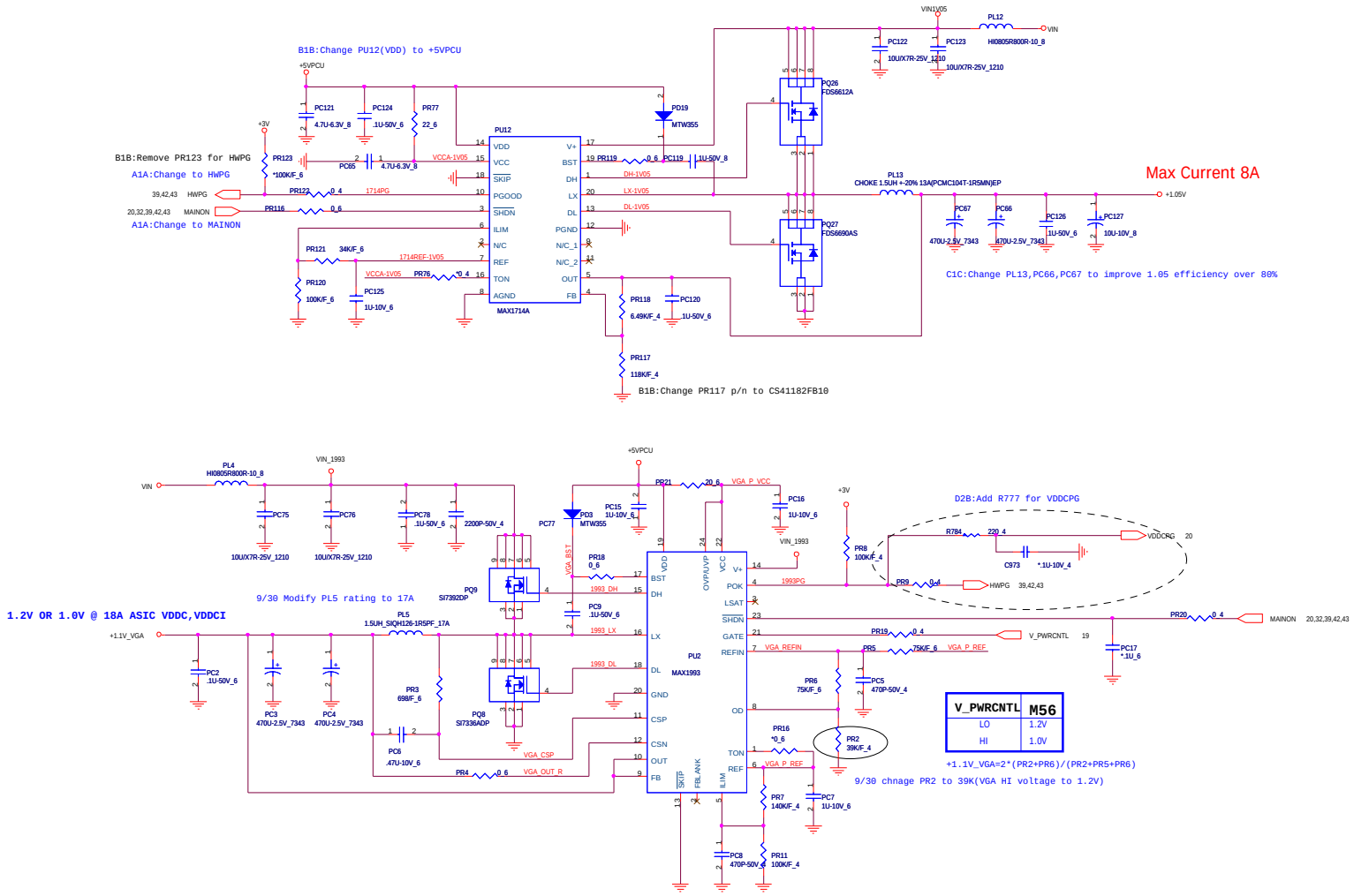

V_PWRCNTL	M56
LO	1.2V
HI	1.0V

B1B:Change PR39 p/n to CS32003F933

D2B:Remove PR39,PR40,PR41,PC46,PC48,PC49,PC98,PC99,PU7 for +1.2V_VPCIE

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Custom	+1.05V/+1.2V_VGA/+1.2V	1A

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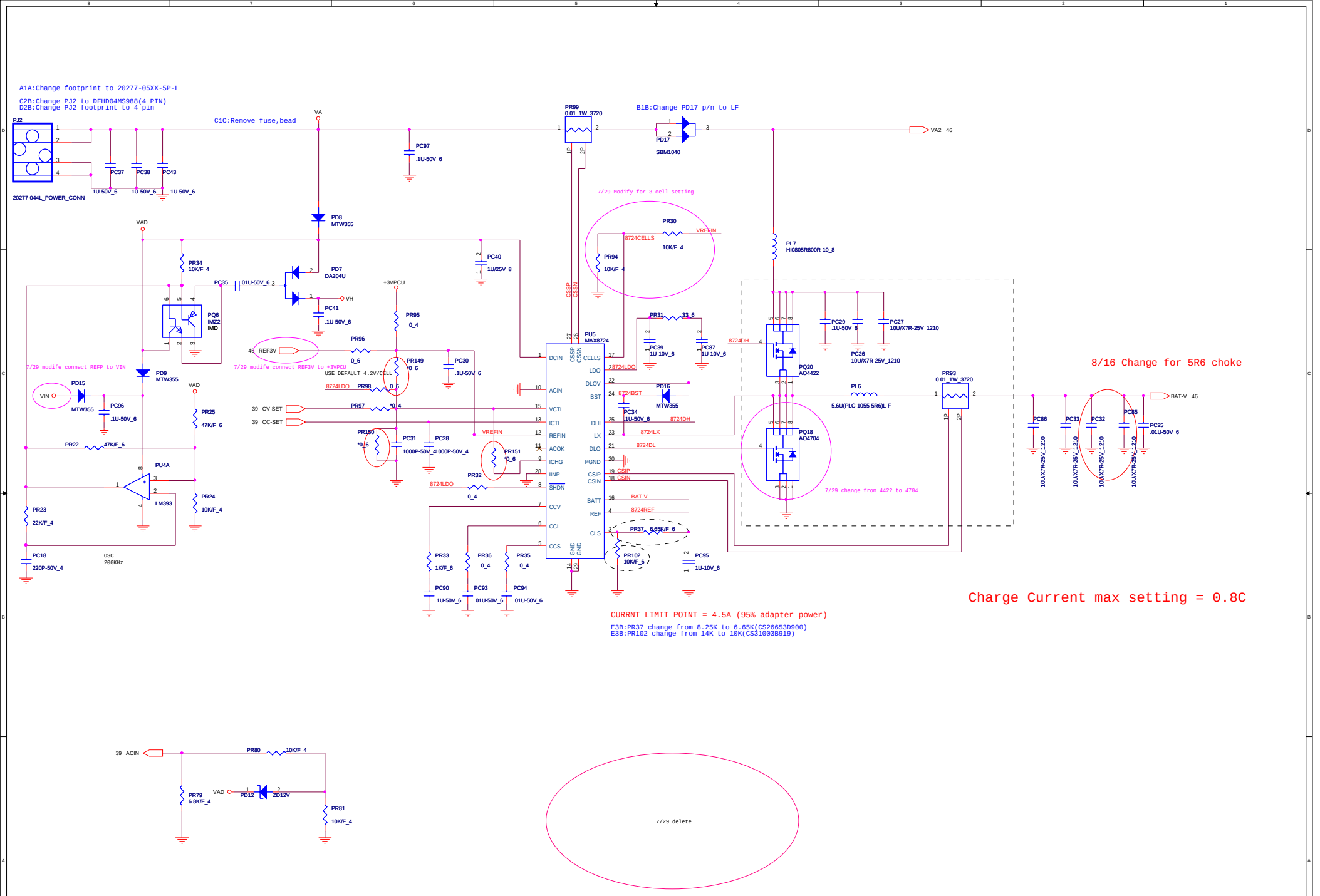
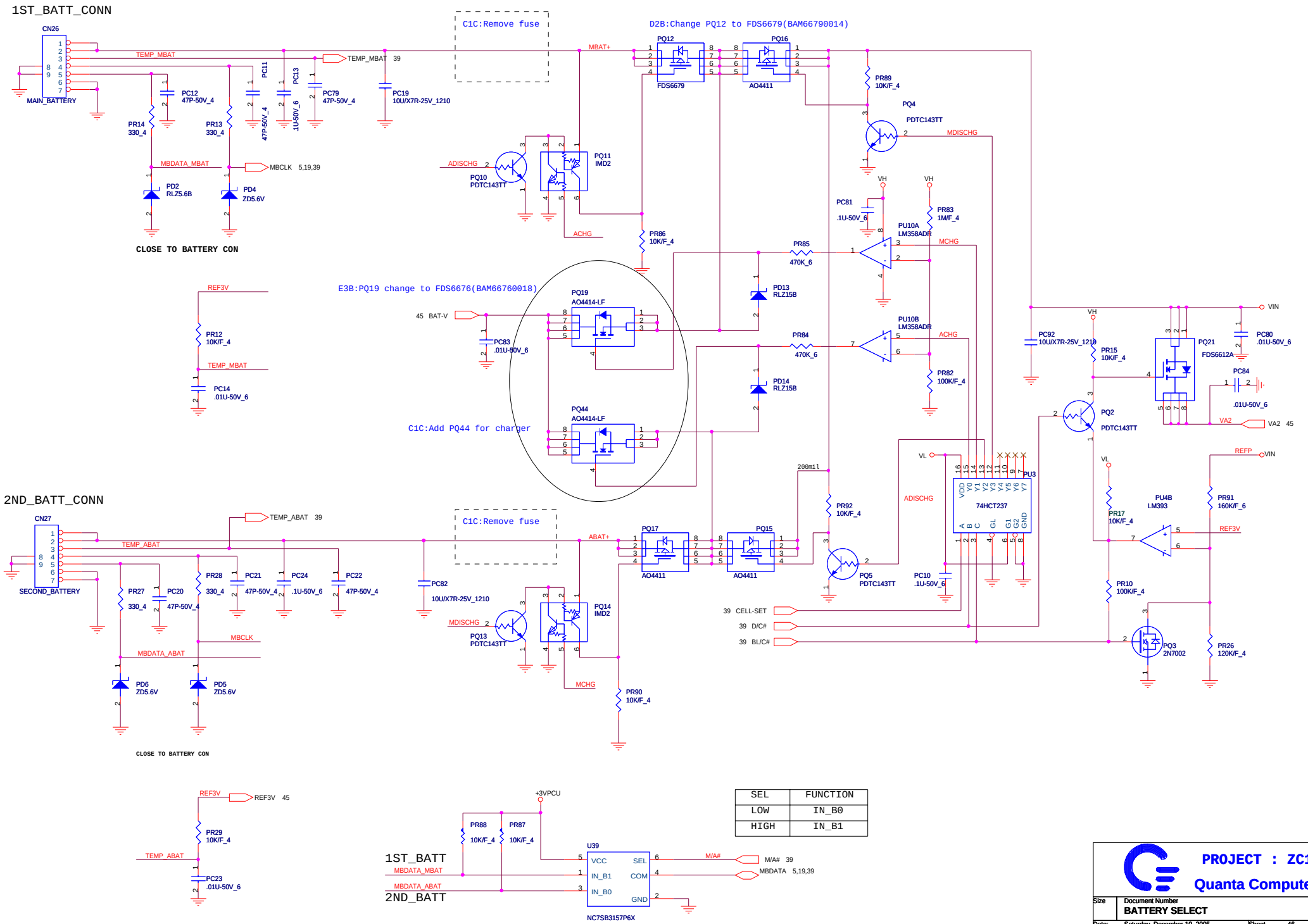


bekenf@hotmail.com

A1A:Change p/n to DFHD07MR391
B1B:Change CN26 footprint to 20175A-07G1-7P-R



SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

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	BATTERY SELECT	A

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