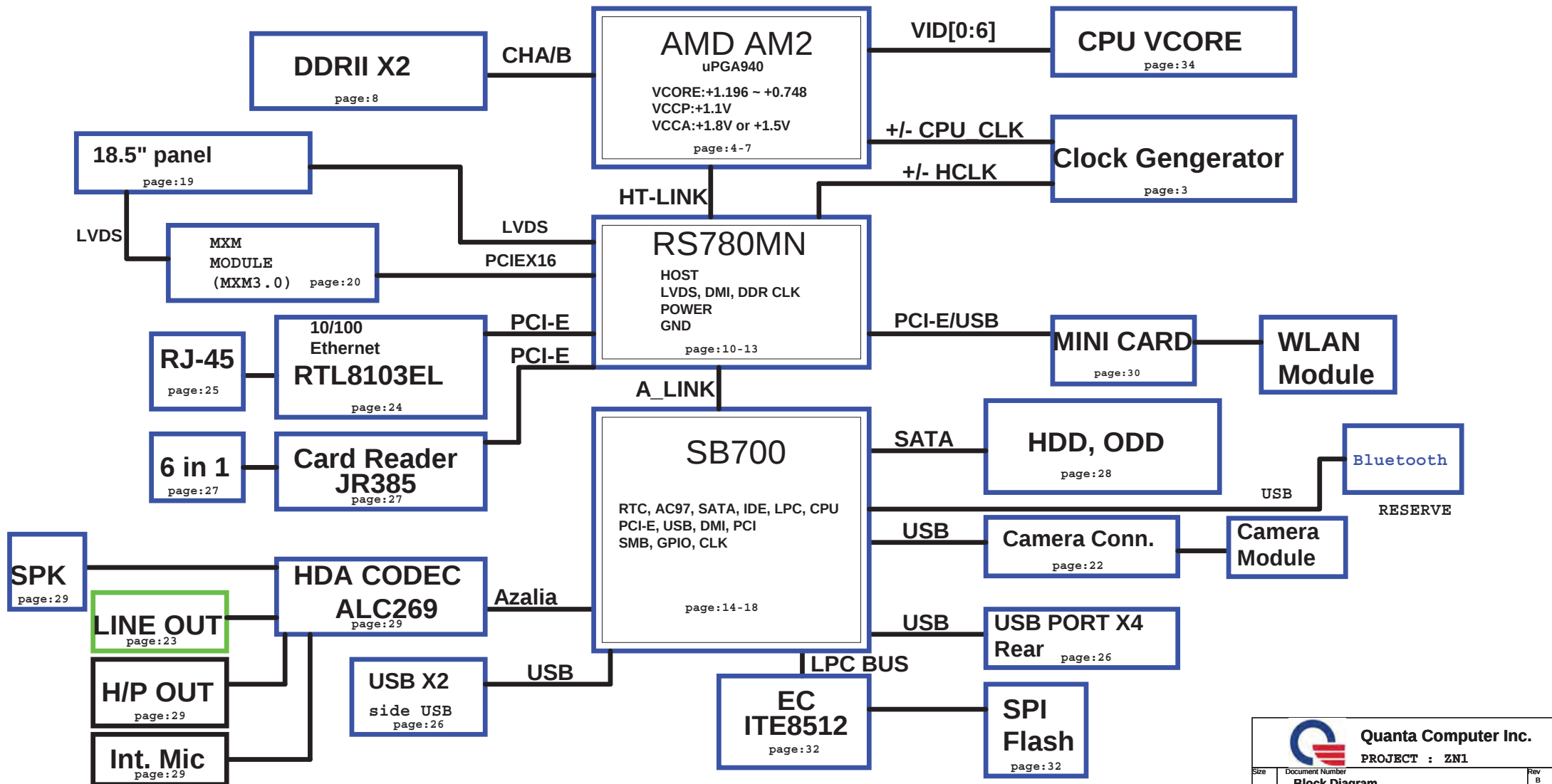


Amazon LCD PC Block Diagram

1

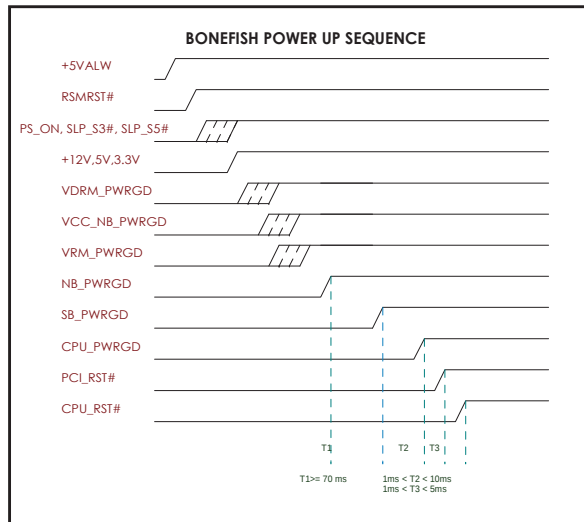


PCB STACK UP

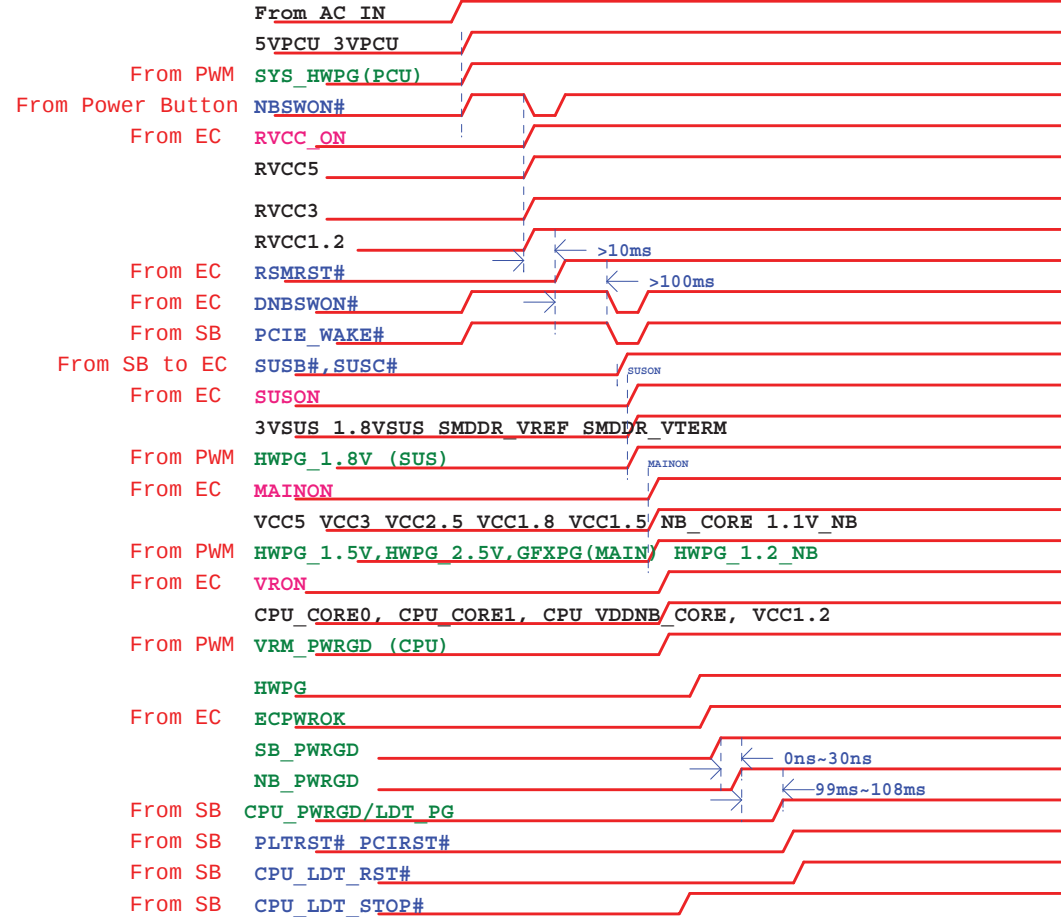
LAYER 1 : TOP
LAYER 2 : VCC
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : GND
LAYER 6 : BOT

Voltage Rails

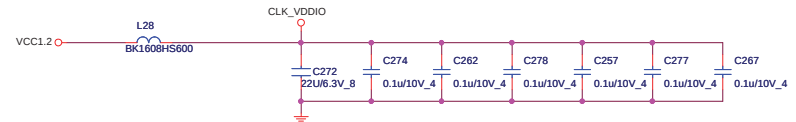
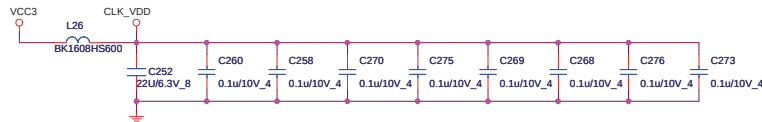
Power	Voltage	S0-S2	S3	S4	S5	Ctl Signal
15VPCU	15V	V	V	V	V	
5VPCU	5V	V	V	V	V	VIN
3VPCU	3V	V	V	V	V	VIN
RVCC3	3V	V	V	V	V	RVCC_ON
RVCC1.2	1.2V	V	V	V	V	RVCC_ON
5VSUS	5V	V	V			SUSD
1.8VSUS	1.8V	V	V			SUSON
VCC5	5V	V				MAIND
VCC3	3V	V				MAIND
VCC1.8	1.8V	V				MAIND
VCC1.5	1.5V	V				MAINON
VCC1.2	1.2V	V				MAINON
CPU_VDDA	2.5V	V				VCC3
NB_CORE	1.2V	V				VRON
SMDDR_VTERM	0.9V	V				SUSON
CPU_CORE	By CPU	V				VR_ON



Power On Sequence

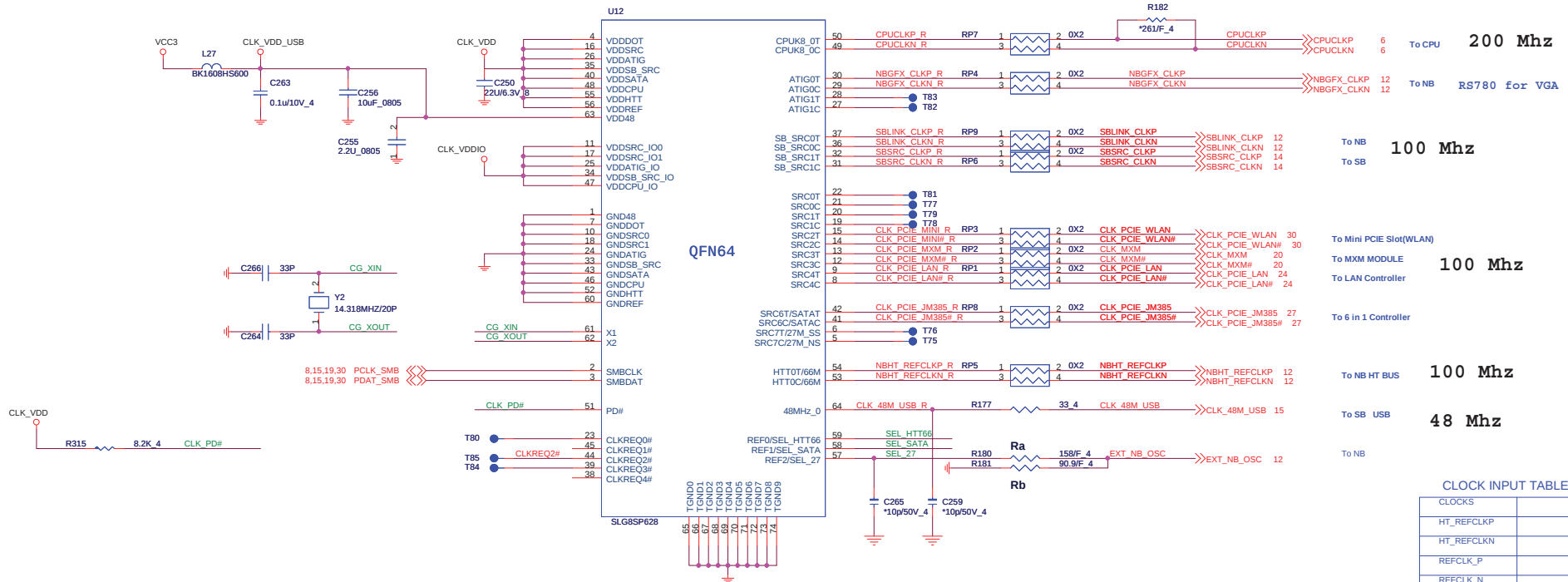


CLK_GEN_SLG8SP628



ICS9LPRS480 P/N : ALPRS480000
SLG8SP628 P/N : AL8SP628000
RTM880N-796 P/N : AL000880000

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.
Place within 0.5" of CLKGEN



CLOCK INPUT TABLE

CLOCKS	RS780
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	vref
GFX_REFCLK	100M DIFF(IN/OUT)*
GPP_REFCLK	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF

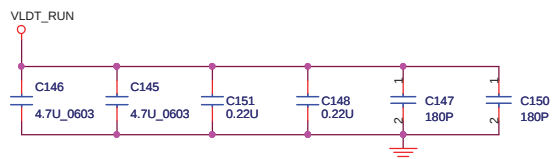
SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

* default

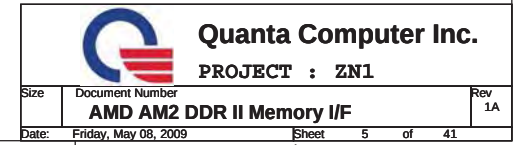


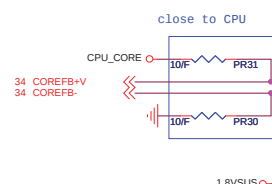
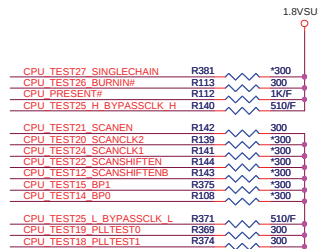
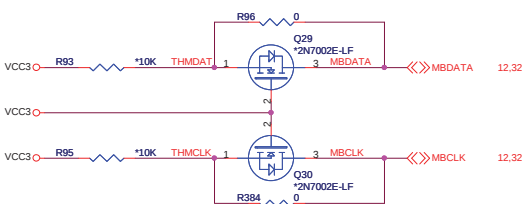
Quanta Computer Inc.
PROJECT : ZN1

Size	Document Number	Rev
	Clock Generator	1A
Date:	Friday, May 08, 2009	Sheet 3 of 41

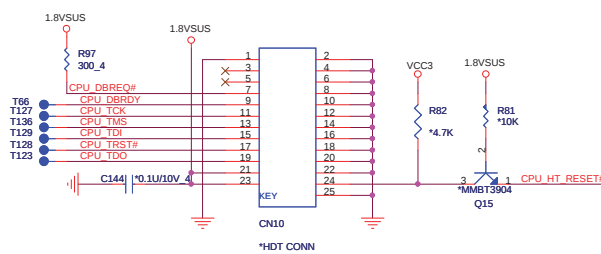
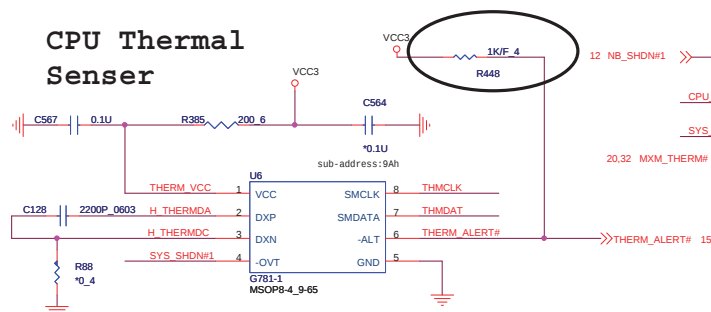


5

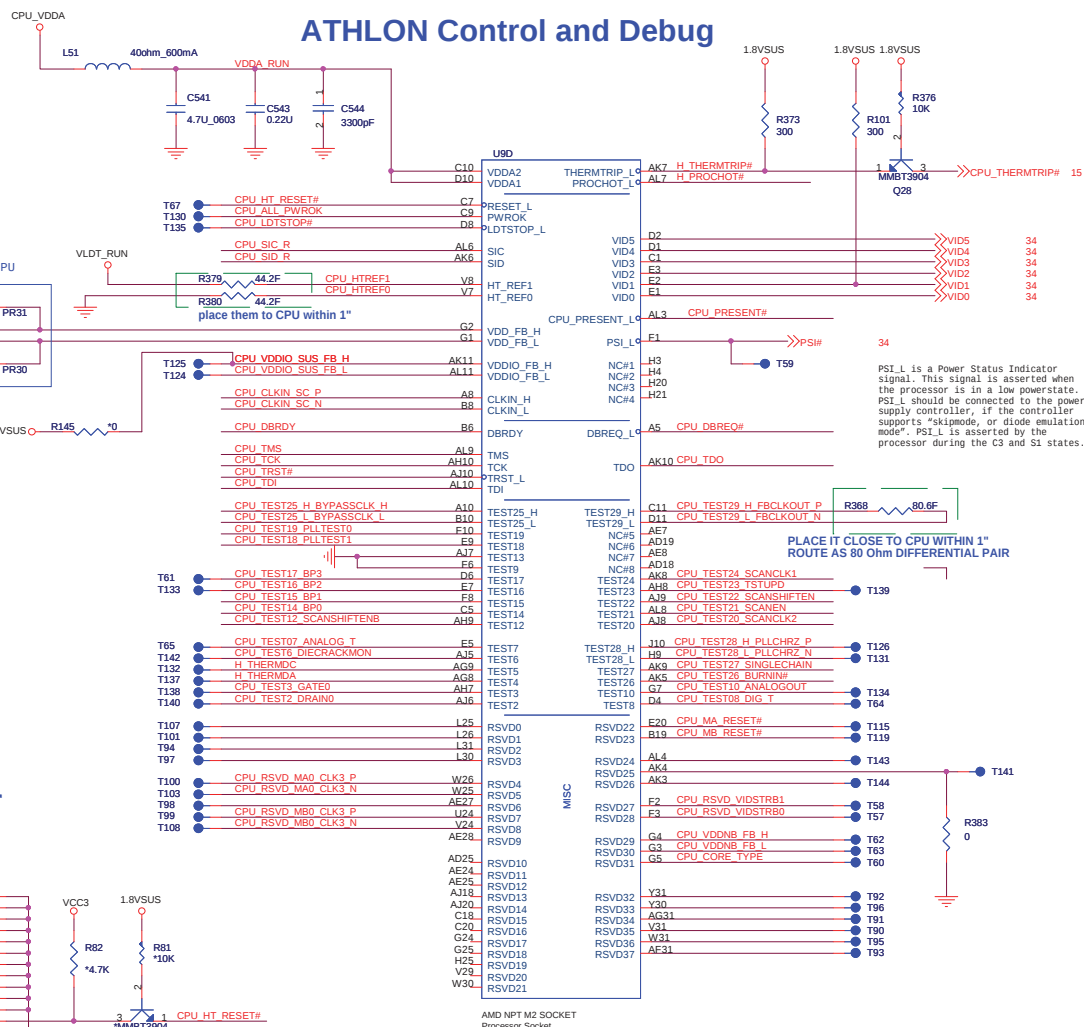




HDT Connector

CPU Thermal
Sensor

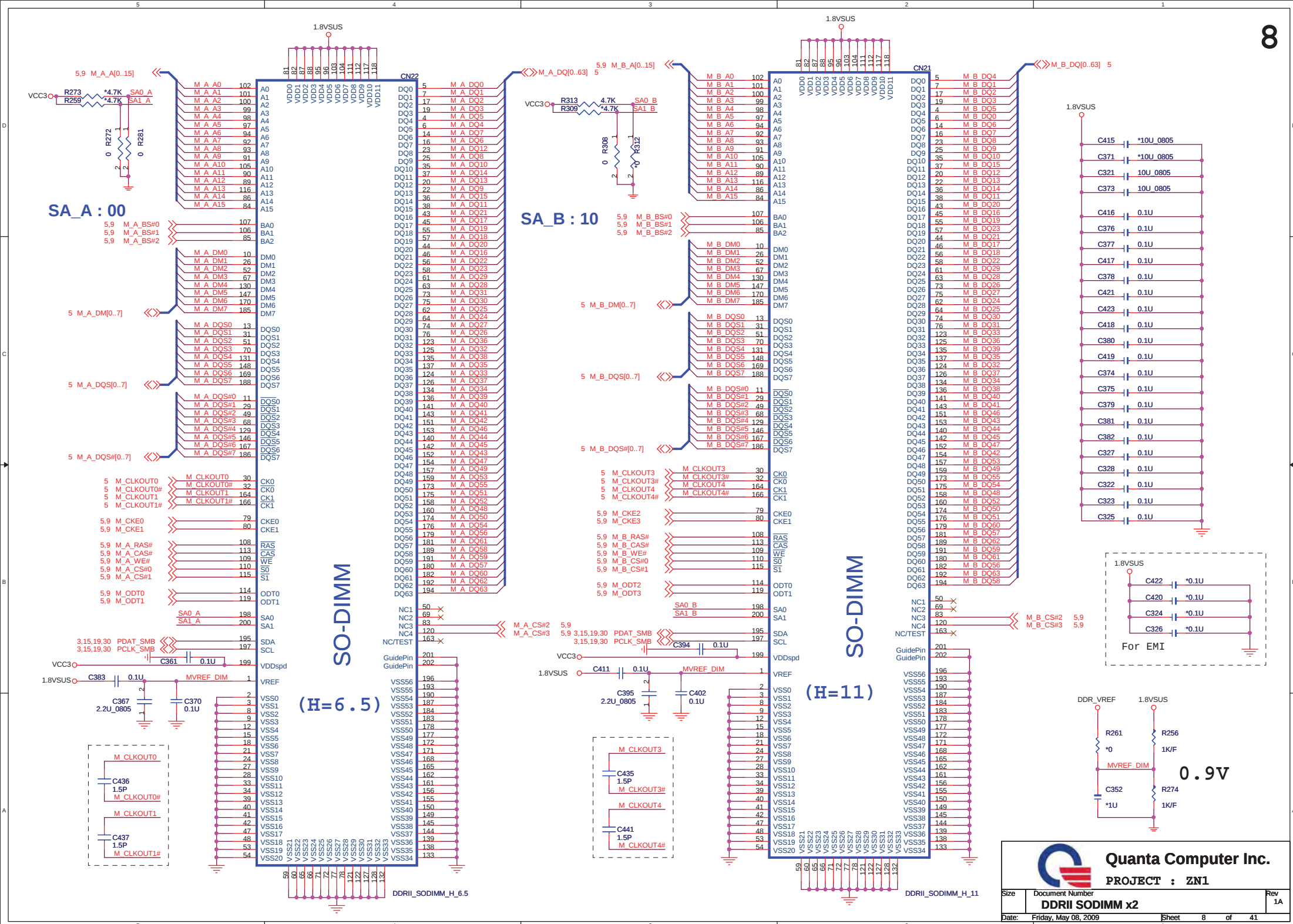
ATHLON Control and Debug



SMBUS SLAVE ADDRESS	
G781	98 (CPU)

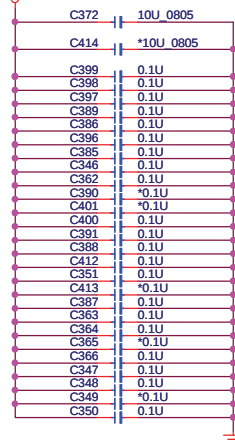
7

[illegible]



0.9V

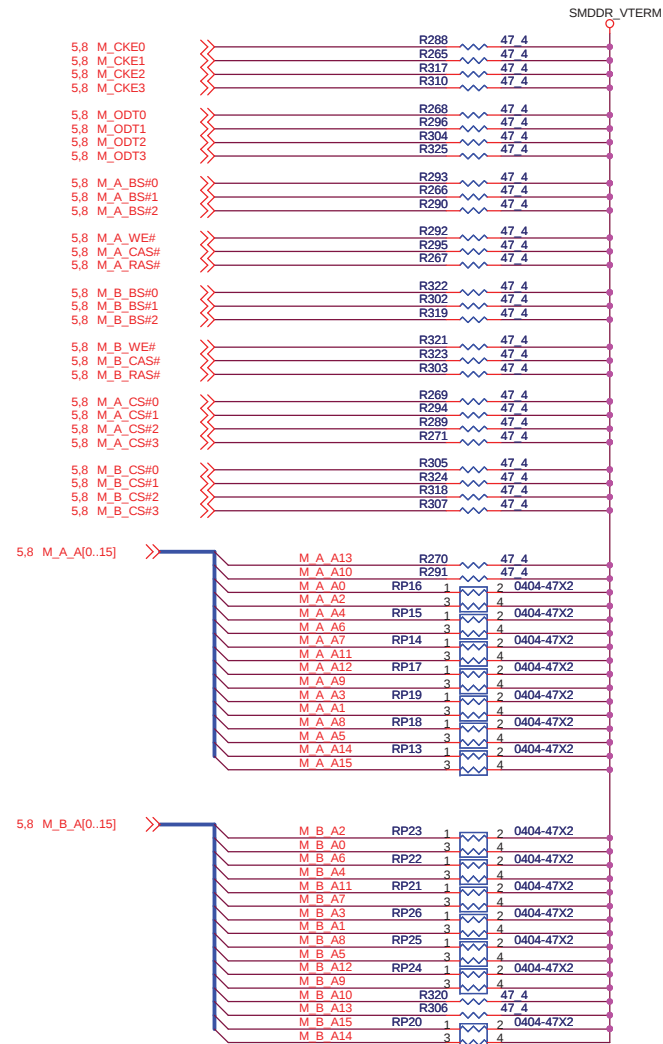
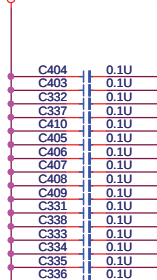
SMDDR_VTERM



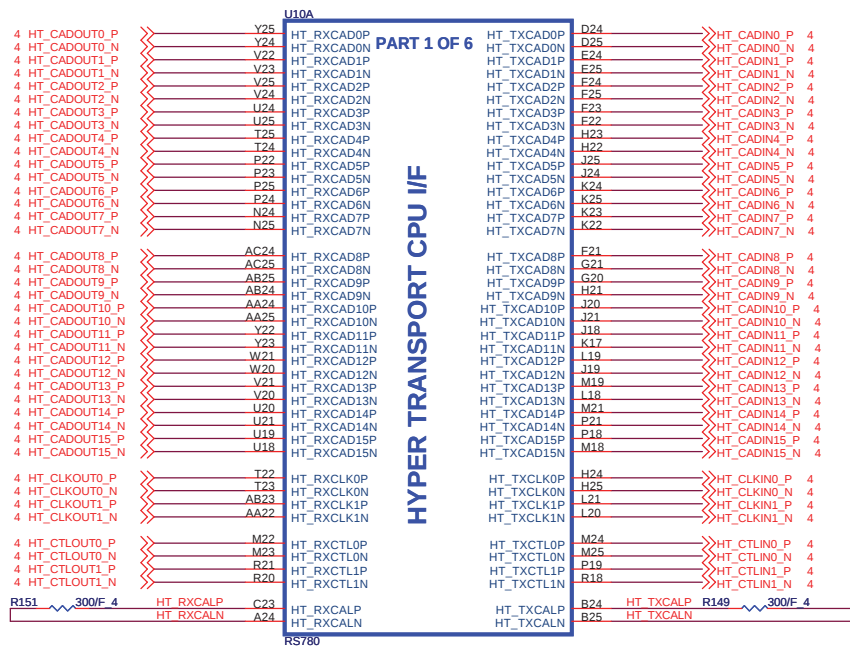
1.8VSUS

0.9V

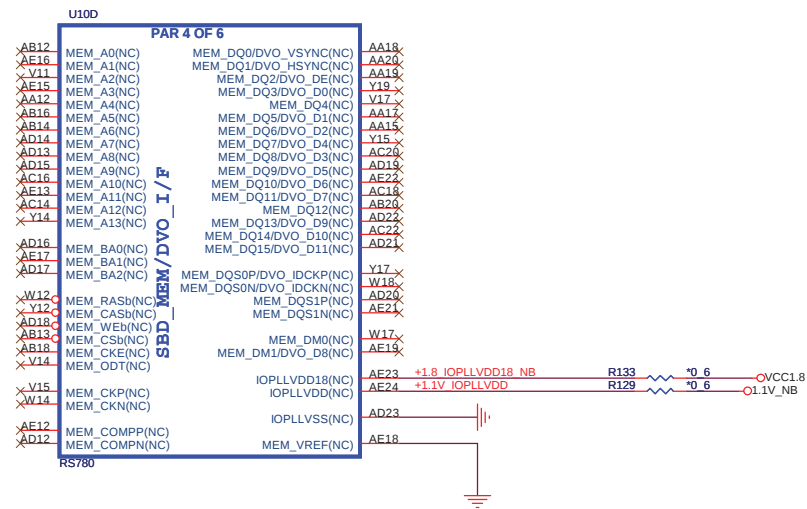
SMDDR_VTERM



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PROJECT : ZN1

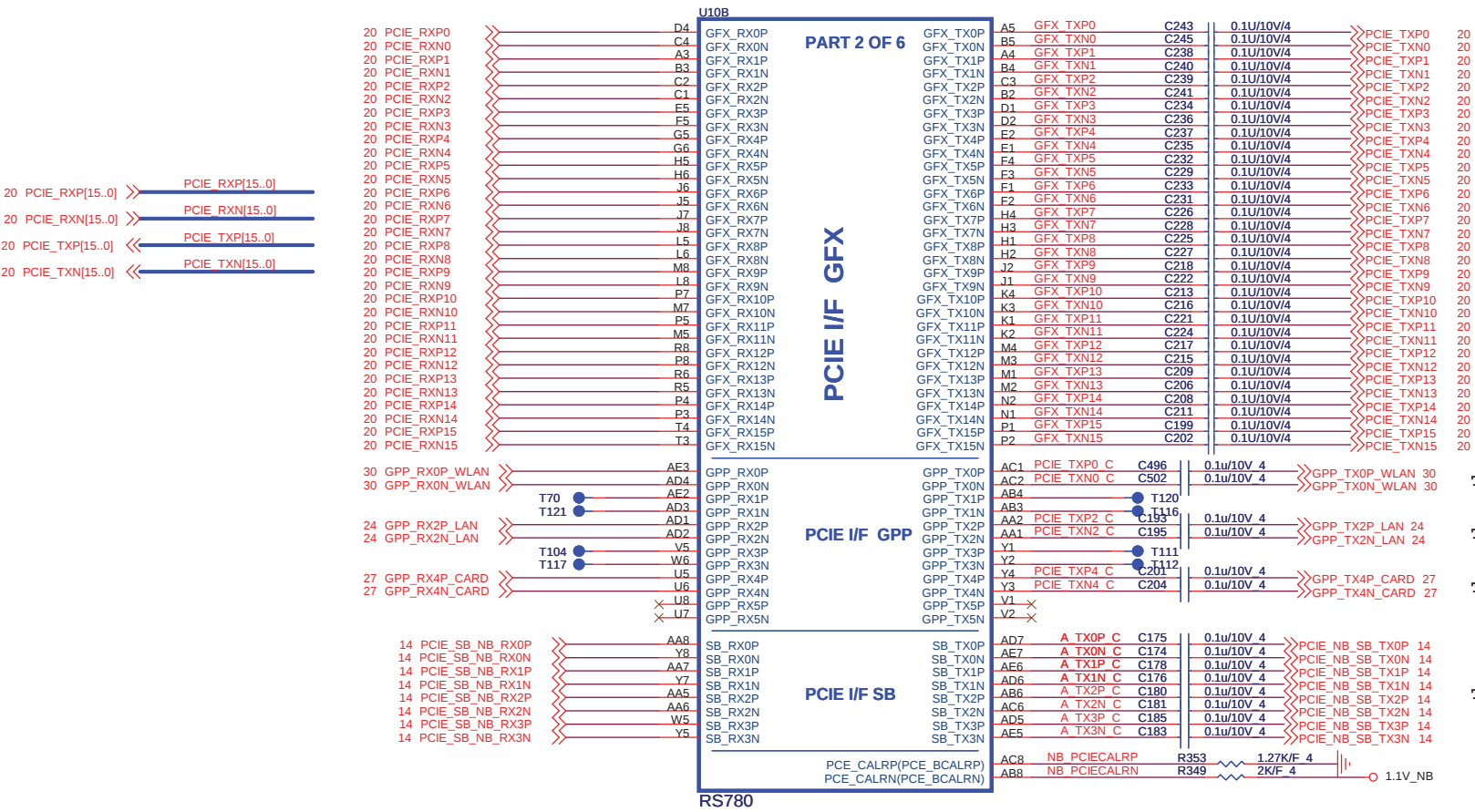


This block is for UMA RS780 only



Quanta Computer Inc.

PROJECT : ZN1



TO MXM MODULE

TO WLAN

TO LAN

TO CARD READER

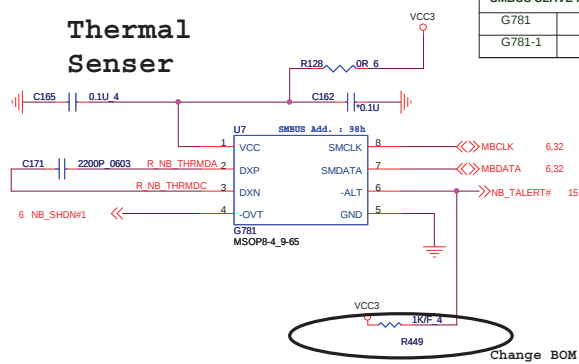
To A-Link



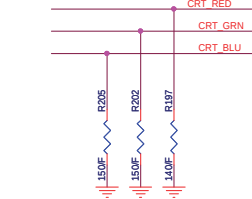
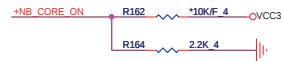
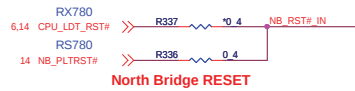
Quanta Computer Inc.
PROJECT : ZN1

Size	Document Number	Rev
	RS780M-PCIE I/F 2/4	1A
Date:	Friday, May 08, 2009	Sheet 11 of 41

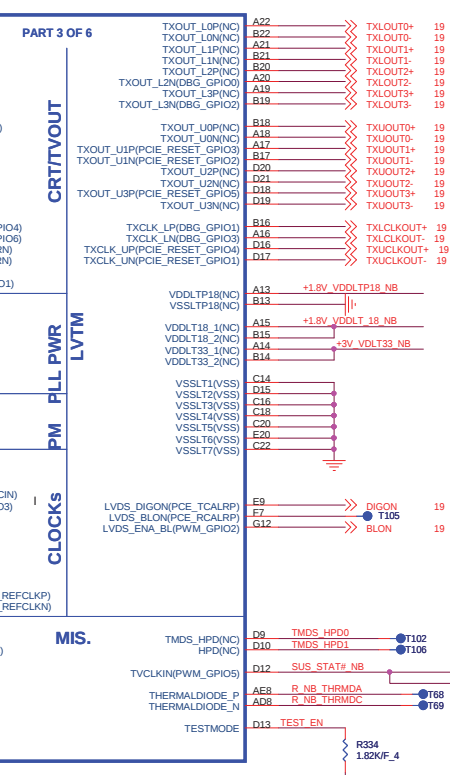
Thermal
Senser



Change BOM value

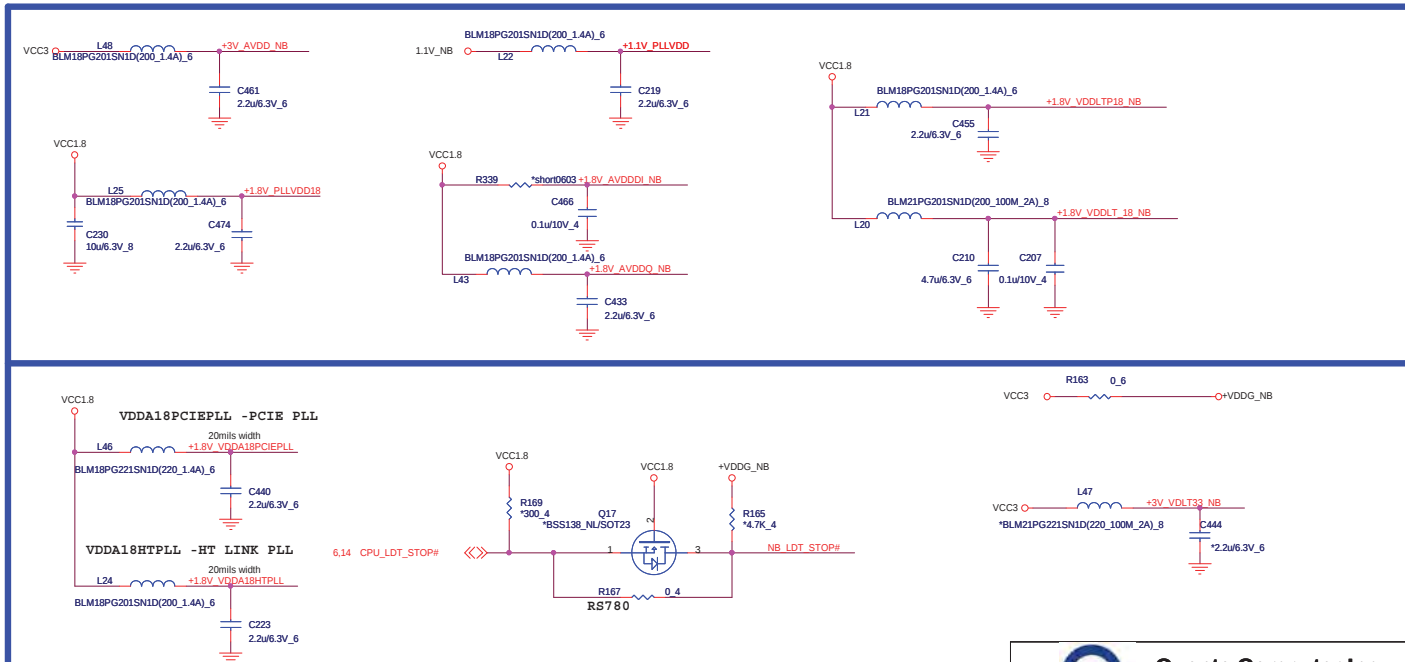
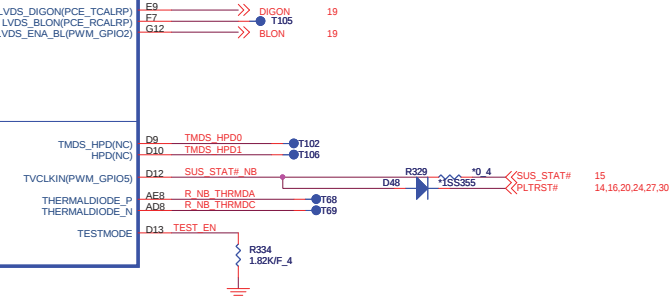


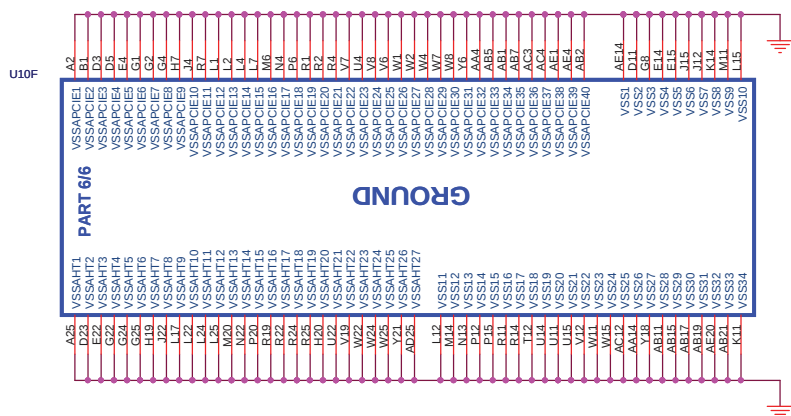
SMBUS SLAVE ADDRESS	
G781	98 (NB)
G781-1	9A (CPU)



To LVDS panel

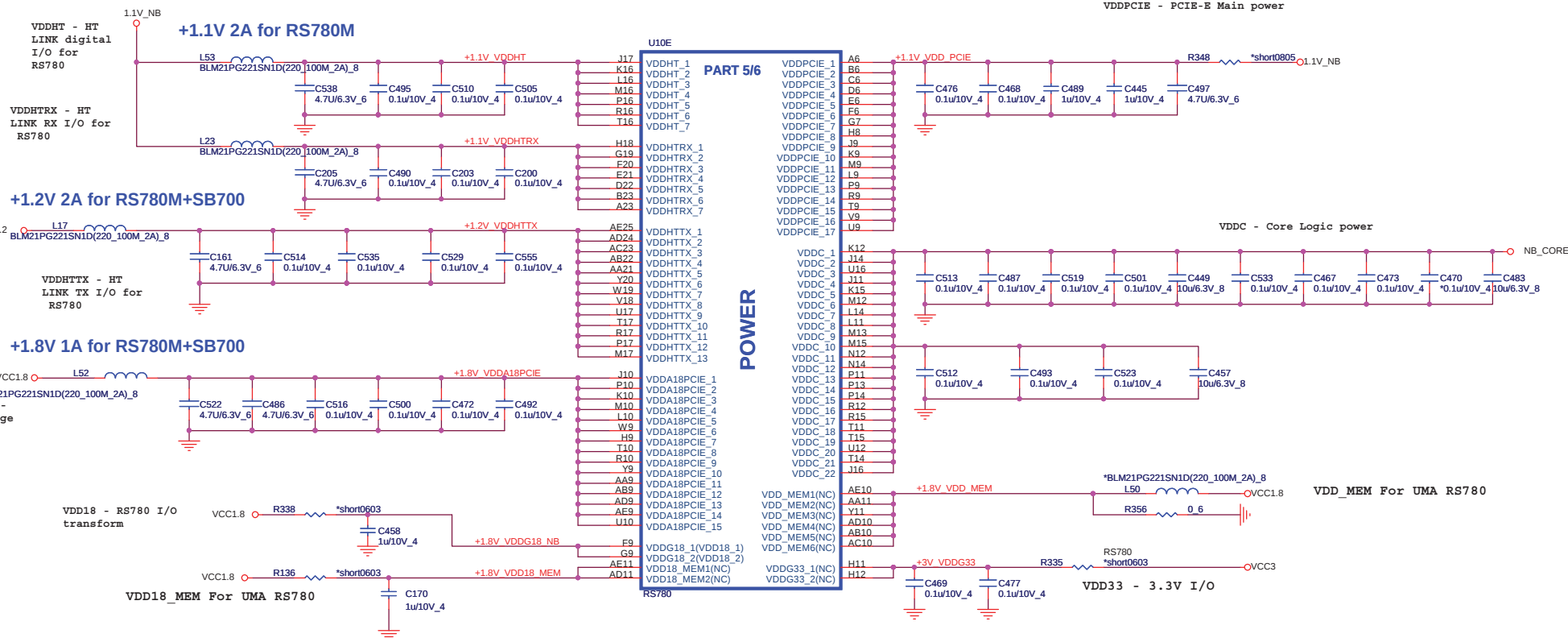
LVDS POWER

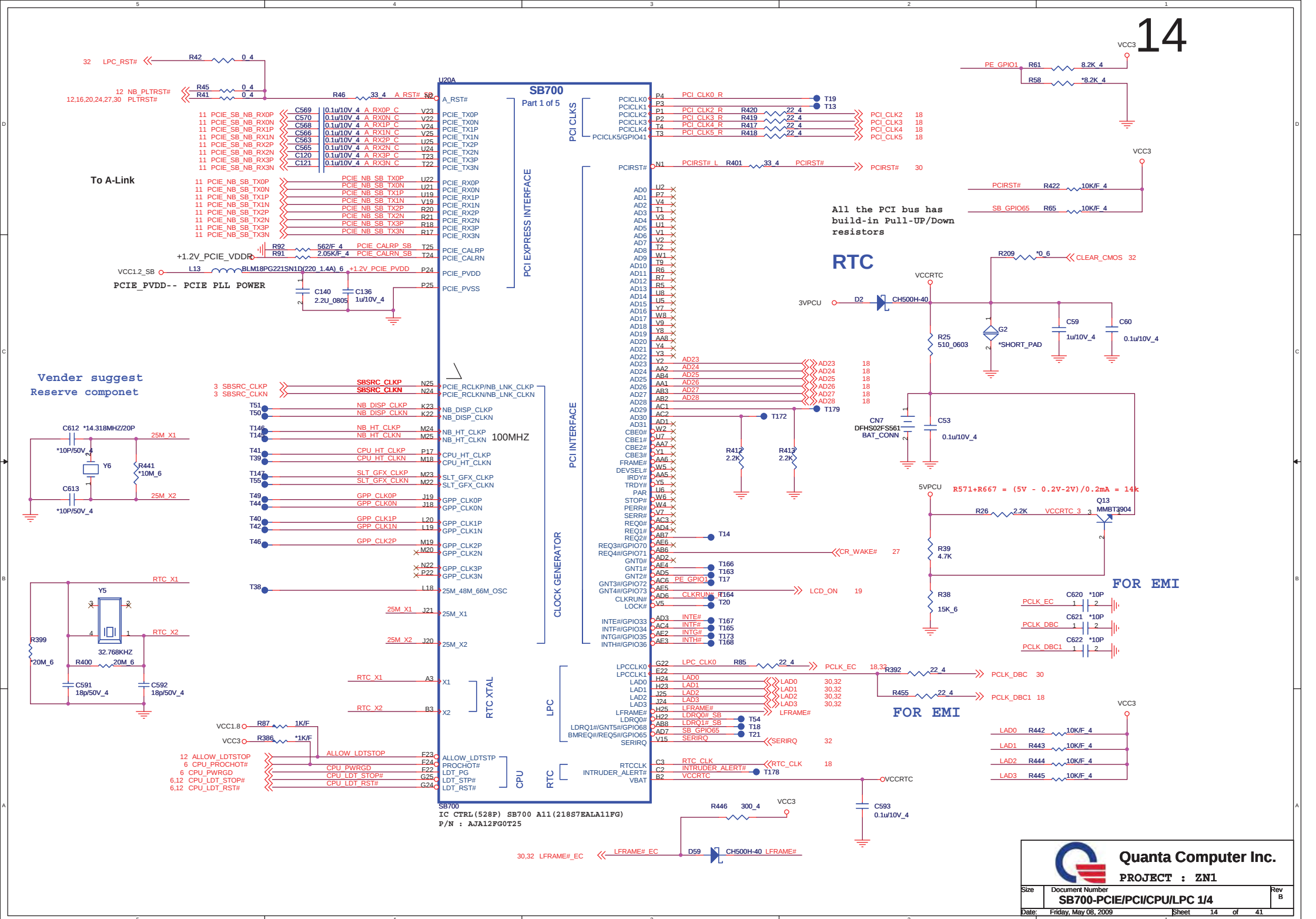


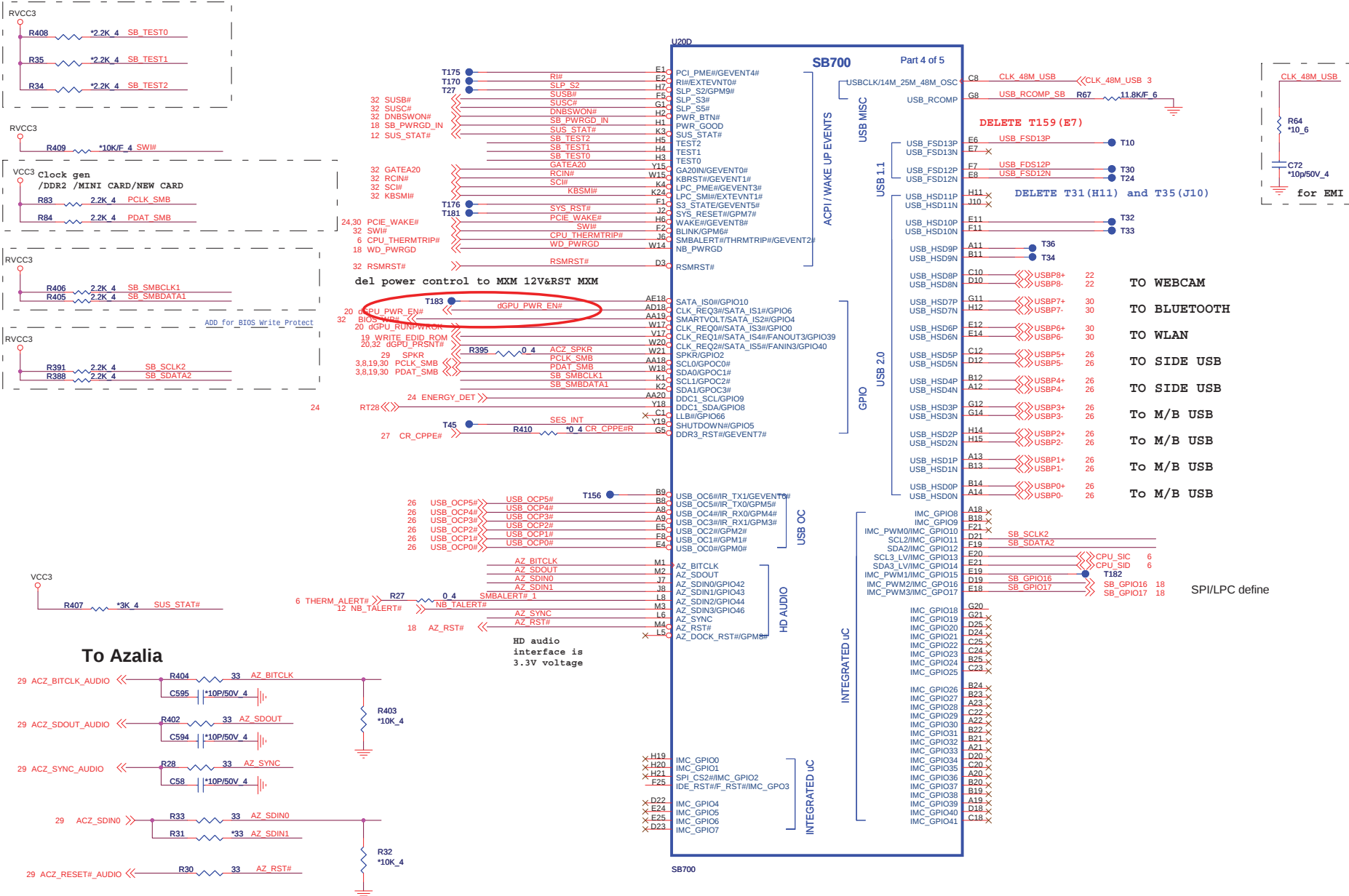


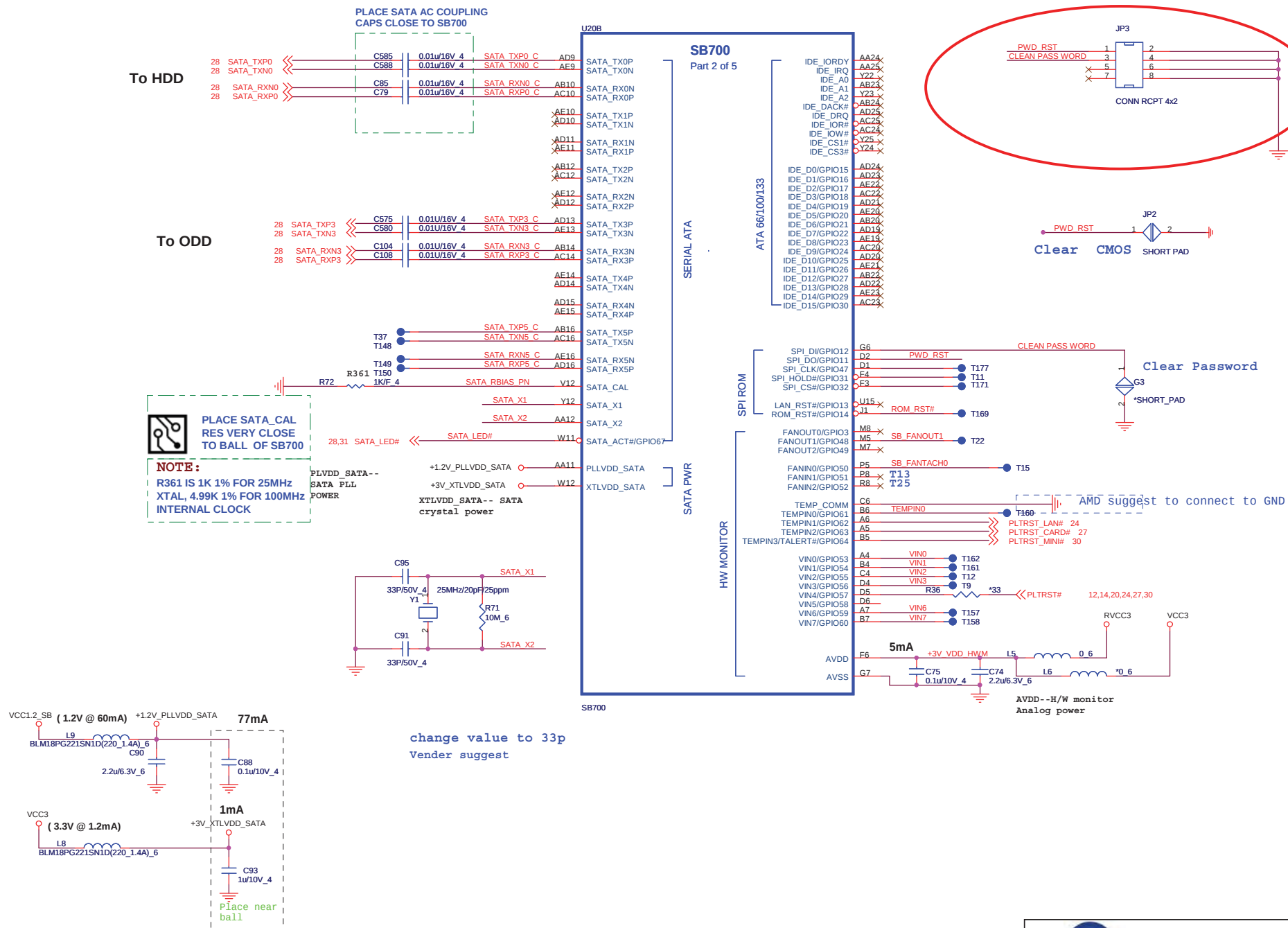
RS780 POWER DIFFERENCE TABLE

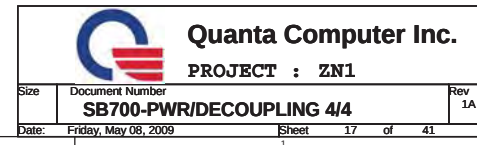
PIN NAME	RS780	PIN NAME	RS780
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDL18	+1.8V
IOPLLVD18	+1.8V	VDDL33	NC







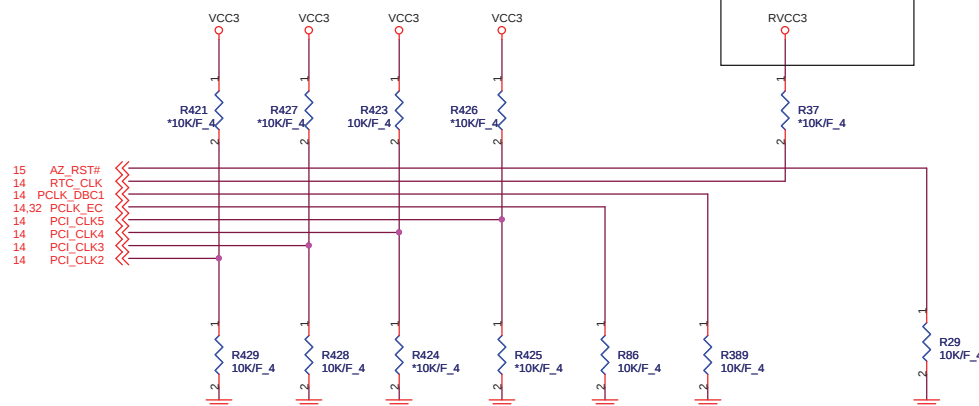






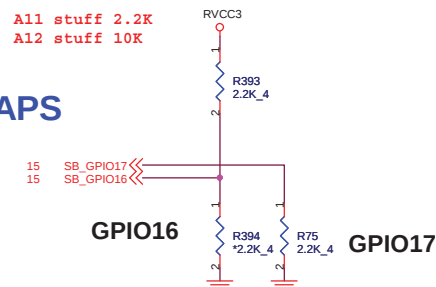
OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

It must ready
before RSMRST#



REQUIRED STRAPS

All stuff 2.2K
All stuff 10K



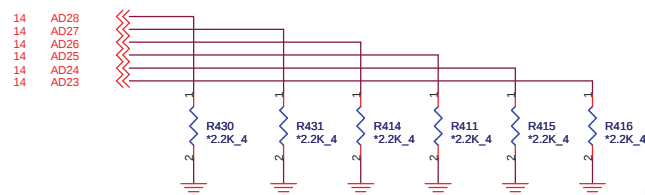
GPIO16

GPIO17

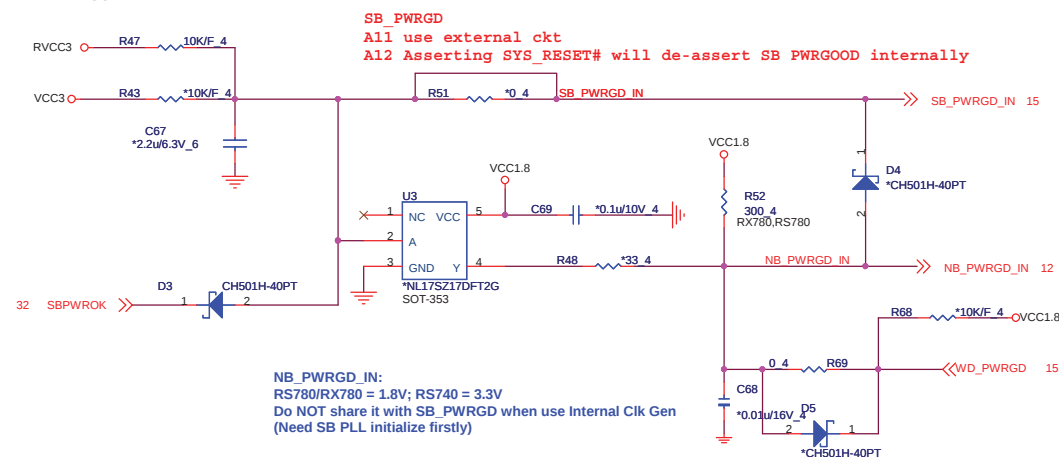
TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

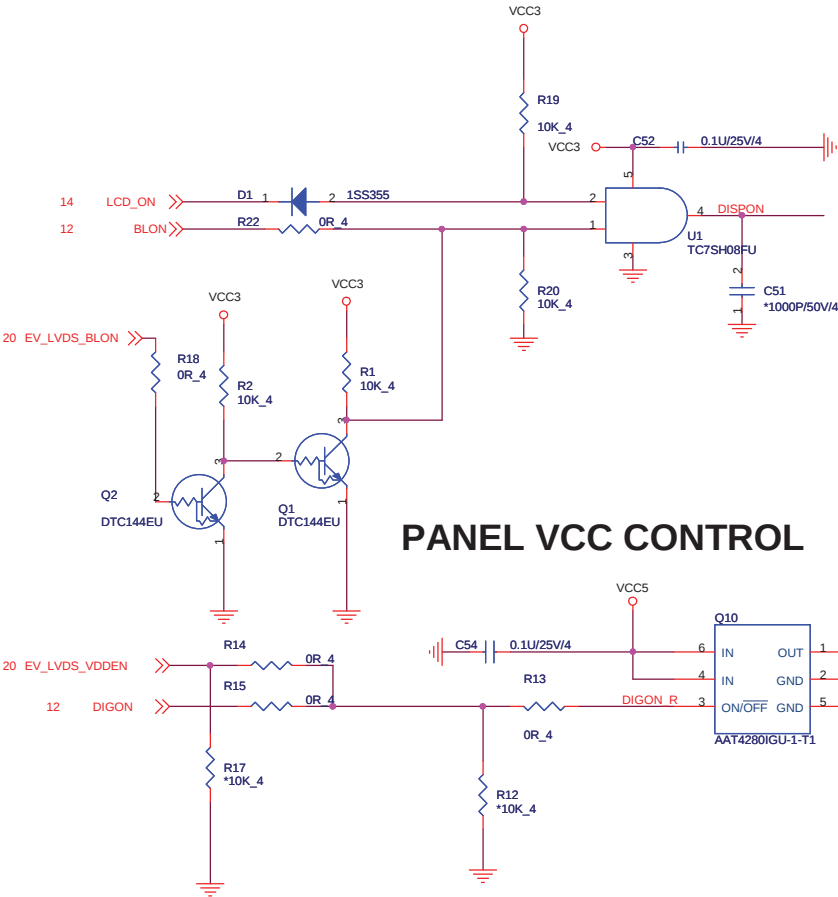


NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

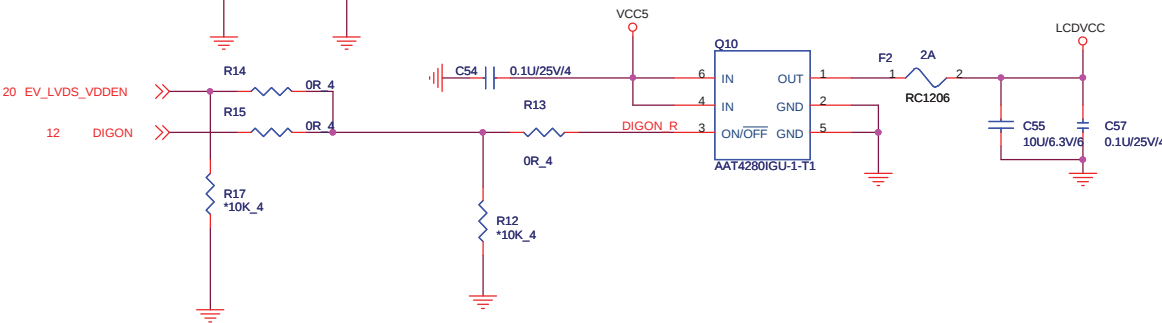


Quanta Computer Inc.
PROJECT : ZN1

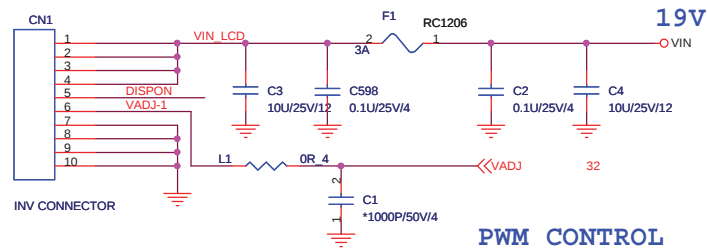
BACKLIGHT CONTROL



PANEL VCC CONTROL



TO INVERTER POWER

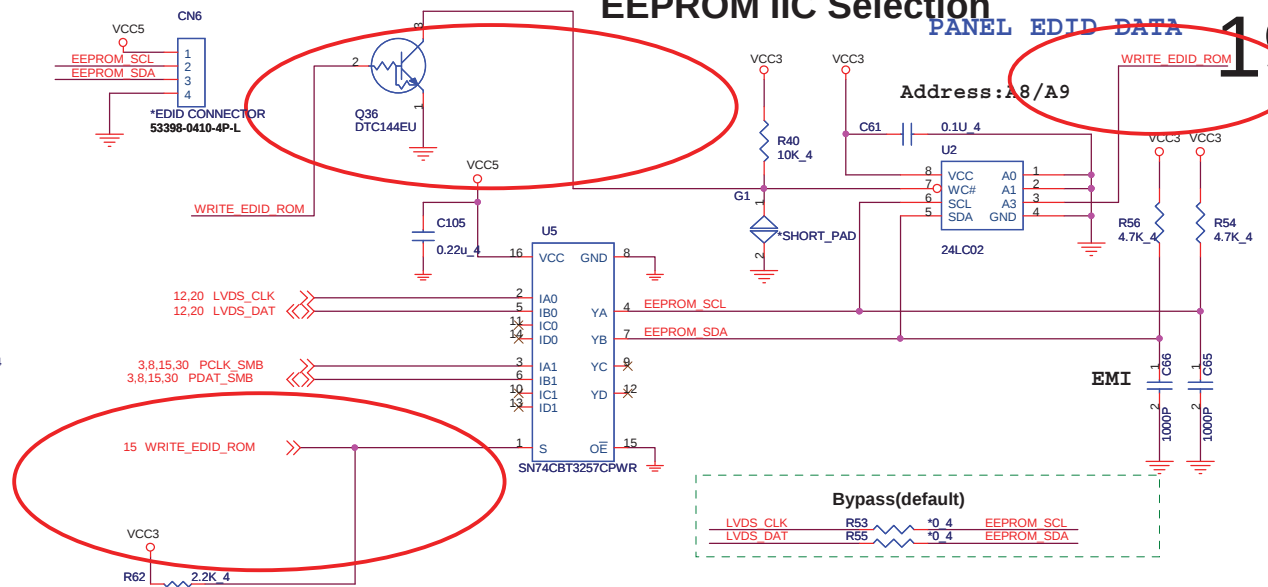


PWM CONTROL

EEPROM IIC Selection

PANEL EDID DATA

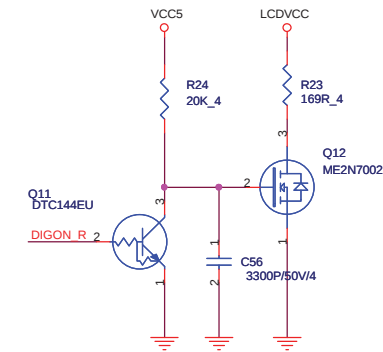
19



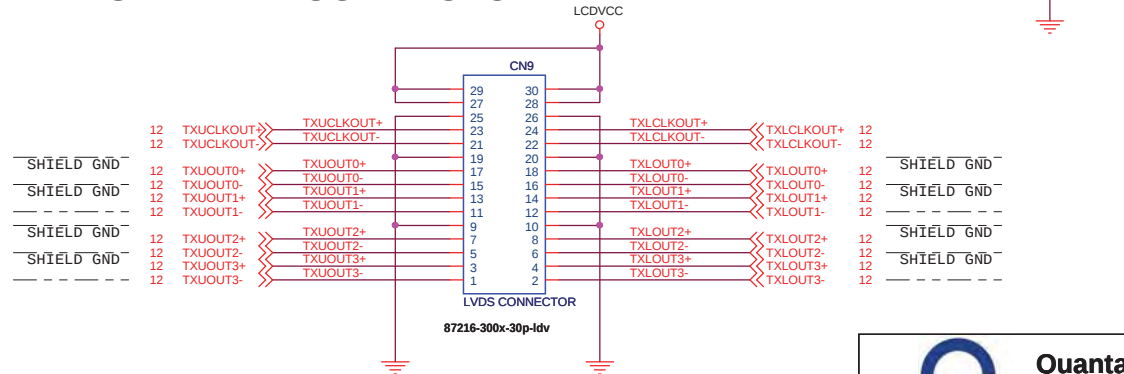
Bypass(default)



Discharge panel power



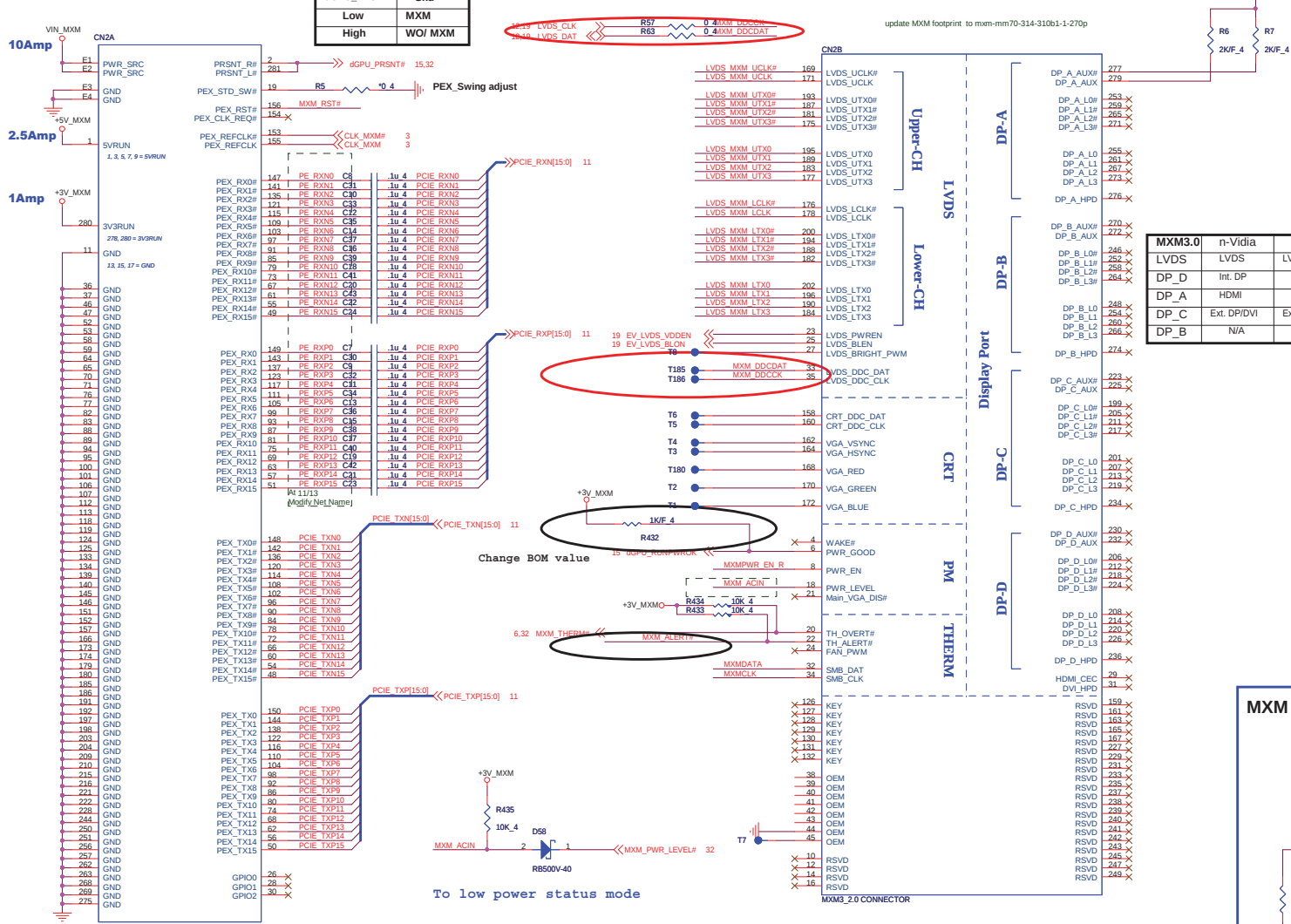
LCD PANEL CONNECTOR



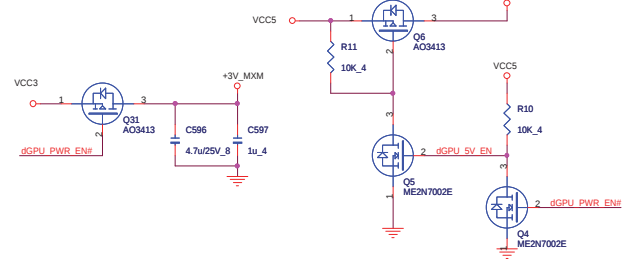
Quanta Computer Inc.

PROJECT : ZN1

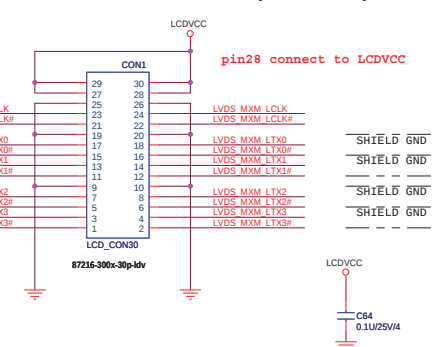
MXM Module



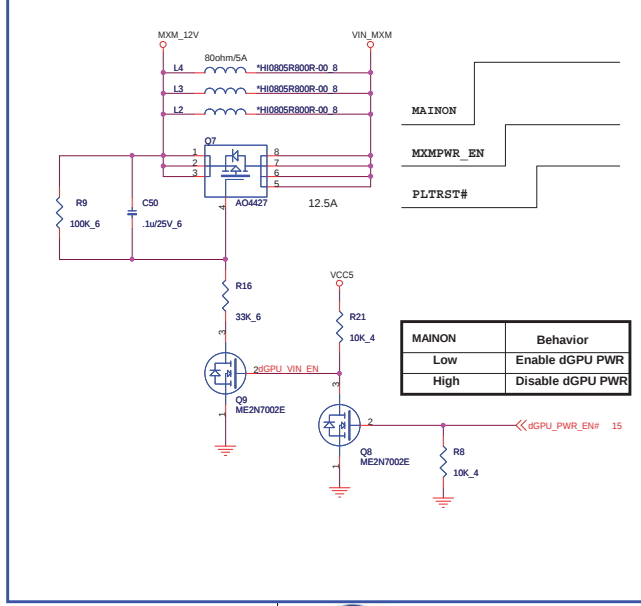
MXM 3V/5V Power switch



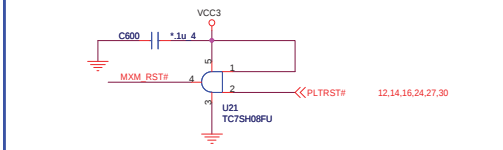
LCD PANEL CONNECTOR(WITH MXM)



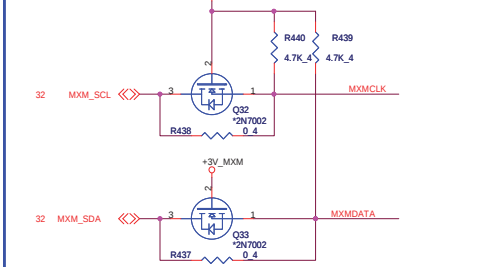
MXM VIN Power switch

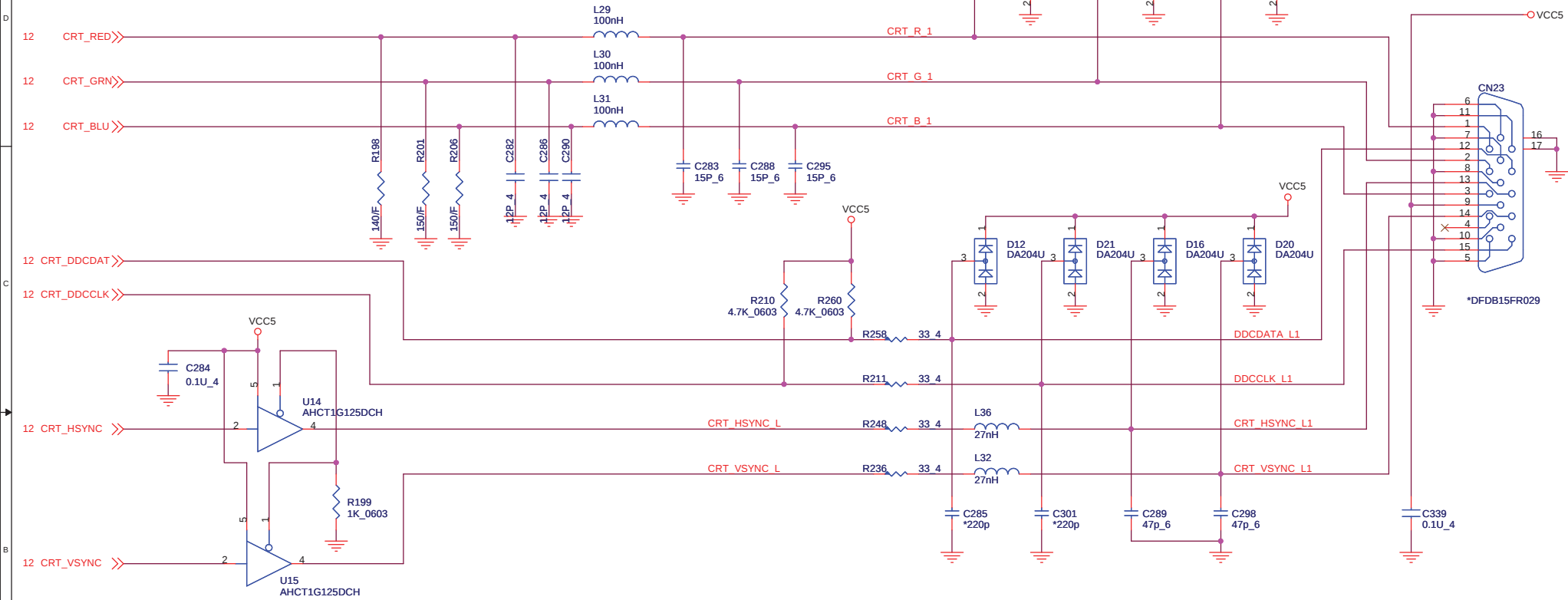


MXM Reset



SMBus



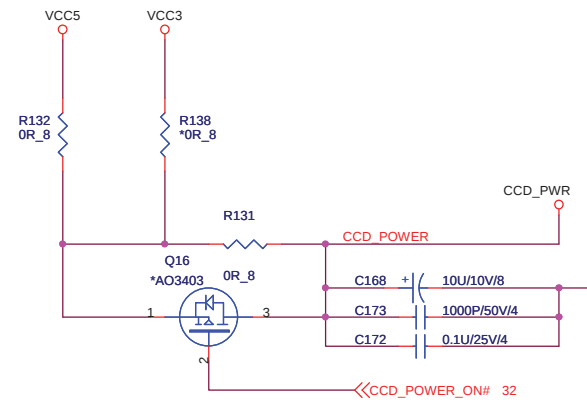


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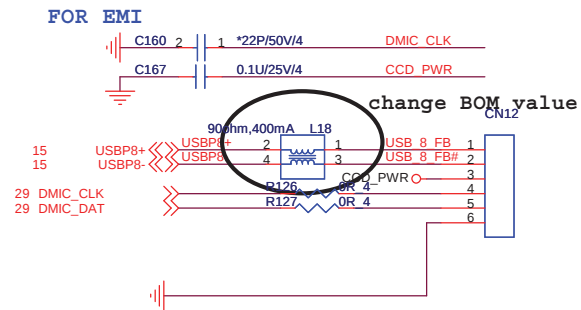
PROJECT : ZN1

Size	Document Number	Rev
	CRT (Reserved for Debug only)	1A
Date:	Friday, May 08, 2009	Sheet 21 of 41

CAMERA POWER CONTROL



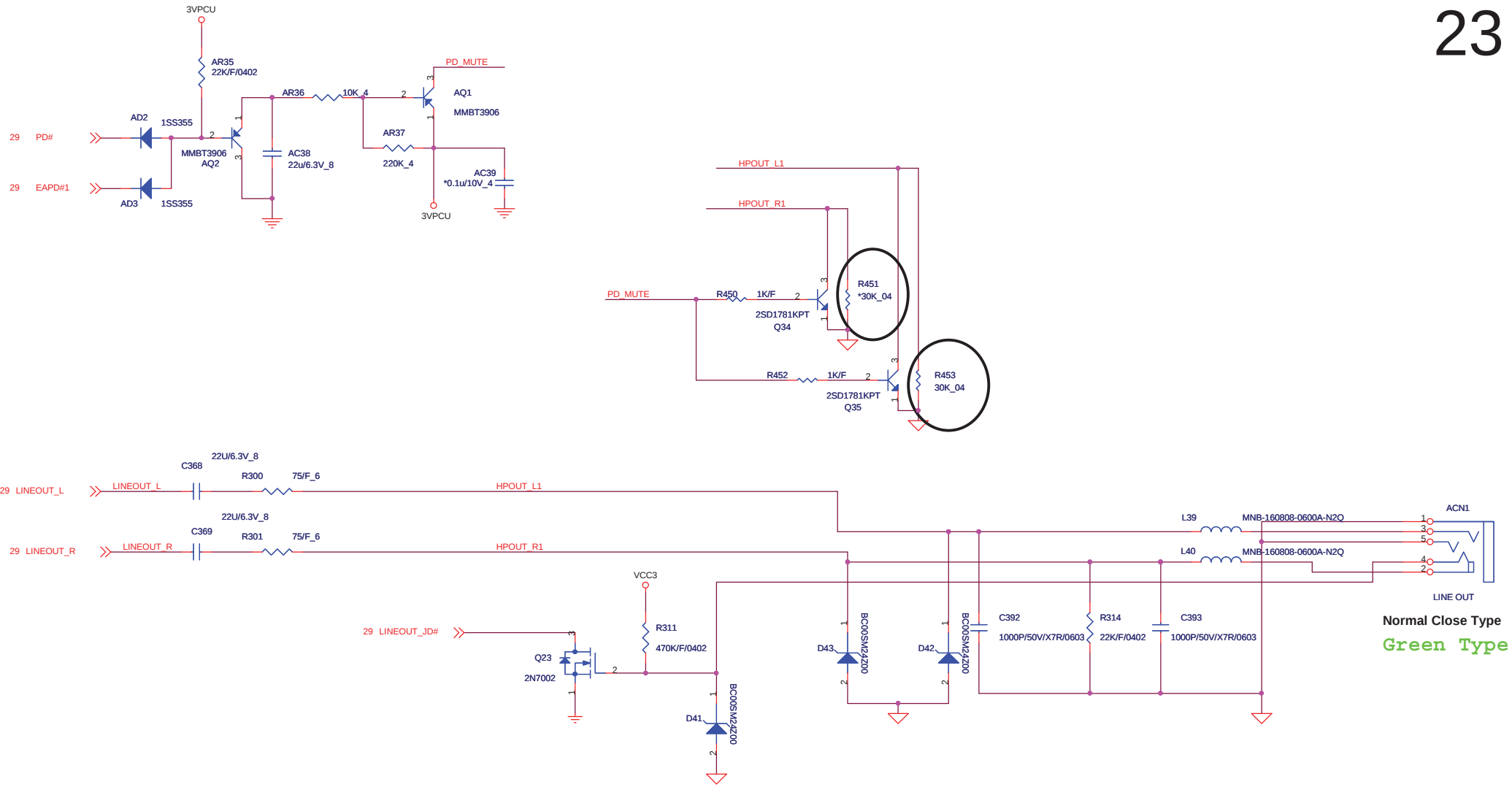
TO WEB CAM MODULE



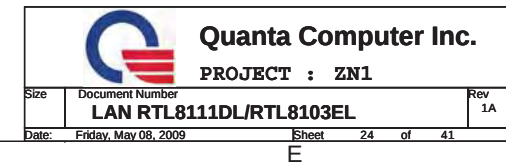
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PROJECT : ZN1

Size	Document Number	Rev
	WEBCAM	1A
Date:	Friday, May 08, 2009	Sheet 22 of 41

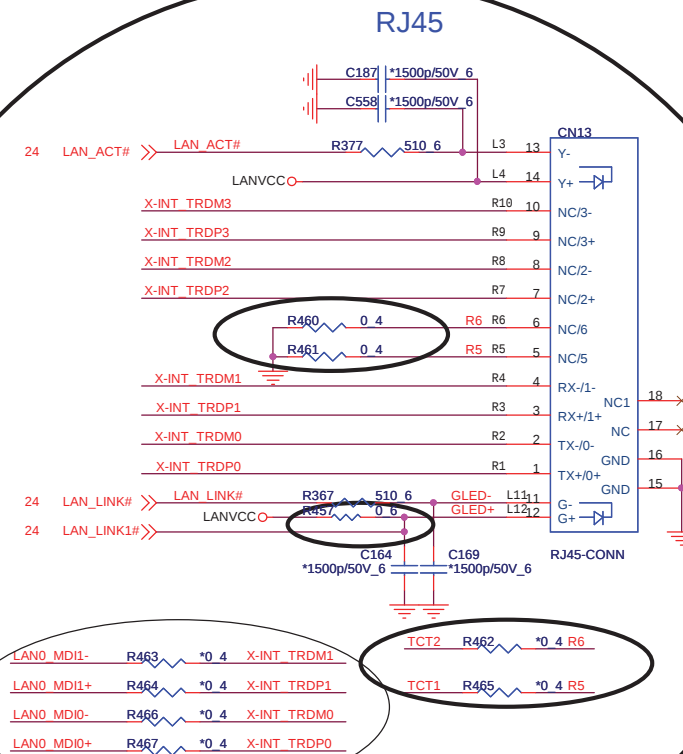
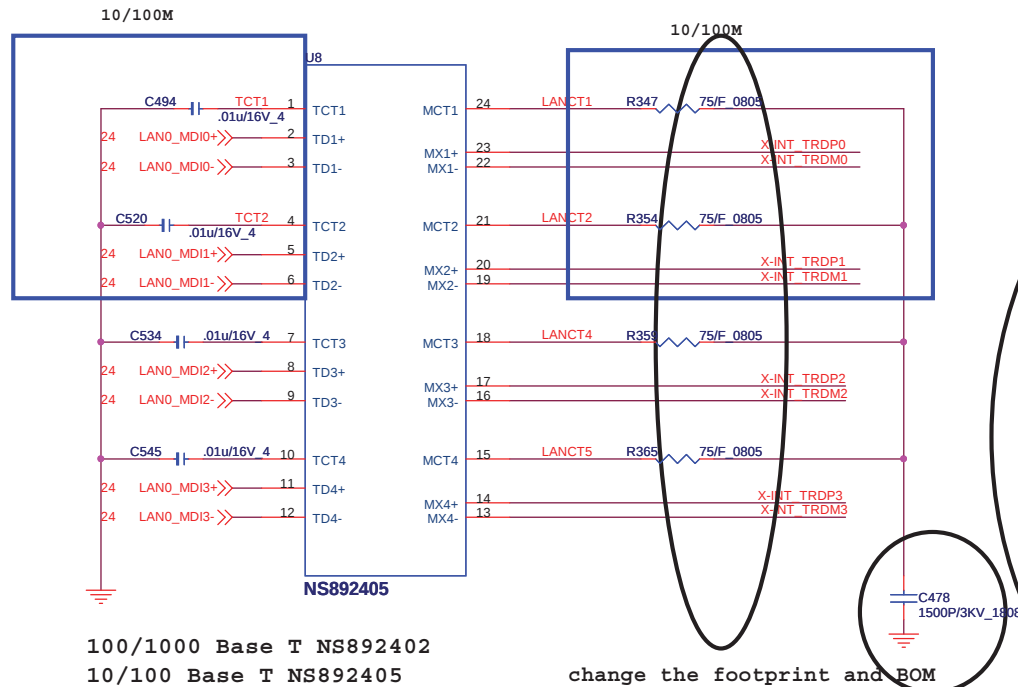


Normal Close Type
Green Type

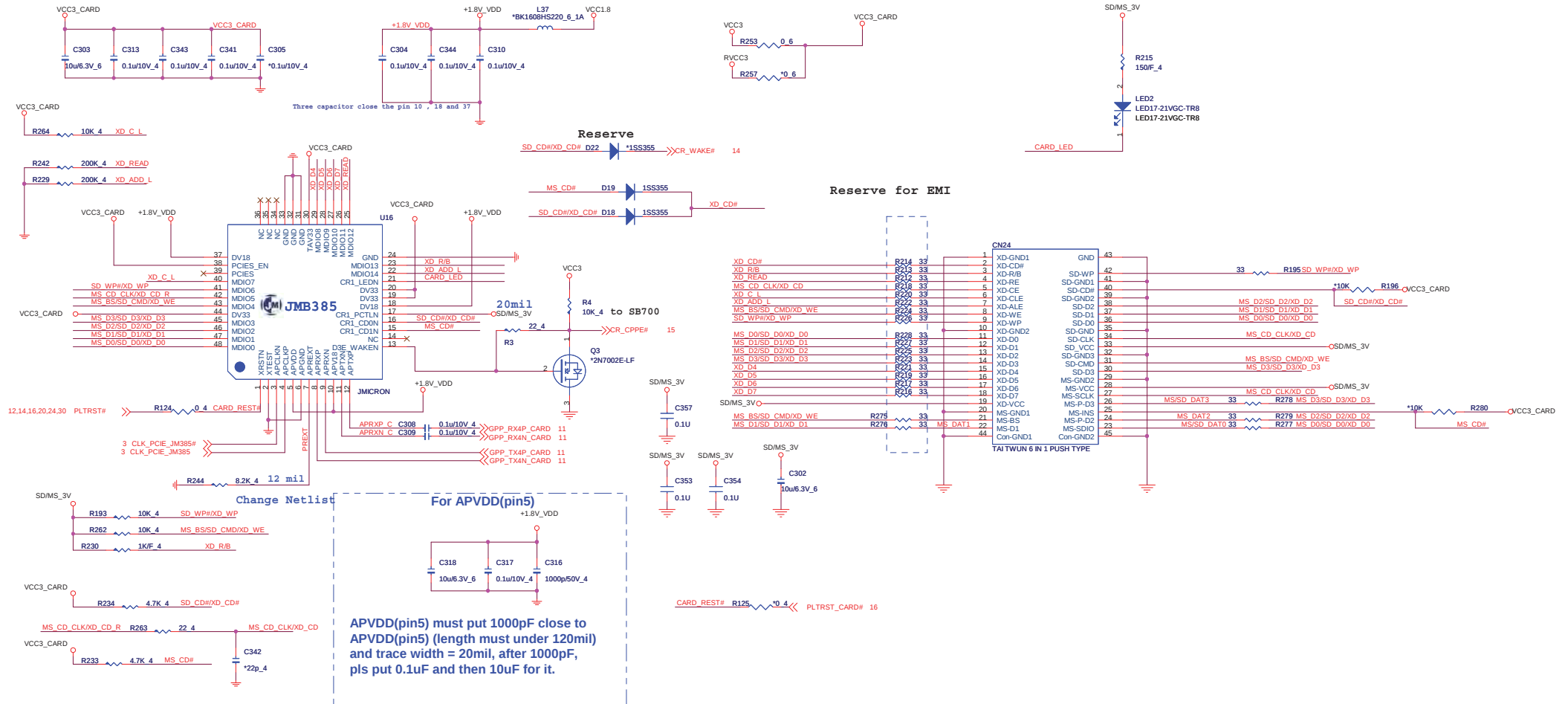


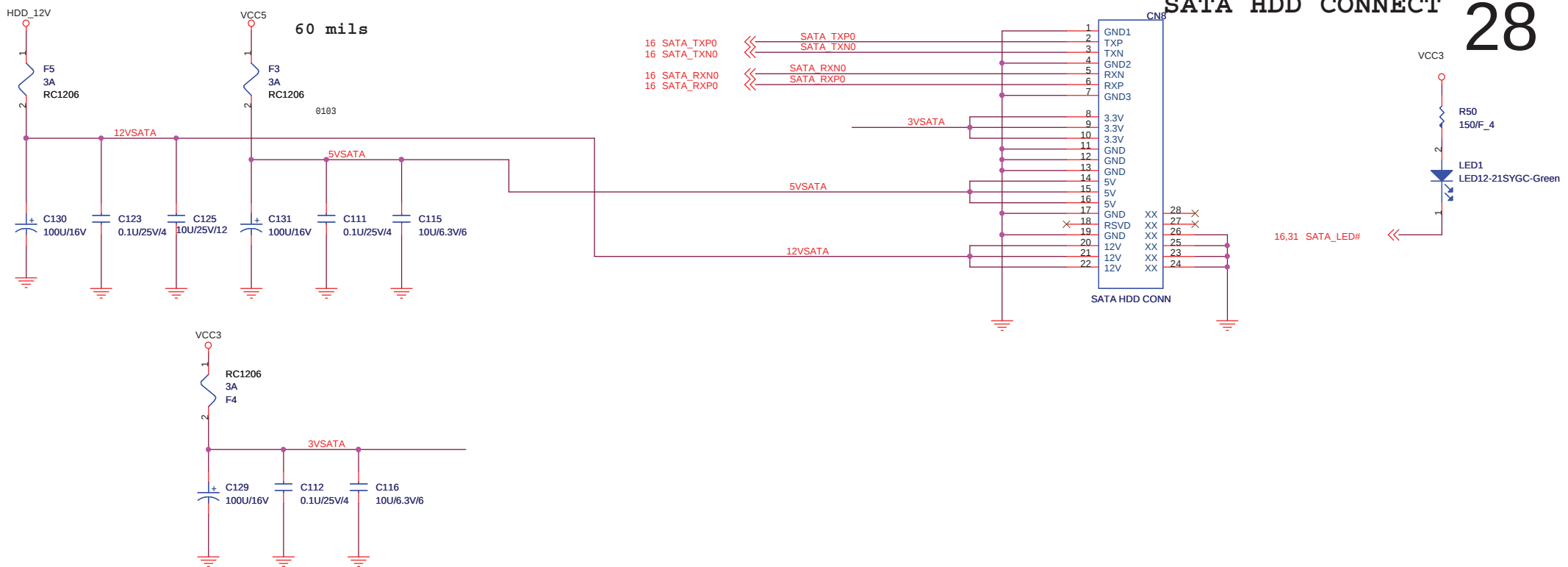
LAN Transformer & WIRE CONN to RJ45

25

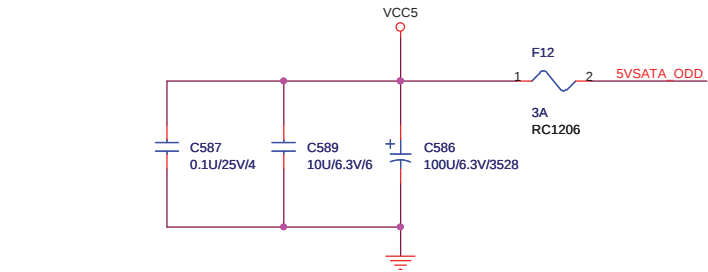


Memory Card Power Supply





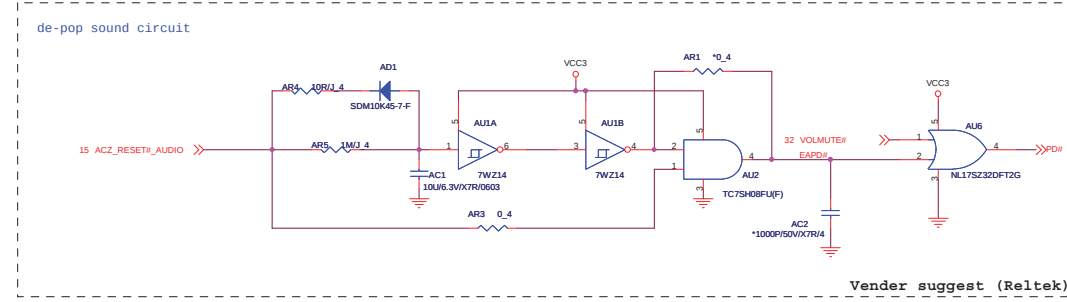
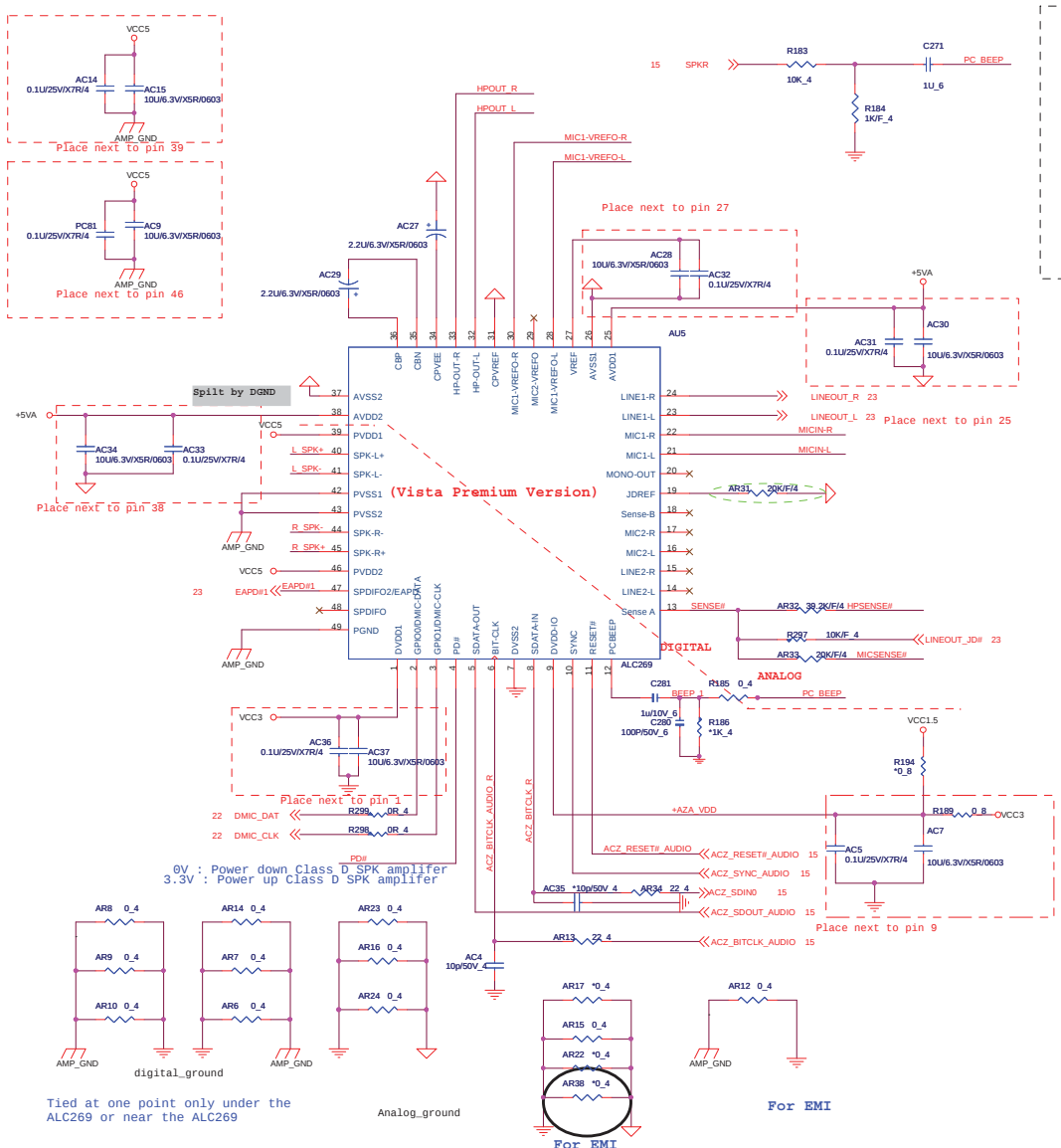
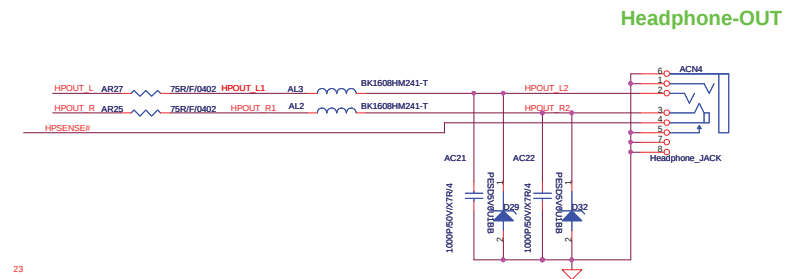
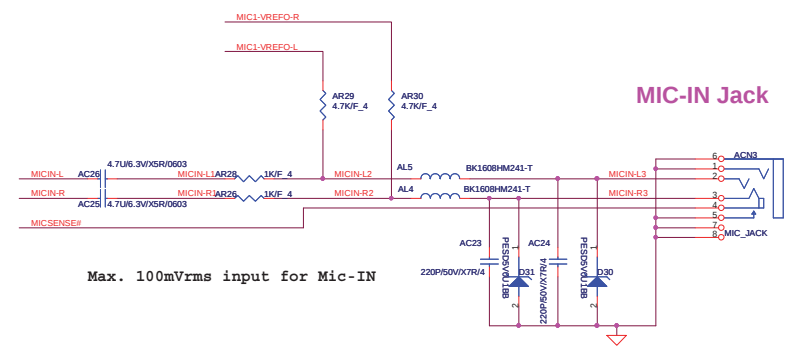
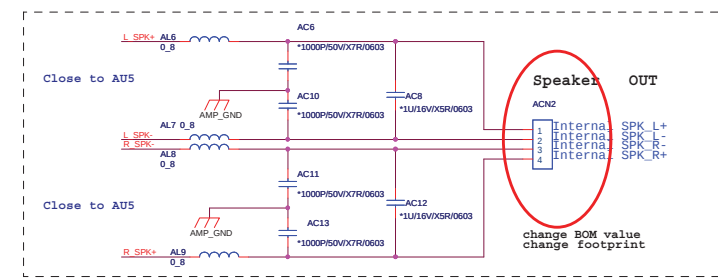
28



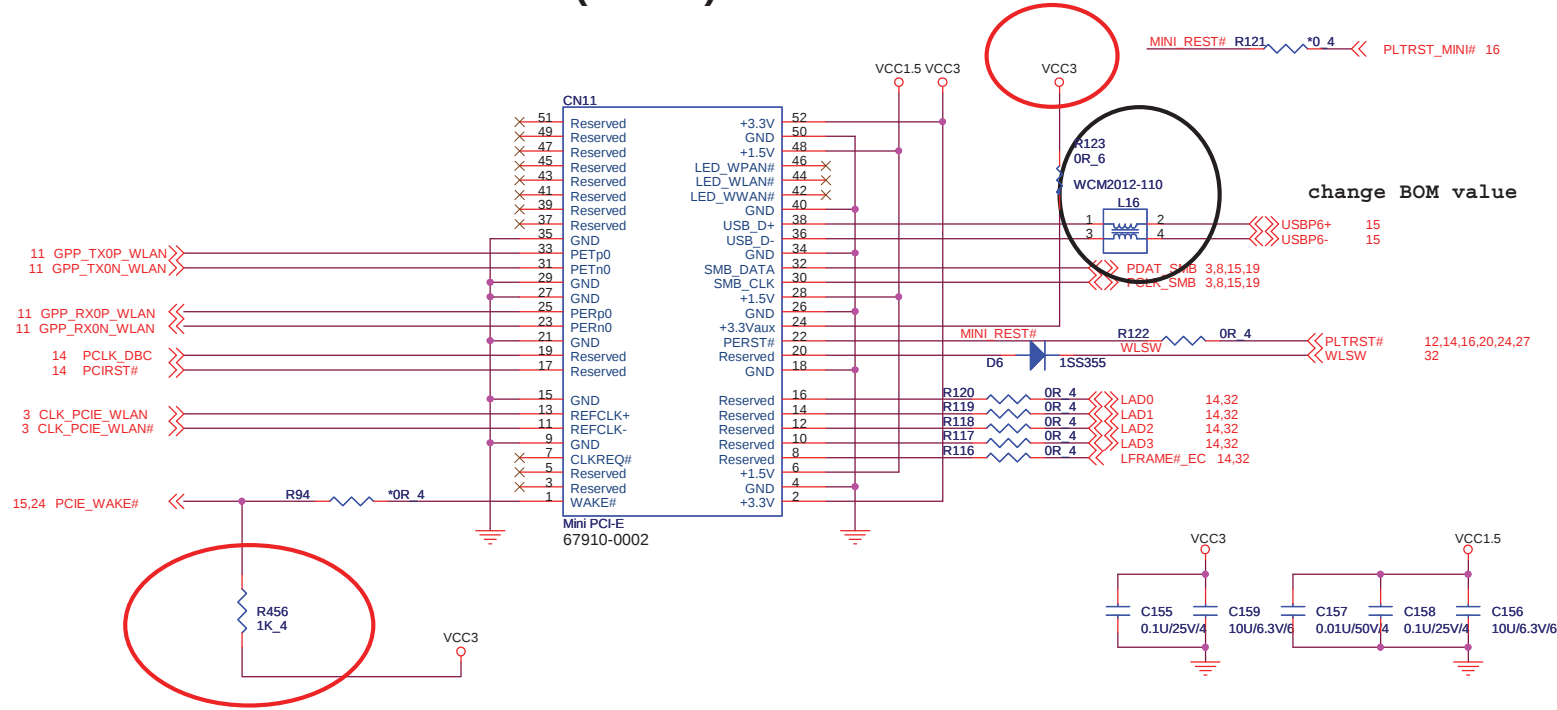


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PROJECT : ZN1

Size	Document Number	Rev
	SATA HDD/ODD	A
Date:	Friday, May 08, 2009	Sheet 28 of 41

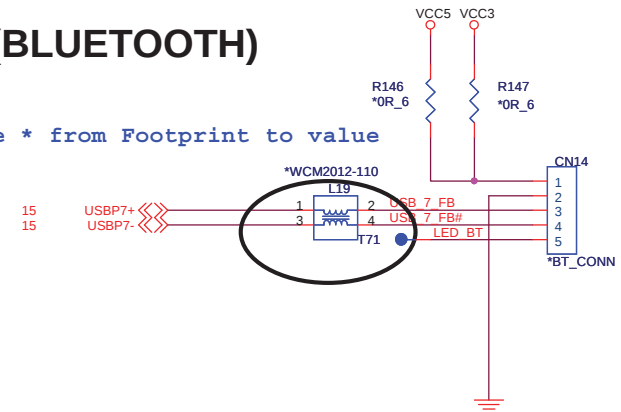


Mini Card (WLAN)

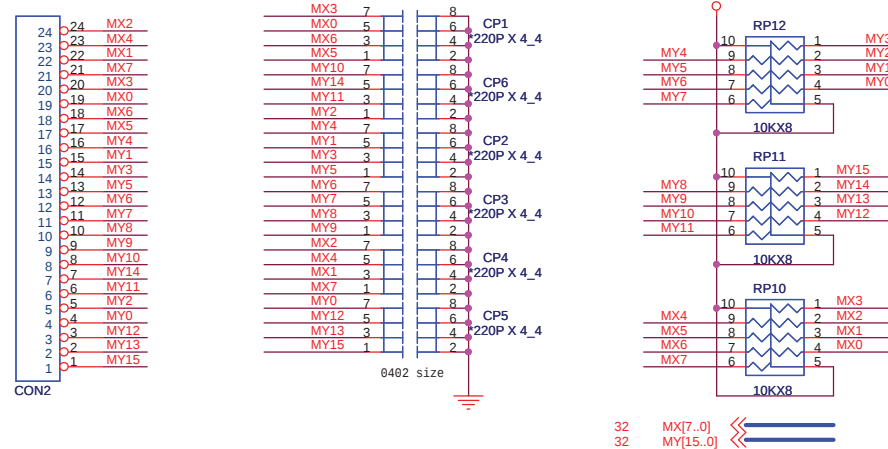


USB(BLUETOOTH)

L19 change * from Footprint to value



88502-2401-24P-L



EC debug port

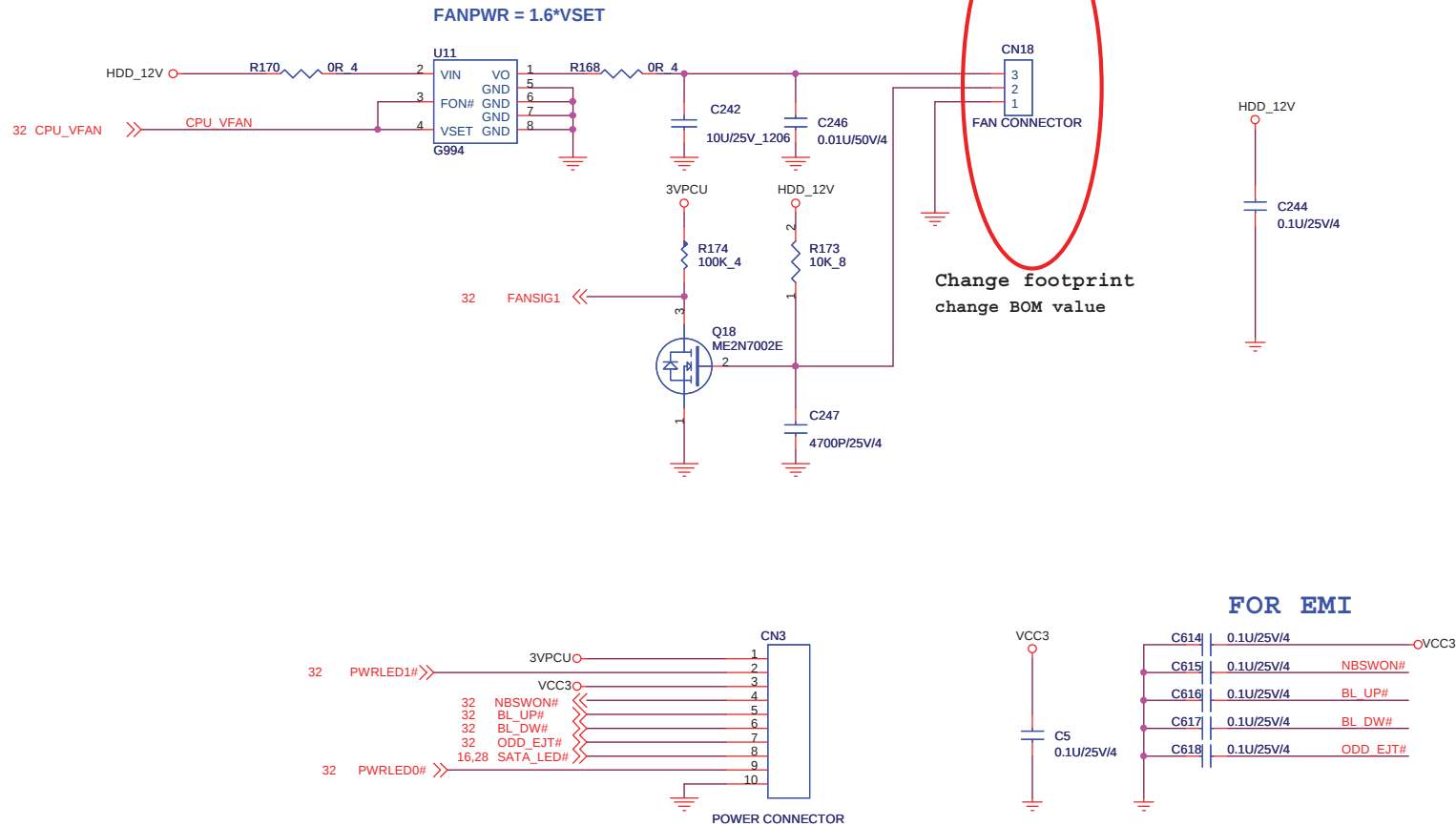


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PROJECT : ZN1

Size	Document Number	Rev
	MINI CARD & BT	A
Date:	Friday, May 08, 2009	Sheet 30 of 41

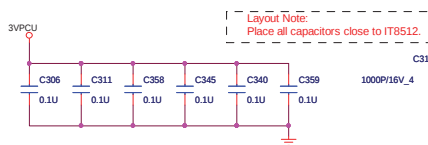
SYSTEM FAN CONN



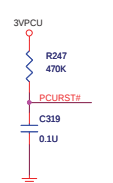
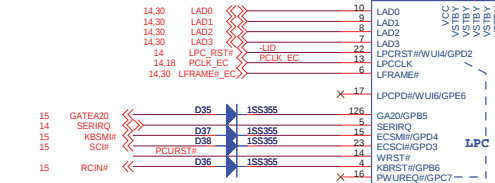
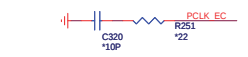
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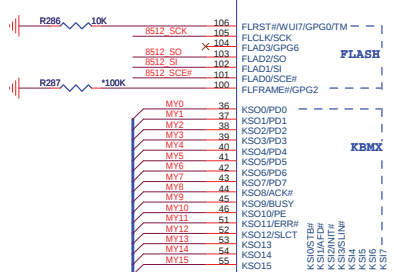


Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

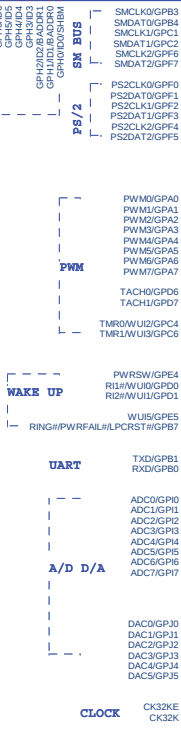


Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below.
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

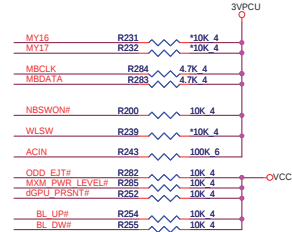


IT8512

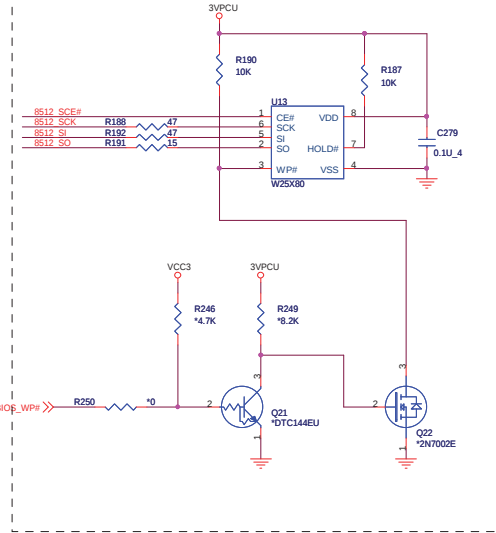


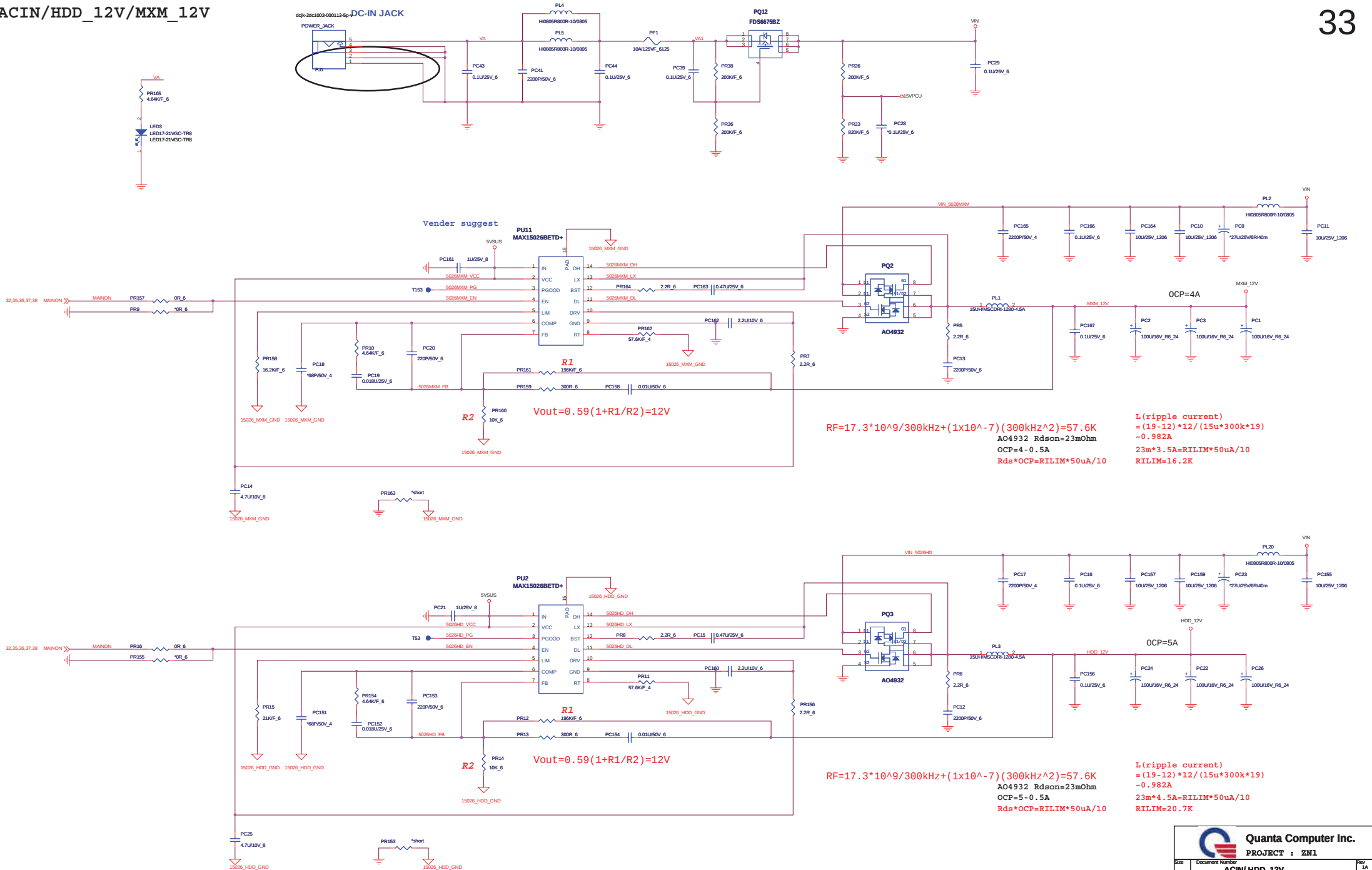
Pull Up for Low Active Pin

SMBUS

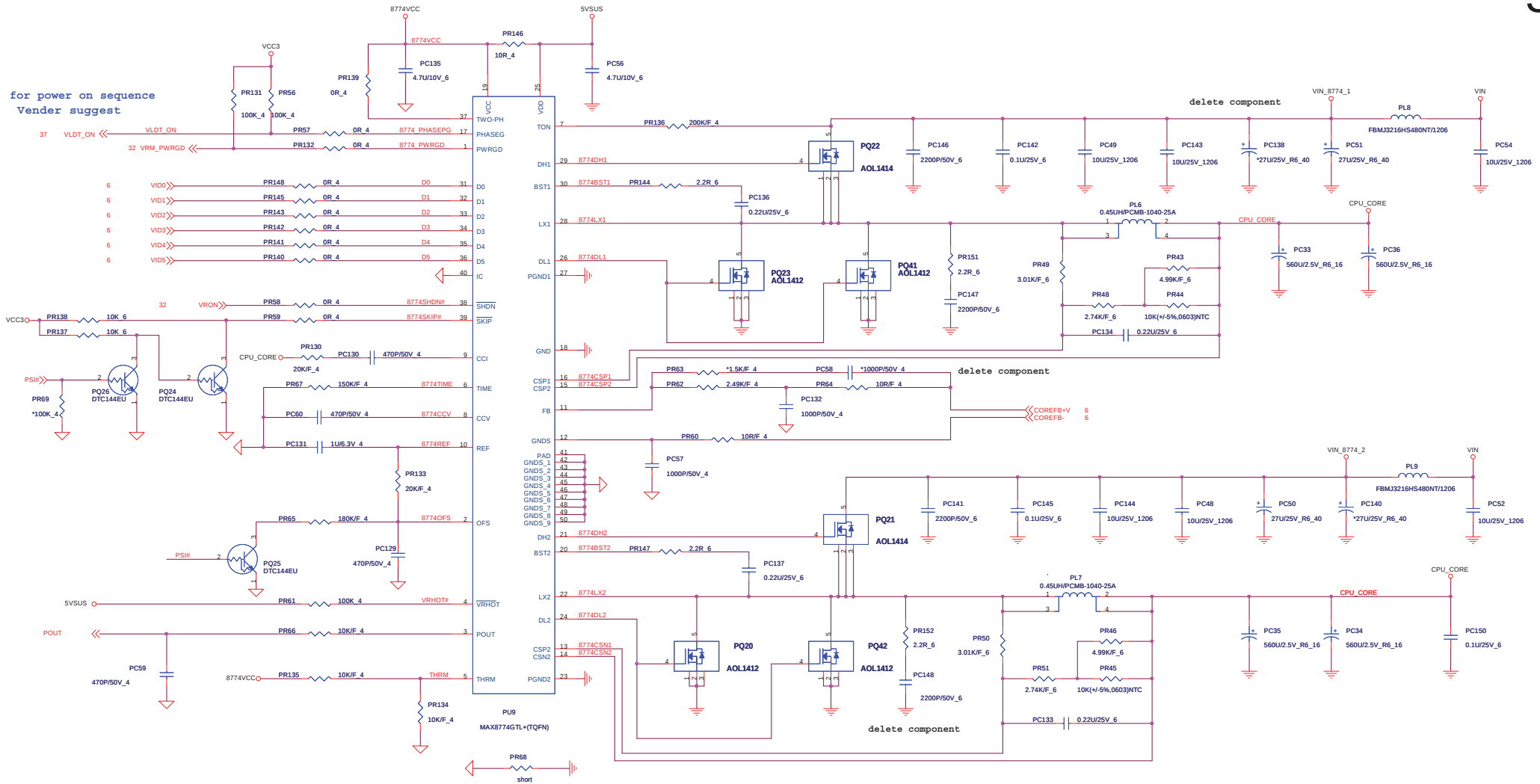


8Mbit , SPI

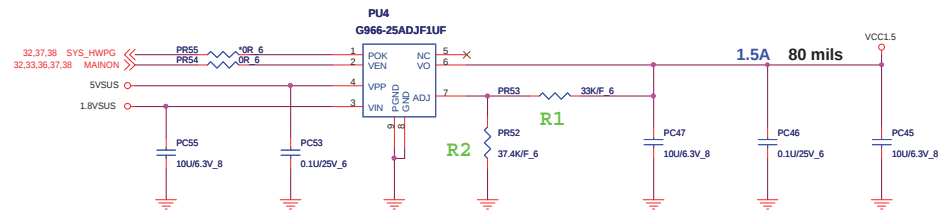
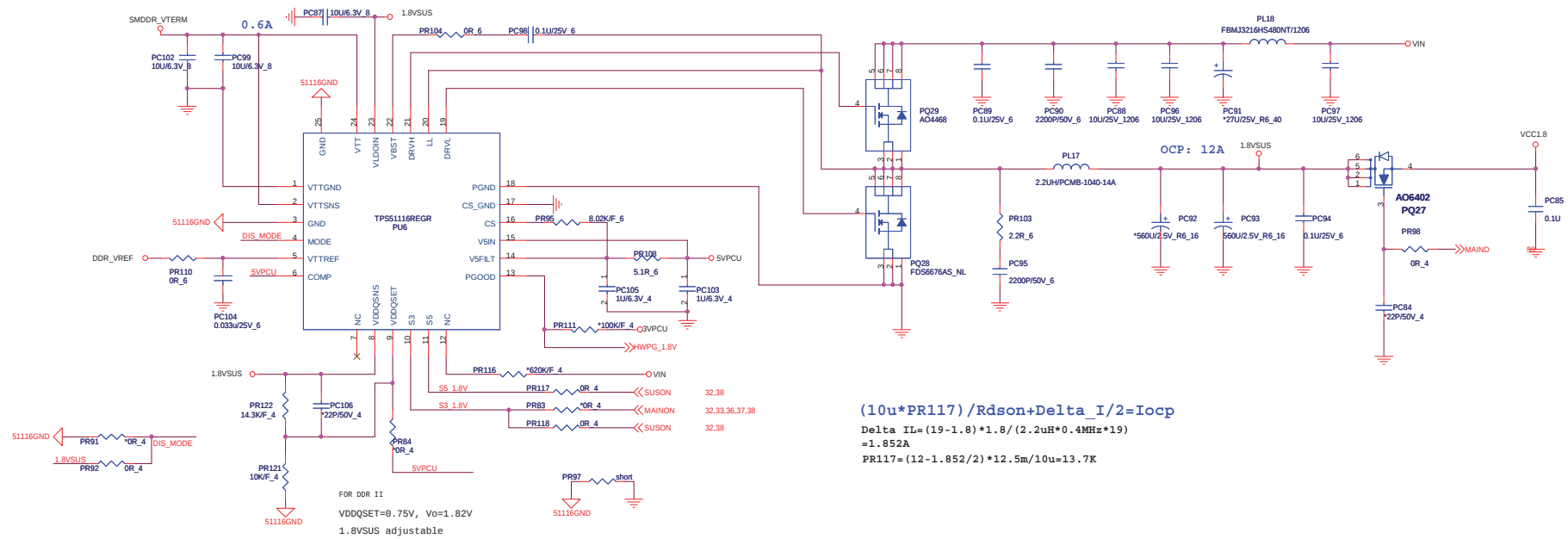


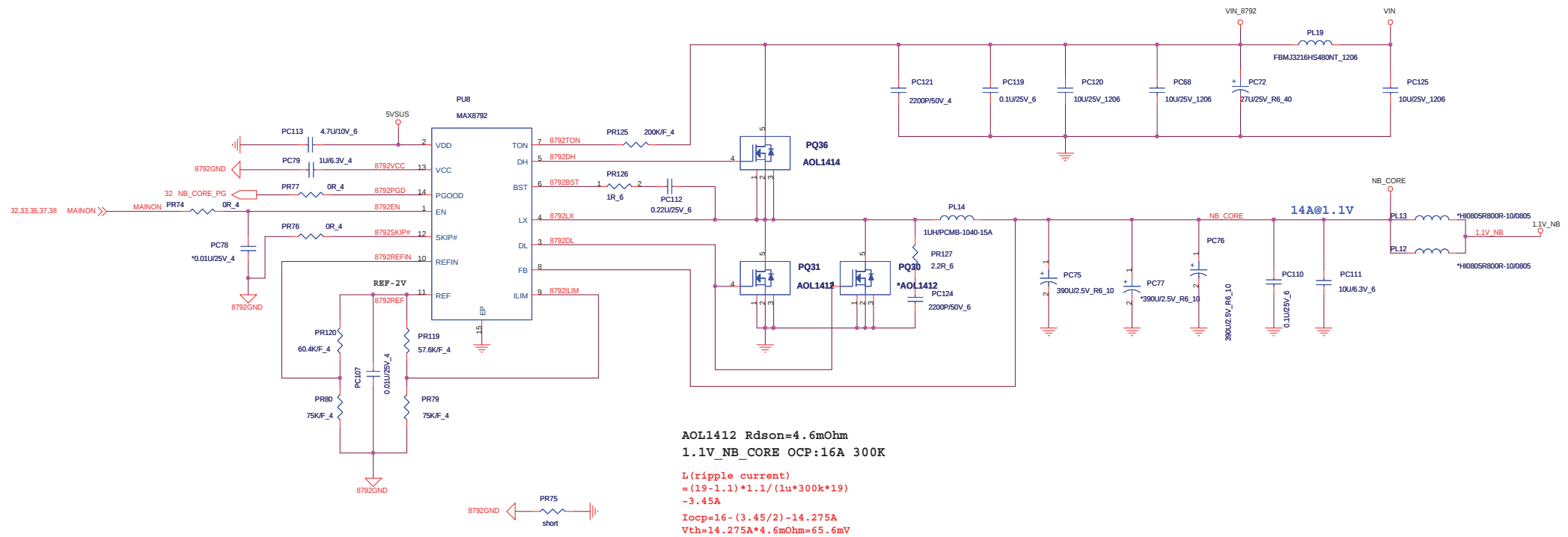


CPU_CORE and CPU_VDDNB_RUN



For AMD AM2 CORE

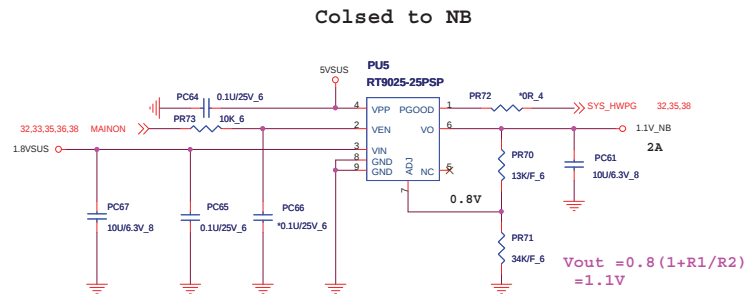
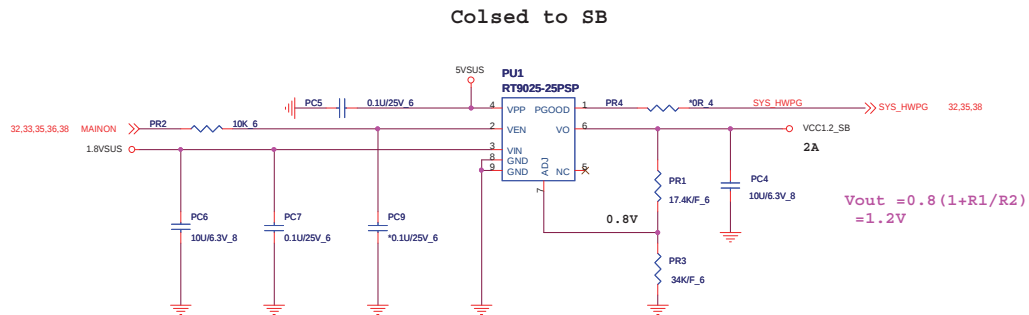
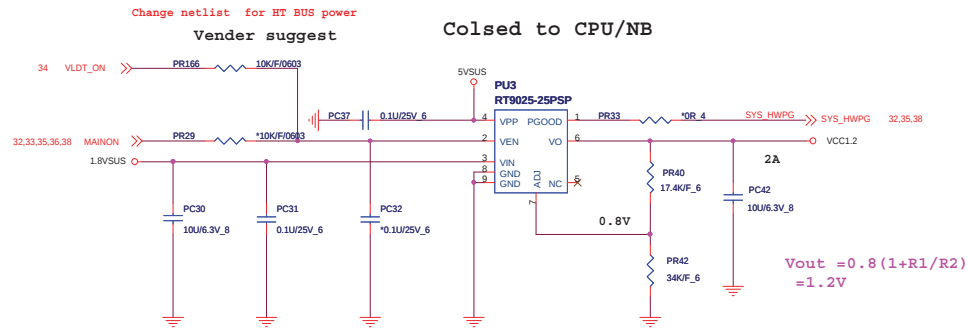


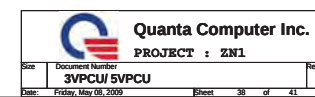


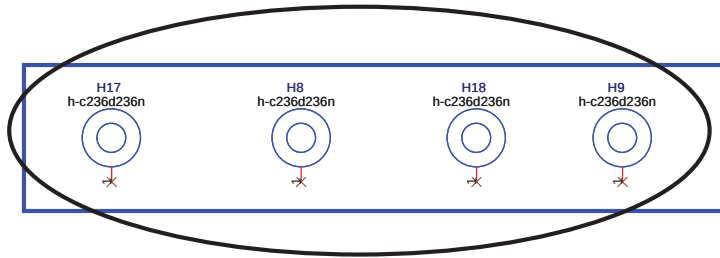
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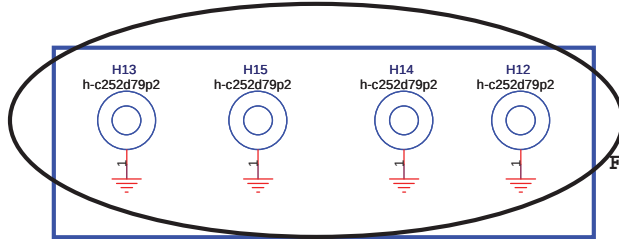
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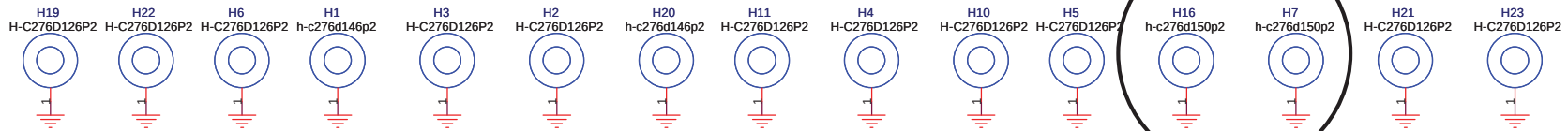




For cpu



For mini card



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DATE	Description	Note	Page
2009 0320	1.change RP1-RP9 to 47 ohm (AMD suggestion)----PAGE 3 2.add R448 10k to VCC3---PAGE 6 3.add R101 300ohm to 1.8VSUS---PAGE 6 4.add R449 10K ohm to VCC3---PAGE12 5.Reserve C612,C613,R441,Y6 to schmatic---page14 6.add D59 and R446 10k to VCC3---page14 7.add R455,C621,C622 to schmatic for EMI---page14 8.add write EDID rom net to control ---page15 9.delete R403 and R32 --page 15 10.change C91,c95 value to 33p---page 16 11.Add 2 short pin for clear cmos and clear password --page16 12.add R86 10k--page 18 13.delete D4,D5 ,C68 component and add R69 0ohm---page18 14.change netlist to SB control (write_edid _rom)and add R62 2.2k ohm--- page19 15.change Q8 control pin to main pin---page 20 16.change MXM reset from pltrst.---page20 17.add ine out mute function---page23 add component ar35,ar36,ar37,ac38,aq1,aq2,ad2,ad3,q34,q35,r450,r452--page23 18.delete Q26,c475 and change LANVCC net to RVCC3 to control ---page24 19.change C447,C448 to 33p---page 24 20.change CN13 footprint for LED pin change---page 25 21.add ESD protect RV17,RV19,RV13,RV15,RV14,RV16, RV18,RV20,RV9,RV10,RV11,RV12---PAGE 26 22.Change CN25,CN26 footprint for ME---page26 23.add D18,D19 for XD detect and change net SD_WP#/XD_WP for SD write protect ---page27 24.change LED2 to Green type---page 27 25.change CN8 to rightangle and change odd connect to vertical type for ME---page 28 26.change au6 to OR-gate from AND-gate for pop sound---page 29 27.change fan control net from Vender suggestion.---page 31 28.add c614--618 0.1u for EMI--- page 31 29.add pr165 ,led3 for power line in ---page33 30.change VLDT_ON net for power on sequence--PAGE 34 31.change pr137,pr138 type to BOM---page 34 33.LED RT value need to change	B2B	

[illegible]