ZRL BLOCK DIAGRAM

VER : 1A	
BOM P/N	Description
31ZRLMB0000	ZRL MB ASSY(UMA,HR,DC)W/O CPU
31ZRLMB0010	ZRL MB(UMA,HR,DC,SURGE)W/O CPU

CHARGER ISL88731 P27

3/5V SYS PWR RT8223M P28

CPU CORE PWR ISL95835 P29

CPU +1.05V_VTT RT8238A P30

+1.8V HPA00835RTER P33

DDR3 +1.5_SUS RT8207A P31

discharger P33

+VCCSA RT8241DZ P32

Thermal protect P33

intel <MCH Processor>

SandyBridge DC 35W

PCI-E X16

rPGA 988 (37.5mm X 37.5mm)

DDR SYSTEM MEMORY

FDI CLK DMI

P4~P7

5GT/s

DDR III - SODIMM 0
DDR III - SODIMM 1
P14, 15

Dual Channel DDR III *1066 MHz*

FDI interface *2.7GT/s*

X4 DMI interface *5GT/s*

intel <PCH>

FDI CLK DMI

SATA Gen3

SATA Gen2

iGFX Interfaces

CougarPoint 0.7

PCI-E

USB

HDA

mBGA 989 (25mm X 25mm)

Note:
HM65 not support USB 6 & 7
HM65 not support SATA 2 & 3

RTC P9

P8~P13

SPI

LPC

HDD (SATA) P20 — SATA0

ODD (SATA) P20 — SATA1

USB 2.0 * 3 USB1,3,9 P24 — USB 2.0

Bluetooth USB4 P24

CCD (Camera) USB8 P16

Card Reader USB12 P23

Azalia

X'TAL 32.768KHz

X'TAL 25MHz

INT_CRT → **CRT** P16

INT_LVDS → **LVDS** P16

INT_HDMI → **HDMI** P17

PCI-Express Gen2 *5GT/s*

PCIE-6 → USB-13 → **MINI CARD WLAN** P19

PCIE-1 → **ATHEROS AR8158 10/100 LAN** P18 → **RJ45** P18

X'TAL 25MHz

Audio CODEC REALTEK ALC271X P21

Dual SPI ROM 4MB x1 (Basic ME+Braidwood) P9

WPCE791/FLASH NPCE971 P26

HP Jack P22

MIC Jack P22

SPK P21

DMIC P21

SPI ROM P26

Touch Pad P25

Keyboard P25

Fan Driver (DA Type) P25

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PROJECT : ZRL

Size	Document Number	Rev
	Block Diagram	1A

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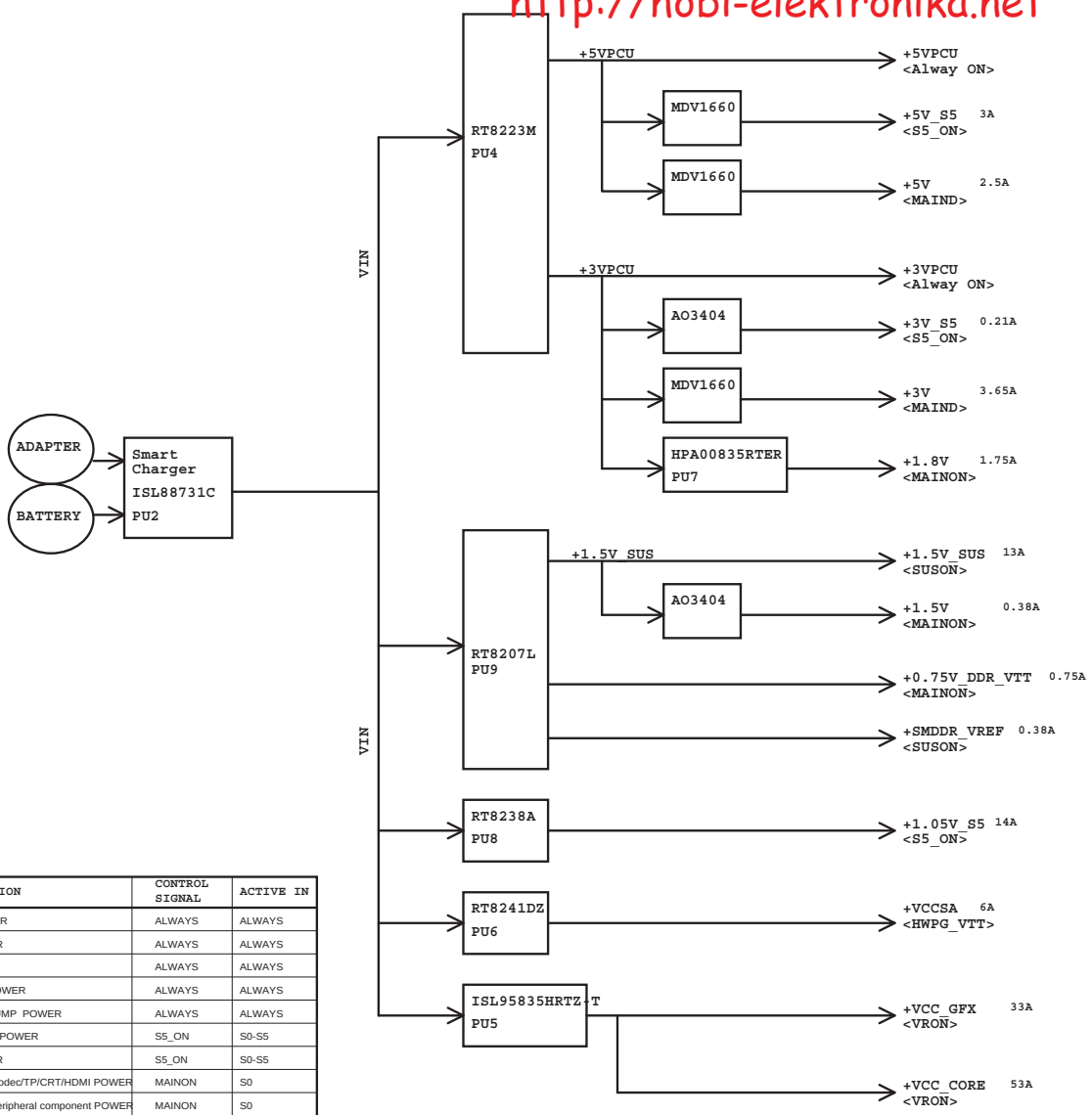
ZRL power tree



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Quanta Computer Inc.
PROJECT : ZRL
Size | Document Number: PWR Status & GPU PWR CRL & THRM | Rev 1A
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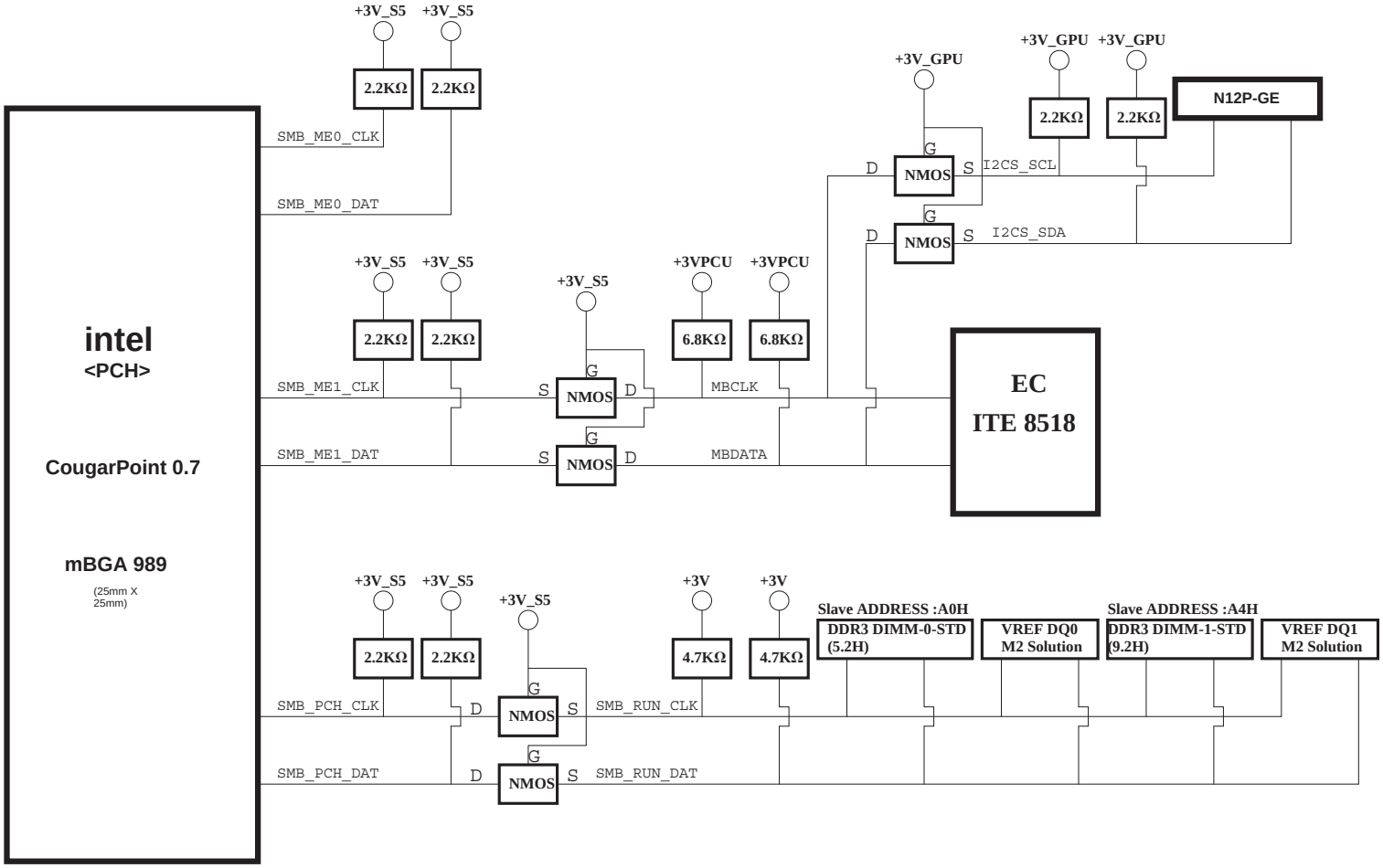


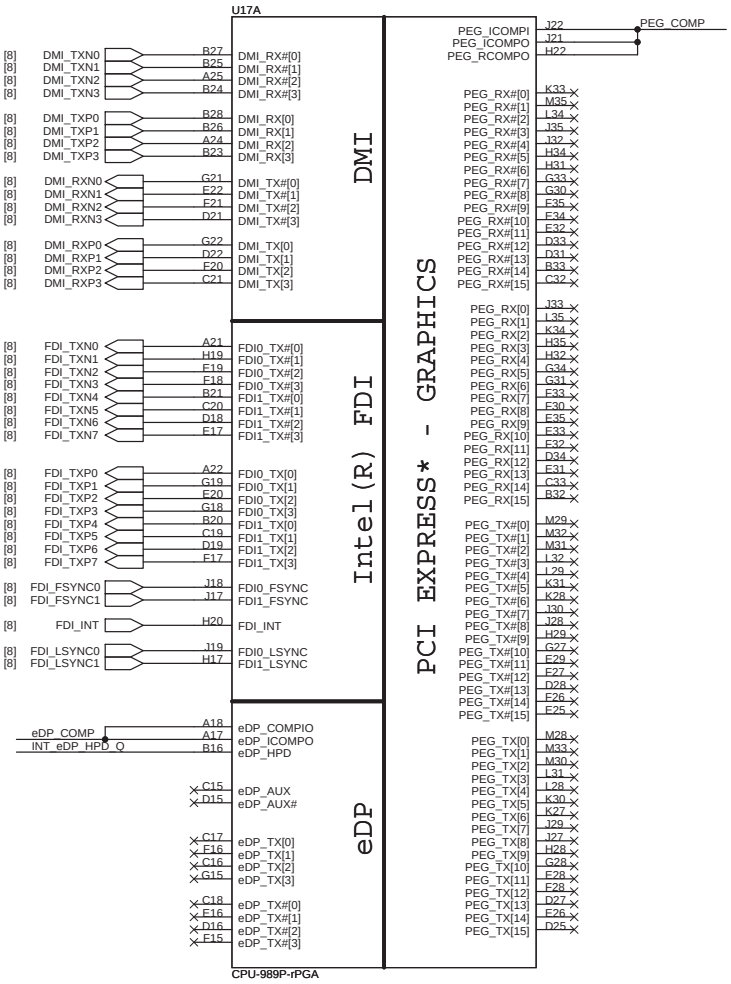
Quanta Computer Inc.
PROJECT : ZRL

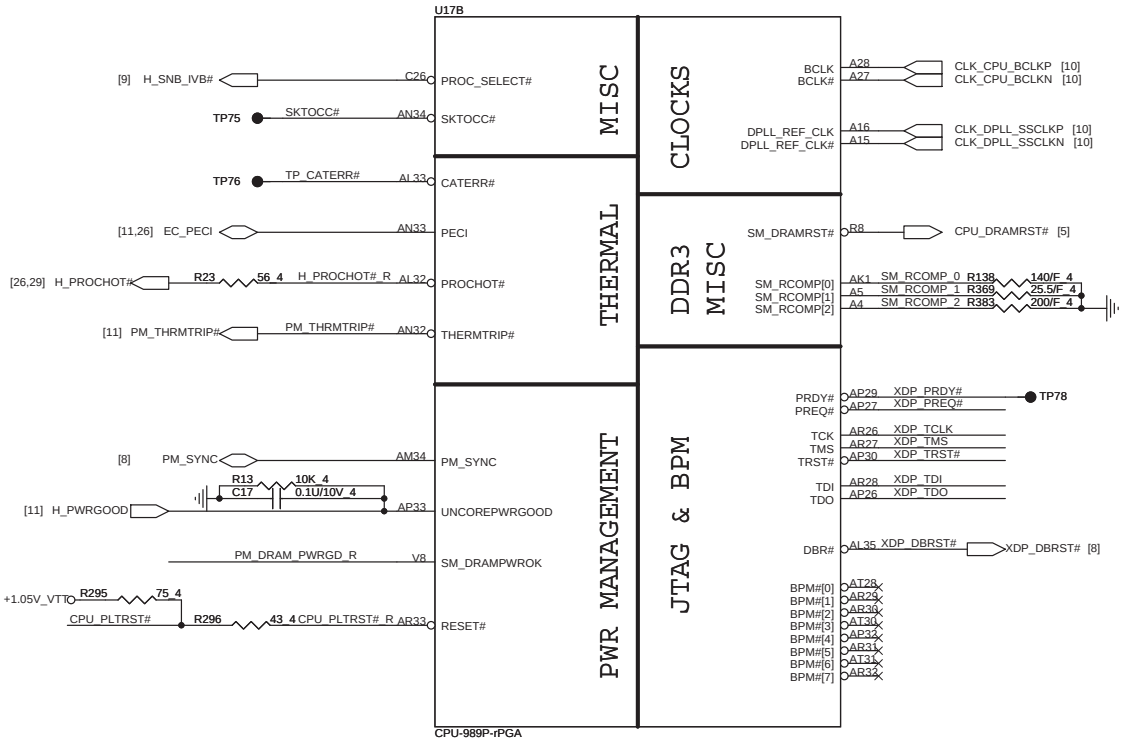
Size	Document Number	Rev
	SMBus Address	1A

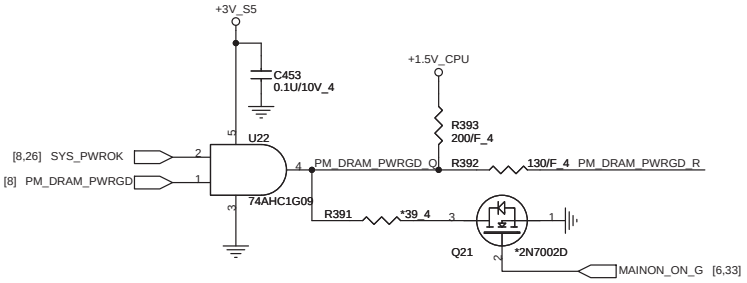
Date: Tuesday, June 21, 2011 Sheet 3 of 34

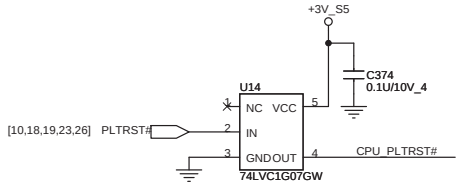
Sandy Bridge Processor (DMI,PEG,FDI)

Sandy Bridge Processor (CLK,MISC,JTAG)

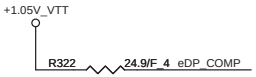




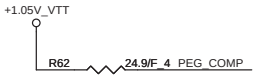




DP & PEG Compensation



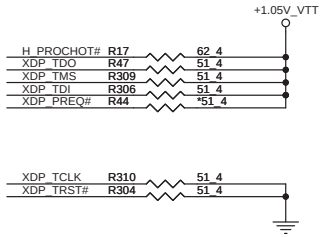
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

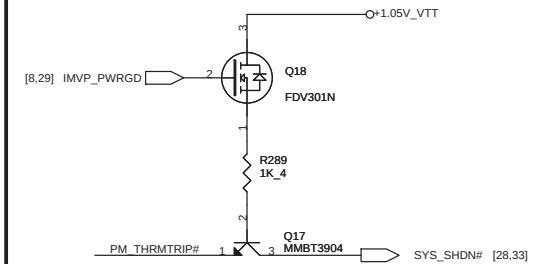


PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms

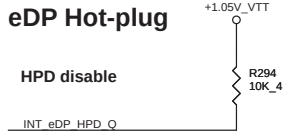
PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up(CPU)





eDP Hot-plug



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Size	Document Number	Rev
	Sandy Bridge 1/4	1A
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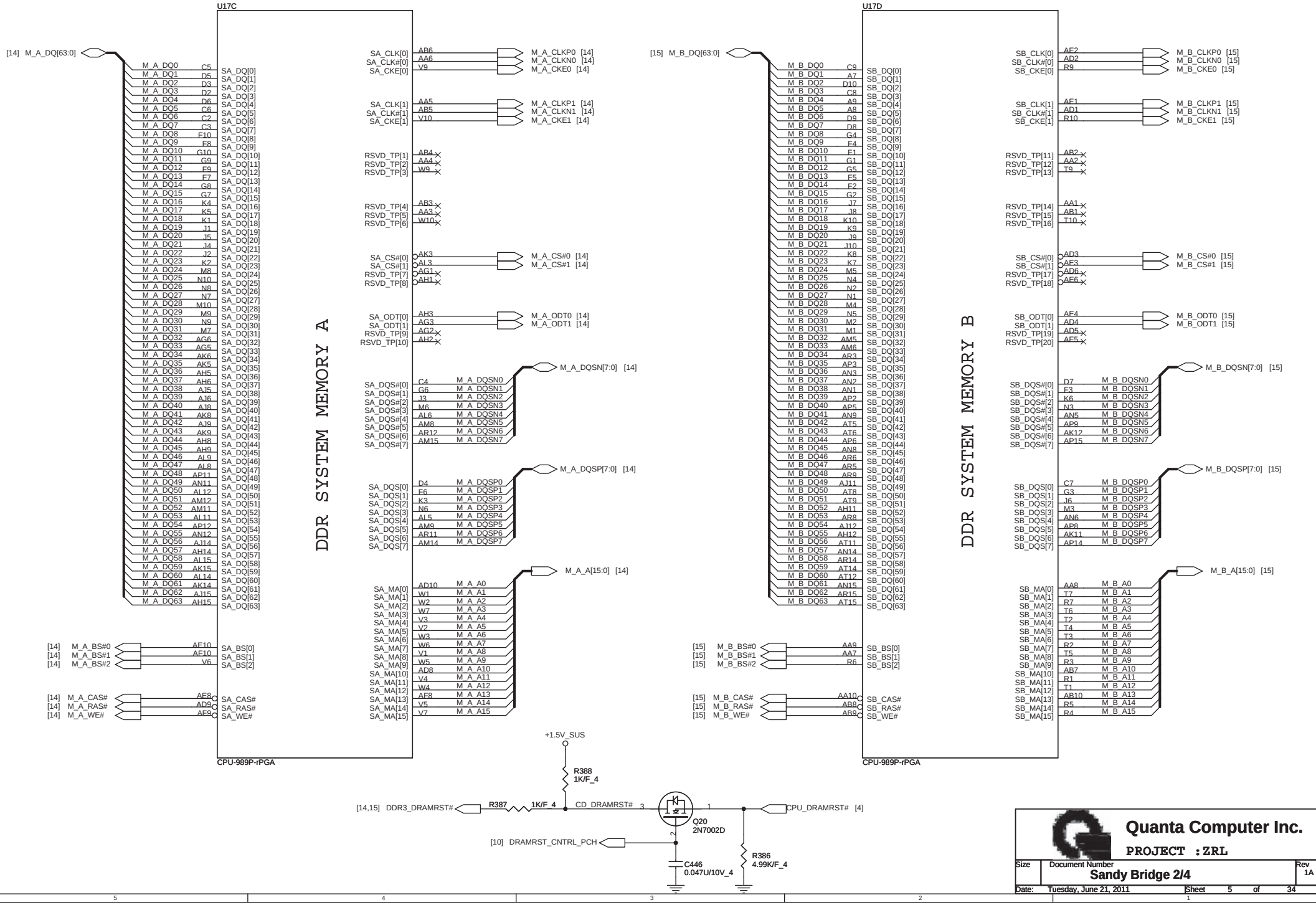
Sandy Bridge Processor (DDR3)



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	Sandy Bridge 2/4	1A
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Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

06

CPU VTT

SNB 45W:8.5A

Spec

330uF/6mohm x 2

22uF x 12

22uF x 7 (Non-stuff)

CPU Core Power

SNB 45W:52A

Spec

470uF/4mohm x 4

22uF x 16

10uF x 10

CPU VGT

SNB 45W:21.5A

Spec

470uF/4mohm x 2

22uF x 12

CPU VCCPL

SNB 45W:1.5A

Spec

330uF/7mohm x 1

10uF x 1

1uF x 2

CPU MCH

SNB 45W: 5A

Spec

330uF/6mohm x 1

10uF x 6

Real

10uF x 6

CPU SA

SNB 45W: 6A

Spec

330uF/7mohm x 1

10uF x 3

Layout note: need routing together and ALERT need between CLK and DATA

Place PU resistor close to CPU

Place PU resistor close to CPU

SVID CLK

SVID DATA

SVID ALERT

4.5A

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PROJECT : ZRL

Size: Document Number: Sandy Bridge 3/4 Rev: 1A

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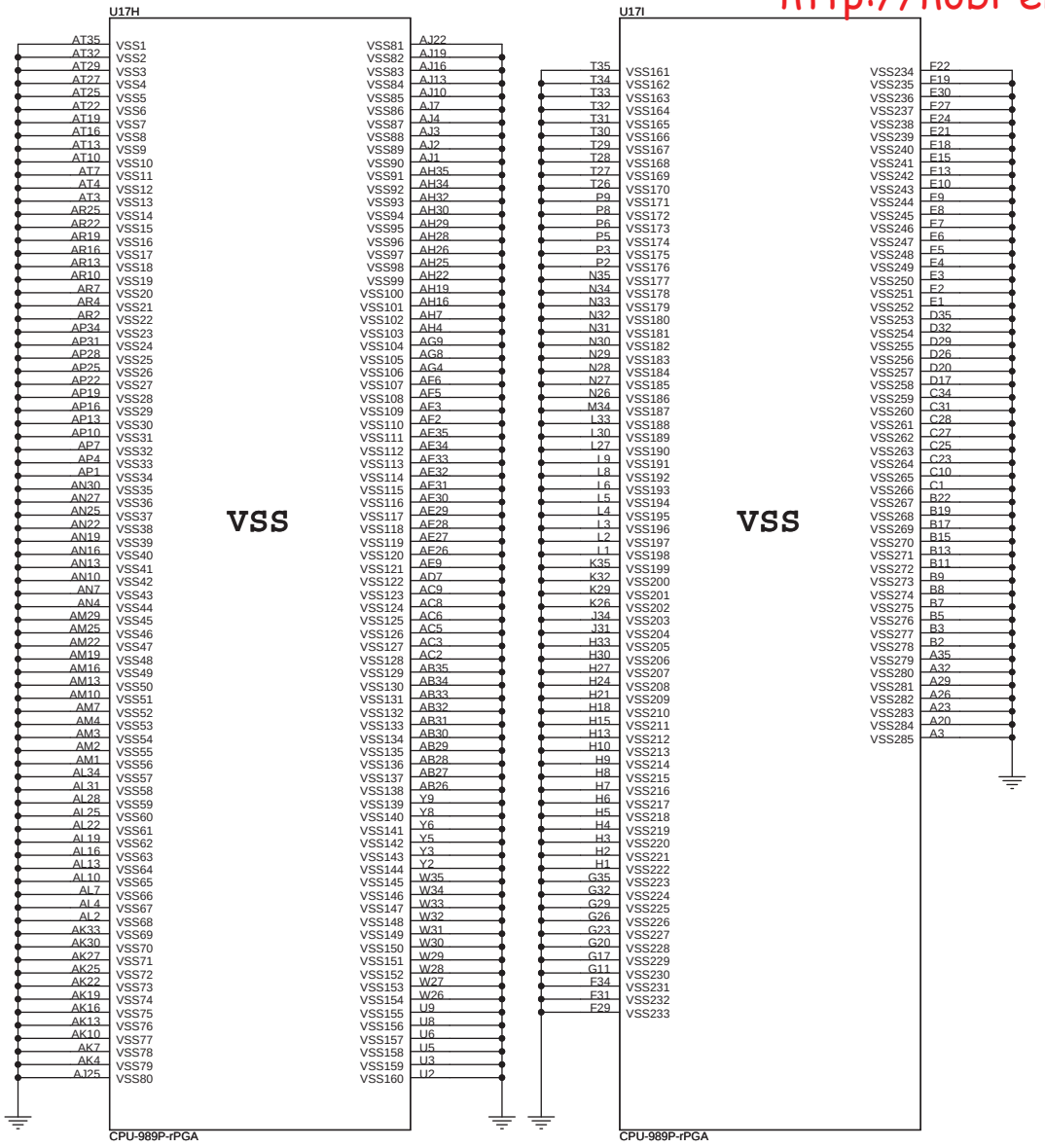
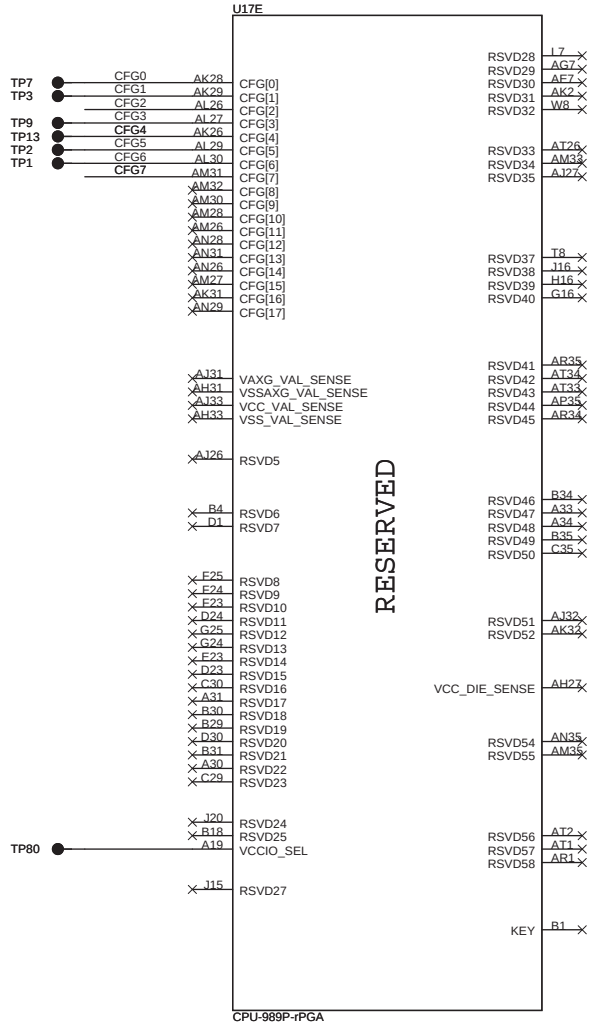
Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)

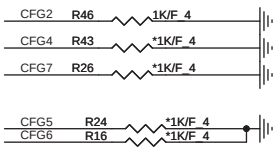
07



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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	Sandy Bridge 4/4	1A
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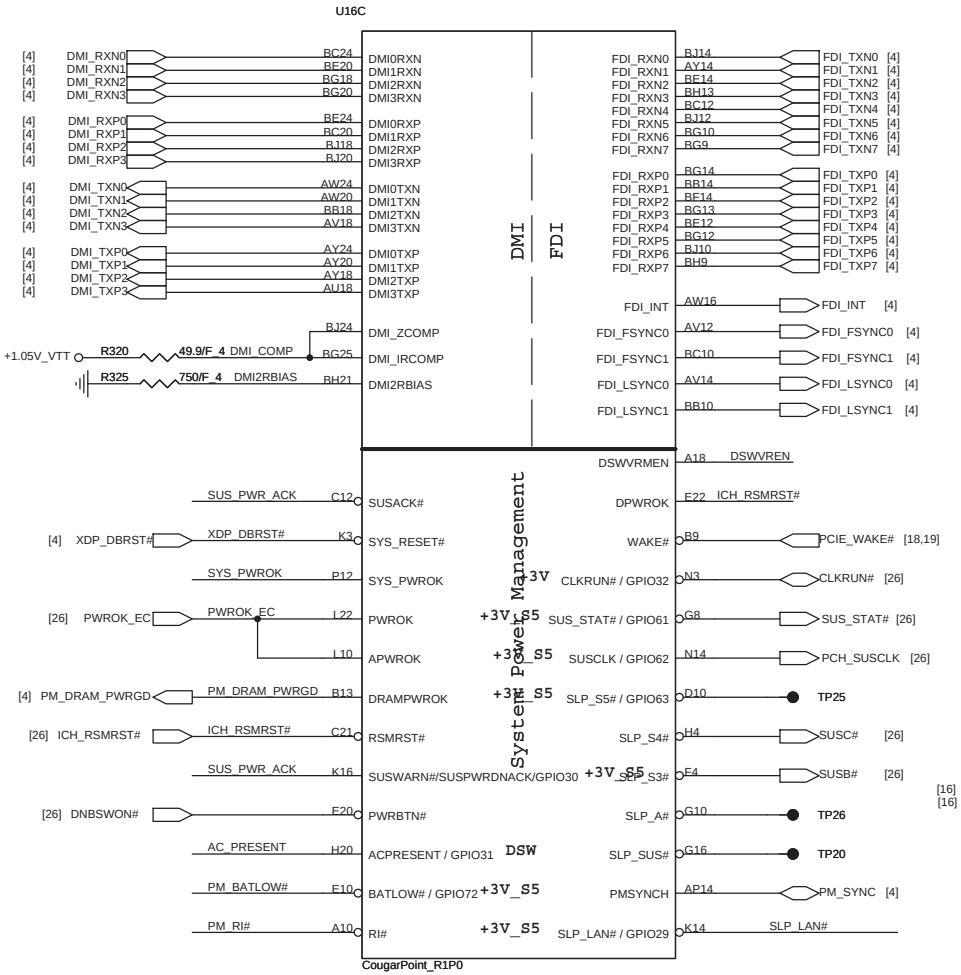
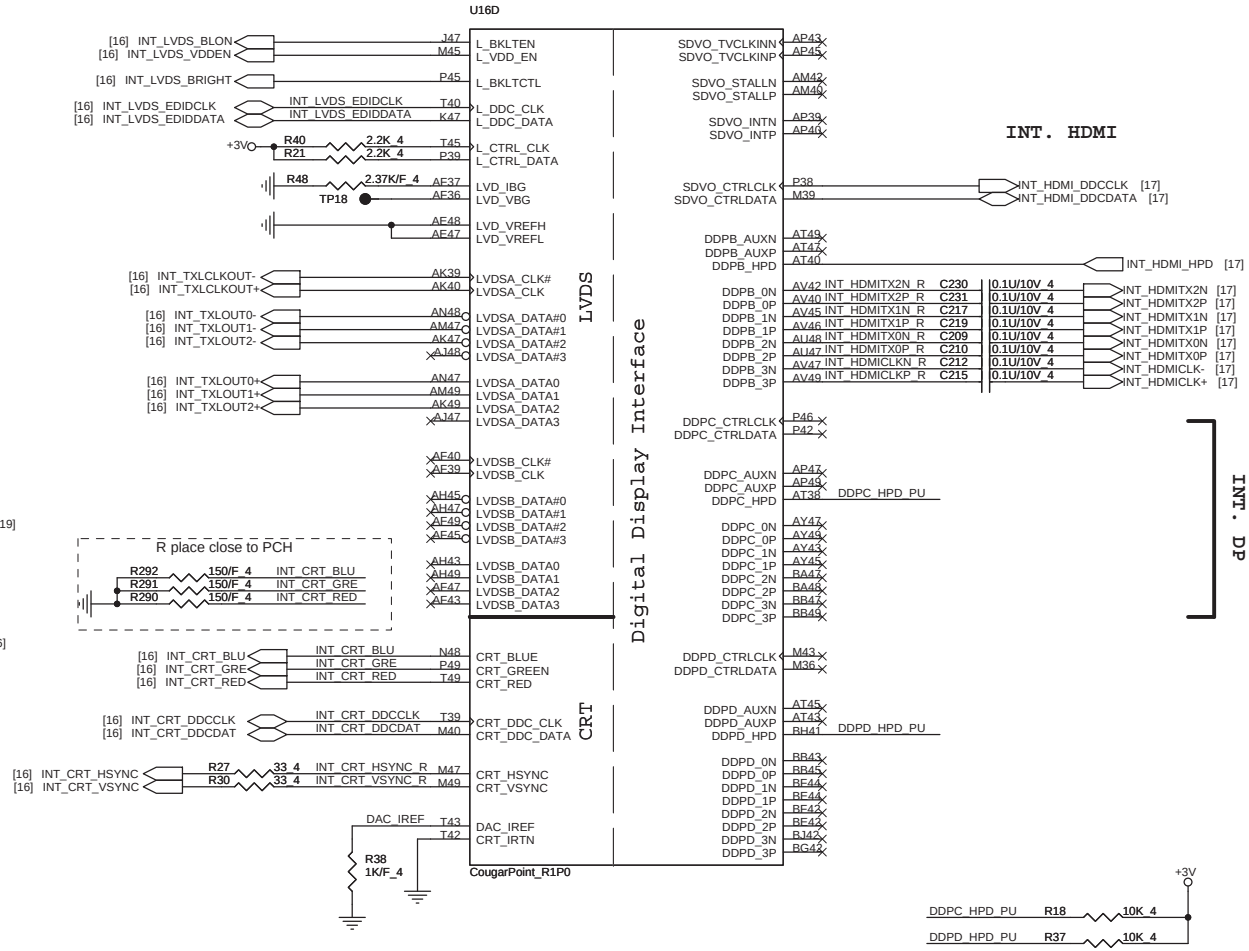
Cougar Point (DMI,FDI,PM)

U16C



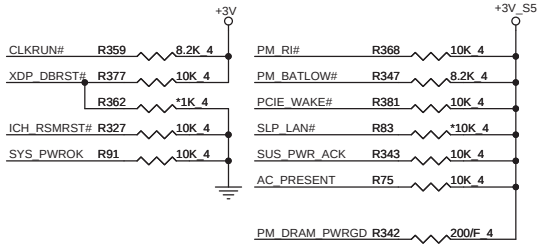
Cougar Point (LVDS,DDI)

U16D

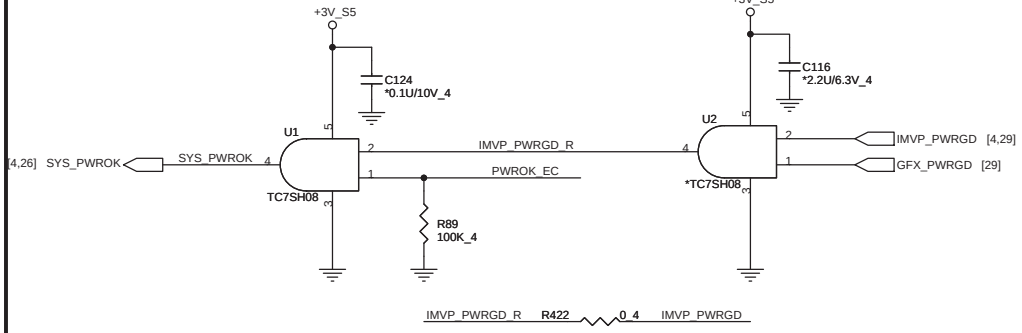


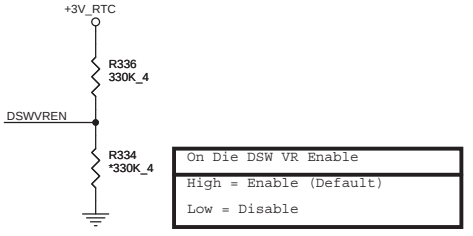
Follow PDG eDP disable guide

PCH Pull-high/low(CLG)



System PWR_OK(CLG)





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	Cougar Point 1/6	1A
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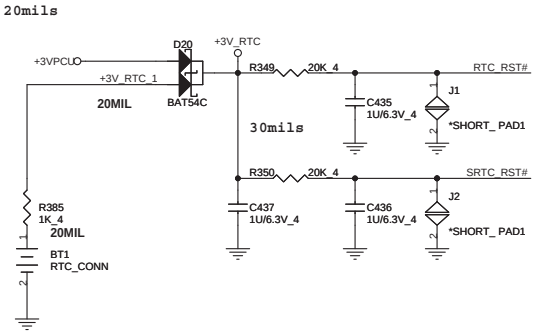
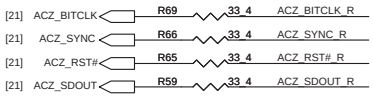
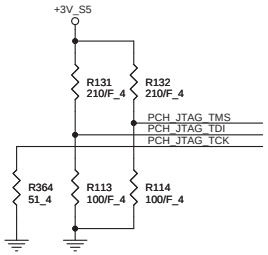
RTC Circuitry(RTC)



HDA Bus(CLG)

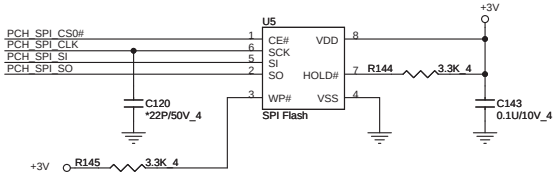


PCH JTAG Debug (CLG)



PCH Dual SPI (CLG)

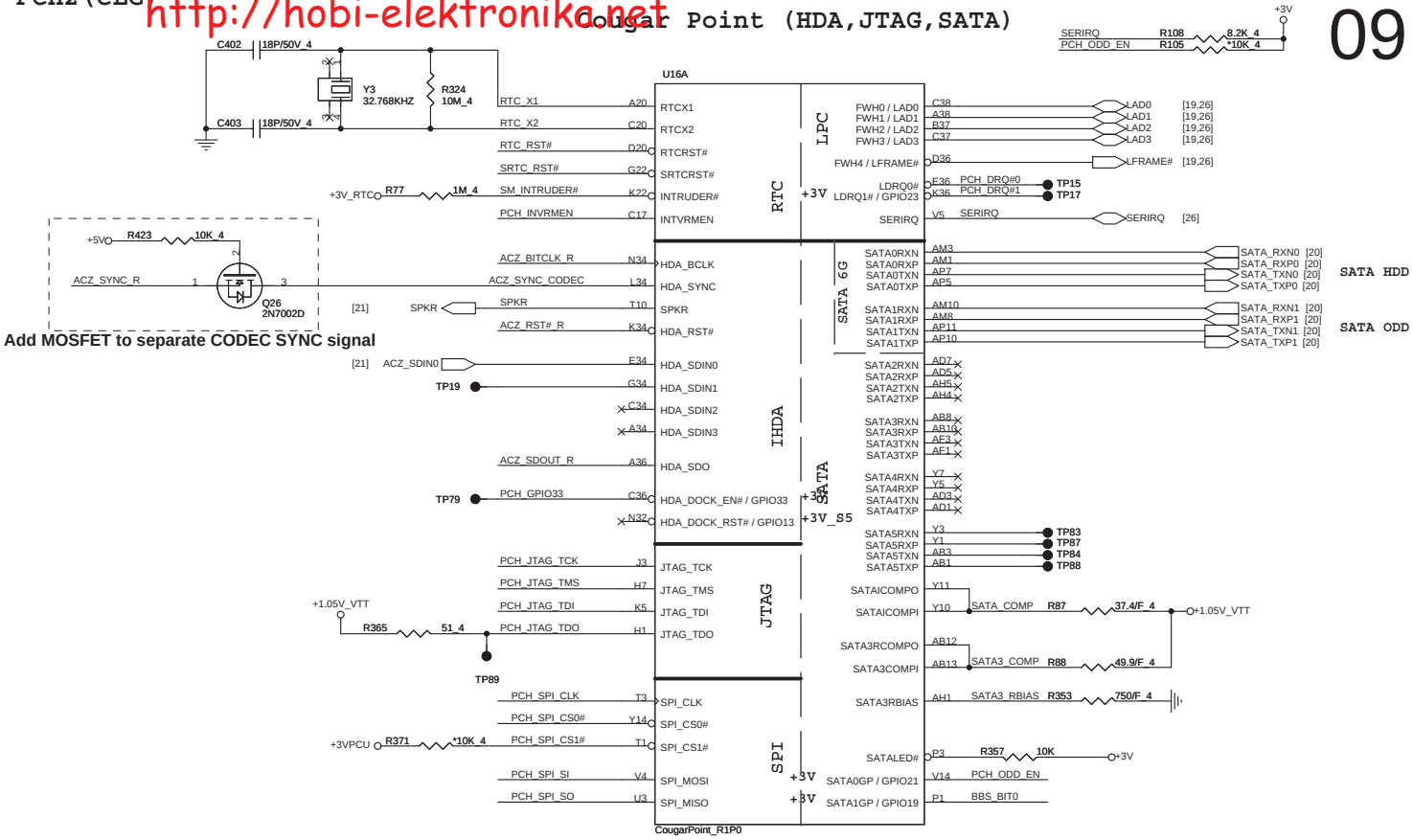
MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00



PCH2 (CLG)

Cougar Point (HDA,JTAG,SATA)

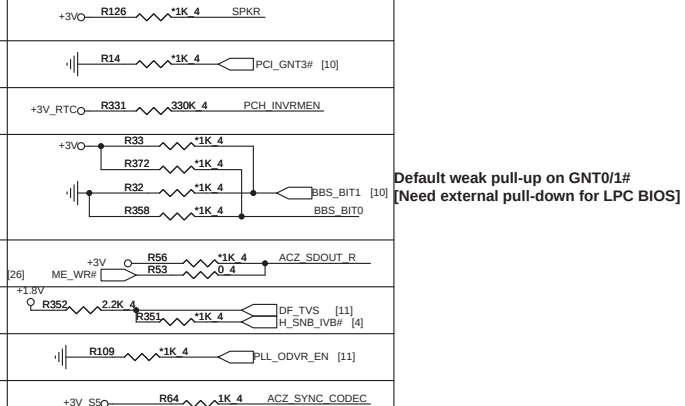
09



Add MOSFET to separate CODEC SYNC signal

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location 1 / 1 / SPI * 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)
DF_TVS	DMI/FDI Termination voltage	PWROK	**0 = Set to Vss** **1 = Set to Vcc (weak pull-down 20K)**
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	**0 = Support by 1.8V (weak pull-down)** **1 = Support by 1.5V**
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)



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PROJECT : ZRL

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	Cougar Point 2/6	1A

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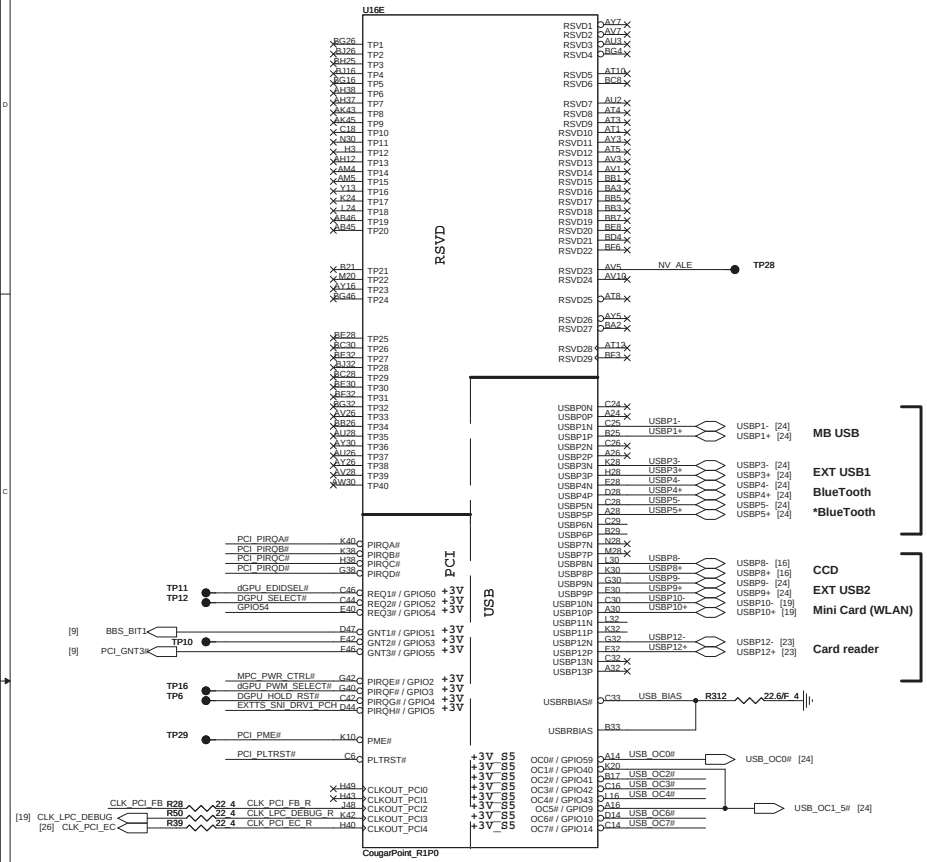
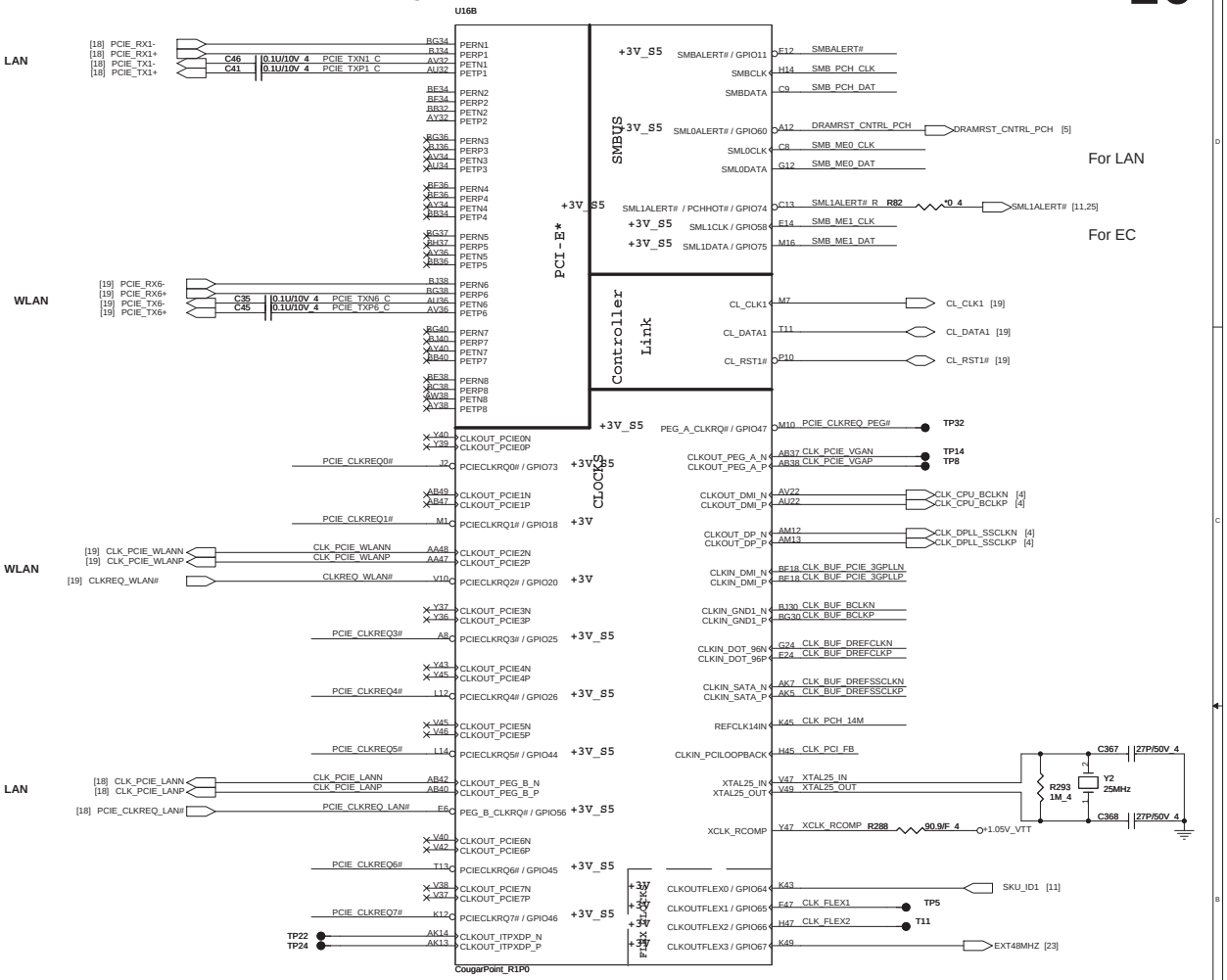
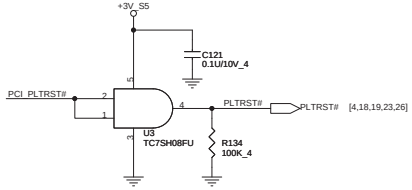
Cougar Point-M (PCI,USB,NVRAM)



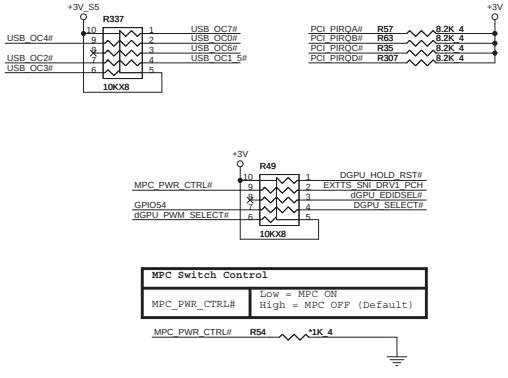
Cougar Point-M (PCI-E,SMBUS,CLK)



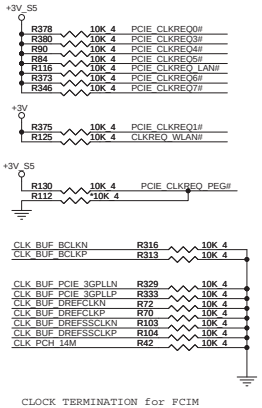
PLTRST#(CLG)



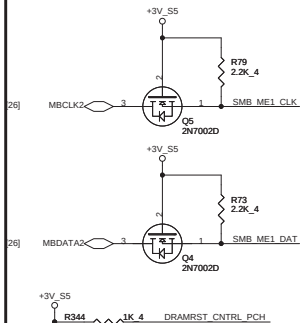
PCI/USBOC# Pull-up(CLG)



CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)



SMBus(PCH)

Quanta Computer Inc.
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	Cougar Point 3/6	1A
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Cougar Point (GPIO,VSS_NCTF,RSVD)

U16F

GPIO

S_GPIO	T7	BMBUSY# / GPIO0	+3V	+3V	TACH4 / GPIO68	C40	dGPU_PWR_CTRL#
[26] EC_EXT_SMI#	A42	TACH1 / GPIO1	+3V	+3V	TACH5 / GPIO69	B41	R298 1.5K/F_4
BOARD_ID1	H36	TACH2 / GPIO6	+3V	+3V	TACH6 / GPIO70	C41	R302 1.5K/F_4 +3V
[26] EC_EXT_SCI#	E38	TACH3 / GPIO7	+3V	+3V	TACH7 / GPIO71	A40	R303 1.5K/F_4
TP86	C10	GPIO8	+3V_S5				
SMIB#	C4	LAN_PHY_PWR_CTRL / GPIO12	+3V_S5				
PCH_GPIO15	G2	GPIO15	+3V_S5				
check VR_ON GPIO	SKU_ID0	U2	SATA4GP / GPIO16	+3V			
TP4	dGPU_PWROK	D40	TACH0 / GPIO17	+3V			
BIOS_REC	T5	SCLOCK / GPIO22	+3V				
CR_WAKER#	F8	GPIO24 / MEM_LED	+3V_S5				
GPIO27	E16	GPIO27	DSW				
[9] PLL_ODVR_EN	PLL_ODVR_EN	P8	GPIO28	+3V_S5			
Need Check	STP_PCI#	K1	STP_PCI# / GPIO34	+3V			
TP27	dGPU_VRON	K4	GPIO35	+3V			
TP30	DMI_OVRVLTG	V8	SATA2GP / GPIO36	+3V			
FDI_OVRVLTG	M5	SATA3GP / GPIO37	+3V				
MFG_MODE	N2	SLOAD / GPIO38	+3V				
BOARD_ID0	M3	SDATAOUT0 / GPIO39	+3V				
TEST_SET_UP	V13	SDATAOUT1 / GPIO48	+3V				
[10,25] SML1ALERT#	R354 *short_4 CRIT_TEMP_REP#	V3	SATA5GP / GPIO49	+3V			
BOARD_ID2	D6	GPIO57	+3V_S5				

CPU/MISC

A20GATE	P4	EC_A20GATE	EC_A20GATE [26]
PECI	AU16	R102 *0_4	EC_PECI [4,26]
RCIN#	P5	EC_RCIN#	EC_RCIN# [26]
PROCPWRGD	AY11	TP23	H_PWRGOOD [4]
THRMTRIP#	AY10	PCH_THRMTRIP# R101 390_4	PM_THRMTRIP# [4]
INIT3_3V#	T14		
DF_TVS	AY1		DF_TVS [9]
TS_VSS1	AH8		
TS_VSS2	AK11		
TS_VSS3	AH10		
TS_VSS4	AK10		
NC_1	P37		

NCTF

A4	VSS_NCTF_1	VSS_NCTF_15	BG2
A44	VSS_NCTF_2	VSS_NCTF_16	BG48
A45	VSS_NCTF_3	VSS_NCTF_17	BH3
A46	VSS_NCTF_4	VSS_NCTF_18	BH47
A5	VSS_NCTF_5	VSS_NCTF_19	BJ4
A6	VSS_NCTF_6	VSS_NCTF_20	BJ44
B3	VSS_NCTF_7	VSS_NCTF_21	BJ45
B47	VSS_NCTF_8	VSS_NCTF_22	BJ46
BD1	VSS_NCTF_9	VSS_NCTF_23	BJ5
BD49	VSS_NCTF_10	VSS_NCTF_24	BJ6
BE1	VSS_NCTF_11	VSS_NCTF_25	C2
BF49	VSS_NCTF_12	VSS_NCTF_26	C48
BF1	VSS_NCTF_13	VSS_NCTF_27	D1
BF49	VSS_NCTF_14	VSS_NCTF_28	D49
		VSS_NCTF_29	E1
		VSS_NCTF_30	F49
		VSS_NCTF_31	F1
		VSS_NCTF_32	F49

CougarPoint_R1P0

R353??

GPIO27:
Un-multiplexed. Can be configured as wake input to allow wakes from Deep Sleep.
If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

	dGPU_PWR_CTRL# (GPIO68)	SKU_ID1 (GPIO64)	SKU_ID0 (GPIO16)	VGA H/W Signal	Setup Menu	
UMA Only	1	0	0	UMA	Hidden	UMA boot
Discrete Only	0 or 1	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	0	1	0	UMA+GPU	DIS/SG	UMA boot
Optimize (Muxless)	0	1	1	UMA	UMA/SG	UMA boot

0 = GPU power is control by PCH GPIO (Discrete, SG or Optimize)
1 = GPU power is control by H/W (pure Discrete SKU)

SV_SET_UP

High = Strong (Default)

TEST_SET_UP R124 10K_4, R107 *0_4 +3V

SGPIO

S_GPIO R111 1K/F_4, R95 *100_4 +3V

PCH_GPIO15 R379 1K_4 +3V_S5

Intel ME Crypto Transport Layer Security (TLS) cipher suite

Low = Disable (Default)

High = Enable

MFG-TEST

MFG_MODE R374 10K_4, R360 *0_4 +3V

GPIO Pull-up/Pull-down(CLG)

+3V_S5: CR_WAKER# R348 10K/F_4; SMIB# R366 10K_4; PLL_ODVR_EN R127 *10K_4

+3V: EC_EXT_SMI# R299 10K_4; EC_EXT_SCI# R34 10K_4; STP_PCI# R363 *10K_4; EC_A20GATE R96 10K_4; EC_RCIN# R93 10K_4; CRIT_TEMP_REP# R355 10K_4; dGPU_PWROK R36 *10K_4; GPIO27 R80 *10K_4

+3V: R297 10K_4, R305 *100K_4 dGPU_PWR_CTRL#

+3V: R15 *10K_4, R22 10K_4 SKU_ID1 [10]

+3V: R370 *10K_4, R356 10K_4 SKU_ID0

+3V: R361 *10K_4 BOARD_ID0; R300 10K_4 BOARD_ID1; R115 10K_4 BOARD_ID2; R376 10K_4; R301 *10K_4; R133 *10K_4

FDI_OVRVLTG R129 *10K/F_4 +3V

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

DMI_OVRVLTG R94 *200K/F_4 +3V

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

BIOS_REC R128 10K_4, R110 *0_4 +3V

BIOS RECOVERY	High = Disable (Default) Low = Enable

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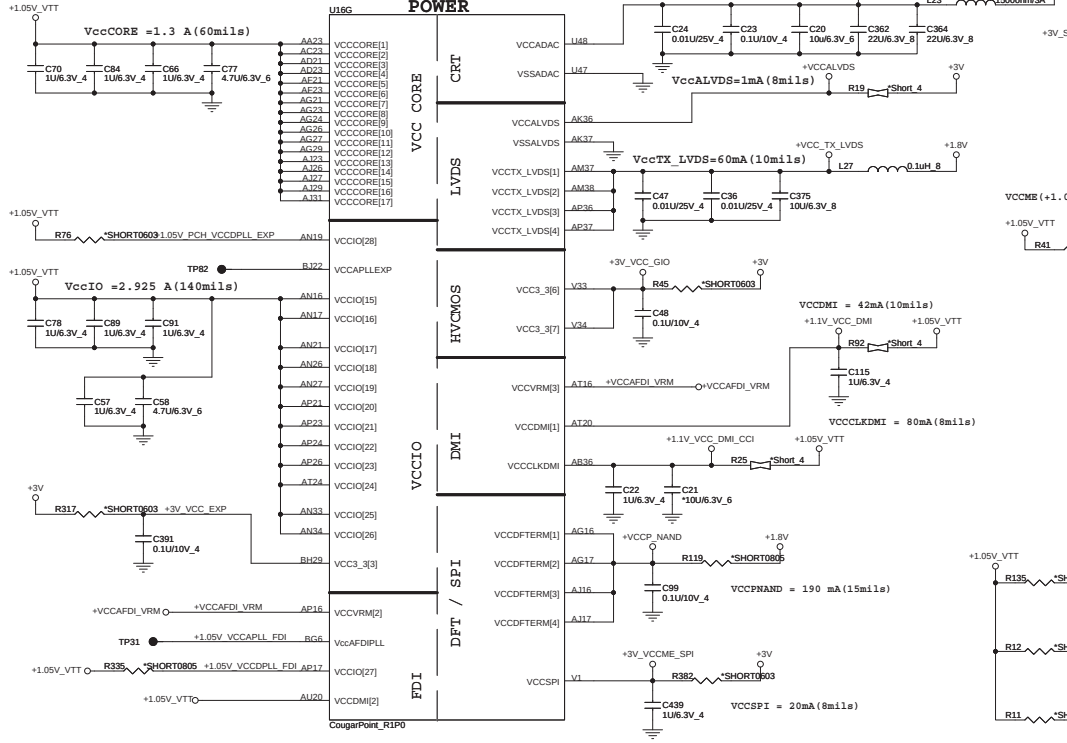
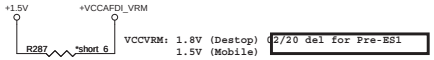
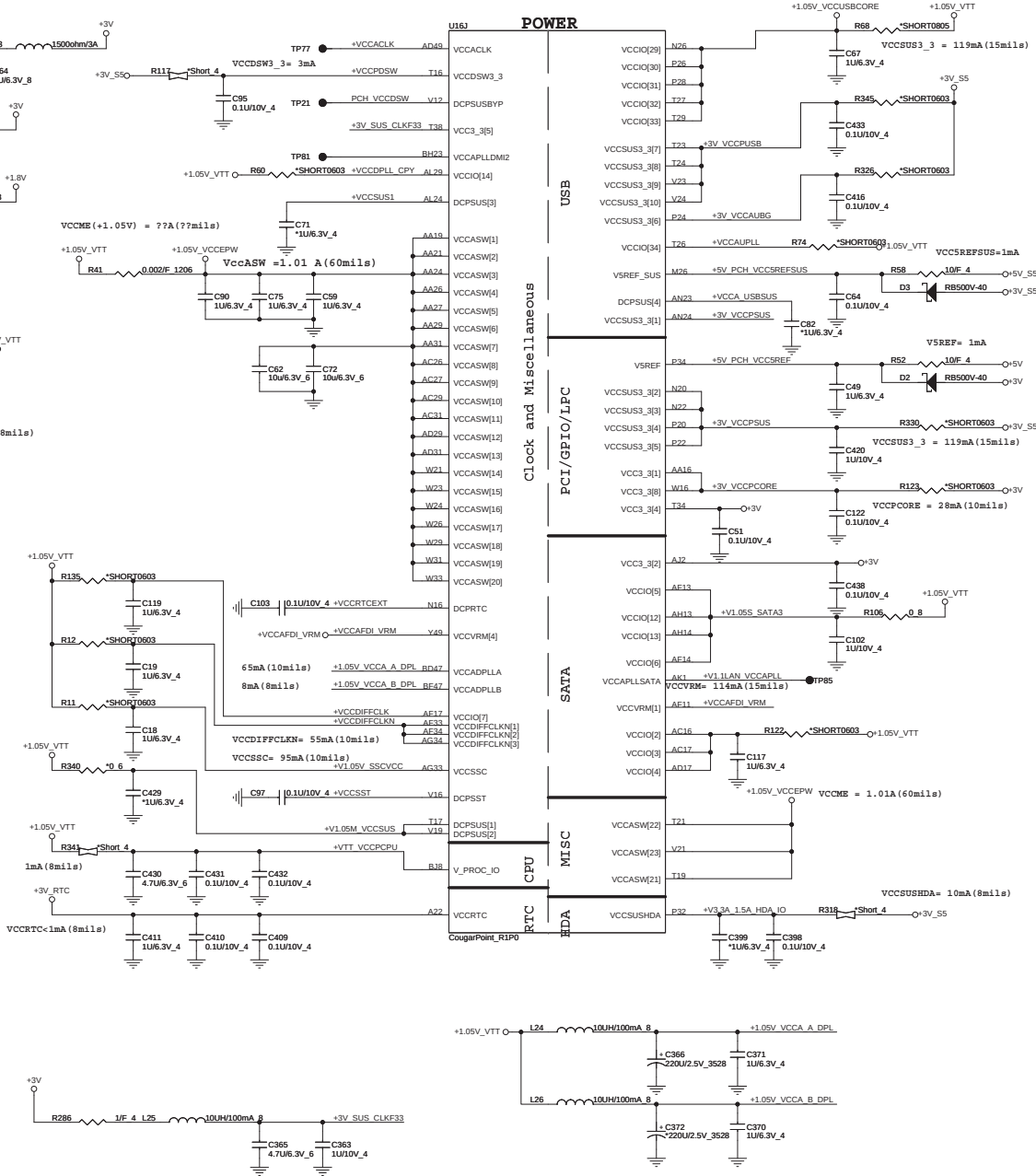
COUGAR POINT (POWER)





Cougar Point-M (POWER)



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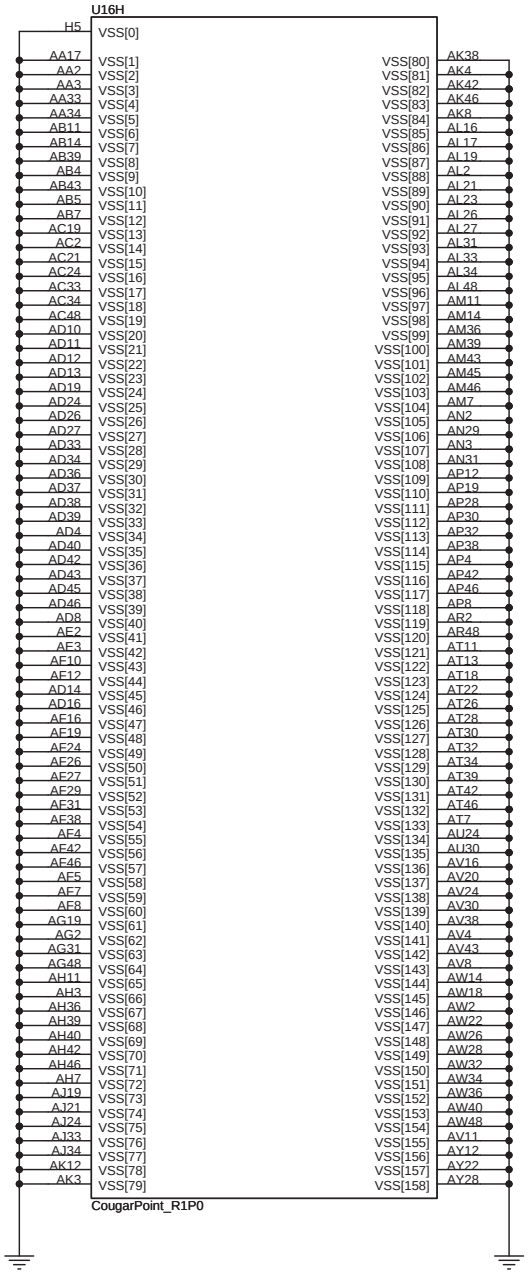
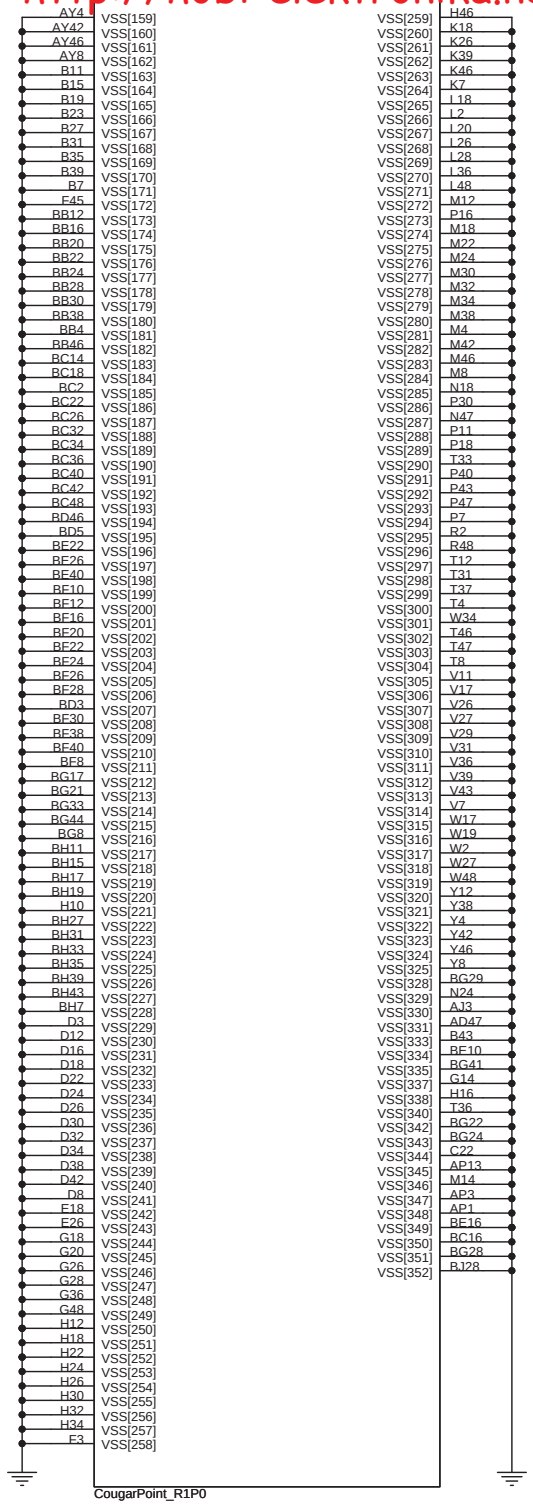
IBEX PEAK-M (GND)





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DDR RVS 4H

[5] M_A_A[15:0]

JDIM2A

M_A_A0 98, M_A_A1 97, M_A_A2 96, M_A_A3 95, M_A_A4 92, M_A_A5 91, M_A_A6 90, M_A_A7 86, M_A_A8 89, M_A_A9 85, M_A_A10 107, M_A_A11 84, M_A_A12 83, M_A_A13 119, M_A_A14 80, M_A_A15 78

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC# A13 A14 A15

[5] M_A_BS#0 109
[5] M_A_BS#1 108
[5] M_A_BS#2 79
[5] M_A_CS#0 114
[5] M_A_CS#1 121
[5] M_A_CLKP0 101
[5] M_A_CLKN0 103
[5] M_A_CLKP1 102
[5] M_A_CLKN1 104
[5] M_A_CKE0 73
[5] M_A_CKE1 74
[5] M_A_CAS# 115
[5] M_A_RAS# 110
[5] M_A_WE# 113

BA0 BA1 BA2 S0# S1# CK0 CK0# CK1 CK1# CKE0 CKE1 CAS# RAS# WE#

R183 10K_4
R182 10K_4

DIMM0_SA0 197
DIMM0_SA1 201

[10,15,19] CLK_SCLK 202
[10,15,19] CLK_SDATA 200

SA0 SA1 SCL SDA

[5] M_A_ODT0 116
[5] M_A_ODT1 120

ODT0 ODT1

PC2100 DDR3 SDRAM SO-DIMM (204P)

M_A_DQ[63:0] [5]

M_A_DQ5 5, M_A_DQ4 7, M_A_DQ6 15, M_A_DQ7 17, M_A_DQ0 4, M_A_DQ1 6, M_A_DQ2 16, M_A_DQ3 18, M_A_DQ12 21, M_A_DQ13 23, M_A_DQ14 33, M_A_DQ15 35, M_A_DQ8 22, M_A_DQ9 24, M_A_DQ10 34, M_A_DQ11 36, M_A_DQ20 39, M_A_DQ21 41, M_A_DQ23 51, M_A_DQ22 53, M_A_DQ17 40, M_A_DQ16 42, M_A_DQ19 50, M_A_DQ18 52, M_A_DQ25 57, M_A_DQ24 59, M_A_DQ27 67, M_A_DQ31 69, M_A_DQ28 56, M_A_DQ29 58, M_A_DQ26 68, M_A_DQ30 70, M_A_DQ33 129, M_A_DQ37 131, M_A_DQ34 141, M_A_DQ38 143, M_A_DQ32 130, M_A_DQ36 132, M_A_DQ39 140, M_A_DQ35 142, M_A_DQ44 147, M_A_DQ40 149, M_A_DQ43 157, M_A_DQ42 159, M_A_DQ45 146, M_A_DQ41 148, M_A_DQ46 158, M_A_DQ47 160, M_A_DQ53 163, M_A_DQ52 165, M_A_DQ54 175, M_A_DQ55 177, M_A_DQ48 164, M_A_DQ49 166, M_A_DQ51 174, M_A_DQ50 176, M_A_DQ61 181, M_A_DQ60 183, M_A_DQ62 191, M_A_DQ63 193, M_A_DQ56 180, M_A_DQ57 182, M_A_DQ59 192, M_A_DQ58 194

DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63

DDR3-DIMM0_H=4_RVS_LTS

02/23 Remove 0ohm to GND

DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7

[5] M_A_DQSP[7:0]

M_A_DQSP0 12, M_A_DQSP1 29, M_A_DQSP2 47, M_A_DQSP3 64, M_A_DQSP4 137, M_A_DQSP5 154, M_A_DQSP6 171, M_A_DQSP7 188, M_A_DQSN0 10, M_A_DQSN1 27, M_A_DQSN2 45, M_A_DQSN3 62, M_A_DQSN4 135, M_A_DQSN5 152, M_A_DQSN6 169, M_A_DQSN7 186

DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7 DQS#0 DQS#1 DQS#2 DQS#3 DQS#4 DQS#5 DQS#6 DQS#7

[5] M_A_DQSN[7:0]

+1.5V_SUS

JDIM2B

2.48A

VDD1 75, VDD2 76, VDD3 81, VDD4 82, VDD5 87, VDD6 88, VDD7 93, VDD8 94, VDD9 99, VDD10 100, VDD11 105, VDD12 106, VDD13 111, VDD14 112, VDD15 117, VDD16 118, VDD17 123, VDD18 124

+3V VDDSPD 199

NC1 77, NC2 122, NCTEST 125

+3V R173 10K_4

EVENT# 198

[5,15] DDR3_DRAMRST# RESET# 30

DDR3_DRAMRST#

SMDDR_VREF_DQ0_M1 VREF_DQ 1

+SMDDR_VREF_DIMM VREF_CA 126

CAD Note: All VREF traces should have 10 mil trace width

VSS1 2, VSS2 3, VSS3 8, VSS4 9, VSS5 13, VSS6 14, VSS7 19, VSS8 20, VSS9 25, VSS10 26, VSS11 31, VSS12 32, VSS13 37, VSS14 38, VSS15 43

VSS16 44, VSS17 48, VSS18 49, VSS19 54, VSS20 55, VSS21 60, VSS22 61, VSS23 65, VSS24 66, VSS25 71, VSS26 72, VSS27 127, VSS28 128, VSS29 133, VSS30 134, VSS31 138, VSS32 139, VSS33 144, VSS34 145, VSS35 150, VSS36 151, VSS37 155, VSS38 156, VSS39 161, VSS40 162, VSS41 167, VSS42 168, VSS43 172, VSS44 173, VSS45 178, VSS46 179, VSS47 184, VSS48 185, VSS49 189, VSS50 190, VSS51 195, VSS52 196

VTT1 203 VTT2 204 +0.75V_DDR_VTT

GND 205 GND 206

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0_H=4_RVS_LTS

DDR3_DRAMRST#
C197
0.1u/10V_4

VREF DQ0 M1 Solution

+1.5V_SUS
R178 1K/F_4
SMDDR_VREF_DQ0_M1
R177 1K/F_4

+1.5V_SUS
R176 10K/F_4
+SMDDR_VREF_DIMM
R175 10K/F_4
C221 470P/50V_4

Place these Caps near So-Dimm0.

+1.5V_SUS

C164 4.7U/6.3V_6, C222 4.7U/6.3V_6, C223 4.7U/6.3V_6, C169 4.7U/6.3V_6, C173 4.7U/6.3V_6, C184 4.7U/6.3V_6, C214 *10U/6.3V_6, C218 1U/10V_4, C224 1U/10V_4, C202 1U/10V_4, C163 1U/10V_4, C241 *330U/2V_7343, C165 4.7U/25V_8, C228 4.7U/25V_8

+3V

C211 2.2U/6.3V_6, C213 0.1u/10V_4

+0.75V_DDR_VTT

C204 1U/6.3V_4, C200 1U/6.3V_4, C196 1u/6.3V_4, C194 1U/6.3V_4, C208 4.7U/6.3V_6, C205 *10U/6.3V_6

+SMDDR_VREF_DIMM

C220 0.1u/10V_4, C225 2.2U/6.3V_6

SMDDR_VREF_DQ0_M1

C226 0.1u/10V_4, C227 2.2U/6.3V_6

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	DDRIII SO-DIMM-0	1A
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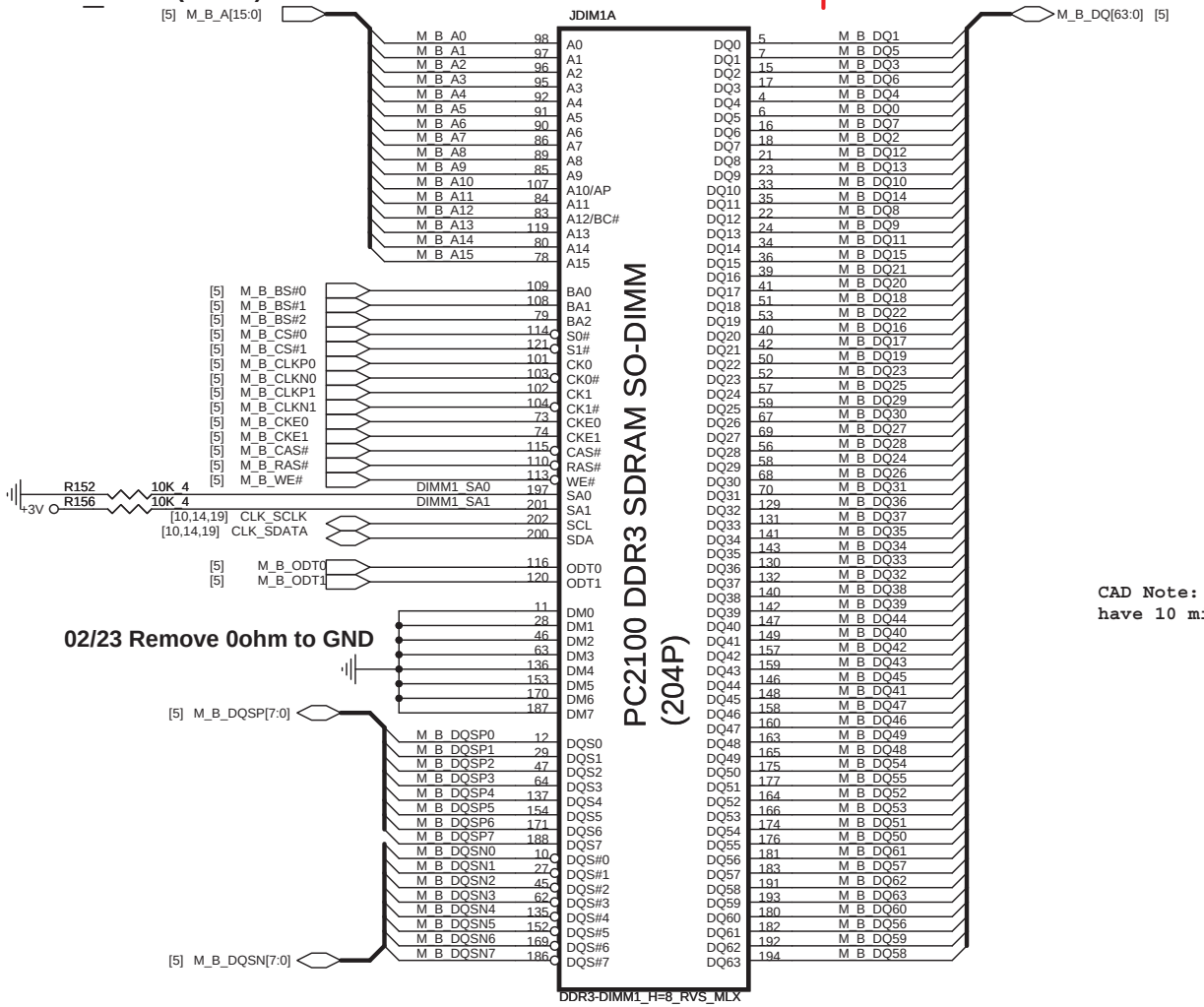
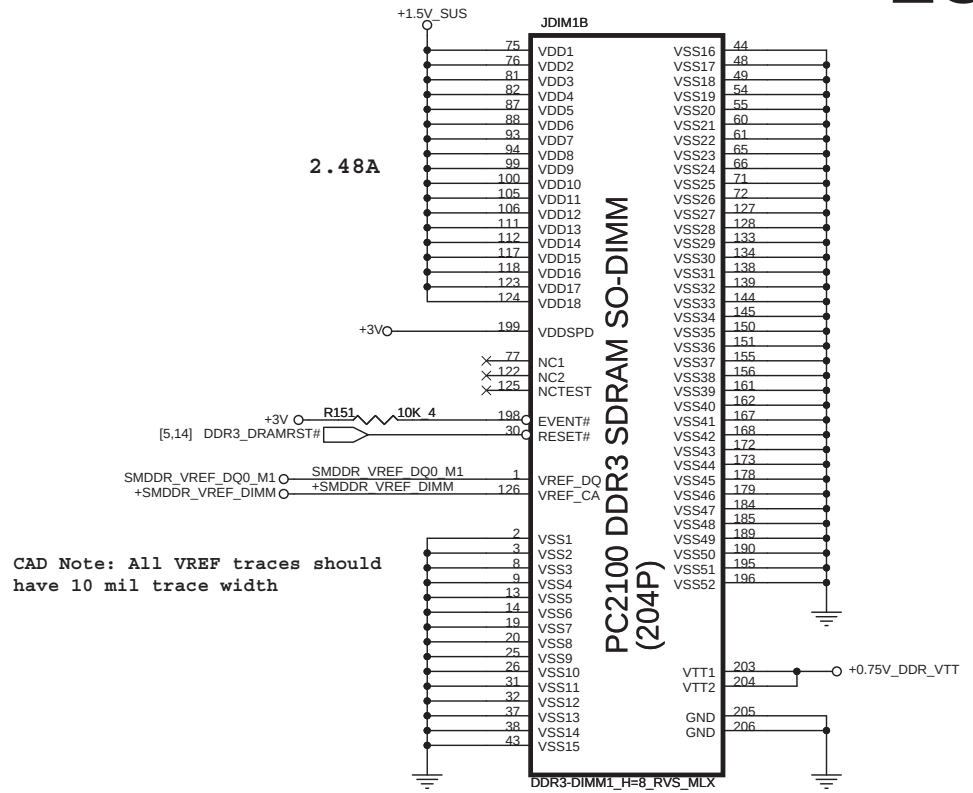
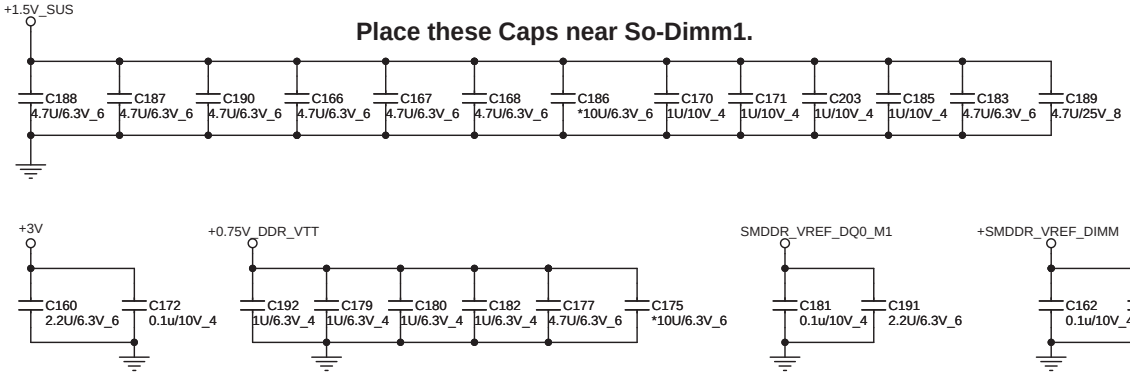
DDR_RVS(DDR)







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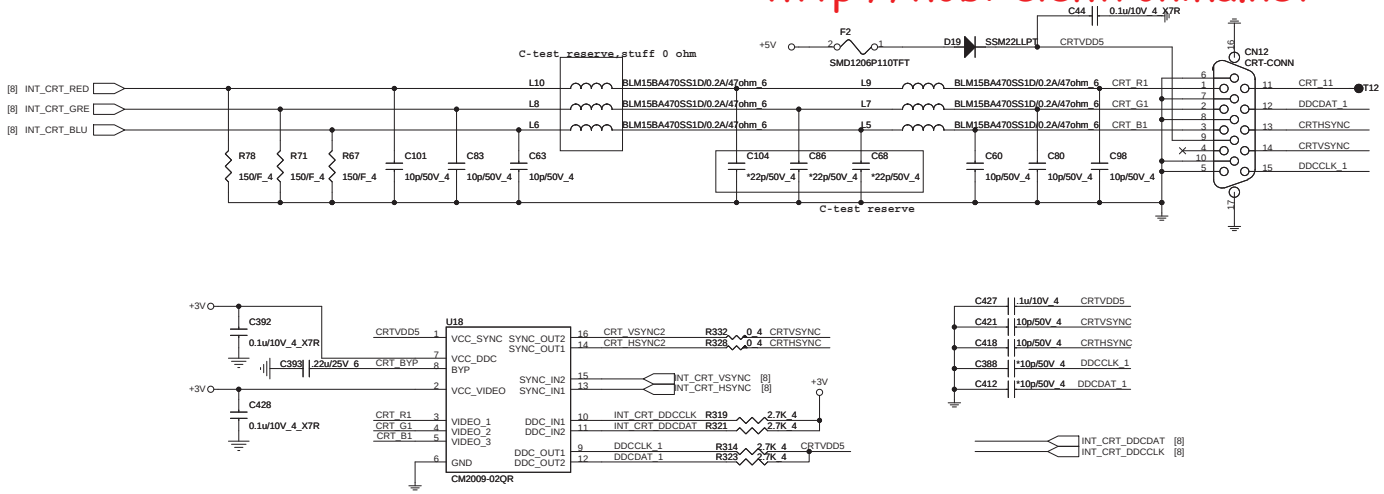
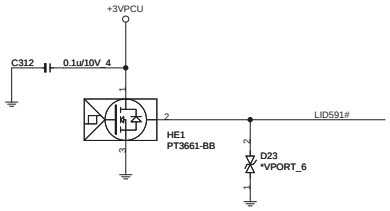
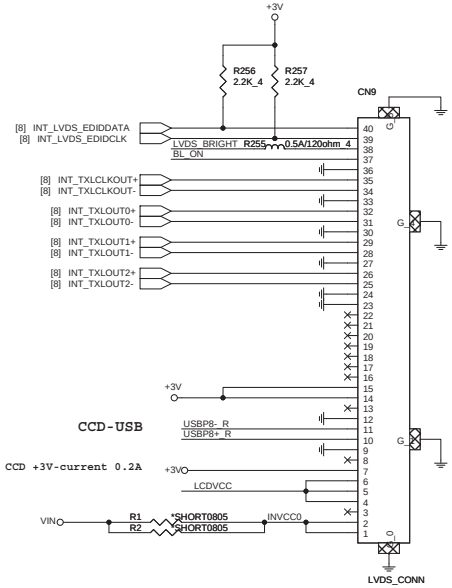
CRT

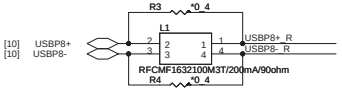


Lid Switch (Hall sensor)

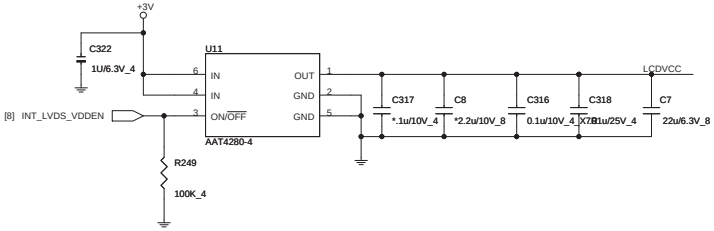


LVDS

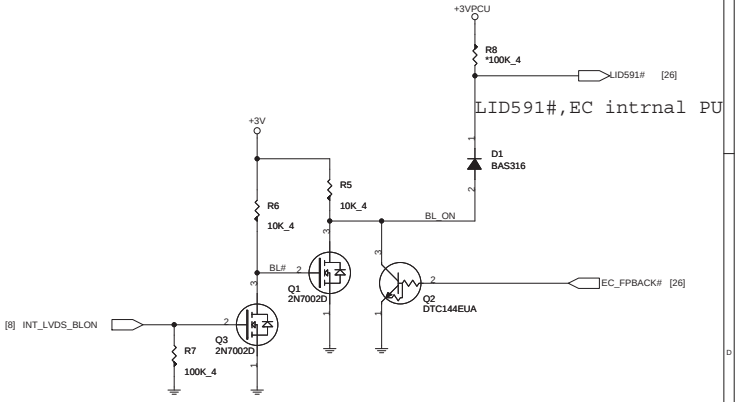




LCD Power



Backlight Control



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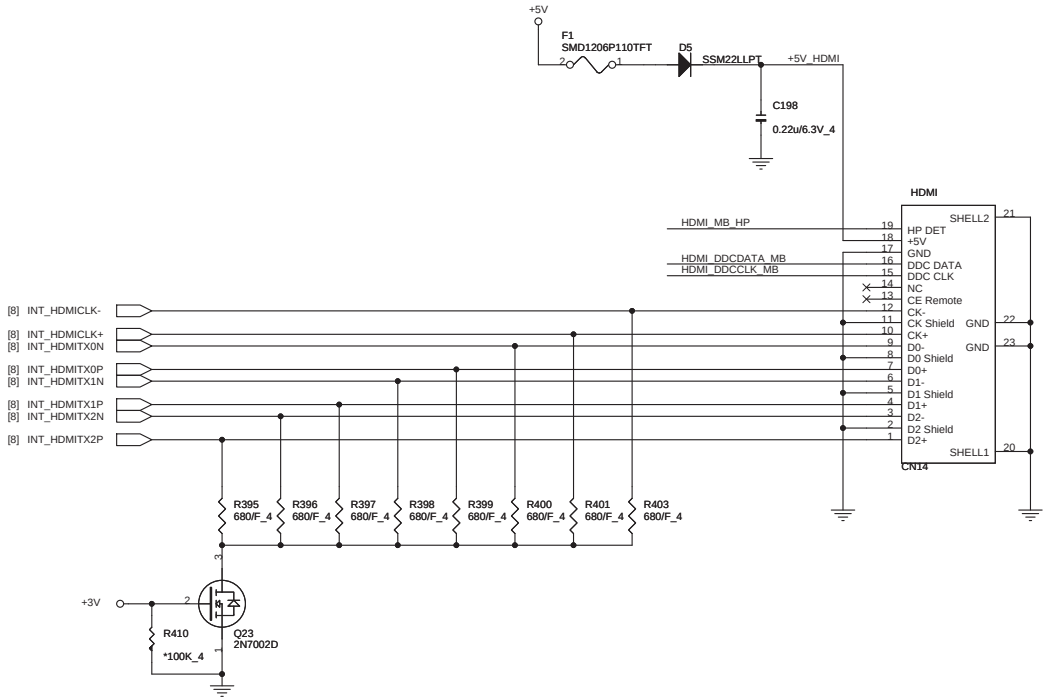
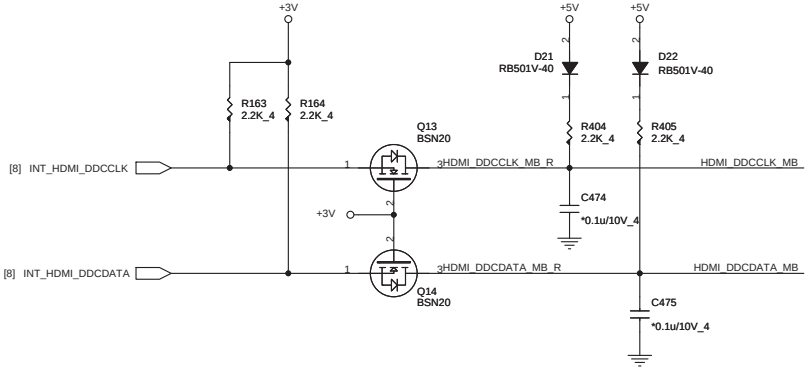
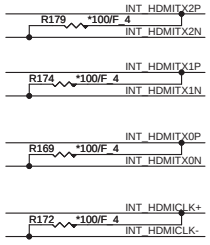
HDMI

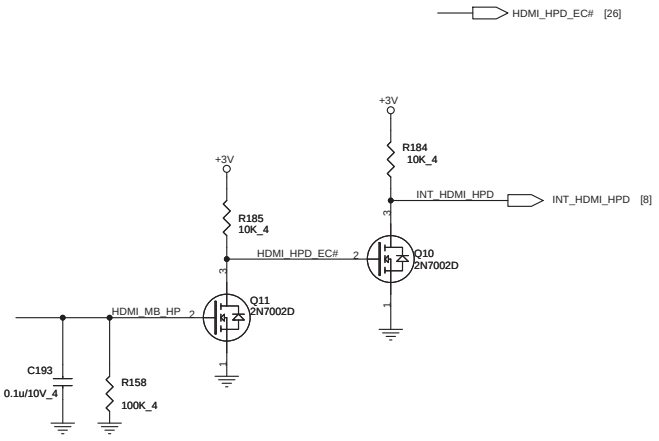




EMI



HDMI-detect



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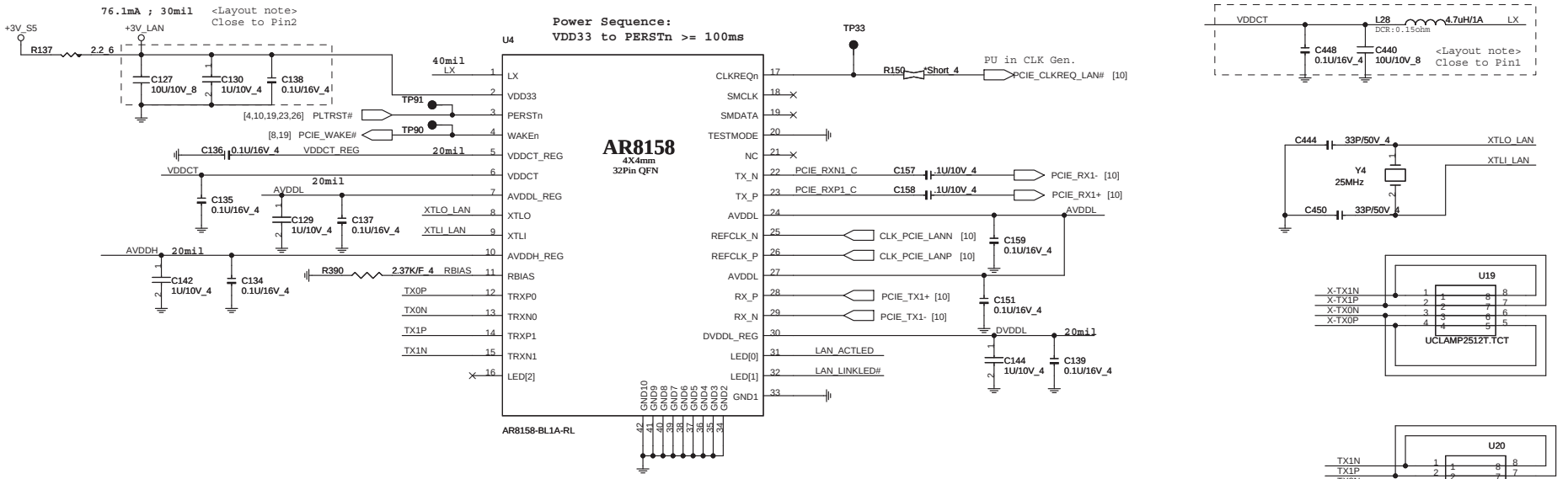
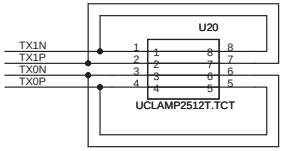
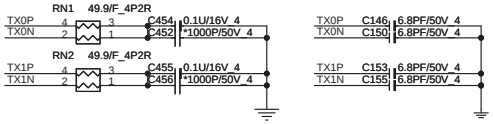
LAN

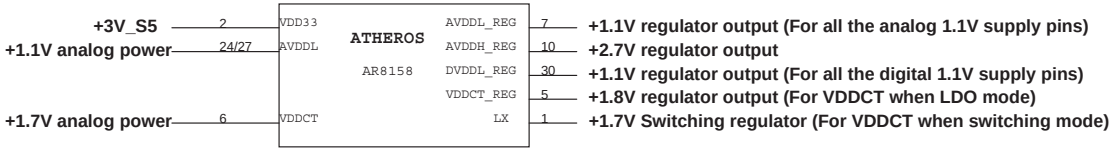
<BOM note>
If switch tap power come from internal switch regulator=>Stuff 52SWR@ (Default)
If center tap power come from internal LDO=>Stuff 52LDO@



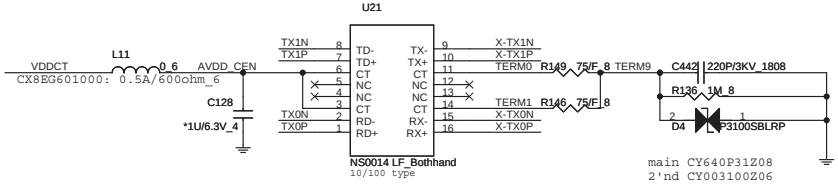


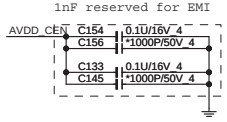
<Layout note>
Close to LAN Chip 1nF reserved for EMI



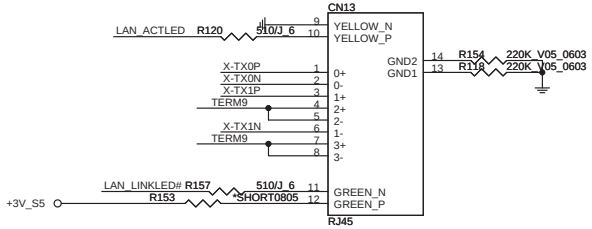


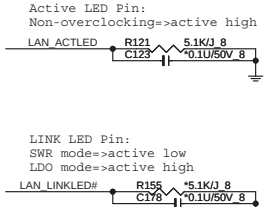
TRANSFORMER





RJ45 Connector





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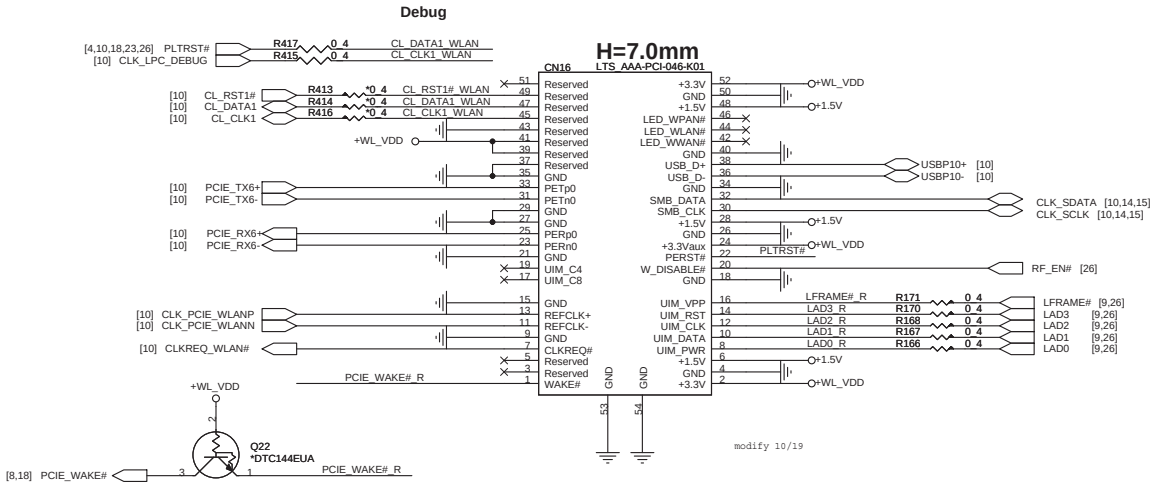
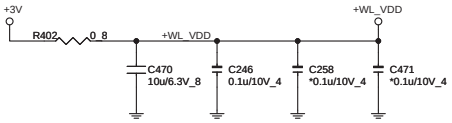
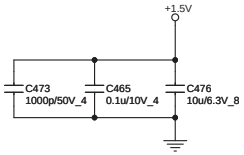
MINI-CARD WLAN

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

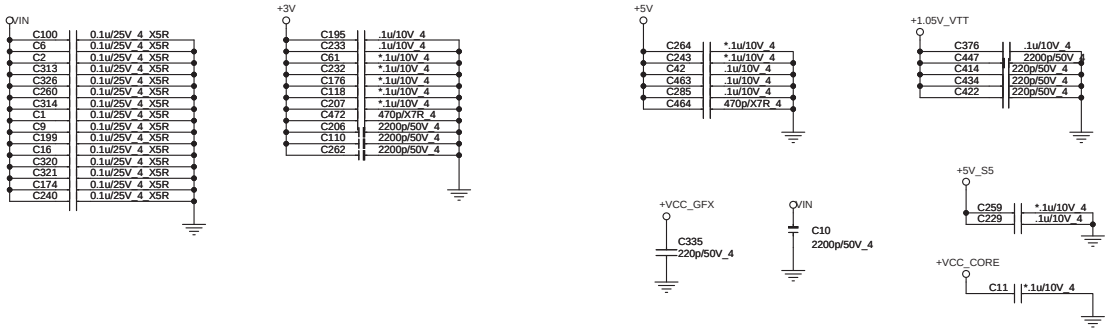






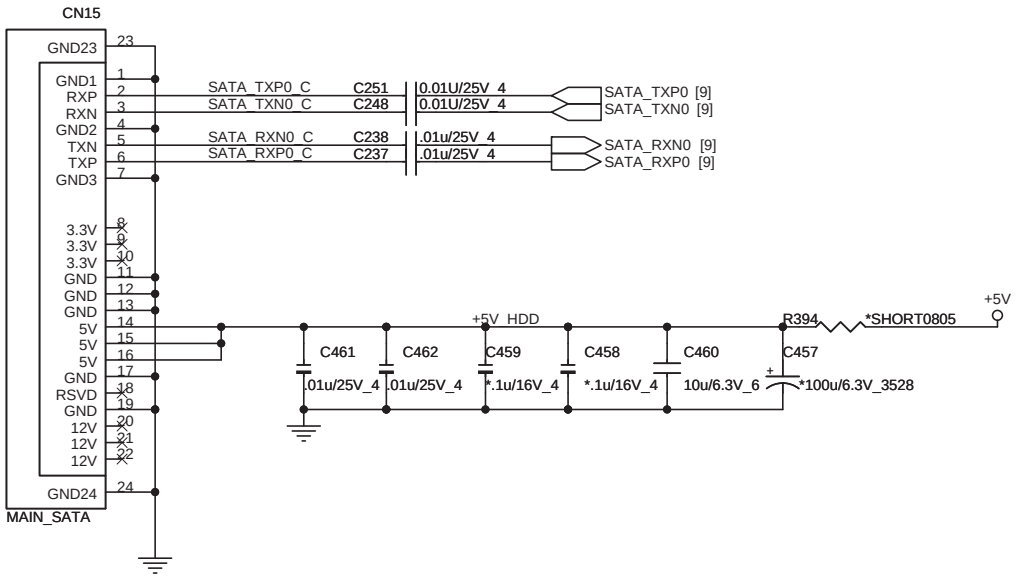
Debug

EE RETURN-PATH CAPACITORS

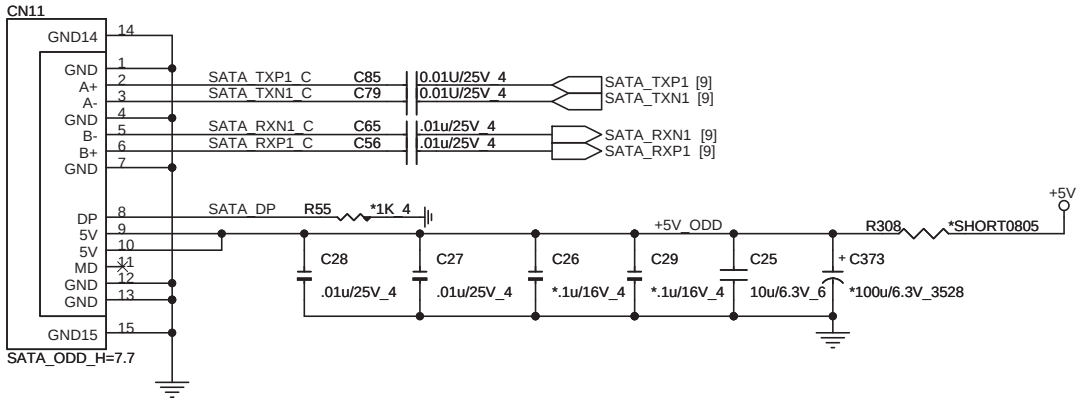


	Quanta Computer Inc.		
	PROJECT : ZRL		
Size	Document Number		Rev
	MINI PCI-E card/TV		1A
Date: Tuesday, June 21, 2011		Sheet 19 of 34	

MAIN SATA HDD



ODD (SATA)

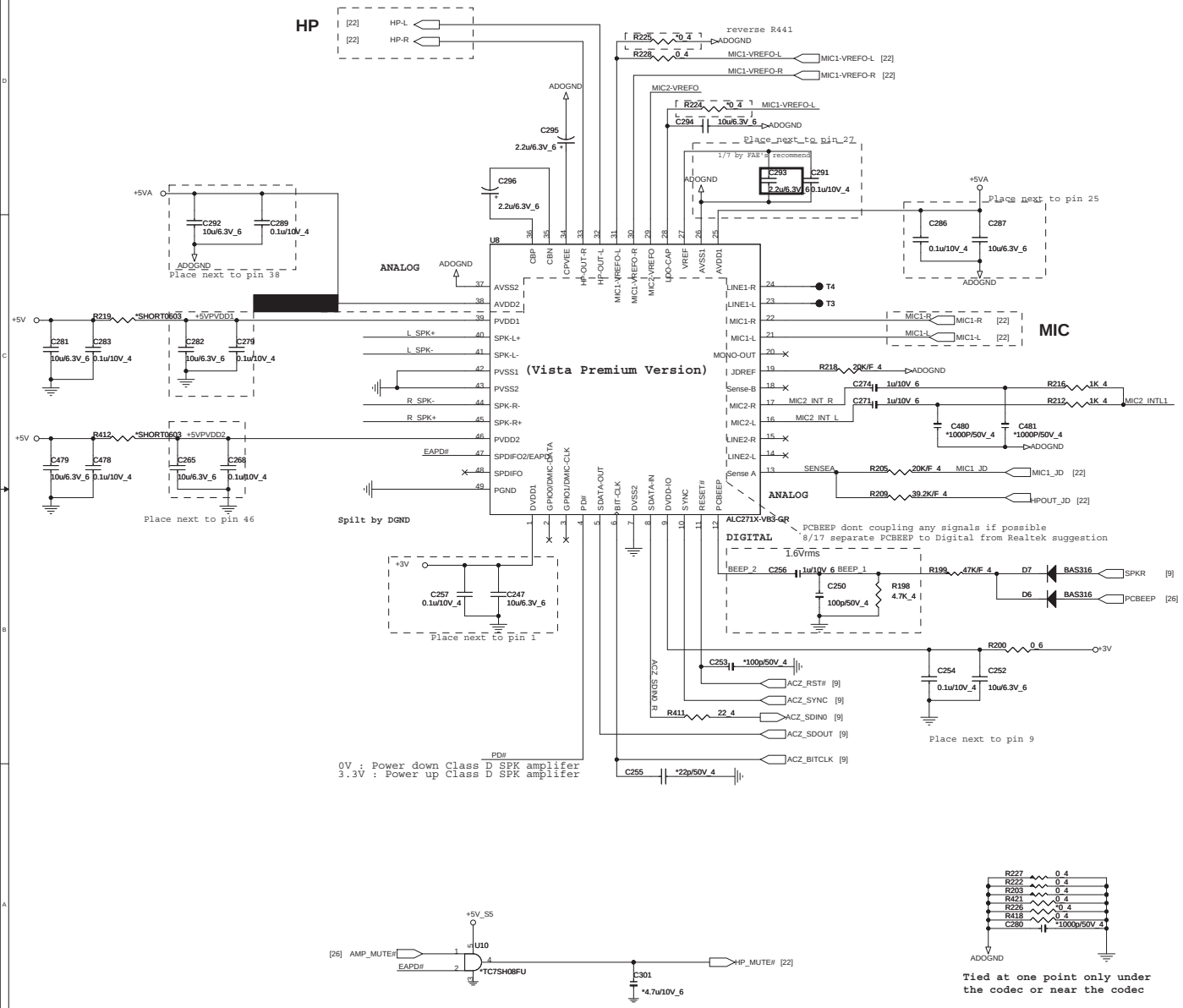


Quanta Computer Inc.

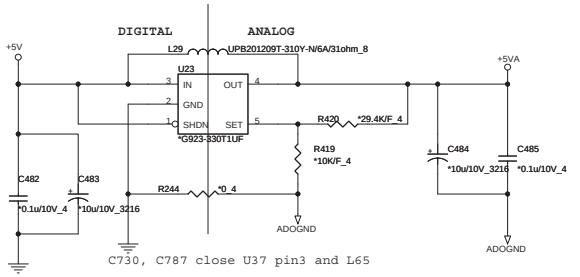
PROJECT : ZRL

Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	1A
Date: Tuesday, June 21, 2011	Sheet 20 of 34	

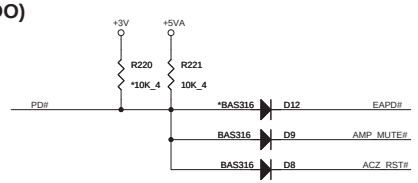
Codec



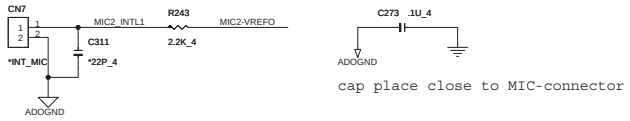
Power



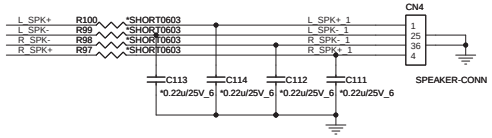
Mute(ADO)



Internal MIC



Internal Speaker



Quanta Computer Inc.
PROJECT : ZRL

Size	Document Number	Rev
	REALTEK ALC271X	1A
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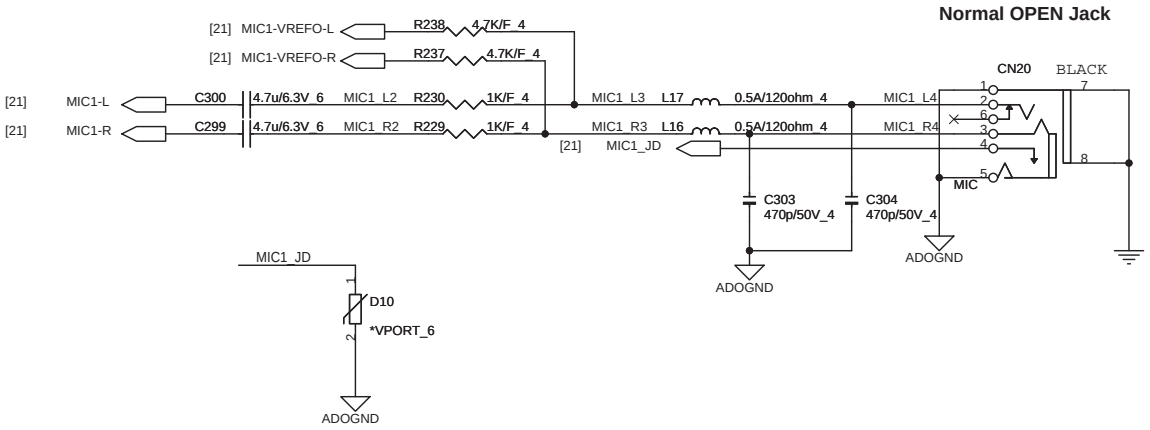
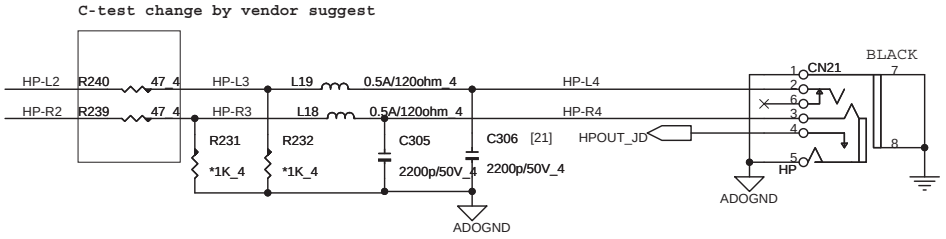
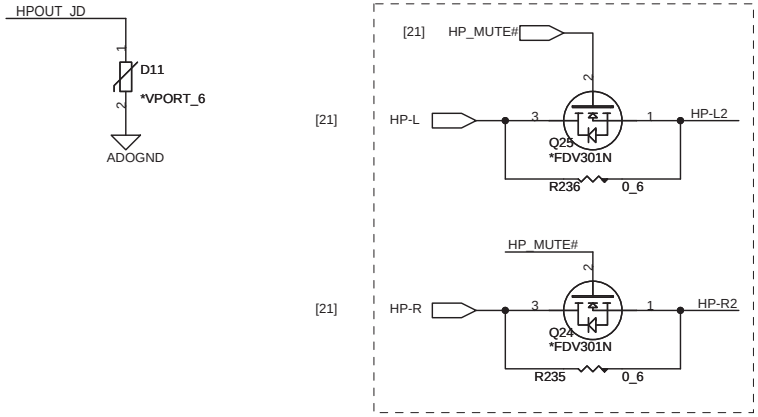
MIC



HP



C-test , remove Q25,Q24, stuff R236,R235 fix POPO sound

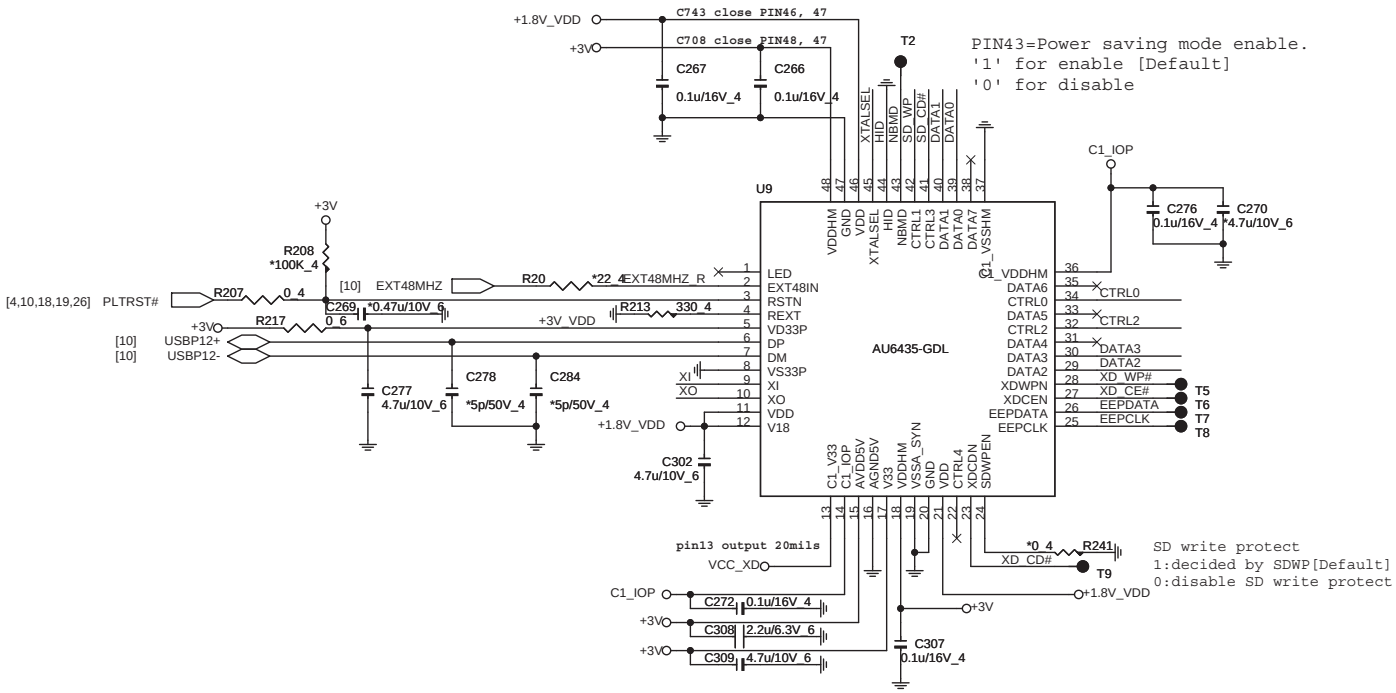


Quanta Computer Inc.

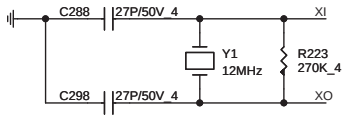
PROJECT : ZRL

Size	Document Number	Rev
	AMP /AUDIO JACK CONN	1A
Date: Tuesday, June 21, 2011	Sheet 22 of 34	

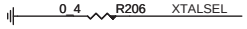
4 in 1 CARD READER IC (SD,MMC,xD,MS)



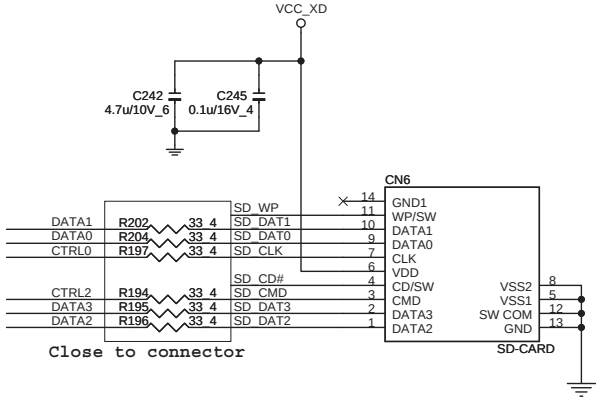
CTRL0, CRTL 1 trace length shorter ,
and surround with GND.



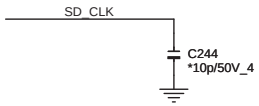
PIN45=Clock input selection
'1' for 48MHz input [Default,Internal PU]
'0' for 12MHz input



2 IN 1 CARD READER CONN (SD/MMC)



CLK Shorter than 1200 mil is good.



Main	DFHS11FR011
Second	DFHS11FR033

PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	AU6433 CardReader	1A
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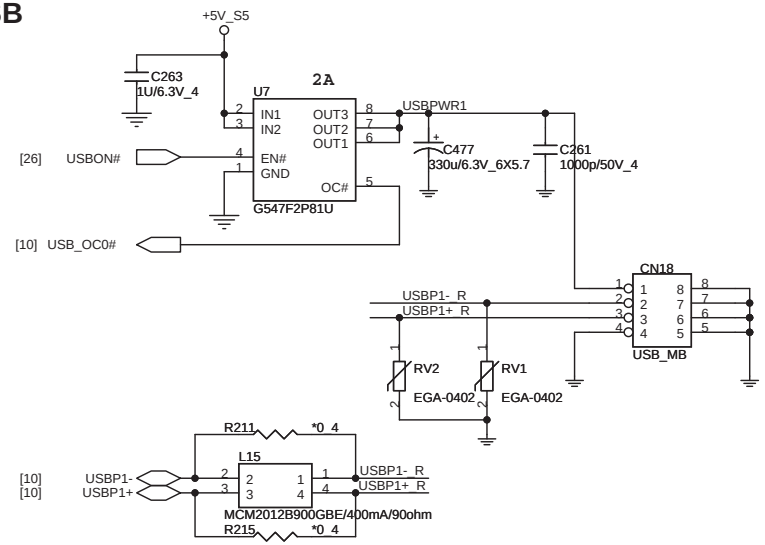
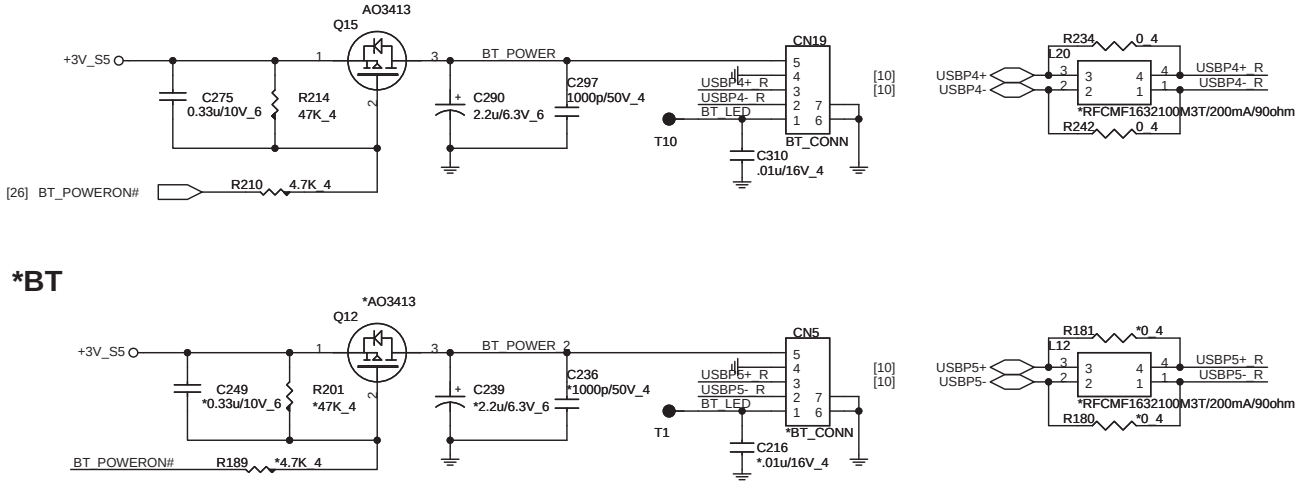
USB

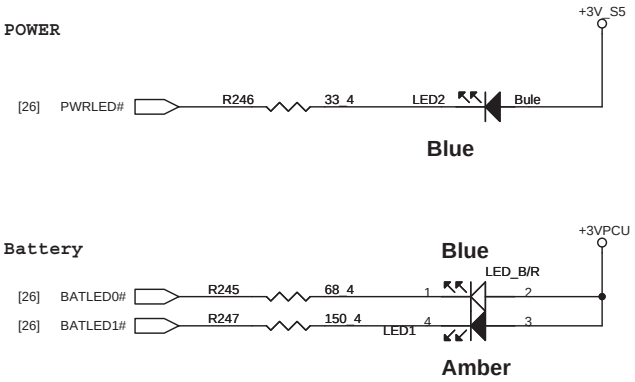


BT

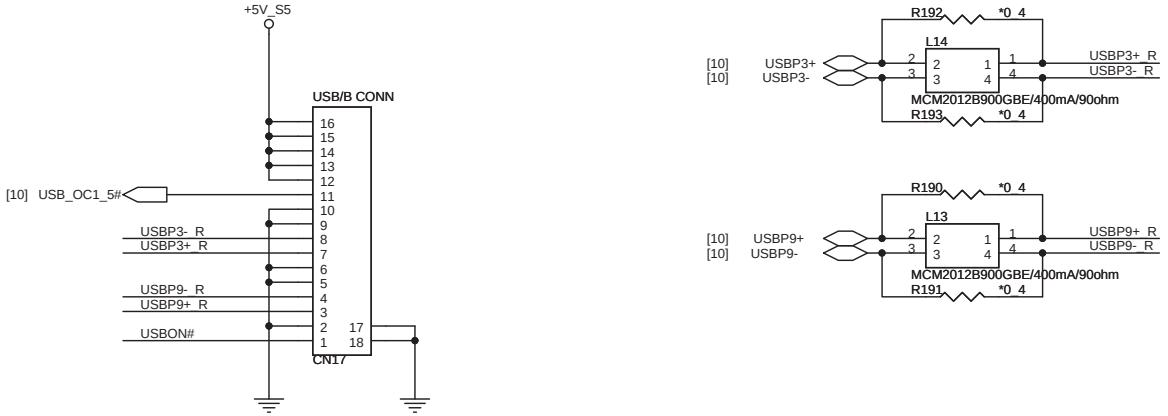


*BT

LED



USB/B



Quanta Computer Inc.

PROJECT : ZRL

Size	Document Number	Rev
	USB/ BT	1A
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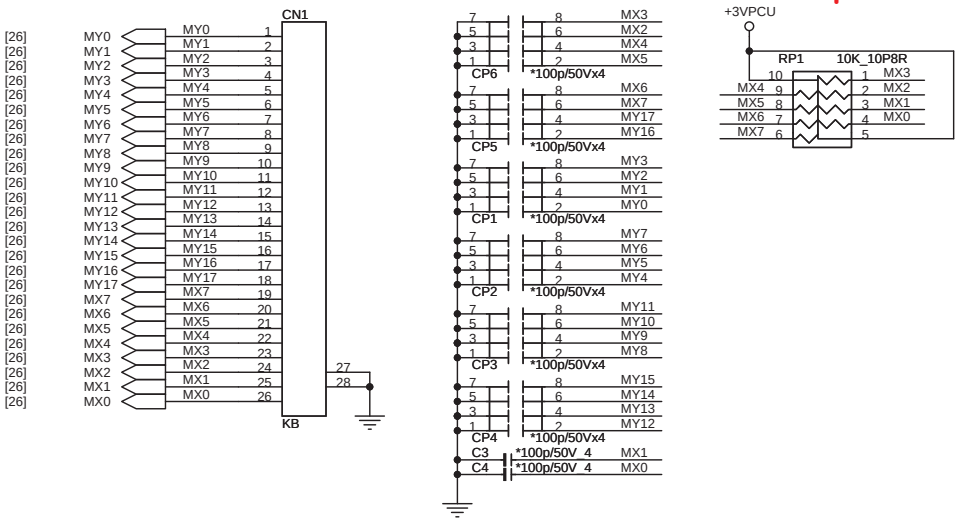
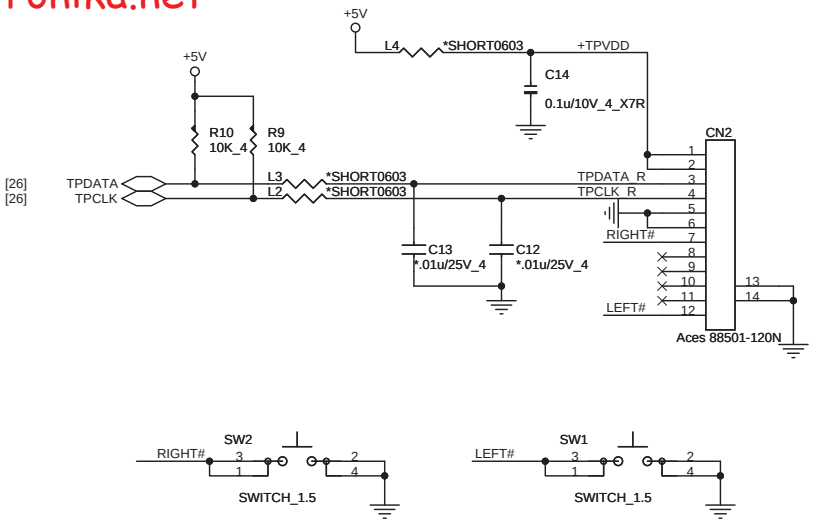
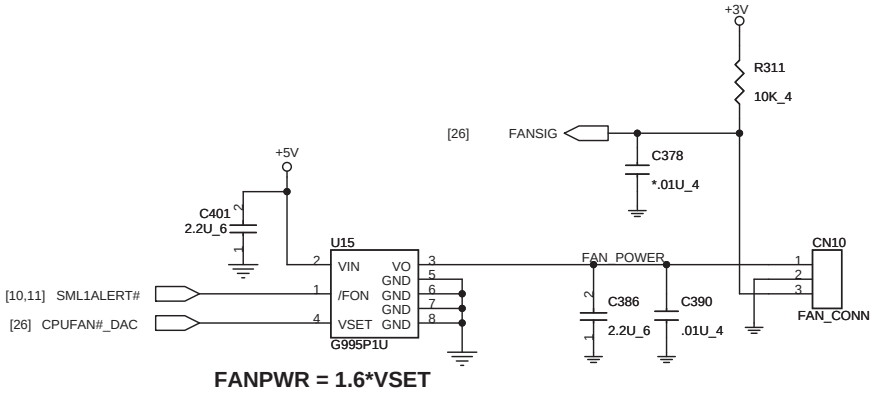
K/B



TP

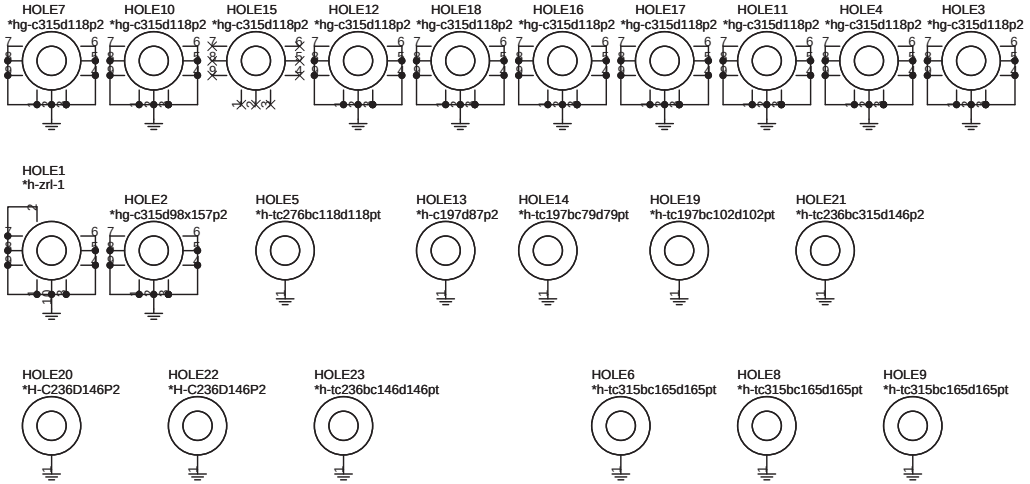


CPU FAN

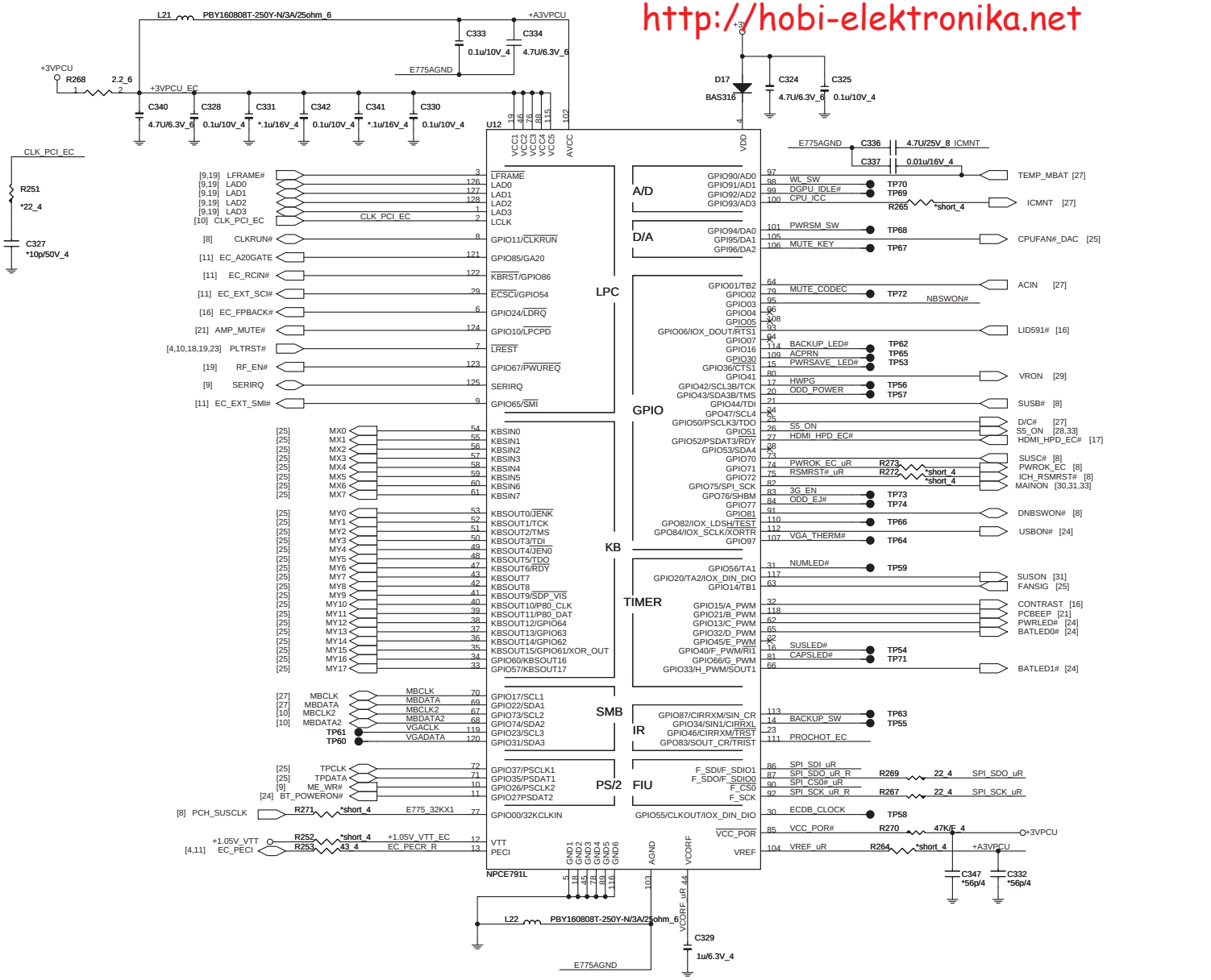


FANPWR = 1.6*VSET

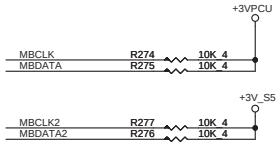
HOLE

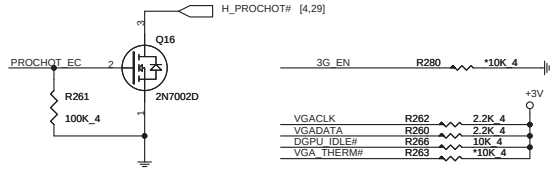


Quanta Computer Inc.		
PROJECT : ZRL		
Size	Document Number: KB/FAN/TP+FP	Rev: 1A
Date: Tuesday, June 21, 2011	Sheet 25 of 34	

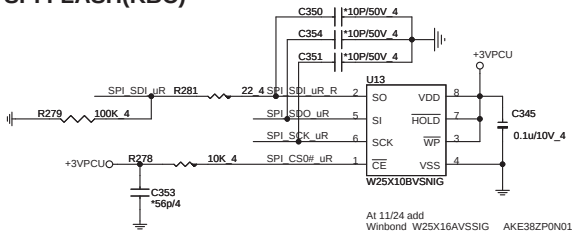


SM BUS PU(KBC)

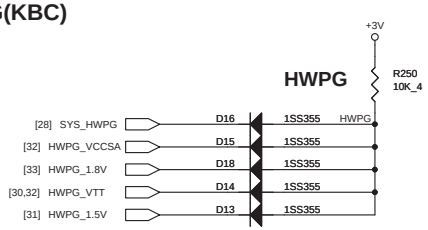




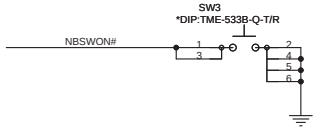
SPI FLASH(KBC)



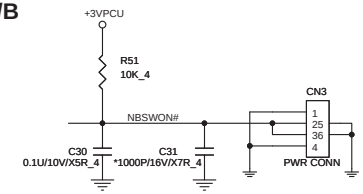
HWPG(KBC)



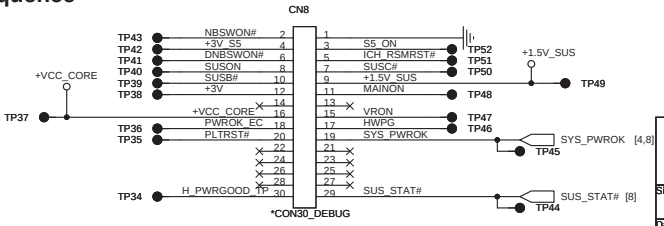
POWER-ON Switch(KBC)

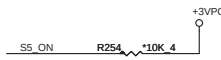


PWR/B

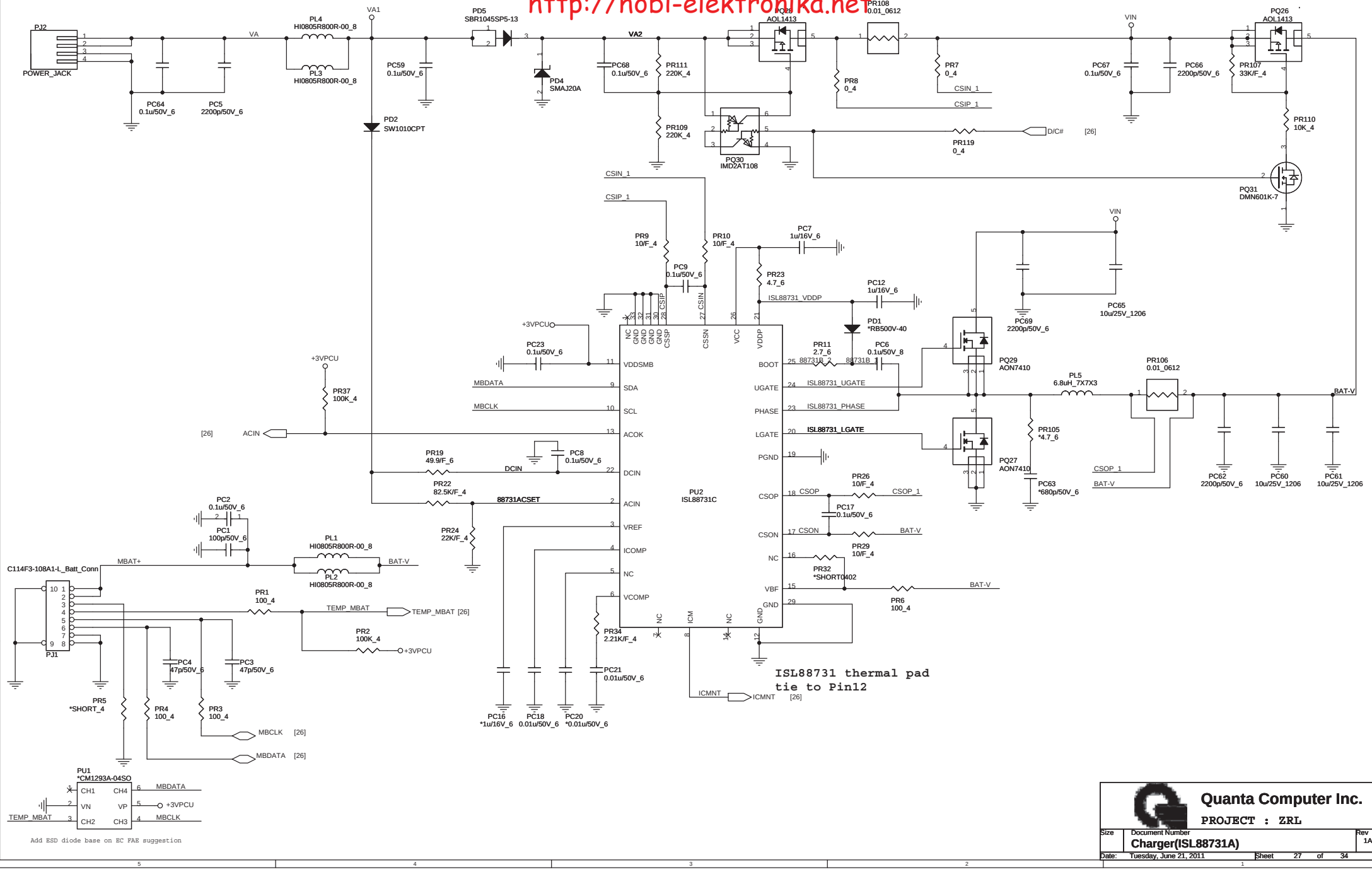


Power sequence





Quanta Computer Inc.			
PROJECT : ZRL			
Size	Document Number		Rev
	WPCE791 & FLASH		1A
Date: Tuesday, June 21, 2011	Sheet 26 of 34		



Quanta Computer Inc.			
PROJECT : ZRL			
Size	Document Number		Rev
	Charger(ISL88731A)		1A
Date: Tuesday, June 21, 2011		Sheet 27 of 34	

MAIND → MAIND [6,31,33]

SYS_SHDN# → SYS_SHDN# [4,33]

Ven=7.23V

[26] SYS_HWPG

+5VPCU
5 Volt +/- 5%
TDC : 4.125A
PEAK : 5.5A
OCP : 6.6A
Width : 170mil

+3VPCU
3.3 Volt +/- 5%
TDC : 3.86A
PEAK : 5.15A
OCP : 6.2A
Width : 160mil

OCP:6.6A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
=2.525A
Iocp=6.6-(2.525/2)=5.34A
Vth=5.34A*14mOhm=0.07472mV
R(Ilim)=(74.72mV*10)/10uA
~74.723K

OCP:6.2A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
~1.9A
Iocp=6.2-(1.9/2)=5.25A
Vth=5.25A*14mOhm=0.0735V
R(Ilim)=(73.5mV*10)/10uA
=73.5K

TDC : 2.25A
PEAK : 3A
Width : 100mil

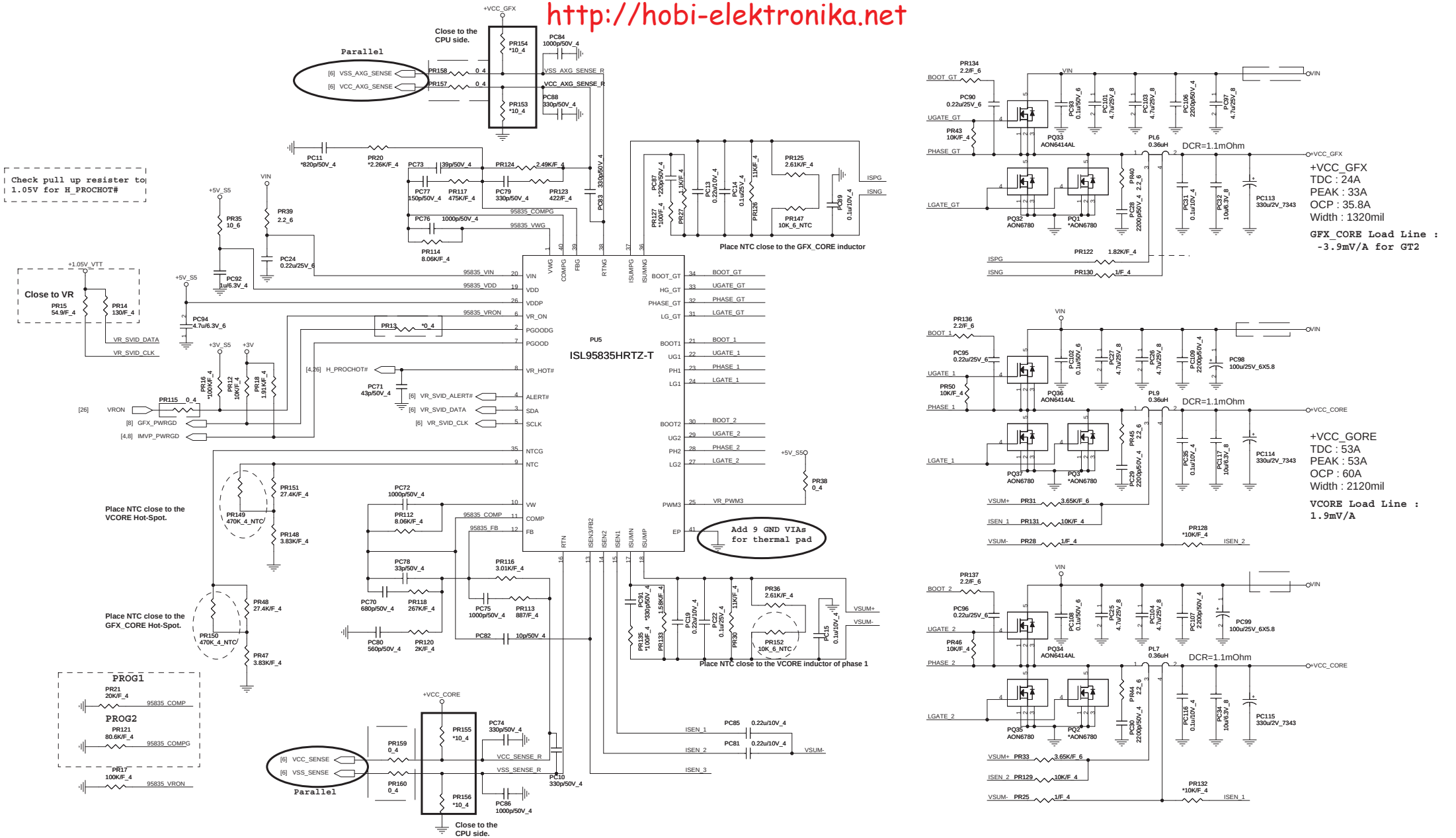
TDC : 1.88A
PEAK : 2.5A
Width : 80mil

TDC : 2.74A
PEAK : 3.65A
Width : 110mil

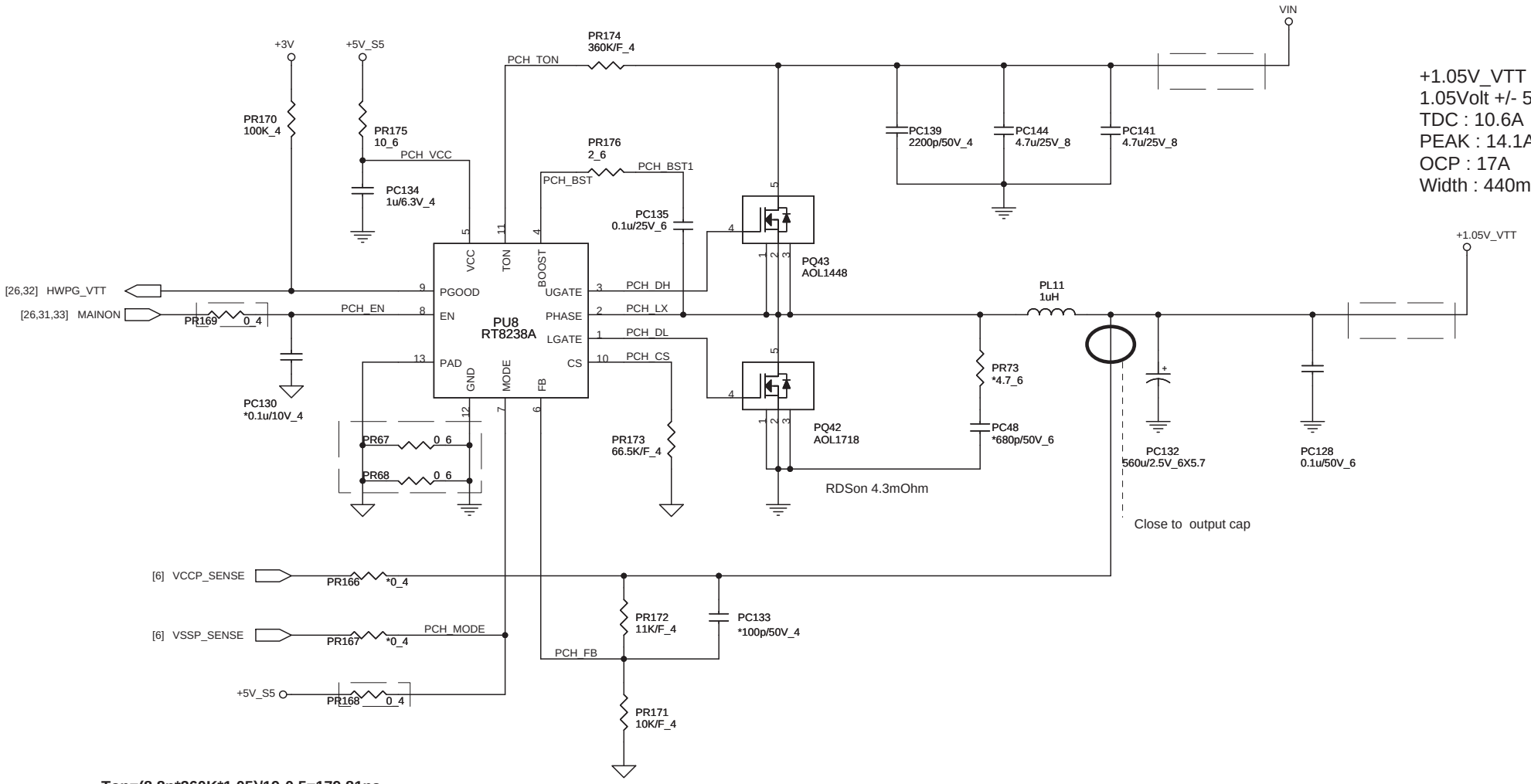
TDC : 0.16A
PEAK : 0.21A
Width : 10mil

Quanta Computer Inc.
PROJECT : ZRL

Size	Document Number	Rev
	SYSTEM 5V/3V (RT8223M)	1A
Date: Tuesday, June 21, 2011	Sheet 28 of 34	



Quanta Computer Inc.		
PROJECT : ZRL		
Size	Document Number: +VCC_CORE & +VCC_GFX (ISL95835)	Rev: 1A
Date: Tuesday, June 21, 2011	Sheet 29 of 34	



Ton=(8.8p*360K*1.05)/19-0.5=179.81ns
Lcurrent=(19-1.05)*179ns/1uH=3.228A
Iocp=17-3.228/2=15.386A
Vcs=15.386*4.3mohm=0.06616V
Rcs=0.06616/1u=66.16Kohm

VOUT=(1+R1/R2)*0.5

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Size	Document Number: +PCH&VTT (RT8238A)	Rev: 1A
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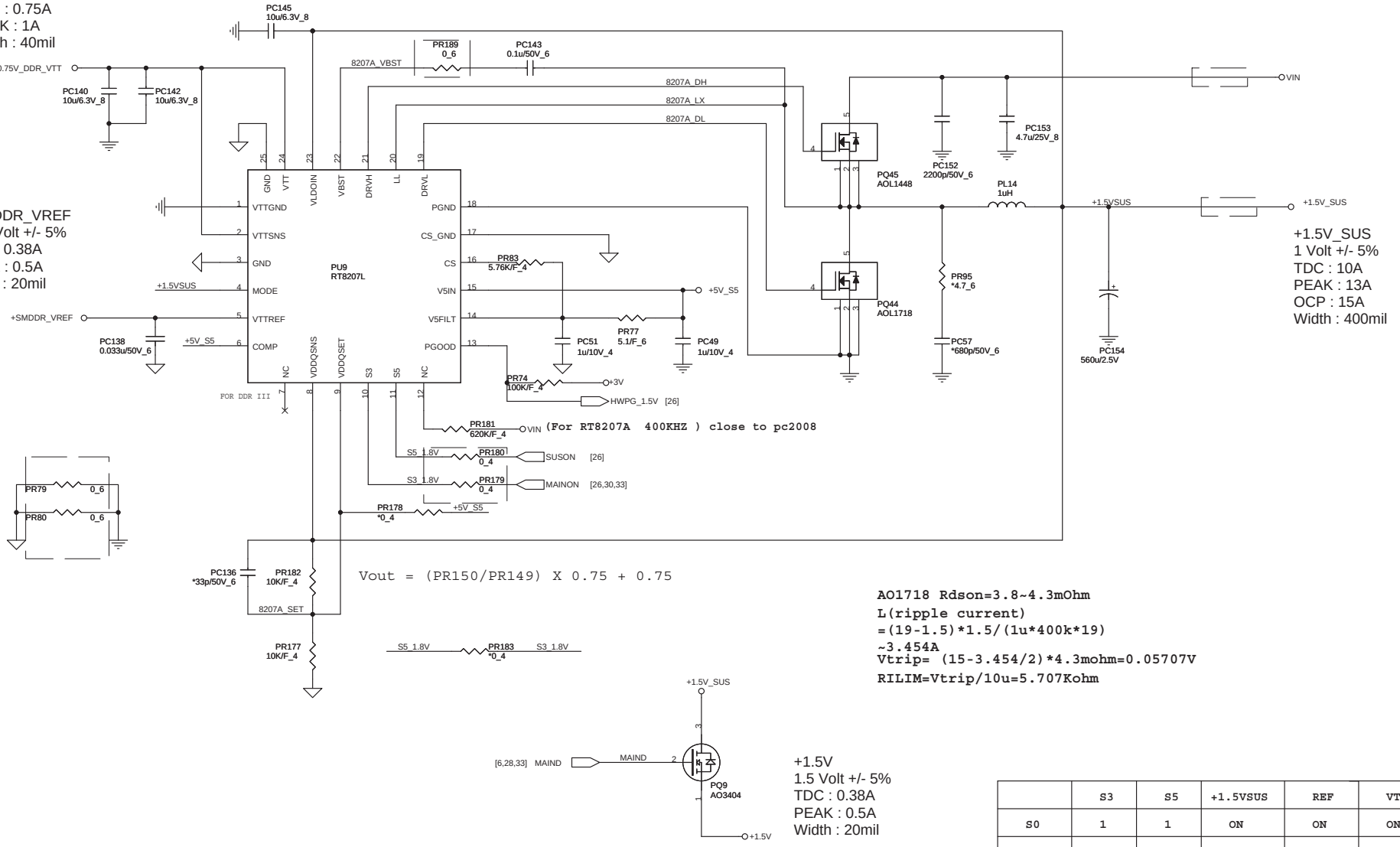
+0.75V_DDR_VTT
0.75 Volt +/- 5%
TDC : 0.75A
PEAK : 1A
Width : 40mil

+SMDDR_VREF
0.75 Volt +/- 5%
TDC : 0.38A
PEAK : 0.5A
Width : 20mil



Vout = (PR150/PR149) X 0.75 + 0.75

AO1718 Rdson=3.8~4.3mOhm
L(ripple current)
=(19-1.5)*1.5/(1u*400k*19)
~3.454A
Vtrip= (15-3.454/2)*4.3mohm=0.05707V
RILIM=Vtrip/10u=5.707Kohm

+1.5V
1.5 Volt +/- 5%
TDC : 0.38A
PEAK : 0.5A
Width : 20mil

+1.5V_SUS
1 Volt +/- 5%
TDC : 10A
PEAK : 13A
OCP : 15A
Width : 400mil

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZRL

Size	Document Number	Rev
	DDR 1.5V(RT8207A)	1A
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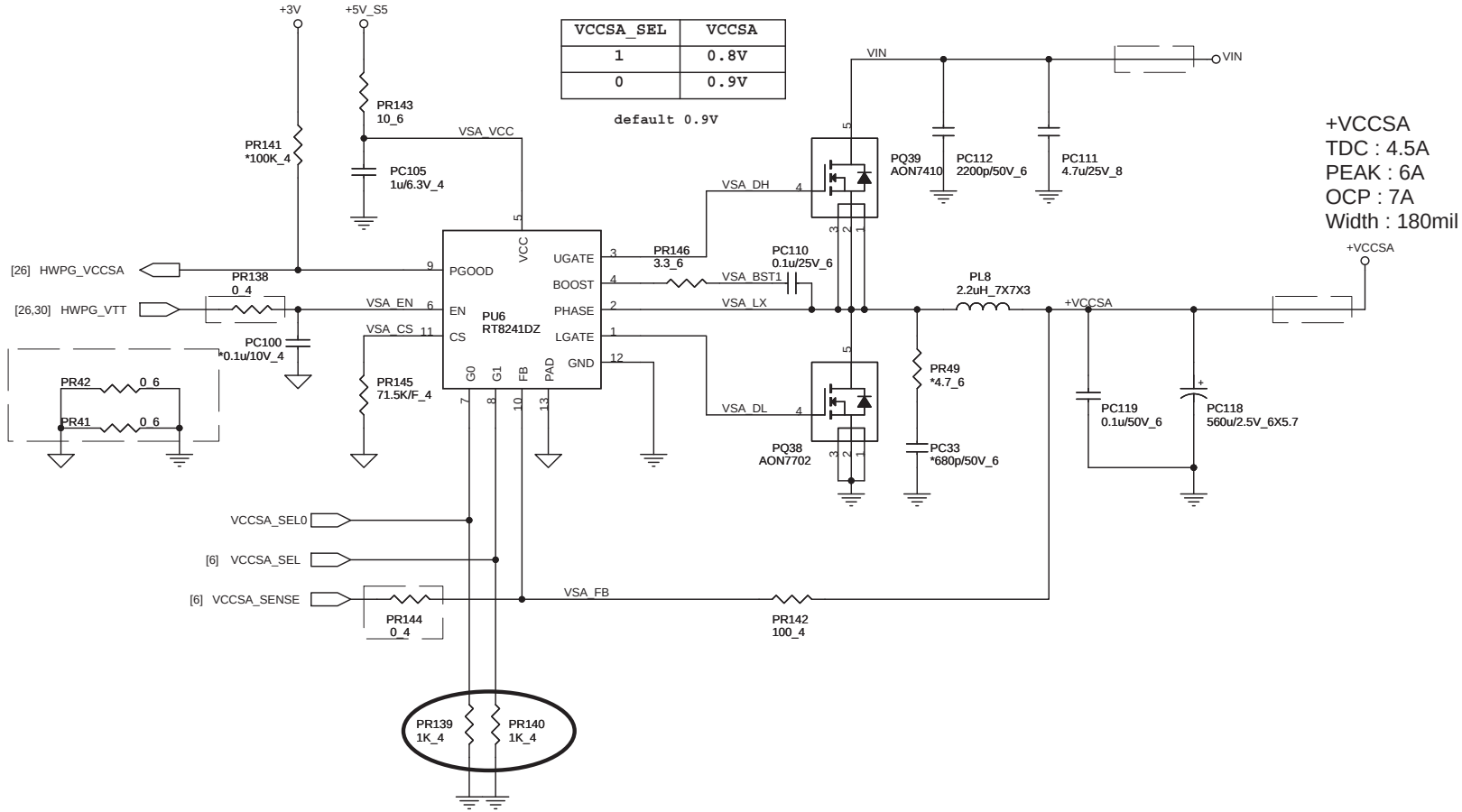
G0	G1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

VCCSA_SEL	VCCSA
1	0.8V
0	0.9V

default 0.9V



+VCCSA
TDC : 4.5A
PEAK : 6A
OCP : 7A
Width : 180mil

OCP=7A
Iripple=(19-0.9)*0.9/(2.2u*300K*19)
=1.299A
Rth=14mohm*8*(7-0.65)/10uA
=71.125K
Ipeak=8.299A

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Size	Document Number	Rev
	+VCCSA	1A
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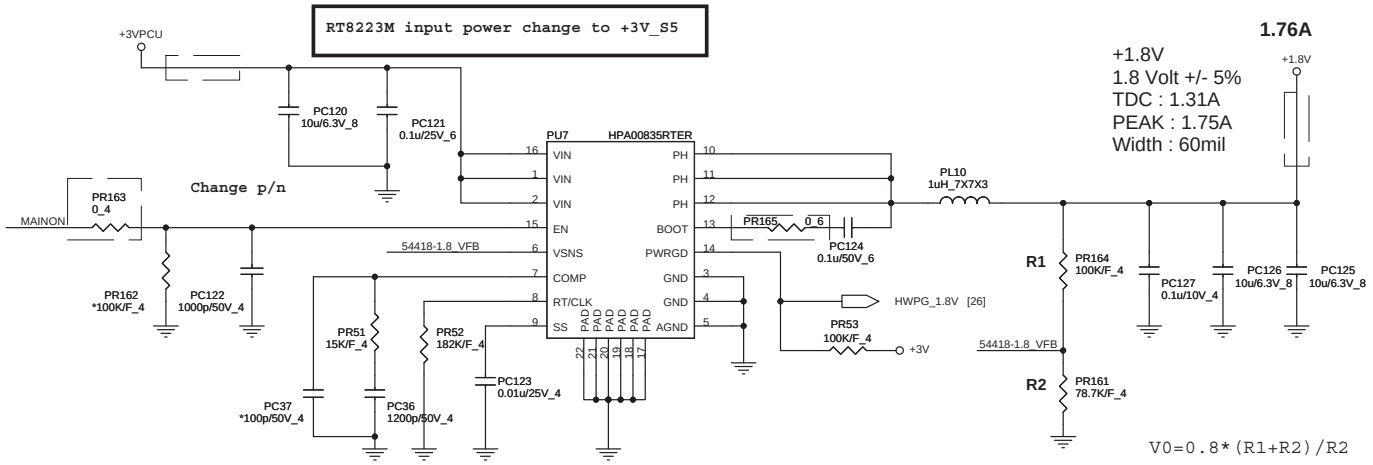
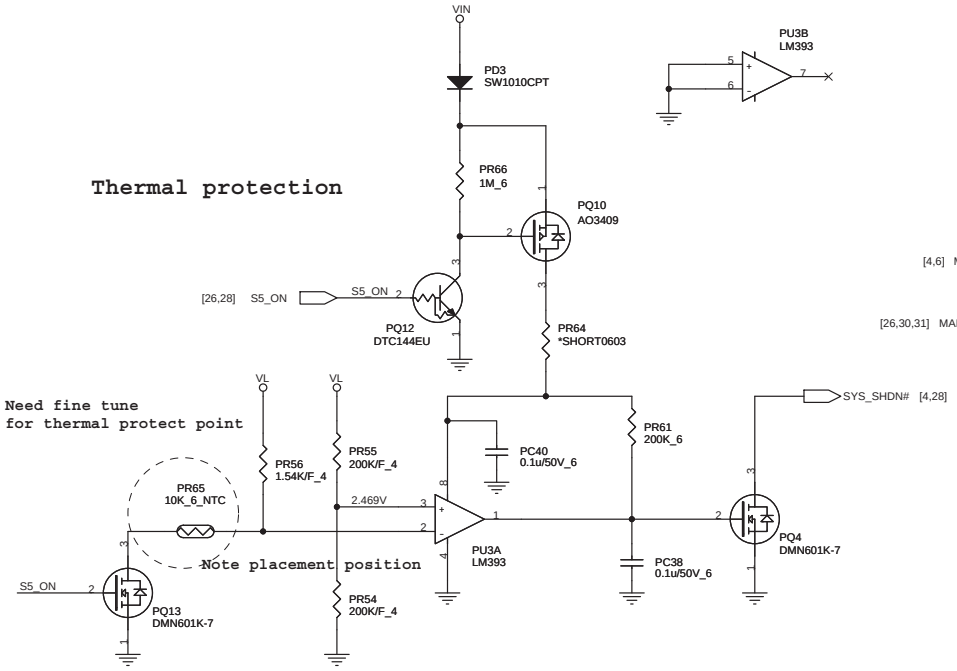
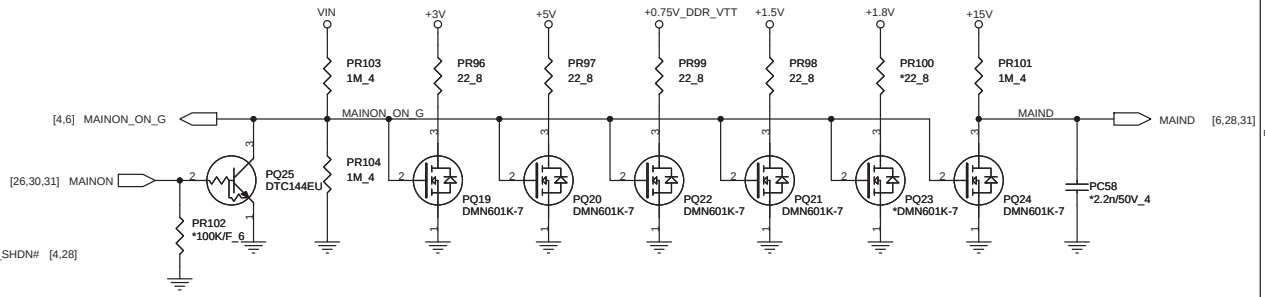


For EC control thermal protection (output 3.3V)





Quanta Computer Inc.

PROJECT : ZRL

Size	Document Number	Rev
	Discharge/1.8V)	1A

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1 7/7 modify

CHANGE LIST

Model	date	CHANGE LIST
ZRL	5/18	page16 : L6,L8,L10 change to 0ohm C104,C86,C68 remove for monitor issue L5,L7,L9 change to 0603 package
		page 8 : add R422 for GFX_PWRGD
		page 27 :PQ26,PQ28 change footprint
		page 17 :Remove U6 HDMI level shift
		page 9 :add Q26,R423 to separate CODEC SYNC signal
		page 22 :change R239,R240 to 47 ohm by realtek
	5/25	page 29 : change PR133 to 1.58K, PR124 to 2.49K ,PC22,PC14 to 0.1u
		page 22 : remove Q25,Q24, stuff R236,R235 fix POPO sound
	6/9	page 24 : change R246 to 33ohm,R245 to 68ohm, R247 to 150ohm for LED brightness.
	2A	

MODEL	ZRL	
	FROM	To
	X	1A
	X	1A
	X	1A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
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	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
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	B2A	C3A
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	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
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	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
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	B2A	C3A
	B2A	C3A
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	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A

Quanta Computer Inc.
PROJECT : ZRL

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	Change list2	1A

Date: Tuesday, June 21, 2011 Sheet 34 of 34

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