AJ6 SYSTEM DIAGRAM

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SVCC
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : GND
- LAYER 6 : BOT

DDRII-SODIMM1 PAGE 6,7 — DDRII 667/800 MHz

DDRII-SODIMM2 PAGE 6,7 — DDRII 667/800 MHz

AMD Griffin Lion Sabie
S1G2 Processor
638P (uPGA)/35W
PAGE 3,4,5

CPU THERMAL SENSOR PAGE 5

14.31818MHz

CLOCK GEN
SLG8SP628
PAGE 2

CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK

HT3

PCI-E

PCI-Express 16X

NORTH BRIDGE
RS780MN
29mm X 29mm, 528pin BGA
PAGE 8,9,10,11,

HDMI PAGE 18

CRT PAGE 20

LVDS PAGE 19

MXM CONN
PAGE 17

LAN
PCIE-LAN
MARVELL_88E8057
(10/100/GagaLAN)
PAGE 21

Express Card X1
(NEW CARD)
PAGE 30

Mini PCI-E Card
(Wireless LAN)
PAGE 25

RJ45 PAGE 21

PCIE X4

SBSRC_CLK

USB2.0

SOUTH BRIDGE
SB700
21mm X 21mm, 528pin BGA
4.5W(Ext)
4.3W(Int)
PAGE 12,13.14.15.16

SATA - HDD PAGE 24 — SATA0 300MB

SATA - ODD PAGE 24 — SATA4 300MB

7	1	4,5	11	0,2,8,9
Camera PAGE 19	Bluetooth PAGE 26	Mini PCI-E X2 PAGE 25	Express Card X1 (NEW CARD) PAGE 30	USB2.0 Ports X2 PAGE27

USB (small/B) X2 PAGE26

PCI BUS / 33MHz

CARD reader
OZ126T
PAGE 22

Azalia

CX20561
AUDIO CODEC
PAGE 23

MDC CONN
PAGE 26

RJ11
PAGE 26

AUDIO Amplifier
TPA6017A2
PAGE 23

AUDIO CONN
(Phone/ MIC)
PAGE 23

Speaker Conn.
PAGE 23

LPC

Keyboard PAGE 29
Touch Pad PAGE 29

KBC
ITE
IT8502
PAGE 28

FAN PAGE 28

SPI FLASH PAGE 28

SYSTEM CHARGER PAGE 31

SYSTEM POWER PAGE 32

DDR II SMDDR_VTERM
1.8V/1.8VSUS
PAGE 34

VCCP +1.2V & +1.1V
PAGE 33

CPU CORE +VCORE0 +VCORE1
PAGE 37

SMBUS TABLE

SB--SCL0/SD0	Clock gen /DDR2/DDR2 thermal/Accelerometer	+3V
SB--SCL1/SD1	Wlan Card	+3V/S5
SB--SCL2/SD2	epress card	+3v/S5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

NB2/RD1

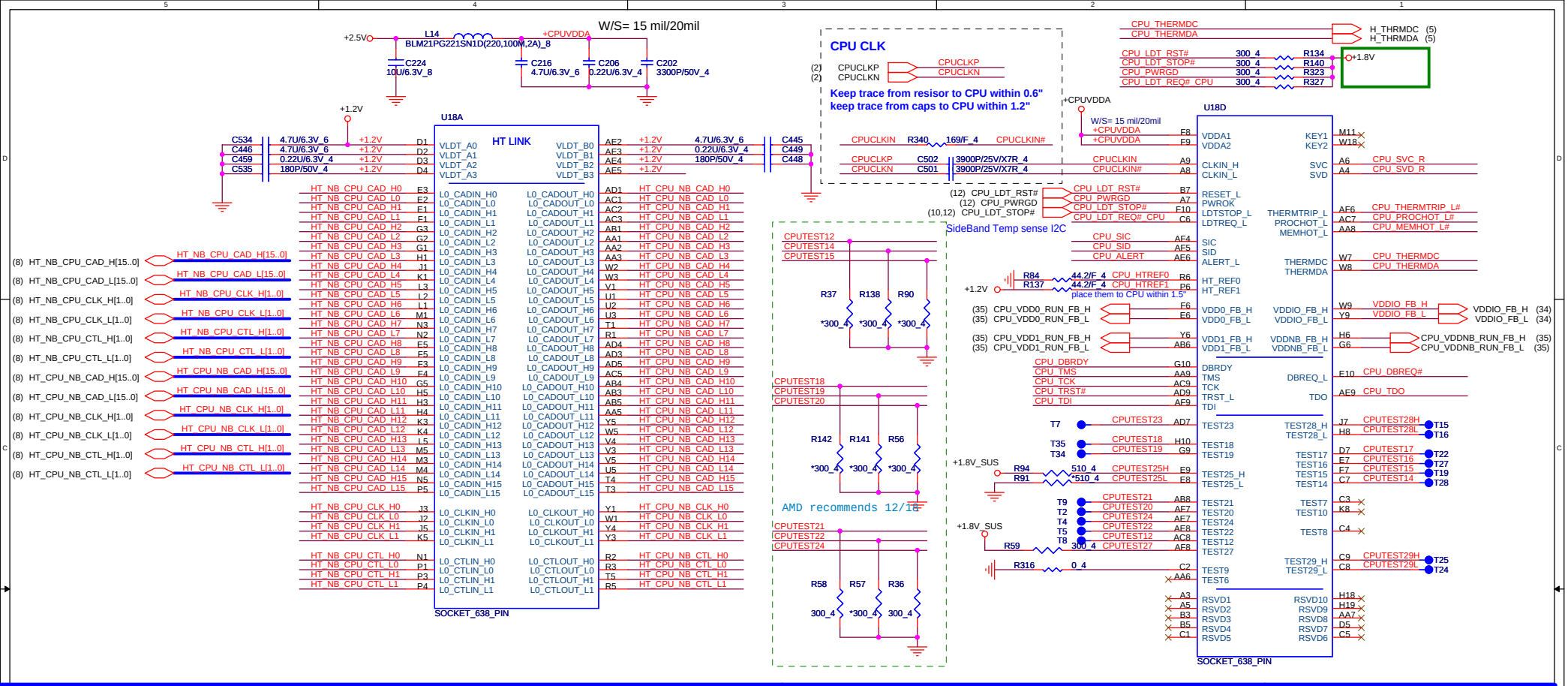
PROJECT : AJ6
Quanta Computer Inc.

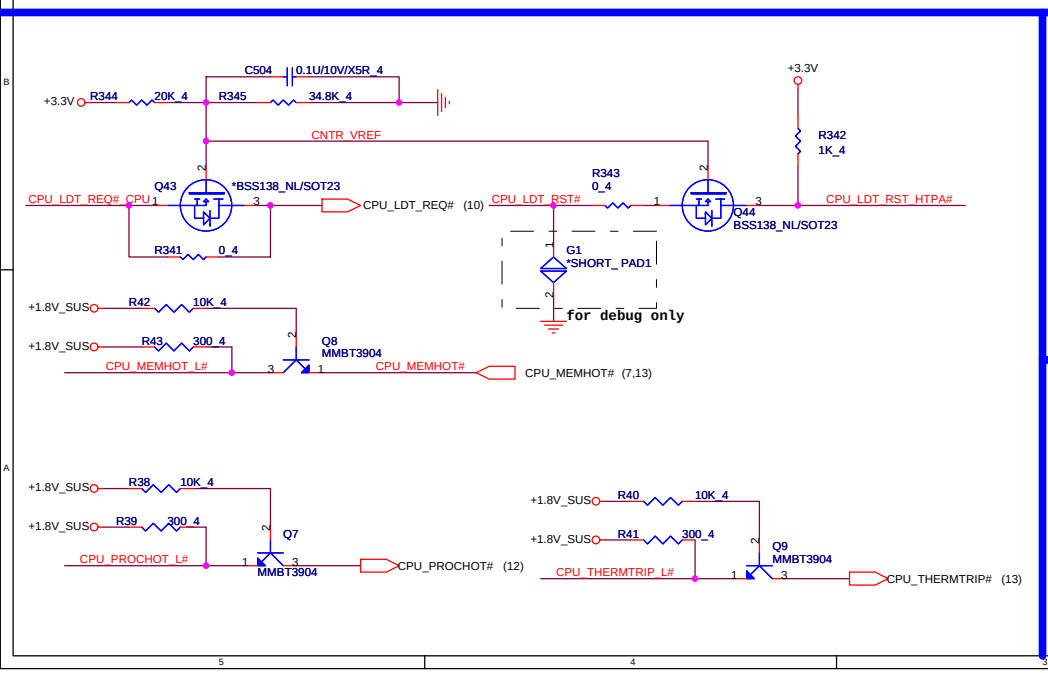
Size	Document Number	Rev
Custom	Block Diagram	1A

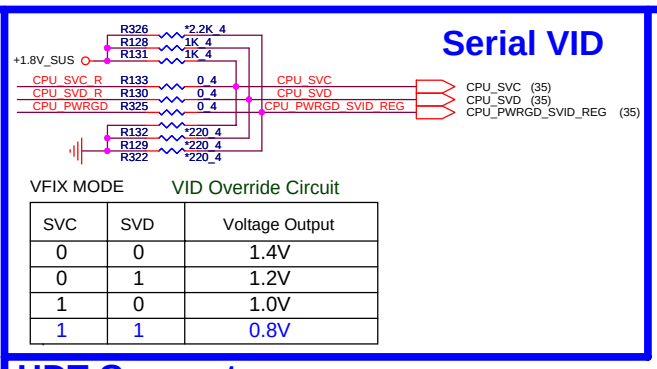
Date: Monday, August 18, 2008 | Sheet 1 of 39

CLOCKS name	UMA	RS780	Clock pin function
NBGFX_CLKP NBGFX_CLKN	RP64 STUFF	RP64 STUFF	to NB for VGA reference clock
EXT_GFX_CLKP EXT_GFX_CLKN	RP5053 NC	RP5053 STUFF	to M86-M external reference clock
NBGPP_CLKP NBGPP_CLKN	RP70 STUFF	RP70 NC	to NB for RX780 for PCIEX2 interface reference clock only RS780 is internal share with AC-LINK clock,RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP72 STUFF	RP72 STUFF	to NB for AC-LINK reference clock

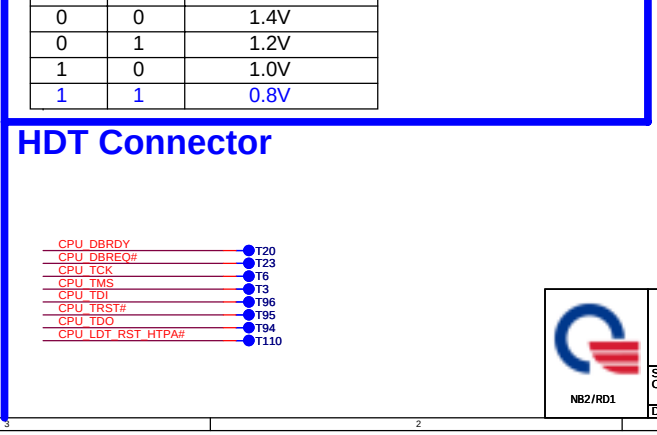
60 ohm, 0.5A
+1.2V
L43 BLM18PG221SN1D(220,1.4A)_6
600 ohms@100Mhz
C648 100P/50V/NPO_4
C532 10U/6.3V_8
C512 0.1U/10V/X5R_4
C515 0.1U/10V/X5R_4
+1.2V_CLKVDDIO
C531 0.1U/10V/X5R_4
C513 0.1U/10V/X5R_4
C524 0.1U/10V/X5R_4
EMI request. 18/08/2008
DCR: 0.5 ohm
600 ohms@100Mhz
+3V_CLKVDD
+3.3V
L45 BLM18PG221SN1D(220,1.4A)_6
60 ohm, 0.5A
C537 10U/6.3V_8
C516 0.1U/10V/X5R_4
C526 0.1U/10V/X5R_4
C538 0.1U/10V/X5R_4
C546 0.1U/10V/X5R_4
C547 0.1U/10V/X5R_4
C514 0.1U/10V/X5R_4
C530 0.1U/10V/X5R_4
C511 0.1U/10V/X5R_4
EMI reserved
Place within 0.5" of CLKGEN
U23
QFN64
SLG8SP628VTR
RELTAK AL000880001
Place very close to C/G
+3V_CLKVDD
L44 BLM18PG221SN1D(220,1.4A)_6
+3V_CLK_VDDA
C545 2.2U/6.3V/X5R_6
C552 0.1U/10V/X5R_4
+1.2V_CLKVDDIO
C289 33P/50V/NPO_4
CG_XIN
Y2 14.318MHZ
C288 33P/50V/NPO_4
CG_XOUT
VDDDOT
VDDSRC
VDDATIG
VDDSB_SRC
VDDSATA
VDDCPU
VDDHTT
VDDREF
VDD48
VDDSRC_IO0
VDDSRC_IO1
VDDATIG_IO
VDDSB_SRC_IO
VDDCPU_IO
GND48
GNDDOT
GNDSRC0
GNDSRC1
GNDATIG
GNDSB_SRC
GNDSATA
GNDCPU
GNDHTT
GNDREF
X1
X2
PCLK_SMB
PDAT_SMB
SMBCLK
SMBDAT
CLK_PD#
PD#
(25) MINI1CLK_REQ#
(25) MINI2CLK_REQ#
(30) NEW-CARD_CLK_REQ#
CLKREQ0#
CLKREQ1#
CLKREQ2#
CLKREQ3#
CLKREQ4#
TGND0 TGND1 TGND2 TGND3 TGND4 TGND5 TGND6 TGND7 TGND8 TGND9
CPUK8_0T
CPUK8_0C
CPUCLK0P
CPUCLK0N
RP51
0_4P2R
CPUCLKP
CPUCLKN
CPUCLKP (3)
CPUCLKN (3)
ATIG0T
ATIG0C
ATIG1T
ATIG1C
NBGFXCLK0P
NBGFXCLK0N
EXTGFXCLK0P
EXTGFXCLK0N
RP43
RP44
NBGFX_CLKP
NBGFX_CLKN
EXT_GFX_CLKP
EXT_GFX_CLKN
NBGFX_CLKP (10)
NBGFX_CLKN (10)
EXT_GFX_CLKP (17)
EXT_GFX_CLKN (17)
SB_SRC0T
SB_SRC0C
SB_SRC1T
SB_SRC1C
PCILANCLK0P
PCILANCLK0N
SBLINKCLK0P
SBLINKCLK0N
RP48
RP42
PCIE_LAN_CLKP
PCIE_LAN_CLKN
SBLINK_CLKP
SBLINK_CLKN
PCIE_LAN_CLKP (21)
PCIE_LAN_CLKN (21)
SBLINK_CLKP (10)
SBLINK_CLKN (10)
SRC0T
SRC0C
SRC1T
SRC1C
SRC2T
SRC2C
SRC3T
SRC3C
SRC4T
SRC4C
PCIEMINICLK1P
PCIEMINICLK1N
PCIEMINICLK2P
PCIEMINICLK2N
NBGPPCLK0P
NBGPPCLK0N
PCIENEWCLK0P
PCIENEWCLK0N
SBSRCCLK0P
SBSRCCLK0N
RP46
RP45
RP47
RP49
RP50
PCIE_MINI1_CLKP
PCIE_MINI1_CLKN
PCIE_MINI2_CLKP
PCIE_MINI2_CLKN
NBGPP_CLKP
NBGPP_CLKN
PCIE_NEW_CLKP
PCIE_NEW_CLKN
SBSRC_CLKP
SBSRC_CLKN
PCIE_MINI1_CLKP (25)
PCIE_MINI1_CLKN (25)
PCIE_MINI2_CLKP (25)
PCIE_MINI2_CLKN (25)
NBGPP_CLKP (10)
NBGPP_CLKN (10)
PCIE_NEW_CLKP (30)
PCIE_NEW_CLKN (30)
SBSRC_CLKP (12)
SBSRC_CLKN (12)
SRC6T/SATAT
SRC6C/SATAC
SRC7T/27M_SS
SRC7C/27M_NS
CLK_VGA_27M_SS
CLK_VGA_27M_NSS
T38
T37
T39
T113
HTT0T/66M
HTT0C/66M
NBHTREFCLK0P
NBHTREFCLK0N
R375 0_4
R374 0_4
NBHT_REFCLKP
NBHT_REFCLKN
NBHT_REFCLKP (10)
NBHT_REFCLKN (10)
48MHz_0
CLK48MUSB
R363 33_4
CLK_48M_USB
CLK_48M_USB (13)
REF0/SEL_HTT66
REF1/SEL_SATA
REF2/SEL_27
SEL_HT66
SEL_SATA
SEL_27
C536 *10P/50VC0G_4
R385 *261_4
Ra
Rb
R377 158/F_4
R389 90.9/F_4
EXT_NB_OSC (10)
RES CHIP 130 1/16W +-1%(0402)L-F -->CS11302FB15
RES CHIP 158 1/16W +-1%(0402) -->CS11582FB00
RES CHIP 90.9 1/16W +-1%(0402) -->CS09092FB15
RES CHIP 82.5 1/16W +-1%(0402) -->CS08252FB11
Clock chip has internal serial terminations
for differential pairs, external resistors are
reserved for debug purpose.
* default
SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock
+3V_CLKVDD
R171 8.2K_4
SEL_SATA
SEL_27
R175 *8.2K_4
R376 8.2K_4
RS780M/RX780M
+3.3V
CLK_PD#
R373 8.2K_4
	RX780 1.8V	RS780 1.1V
Ra	82.5R	158R
Rb	130R	90.9R
SLG8SP628VTR P/N : AL8SP628000
RTM880N-796 P/N : AL000880000
PROJECT : AJ6
Quanta Computer Inc.
NB2/RD1
Size Custom
Document Number Clock Gen
Rev 3B
Date: Thursday, August 21, 2008
Sheet 2 of 39

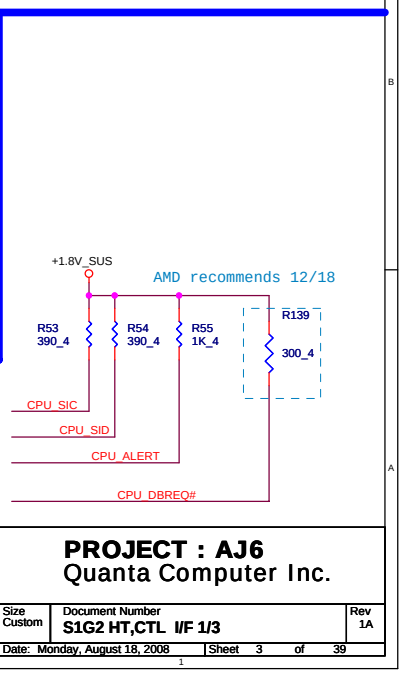






SVC	SVD	Voltage Output
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V





NB2/RD1	PROJECT : AJ6 Quanta Computer Inc.		
Size: Custom	Document Number: S1G2 HT,CTL I/F 1/3		Rev: 1A
Date: Monday, August 18, 2008	Sheet 3 of 39		

Processor Memory Interface

PLACE THEM CLOSE TO CPU WITHIN 1"

U18B — SOCKET_638_PIN

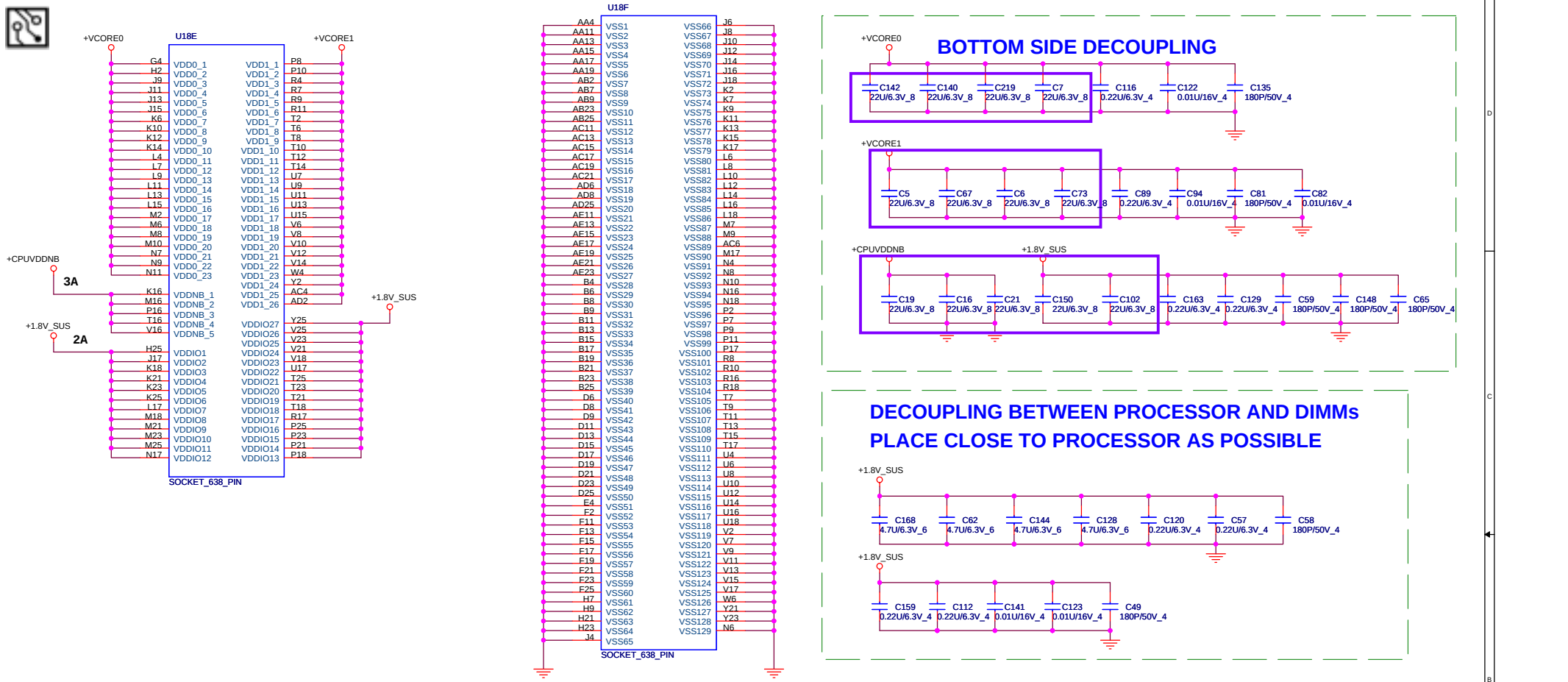
U18C — MEM:DATA — SOCKET_638_PIN

750 mA

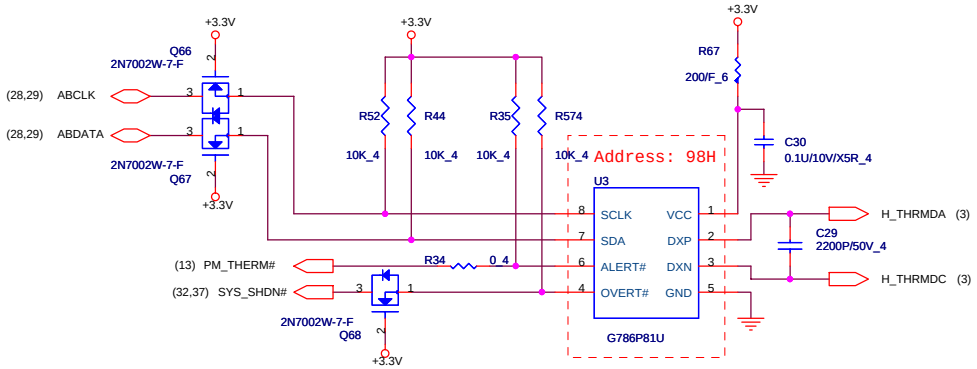
Place close to socket

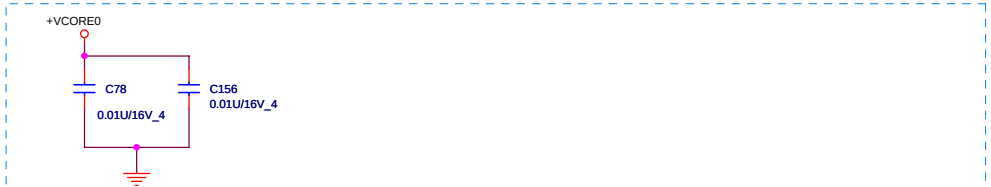
Close to CPU within 1200 mils

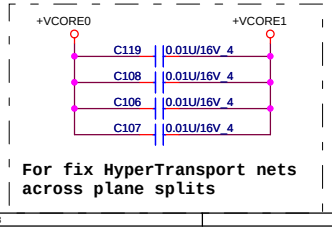
Project	PROJECT : AJ6
Company	Quanta Computer Inc.
Size	Custom
Document Number	S1G2 DDRII MEMORY I/F 2/3
Rev	1A
Date	Monday, August 18, 2008
Sheet	4 of 39



PROCESSOR POWER AND GROUND





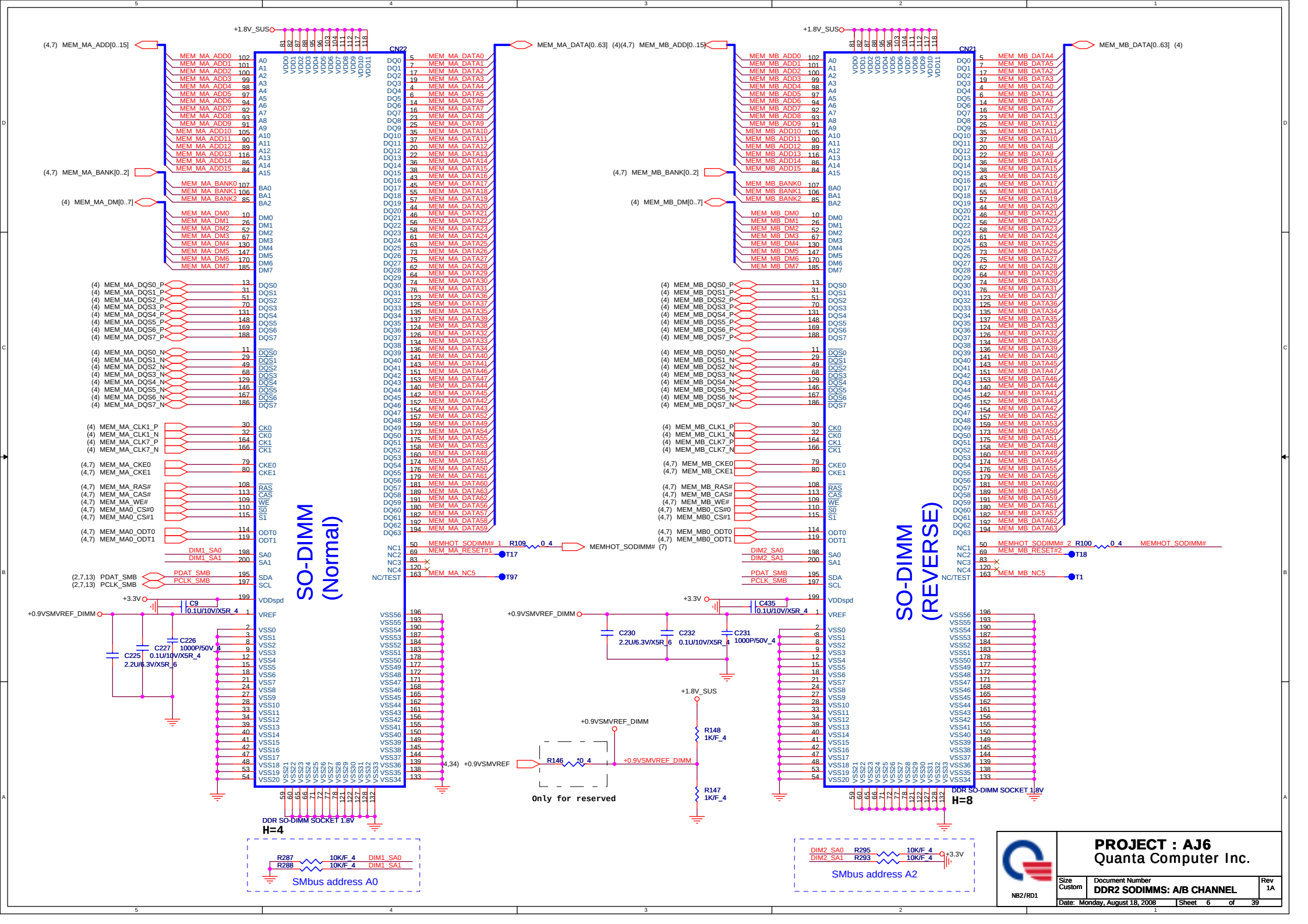


PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	S1G2 PWR & GND 3/3	2A

NB2/RD1

Date: Tuesday, August 19, 2008 | Sheet 5 of 39


SO-DIMM (Normal)
CN22
DDR SO-DIMM SOCKET 1.8V
H=4
SO-DIMM (REVERSE)
CN21
DDR SO-DIMM SOCKET 1.8V
H=8
Only for reserved
SMbus address A0
SMbus address A2
PROJECT : AJ6
Quanta Computer Inc.
DDR2 SODIMMS: A/B CHANNEL
NB2/RD1
Date: Monday, August 18, 2008
Sheet 6 of 39

(4,6) MEM_MA_ADD[0..15] → MEM_MA_ADD[0..15]
(4,6) MEM_MA_BANK[0..2] → MEM_MA_BANK[0..2]

+0.9VSMVTT

(4,6) MEM_MA_CKE0 — MEM_MA_CKE0 RP35 — MEM_MA_BANK2 — MEM_MA_ADD12 RP32 — MEM_MA_ADD9 — MEM_MA_ADD8 RP27 — MEM_MA_ADD5 — MEM_MA_ADD3 RP23 — MEM_MA_ADD1 — MEM_MA_ADD10 RP17 — MEM_MA_BANK0 — MEM_MA_WE# RP14 — MEM_MA_CAS# — MEM_MA0_ODT1 RP9 — MEM_MA0_CS#1 — MEM_MA_ADD15 RP34 — MEM_MA_CKE1 — MEM_MA_ADD7 RP30 — MEM_MA_ADD14 — MEM_MA_ADD6 RP26 — MEM_MA_ADD11 — MEM_MA_ADD2 RP21 — MEM_MA_ADD4 — MEM_MA_BANK1 RP19 — MEM_MA_ADD0 — MEM_MA0_CS#0 RP12 — MEM_MA_RAS# — MEM_MA_ADD13 RP10 — MEM_MA0_ODT0

(4,6) MEM_MA_WE#
(4,6) MEM_MA_CAS#
(4,6) MEM_MA0_ODT1
(4,6) MEM_MA0_CS#1
(4,6) MEM_MA_CKE1
(4,6) MEM_MA0_CS#0
(4,6) MEM_MA_RAS#
(4,6) MEM_MA0_ODT0

47_4P2R_4

C126 C154 C84 C130 C99 C44 C90 C97 C93 C47 C111 C117 C74 C48 C88 C109
0.1U/10V/X5R_4
+1.8V_SUS

(4,6) MEM_MB_ADD[0..15] → MEM_MB_ADD[0..15]
(4,6) MEM_MB_BANK[0..2] → MEM_MB_BANK[0..2]

+0.9VSMVTT

(4,6) MEM_MB_CKE0 — MEM_MB_CKE0 RP31 — MEM_MB_BANK2 — MEM_MB_ADD12 RP28 — MEM_MB_ADD9 — MEM_MB_ADD8 RP24 — MEM_MB_ADD5 — MEM_MB_ADD3 RP22 — MEM_MB_ADD1 — MEM_MB_ADD10 RP16 — MEM_MB_BANK0 — MEM_MB_WE# RP13 — MEM_MB_CAS# — MEM_MB0_ODT1 RP8 — MEM_MB0_CS#1 — MEM_MB_CKE1 RP33 — MEM_MB_ADD15 — MEM_MB_ADD7 RP29 — MEM_MB_ADD14 — MEM_MB_ADD6 RP25 — MEM_MB_ADD11 — MEM_MB_ADD2 RP20 — MEM_MB_ADD4 — MEM_MB_BANK1 RP18 — MEM_MB_ADD0 — MEM_MB0_CS#0 RP15 — MEM_MB_RAS# — MEM_MB0_ODT0 RP11 — MEM_MB_ADD13

(4,6) MEM_MB_WE#
(4,6) MEM_MB_CAS#
(4,6) MEM_MB0_ODT1
(4,6) MEM_MB0_CS#1
(4,6) MEM_MB_CKE1
(4,6) MEM_MB0_CS#0
(4,6) MEM_MB_RAS#
(4,6) MEM_MB0_ODT0

47_4P2R_4

C103 C121 C66 C95 C52 C79 C76 C69 C113 C151 C153 C155 C45 C152 C127 C157
0.1U/10V/X5R_4
+1.8V_SUS

PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

+1.8V_SUS

C54 C60 C75 C61 C167 C92
0.1U/10V/X5R_4

PLACE CLOSE TO SOCKET(PER EMI/EMC)

PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

+1.8V_SUS

C143 C80 C145 C164 C55 C46
0.1U/10V/X5R_4

PLACE CLOSE TO SOCKET(PER EMI/EMC)

Close DDR2 socket

U17 *DS75U+T&R
A0 A1 A2 SDA SCL +VS O.S GND

+3.3V
C434 0.1U/10V/X5R_4
MEMHOT_SODIMM#
PDAT_SMB
PCLK_SMB
(2,6,13) PDAT_SMB
(2,6,13) PCLK_SMB
Address:92h

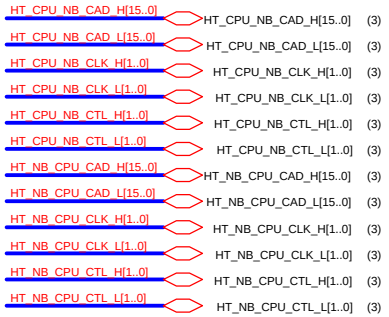
R289 *10K/F_4
R285 *10K/F_4
R286 *33_4
Q31 *2N7002E-G
Q32 *2N7002E-G
CPU_MEMHOT# (3,13)

+3.3V R292 10K/F_4 MEMHOT_SODIMM# MEMHOT_SODIMM# (6)

NB2/RD1

PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2 SODIMMS TERMINATIONS	1A
Date: Monday, August 18, 2008	Sheet 7 of 39	

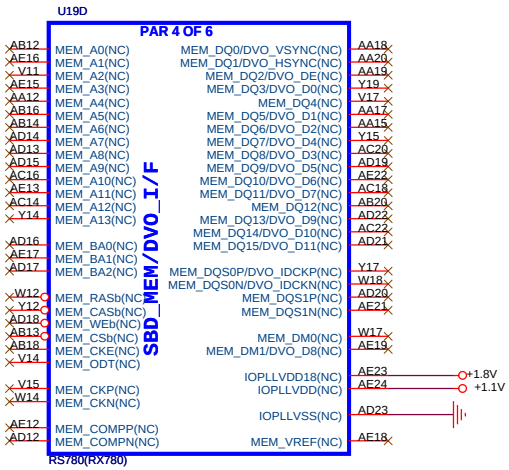


signals	RS780	RX780
HT_TXCALP	R641 300 ohm 1%	R641 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R655 300 ohm 1%	R655 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

RES CHIP 300 1/16W +-1%(0402)
P/N : CS13002FB00

This block is for UMA RS780 only , RX780 NC



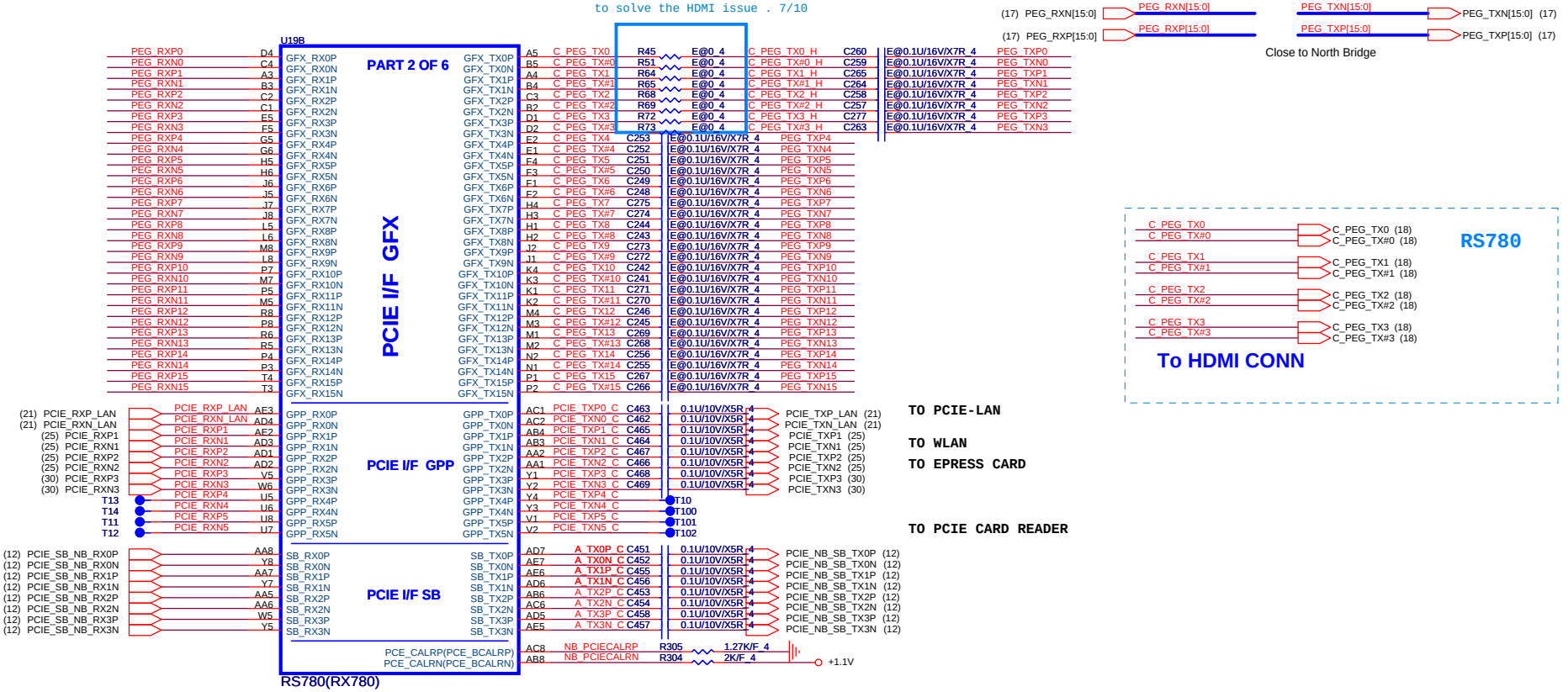
PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS780MN-HT LINK I/F 1/4	1A

NB2/RD1

Date: Monday, August 18, 2008 | Sheet 8 of 39

to solve the HDMI issue . 7/10



RX780/RS740/RS780 difference table (PCIE LINK)

	RX780/RS780
NB_PCIECALRP	1.27K (GND)
GPP4	GPP4
GPP5	GPP5

RS780 Display Port Support (muxed on GFX)

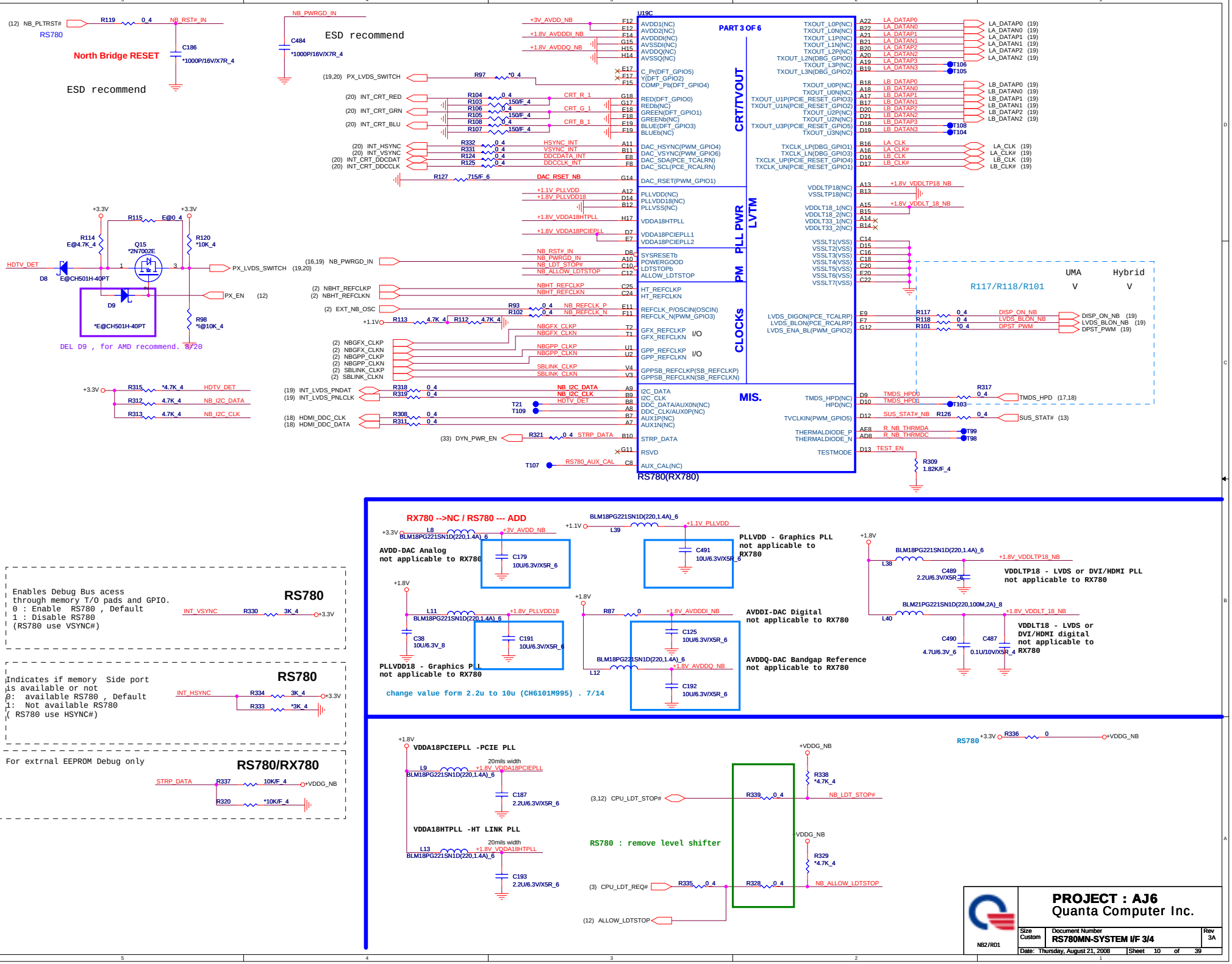
DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

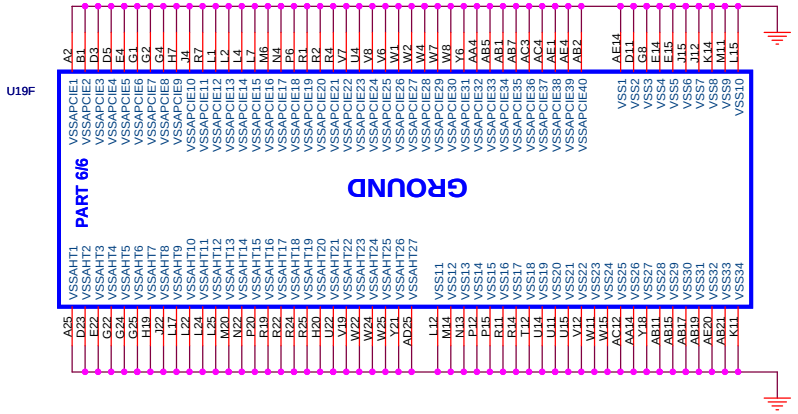
NB2/RD1

PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS780MN-PCIE I/F 2/4	3A

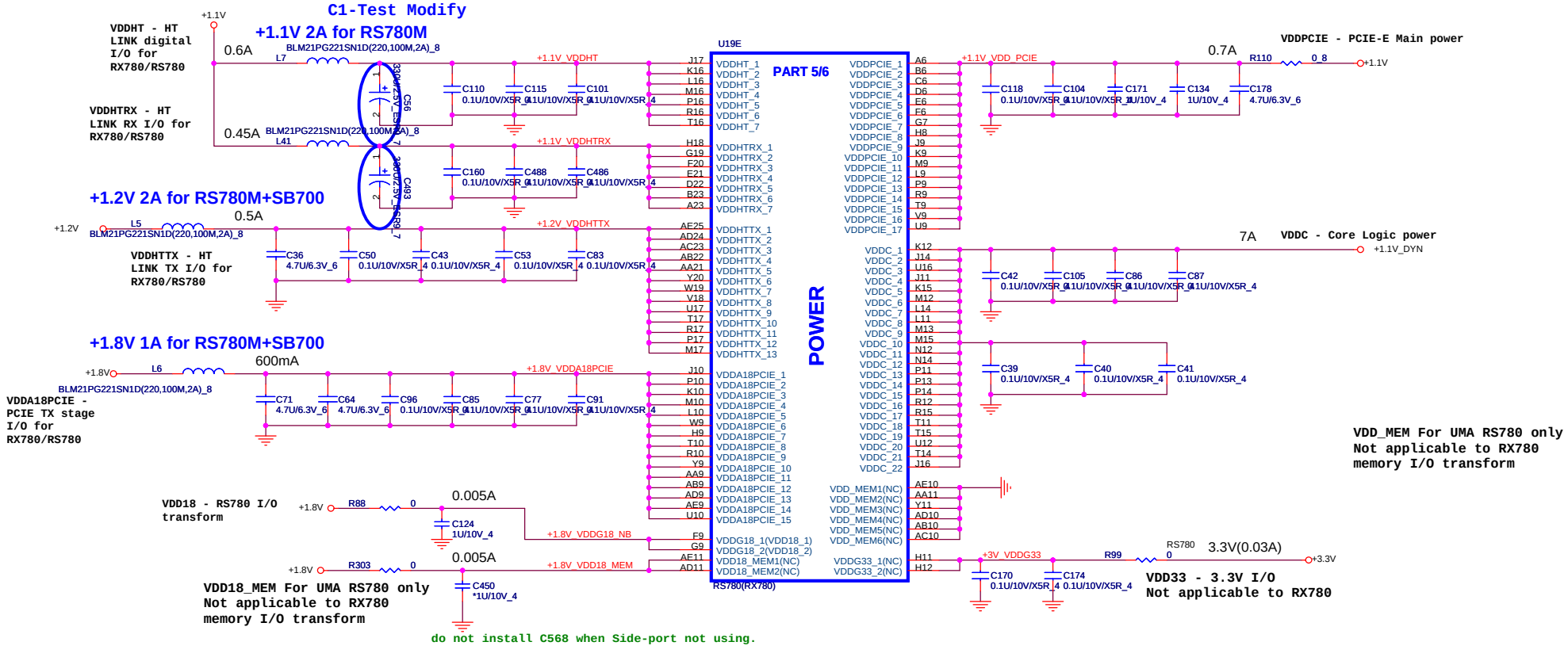
Date: Thursday, August 21, 2008 | Sheet 9 of 39


(12) NB_PLTRST#
R119 0_4 NB_RST#_IN
RS780
North Bridge RESET
C186 *1000P/16V/X7R_4
ESD recommend
NB_PWRGD_IN
C484 *1000P/16V/X7R_4
ESD recommend
U19C
PART 3 OF 6
RS780(RX780)
CRT/TVOUT
LVTM
PLL PWR
PM
CLOCKs
MIS.
(19,20) PX_LVDS_SWITCH R97 *0_4
(20) INT_CRT_RED R104 0_4 CRT_R_1
(20) INT_CRT_GRN R106 0_4 CRT_G_1
(20) INT_CRT_BLU R108 0_4 CRT_B_1
R103 150/F_4
R105 150/F_4
R107 150/F_4
(20) INT_HSYNC R332 0_4 HSYNC_INT
(20) INT_VSYNC R331 0_4 VSYNC_INT
(20) INT_CRT_DDCDAT R124 0_4 DDCDATA_INT
(20) INT_CRT_DDCCLK R125 0_4 DDCCLK_INT
R127 715/F_6 DAC_RSET_NB
+3V_AVDD_NB
+1.8V_AVDDDI_NB
+1.8V_AVDDQ_NB
+1.1V_PLLVDD
+1.8V_PLLVDD18
+1.8V_VDDA18HTPLL
+1.8V_VDDA18PCIEPLL
(16,19) NB_PWRGD_IN
NB_RST#_IN
NB_PWRGD_IN
NB_LDT_STOP#
NB_ALLOW_LDTSTOP
(2) NBHT_REFCLKP
(2) NBHT_REFCLKN
(2) EXT_NB_OSC
R93 0_4 NB_REFCLK_P
R102 0_4 NB_REFCLK_N
+1.1V R113 4.7K_4 R112 4.7K_4
(2) NBGFX_CLKP
(2) NBGFX_CLKN
(2) NBGPP_CLKP
(2) NBGPP_CLKN
(2) SBLINK_CLKP
(2) SBLINK_CLKN
(19) INT_LVDS_PNDAT
(19) INT_LVDS_PNLCLK
R318 0_4 NB_I2C_DATA
R319 0_4 NB_I2C_CLK
HDTV_DET
(18) HDMI_DDC_CLK
(18) HDMI_DDC_DATA
R308 0_4
R311 0_4
(33) DYN_PWR_EN
R321 0_4 STRP_DATA
T107 RS780_AUX_CAL
T21
T109
LA_DATAP0 (19)
LA_DATAN0 (19)
LA_DATAP1 (19)
LA_DATAN1 (19)
LA_DATAP2 (19)
LA_DATAN2 (19)
T106
T105
LB_DATAP0 (19)
LB_DATAN0 (19)
LB_DATAP1 (19)
LB_DATAN1 (19)
LB_DATAP2 (19)
LB_DATAN2 (19)
T108
T104
LA_CLK (19)
LA_CLK# (19)
LB_CLK (19)
LB_CLK# (19)
+1.8V_VDDLTP18_NB
+1.8V_VDDLT_18_NB
UMA Hybrid
R117/R118/R101 V V
R117 0_4 DISP_ON_NB
R118 0_4 LVDS_BLON_NB
R101 *0_4 DPST_PWM
DISP_ON_NB (19)
LVDS_BLON_NB (19)
DPST_PWM (19)
R317 0_4
TMDS_HPD (17,18)
T103
R126 0_4
SUS_STAT# (13)
T99
T98
R309 1.82K/F_4
+3.3V R115 E@0_4
R114 E@4.7K_4
R120 *10K_4
Q15 *2N7002E
HDTV_DET
D8 E@CH501H-40PT
PX_LVDS_SWITCH (19,20)
PX_EN (12)
D9
*E@CH501H-40PT
R98 *1@10K_4
DEL D9 , for AMD recommend. 8/20
R315 *4.7K_4
R312 4.7K_4 NB_I2C_DATA
R313 4.7K_4 NB_I2C_CLK
RX780 -->NC / RS780 --- ADD
L8 BLM18PG221SN1D(220,1.4A)_6
+3V_AVDD_NB
C179 10U/6.3V/X5R_6
AVDD-DAC Analog
not applicable to RX780
L39 BLM18PG221SN1D(220,1.4A)_6
+1.1V_PLLVDD
C491 10U/6.3V/X5R_6
PLLVDD - Graphics PLL
not applicable to
RX780
L11 BLM18PG221SN1D(220,1.4A)_6
+1.8V_PLLVDD18
C38 10U/6.3V_8
C191 10U/6.3V/X5R_6
PLLVDD18 - Graphics PLL
not applicable to RX780
R87 0
+1.8V_AVDDDI_NB
C125 10U/6.3V/X5R_6
AVDDI-DAC Digital
not applicable to RX780
L12 BLM18PG221SN1D(220,1.4A)_6
+1.8V_AVDDQ_NB
C192 10U/6.3V/X5R_6
AVDDQ-DAC Bandgap Reference
not applicable to RX780
change value form 2.2u to 10u (CH6101M995) . 7/14
L38 BLM18PG221SN1D(220,1.4A)_6
C489 2.2U/6.3V/X5R_6
VDDLTP18 - LVDS or DVI/HDMI PLL
not applicable to RX780
L40 BLM21PG221SN1D(220,100M,2A)_8
C490 4.7U/6.3V_6
C487 0.1U/10V/X5R_4
VDDLT18 - LVDS or
DVI/HDMI digital
not applicable to
RX780
Enables Debug Bus acess
through memory T/O pads and GPIO.
0 : Enable RS780 , Default
1 : Disable RS780
(RS780 use VSYNC#)
RS780
INT_VSYNC R330 3K_4 +3.3V
Indicates if memory Side port
is available or not
0: available RS780 , Default
1: Not available RS780
(RS780 use HSYNC#)
RS780
INT_HSYNC R334 3K_4 +3.3V
R333 *3K_4
For extrnal EEPROM Debug only
RS780/RX780
STRP_DATA R337 10K/F_4 +VDDG_NB
R320 *10K/F_4
VDDA18PCIEPLL -PCIE PLL
L9 BLM18PG221SN1D(220,1.4A)_6
20mils width
+1.8V_VDDA18PCIEPLL
C187 2.2U/6.3V/X5R_6
VDDA18HTPLL -HT LINK PLL
L13 BLM18PG221SN1D(220,1.4A)_6
20mils width
+1.8V_VDDA18HTPLL
C193 2.2U/6.3V/X5R_6
RS780 : remove level shifter
(3,12) CPU_LDT_STOP#
R339 0_4 NB_LDT_STOP#
R338 *4.7K_4
(3) CPU_LDT_REQ#
R335 0_4
R328 0_4 NB_ALLOW_LDTSTOP
R329 *4.7K_4
(12) ALLOW_LDTSTOP
RS780 +3.3V R336 0 +VDDG_NB
PROJECT : AJ6
Quanta Computer Inc.
Size Custom
Document Number RS780MN-SYSTEM I/F 3/4
Rev 3A
Date: Thursday, August 21, 2008
Sheet 10 of 39
NB2/RD1

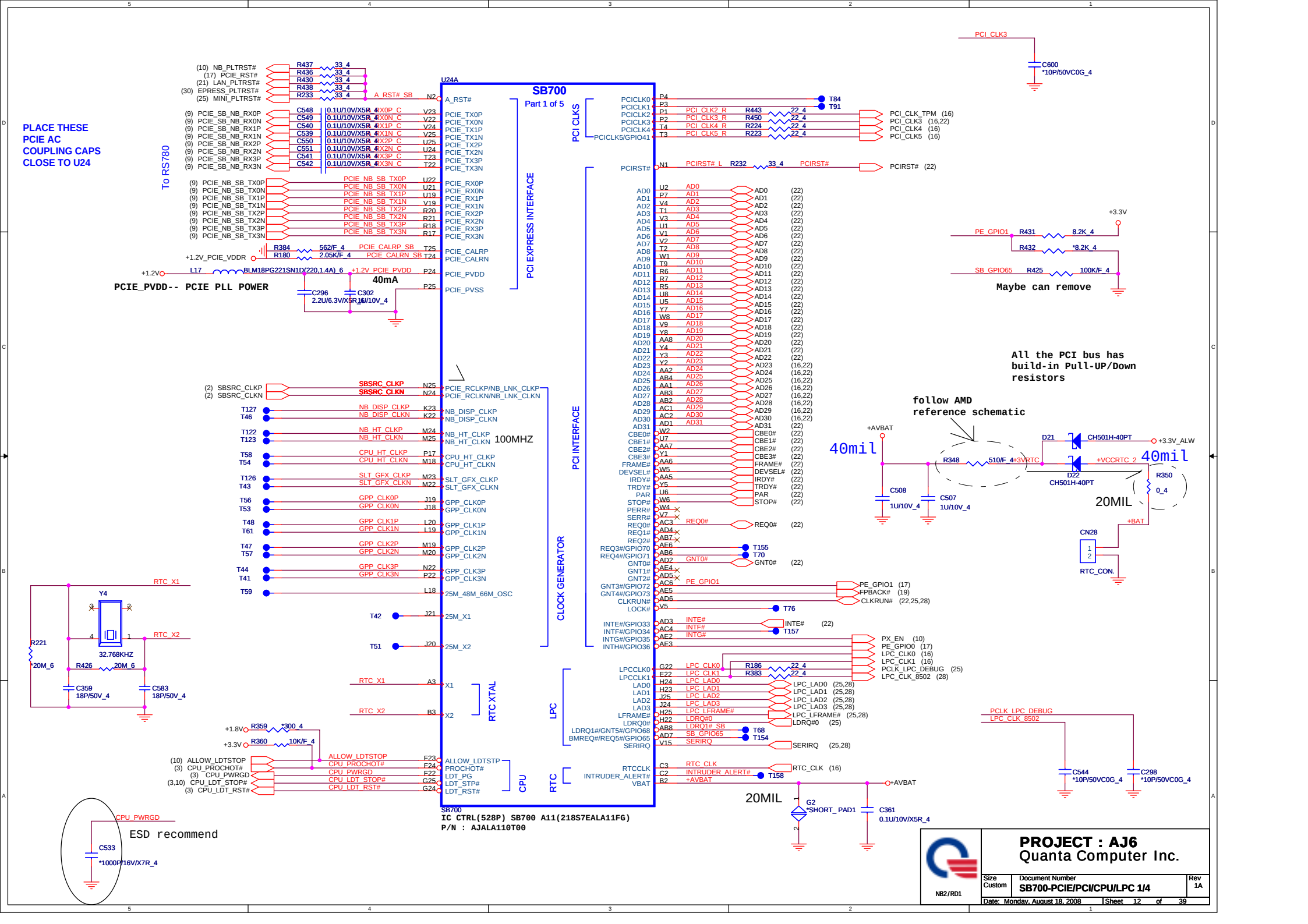


RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVDD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVDD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVDD18	NC	+1.8V	VDDLT33	NC	NC



NB2/RD1	PROJECT : AJ6 Quanta Computer Inc.	
	Size: Custom Document Number: RS780MN-POWER 4/4	Rev: 3B
	Date: Thursday, August 21, 2008	Sheet 11 of 39


PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO U24
To RS780
U24A
SB700
Part 1 of 5
SB700
IC CTRL(528P) SB700 A11(218S7EALA11FG)
P/N : AJALA110T00
PCIE_PVDD-- PCIE PLL POWER
40mA
PCI EXPRESS INTERFACE
PCI CLKS
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
100MHZ
20MIL
40mil
Maybe can remove
All the PCI bus has
build-in Pull-UP/Down
resistors
follow AMD
reference schematic
ESD recommend
32.768KHZ
PROJECT : AJ6
Quanta Computer Inc.
SB700-PCIE/PCI/CPU/LPC 1/4
NB2/RD1
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NC only ,Can't be install

+3.3V_SUS
R461 *2.2K_4 SB_TEST0
R256 *2.2K_4 SB_TEST1
R242 *2.2K_4 SB_TEST2

+3.3V_SUS
R236 *10K/F_4 SWI#

+3.3V
SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
R170 2.2K_4 PCLK_SMB
R173 2.2K_4 PDAT_SMB

Clock gen/Robson
/DDR2/DDR2
thermal/Accelerometer

+3.3V_S5
SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it
R245 2.2K_4 SB_SMBCLK1
R244 2.2K_4 SB_SMBDATA1

+3.3V_S5
SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it
R381 2.2K_4 SB_SCLK2
R380 2.2K_4 SB_SDATA2
R249 1K_4 DNBSWON#

+3.3V
R406 10K_4 GPIO10
R240 *4.7K_4 SUS_STAT#
R179 *10K_4 GPIO0
R182 *10K_4 GPIO39
R185 *10K_4 GPIO40
R167 10K_4 GPIO4
R400 10K_4 GPIO6

Not connected (internal pull-down).
remove external pull up resistor.

G3
2 1 SYS_RST#
*SHORT_ PAD1

MXM
(17) PE_RESET_MXM#

(3,7) CPU_MEMHOT#
(5) PM_THERM#
D23 CH501H-40PT
R419 *0_4
R420 *10K/F_4
+3.3V
CPU_MEMHOT# IN
SMBALERT# 1

(30) NEWCARD_DETECT
(26) USB_OC2#
(27) USB_OC1#
T169 SB_JTAG_TDO
SB_JTAG_TCK
SB_JTAG_TDI
SB_JTAG_RST#
T163

ACZ_BCLK
ACZ_SDOUT
ACZ_SDIN0_R
ACZ_SDIN1_R
ACZ_SDIN2_R
T89
ACZ_SYNC
ACZ_RST#
(16) ACZ_RST#

HD audio
interface is
3.3V voltage

ADD GPIO pin for MXM 0215
+3.3V
(17) MXM_PRESENT#
T50 MXM_RUNPWROK
R361 22K_4 HDD_AUX_RST#
T45 MXM_PWR_EN

U24D
SB700
Part 4 of 5

(22) PCI_PME#
T167
T74
(28) SUSB#
(28) SUSC#
(28) DNBSWON#
(16) SB_PWRGD_IN
(10) SUS_STAT#
R231 0_4
R234 0_4
PCI_PME#
RI#
SLP_S2
SUSB#_R
SUSC#_R
SB_PWRGD_IN
SUS_STAT#
SB_TEST2
SB_TEST1
SB_TEST0

(28) GATEA20
(28) RCIN#
(28) SCI#
(28) KBSMI#
T161
(21,25,30) PCIE_WAKE#
(28) SWI#
(3) CPU_THERMTRIP#
(16) WD_PWRGD
R235 0_4
GATEA20
RCIN#
SCI#
KBSMI#
SYS_RST#
PCIE_WAKE#
SWI#_R
CPU_THERMTRIP#
WD_PWRGD

(28) RSMRST#
R456 0_4 RSMRST#_R

GPIO10
GPIO6
GPIO4
GPIO0
GPIO39
GPIO40
(23) ACZ_SPKR
(2,6,7) PCLK_SMB
(2,6,7) PDAT_SMB
(25) SB_SMBCLK1
(25) SB_SMBDATA1
PCLK_SMB
PDAT_SMB
SB_SMBCLK1
SB_SMBDATA1
T160 PM_BATLOW#
T52 SES_INT
T79 GEVENT7#

USB OC
HD AUDIO
INTEGRATED uC
GPIO
USB 2.0
USB 1.1
USB MISC
ACPI / WAKE UP EVENTS

SB700

USB Connector EMI recommend
Min-Card
USB Connector
USB Connector
WLAN Min-Card
NEW CARD
Carama USB
BLUETOOTH
USB Connector

SB_SCLK2 (30)
SB_SDATA2 (30)
SB_GPIO16 (16)
SB_GPIO17 (16)
SPI/LPC define

CLK_48M_USB (2)
R418 *33_4
C577 *0.1U/10V_4

CN13
SB JTAG
SB_JTAG_TCK
SB_JTAG_TDO
SB_JTAG_TDI
SB_TEST1
SB_JTAG_RST#
*S/W JTAG DEBUG

To Azalia
ADD HDA for MXM 0215
ACZ_SDOUT R453 33_4 ACZ_SDOUT_AUDIO (23)
R455 E@33_4 ACZ_SDOUT_MXM (17)
ACZ_SYNC R250 33_4 ACZ_SYNC_AUDIO (23)
R238 E@33_4 ACZ_SYNC_MXM (17)
ACZ_BCLK R444 33_4 BIT_CLK_AUDIO (23)
R239 E@33_4 ACZ_BITCLK_MXM (17)
ACZ_RST# R459 33_4 ACZ_RST#_AUDIO (23)
R460 E@33_4 ACZ_RESET#_MXM (17)
ACZ_SDIN2_R R248 0_4 ACZ_SDIN2 (17)

ACZ_SDIN0_R R243 0_4 ACZ_SDIN0 (23)

To Modem Board
ACZ_SDOUT R454 33_4 ACZ_SDOUT_AUDIO_MDC (26)
C603 *10P/50VC0G_4
ACZ_SYNC R246 33_4 ACZ_SYNC_AUDIO_MDC (26)
C374 *10P/50VC0G_4
ACZ_BCLK R445 33_4 BIT_CLK_AUDIO_MDC (26)
C375 *10P/50VC0G_4
ACZ_RST# R463 33_4 ACZ_RST#_AUDIO_MDC (26)
ACZ_SDIN1_R R410 33_4 ACZ_SDIN1 (26)

NB2/RD1

PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
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Date: Monday, August 18, 2008 Sheet 13 of 39

SATA PORT 0,1,2,3 can support AHCI mode

SATA1

PLACE SATA AC COUPLING CAPS CLOSE TO SB700

(24) SATA_TXP0 — C581 0.01U/16V_4 — SATA_TXP0_C — AD9 SATA_TX0P
(24) SATA_TXN0 — C578 0.01U/16V_4 — SATA_TXN0_C — AE9 SATA_TX0N
(24) SATA_RXN0 — AB10 SATA_RX0N
(24) SATA_RXP0 — AC10 SATA_RX0P

T148 — SATA_TXP1_C — AE10 SATA_TX1P
T147 — SATA_TXN1_C — AD10 SATA_TX1N

T144 — SATA_RXN1_C — AD11 SATA_RX1N
T146 — SATA_RXP1_C — AE11 SATA_RX1P

AB12 SATA_TX2P
AC12 SATA_TX2N

AE12 SATA_RX2N
AD12 SATA_RX2P

AD13 SATA_TX3P
AE13 SATA_TX3N

AB14 SATA_RX3N
AC14 SATA_RX3P

SATA PORT 4,5 are only support IDE mode

SATA ODD

(24) SATA_TXP4 — C575 0.01U/16V_4 — SATA_TXP4_C — AE14 SATA_TX4P
(24) SATA_TXN4 — C574 0.01U/16V_4 — SATA_TXN4_C — AD14 SATA_TX4N
(24) SATA_RXN4 — AD15 SATA_RX4N
(24) SATA_RXP4 — AE15 SATA_RX4P

T139 — SATA_TXP5_C — AB16 SATA_TX5P
T143 — SATA_TXN5_C — AC16 SATA_TX5N

T140 — SATA_RXN5_C — AE16 SATA_RX5N
T141 — SATA_RXP5_C — AD16 SATA_RX5P

R201 1K/F_4 — SATA_RBIAS_PN — V12 SATA_CAL

SATA_X1 — Y12 SATA_X1
SATA_X2 — AA12 SATA_X2

SB_SATA_LED# — W11 SATA_ACT#/GPIO67

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB700

NOTE:
R201 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

PLVDD_SATA-- SATA PLL POWER

+3.3V — R163 10K/F_4 — +1.2V_PLLVDD_SATA — AA11 PLLVDD_SATA
+3V_XTLVDD_SATA — W12 XTLVDD_SATA

XTLVDD_SATA-- SATA crystal power

C338 33P/50V/NPO_4 — SATA_X1
Y3 25MHZ
R198 10M_6
C327 33P/50V/NPO_4 — SATA_X2

U24B

SB700
Part 2 of 5

SERIAL ATA

ATA 66/100/133

IDE_IORDY AA24 T114
IDE_IRQ AA25 T115
IDE_A0 Y22 T40
IDE_A1 AB23 T120
IDE_A2 Y23 T119
IDE_DACK# AB24 T118
IDE_DRQ AD25 T117
IDE_IOR# AC25 T125
IDE_IOW# AC24 T116
IDE_CS1# Y25 T124
IDE_CS3# Y24 T121

IDE_D0/GPIO15 AD24 R388 0_4 WLAN_RF_OFF# — WLAN_RF_OFF# (25,29)
IDE_D1/GPIO16 AD23 T129
IDE_D2/GPIO17 AE22 T131
IDE_D3/GPIO18 AC22 T130
IDE_D4/GPIO19 AD21 T132
IDE_D5/GPIO20 AE20 T135
IDE_D6/GPIO21 AB20 T133
IDE_D7/GPIO22 AD19 T138
IDE_D8/GPIO23 AE19 T137
IDE_D9/GPIO24 AC20 T134
IDE_D10/GPIO25 AD20 T136
IDE_D11/GPIO26 AE21 BOARD_ID0
IDE_D12/GPIO27 AB22 BOARD_ID1
IDE_D13/GPIO28 AD22 BOARD_ID2
IDE_D14/GPIO29 AE23 BOARD_ID3
IDE_D15/GPIO30 AC23 BOARD_ID4

IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

SPI ROM

SPI_DI/GPIO12 G6 T73
SPI_DO/GPIO11 D2 T164
SPI_CLK/GPIO47 D1 T165
SPI_HOLD#/GPIO31 F4 T83
SPI_CS#/GPIO32 F3 T85

LAN_RST#/GPIO13 U15
ROM_RST#/GPIO14 J1 ROM_RST# T159
R193 0_4 — BT_ON# (26,29)

FANOUT0/GPIO3 M8 SB_FANOUT0 T72
FANOUT1/GPIO48 M5 SB_FANOUT1 T75
FANOUT2/GPIO49 M7

FANIN0/GPIO50 P5 SB_FANTACH0 T87
FANIN1/GPIO51 P8 SB_FANTACH1 T77
FANIN2/GPIO52 R8 PORT_80_PWR_DWN T69

HW MONITOR

TEMP_COMM C6 TEMP_COMM
TEMPIN0/GPIO61 B6 TEMPIN0 T150
TEMPIN1/GPIO62 A6 TEMPIN1 T149
TEMPIN2/GPIO63 A5 MB_THRMDA_SB T153
TEMPIN3/TALERT#/GPIO64 B5 T151

VIN0/GPIO53 A4
VIN1/GPIO54 B4
VIN2/GPIO55 C4
VIN3/GPIO56 D4
VIN4/GPIO57 D5
VIN5/GPIO58 D6
VIN6/GPIO59 A7
VIN7/GPIO60 B7

SATA PWR

AVDD F6 — 5mA — +3V_VDD_HWM — L24 0 — +3.3V
AVSS G7 — C358 *0.1U/10V_4 — C356 *2.2U/6.3V_6

AVDD--H/W monitor Analog power

SB700

+3.3V — C280 0.1U/10V/X5R_4
(29) SATA_LED# — U12 TC7SH08FU — SB_SATA_LED#

+1.2V — (1.2V @ 60mA) — L23 BLM18PG221SN1D(220,1.4A)_6 — +1.2V_PLLVDD_SATA — 77mA
C346 1U/10V_4
C345 0.1U/10V/X5R_4

+3.3V — (3.3V @ 1.2mA) — L25 BLM18PG221SN1D(220,1.4A)_6 — +3V_XTLVDD_SATA — 1mA
C357 1U/10V_4
Place near ball

+3.3V — R392 E@10K/F_4 — BOARD_ID0 — R391 *I@10K/F_4
R184 *10K/F_4 — BOARD_ID1 — R183 10K/F_4
R372 *10K/F_4 — BOARD_ID2 — R387 10K/F_4
R371 *10K/F_4 — BOARD_ID3 — R386 10K/F_4
R368 10K/F_4 — BOARD_ID4 — R370 *10K/F_4

Modify 5/7/2008

	UMA	MXM
ID0	0	1
ID1	0	0
ID2	0	0
ID3	0	0
ID4	1	1

change the board ID. 7/10

NB2/RD1

PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB700-ACPI/GPIO/USB 2/4	3A

Date: Thursday, August 21, 2008 | Sheet 14 of 39

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

For SB700 issue(6/22)
A1-1 chip bug
use A1-2 chip can remove

POWER

VDDQ--3.3V I/O power

0.8A

1.8V : FLASH MEMORY MODE(DEFAULT)
3.3V: IDE MODE

VDD-- S/B CORE power

604mA

CKVDD_1.2V-- Internal clock Generator I/O power

286mA

VDD33_18--3.3V IDE I/O power
1.8V flash memory I/O power

0.45A

PCIE_VDDR--PCIE I/O power

844mA

AVDD_SATA--SATA phy power

0.2A

AVDDTX--USB Phy Analog I/O power

0.2A

For support USB wakeup-->3V_S5

S5_3.3--3.3v standby power

0.01A

S5_1.2V--1.2V standby power

0.22A

0.2A

V5_VREF--PCI 5V TOLERANCE

4mA
7mA
44mA
16mA

USB_PHY_1.2V--USB Phy digital power

AVDDC--USB Analog PLL power

AVDDCK_1.2--USB Phy digital power

AVDDCK_3.3--Analog system PLL power

SB700
Part 3 of 5

SB700
Part 5 of 5

GROUND

Project	PROJECT : AJ6 Quanta Computer Inc.
Size	Custom
Document Number	SB700-PWR/DECOUPLING 4/4
Rev	2A
Date	Monday, August 18, 2008
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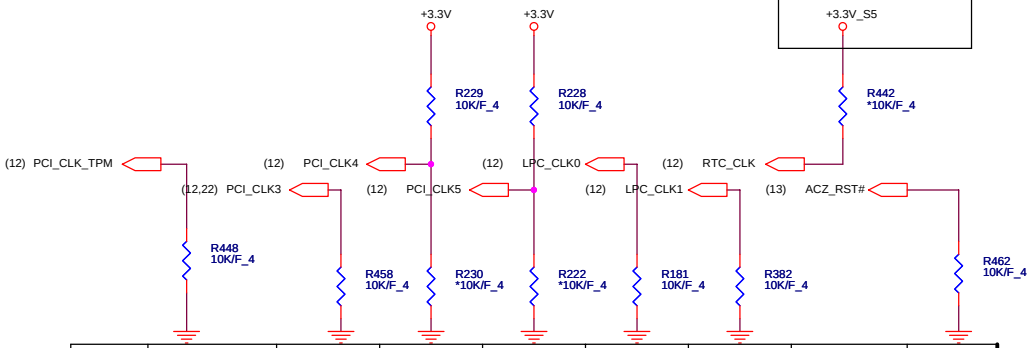
	NB2/RD1

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

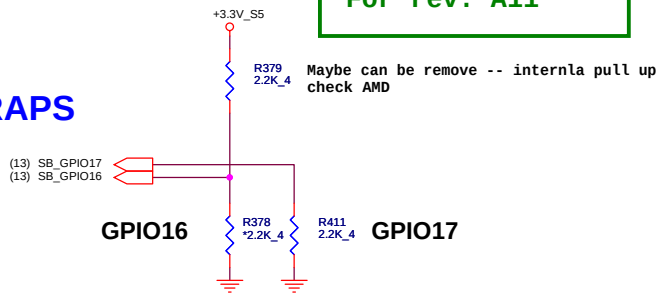
It must ready refore RSMRST#

REQUIRED STRAPS



	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT

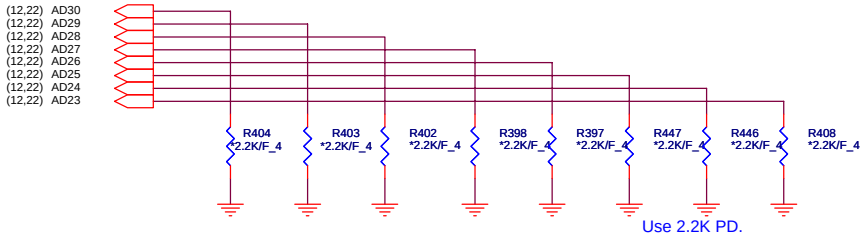
For rev. A11



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

DEBUG STRAPS

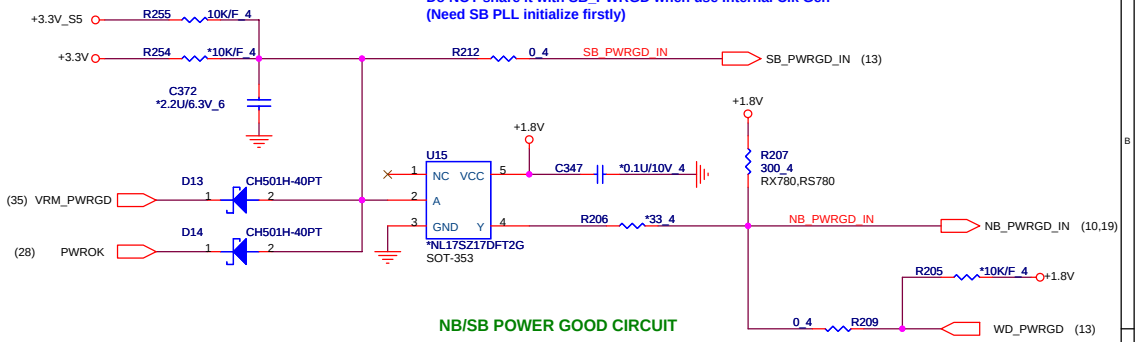
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



Use 2.2K PD.

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)



NB/SB POWER GOOD CIRCUIT

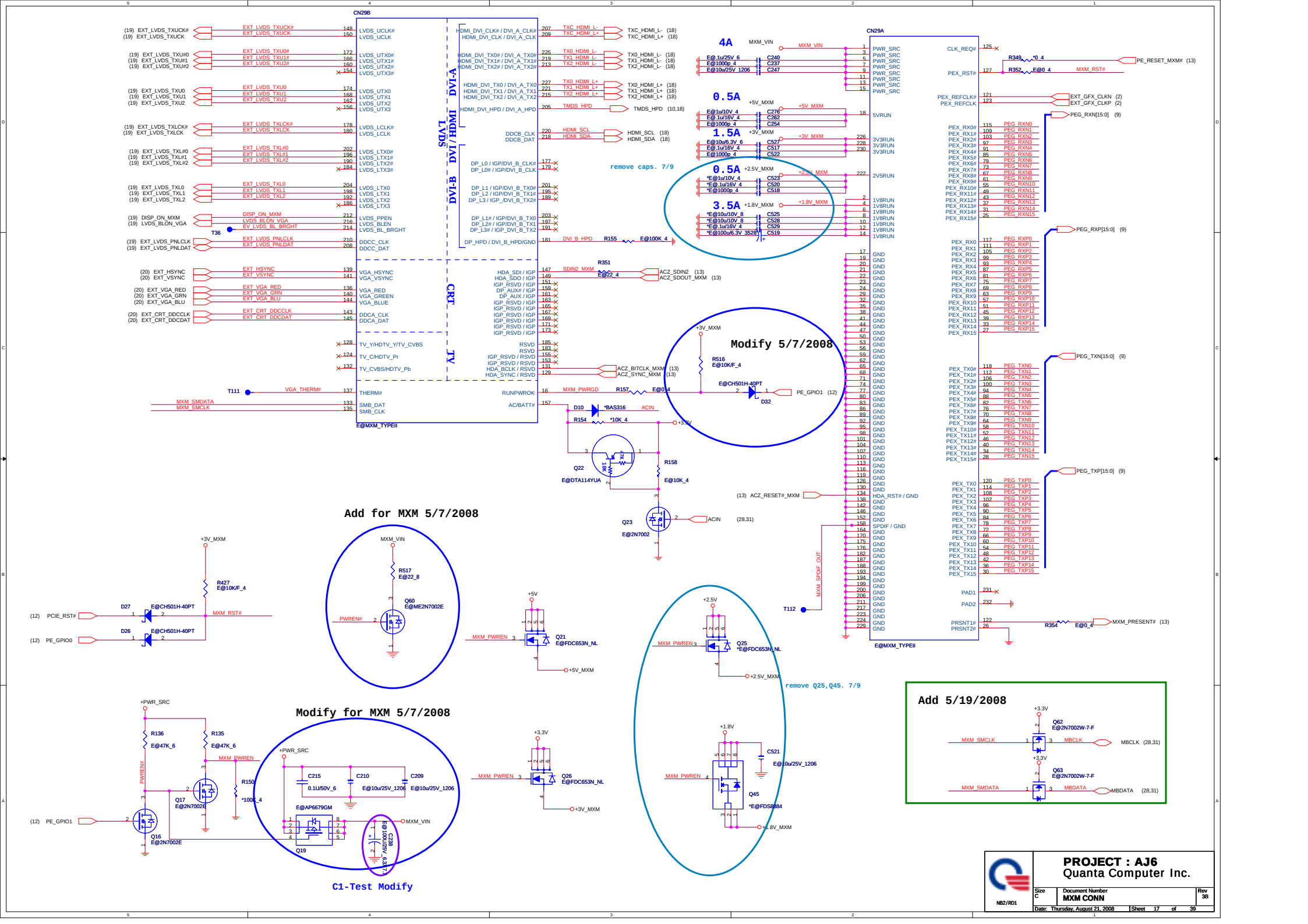
AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

NB2/RD1

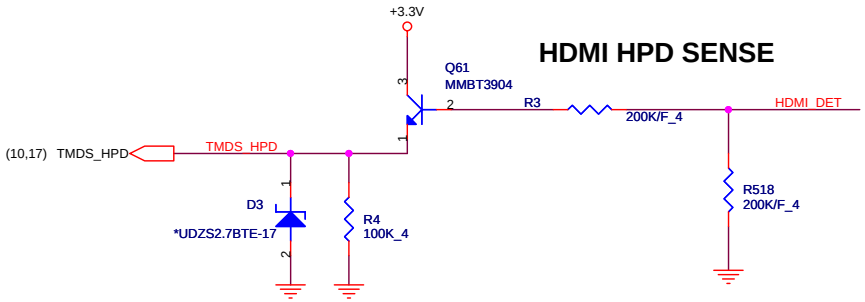
PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB700-STRAPS	1A

Date: Monday, August 18, 2008 Sheet 16 of 39

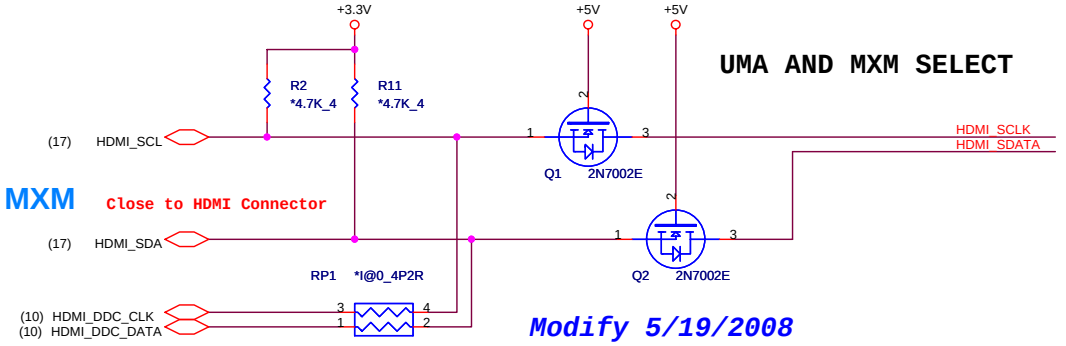

CN29B
CN29A
LVDS
DVI-A
DVI / HDMI
DVI-B
CRT
TV
E@MXM_TYPEII
remove caps. 7/9
Modify 5/7/2008
Add for MXM 5/7/2008
Modify for MXM 5/7/2008
remove Q25,Q45. 7/9
Add 5/19/2008
C1-Test Modify
PROJECT : AJ6
Quanta Computer Inc.
MXM CONN
NB2/RD1
Thursday, August 21, 2008

HDMI HPD SENSE



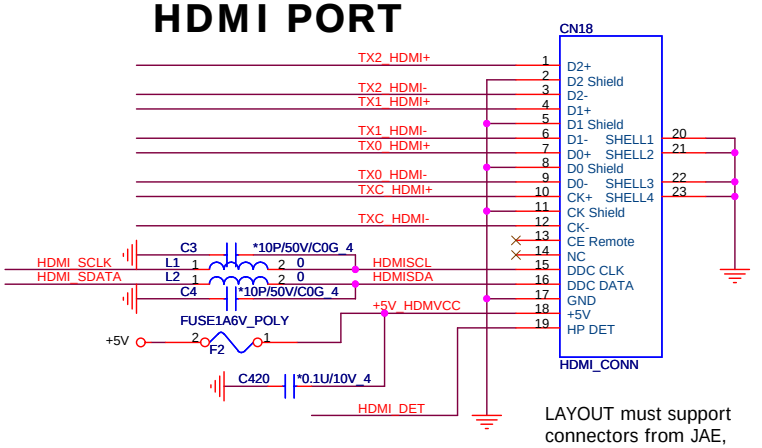
Modify 5/19/2008

UMA AND MXM SELECT



Modify 5/19/2008

HDMI PORT



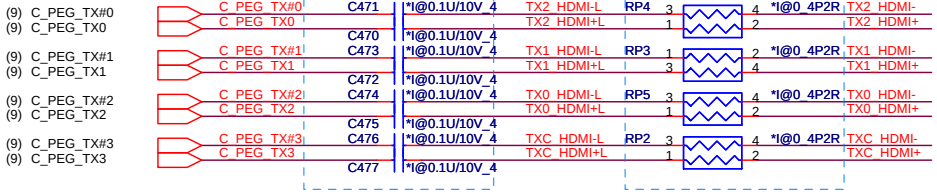
LAYOUT must support connectors from JAE, Molex, and Acon

Modify 5/26/2008

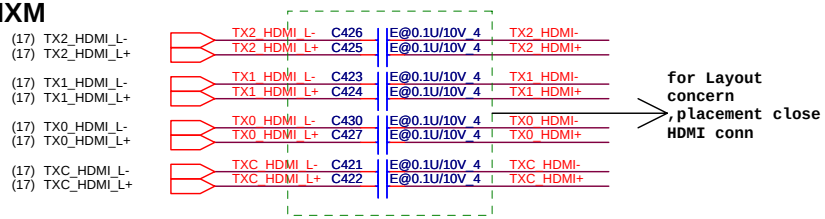
From RS780M

for Layout concern ,placement close north bridge

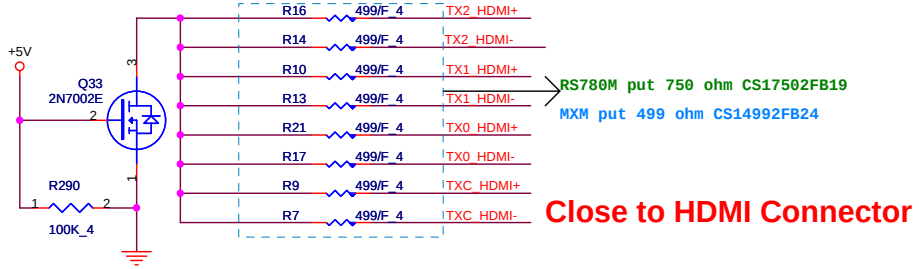
for Layout concern ,placement close HDMI conn



MXM



for Layout concern ,placement close HDMI conn

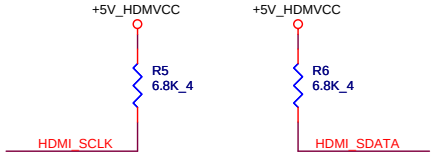


RS780M put 750 ohm CS17502FB19

MXM put 499 ohm CS14992FB24

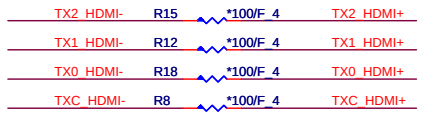
Close to HDMI Connector

Modify 5/19/2008



Close to HDMI Connector

DDC4 is 5V tolerance , the MOSFET level shifter no need

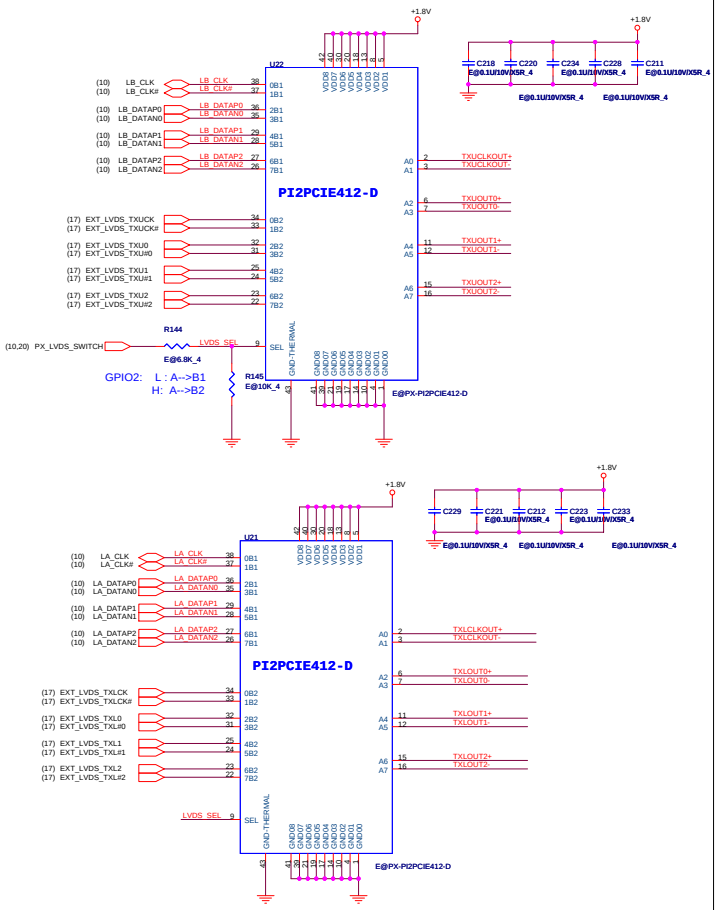


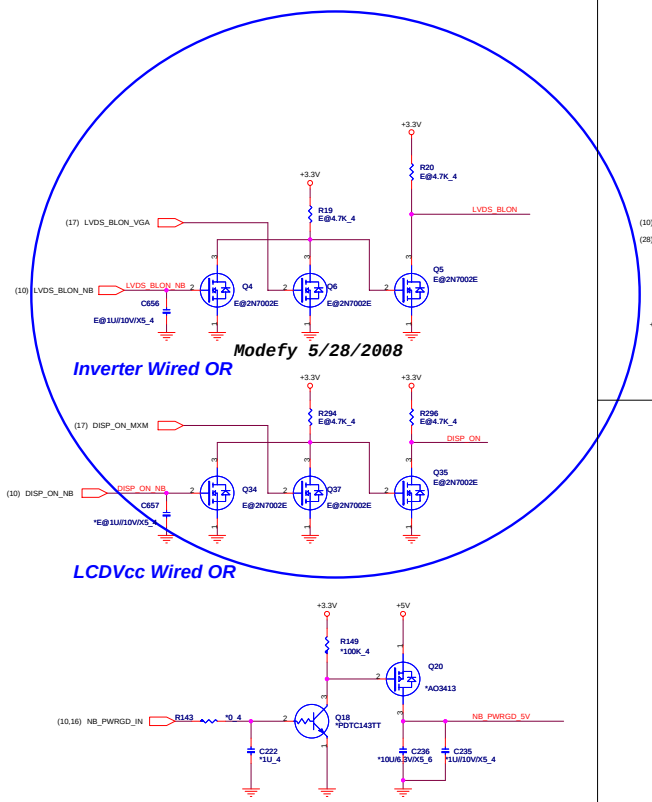
RS780: Pulled up to +5.0 V on the Northbridge side with a 4.7k 5% resistor

NB2/RD1

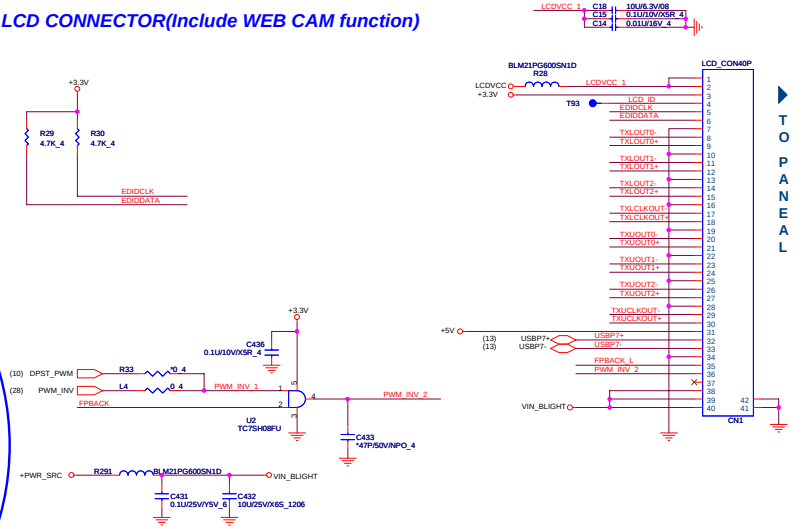
PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
B	HDMI CONN	2A
Date: Monday, August 18, 2008	Sheet 18 of 39	

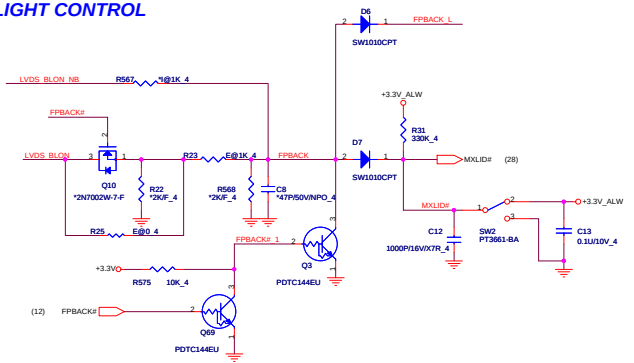




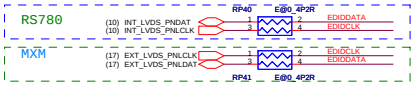
LCD CONNECTOR(Include WEB CAM function)



BACKLIGHT CONTROL

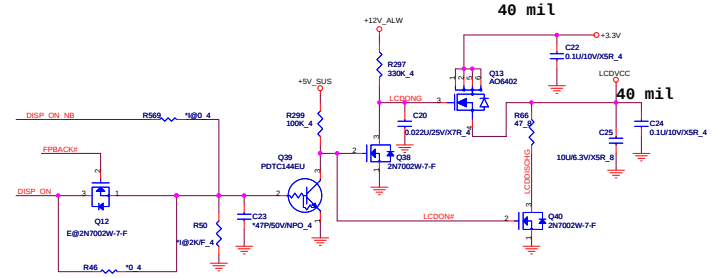


Close to NB & VGA between



Close to NB & VGA between

PANEL VCC CONTROL

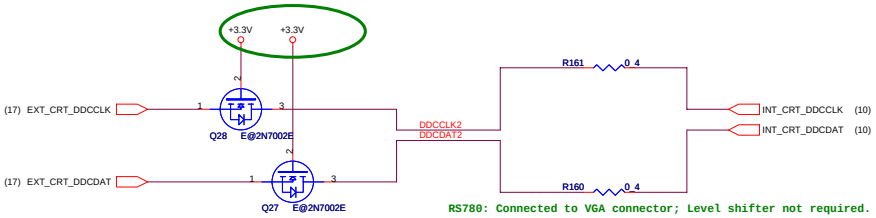


PROJECT : AJ6
Quanta Computer Inc.

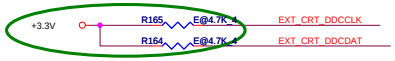
Size	Document Number	Rev
Custom	LCD CONN & MUX	3A
Date: Thursday, August 21, 2008	Sheet 19 of 39	

NB2/RD1

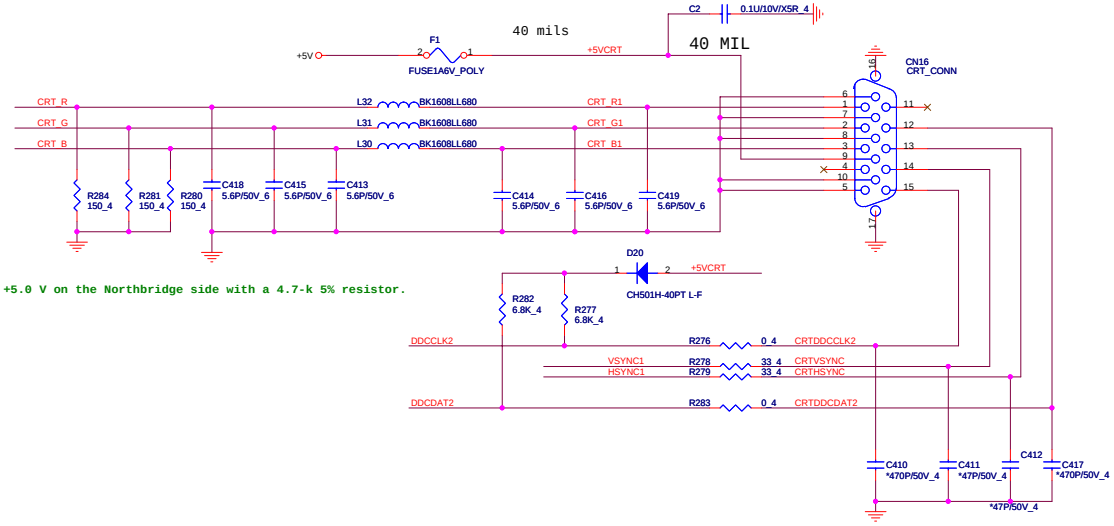
CRT PORT



RS780: Connected to VGA connector; Level shifter not required.

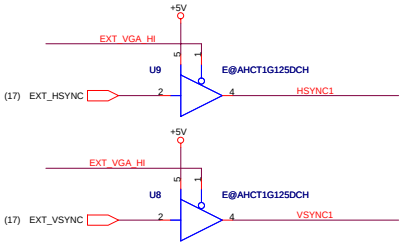


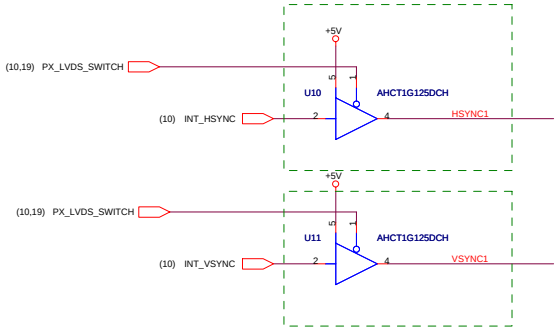
	RS780	Hybrid
Q28,Q27	X	V
R165,R164	X	V

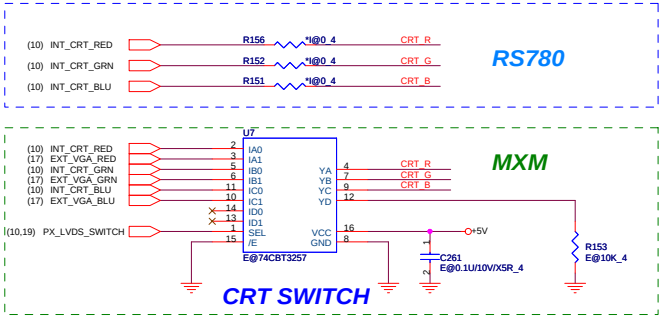


RS780: Pulled up to +5.0 V on the Northbridge side with a 4.7-k 5% resistor.

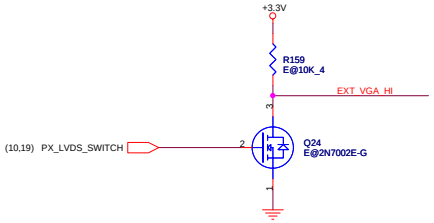
U9/U8 FOR RS780 ONLY
U8/U9/U10/U11 FOR RS780+MXM HYBRID

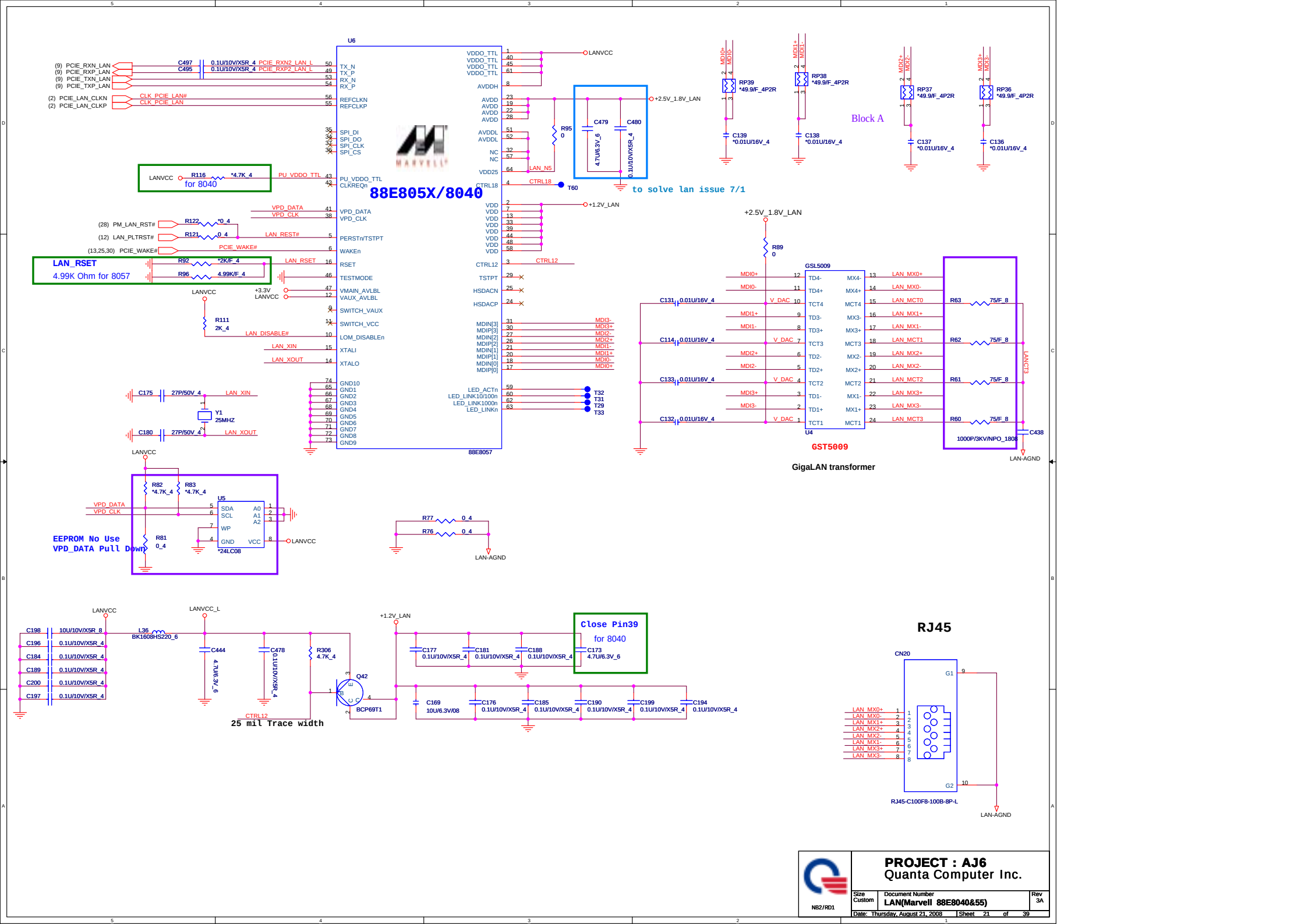


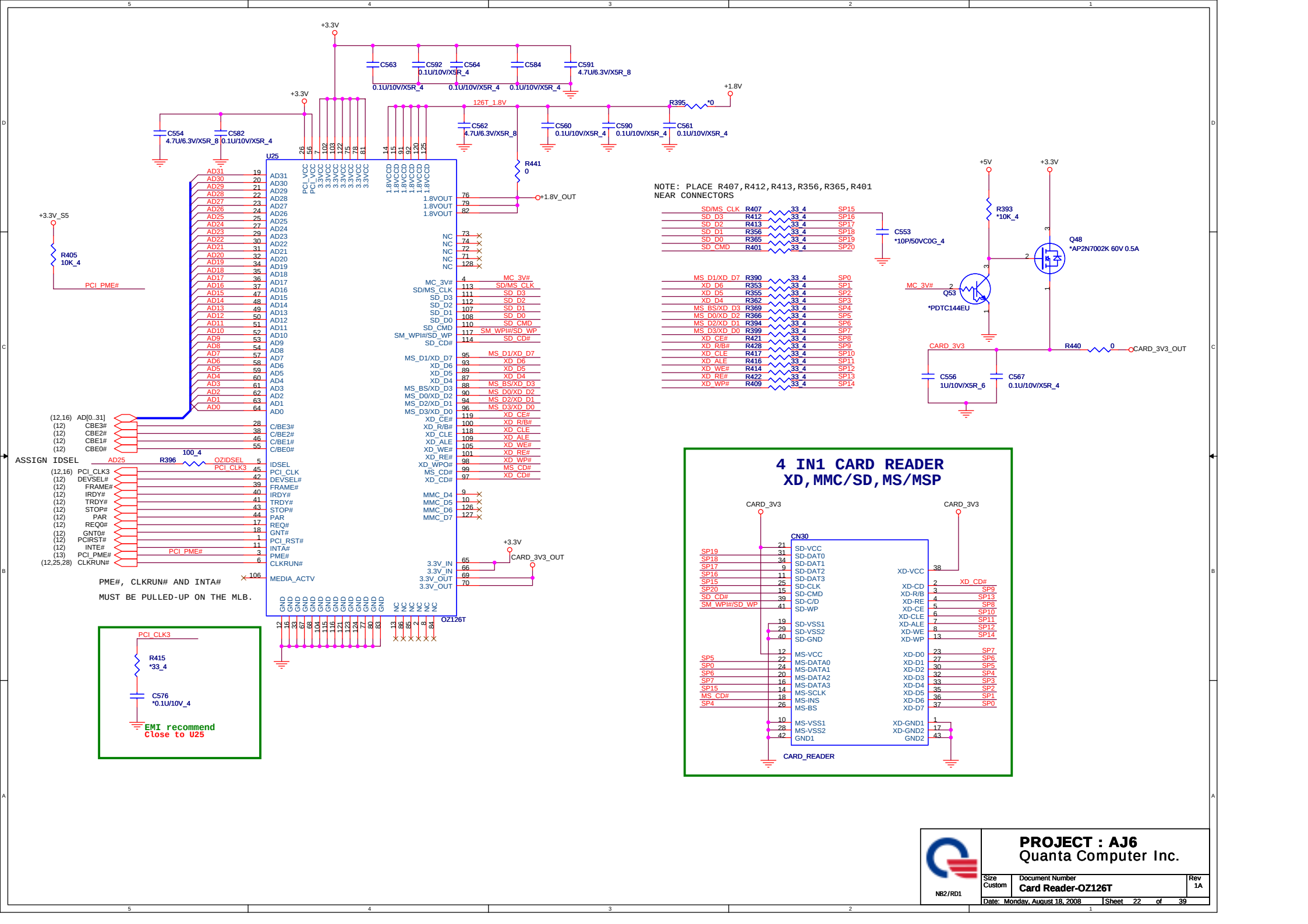




inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

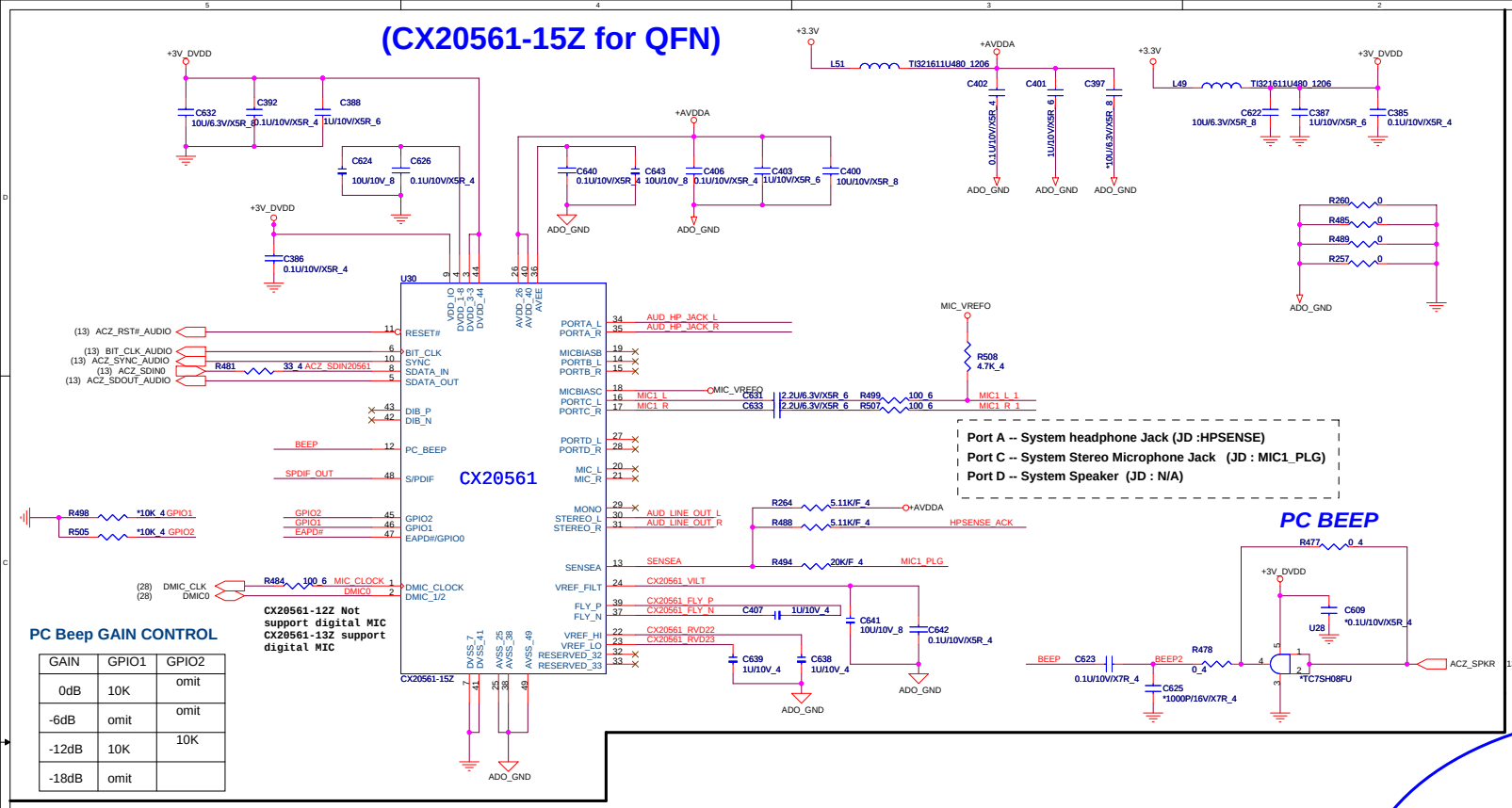



U6
88E805X/8040
88E8057
LANVCC
+2.5V_1.8V_LAN
+1.2V_LAN
+3.3V
LANVCC
(9) PCIE_RXN_LAN
(9) PCIE_RXP_LAN
(9) PCIE_TXN_LAN
(9) PCIE_TXP_LAN
(2) PCIE_LAN_CLKN
(2) PCIE_LAN_CLKP
C497 0.1U/10V/X5R_4 PCIE_RXN2_LAN_L
C495 0.1U/10V/X5R_4 PCIE_RXP2_LAN_L
CLK_PCIE_LAN#
CLK_PCIE_LAN
TX_N
TX_P
RX_N
RX_P
REFCLKN
REFCLKP
SPI_DI
SPI_DO
SPI_CLK
SPI_CS
R116 *4.7K_4 PU_VDDO_TTL
for 8040
PU_VDDO_TTL
CLKREQn
VPD_DATA
VPD_CLK
(28) PM_LAN_RST#
R122 *0_4
(12) LAN_PLTRST#
R121 0_4 LAN_REST#
(13,25,30) PCIE_WAKE#
PCIE_WAKE#
PERSTn/TSTPT
WAKEn
LAN_RSET
4.99K Ohm for 8057
R92 *2K/F_4
R96 4.99K/F_4
RSET
TESTMODE
VMAIN_AVLBL
VAUX_AVLBL
SWITCH_VAUX
SWITCH_VCC
R111 2K_4
LAN_DISABLE#
LOM_DISABLEn
LAN_XIN
LAN_XOUT
XTALI
XTALO
C175 27P/50V_4 LAN_XIN
Y1 25MHZ
C180 27P/50V_4 LAN_XOUT
GND10
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
VDDO_TTL
AVDDH
AVDD
AVDDL
NC
VDD25
CTRL18
VDD
CTRL12
TSTPT
HSDACN
HSDACP
MDIN[3]
MDIP[3]
MDIN[2]
MDIP[2]
MDIN[1]
MDIP[1]
MDIN[0]
MDIP[0]
LED_ACTn
LED_LINK10/100n
LED_LINK1000n
LED_LINKn
T32
T31
T29
T33
R95 0
C479 4.7U/6.3V_6
C480 0.1U/10V/X5R_4
LAN_N5
CTRL18
T60
to solve lan issue 7/1
RP39 *49.9/F_4P2R
RP38 *49.9/F_4P2R
RP37 *49.9/F_4P2R
RP36 *49.9/F_4P2R
C139 *0.01U/16V_4
C138 *0.01U/16V_4
C137 *0.01U/16V_4
C136 *0.01U/16V_4
Block A
R89 0
GSL5009
U4
GST5009
V_DAC
TD4- TD4+ TCT4 TD3- TD3+ TCT3 TD2- TD2+ TCT2 TD1- TD1+ TCT1
MX4- MX4+ MCT4 MX3- MX3+ MCT3 MX2- MX2+ MCT2 MX1- MX1+ MCT1
LAN_MX0+ LAN_MX0- LAN_MCT0 LAN_MX1+ LAN_MX1- LAN_MCT1 LAN_MX2+ LAN_MX2- LAN_MCT2 LAN_MX3+ LAN_MX3- LAN_MCT3
C131 0.01U/16V_4
C114 0.01U/16V_4
C133 0.01U/16V_4
C132 0.01U/16V_4
R63 75/F_8
R62 75/F_8
R61 75/F_8
R60 75/F_8
1000P/3KV/NPO_1808
C438
LANCT3
LAN-AGND
GigaLAN transformer
R82 *4.7K_4
R83 *4.7K_4
U5
SDA SCL WP GND VCC A0 A1 A2
*24LC08
R81 0_4
EEPROM No Use
VPD_DATA Pull Down
R77 0_4
R76 0_4
LAN-AGND
C198 10U/10V/X5R_8
C196 0.1U/10V/X5R_4
C184 0.1U/10V/X5R_4
C189 0.1U/10V/X5R_4
C200 0.1U/10V/X5R_4
C197 0.1U/10V/X5R_4
L36 BK1608HS220_6
LANVCC_L
C444 4.7U/6.3V_6
C478 0.1U/10V/X5R_4
R306 4.7K_4
CTRL12
25 mil Trace width
Q42 BCP69T1
C177 0.1U/10V/X5R_4
C181 0.1U/10V/X5R_4
C188 0.1U/10V/X5R_4
C173 4.7U/6.3V_6
Close Pin39
for 8040
C169 10U/6.3V/08
C176 0.1U/10V/X5R_4
C185 0.1U/10V/X5R_4
C190 0.1U/10V/X5R_4
C199 0.1U/10V/X5R_4
C194 0.1U/10V/X5R_4
RJ45
CN20
LAN_MX0+ LAN_MX0- LAN_MX1+ LAN_MX2+ LAN_MX2- LAN_MX1- LAN_MX3+ LAN_MX3-
G1 G2
RJ45-C100F8-100B-8P-L
LAN-AGND
PROJECT : AJ6
Quanta Computer Inc.
NB2/RD1
Size Custom
Document Number
LAN(Marvell 88E8040&55)
Rev 3A
Date: Thursday, August 21, 2008
Sheet 21 of 39



NB2/RD1	PROJECT : AJ6 Quanta Computer Inc.		
	Size: Custom	Document Number: Card Reader-OZ126T	Rev: 1A
	Date: Monday, August 18, 2008	Sheet 22 of 39	

(CX20561-15Z for QFN)



CX20561-12Z Not support digital MIC
CX20561-13Z support digital MIC

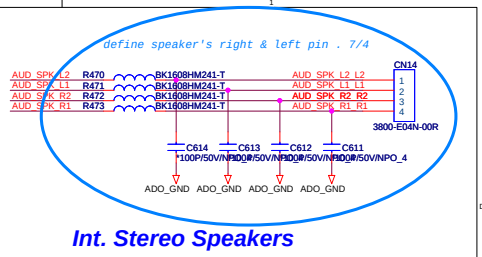
PC Beep GAIN CONTROL

GAIN	GPIO1	GPIO2
0dB	10K	omit
-6dB	omit	omit
-12dB	10K	10K
-18dB	omit	

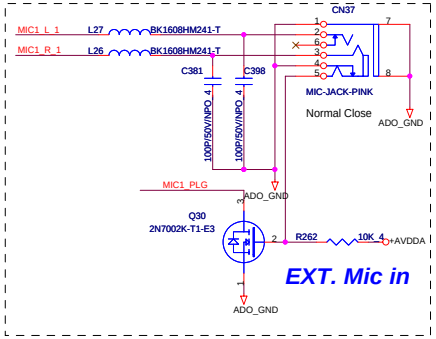
Port A -- System headphone Jack (JD :HPSENSE)
Port C -- System Stereo Microphone Jack (JD : MIC1_PLG)
Port D -- System Speaker (JD : N/A)

PC BEEP

Int. Stereo Speakers

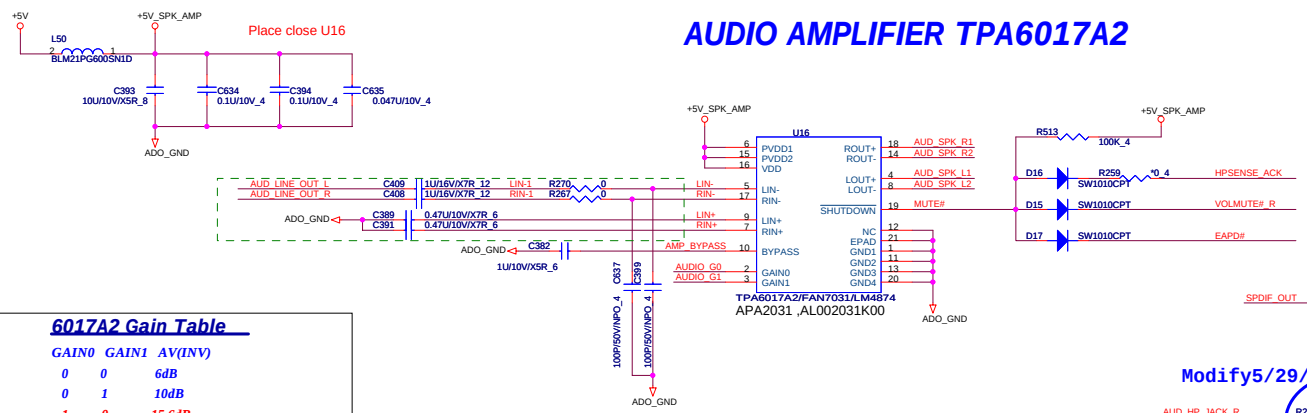


EXT. Mic in



Headphone out + Spdif Out (normal open)

AUDIO AMPLIFIER TPA6017A2

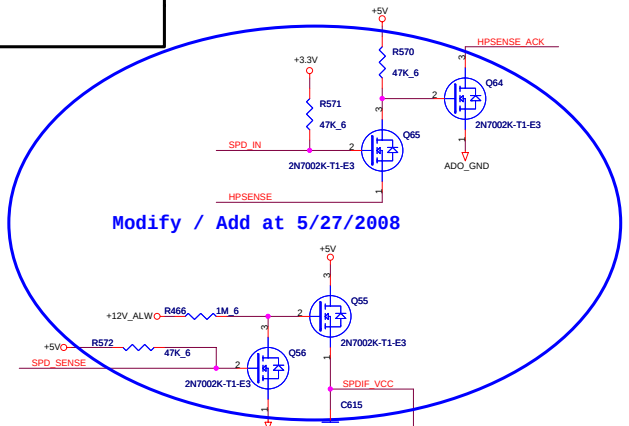


6017A2 Gain Table

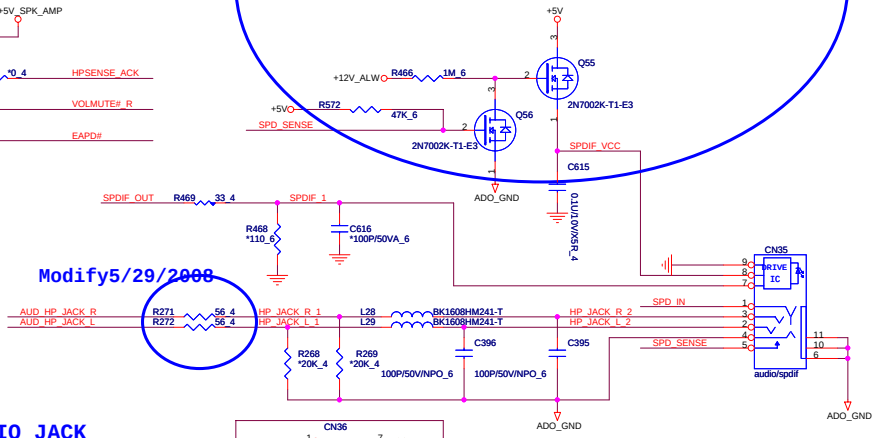
GAIN0	GAIN1	AV(INV)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

change Gain from 15.6 to 10 db. 7/8

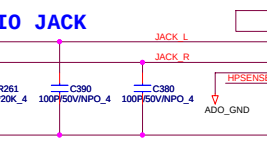
Modify / Add at 5/27/2008



Modify5/29/2008



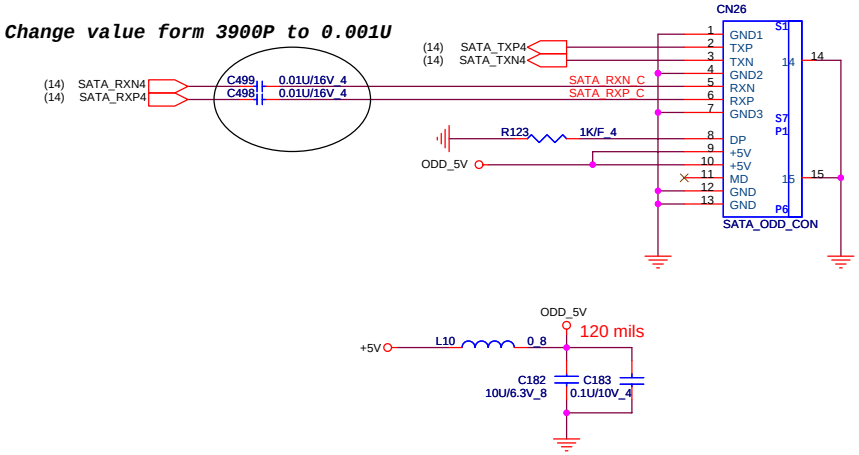
Modify5/29/2008



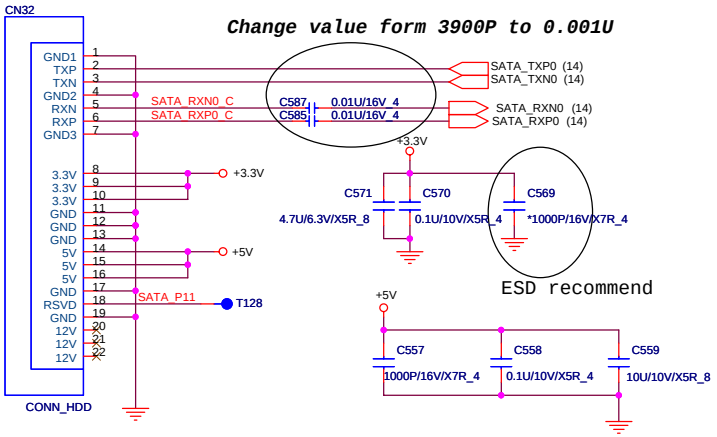
AUDIO JACK

SATA CD-ROM

NEW PART check Pin define

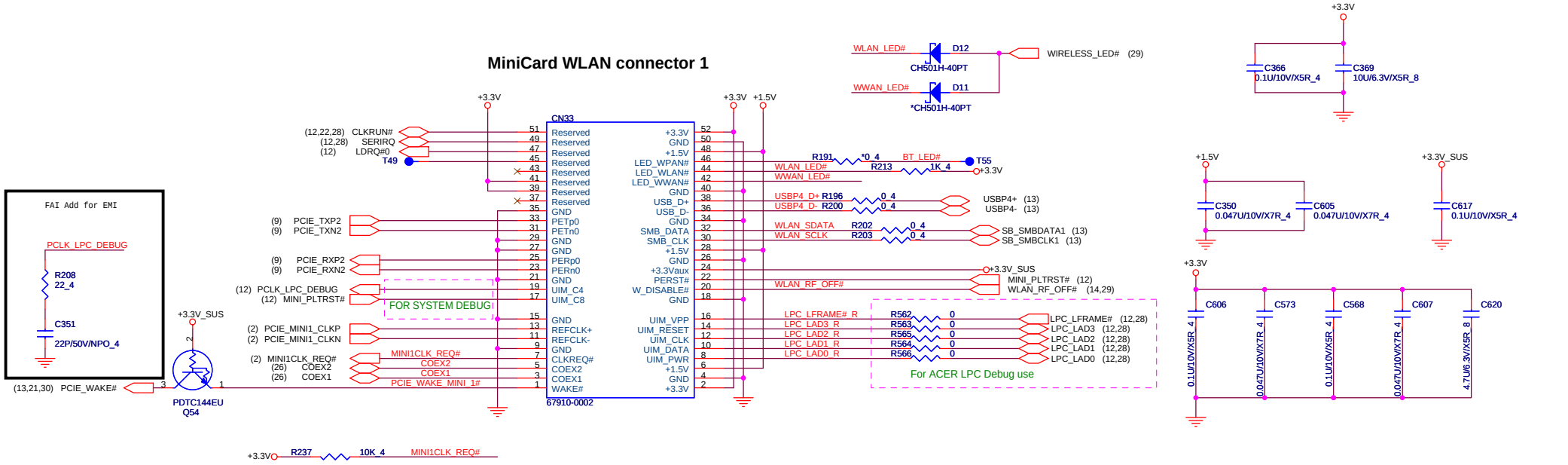


SATA CONNECTOR

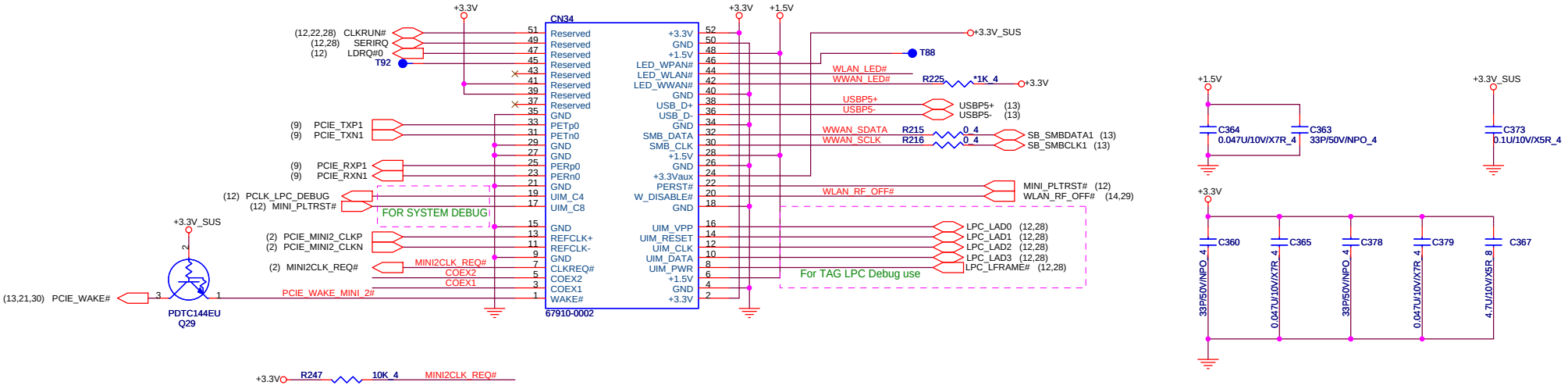


NB2/RD1	**PROJECT : AJ6** Quanta Computer Inc.	
Size: Custom	Document Number: **SATA HDD ODD**	Rev: 3A
Date: Monday, August 18, 2008	Sheet 24 of 39	

MiniCard WLAN connector 1

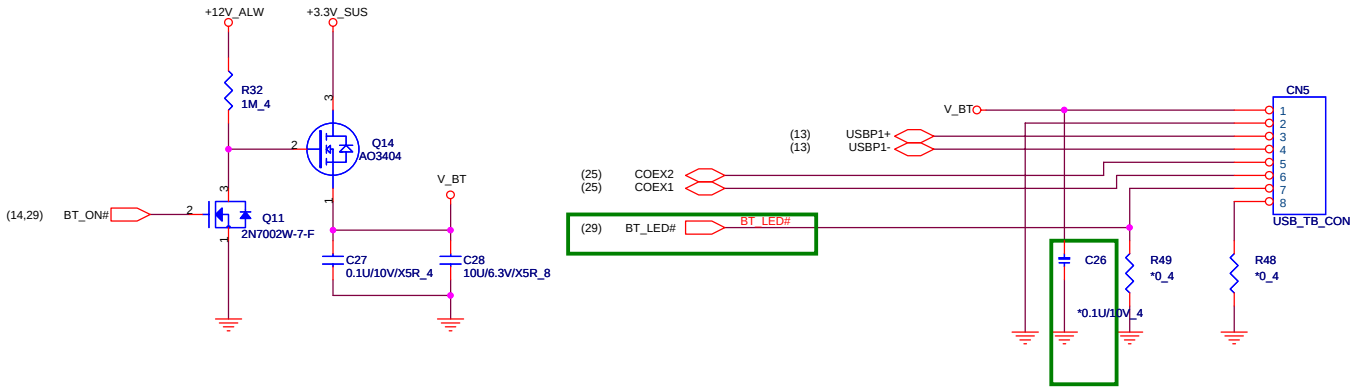


MiniCard connector 2

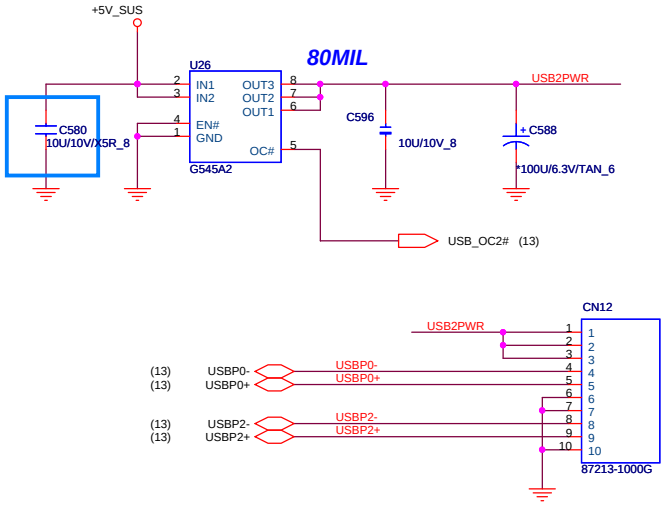


NB2/RD1	**PROJECT : AJ6** Quanta Computer Inc.	
Size: Custom	Document Number: **MINI PCI-E Card X2**	Rev: 2A
Date: Monday, August 18, 2008	Sheet 25 of 39	

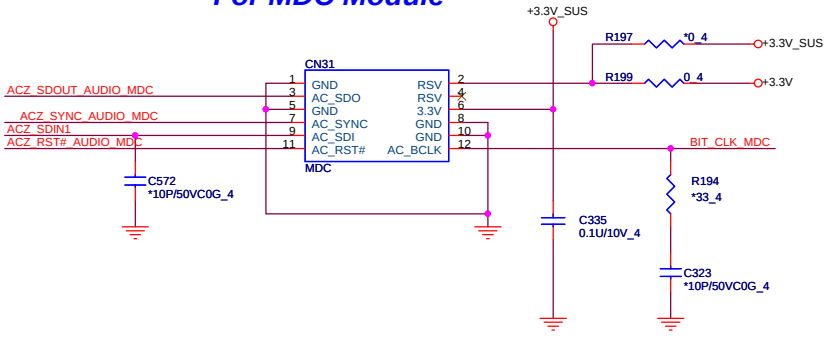
BLUETOOTH CONNECTOR



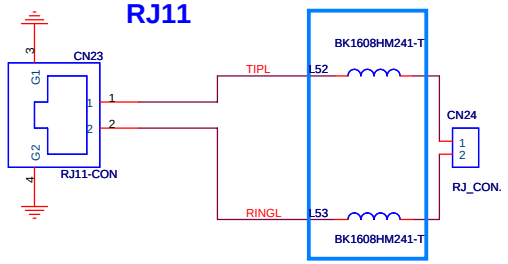
TO USB Board



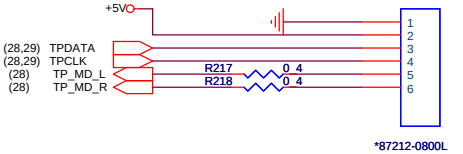
For MDC Module



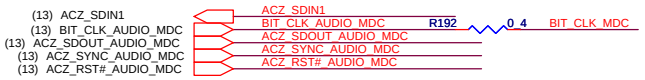
RJ11



TP module CONNECTOR



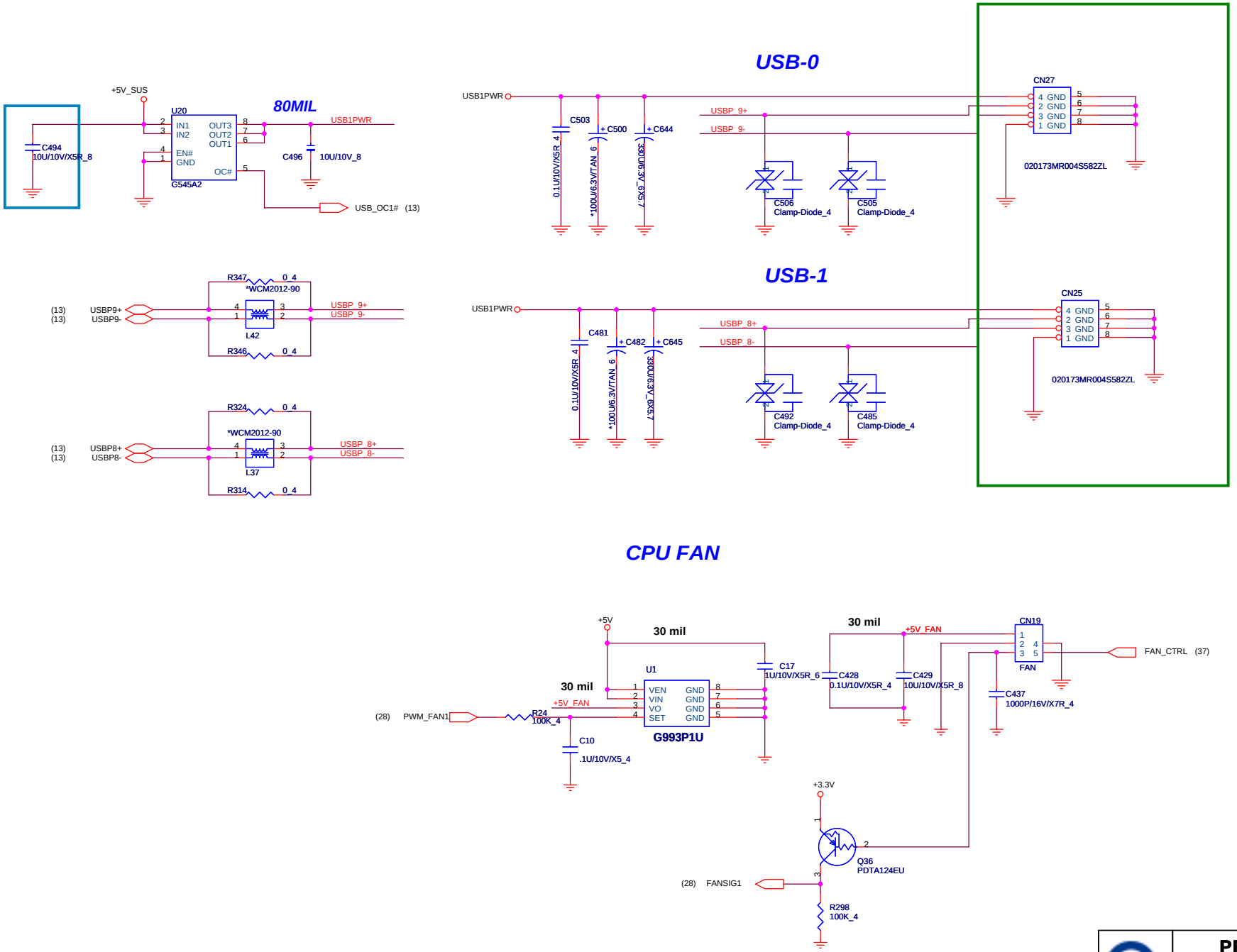
check Footprint & PN



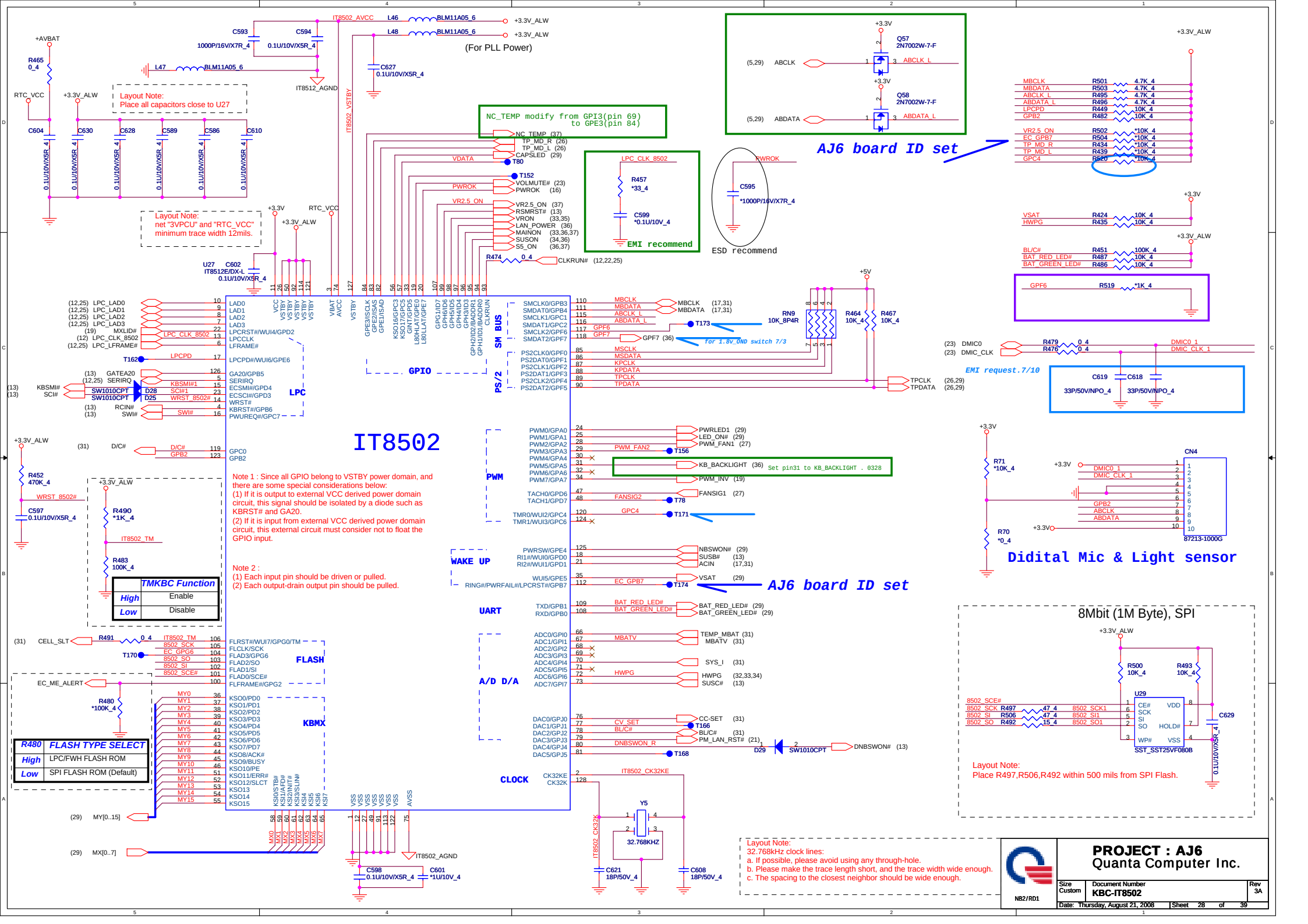
NB2/RD1

PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Bluetooth,RJ11, MDC,Small/B	3A
Date: Thursday, August 21, 2008	Sheet 26 of 39	



NB2/RD1	**PROJECT : AJ6** Quanta Computer Inc.	
Size: Custom	Document Number: **USB CONN X3ports**	Rev: 2A
Date: Monday, August 18, 2008	Sheet 27 of 39	


IT8502
AJ6 board ID set
AJ6 board ID set
Didital Mic & Light sensor
8Mbit (1M Byte), SPI
PROJECT : AJ6
Quanta Computer Inc.
KBC-IT8502
Rev 3A
Date: Thursday, August 21, 2008
Sheet 28 of 39
NB2/RD1
(For PLL Power)
EMI recommend
ESD recommend
EMI request.7/10
for 1.8V_DND switch 7/3
Set pin31 to KB_BACKLIGHT . 0328
Layout Note:
Place all capacitors close to U27
Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.
Layout Note:
Place R497,R506,R492 within 500 mils from SPI Flash.
Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.
Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.
Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.
NC_TEMP modify from GPI3(pin 69) to GPE3(pin 84)
TMKBC Function
High Enable
Low Disable
FLASH TYPE SELECT
High LPC/FWH FLASH ROM
Low SPI FLASH ROM (Default)
GPIO
SM BUS
PS/2
LPC
PWM
WAKE UP
UART
A/D D/A
FLASH
KBMX
CLOCK

TOUCHPAD SWITCH CONN

TP_L, R251 1K_4, SW3, C376 680P/50V/_4, RV1 *VARISTOR_6, TMG-533-S-V-T/R

TP_R, R252 1K_4, SW4, C377 680P/50V/_4, RV2 *VARISTOR_6, TMG-533-S-V-T/R

CN7 TOUCH PAD 12P

(26,28) TPCLK, (26,28) TPDATA, L34 BLM11A05_6, L35 BLM11A05_6, TPCLK-1, TPDATA-1

C461 *100P-ESD_6, C460 *100P-ESD_6

12 MIL

+5V, L33 0_8 5VTP, C447 0.1U/10V/X5R_4

Modify 5/20/2008

To LED board

+3.3V_LED, C100 0.1U/10V_4, CN9 88501-1001

(14) SATA_LED#

(28) CAPSLED

(25) WIRELESS_LED#

(26) BT_LED#

(14,25) WLAN_RF_OFF#

(14,26) BT_ON#

KEYBOARD
For New Keyboard use.

KEYBOARD, CN2

MX0 MX3 MX4 MY3 MX1 MX2 MY4 MX5 MX7 MY0 MY1 MX6 MY2 MY6 MY7 MY8 MY5 MY10 MY11 MY12 MY13 MY14 MY15

CP2 MY15 MY14 MY13 MY12 220PX4

CP1 MY11 MY10 MY5 MY8 220PX4

CP6 MY7 MY6 MY9 MY2 220PX4

CP5 MX5 MX4 MX2 MX1 220PX4

CP4 MY3 MX4 MX3 MX0 220PX4

CP3 MX6 MY1 MY0 MX7 220PX4

+3.3V_ALW, RP7 10KX8 (MY10 MY11 MY12 MY13)

+3.3V_ALW, RP6 10KX8 (MY0 MY1 MY2 MY9)

(36) KEY_LED_POWER, (36) KEY_LED_GND, C11 .1U/10V_4, BL121-04R-4P-L-QT6, CN3

Modify 5/20/2008

Modify 6/02/2008

(5,28) ABCLK, (5,28) ABDATA, (28) VSAT, 88513-0601, CN6

+3.3V, C32 *Varistor_4

MMB (R)

88513-0601, ABCLK, ABDATA, VSAT, GND, CN8

+3.3V, C35 *Varistor_4

MMB (L)

+3.3V_ALW, R1 10K_4, (28) NBSWON#, SW1, C1 .1U/10V/X5_4, SWITCH_POWER

SWITCH LED

+3.3V_LED, D2, D1, R86 300_4, R85 300_4

LED INDICATOR

(28) BAT_GREEN_LED#, (28) BAT_RED_LED#

R273 *300_4 BAT_G_LED#_R, R274 *300_4 BAT_R_LED#_R

D19 LED_BLUE/RED, +3.3V_ALW

Charge LED

+3.3V_ALW, R275 300_4, -PWRLED_R, D18 LED

POWER LED

R509 *0_4, R510 2M_4, D31 SW1010CPT, C636 0.47U/10V/X7R_6, Q59 2N7002E

(28) PWRLED1, +3.3V_S5

+12V_ALW, LED_ON#1, R364 1M_6, Q49 PDTC144EU, Q47 *2N7002E, Q52 2N7002E

(28) LED_ON#, +5V_LED, +3.3V_LED, C543 *0.1U/10V/X5R_4, C555 0.1U/10V/X5R_4

reserver circuit

+5V, +5V_LED, +3.3V_LED, R358 100K_4, R357 *47_4, R367 47_4

Q50 2N7002W-7-F, Q46 *2N7002W-7-F, Q51 2N7002W-7-F

LED_ON#1

R521 300_4, R302 300_4

R577 2M_4, Q71 2N7002E, D35 SW1010CPT, C647 0.47U/10V/X7R_6

+3.3V_S5

R576 2M_4, Q70 2N7002E, D34 SW1010CPT, C646 0.47U/10V/X7R_6

"slowly pulse" light to dark about 2 second ,Modify by 8/18

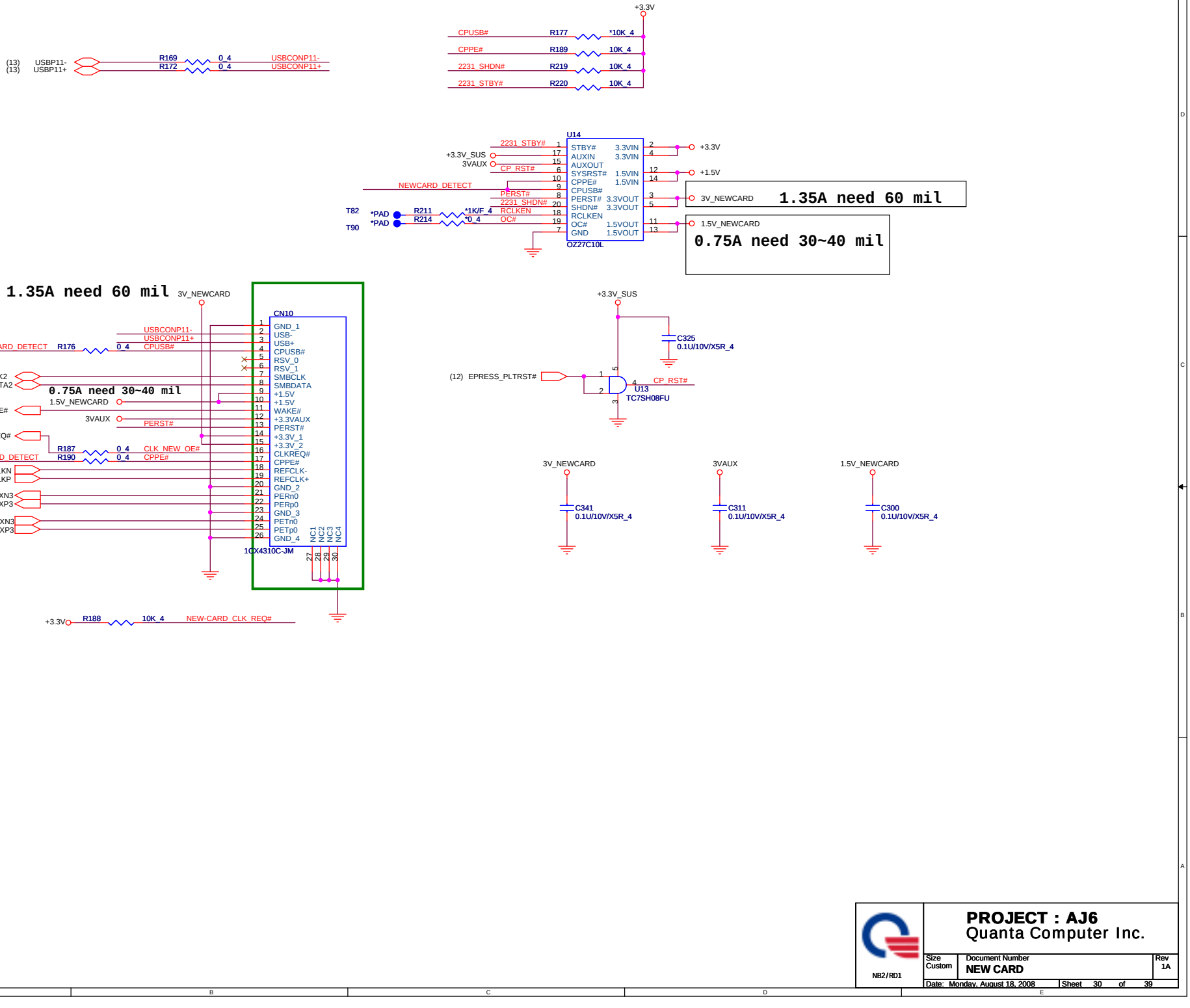
NB2/RD1

PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	TP/KB/LED/SW CONN.	3B

Date: Thursday, August 21, 2008 Sheet 29 of 39

NEWCARD



NB2/RD1	PROJECT : AJ6 Quanta Computer Inc.		
	Size: Custom	Document Number: NEW CARD	Rev: 1A
	Date: Monday, August 18, 2008	Sheet 30 of 39	

BATTERY CHARGER

TOP DC_JACK
MXM 90W (DFPJ05MR006) Blue
UMA 65W (DFPJ05MR007) yellow

Place close to EC,

Modify 8/18/2008

Place these CAPs close to FETs

R1

R2

CELL_SLT = 1 -- 3 S (Cells = GND 3S)
CELL_SLT = 0 -- 4 S (Cells = VDD 4S)

Setting the Vin min to 12V
For ACSET 1.26V

Setting the Vin min to 17V
For EN = 1.06V

Charging Curret setting =>
I chg = 165mV / R2 * (Vchlim / 3.3V)

V ACLIM = VREF * (Rlow // 152K) / (Rhigh // 152K + Rlow// 152K)
Iin_max = (1/R1)[(0.05/Vref) * Vaclim + 0.05]

VADJ =
VERF >> 4.2V +5%
Float >> 4.2V
GND >> 4.2 -5%

Input Current monitor
V icm = 19.9 * (Vcsip - Vcsin)

Battery Low 7.5V

ADP TYPE	Rhigh	P/N
65W	178K/F_4	CS41782FB11
90W	11K/F_4	CS31102FB11

PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CHARGER (ISL6251)	3A

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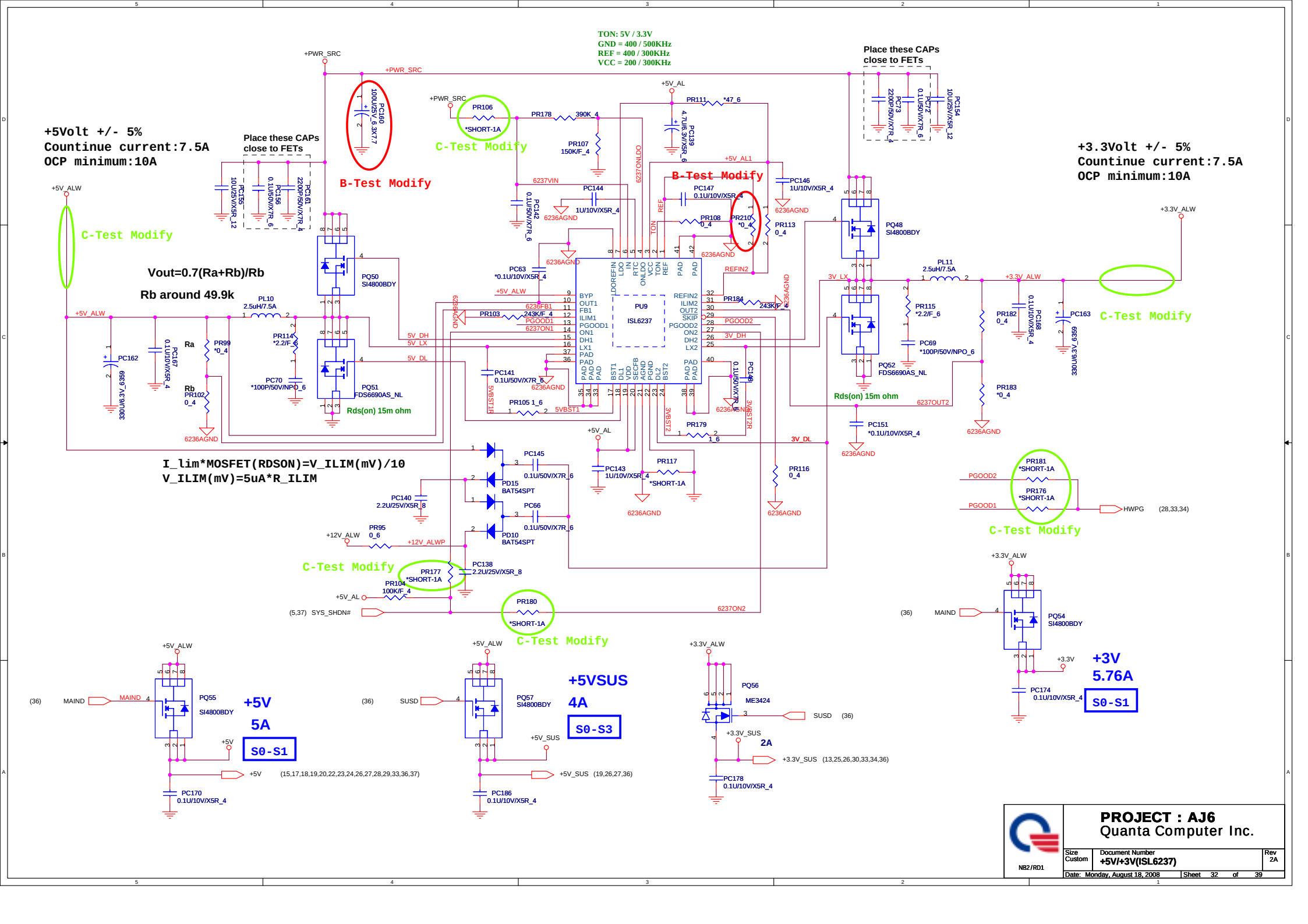
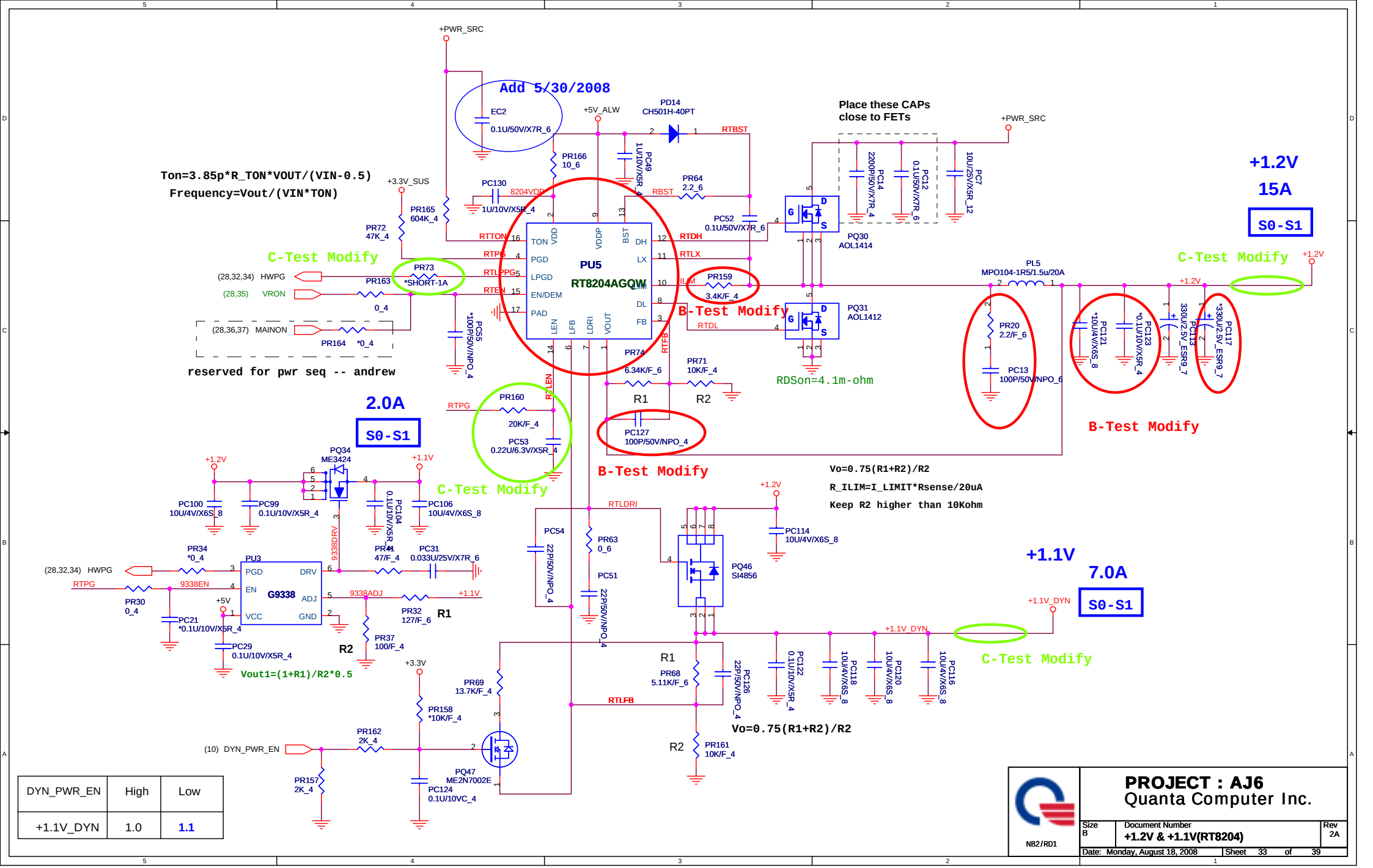
NB2/RD1


TON: 5V / 3.3V
GND = 400 / 500KHz
REF = 400 / 300KHz
VCC = 200 / 300KHz
+5Volt +/- 5%
Countinue current:7.5A
OCP minimum:10A
+3.3Volt +/- 5%
Countinue current:7.5A
OCP minimum:10A
Place these CAPs close to FETs
Place these CAPs close to FETs
B-Test Modify
B-Test Modify
C-Test Modify
C-Test Modify
C-Test Modify
C-Test Modify
C-Test Modify
C-Test Modify
Vout=0.7(Ra+Rb)/Rb
Rb around 49.9k
I_lim*MOSFET(RDSON)=V_ILIM(mV)/10
V_ILIM(mV)=5uA*R_ILIM
Rds(on) 15m ohm
Rds(on) 15m ohm
PU9
ISL6237
PQ48 SI4800BDY
PQ50 SI4800BDY
PQ51 FDS6690AS_NL
PQ52 FDS6690AS_NL
PQ54 SI4800BDY
PQ55 SI4800BDY
PQ56 ME3424
PQ57 SI4800BDY
PD15 BAT54SPT
PD10 BAT54SPT
PL10 2.5uH/7.5A
PL11 2.5uH/7.5A
+5V
5A
S0-S1
+5VSUS
4A
S0-S3
+3V
5.76A
S0-S1
2A
PROJECT : AJ6
Quanta Computer Inc.
+5V/+3V(ISL6237)
Monday, August 18, 2008
NB2/RD1



DYN_PWR_EN	High	Low
+1.1V_DYN	1.0	1.1

NB2/RD1

PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
B	+1.2V & +1.1V(RT8204)	2A

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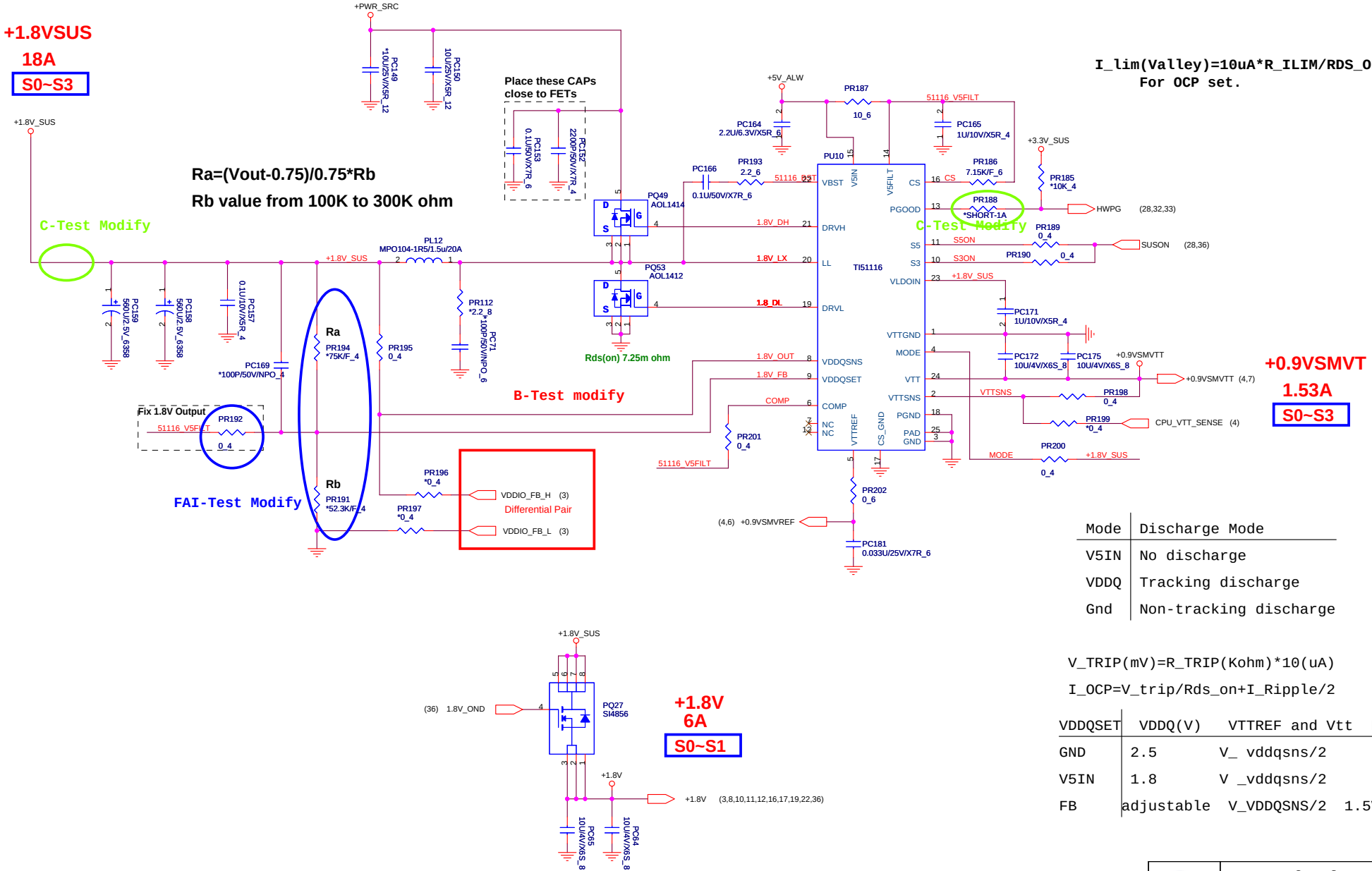

Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

V_TRIP(mV)=R_TRIP(Kohm)*10(uA)

I_OCP=V_trip/Rds_on+I_Ripple/2

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	V_ vddqsns/2	DDR
V5IN	1.8	V _vddqsns/2	DDR2
FB	adjustable	V_VDDQSNS/2	1.5V<VDDQ<3V

PROJECT : AJ6
Quanta Computer Inc.

NB2/RD1

Size	Document Number	Rev
Custom	1.8VSUS/DDR_VTER/+1.8V/2.5V	2A
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OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	0	0	X
+3.3V	X	X	0
+5V	X	0	X

Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

C-Test Modify

Close to CPU socket

B-Test Modify

C1-Test Modify

FAI Modify

Pin 49 is GND Pin

ISL6265HRTZ-T

Close to CPU socket

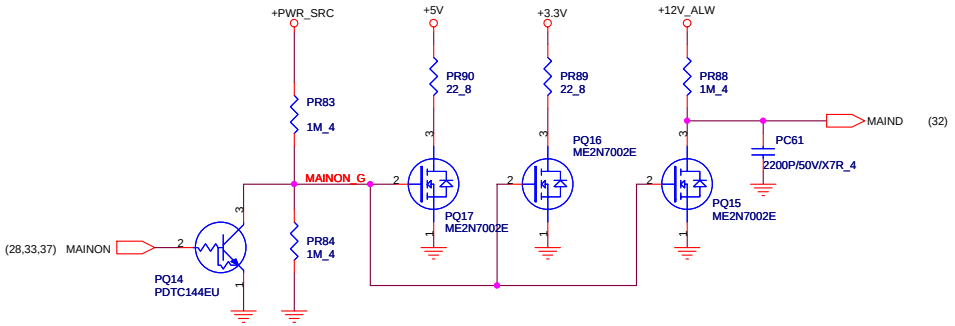
Parallel

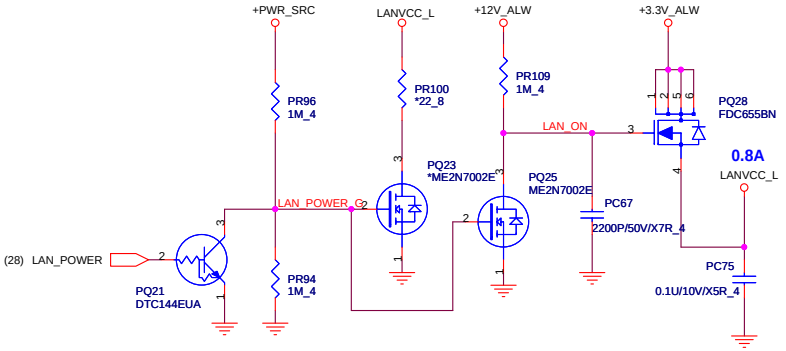
Close to CPU socket

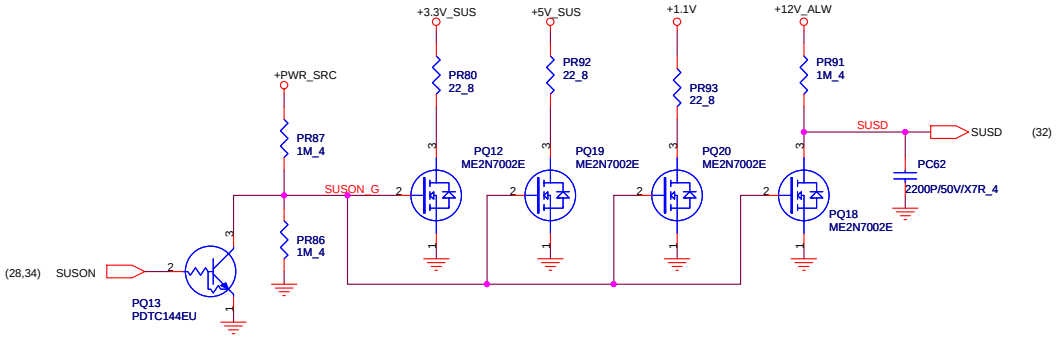
Reserve for uni-plane

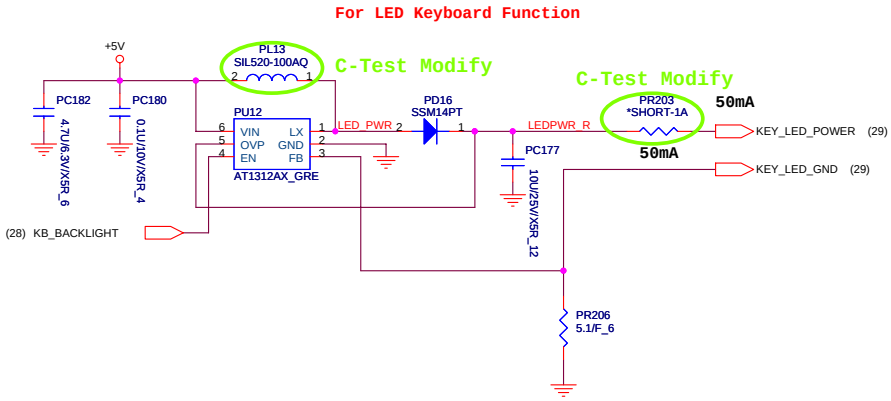
Reserve for uni-plane

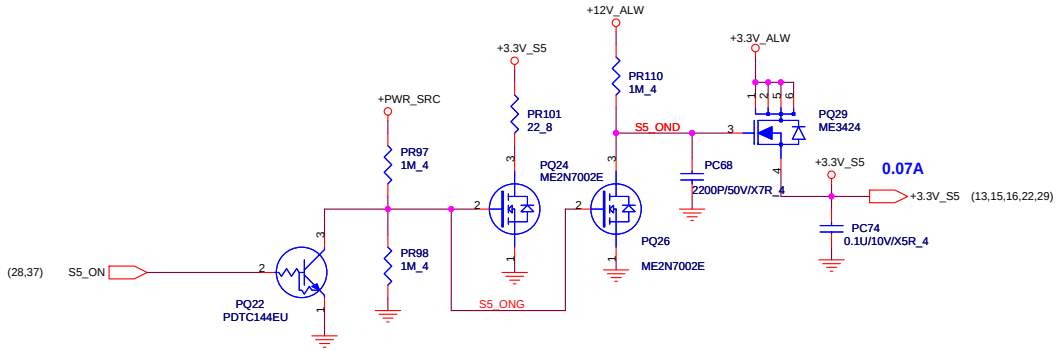
PROJECT : AJ6	
Quanta Computer Inc.	
Size: C	Document Number: CPU_CORE(ISL6265)
Rev: 3B	
NB2/RD1	
Date: Thursday, August 21, 2008	Sheet 35 of 39

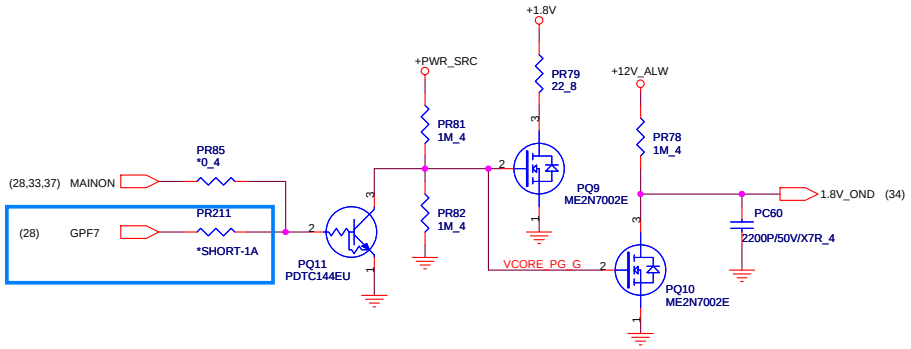




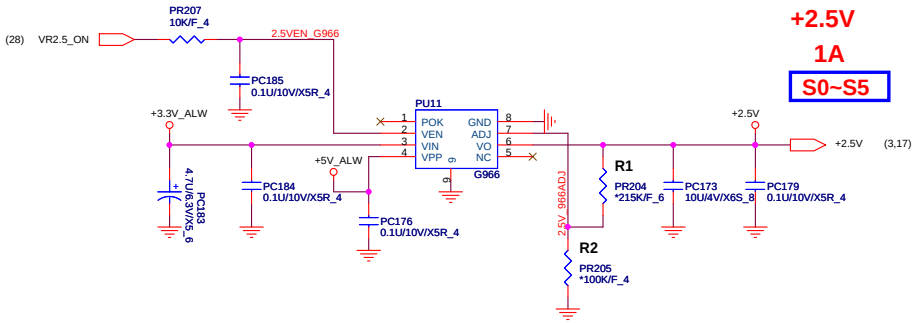








N82/RD1	**PROJECT : AJ6** Quanta Computer Inc.	
	Size: Custom Document Number: **DISCHARGE**	Rev: 2A
	Date: Monday, August 18, 2008	Sheet 36 of 39

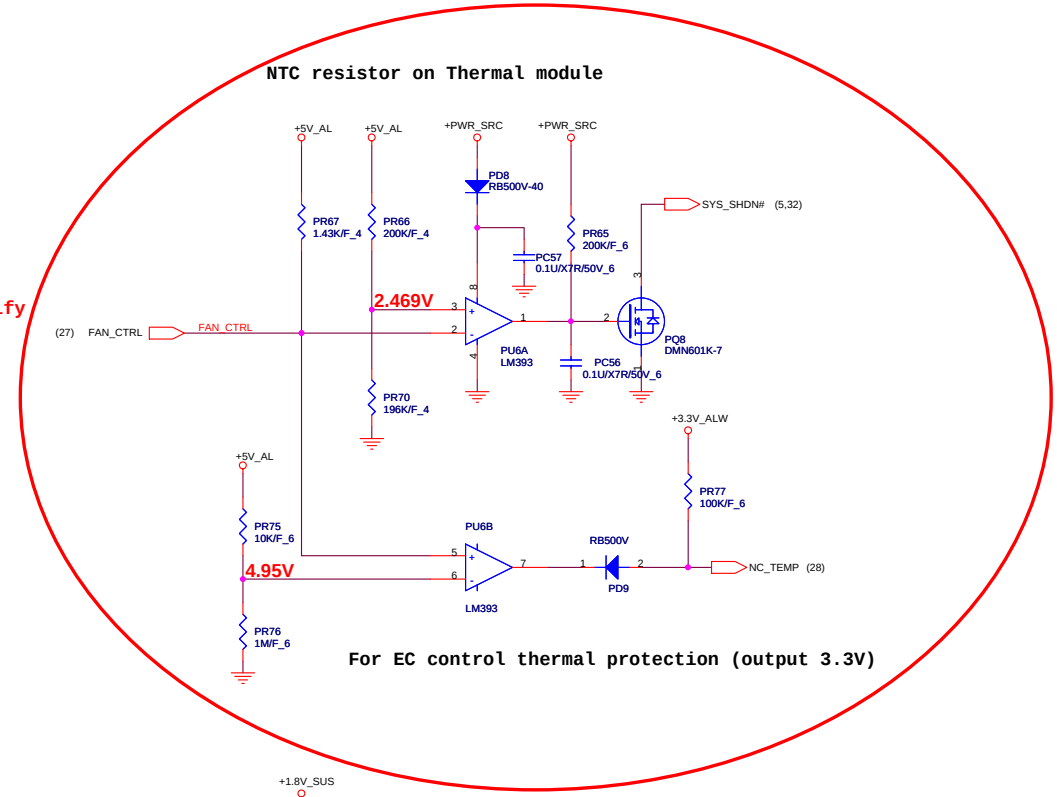


+2.5V

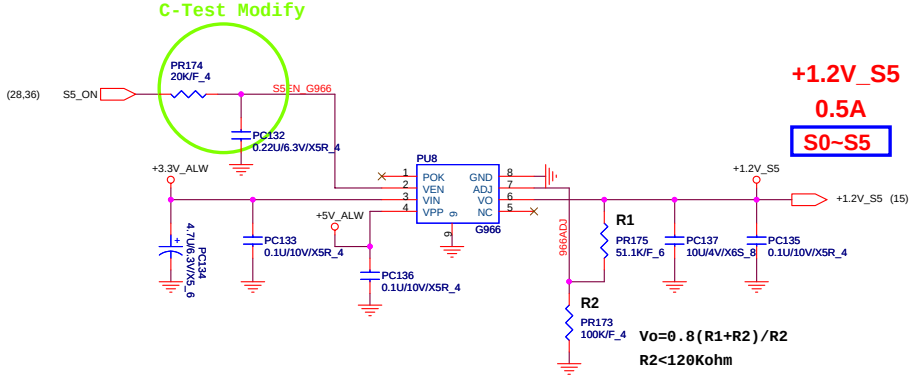
1A

S0~S5

B-Test Modify



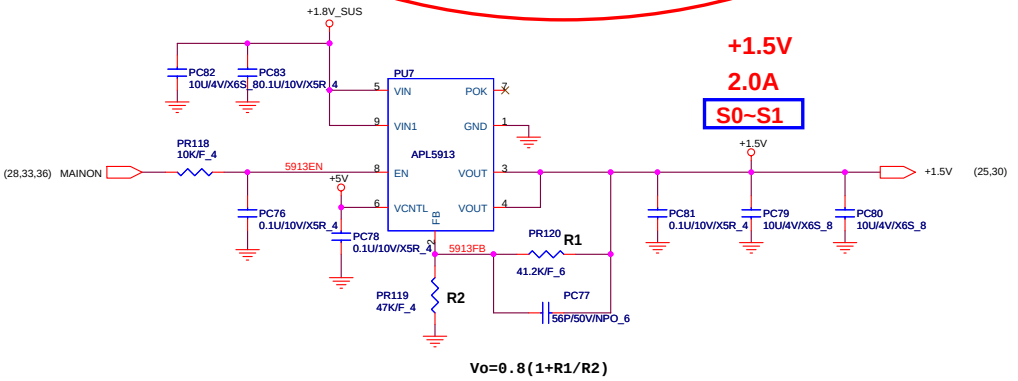
C-Test Modify



+1.2V_S5

0.5A

S0~S5

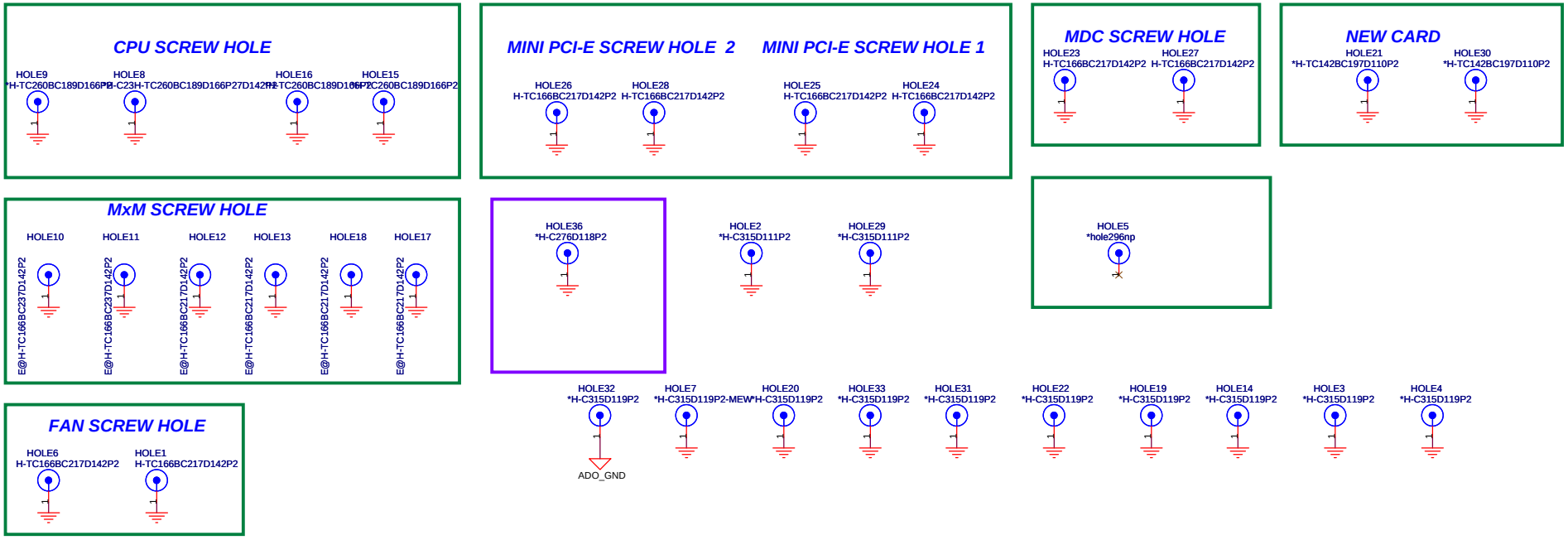


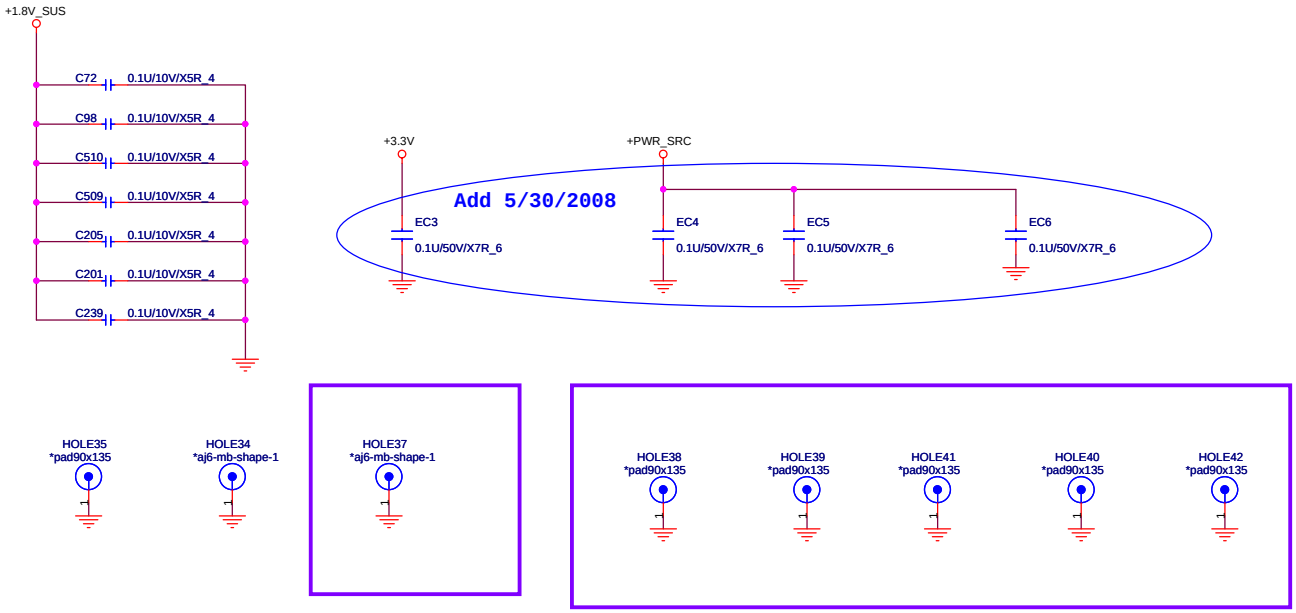
+1.5V

2.0A

S0~S1

NB2/RD1	PROJECT : AJ6 Quanta Computer Inc.	
Size: Custom	Document Number: 1.2V_S5/+1.5/+2.5V	Rev: 2A
Date: Monday, August 18, 2008	Sheet 37 of 39	





EMI request 19/08/2008

NB2/RD1

PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EMI PAD &Hole	2A
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MODEL: REV

CHANGE LIST

AJ6 MB

1A	***First release***
2A	***Page5:Add Q66,Q67 for EC drivinng / Add Q68,R574 & swap U3 pin4, pin6 for system shootdown*** ***Page9:Change PCIE CAP. from X5R to X7R & modify C_PEG_TX for UMA's HDMI detect issue*** ***Page10:Delet R115 for UMA SKU.*** ***Page15:Modify R83,R184,R368,R370,R371,R372,R,386,R387,R391,R392 for board ID / Chanhe C338,C327 for accuracy*** ***Page17:Add Q60,R517 for MXM discharge / Add R516,D32 for MXM timming / Modify C215,C210,C209,Q19,C238 for MXM power express /Add Q62,Q63 for MXM smbus*** ***Page18:Add Q61,R518 for HDMI HPD sense issue / modify Q1,Q2 for UMA HDMI smbus issue / delete D4,D5 & change R5,R6 value*** ***Page19:Modify & add Q69,C656,C657R567,R569 for LCD slight light issue / Add RP40 for MXM*** ***Page21:Add R95 for Lan chip power / change R60,R61,R62,R63 package*** ***Page23:Add Q64,Q65,R570,R571,R572 for SPDIF's LED issue / Change R271,R272,R265,R266 for volume issue /Change R473,R472,R471,R470 for EMI issue*** ***Page25:Add R562,R563,R564,R565,R566 for Acer LPC debug use / Add D12,R213 for WLAN LED*** ***Page26:Delete MODEM CAP. C166,C165*** ***Page27:Add C644,C645 for USB*** ***Page28:Modify U27 pin112 to AJ6 board ID setting / Swap pin98 & pin107 / Delete C601 for IT8502 issue /Change C621, C608 of value for accuracy*** ***Page29:Swap NC7,CN3 connector & modify circuit / Modify CN8 circuit / Delete R357 is no use*** ***Page32:Add a resister to connect PU9 pin1 and pin32 / Add PC160 in the circuit.*** ***Page33:Change PU5 PN from AL008204000 to AL08204001 / Change PR159 PN to CS23402FB08 / Add PR20, PC13, PC127 in the circuit / Delete PC117, PC123, PC121 in the circuit*** ***Page34:Change PR191 from 51.1K/F_4 to 52.3K/F_4 (CS35232FB10).*** ***Page35:Delete PC17, PC18 in the circuit / Add PC91 in the circuit*** ***Page36:Add PR90,PR89,PR80,PR92,PR93,PR101,PR79,PQ17,PQ16,PQ12,PQ19,PQ20,PQ24,PQ9 in the circuit for discharge*** ***Page37:Add PR67, PR66, PD8, PC57, PR65, PQ8, PC56, PU6, PR70, PR75, PR76, PD9, PR77 in the circuit for Acer thermal protection*** ***Page38:Add EC3,EC4,EC5,EC6 for EMI***
3A	***Page9:Add R45,R51,R64,R65,R68,R69,R72,E73 to solve the HDMI issue*** ***Page10 : for CRT filicker, change C179,C191,C491,C125,C192 value from 2.2u to 10u.*** ***Page14 : change the board ID. 7/10*** ***Page17 : Duo to cost down, so to remove Q25 ,Q45 from MXM BOM.*** ***Page19 : add LCD panel circuit to fix white display when system boot up.*** ***Page21 : to solve the Lan issue, ADD C479,C480*** ***Page23 : change Gain from 15.6 to 10 db. 7/8*** ***Page24 : Change C498,C499 ,C585,C587 value form 3900P to 0.001U*** ***Page26 : to solve the EMI issue, ADD L52,L53*** ***Page28 : For EMI request. add C618,C619 7/10*** ***Page26 : to solve the EMI issue, ADD L52,L53*** ***Page29 : Change R509 PN from 2M to 0ohm. Change R85,R86,R275 ,R273,R274 to 300 ohm, Del D31& C636 & D2 from BOM*** ***Page26 : to solve the EMI issue, ADD L52,L53*** ***Page31 : PL13 PN change to CV01014TZ01***
3B	***Page2 : ADD C648(CH11006JB00) , for EMI request (+1.2v)*** ***Page11 :Change C56 and C493 from 4.7u/6.3V to 330u/2V (CH733RY8802) to solve" HIGH POWER NOSIE ISSUE"*** ***Page17 :Add C238 (CC71004MZ81) to solve" HIGH POWER NOSIE ISSUE"*** ***Page29 :For slowly pulse" light to dark about 2 second, ADD R510,R576,R577, Q70,Q71,D34,D35 ,C636,C646,C647 ,R302 ,R521 ; DEL R273,R274,R509*** ***Page35 :Change PC90 and PC92 from 10u/25V to 27u/25V (CC62704MZ02) to solve" HIGH POWER NOSIE ISSUE"***

MODEL / PAGE	AJ6 MB FROM	AJ6 MB TO
1	1A	
2	1A	3B
3	1A	
4	1A	
5	2A	
6	1A	
7	1A	
8	1A	
9	3A	
10	3A	
11	1A	3B
12	1A	
13	1A	
14	3A	
15	2A	
16	1A	
17	3A	3B
18	2A	
19	3A	
20	1A	
21	3A	
22	1A	
23	3A	
24	3A	
25	2A	
26	3A	
27	2A	
28	3A	
29	3A	3B
30	1A	
31	3A	
32	2A	
33	2A	
34	2A	
35	2A	3B
36	2A	
37	2A	
38	2A	
39	3A	3B

Project :AJ6 MB	MB Assy' P/N: 31AJ6MB0030/40	Document No.:
Approved by : Johnny_O	Drawing by :Kenneth Huang	DATE: 2008/8/19

NB2/RD1

PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EC	3B

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