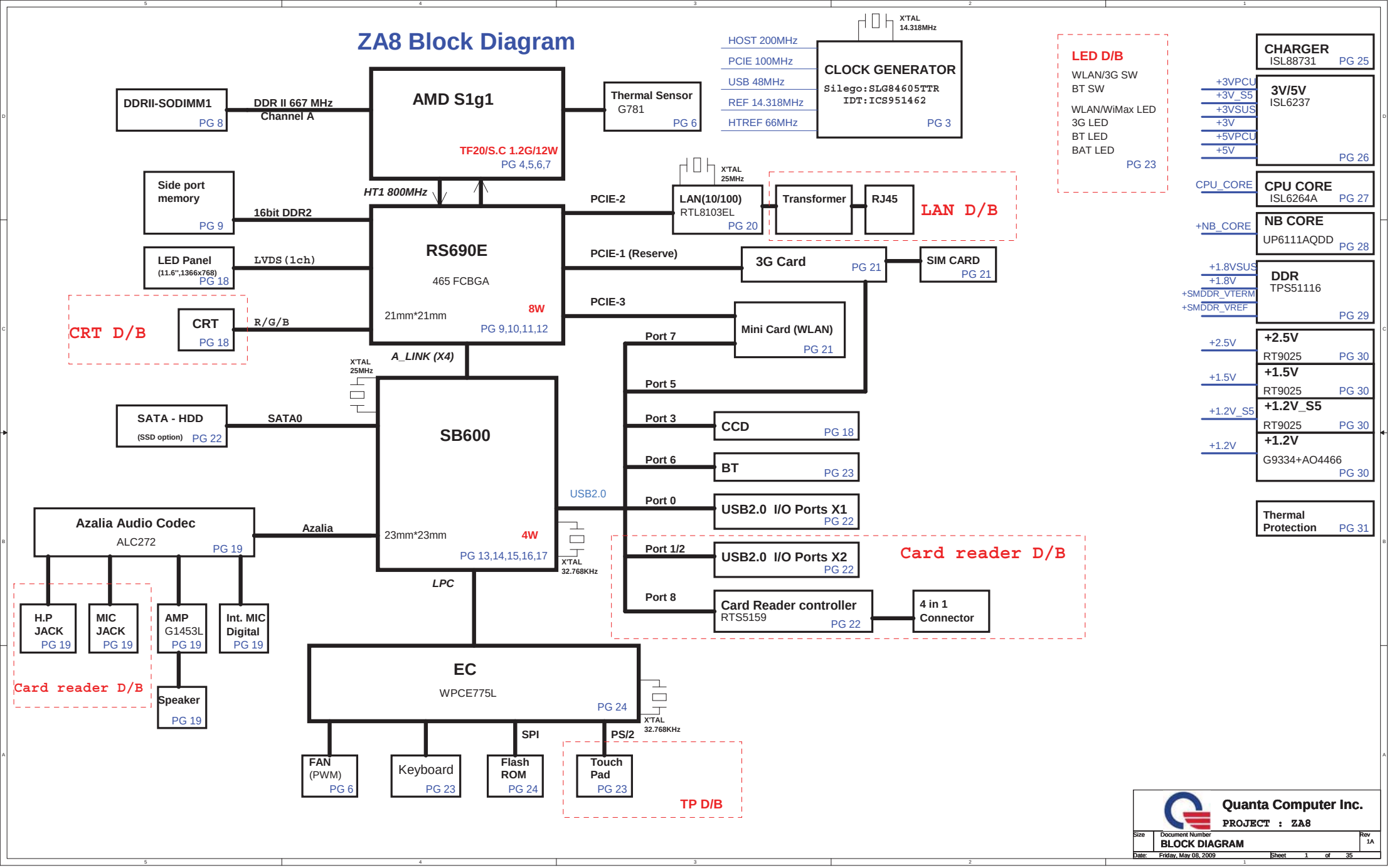
ZA8 Block Diagram



Quanta Computer Inc.

PROJECT : ZA8

Size	Document Number	Rev
	BLOCK DIAGRAM	1A

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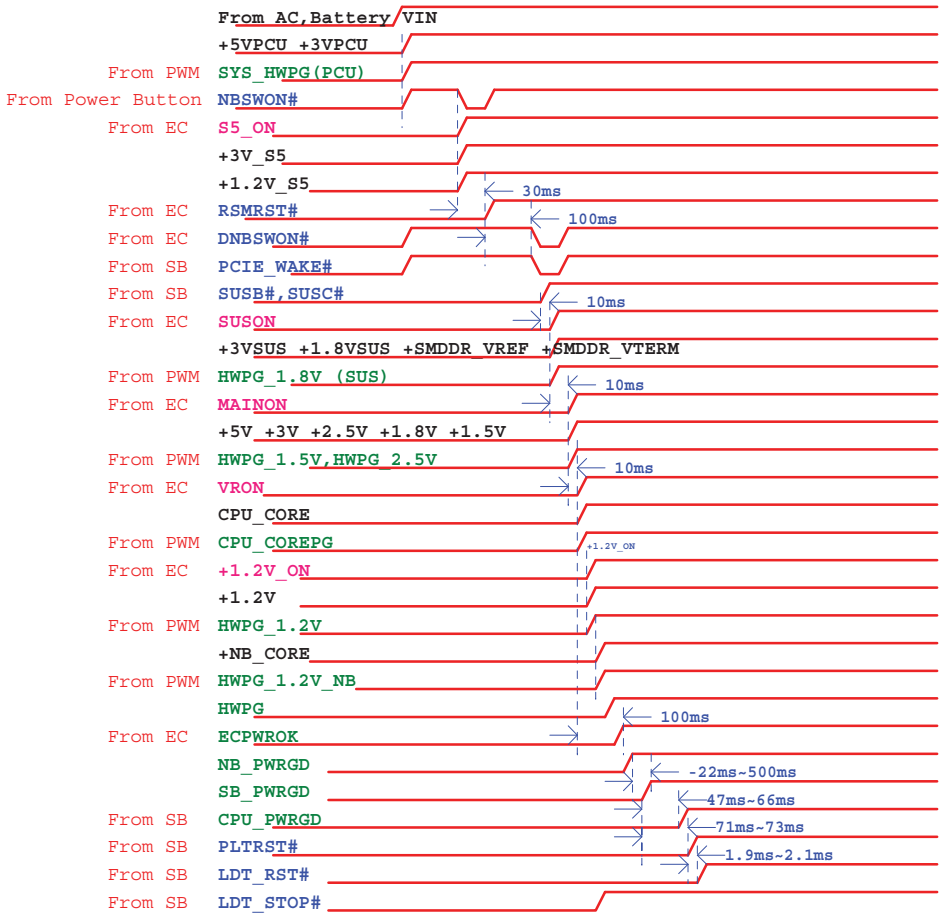
ZA8 Power On Sequence



*Note: EC will sampling SUSB# & SUSC# every 5ms.

BOM naming rule

Items	Function	Name	Description
1	3G Module	3G@	
2	HDT debug function	HDT@	
3			
4			
5			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			

AMD SB600 SMBUS Table

	CLK GEN	RAM	Mini Card (WLAN)
SB600 SDATA0/SCLK0(+3V)	V	V	V
SB600 SDATA1/SCLK1(+3V_S5)			
Power Plane	+3V	+3V	+3V
MOS CKT	Reserve	Reserve	Reserve

EC SMBUS Table

	Battery	CPU thermal Sensor	EC EEPROM
EC775 SDATA1/SCLK1(+3VPCU)	V		
EC775 SDATA2/SCLK2(+3VPCU)		V	
EC775 SDATA3/SCLK3(+3VPCU)			V
EC775 SDATA4/SCLK4(+3VPCU)			
Power Plane	+3VPCU	+3V	+3VPCU
MOS CKT	X	X	X

Quanta Computer Inc.
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Size | Document Number: SYSTEM INFORMATION | Rev 1A
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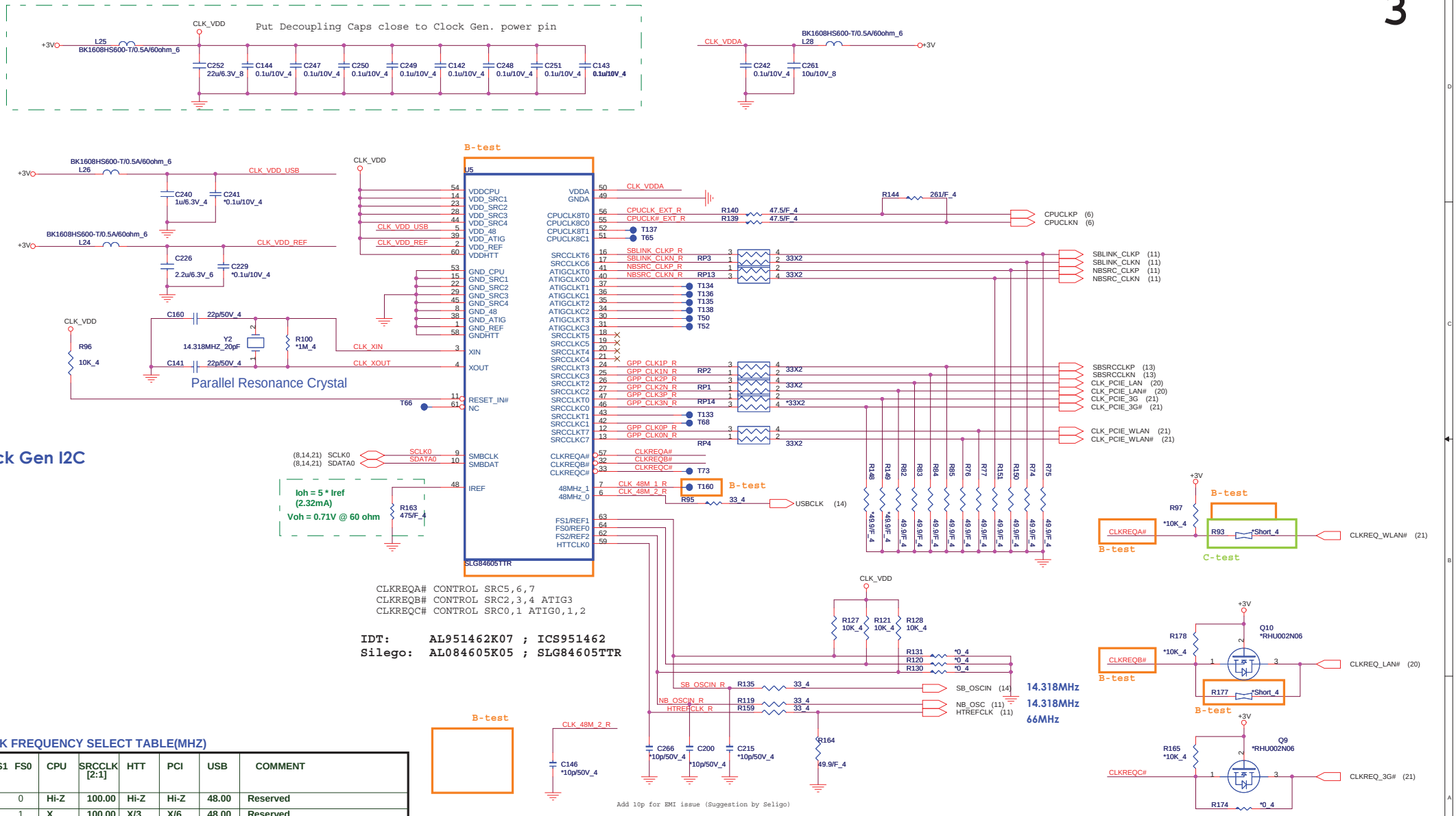
CLK_GEN(CLK)



CLKREQA# CONTROL SRC5,6,7
CLKREQB# CONTROL SRC2,3,4 ATIG3
CLKREQC# CONTROL SRC0,1 ATIG0,1,2

IDT: AL951462K07 ; ICS951462
Silego: AL084605K05 ; SLG84605TTR

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal Turion/Sempron operation

Quanta Computer Inc.
PROJECT : ZA8

Size	Document Number	Rev
	CLOCK GENERATOR	1A

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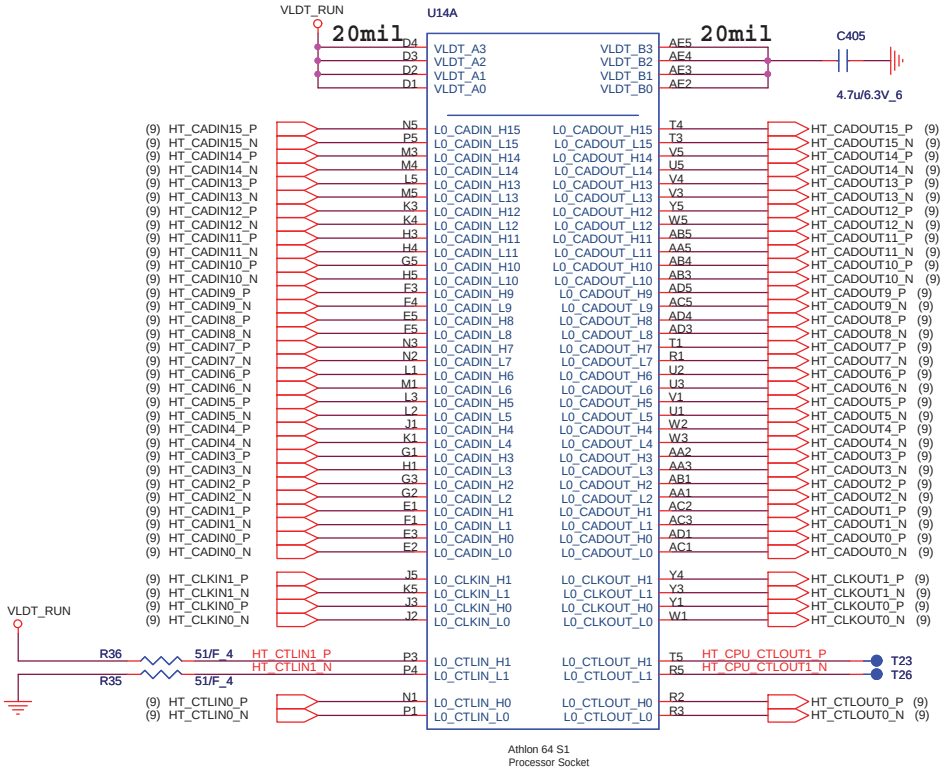

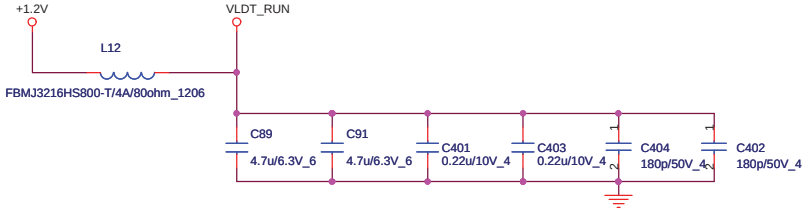

Power name	Description	Voltage
VLDT_A/B	HyperTransport I/O ring power supply	1.2V

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Size	Document Number	Rev
	TURION 64 HT I/F	1A
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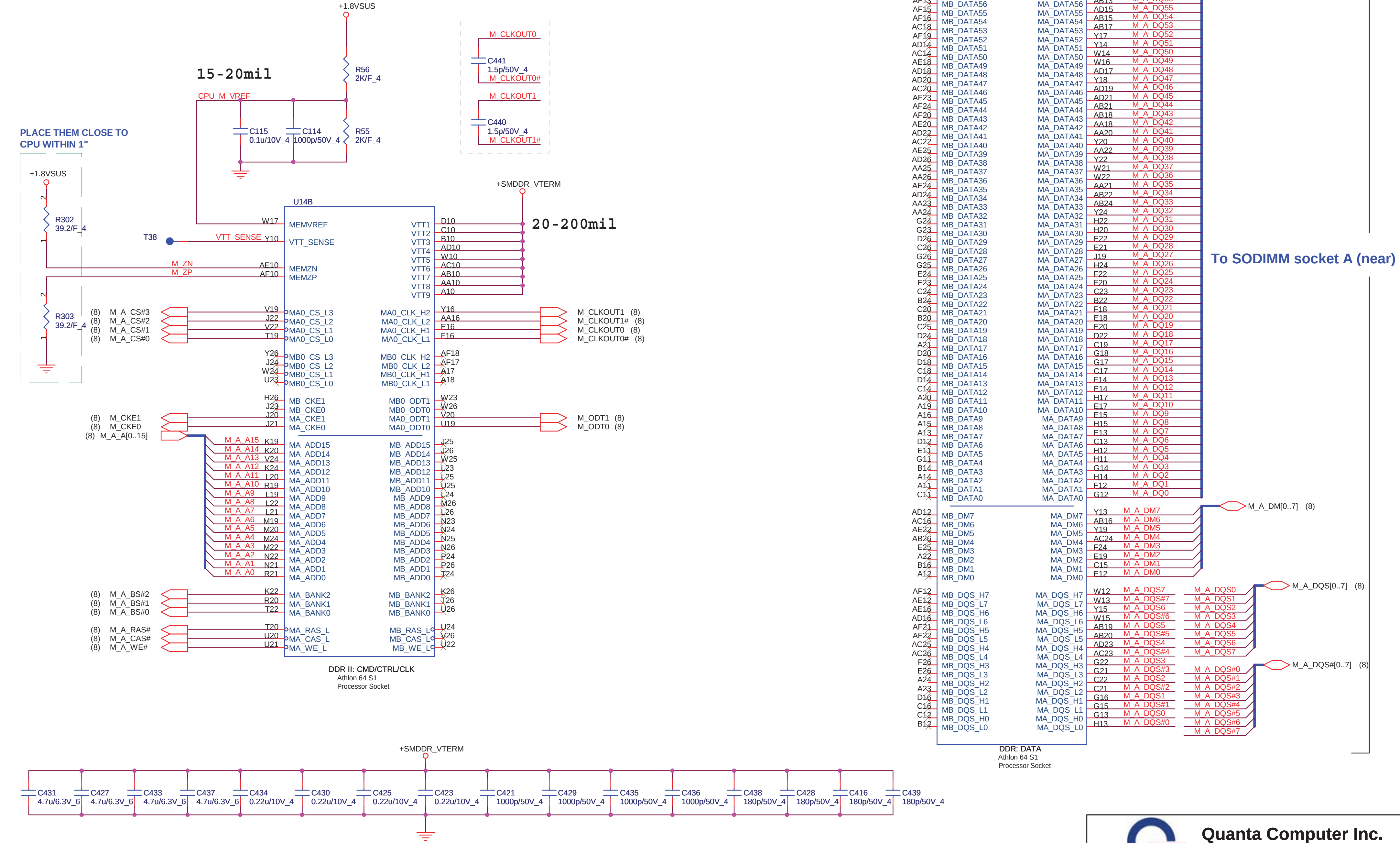
(CPU)

Processor DDR2 Memory Interface



15-20mil
+1.8VSUS
R56 2K/F_4
R55 2K/F_4
CPU_M_VREF
C115 0.1u/10V_4
C114 1000p/50V_4
PLACE THEM CLOSE TO CPU WITHIN 1"
R302 39.2/F_4
R303 39.2/F_4
T38
VTT_SENSE
M_ZN
M_ZP
M_CLKOUT0
C441 1.5p/50V_4
M_CLKOUT0#
M_CLKOUT1
C440 1.5p/50V_4
M_CLKOUT1#
+SMDDR_VTERM
20-200mil
U14B
MEMVREF
VTT_SENSE
MEMZN
MEMZP
VTT1 VTT2 VTT3 VTT4 VTT5 VTT6 VTT7 VTT8 VTT9
(8) M_A_CS#3
(8) M_A_CS#2
(8) M_A_CS#1
(8) M_A_CS#0
M_CLKOUT1 (8)
M_CLKOUT1# (8)
M_CLKOUT0 (8)
M_CLKOUT0# (8)
(8) M_CKE1
(8) M_CKE0
(8) M_A_A[0..15]
M_ODT1 (8)
M_ODT0 (8)
(8) M_A_BS#2
(8) M_A_BS#1
(8) M_A_BS#0
(8) M_A_RAS#
(8) M_A_CAS#
(8) M_A_WE#
DDR II: CMD/CTRL/CLK
Athlon 64 S1
Processor Socket
U14C
M_A_DQ[0..63] (8)
To SODIMM socket A (near)
M_A_DM[0..7] (8)
M_A_DQS[0..7] (8)
M_A_DQS#[0..7] (8)
DDR: DATA
Athlon 64 S1
Processor Socket
+SMDDR_VTERM
C431 4.7u/6.3V_6
C427 4.7u/6.3V_6
C433 4.7u/6.3V_6
C437 4.7u/6.3V_6
C434 0.22u/10V_4
C430 0.22u/10V_4
C425 0.22u/10V_4
C423 0.22u/10V_4
C421 1000p/50V_4
C429 1000p/50V_4
C435 1000p/50V_4
C436 1000p/50V_4
C438 180p/50V_4
C428 180p/50V_4
C416 180p/50V_4
C439 180p/50V_4

Power name	Description	Voltage
VTT	VTT Power	0.9V

Quanta Computer Inc.

PROJECT : ZA8

Size	Document Number	Rev
	TURION 64 DDRII I/F	1A

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ATHLON Control and Debug

(CPU)

If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pulldown to VSS.

+1.8VSUS
R283 *300_4
R278 *300_4
R274 300_4
(13) CPU_SIC
(13) CPU_SID
R277 *0_4
R281 *0_4
CPU_SIC_R
CPU_SID_R

+1.8VSUS
(24,27) CPU_COREPG
Q24 FDV301N
R264 *10K_4
D18 *BAS316
R267 100K_6
R265 10K_4
H_THERMTRIP#
Q25 MMBT3904
R262 *0_6
SB_THERMTRIP# (14)
SYS_SHDN# (26,31)

(3) CPUCLKP
C422 3900p/50V_4
CPU_CLKIN_SC_P
R309 169/F_6
(3) CPUCLKN
C417 3900p/50V_4
CPU_CLKIN_SC_N

B-test
(13) CPU_PWRGD
(11,13) LDT_STOP#
(13) LDT_RST#
CPU_ALL_PWROK
CPU_LDTSTOP#
CPU_HT_RESET#
R280 680_4
R297 680_4
R289 680_4

+1.8VSUS
CPU_TEST27_SINGLECHAIN R300 *300_4
CPU_TEST26_BURNIN# R286 300_4
CPU_PRESENT# R42 *1K/F_4
CPU_TEST25_H_BYPASSCLK_H R51 510/F_4
CPU_TEST21_SCANEN R45 300_4
CPU_TEST20_SCANCLK2 R290 *300_4
CPU_TEST24_SCANCLK1 R293 *300_4
CPU_TEST22_SCANSHIFTEN R298 *300_4
CPU_TEST12_SCANSHIFTENB R46 *300_4
CPU_TEST15_BP1 R50 *300_4
CPU_TEST14_BP0 R49 *300_4
CPU_TEST25_L_BYPASSCLK_L R52 510/F_4
CPU_TEST19_PLLTEST0 R53 300_4
CPU_TEST18_PLLTEST1 R54 300_4

+2.5V
PBY201209T-300Y-N/4A/30ohm_8
L17
VDDA_RUN
C93 *100u/6.3V_3528
C94 4.7u/6.3V_6
C106 0.22u/10V_4
C96 3300p/50V_4

+1.8VSUS
R263 300_4
R276 300_4

U14D
F8 VDDA2
F9 VDDA1
AF6 THERMTRIP_L
AC7 PROCHOT_L
H_THERMTRIP#
H_PROCHOT#

T35 CPU_HT_RESET#
T121 CPU_ALL_PWROK
T122 CPU_LDTSTOP#
B7 PRESET_L
A7 PWROK
F10 PLDTSTOP_L

CPU_SIC_R
CPU_SID_R
AF4 SIC
AF5 SID

VLDT_RUN
R37 44.2/F_4
R38 44.2/F_4
CPU_HTREF1
CPU_HTREF0
P6 HT_REF1
R6 HT_REF0
place them to CPU within 1"

T33
T31
F6 VDD_FB_H
E6 VDD_FB_L
T29
T30
W9 VDDIO_FB_H
Y9 VDDIO_FB_L

CPU_CLKIN_SC_P
CPU_CLKIN_SC_N
A9 CLKIN_H
A8 CLKIN_L

CPU_DBRDY
G10 DBRDY

CPU_TMS
CPU_TCK
CPU_TRST#
CPU_TDI
AA9 TMS
AC9 TCK
AD9 TRST_L
AF9 TDI

DBREQ_L
E10 CPU_DBREQ#
TDO
AF9 CPU_TDO

CPU_TEST25_H_BYPASSCLK_H F9
CPU_TEST25_L_BYPASSCLK_L E8
CPU_TEST19_PLLTEST0 G9
CPU_TEST18_PLLTEST1 H10
AA7
C2
D7
E7
F7
C7
AC8
TEST25_H
TEST25_L
TEST19
TEST18
TEST13
TEST9
TEST17
TEST16
TEST15
TEST14
TEST12

T120 CPU_TEST17_BP3
T39 CPU_TEST16_BP2
CPU_TEST15_BP1
CPU_TEST14_BP0
CPU_TEST12_SCANSHIFTENB

C3
AA6
W7
W8
Y6
AB6
TEST7
TEST6
TEST5
TEST4
TEST3
TEST2

H_THERMDC
H_THERMDA

TEST29_H
TEST29_L
C9 CPU_TEST29_H_FBCLKOUT_P
C8 CPU_TEST29_L_FBCLKOUT_N
R48 80.6/F_4
PLACE IT CLOSE TO CPU WITHIN 1"
ROUTE AS 80 Ohm DIFFERENTIAL PAIR

TEST24 AE7 CPU_TEST24_SCANCLK1
TEST23 AD7 CPU_TEST23_TSTUPD
TEST22 AE8 CPU_TEST22_SCANSHIFTEN
TEST21 AB8 CPU_TEST21_SCANEN
TEST20 AF7 CPU_TEST20_SCANCLK2
T36

TEST28_H J7 CPU_TEST28_H_PLLCHRZ_P
TEST28_L H8 CPU_TEST28_L_PLLCHRZ_N
TEST27 AF8 CPU_TEST27_SINGLECHAIN
TEST26 AE6 CPU_TEST26_BURNIN#
TEST10 K8
TEST8 K4
T28
T37

T44 CPU_RSVD_MA0_CLK3_P
T130 CPU_RSVD_MA0_CLK3_N
T43 CPU_RSVD_MA0_CLK0_P
T129 CPU_RSVD_MA0_CLK0_N
P20 RSVD0
P19 RSVD1
N20 RSVD2
N19 RSVD3

T48 CPU_RSVD_MB0_CLK3_P
T47 CPU_RSVD_MB0_CLK3_N
T45 CPU_RSVD_MB0_CLK0_P
T46 CPU_RSVD_MB0_CLK0_N
R26 RSVD4
R25 RSVD5
P22 RSVD6
R22 RSVD7

RSVD8 H16 CPU_MA_RESET#
RSVD9 B18 CPU_MB_RESET#
T41
T125
RSVD10 B3 CPU_RSVD_VIDSTRB1
RSVD11 C1 CPU_RSVD_VIDSTRB0
T119
T118
RSVD12 H6 CPU_RSVD_VDDNB_FB_P
RSVD13 G6 CPU_RSVD_VDDNB_FB_N
RSVD14 D5 CPU_RSVD_CORE_TYPE
T25
T27
T32
RSVD15 B24
RSVD16 V18
RSVD17 B23
RSVD18 AA8
RSVD19 U18
RSVD20 D19

MISC

AMD NPT S1 SOCKET Processor Socket

VID5 A5 H_VID5 (27)
VID4 C6 H_VID4 (27)
VID3 A6 H_VID3 (27)
VID2 A4 H_VID2 (27)
VID1 C5 H_VID1 (27)
VID0 B5 H_VID0 (27)

CPU_PRESENT_L
AC6 CPU_PRESENT#
PSI_L
A3 PSI# (27)

PSI_L is a Power Status Indicator signal. This signal is asserted when the processor is in a low powerstate. PSI_L should be connected to the power supply controller, if the controller supports "skipmode, or diode emulation mode". PSI_L is asserted by the processor during the C3 and S1 states.

CPU Thermal monitor(THM)

+3V
C410 0.1u/10V_4
H_THERMDA
C407 2200p/50V_4
H_THERMDC

(24) 2ND_MBCLK
(24) 2ND_MBDATA
U12
SCLK VCC
SDA DXP
ALERT# DXN
OVERT# GND
G781P8
ADDRESS: 98H

+3V
R266 *8.2K_4
B-test
R269 *10K_4
(14) THERM_ALERT#
*2N7002E-LF
Q26
THERM_ALERT#_R
+3V
R268 10K_4
THER_OVERT#

<check list>
Layout Note:Routing 10:10 mils and away from noise source with ground gard

CPU FAN(THM)

+3V
R221 10K_4
(24) FANSIG
B-test
+5V
R220 *Short_6
TH_FAN_POWER
C354 *0.01u/16V_4
CN10
FAN CONN
B-test
Update footprint

+3V
R230 10K_4
FAN_PWM_E
+3V
R223 10K_4
+5V
R224 10K_4
THER_OVERT#
R228 10K_4
THER_OVERT#_B
Q18 MMBT3904
Q17 MMBT3904
FAN_PWM_CN
(24) CPUFAN#
R235 *Short_4
FAN_PWM_EC
C-test

+1.8VSUS +3V
FD1 *HDT@BAS316
R44 *2.2K_4
R47 *HDT@2K/F_4
CPU_HT_RESET#
Q4 *HDT@FDV301N
CPU to HDT RESET#

+1.8VSUS +1.8VSUS +3V
C-test
R43 300_4
R41 *10K_4
R40 *4.7K_4
H_PROCHOT#
Q3 *MMBT3904
AMD_PROCHOT (13,24)

+1.8VSUS
IF no use which Net need pull-up or down
HDT CONNECTOR
R65 *220_4
R62 *220_4
R61 *220_4
R60 *220_4
R59 220_4
CPU_DBREQ#
CPU_DBRDY
CPU_TCK
CPU_TMS
CPU_TDI
CPU_TRST#
CPU_TDO
C126 *0.1u/10V_4
CPU to HDT RESET#
KEY
CN5 *HDT CONN
NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.

Power name	Description	Voltage
VDDA	Filtered PLL supply voltage	2.5V

Quanta Computer Inc.
PROJECT : ZA8

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	TURION 64 CTRL & DEBUG	1A

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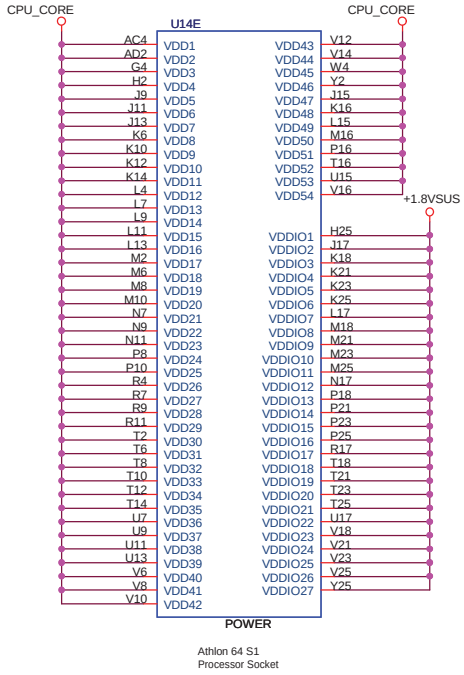
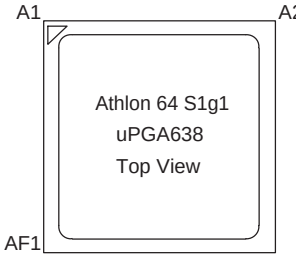
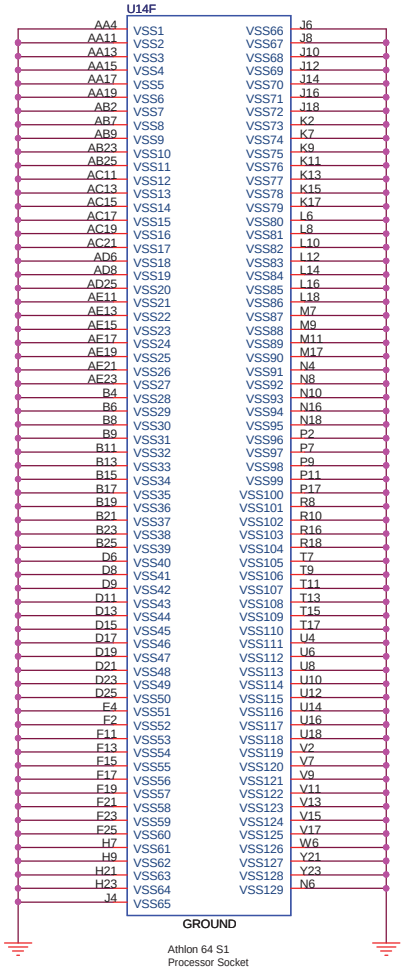
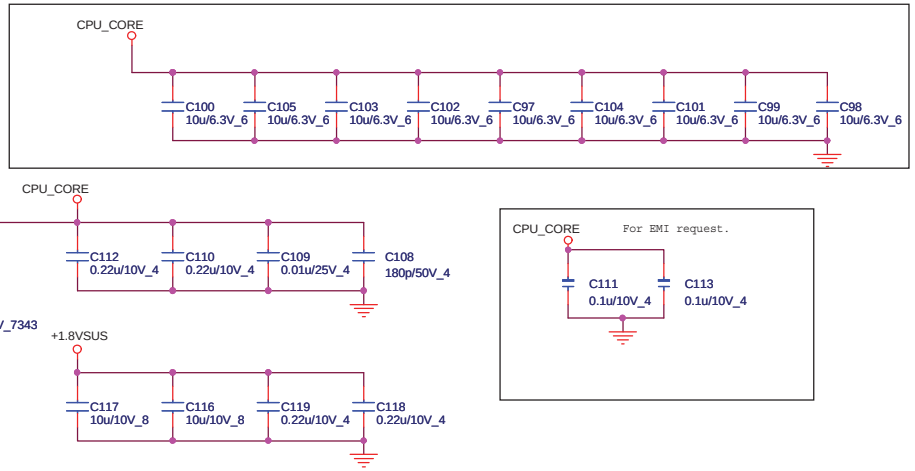
PROCESSOR POWER AND GROUND(CPU)



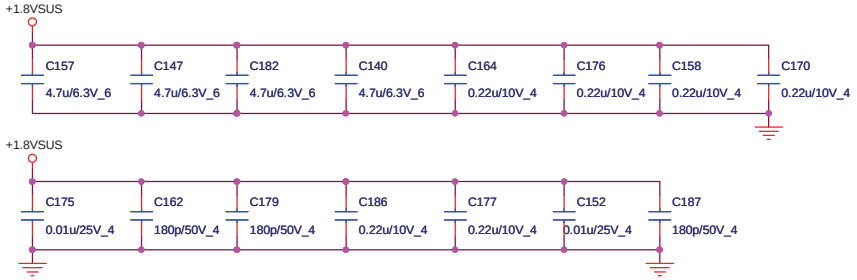




BOTTOMSIDE DECOUPLING



DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE



Power name	Description	Voltage
VDD	Core power supply	1.05V
VDDIO	DDR SDRAM I/O ring power supply	1.8V

Quanta Computer Inc.

PROJECT : ZA8

Size	Document Number	Rev
	TURION 64 PWR & GND	1A

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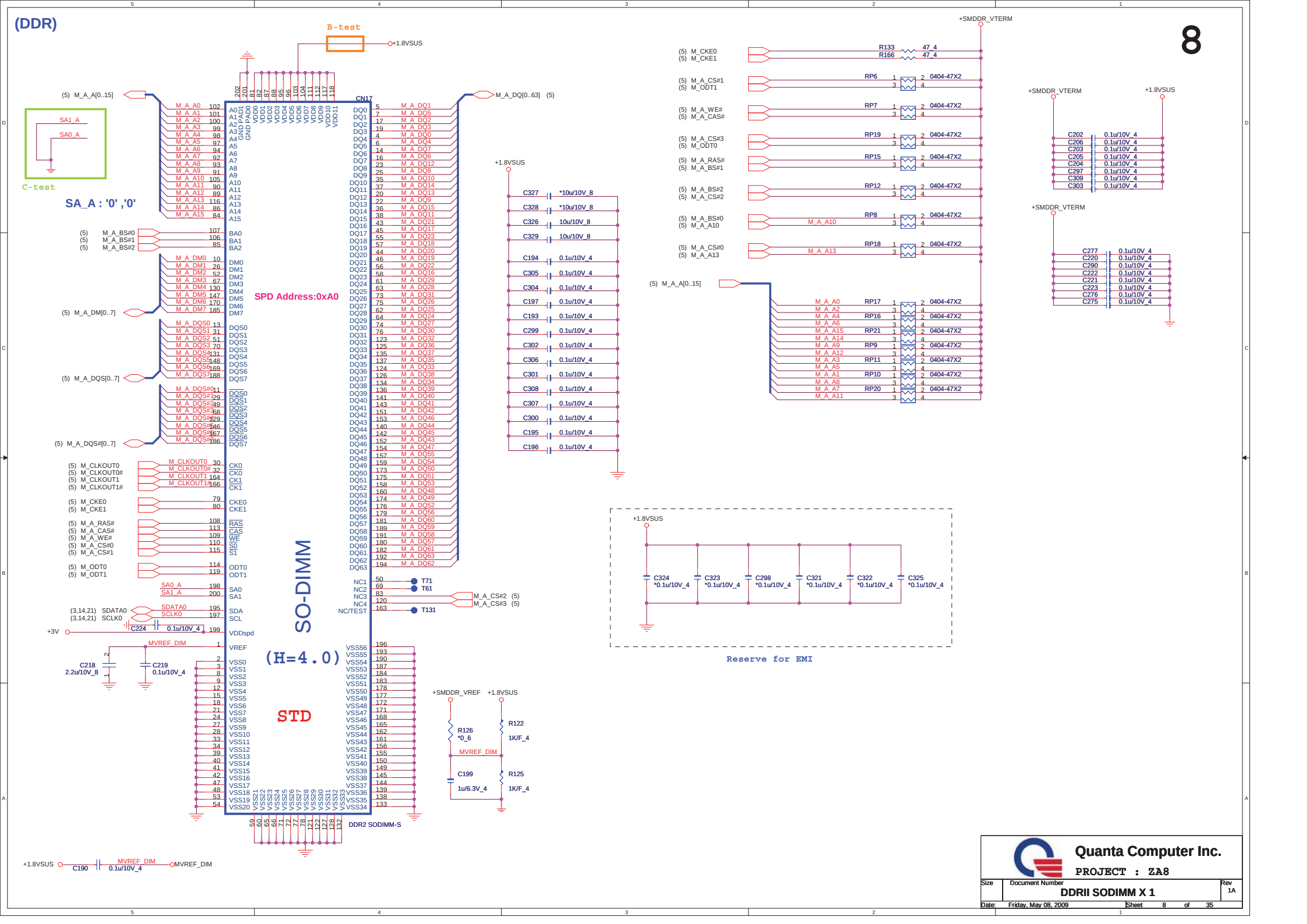
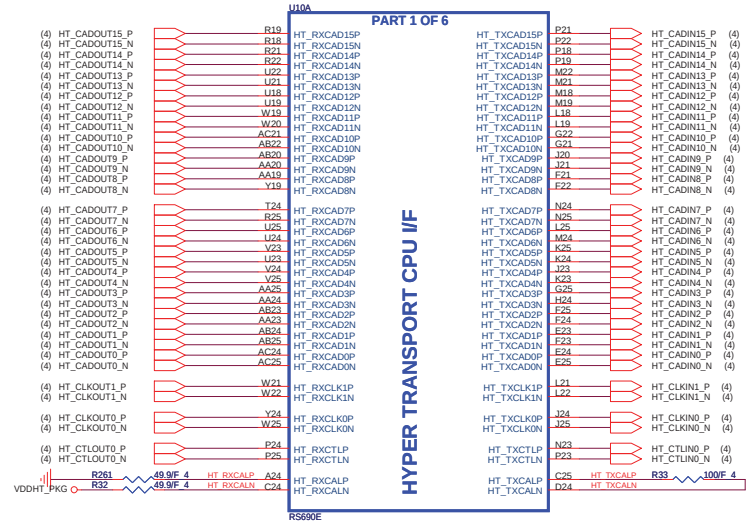

(DDR)
8
B-test
+1.8VSUS
C-test
SA1_A
SA0_A
SA_A : '0' ,'0'
CN17
SO-DIMM
(H=4.0)
STD
SPD Address:0xA0
DDR2 SODIMM-S
(5) M_A_A[0..15]
(5) M_A_DM[0..7]
(5) M_A_DQS[0..7]
(5) M_A_DQS#[0..7]
M_A_DQ[0..63] (5)
(5) M_A_BS#0
(5) M_A_BS#1
(5) M_A_BS#2
(5) M_CLKOUT0
(5) M_CLKOUT0#
(5) M_CLKOUT1
(5) M_CLKOUT1#
(5) M_CKE0
(5) M_CKE1
(5) M_A_RAS#
(5) M_A_CAS#
(5) M_A_WE#
(5) M_A_CS#0
(5) M_A_CS#1
(5) M_ODT0
(5) M_ODT1
SA0_A
SA1_A
(3,14,21) SDATA0
(3,14,21) SCLK0
SDATA0
SCLK0
+3V
C224 0.1u/10V_4
MVREF_DIM
C218 2.2u/10V_8
C219 0.1u/10V_4
+1.8VSUS
C190 0.1u/10V_4
MVREF_DIM
+SMDDR_VREF
+1.8VSUS
R126 *0_6
R122 1K/F_4
MVREF_DIM
C199 1u/6.3V_4
R125 1K/F_4
NC1 T71
NC2 T61
NC3 M_A_CS#2 (5)
NC4 M_A_CS#3 (5)
NC/TEST T131
+1.8VSUS
C327 *10u/10V_8
C328 *10u/10V_8
C326 10u/10V_8
C329 10u/10V_8
C194 0.1u/10V_4
C305 0.1u/10V_4
C304 0.1u/10V_4
C197 0.1u/10V_4
C193 0.1u/10V_4
C299 0.1u/10V_4
C302 0.1u/10V_4
C306 0.1u/10V_4
C301 0.1u/10V_4
C308 0.1u/10V_4
C307 0.1u/10V_4
C300 0.1u/10V_4
C195 0.1u/10V_4
C196 0.1u/10V_4
+1.8VSUS
C324 *0.1u/10V_4
C323 *0.1u/10V_4
C298 *0.1u/10V_4
C321 *0.1u/10V_4
C322 *0.1u/10V_4
C325 *0.1u/10V_4
Reserve for EMI
+SMDDR_VTERM
(5) M_CKE0
(5) M_CKE1
R133 47_4
R166 47_4
(5) M_A_CS#1
(5) M_ODT1
RP6 0404-47X2
(5) M_A_WE#
(5) M_A_CAS#
RP7 0404-47X2
(5) M_A_CS#3
(5) M_ODT0
RP19 0404-47X2
(5) M_A_RAS#
(5) M_A_BS#1
RP15 0404-47X2
(5) M_A_BS#2
(5) M_A_CS#2
RP12 0404-47X2
(5) M_A_BS#0
(5) M_A_A10
RP8 0404-47X2
M_A_A10
(5) M_A_CS#0
(5) M_A_A13
RP18 0404-47X2
M_A_A13
(5) M_A_A[0..15]
RP17 0404-47X2
RP16 0404-47X2
RP21 0404-47X2
RP9 0404-47X2
RP11 0404-47X2
RP10 0404-47X2
RP20 0404-47X2
+SMDDR_VTERM
+1.8VSUS
C202 0.1u/10V_4
C206 0.1u/10V_4
C203 0.1u/10V_4
C205 0.1u/10V_4
C204 0.1u/10V_4
C297 0.1u/10V_4
C309 0.1u/10V_4
C303 0.1u/10V_4
+SMDDR_VTERM
C277 0.1u/10V_4
C220 0.1u/10V_4
C290 0.1u/10V_4
C222 0.1u/10V_4
C221 0.1u/10V_4
C223 0.1u/10V_4
C276 0.1u/10V_4
C275 0.1u/10V_4
Quanta Computer Inc.
PROJECT : ZA8
Size
Document Number
DDRII SODIMM X 1
Rev 1A
Date: Friday, May 08, 2009
Sheet 8 of 35

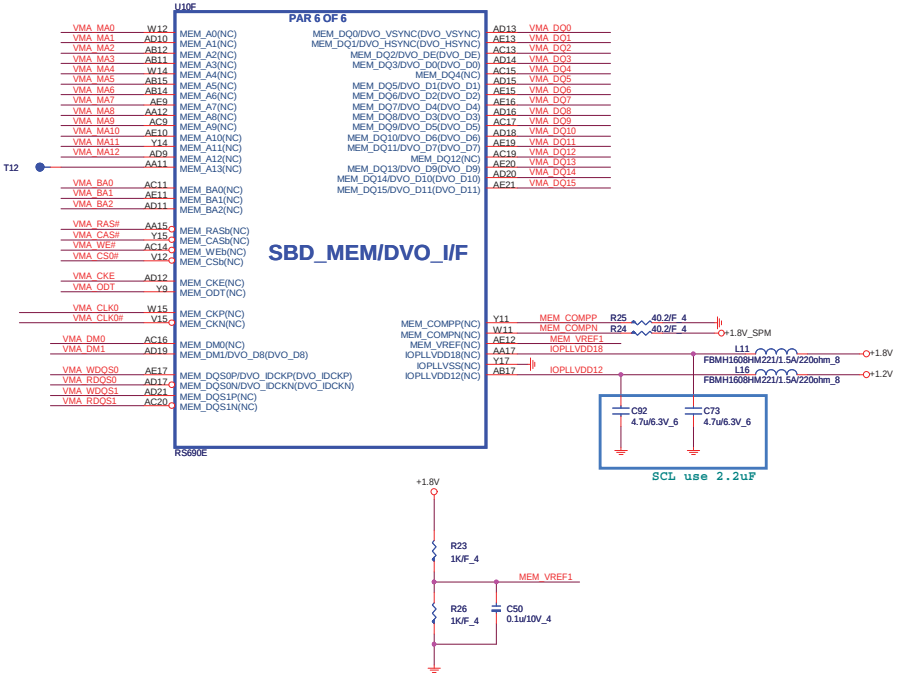
(CLG)

Power rail (RS690)	Measured value	CRB spec
+NB_CORE	3A	2.5A
+1.2V	0.6A	0.7A
+1.8V	0.07A	0.05A
+3.3V	0.13A	0.3A



(CLG)

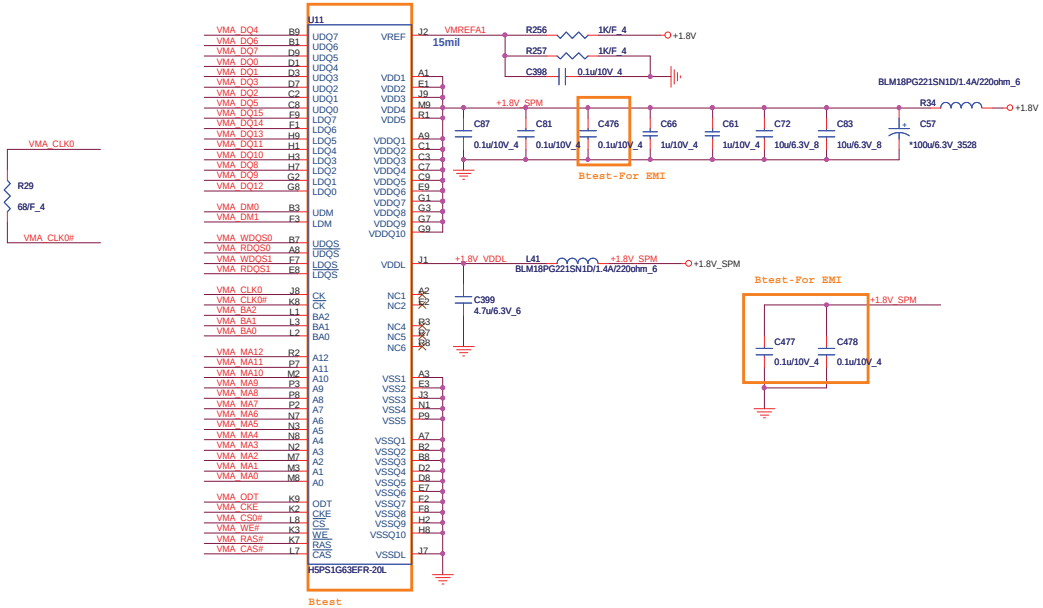
DESIGN NOTE:THE FOLLOWING DEBUG POINTS SHOULD BE PROVIDED.



Power name	Description	Voltage
IOPLLVDD18	1.2V power for memory I/O PLLs	1.8V
IOPLLVDD12	1.8V power for memory I/O PLLs	1.2V

SPM(CLG)

Hynix 64MB	AKD5FG-TW03	IC SDRAM(84P) H5PS5162FFR-25C(FBGA)
Samsung 64MB	AKD5FG-T501	IC SDRAM(84P) K4N51163QG-HC25(FBGA)
Hynix 128MB	AKD5LG-TW02	IC SDRAM(84P) H5PS1G63EFR-20L(FBGA)STNBS
Samsung 128MB	AKD5LG-T510	IC SDRAM(84P)K4N1G164QE-HC20(FBGA)STNBSQ



Power name	Description	Voltage
IOPLLVDD18	1.2V power for memory I/O PLLs	1.8V
IOPLLVDD12	1.8V power for memory I/O PLLs	1.2V

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Size	Document Number	Rev
	RS690E HT LINK I/F	1A

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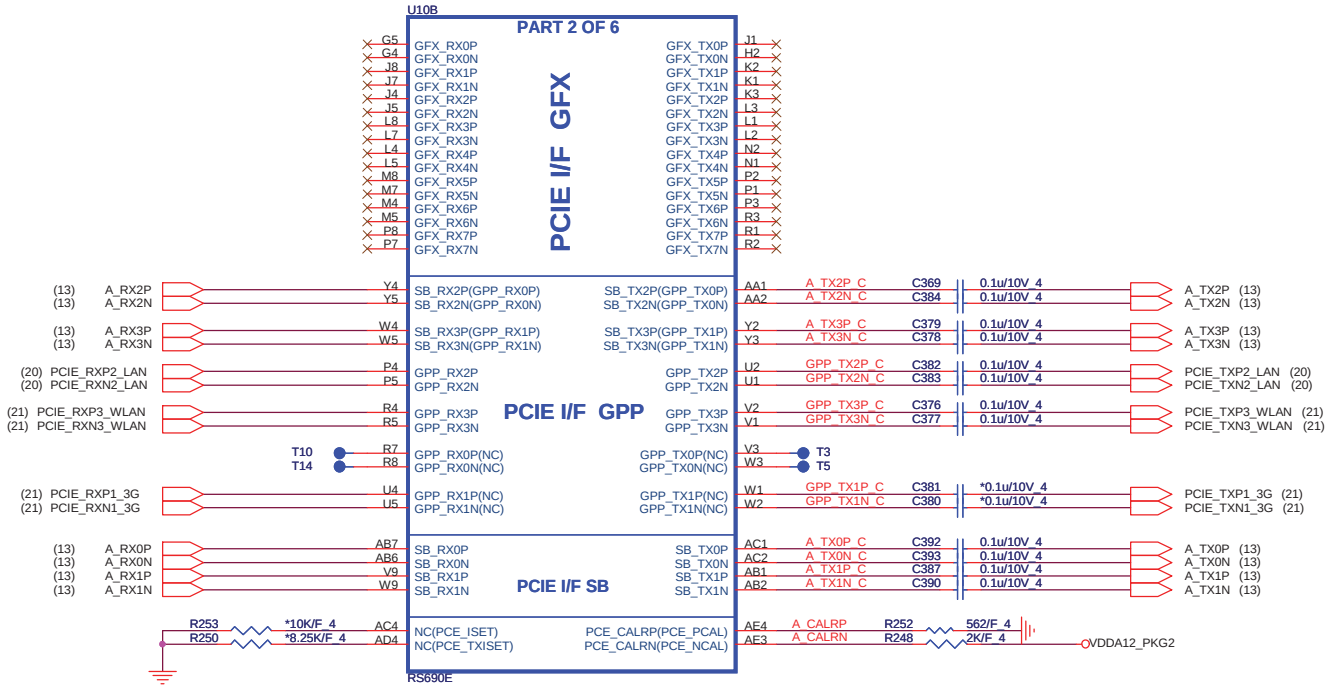
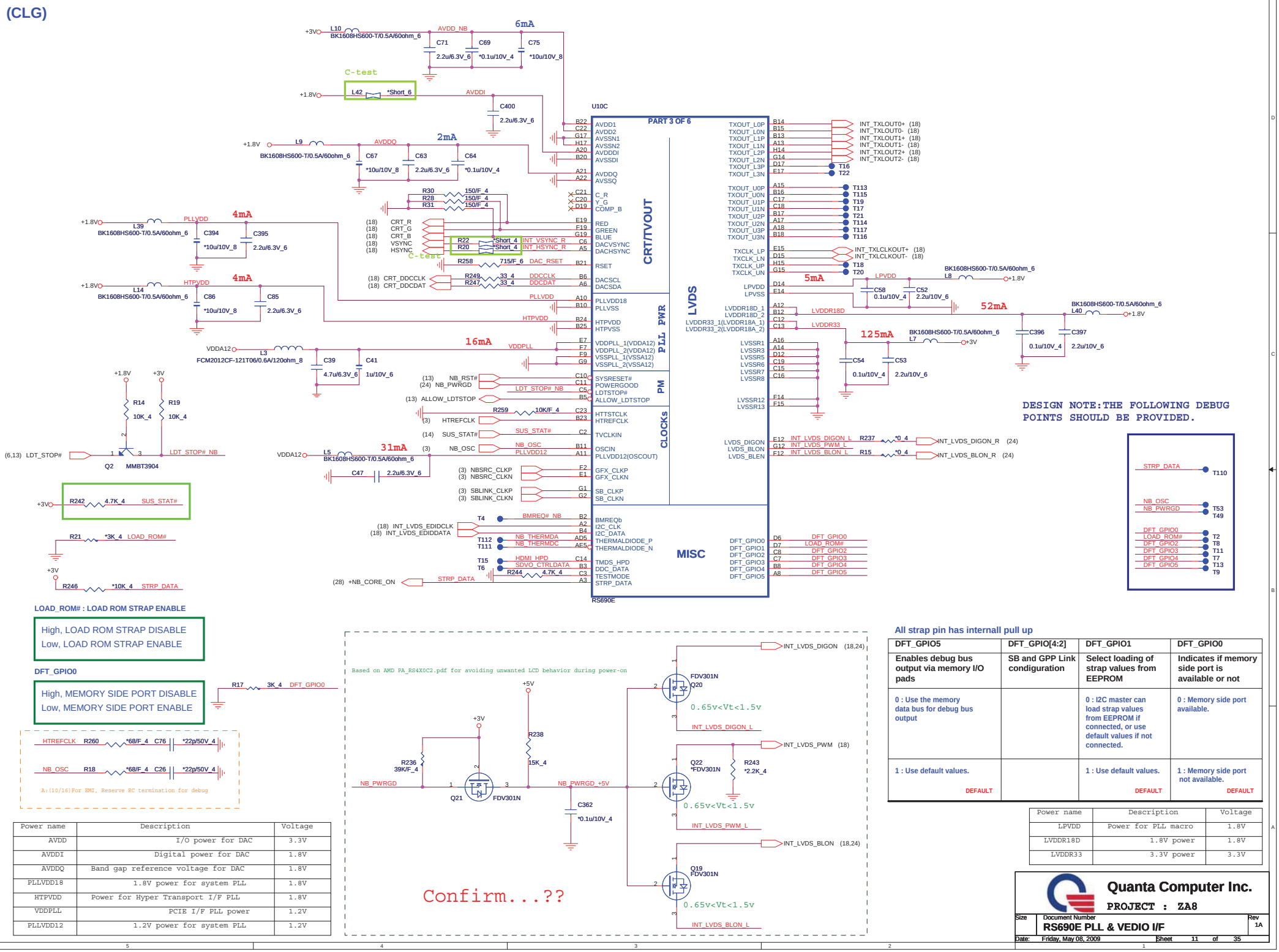
(CLG)

PCIE-->Single-Channel DVI/HDMI	
RS690/RS600	DVI/HDMI Connector
Signal	**Pin Name**
GFX_TX0P	Data2+
GFX_TX0P	Data2-
GFX_TX1P	Data1+
GFX_TX1P	Data1-
GFX_TX2P	Data0+
GFX_TX2P	Data0-
GFX_TX3P	Clock+
GFX_TX3P	Clock-

Follow AMD check list, use X7R for all caps in this page



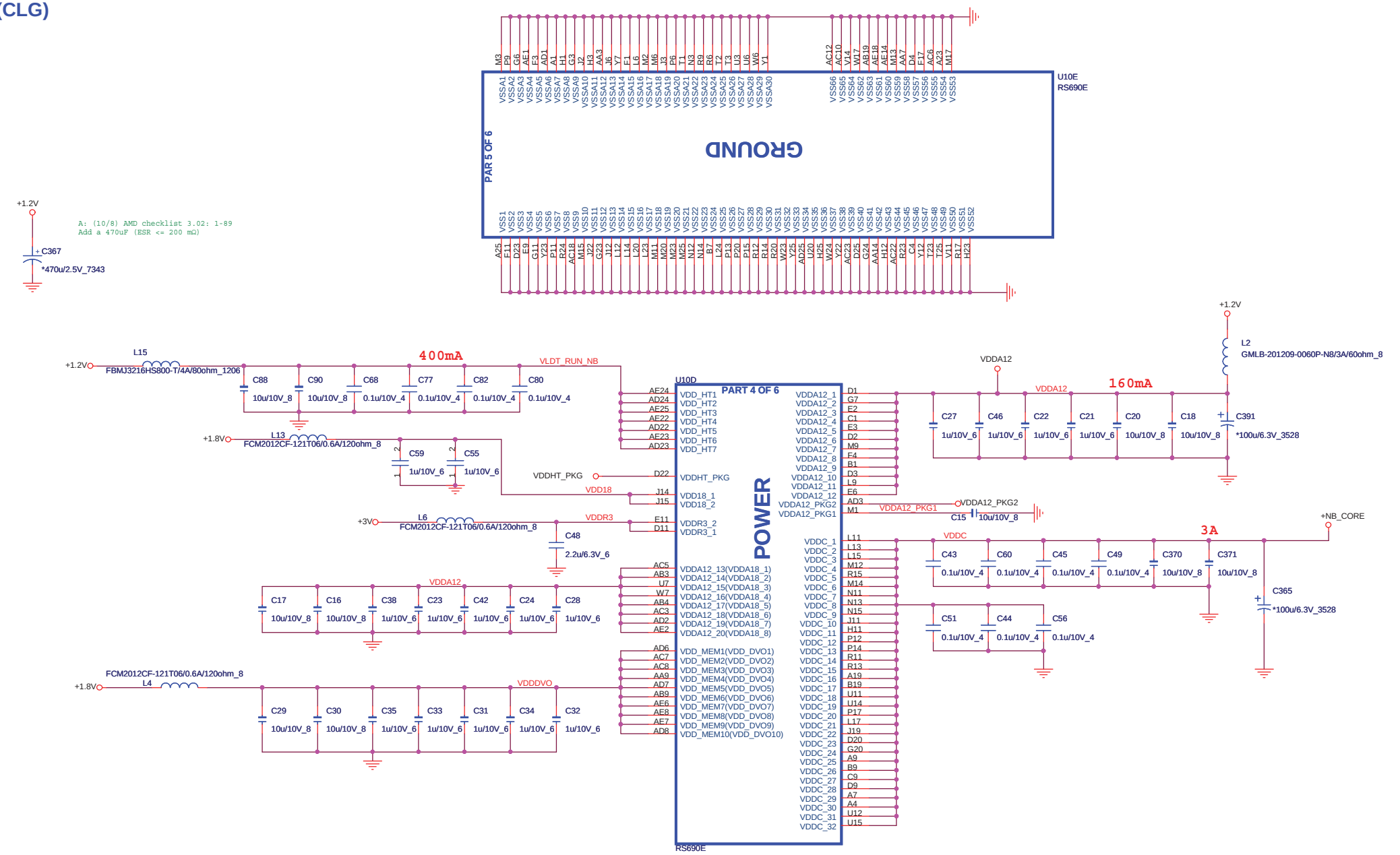
Quanta Computer Inc.			
PROJECT : ZA8			
Size	Document Number		Rev
	RS690E PCIE LINK I/F		1A
Date: Friday, May 08, 2009		Sheet 10 of 35	



Power name	Description	Voltage
AVDD	I/O power for DAC	3.3V
AVDDI	Digital power for DAC	1.8V
AVDDQ	Band gap reference voltage for DAC	1.8V
PLLVDD18	1.8V power for system PLL	1.8V
HTPVDD	Power for Hyper Transport I/F PLL	1.8V
VDDPLL	PCIE I/F PLL power	1.2V
PLLVDD12	1.2V power for system PLL	1.2V

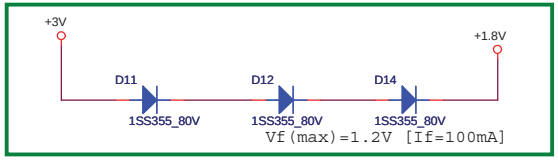
Power name	Description	Voltage
LPVDD	Power for PLL macro	1.8V
LVDDR18D	1.8V power	1.8V
LVDDR33	3.3V power	3.3V

(CLG)



Power name	Description	Voltage
VDD_HT	I/O power for Hyper Transport I/F	1.2V
VDD18	Core transform power for GPIO and power for DFT_GPIO	1.8V
VDDR3	3.3V I/O power	3.3V
VDDA12	PCIE I/F main I/O power	1.2V
VDD_MEM	I/O power for DDR memory/DVO and debug I/O	1.8V

Un-Stuff D11, D12 and D14 at no-3G sku.



Power name	Description	Voltage
VDDA12	PCIE I/F main I/O power	1.2V
VDD_CORE	ASIC core power	1.0~1.2V

Quanta Computer Inc.

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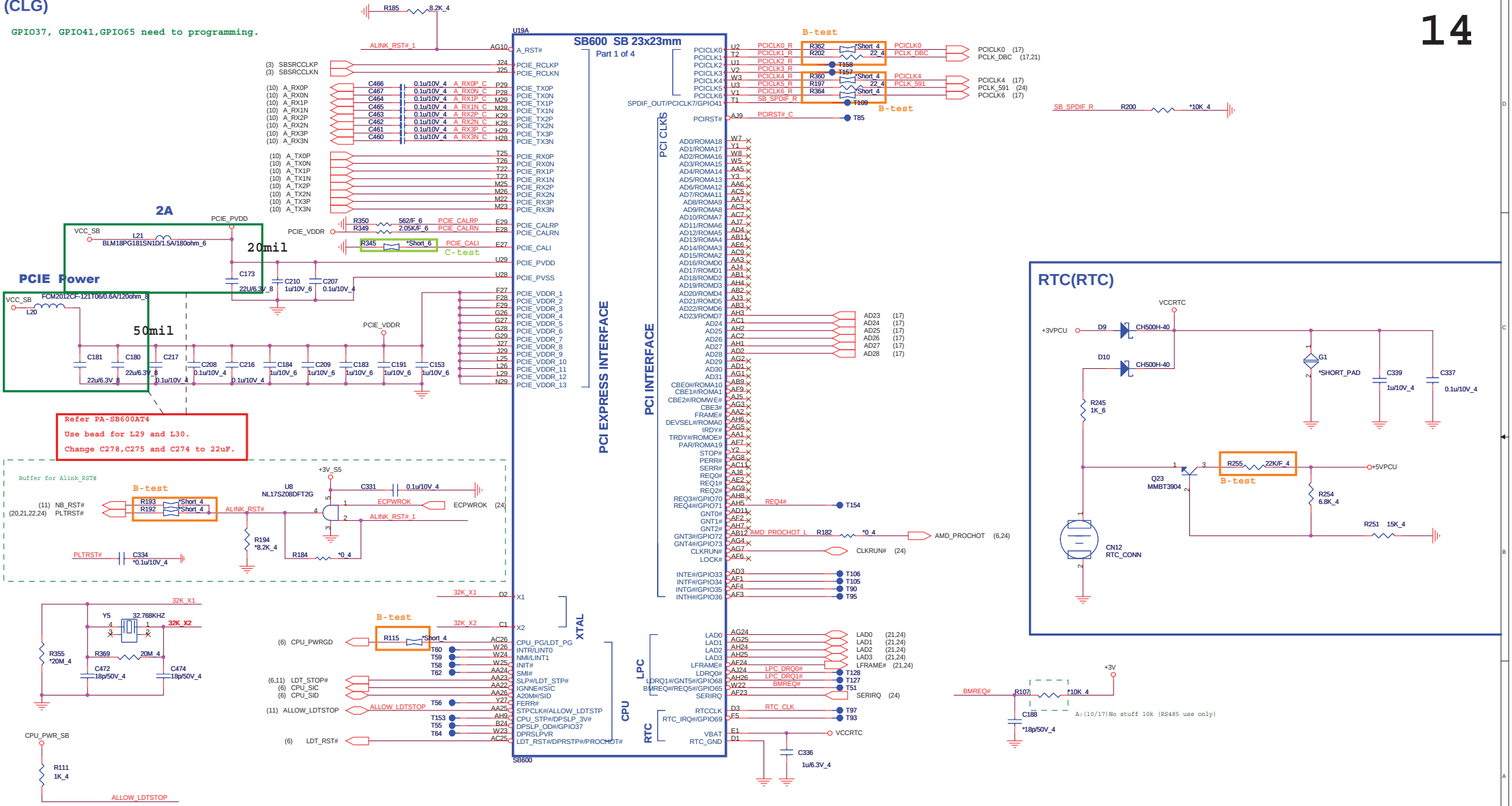
Size	Document Number	Rev
	RS690E POWER	1A
Date: Friday, May 08, 2009	Sheet 12 of 35	

(CLG)

GPIO37, GPIO41,GPIO65 need to programming.



Power name	Description	Voltage
PCIE_PVDD	A-Link Express II PLL Power	1.2V
PCIE_VDDR	A-Link Express II Analog Power	1.2V

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PROJECT : ZA8

Size	Document Number	Rev
	SB600 PCIE/PCI/CPU/LPC	1A

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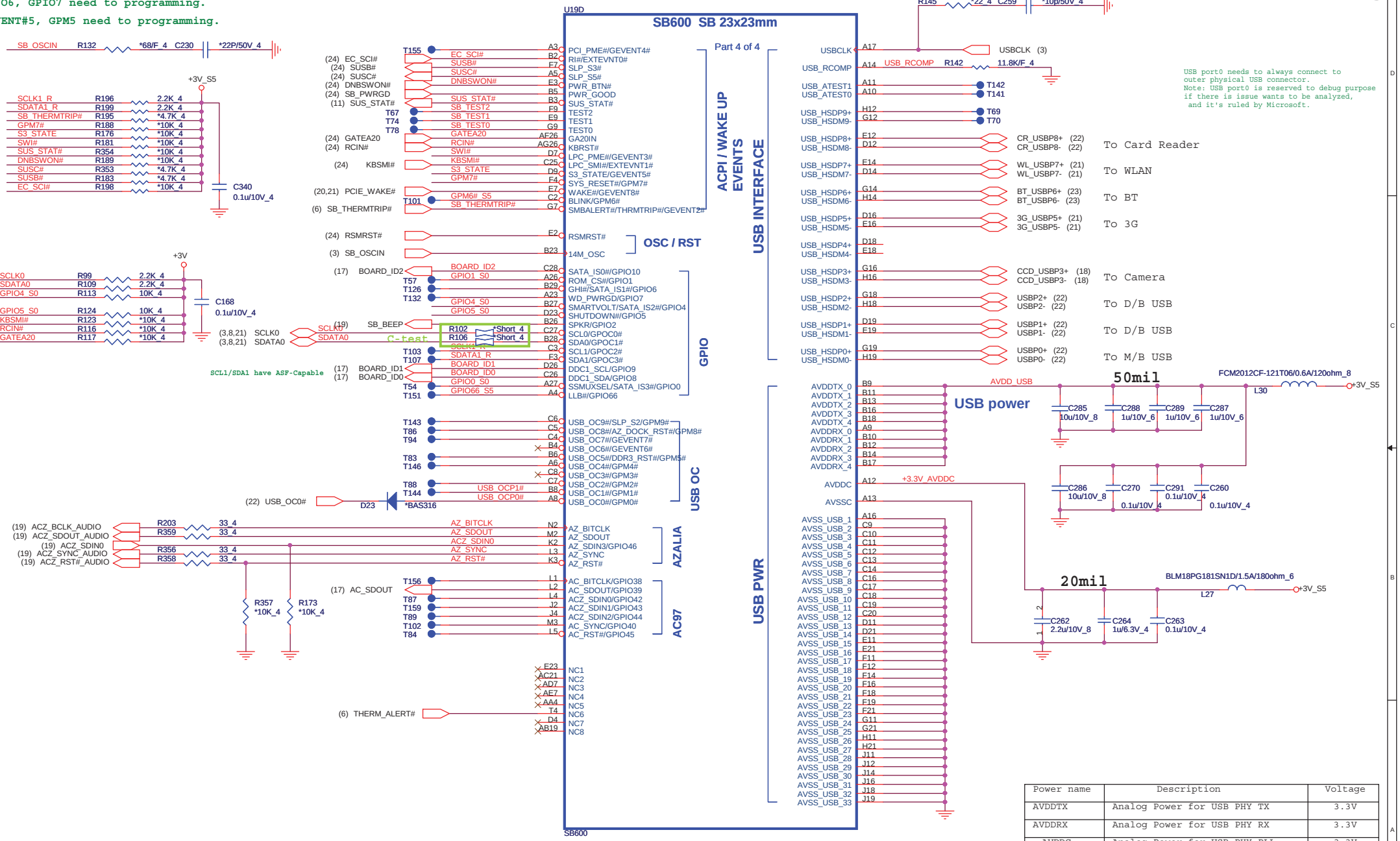
(CLG)

GPM7#, GPIO4, GPIO5 need to programming.

GPIO6, GPIO7 need to programming.

GEVENT#5, GPM5 need to programming.



Power name	Description	Voltage
AVDDTX	Analog Power for USB PHY TX	3.3V
AVDDRX	Analog Power for USB PHY RX	3.3V
AVDDC	Analog Power for USB PHY PLL	3.3V

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PROJECT : ZA8

Size	Document Number	Rev
	SB600 ACPI/GPIO/USB/AC97	1A
Date: Friday, May 08, 2009	Sheet 14 of 35	

GPIO[50~63] need to programming.

U19B

SB600 SB 23x23mm

Part 2 of 4

SERIAL ATA

ATA 66/100

SPI ROM

HW MONITOR

SERIAL ATA POWER

SB600

(22) SATA_TXP0 — C79 0.01u/25V_4 — SATA_TXP0_C — AH21 SATA_TX0+
(22) SATA_TXN0 — C78 0.01u/25V_4 — SATA_TXN0_C — AJ21 SATA_TX0-
(22) SATA_RXN0 — C74 0.01u/25V_4 — SATA_RXN0_C — AH20 SATA_RX0-
(22) SATA_RXP0 — C70 0.01u/25V_4 — SATA_RXP0_C — AJ20 SATA_RX0+

T139 — AH18 SATA_TX1+
T140 — AJ18 SATA_TX1-
T145 — AH17 SATA_RX1-
T147 — AJ17 SATA_RX1+
T152 — AH13 SATA_TX2+
T150 — AH14 SATA_TX2-
T148 — AH16 SATA_RX2-
T149 — AJ16 SATA_RX2+
AJ11 SATA_TX3+
AH11 SATA_TX3-
AH12 SATA_RX3-
AJ13 SATA_RX3+

R156 1K/F_4 SATA_CAL — AF12 SATA_CAL
SATA_X1 — AD16 SATA_X1
SATA_X2 — AD18 SATA_X2
(18) SATA_LED# — AC12 SATA_ACT#/GPIO67

PLLVDD_ATA — AD14 PLLVDD_SATA_1, AJ10 PLLVDD_SATA_2
XTLVDD_ATA — AC16 XTLVDD_SATA
AVDD_SATA — AE14 AVDD_SATA_1, AE16 AVDD_SATA_2, AE18 AVDD_SATA_3, AE19 AVDD_SATA_4, AF19 AVDD_SATA_5, AF21 AVDD_SATA_6, AG22 AVDD_SATA_7, AG23 AVDD_SATA_8, AH22 AVDD_SATA_9, AH23 AVDD_SATA_10, AJ12 AVDD_SATA_11, AJ14 AVDD_SATA_12, AJ19 AVDD_SATA_13, AJ22 AVDD_SATA_14, AJ23 AVDD_SATA_15

AB14 AVSS_SATA_1, AB16 AVSS_SATA_2, AB18 AVSS_SATA_3, AC14 AVSS_SATA_4, AC18 AVSS_SATA_5, AC19 AVSS_SATA_6, AD12 AVSS_SATA_7, AD19 AVSS_SATA_8, AD21 AVSS_SATA_9, AE12 AVSS_SATA_10, AE21 AVSS_SATA_11, AF11 AVSS_SATA_12, AF14 AVSS_SATA_13, AF16 AVSS_SATA_14, AF18 AVSS_SATA_15, AG11 AVSS_SATA_16, AG12 AVSS_SATA_17, AG13 AVSS_SATA_18, AG14 AVSS_SATA_19, AG16 AVSS_SATA_20, AG17 AVSS_SATA_21, AG18 AVSS_SATA_22, AG19 AVSS_SATA_23, AG20 AVSS_SATA_24, AG21 AVSS_SATA_25, AH10 AVSS_SATA_26, AH19 AVSS_SATA_27

IDE_IORDY AB29, IDE_IRQ AA28, IDE_A0 AA29, IDE_A1 AB27, IDE_A2 Y28, IDE_DACK# AB28, IDE_DRQ AC27, IDE_IOR# AC29, IDE_IOW# AC28, IDE_CS1# W28, IDE_CS3# W27
IDE_D0/GPIO15 AD28, IDE_D1/GPIO16 AD26, IDE_D2/GPIO17 AE29, IDE_D3/GPIO18 AE27, IDE_D4/GPIO19 AG29, IDE_D5/GPIO20 AH28, IDE_D6/GPIO21 AJ28, IDE_D7/GPIO22 AJ27, IDE_D8/GPIO23 AH27, IDE_D9/GPIO24 AG27, IDE_D10/GPIO25 AG28, IDE_D11/GPIO26 AF28, IDE_D12/GPIO27 AF29, IDE_D13/GPIO28 AF28, IDE_D14/GPIO29 AD25, IDE_D15/GPIO30 AD29

SPI_DI/GPIO12 J3, SPI_DO/GPIO11 J6, SPI_CLK/GPIO47 G3, SPI_HOLD#/GPIO31 G2, SPI_CS#/GPIO32 G6
LAN_RST#/GPIO13 C23, ROM_RST#/GPIO14 G5

FANOUT0/GPIO3 M4 — SB600_FOUT0 — R191 *10K_4 — T99, T96
FANOUT1/GPIO48 T3
FANOUT2/GPIO49 V4
FANIN0/GPIO50 N3 — T104
FANIN1/GPIO51 P2 — T98
FANIN2/GPIO52 W4 — T92
TEMP_COMM P5
TEMPIN0/GPIO61 P7 — T100
TEMPIN1/GPIO62 P8 — T77
TEMPIN2/GPIO63 T8 — T76
TEMPIN3/TALERT#/GPIO64 T7 — T161 — B-test
VIN0/GPIO53 V5 — T82
VIN1/GPIO54 L7 — T72
VIN2/GPIO55 M8 — T75
VIN3/GPIO56 V6 — T79
VIN4/GPIO57 M6 — T108
VIN5/GPIO58 P4 — T91
VIN6/GPIO59 M7 — T81
VIN7/GPIO60 V7 — T80

C-test — +3V — R375 *Short_6

AVDD_HWM
AVDD N1
AVSS M1
C471 *0.1u/10V_4
C473 *2.2u/6.3V_6
HWM_AGND
R374 *Short_6

Rev:C R474 and R473 change Footprint short

Check List Rev3.01(Item 1-33,1-34): C-test
HWM not implemented:
(1)Bead not used, change bead to 0 ohm(no stuff)
(2)Decoupling caps not used

B-test

C254 27p/50V_4 — Y3 25MHZ_SATA — C238 27p/50V_4
SATA_X1 — R138 10M_4 — SATA_X2

SATA Power

+3V — L29 BLM18PG181SN1D/1.5A/180ohm_6 — XTLVDD_ATA
C269 1u/10V_6
C245 1u/10V_6

VCC_SB — L32 BLM18PG181SN1D/1.5A/180ohm_6 — PLLVDD_ATA
C294 1u/10V_6
C271 1u/10V_6

VCC_SB — L31 FCM2012CF-121T06/0.6A/120ohm_8 — AVDD_SATA
C267 22u/6.3V_8
C237 1u/10V_6
C279 1u/10V_6
C253 0.1u/10V_4
C244 0.1u/10V_4
C239 0.1u/10V_4

A:(10/17)Follow AMD check list 3.02:
Change from two 10uF to one 22uF

Power name	Description	Voltage
PLLVDD_SATA	SATA PLL Power	1.2V
XTLVDD_SATA	SATA XTAL power	3.3V
AVDD_SATA	SATA Analog Power	1.2V

Power name	Description	Voltage
AVDD	HW Monitor Analog PWR	3.3V

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PROJECT : ZA8

Size	Document Number	Rev
	SB600 SATA/IDE	1A

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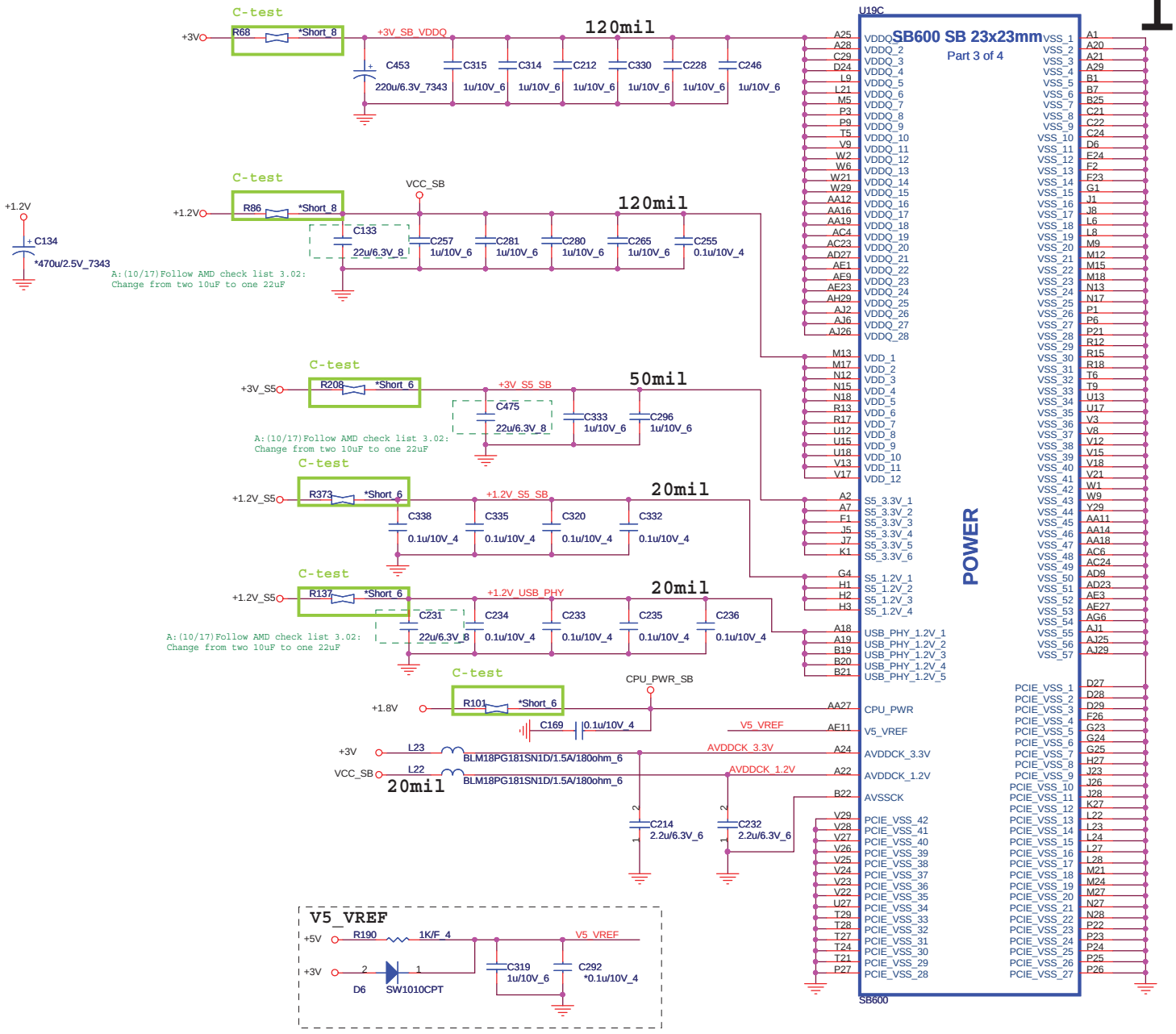

Power name	Description	Voltage
VDDQ	3.3V I/O Power	3.3V
VDD	Core Power	1.2V
S5_3.3V	3.3V S5 Power	3.3V
S5_1.2V	1.2V S5 Power	1.2V
USB_PHY_1.2V	1.2V USB PHY standby Power	1.2V
CPU_PWR	CPU I/O reference voltage	1.8V
V5_VREF	5V Reference voltage for PCI interface	5V
AVDDCK_3.3V	3.3V power for analog PLLs	3.3V
AVDDCK_1.2V	1.2V power for analog PLLs	1.2V

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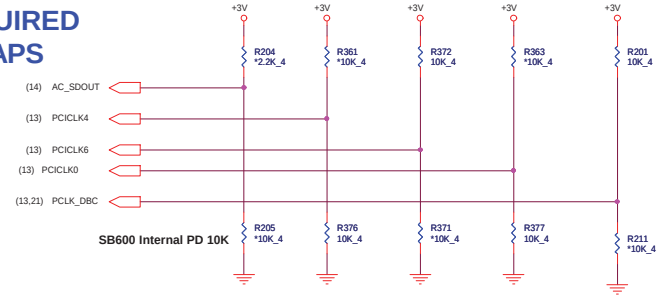
PROJECT : ZA8

Size	Document Number	Rev
	SB600 POWER/DECOUPLING	1A

Date: Friday, May 08, 2009 Sheet 16 of 35

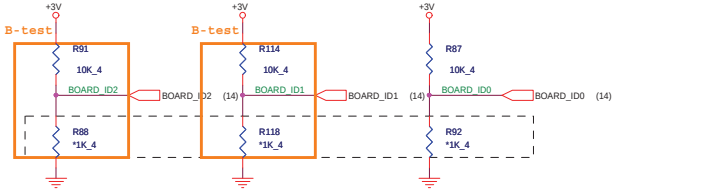
REQUIRED STRAPS



	AC_SDOUT	PCICLK4	PCICLK6	PCLK_OZ129 PCI_CLK0	PCLK_DBC PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

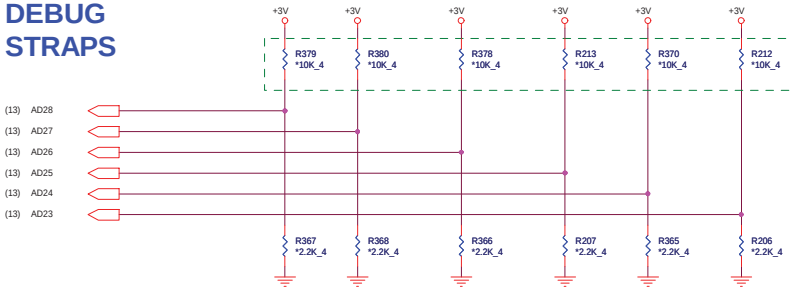
Board ID2	Board ID1	
0	0	Samsung 64MB
0	1	Samsung 128MB
1	0	Hynix 64MB
1	1	Hynix 128MB (Default)

Board ID0	
0	w/o side port
1	w side port (Default)



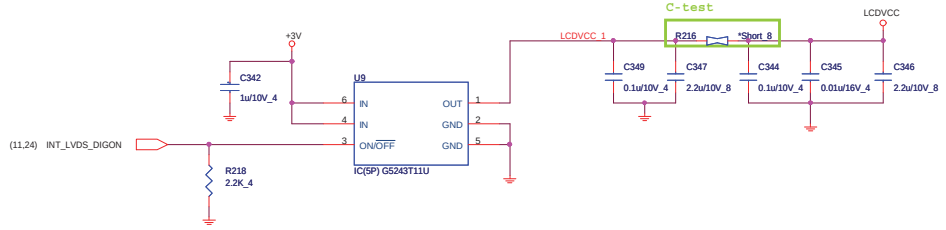
(1)Because GPIO pin of South Bridge have internal PU or PD.It will let Board ID become floating(+1.5V) when external circuit PD
(2)Change external Pull down to 1K ohm for all BOARD_ID

DEBUG STRAPS

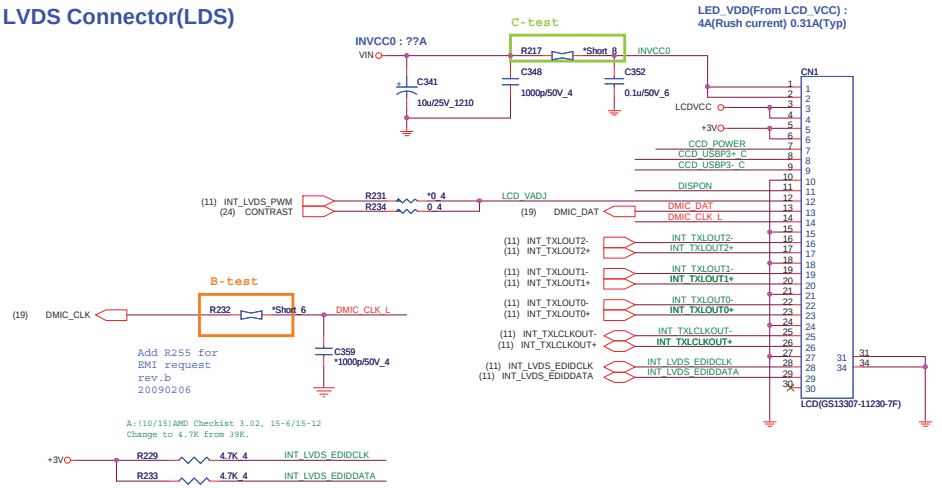


	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

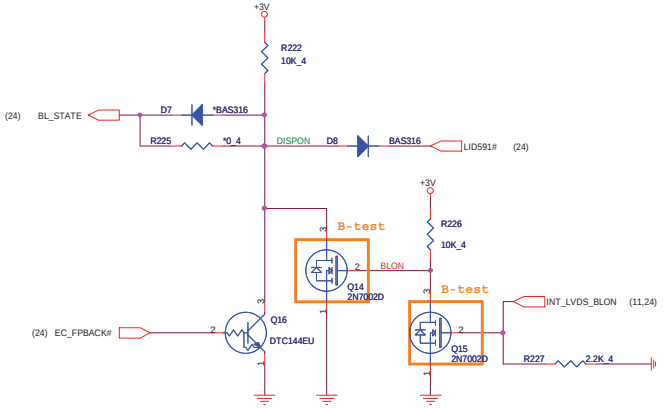
Panel Power(LDS)



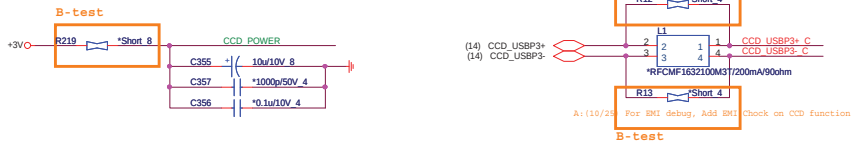
LVDS Connector(LDS)



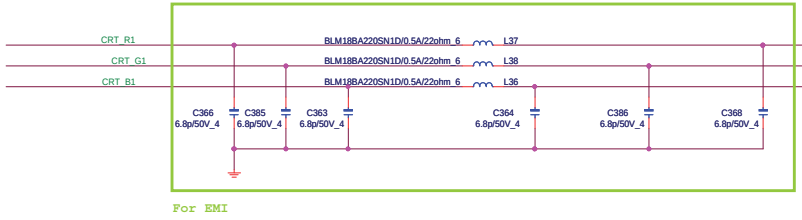
Backlight(LDS)

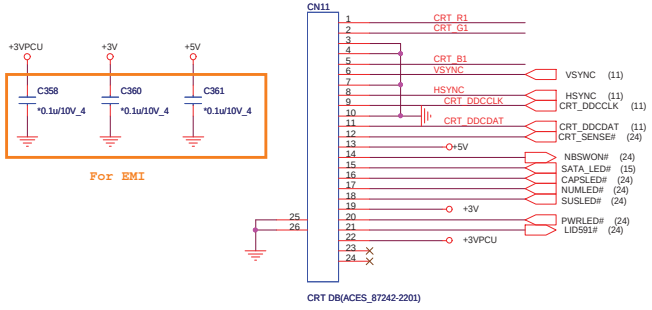


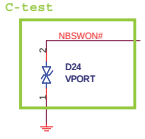
CAMERA Module (CMOS sensor)(CCD)



CRT/Hall sensor/PWR and function LED (DB)(CRT)







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PROJECT : ZA8

Size	Document Number	Rev
	LED PANEL/LID/CCD/CRT	1A
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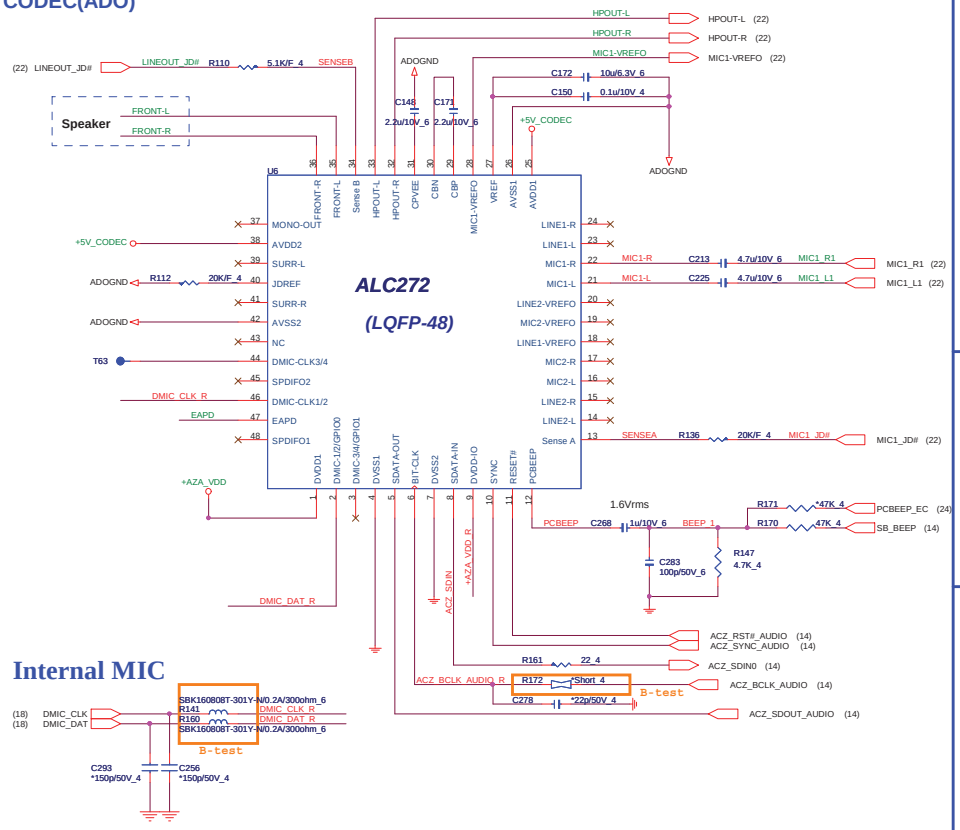
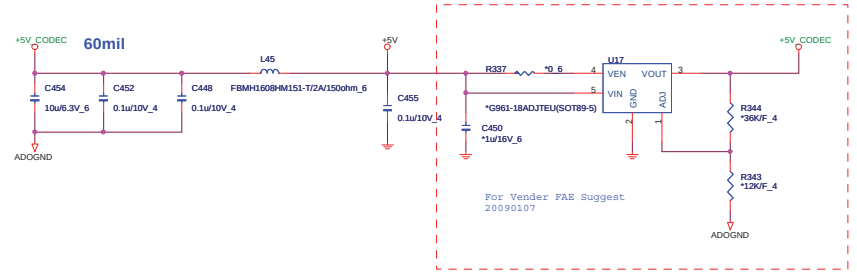
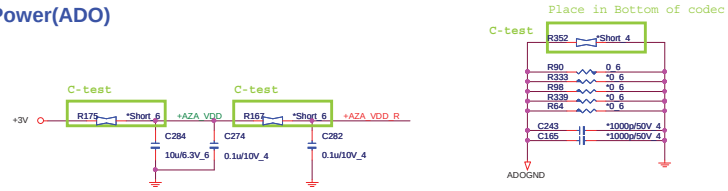
CODEC(ADO)



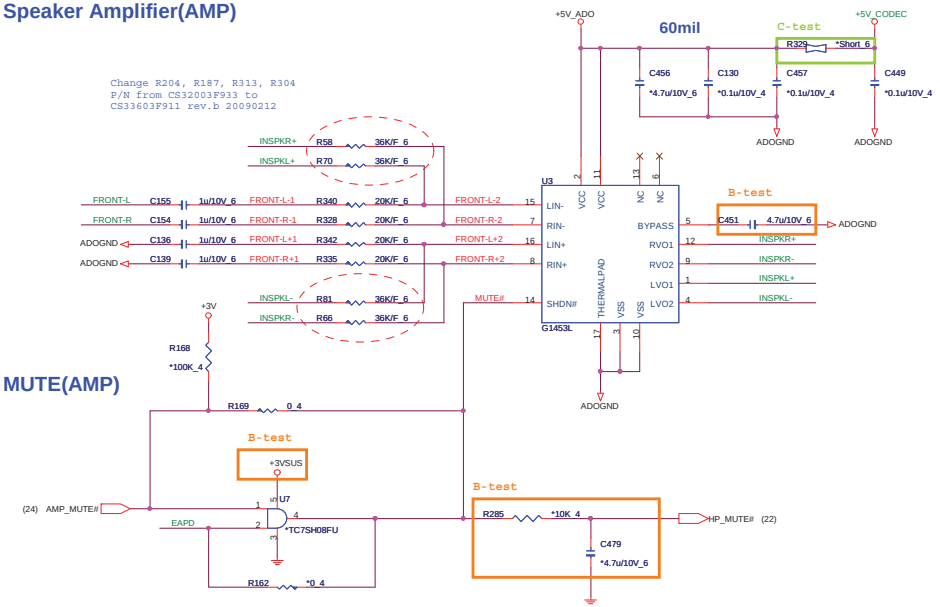
Codec Power(ADO)



HDA Power(ADO)

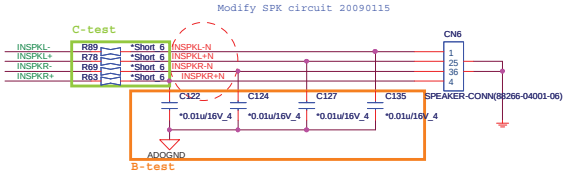


Speaker Amplifier(AMP)



MUTE(AMP)

Speaker(AMP)



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PROJECT : ZA8		
Size	Document Number: AL272/AMP/MIC/LINE-OUT	Rev: 1A
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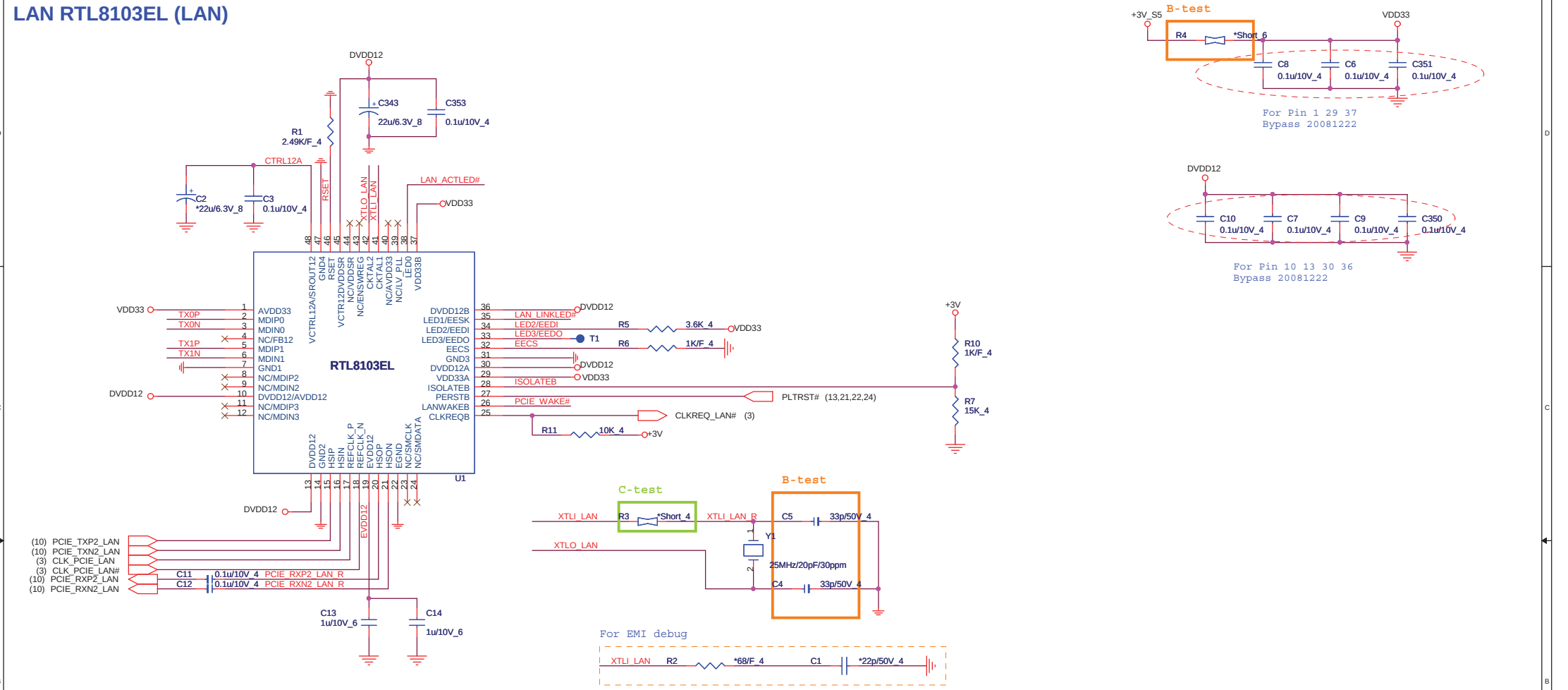
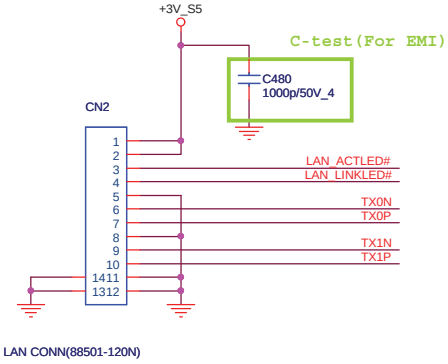
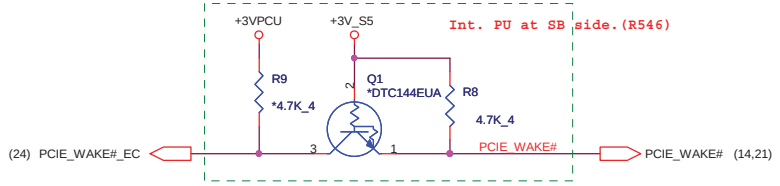
LAN RTL8103EL (LAN)



LAN D/B CONNECTER(LAN)



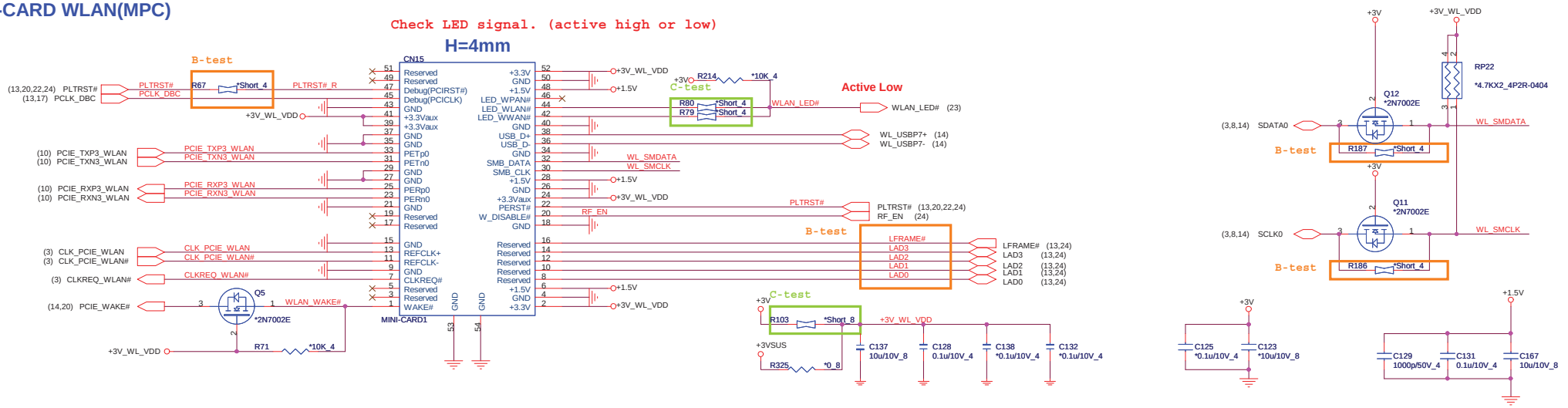


Quanta Computer Inc.

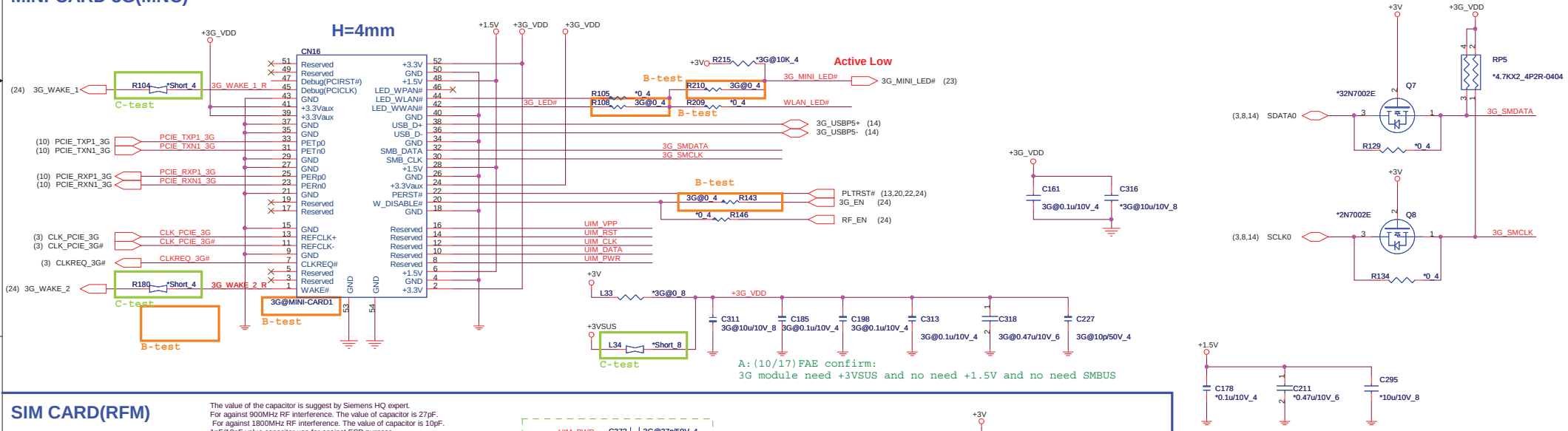
PROJECT : ZA8

Size	Document Number	Rev
	LAN RTL8103EL	1A
Date: Friday, May 08, 2009	Sheet 20 of 35	

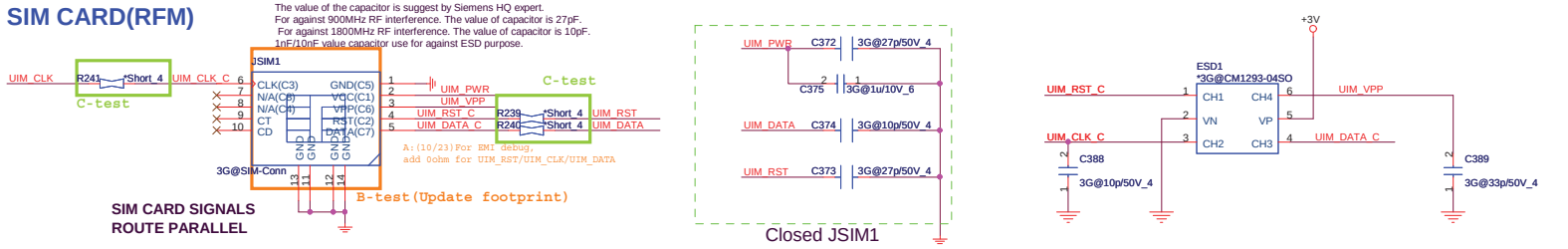
MINI-CARD WLAN(MPC)



MINI-CARD 3G(MNC)



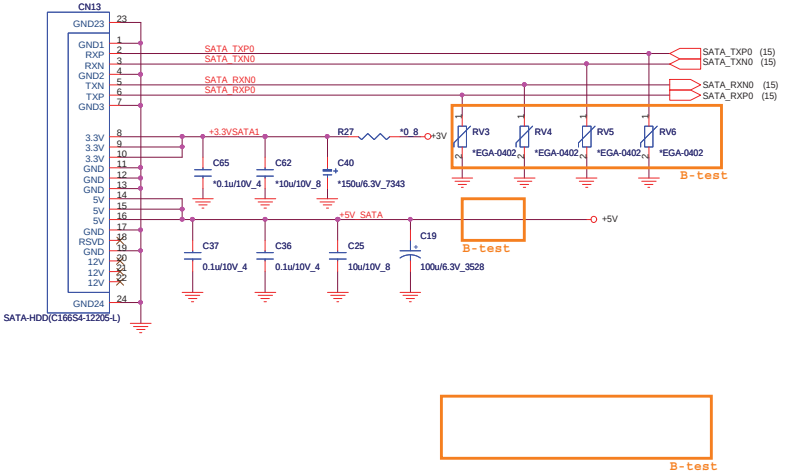
SIM CARD(RFM)



Quanta Computer Inc.		
PROJECT : ZA8		
Size	Document Number: Mini-Card/WL/3G/SIM	Rev: 1A
Date: Friday, May 08, 2009	Sheet 21 of 35	

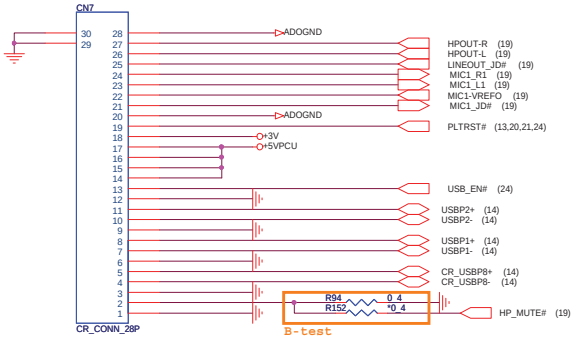
2.5" SATA HDD OR SSD(HDD)

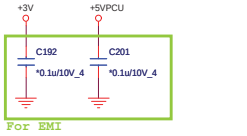
Check SATA HDD in AVL for +3V

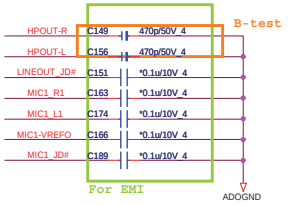


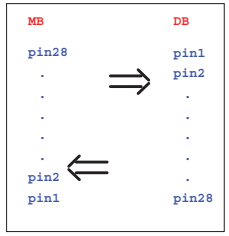
Audio, USBx2, Cardreader DB(AMP)

1pin=0.5A (ACES)



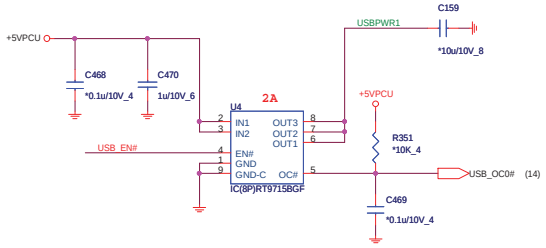




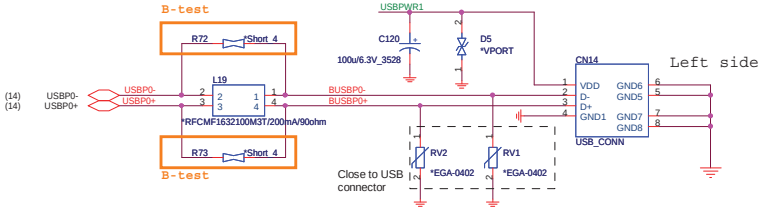


+5VPCU	USB PWR	2A	2A
+3V	Card reader Codec	250mA 25mA	275mA

(USB)



Please reserve Cin = 1uF(stuff),Cout = 10uF(don't stuff) for Richtek RT9711BPF
Please reserve Cin = 4.7uF(stuff),Cout = 10uF(don't stuff) for GMT solution



Placed common mode chokes within 1.0" of the USB connectors

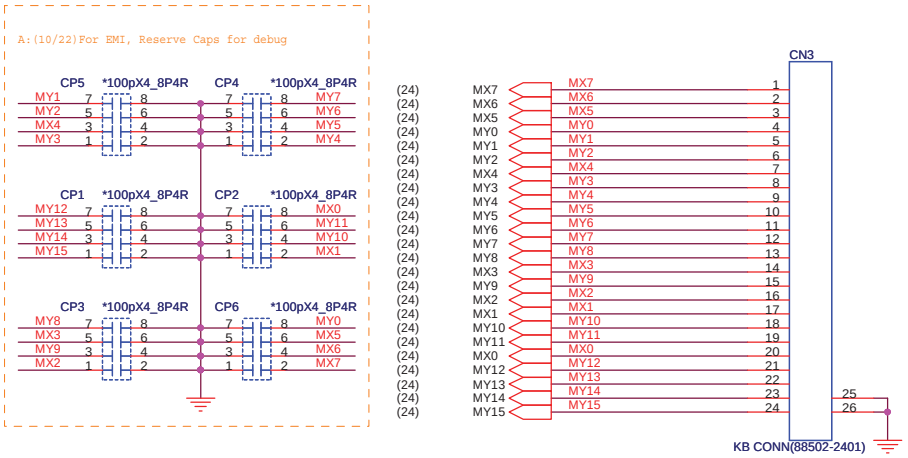
Quanta Computer Inc.

PROJECT : ZA8

Size	Document Number	Rev
	SATA HDD/ODD	1A

Date: Friday, May 08, 2009 Sheet 22 of 35

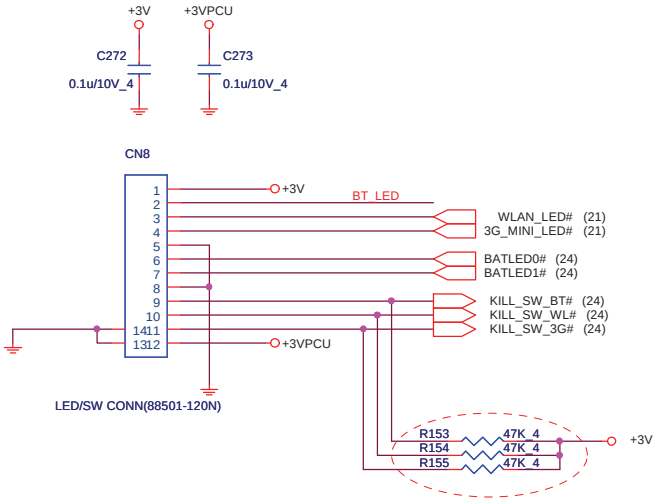
Keyboard(KBC)



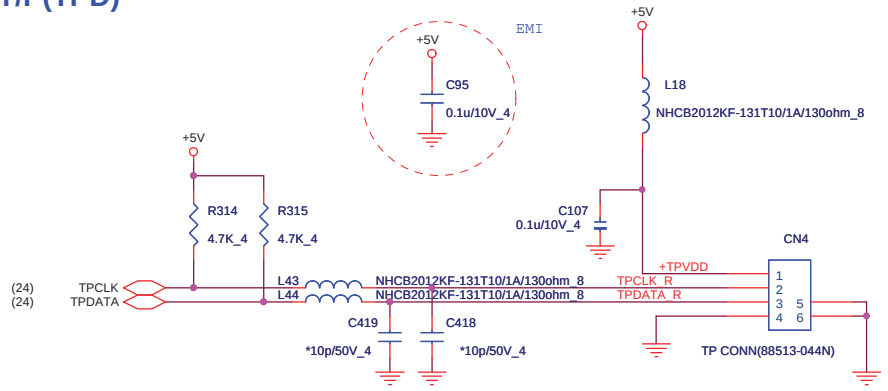
WLAN LED and SW DB(UIF)

K/B Matrix	Button
MX1/MY0	WLAN Switch
MX2/MY0	T/P Switch

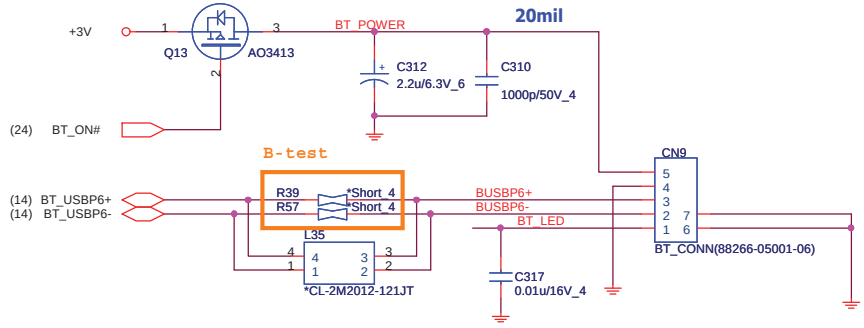
Function	LED Color
Power	Blue/Orange
BATT	Blue/Orange
HDD	Blue
Caps	Blue
Num	Blue
WLAN	Orange
T/P	Orange
3G	Green



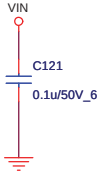
T/P(TPD)



BT(BTM)



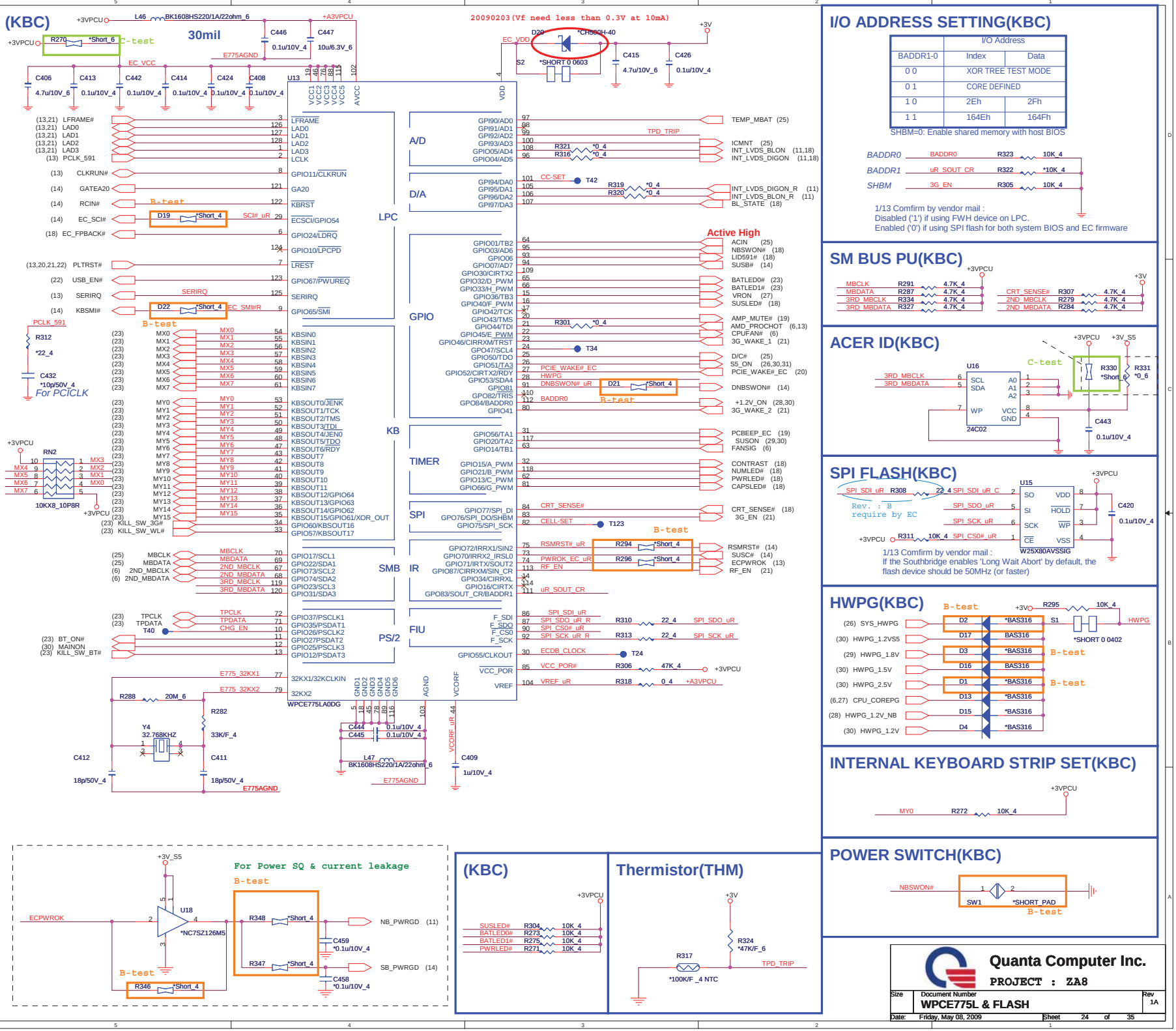
EMI



Quanta Computer Inc.

PROJECT : ZA8

Size	Document Number	Rev
	PB/ TP/ USB/ KB	1A
Date: Friday, May 08, 2009	Sheet 23 of 35	



I/O ADDRESS SETTING(KBC)

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

BADDR0 — BADDR0 — R323 — 10K_4

BADDR1 — uR_SOUT_CR — R322 — *10K_4

SHBM — 3G_EN — R305 — 10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU(KBC)

+3VPCU

MBCLK — R291 — 4.7K_4
MBDATA — R287 — 4.7K_4
3RD_MBCLK — R334 — 4.7K_4
3RD_MBDATA — R327 — 4.7K_4

+3V

CRT_SENSE# — R307 — 4.7K_4
2ND_MBCLK — R279 — 4.7K_4
2ND_MBDATA — R284 — 4.7K_4

ACER ID(KBC)

+3VPCU, +3V_S5

U16 (24C02)
SCL, SDA, A0, A1, A2, WP, VCC, GND

3RD_MBCLK
3RD_MBDATA

C-test
R330 *Short_6
R331 *0_6

C443 0.1u/10V_4

SPI FLASH(KBC)

SPI_SDI_uR — R308 — 22_4 — SPI_SDI_uR_C

Rev. : B require by EC

SPI_SDO_uR
SPI_SCK_uR
SPI_CS0#_uR — R311 — 10K_4

U15 (W25X80AVSSIG)
SO, SI, SCK, CE, VDD, HOLD, WP, VSS

+3VPCU

C420 0.1u/10V_4

1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

HWPG(KBC)

B-test

+3V — R295 — 10K_4 — S1 — HWPG

*SHORT 0 0402

(26) SYS_HWPG	D2	*BAS316
(30) HWPG_1.2VS5	D17	BAS316
(29) HWPG_1.8V	D3	*BAS316
(30) HWPG_1.5V	D16	BAS316
(30) HWPG_2.5V	D1	*BAS316
(6,27) CPU_COREPG	D13	*BAS316
(28) HWPG_1.2V_NB	D15	*BAS316
(30) HWPG_1.2V	D4	*BAS316

INTERNAL KEYBOARD STRIP SET(KBC)

+3VPCU

MY0 — R272 — 10K_4

POWER SWITCH(KBC)

NBSWON# — SW1 — *SHORT_PAD

B-test

(KBC)

+3VPCU

SUSLED# — R304 — 10K_4
BATLED0# — R273 — 10K_4
BATLED1# — R275 — 10K_4
PWRLED# — R271 — 10K_4

Thermistor(THM)

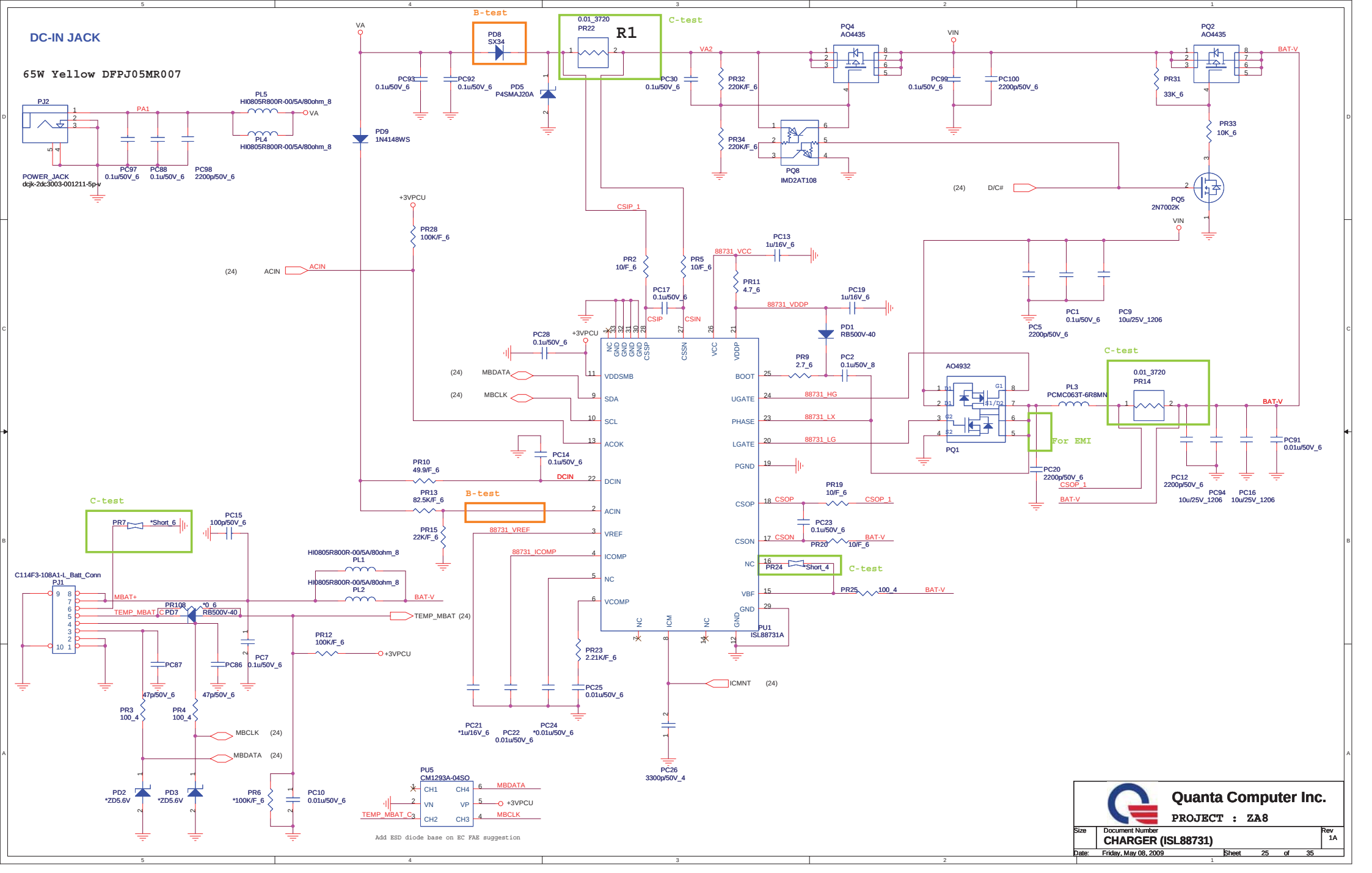
+3V

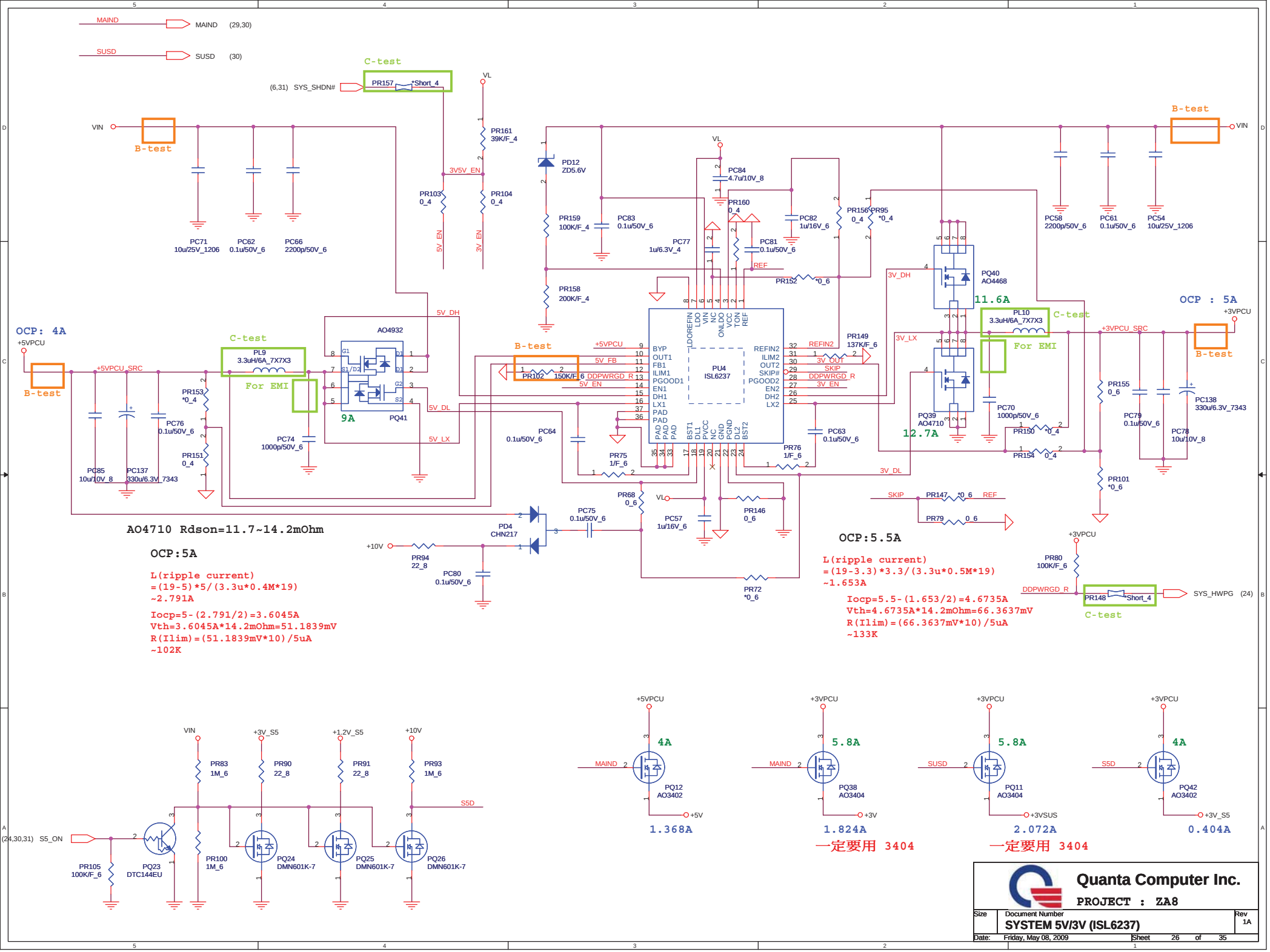
R324 *47K/F_6

R317 *100K/F_4 NTC

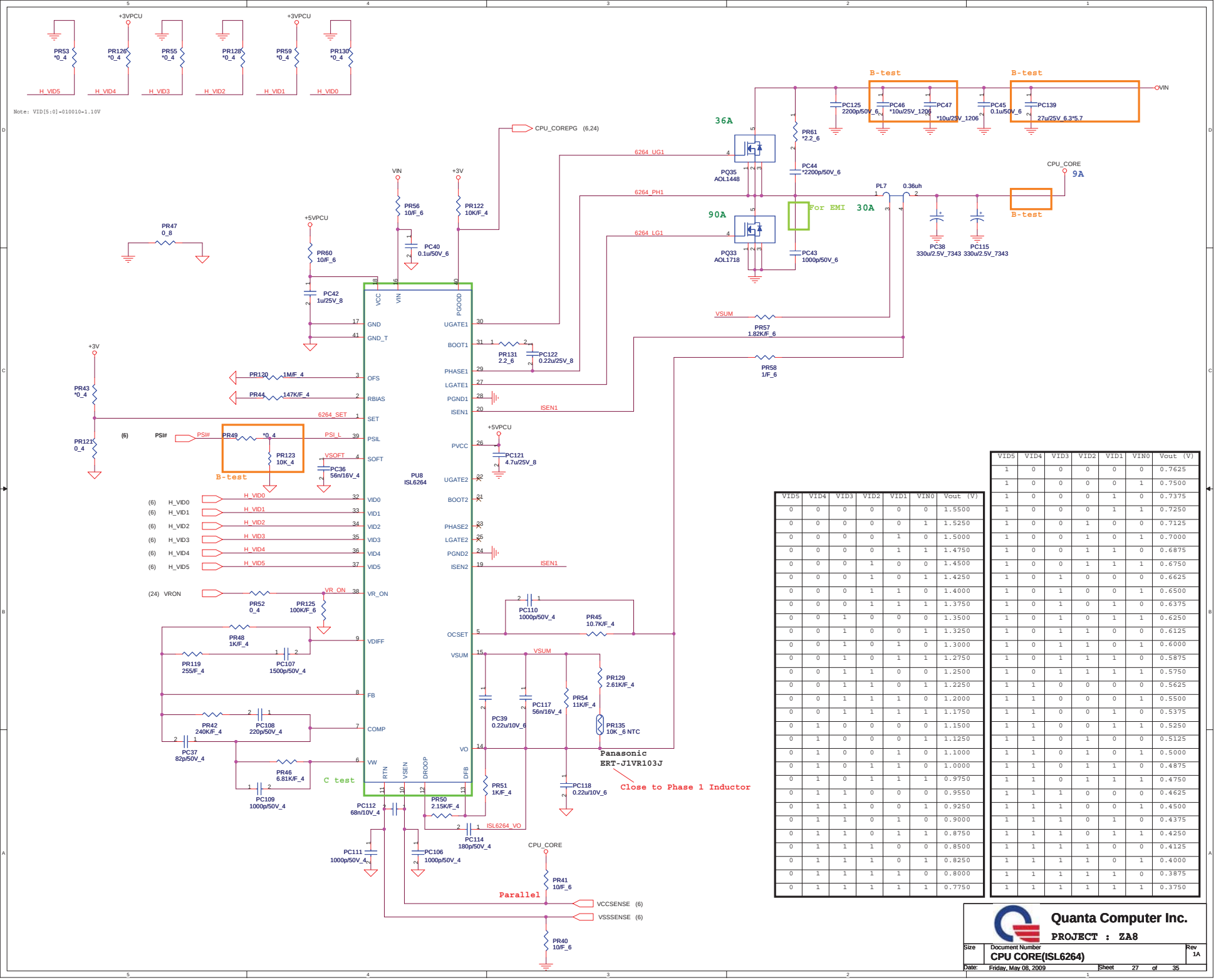
TPD_TRIP

Quanta Computer Inc.	
PROJECT : ZA8	
Size	Document Number: WPCE775L & FLASH — Rev: 1A
Date: Friday, May 08, 2009	Sheet 24 of 35


DC-IN JACK
65W Yellow DFPJ05MR007
B-test
C-test
R1
0.01_3720
PR22
PD8
SX34
PD5
P4SMAJ20A
PD9
1N4148WS
PJ2
POWER_JACK
dcjk-2dc3003-001211-5p-v
PA1
PL5
HI0805R800R-00/5A/80ohm_8
PL4
HI0805R800R-00/5A/80ohm_8
PC93
PC92
PC97
PC88
PC98
PC30
PR32
PR34
PQ4
AO4435
PQ8
IMD2AT108
PQ2
AO4435
PR31
PR33
PQ5
2N7002K
PC99
PC100
VIN
BAT-V
D/C#
+3VPCU
PR28
ACIN
CSIP_1
CSIP
CSIN
PR2
PR5
PR11
88731_VCC
88731_VDDP
PC13
PC17
PC19
PD1
RB500V-40
PC28
PC14
PR10
DCIN
PR13
PR15
PC15
PR7
*Short_6
PR108
*0_6
RB500V-40
PD7
PC1
PC9
PC5
AO4932
PQ1
PL3
PCMC063T-6R8MN
For EMI
PC20
PR9
PC2
PR19
PC23
PR20
PR24
Short_4
PR25
100_4
PC12
PC94
PC16
PC91
CSOP_1
PU1
ISL88731A
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
VBF
GND
88731_HG
88731_LX
88731_LG
88731_VREF
88731_ICOMP
MBDATA
MBCLK
ICMNT
C114F3-108A1-L_Batt_Conn
PJ1
MBAT+
TEMP_MBAT
PL1
PL2
PR12
PR3
PR4
PC87
PC86
PC7
PR23
PC25
PC21
PC22
PC24
PC26
PD2
*ZD5.6V
PD3
*ZD5.6V
PR6
*100K/F_6
PC10
PU5
CM1293A-04SO
CH1
VN
CH2
CH4
VP
CH3
Add ESD diode base on EC FAE suggestion
Quanta Computer Inc.
PROJECT : ZA8
Size
Document Number
CHARGER (ISL88731)
Rev
1A
Date: Friday, May 08, 2009
Sheet 25 of 35



Quanta Computer Inc.		
PROJECT : ZA8		
Size	Document Number: SYSTEM 5V/3V (ISL6237)	Rev: 1A
Date: Friday, May 08, 2009	Sheet 26 of 35	



VID5	VID4	VID3	VID2	VID1	VIN0	Vout (V)
0	0	0	0	0	0	1.5500
0	0	0	0	0	1	1.5250
0	0	0	0	1	0	1.5000
0	0	0	0	1	1	1.4750
0	0	0	1	0	0	1.4500
0	0	0	1	0	1	1.4250
0	0	0	1	1	0	1.4000
0	0	0	1	1	1	1.3750
0	0	1	0	0	0	1.3500
0	0	1	0	0	1	1.3250
0	0	1	0	1	0	1.3000
0	0	1	0	1	1	1.2750
0	0	1	1	0	0	1.2500
0	0	1	1	0	1	1.2250
0	0	1	1	1	0	1.2000
0	0	1	1	1	1	1.1750
0	1	0	0	0	0	1.1500
0	1	0	0	0	1	1.1250
0	1	0	0	1	0	1.1000
0	1	0	1	1	0	1.0000
0	1	0	1	1	1	0.9750
0	1	1	0	0	0	0.9550
0	1	1	0	0	1	0.9250
0	1	1	0	1	0	0.9000
0	1	1	0	1	1	0.8750
0	1	1	1	0	0	0.8500
0	1	1	1	0	1	0.8250
0	1	1	1	1	0	0.8000
0	1	1	1	1	1	0.7750

VID5	VID4	VID3	VID2	VID1	VIN0	Vout (V)
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.7500
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.7250
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7000
1	0	0	1	1	0	0.6875
1	0	0	1	1	1	0.6750
1	0	1	0	0	0	0.6625
1	0	1	0	0	1	0.6500
1	0	1	0	1	0	0.6375
1	0	1	0	1	1	0.6250
1	0	1	1	0	0	0.6125
1	0	1	1	0	1	0.6000
1	0	1	1	1	0	0.5875
1	0	1	1	1	1	0.5750
1	1	0	0	0	0	0.5625
1	1	0	0	0	1	0.5500
1	1	0	0	1	0	0.5375
1	1	0	0	1	1	0.5250
1	1	0	1	0	0	0.5125
1	1	0	1	0	1	0.5000
1	1	0	1	1	0	0.4875
1	1	0	1	1	1	0.4750
1	1	1	0	0	0	0.4625
1	1	1	0	0	1	0.4500
1	1	1	0	1	0	0.4375
1	1	1	0	1	1	0.4250
1	1	1	1	0	0	0.4125
1	1	1	1	0	1	0.4000
1	1	1	1	1	0	0.3875
1	1	1	1	1	1	0.3750

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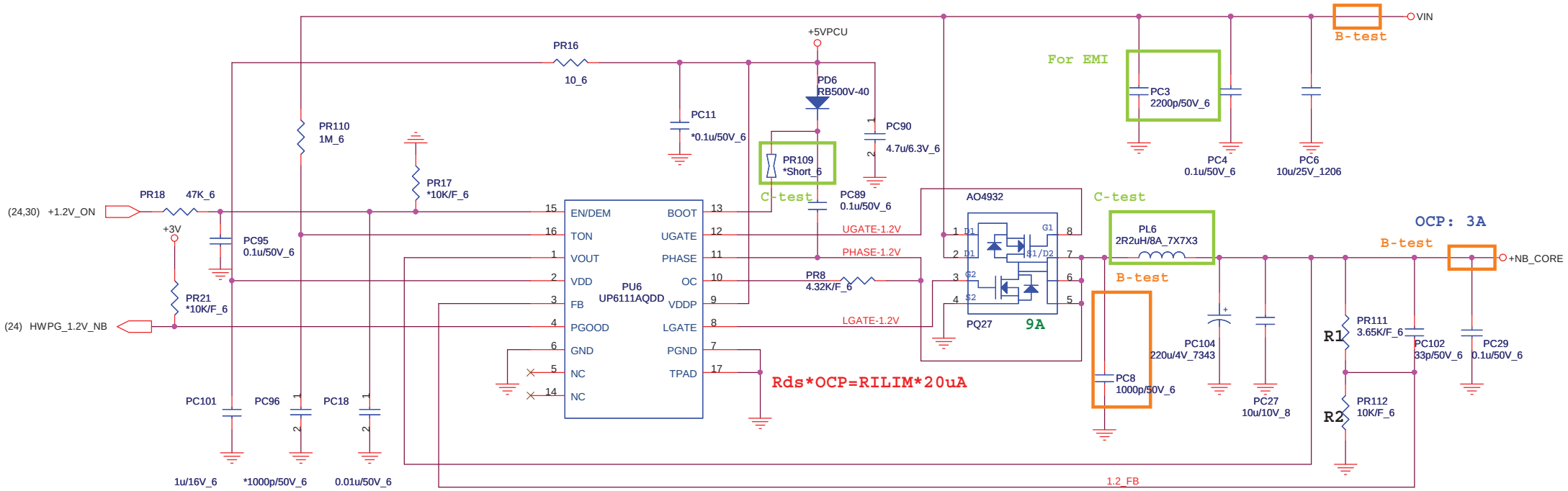
PROJECT : ZA8

Size	Document Number	Rev
	CPU CORE(ISL6264)	1A

Date: Friday, May 08, 2009 Sheet 27 of 35



TON=3.85p*RTON*Vout/(Vin-0.5)
Frequency=Vout/(Vin*TON)

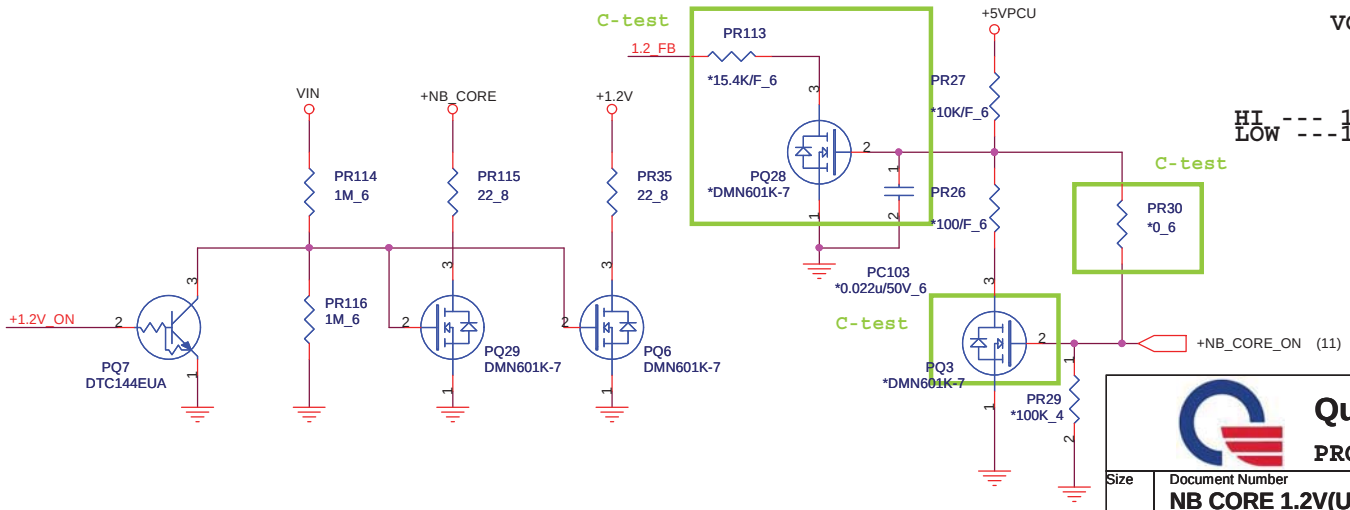
TON=3.85p*1M*1/(Vin-0.5)
Frequency=1/(0.0036767)=272K

AO4710 Rdson=11.7~14.2mOhm

L(ripple current)
=(19-1.2)*1.2/(3.3u*272k*19)
~1.878A

14.2m*6=RILIM*20uA
RILIM=4.26K(4.32K)

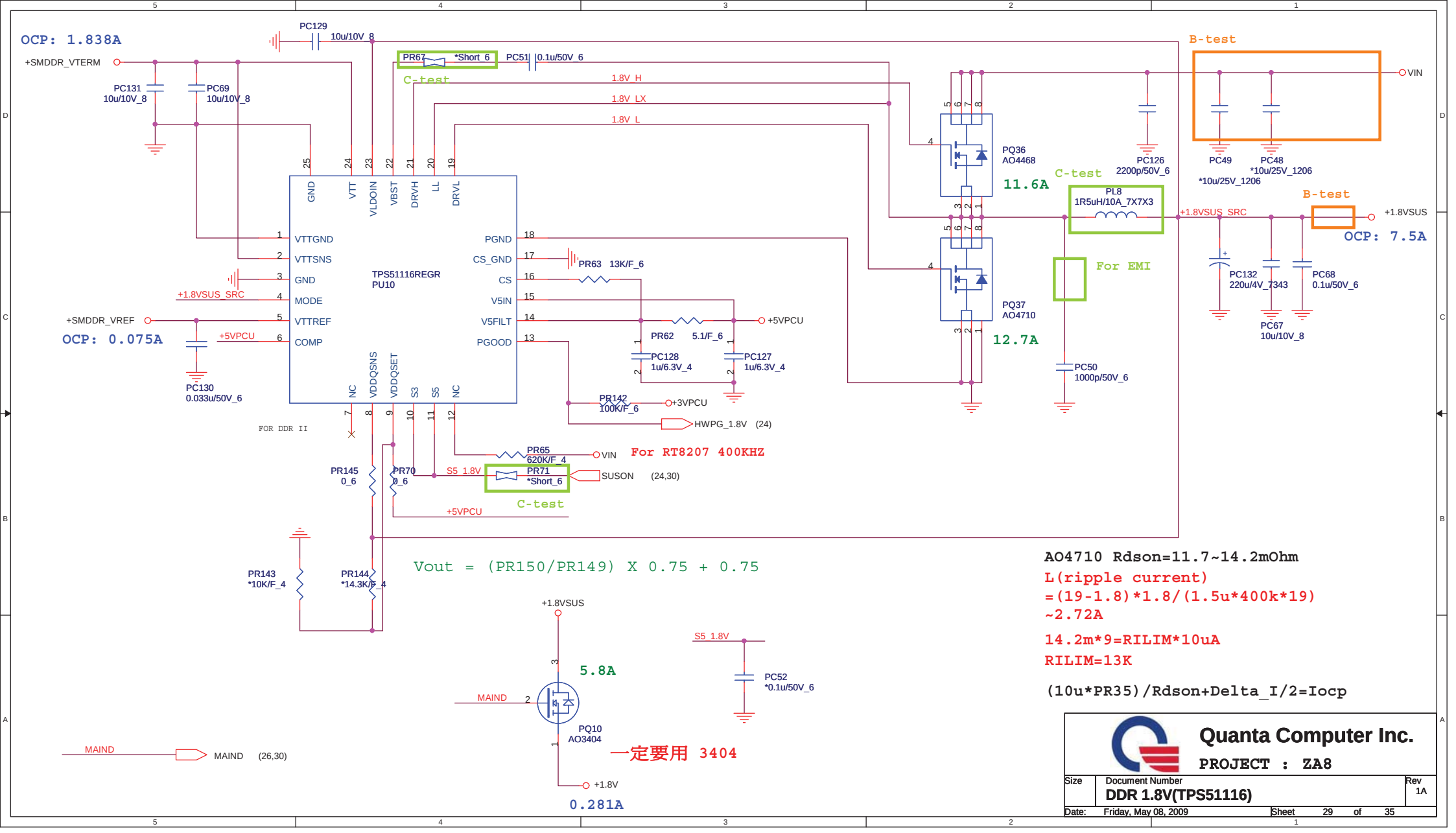
VOUT=(1+R1/R2)*0.75



Quanta Computer Inc.

PROJECT : ZA8

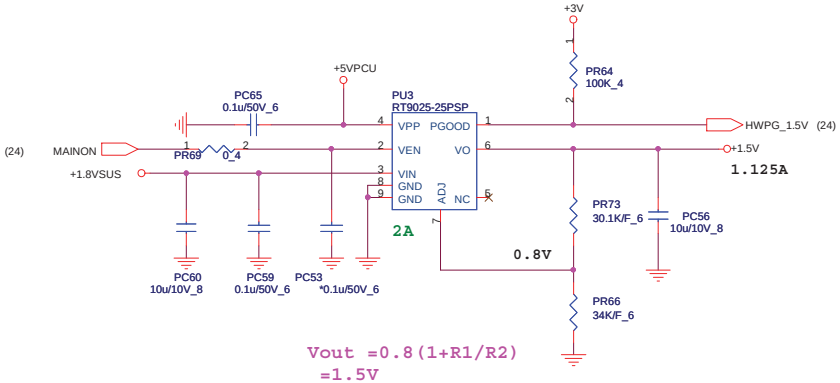
Size	Document Number	Rev
	NB CORE 1.2V(UP6111AQDD)	1A
Date: Friday, May 08, 2009	Sheet 28 of 35	



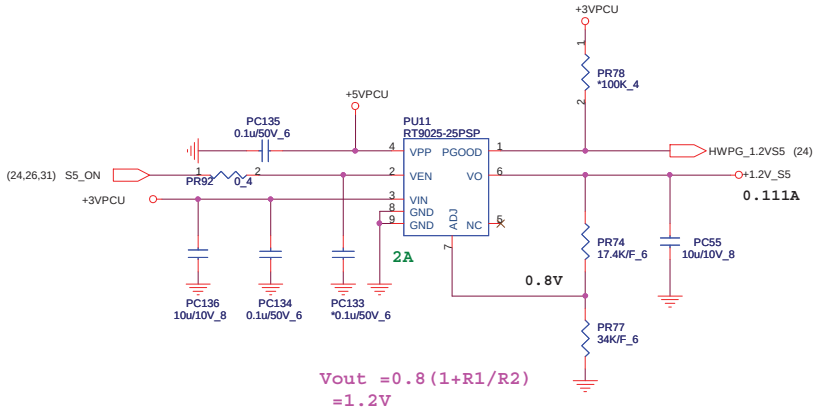
Quanta Computer Inc.

PROJECT : ZA8

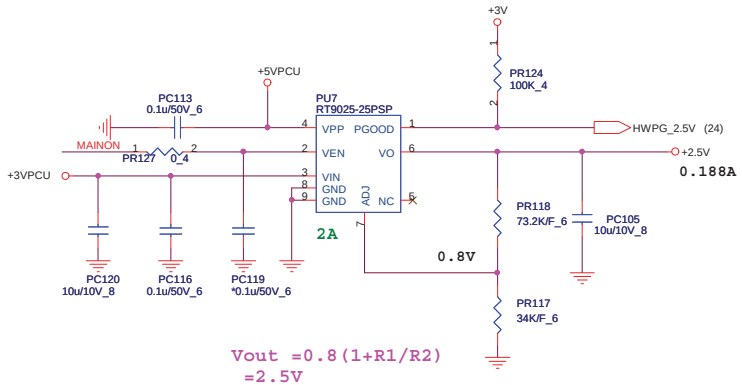
Size	Document Number	Rev
	DDR 1.8V(TPS51116)	1A
Date: Friday, May 08, 2009	Sheet 29 of 35	



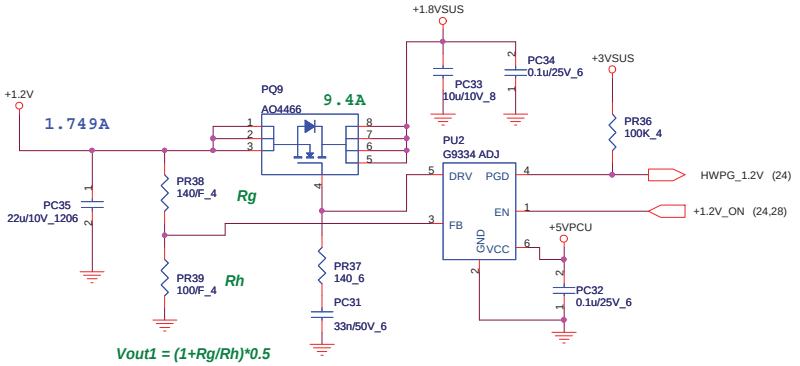
Vout =0.8(1+R1/R2)
=1.5V



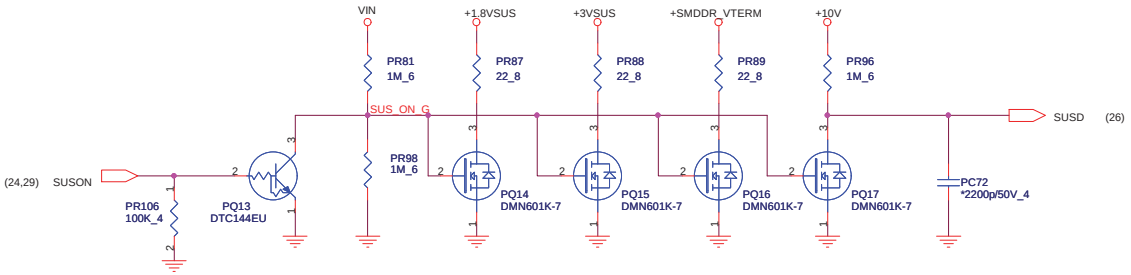
Vout =0.8(1+R1/R2)
=1.2V

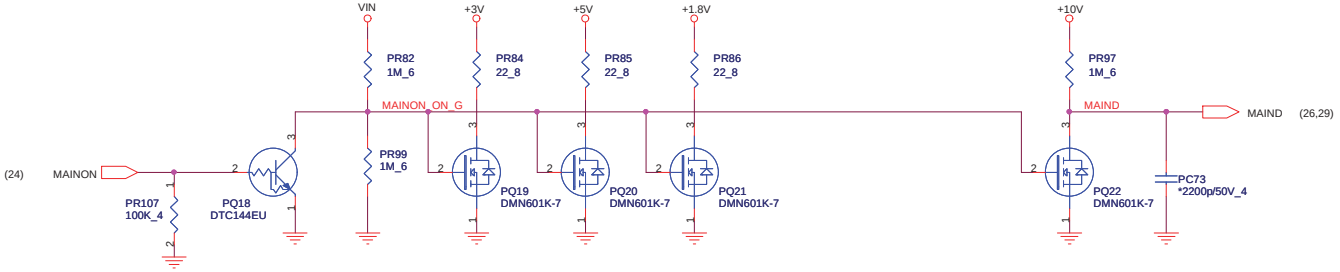


Vout =0.8(1+R1/R2)
=2.5V



*Vout1 = (1+Rg/Rh)*0.5*





Quanta Computer Inc.

PROJECT : ZA8

Size	Document Number	Rev
	Discharge (2.5V/1.5V/1.2V)	1A

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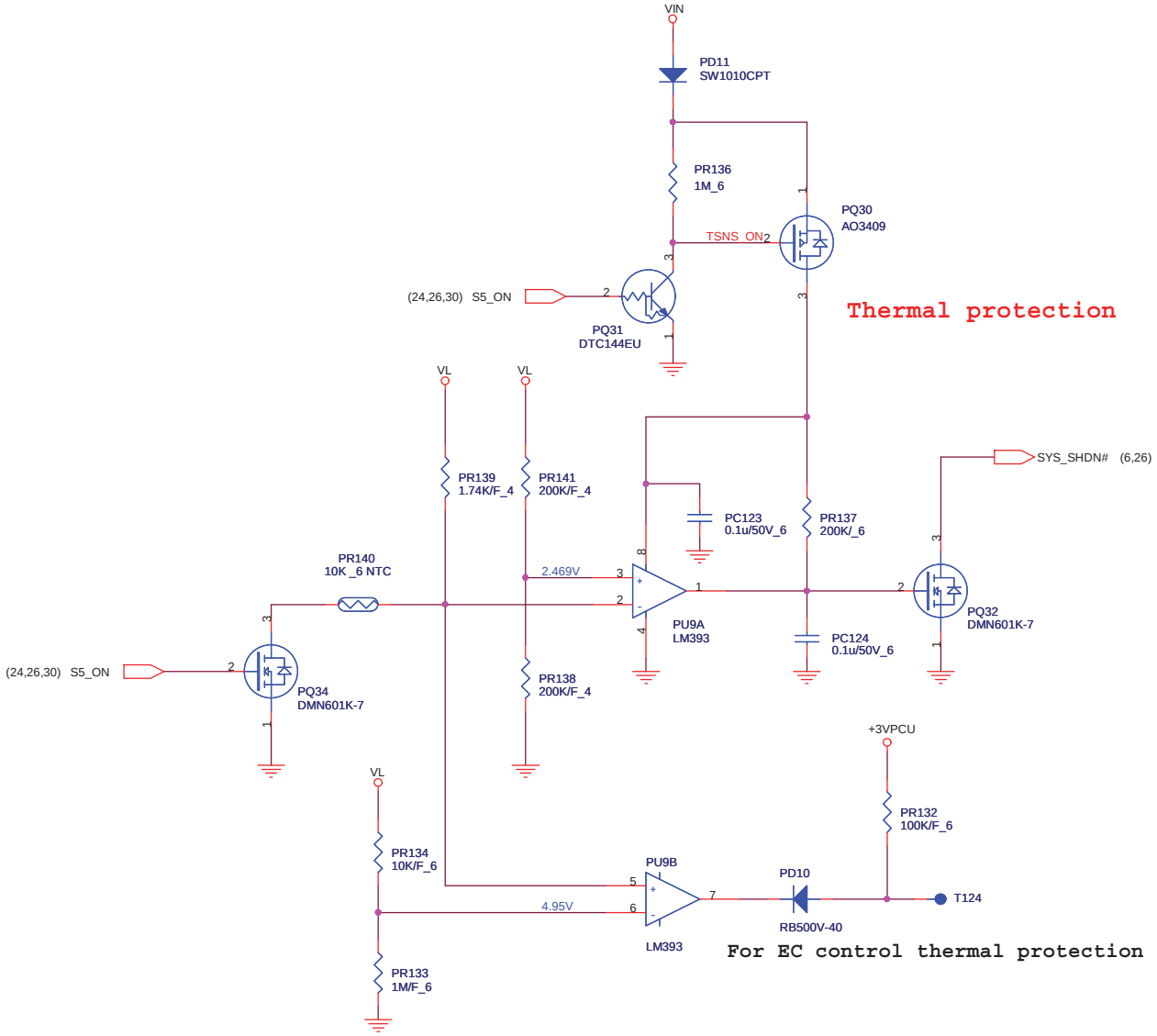
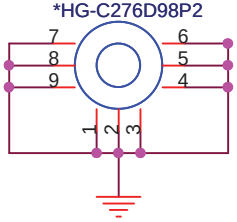
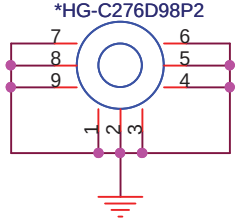


Quanta Computer Inc.		
PROJECT : ZA8		
Size	Document Number: Thermal protect	Rev 1A
Date: Friday, May 08, 2009	Sheet 31 of 35	

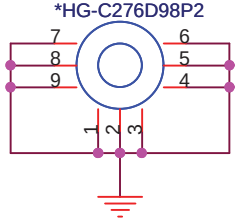
HOLE1
*HG-C276D98P2



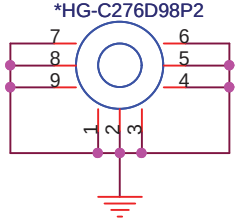
HOLE3
*HG-C276D98P2



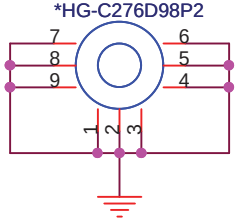
HOLE2
*HG-C276D98P2



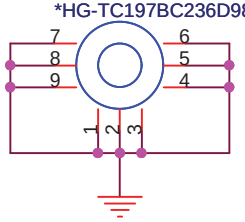
HOLE13
*HG-C276D98P2



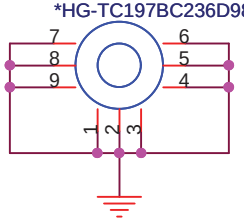
HOLE8
*HG-C276D98P2



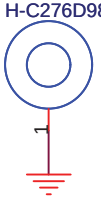
HOLE18
*HG-TC197BC236D98P2



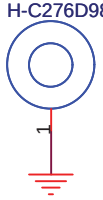
HOLE16
*HG-TC197BC236D98P2



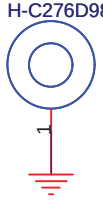
HOLE6
H-C276D98P2



HOLE10
H-C276D98P2

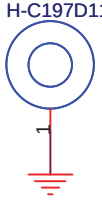


HOLE12
H-C276D98P2

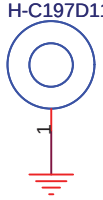


B-test

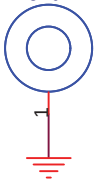
HOLE4
H-C197D118P2



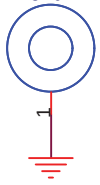
HOLE5
H-C197D118P2



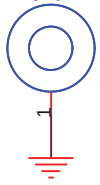
HOLE7
H-C197D118P2



HOLE9
H-C197D118P2

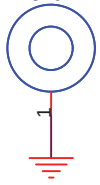


HOLE11
H-C197D118P2

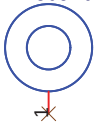


B-test

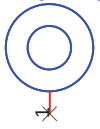
HOLE14
H-C197D102P2



HOLE17
*H-C98D98N



HOLE15
*H-O114X98D114X98N



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	HOLE	1A
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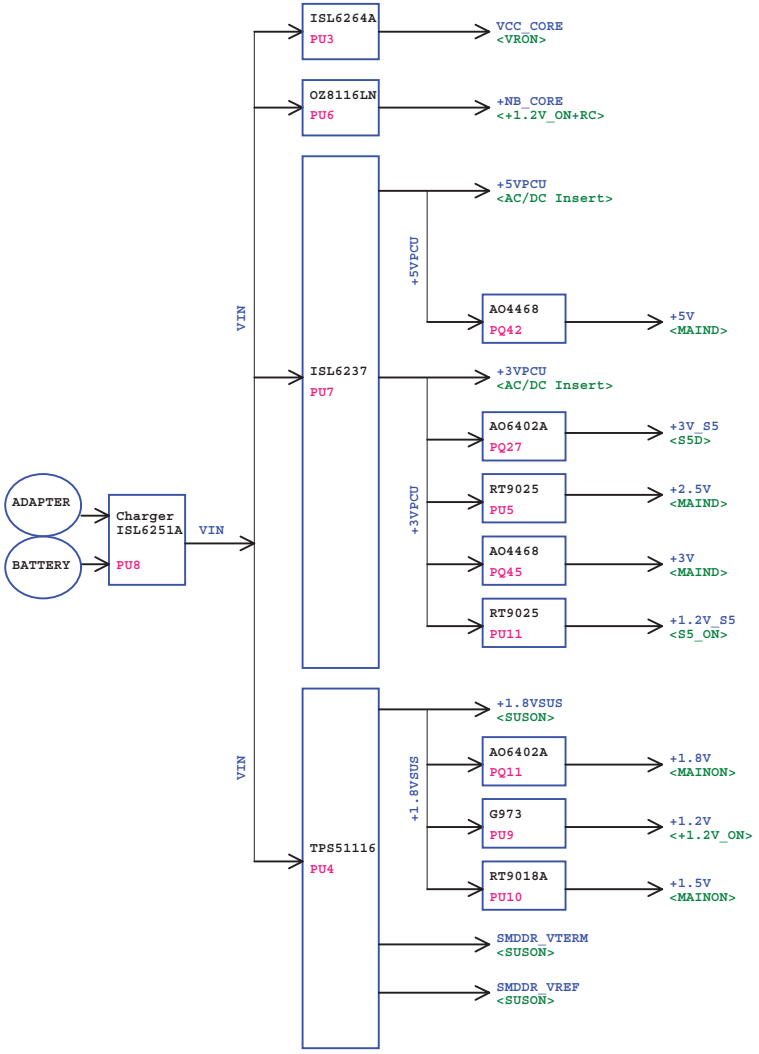

POWER	Distribution
VCC_CORE	CPU
+5VPCU	Battery LED , Power LED , RTC , USB , Power Board
+3VPCU	HALL SENSOR , Battery LED , KB , EC , ID , SPI Flash , RTC
+NB_CORE	RS690M
+5V	CAMERA , SATA ODD/HDD , T/P , CRT , SB600 , CPU FAN , EC , INT SPK AMP
+3V	HALL SENSOR , LVDS , WLAN , KB , KB LED , Blue tooth , Touch sensor , Card Reader CRT , REQUIRED STRAPS , DEBUG STRAPS , SB600 , RS690M , DDR , CPU Thermal monitor , CPU FAN , CLK EC , Codec(CX 20561) , SIM Card , 3G MINI Card
+3V_S5	WLAN , SB600 , LAN
+2.5V	CPU
+1.2V_S5	SB600
+1.8VSUS	SB600 , DDR , CPU
+1.8V	SB600 , RS690M
+1.5V	SIM Card , 3G MINI Card , WLAN
+1.2V	SB600 , RS690M , CPU
+SMDDR_VTERM	DDR , CPU
+SMDDR_VREF	DDR

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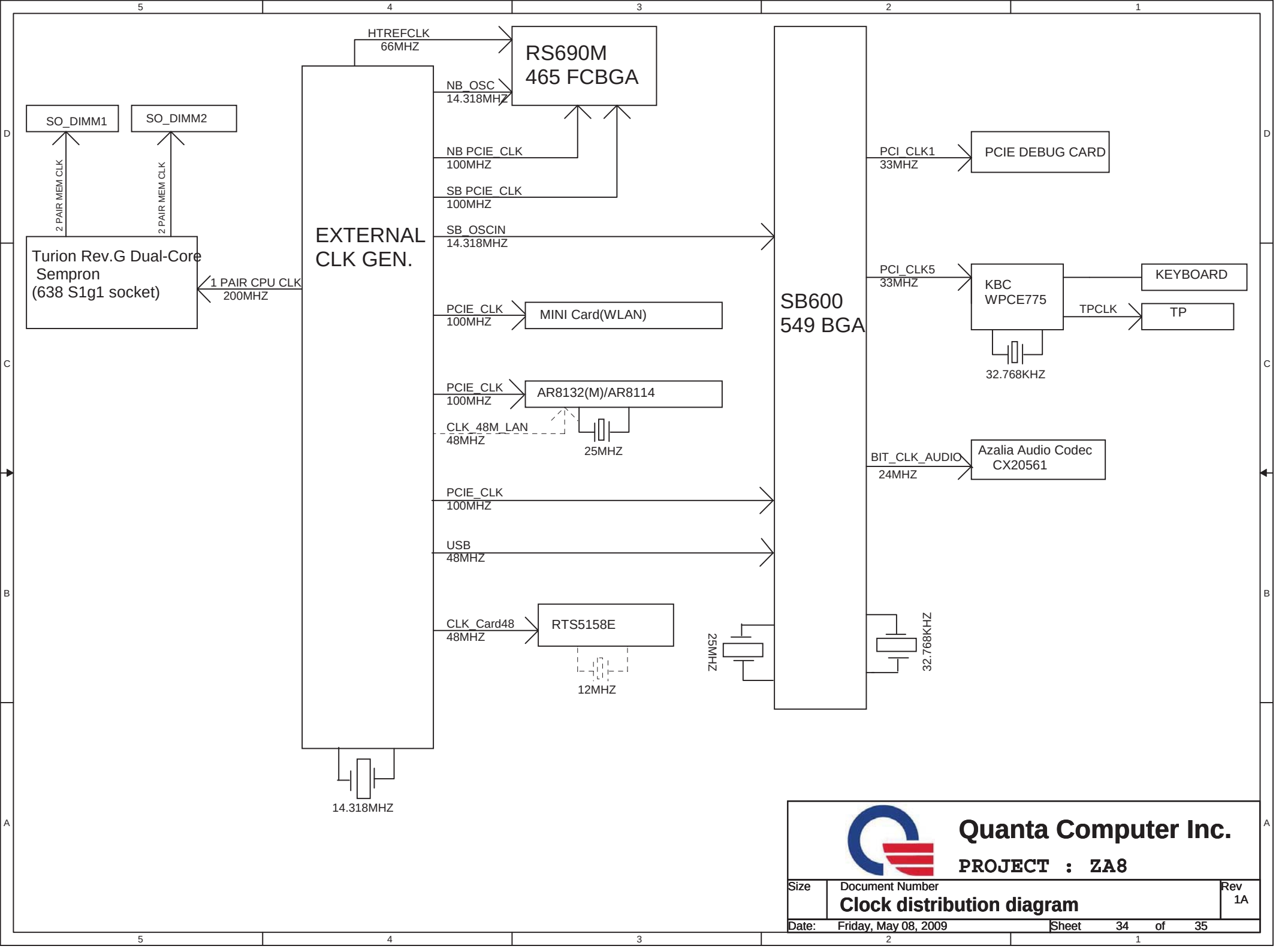

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Size	Document Number	Rev
	Clock distribution diagram	1A
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Model	REV	DATE	CHANGE LIST	NOTE
ZA8	A	20090312	**FIRST RELEASED : Import BOM ECN E200903-2235**	ECN Release
	SMT inner doc.	20090316	Page17: Stuff R87 and non Stuff R92. (Update board ID setting)	
		20090317	Page28: Change PR113 from 35.7K (CS33573F910) to 15.4K (CS31543F929). (+NB_CORE setting)	
	B	20090410	Page03: Change U5 PN to Silego(AL084605K05)	
			Swap CLKREQA# and CLKREQB#	
			Delete Q6, R94 and C145, then add test point (T160).	
			Change R177 footprint from 0Ω 0402 to short pad.	
			Page06: Change CN10 footprint.	
			Un-stuff C354 and R269.	
			Change R220 footprint from 0Ω 0603 to short pad.	
			Delete R39. (TALERT# net)	
			Stuff Q3, R41 and R40.	
			Page08: Delete Jumper. (JP8, JP9, JP11 and JP12)	
			Page09: Change U11 PN to AKD5LG-TW02. (Hynix 128MB)	
			Add C476, C477 and C478 for EMI request.	
			Page13: Chagne R255 from 16KΩ to 22KΩ for fine tune RTC charge current	
			Change R192, R193 and R115 footprint from 0Ω 0402 to short pad.	
			Change R362, R360 and R364 footprint from 22Ω 0402 to short pad.	
			Page15: Change C254 and C238 from 10pF to 27pF for vendor recommend.	
			Delete TALERT# net and add test point T161 on pin T7.	
			Page17: Update BID1, BID2 default setting. (Stuff R91 and R114, un-stuff R88 and R118)	
			Page18: Change R232, R12 and R13 footprint from 0Ω 0402 to short pad.	
			Change R219 footprint from 0Ω 0805 to short pad.	
			Change Q14 and Q15 from BAM700200F6 to BAM700200H2 for SMT request.	
			Page19: Change R141 and R160 from 0Ω 0402 to 0063 bead(CX08T301016) for EMI request.	
			Change R172 footprint from 0Ω 0402 to short pad.	
			Change C451 from 1uF to 4.7uF for pop sound issue.	
			Change U7 power from +3V to +3VSUS and reserve R285, C479 for HP pop sound issue.	
			Change C122, C124, C127 and C135 to 0.01uF for EMI request. (Reserve only)	
			Page20: Change R4 footprint from 0Ω 0603 to short pad.	
			Change C4 and C5 from 27pF to 33pF for vendor request.	
			Page21: Change JSIM1 footprint.	
			Change R67, R187 and R186 footprint from 0Ω 0402 to short pad.	
			Delete R57, R326, R332, R336, R341 and R338.	
			Delete R57, R326, R332, R336, R341, R338 and R179.	
			Add 3G@ on CN16, R108, R210 and R143.	
			Page22: Update SATA ESD solution to VPORT. (Delete U2 and add RV3~RV6)	
			Delete R16 and short it directly.	
			Change R72 and R73 from 0Ω 0402 to short pad.	
			Change R149 and C156 to 470pF, then stuff them for EMI request.	
			Delete card reader 48MHz and reserve GND and HP_MUTE# on CN7 pin2. (Delete C258, stuff R152 0Ω 0402and add R94 0Ω 0402)	
			Page23: Change R39 and R57 footprint from 0Ω 0402 to short pad.	
			Change R294, R296, R348, R347 and R346 from 0Ω 0402 to short pad.	
			Change D19, D22 and D21 from 0Ω 0603 to short pad.	
			Un-stuff D2, D3 and D1.	
			Change SW1 from switch to jumper.	
			Page25: Stuff PR7.	
			Change PD8 from BC01040SZ01 to BC00SX34Z04.	
			Change PR22 and PR14 from 0.02Ω to 0.01Ω.	
			Delete ACIN net name on PU1.pin2 for wrong net name.	
			Page26: Change PR102 from 102K to 150K for OCP setting.	
			Delete jumper. (JP2, JP3, JP13 and JP14)	
			Page27: Change PR123 from 0Ω to 10K and stuff it.	
			Un-stuff PC46 and PC47 for noise issue.	
			Add PC139(27uF) for noise issue.	
			Un-stuff PR49.	
			Delete jumper. (JP7 and JP9)	
			Page28: Delete PR1 ; Change PC8 from 2200pF to 1000pF and stuff it.	
			Delete jumper.(JP5 and JP6)	
			Page29: Un-stuff PC49 and PC48 for noise issue.	
			Delete jumper. (JP1 and JP4)	

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Model	REV	DATE	CHANGE LIST	NOTE
				ECN Release
ZA8	C	20090507	Page03: Change R93 from 0402 0Ω to short pad.	
			Page06: Un-stuff R41, R40 and Q3.	
			Change R235 from 0402 0Ω to short pad.	
			Page08: Delete R157 and R158, then short directly.	
			Page11: Change R20 and R22 from 0402 0Ω to short pad.	
			Change L42 from 0603 0Ω to short pad.	
			Page13: Change R345 from 0603 0Ω to short pad.	
			Page14: Change R102 and R106 from 0402 0Ω to short pad.	
			Page15: Change R375 and R374 from 0603 0Ω to short pad.	
			Page16: Change R68 and R86 from 0805 0Ω to short pad.	
			Change R208, R373, R137 and R101 from 0603 0Ω to short pad.	
			Page18: Change R216 and R217 from 0805 0Ω to short pad.	
			Add D24 for SMT request.	
			Page19: Change R329, R89, R78, R69 ,R63, R175 and R167 from 0603 0Ω to short pad.	
			Change R352 from 0402 0Ω to short pad.	
			Page20: Change R3 from 0402 0Ω to short pad.	
			Add C480 for EMI request.	
			Page21: Change R79 ,R80, R104, R180, R241, R239 and R240 from 0402 0Ω to short pad.	
			Change R103 and L34 from 0805 0Ω to short pad.	
			Page24: Change R270 and R330 from 0603 0Ω to short pad.	
			Page25: Change PR24 from 0402 0Ω to short pad.	
			Change PR7 from 0603 0Ω to short pad.	
			Update PR22 and PR14 footprint for SMT request.	
			Page26: Update PL10 and PL9 footprint for SMT request.	
			Change PR157 and PR148 from 0402 0Ω to short pad.	
			Page27: Update PU8 footprint for SMT request.	
			Page28: Change PR109 from 0603 0Ω to short pad.	
			Update PL6 footprint for SMT request.	
			Un-stuff PR113, PQ28, PC103, PQ3 and PR30.	
			Page29: Change PR67 and PR71 from 0603 0Ω to short pad.	
			Update PL8 footprint for SMT request.	

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