

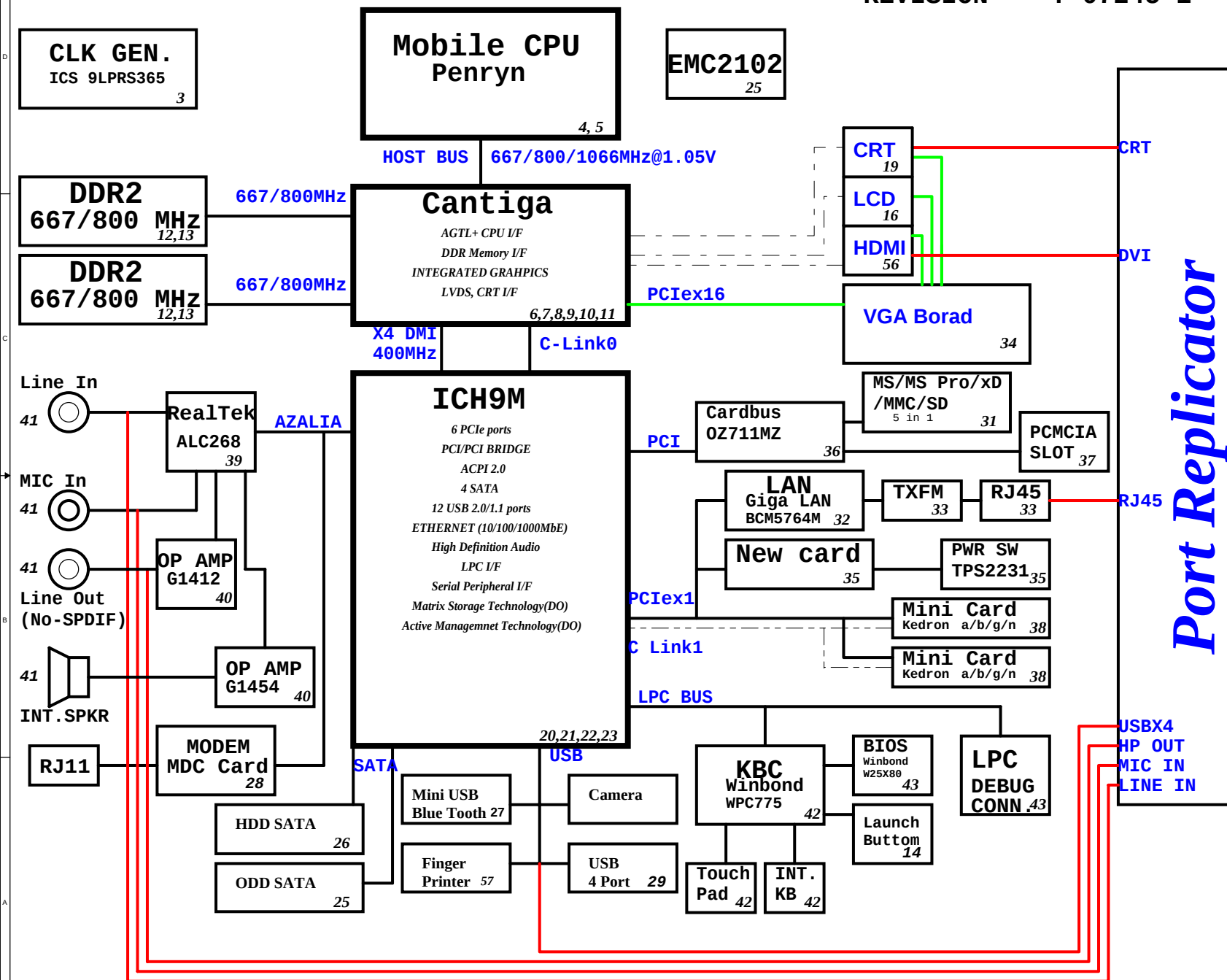
Homa (TM15") Block Diagram

Project code: 91.4Z401.001
PCB P/N : 48.4Z401.011
REVISION : 07245-1

PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

SYSTEM DC/DC TPS51125 49	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(7A) 3D3V_S5(7A)
SYSTEM DC/DC TPS51124 51	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(16A) 1D8V_S3(16A)
TPS51100 50	
5V_S5	DDR_VREF_S3 (1.5A) DDR_VREF_S3_1
G9131	
3D3V_S0	2D5V_S0 (300mA)
APL5912 50	
1D8V_S3	1D5V_S0 (2.5A)
CHARGER BQ24750 53	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA
CPU DC/DC ISL6266A 48	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 38A
GFX DC/DC ISL6263 48	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 5.5A



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ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config 1bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIe config 1 bit 0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIe config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved, Rising Edge of PWROK.	This signal has a weak internal pull-down. This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	Tying this strap low configures DMI for ESI-compatible operation. This signal has a weak internal pull up. ESI compatible mode is for server platforms only.This signal should not be pulled low for desttop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing. It has a weak internal pull up.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

PCI Routing

page 31

	IDSEL	INT	REQ	GNT
RTS5158	AD25	G:CARDBUS	0	0

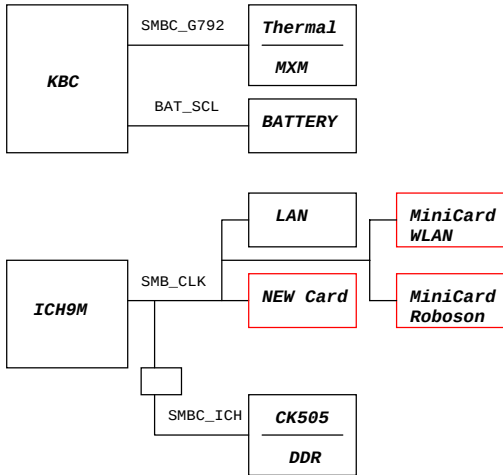
PCIe Routing

LANE1	LAN BCM5764MKMLG
LANE2	MiniCard WLAN
LANE3	MiniCard Roboson
LANE4	NewCard

SMBus

USB Table

USB	
Pair	Device
0	USB1
1	USB4
2	USB2
3	DOCK USB
4	USB3
5	Bluetooth
6	FP
7	MINIC1
8	WEBCAM
9	NEW1
10	MINIC2
11	NC



ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5 page 97

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 10K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for nativeCFG9 GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55, 53, 51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LAD[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

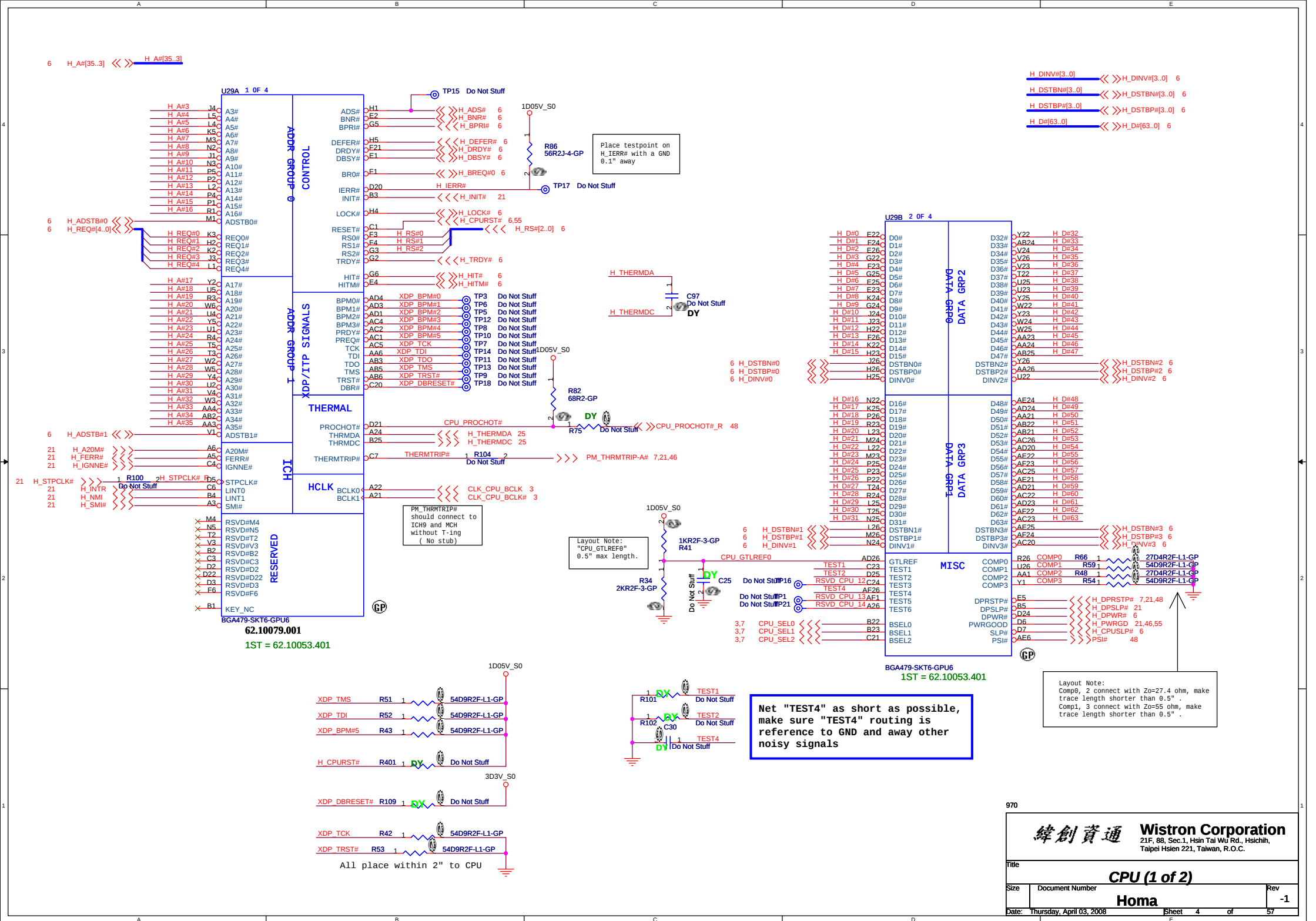
Montevina Platform Design guide 22339 0.5 page 218

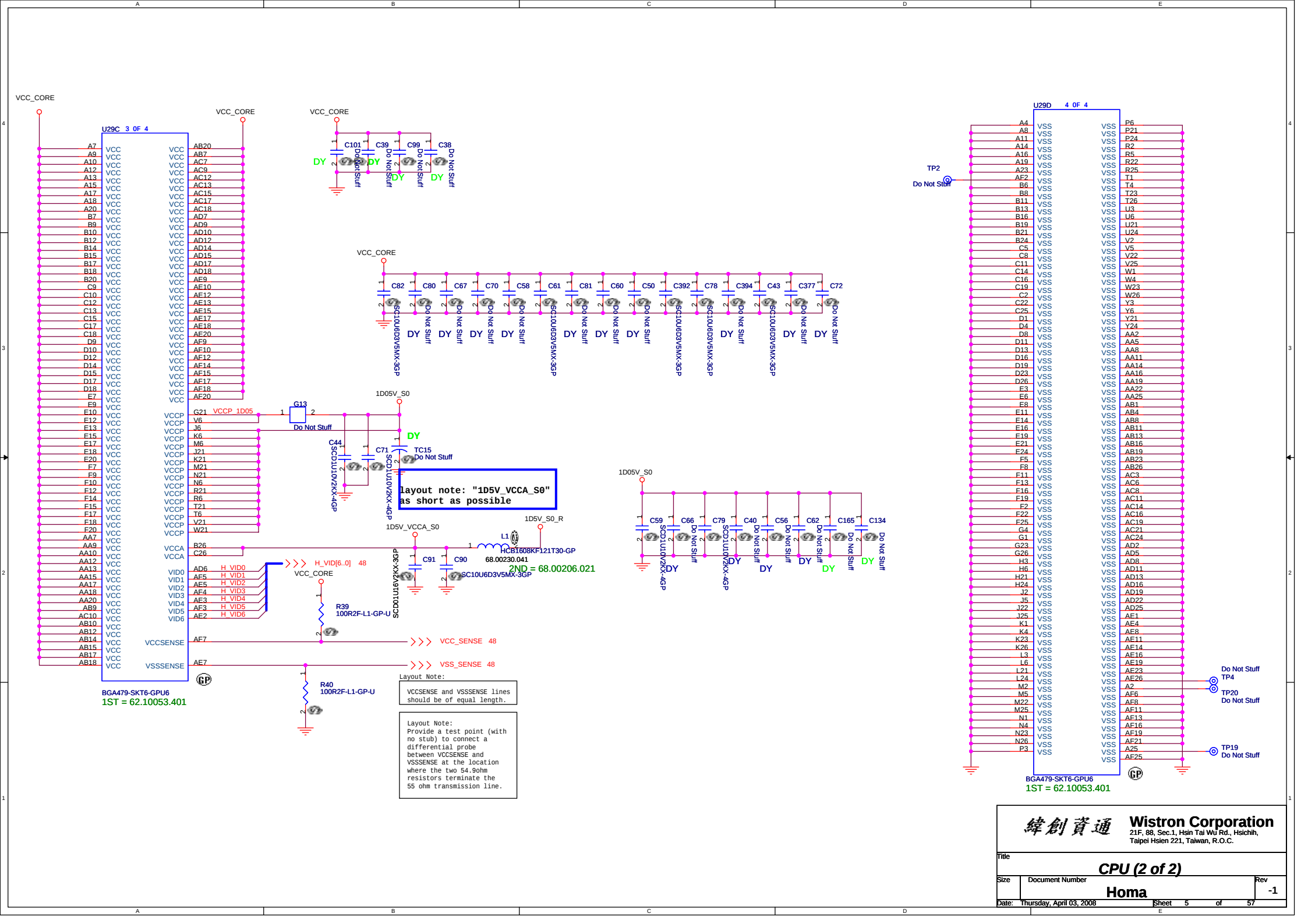
Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1066 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIe Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIe Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG12	ALLZ	0 = ALLZ mode enabled (Note 3) 1 = Disabled (default)
CFG13	XOR	0 = XOR mode enabled (Note 3) 1 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display Port or PCIe is operational (Default) 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIe disabled

- NOTE:
- All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
 - iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.
 - Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

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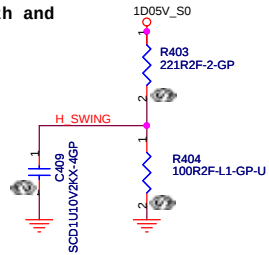
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Reference	
Size A3	Document Number
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Date: Thursday, April 03, 2008	Sheet 2 of 57
Rev -1	



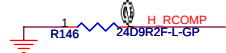


H_SWING routing Trace width and Spacing use 10 / 20 mil

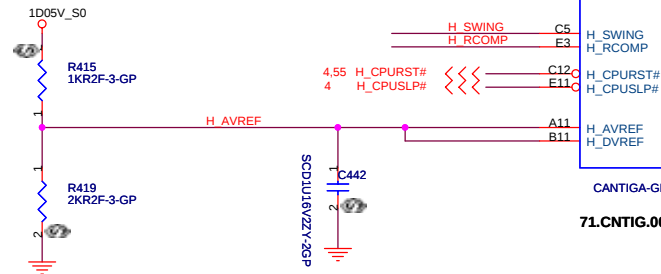
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



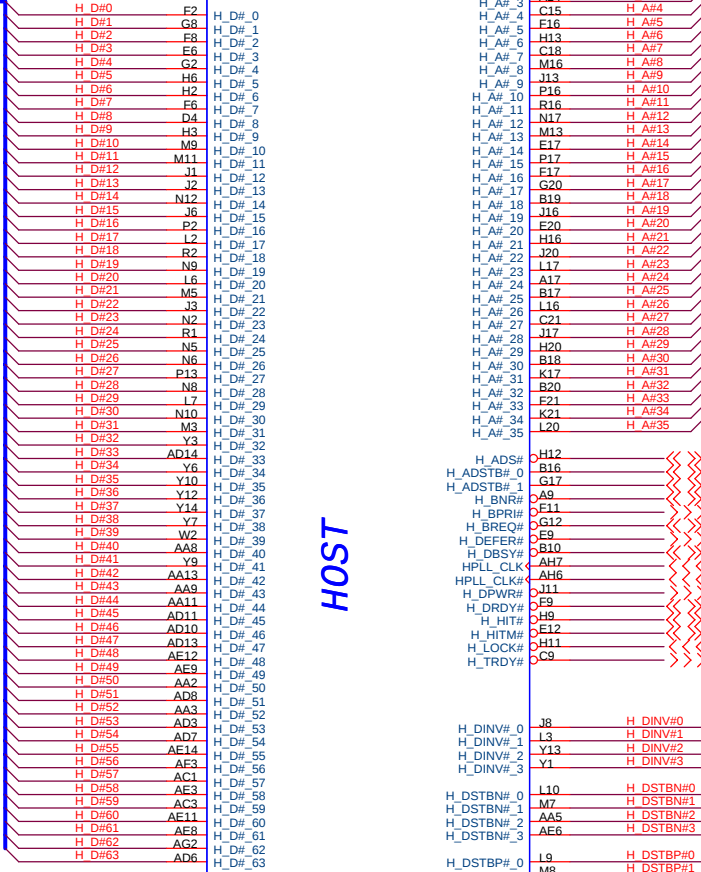
H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



U37A 1 OF 10



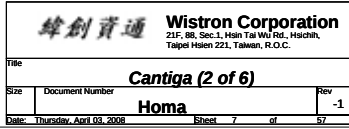
HOST

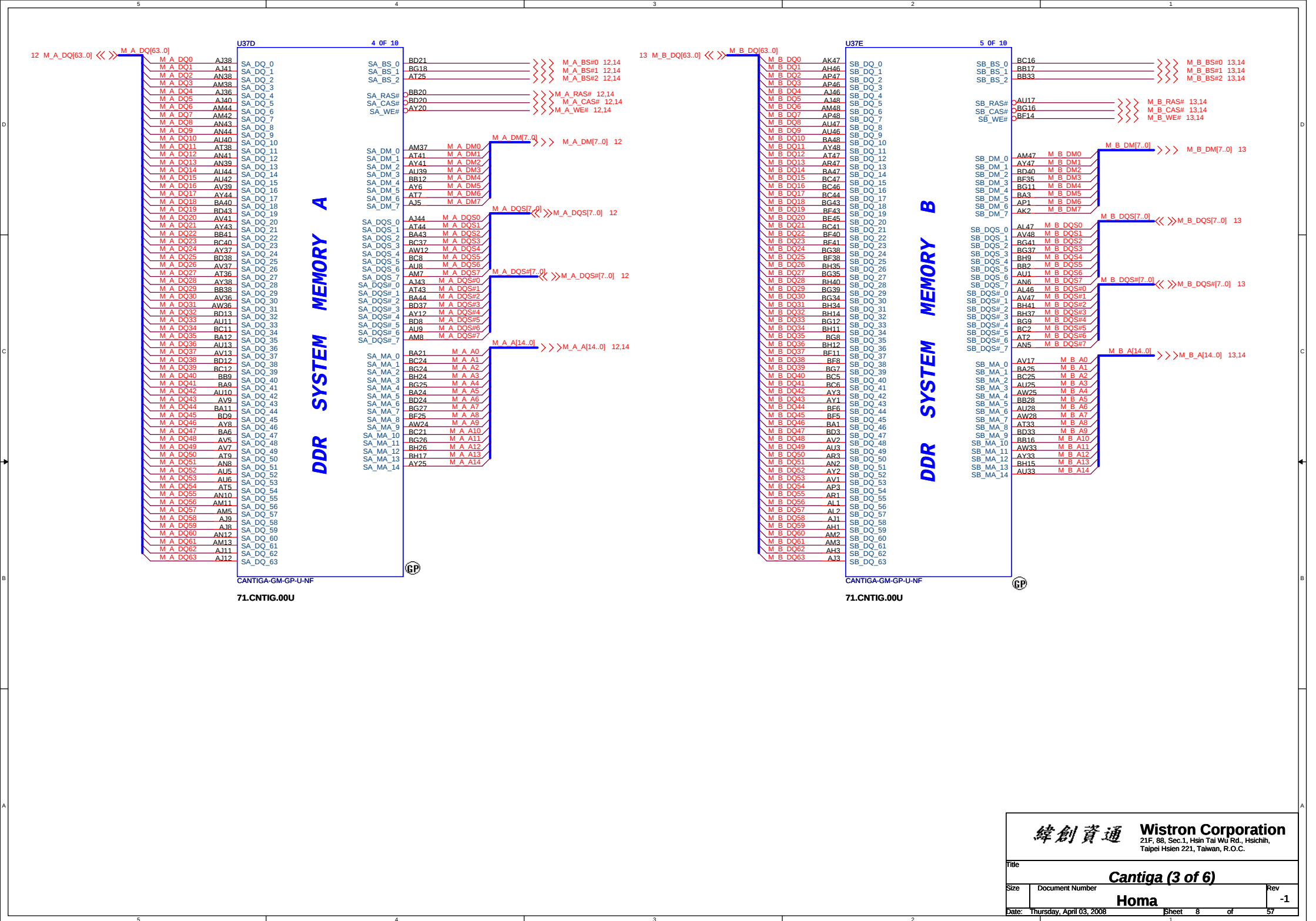
CANTIGA-GM-GP-U-NF

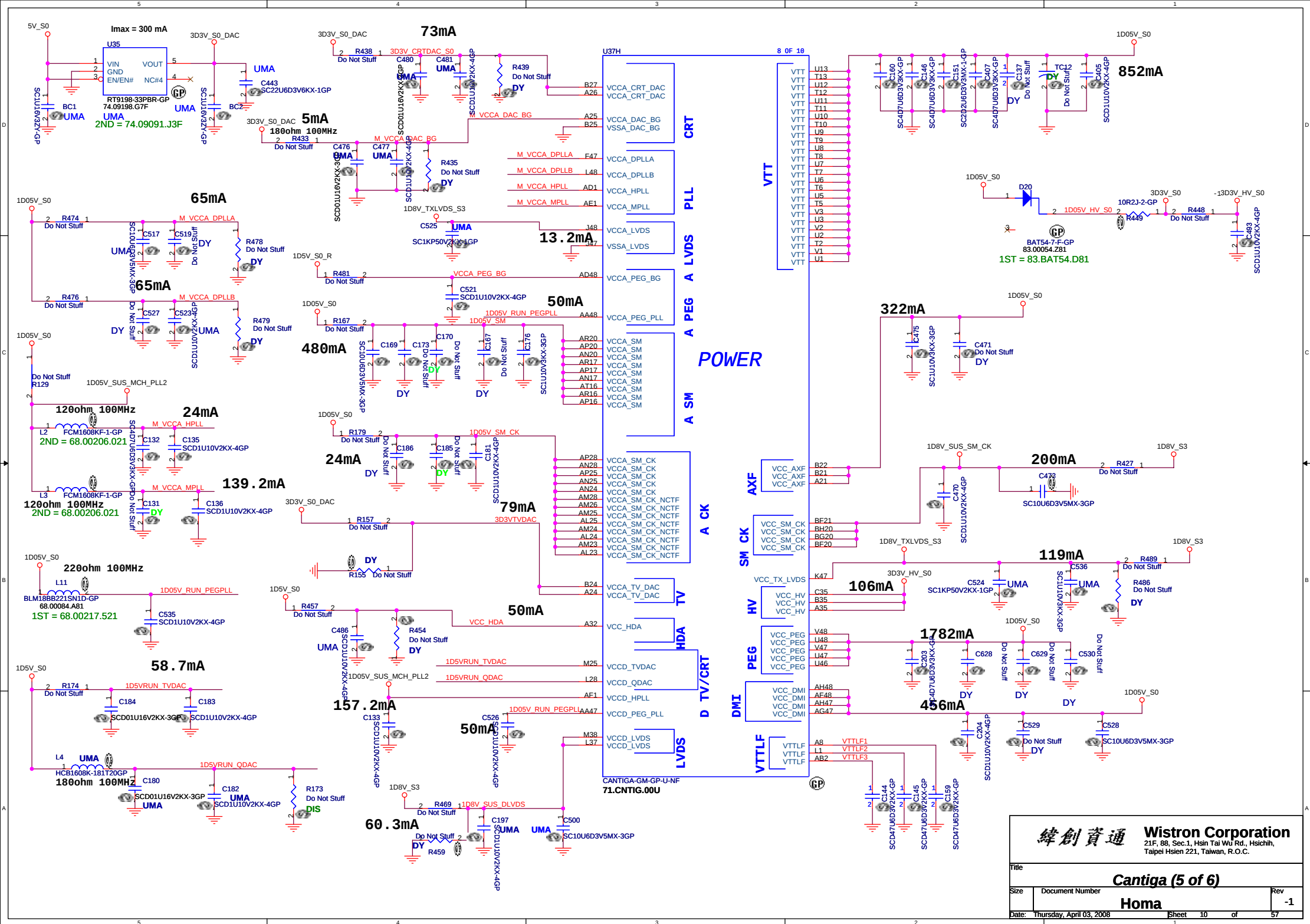
71.CNTIG.00U

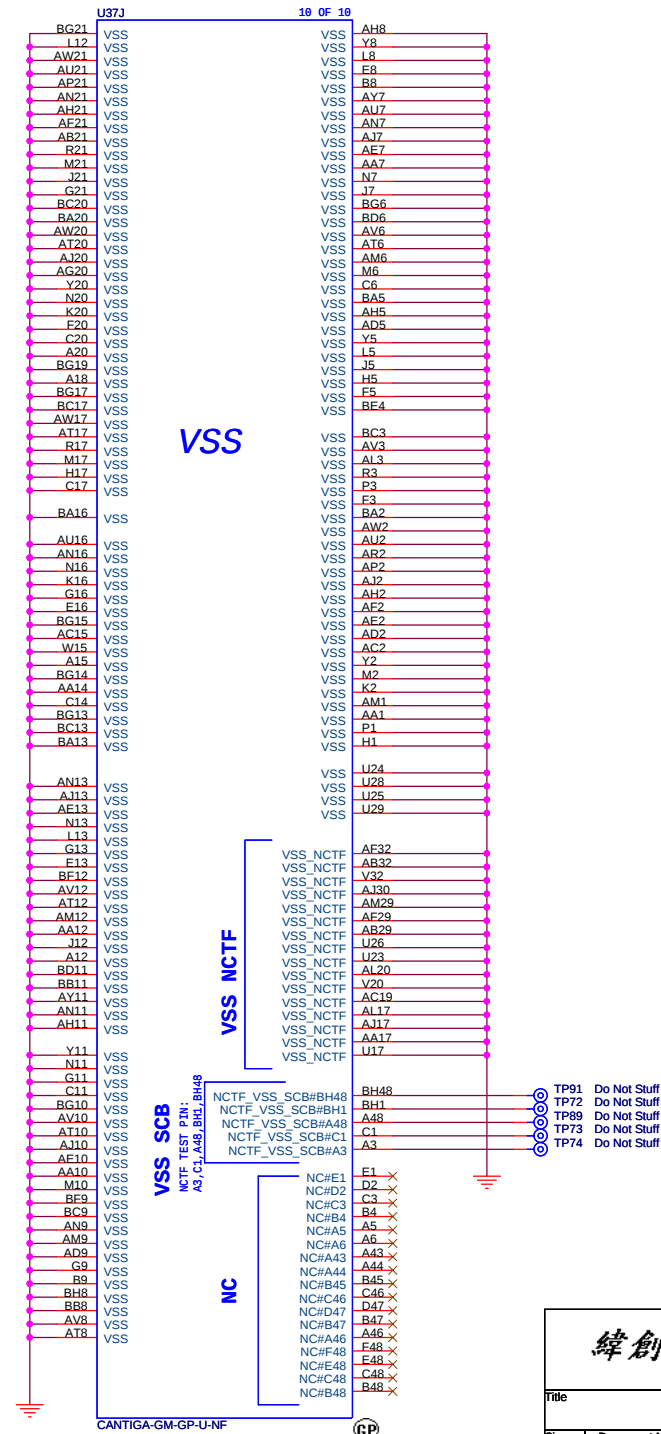
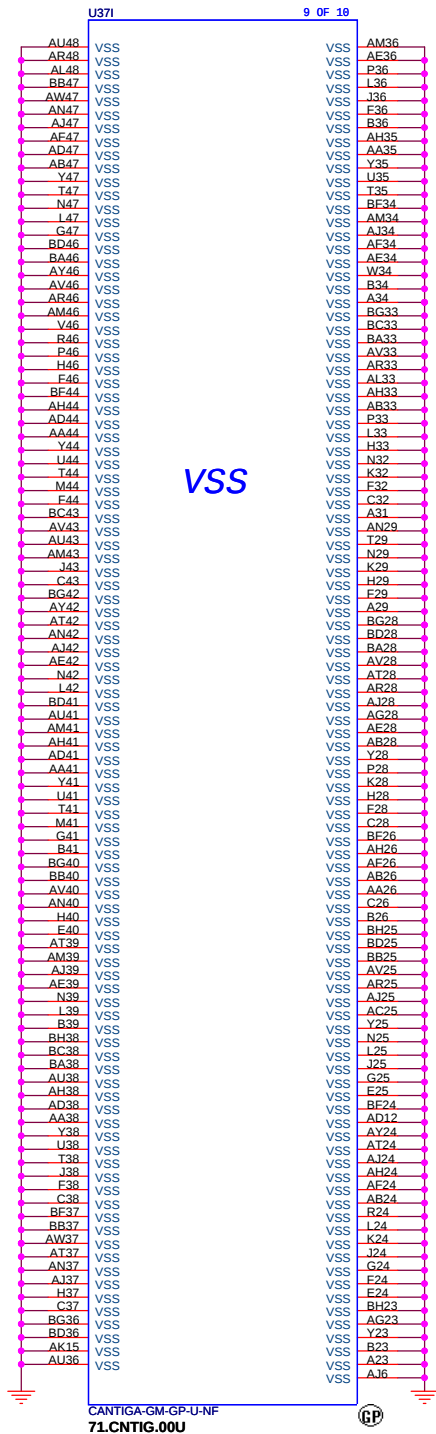
970

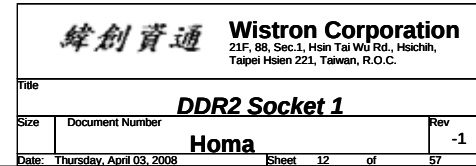
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.







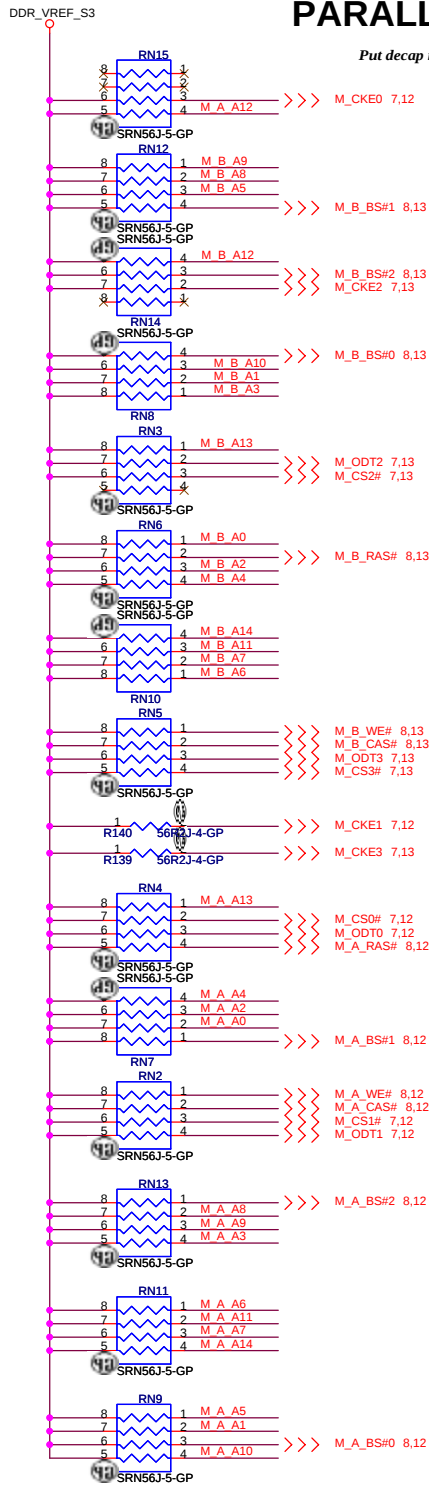






PARALLEL TERMINATION

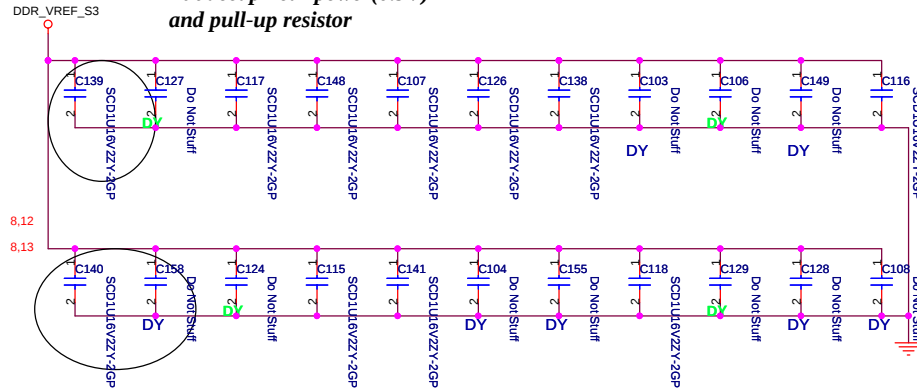
Put decap near power(0.9V) and pull-up resistor



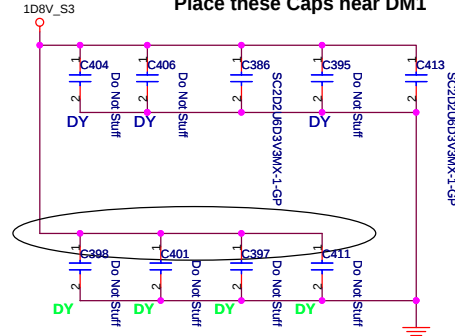
M_A A[14..0] << M_A_A[14..0] 8,12
M_B A[14..0] << M_B_A[14..0] 8,13

Decoupling Capacitor

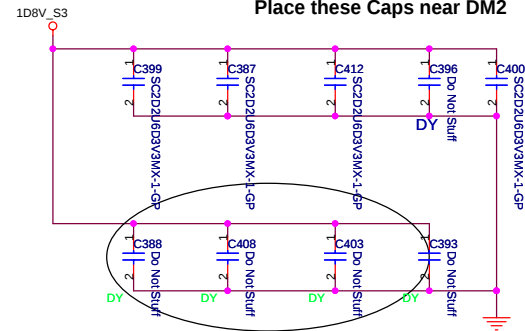
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



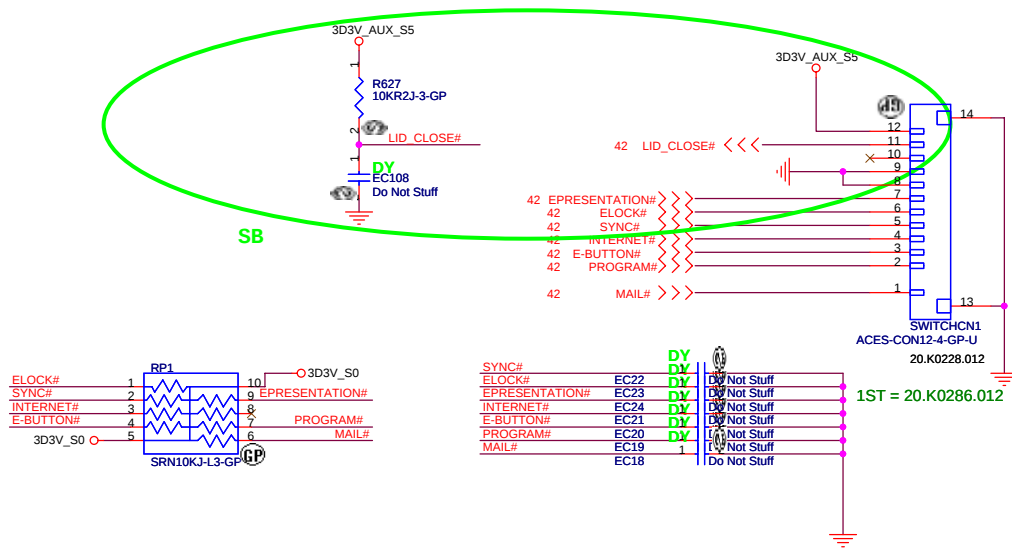
Place these Caps near DM2



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Title			
SWITCH			
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Date:	Thursday, April 03, 2008	Sheet 15 of	57



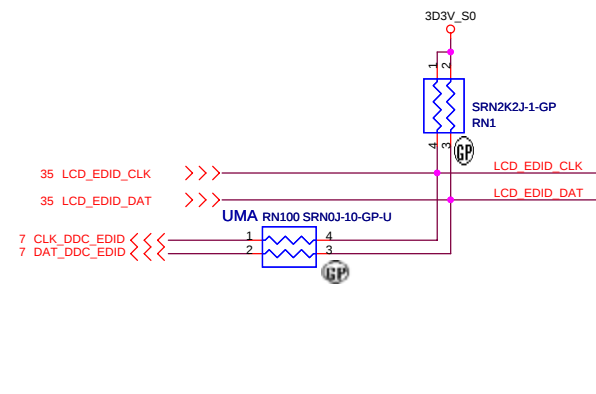
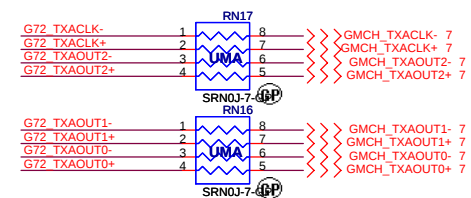
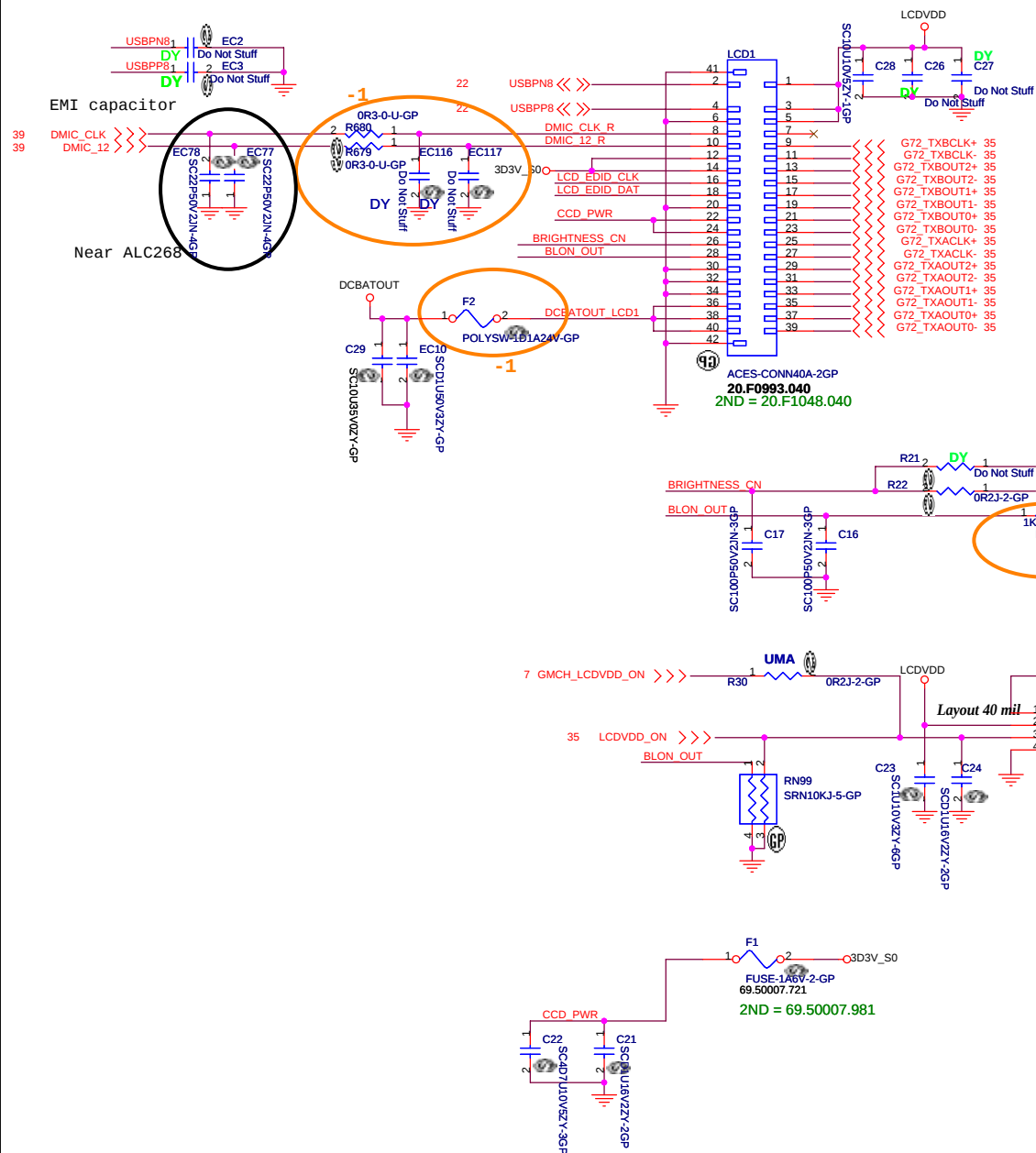
3D3V_AUX_S5	1	TP118	Do Not Stuff
LID_CLOSE#	1	TP121	Do Not Stuff
SYNC#	1	TP120	Do Not Stuff
ELOCK#	1	TP122	Do Not Stuff
EPRESENTATION#	1	TP124	Do Not Stuff
INTERNET#	1	TP123	Do Not Stuff
E-BUTTON#	1	TP126	Do Not Stuff
PROGRAM#	1	TP125	Do Not Stuff
MAIL#	1	TP127	Do Not Stuff

SYNC#	DY	Do Not Stuff
ELOCK#	EC22	Do Not Stuff
EPRESENTATION#	EC23	Do Not Stuff
INTERNET#	EC24	Do Not Stuff
E-BUTTON#	EC21	Do Not Stuff
PROGRAM#	EC20	Do Not Stuff
MAIL#	EC19	Do Not Stuff
	EC18	Do Not Stuff

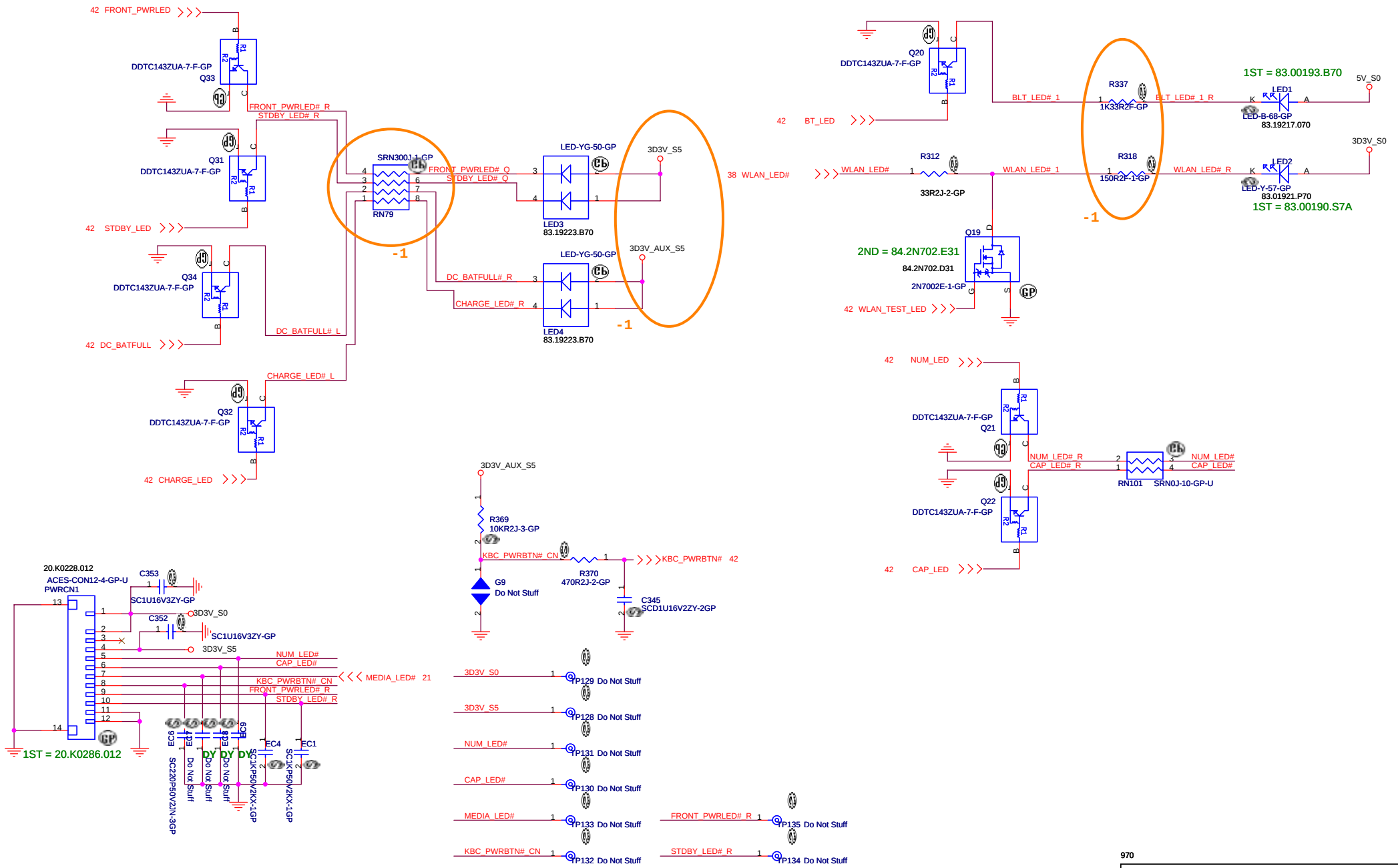
1ST = 20.K0286.012

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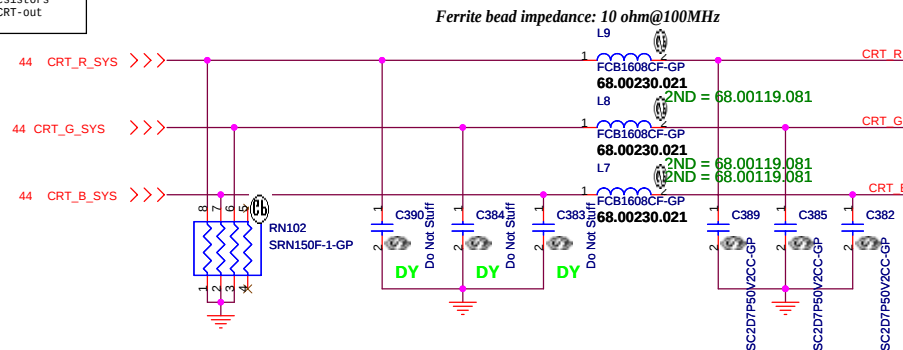
LCD/INVERTER/CCD CONN



LED



Layout Note:
Place these resistors
close to the CRT-out
connector



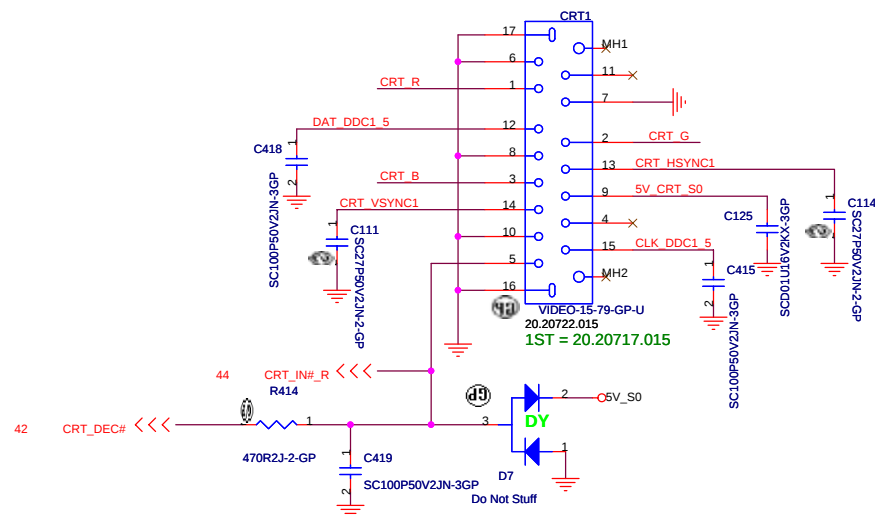
Ferrite bead impedance: 10 ohm@100MHz

Layout Note:

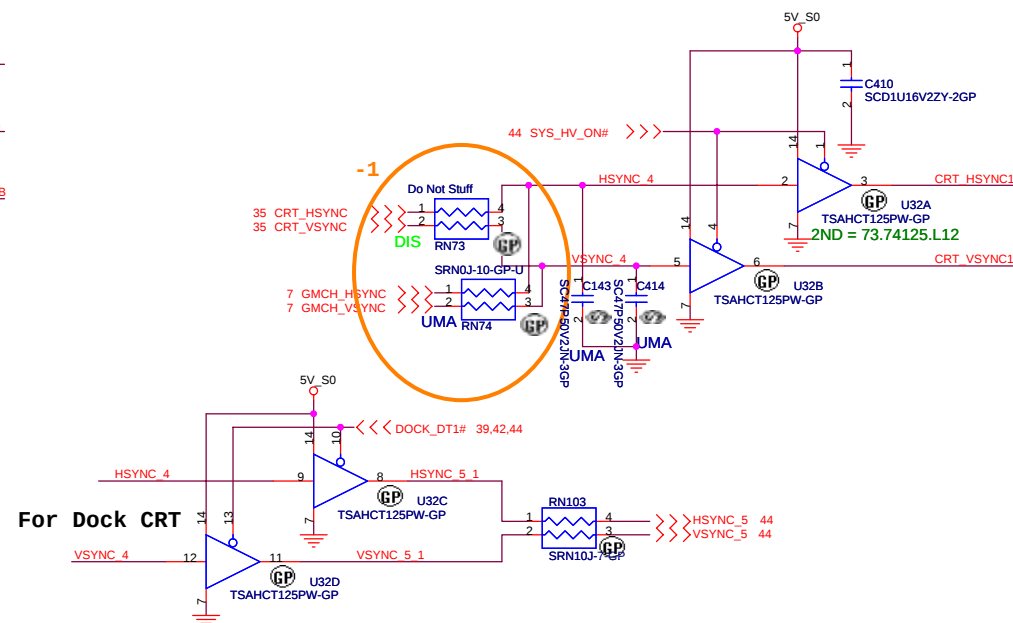
*** Must be a ground return path between this ground and the ground on the VGA connector.**

Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

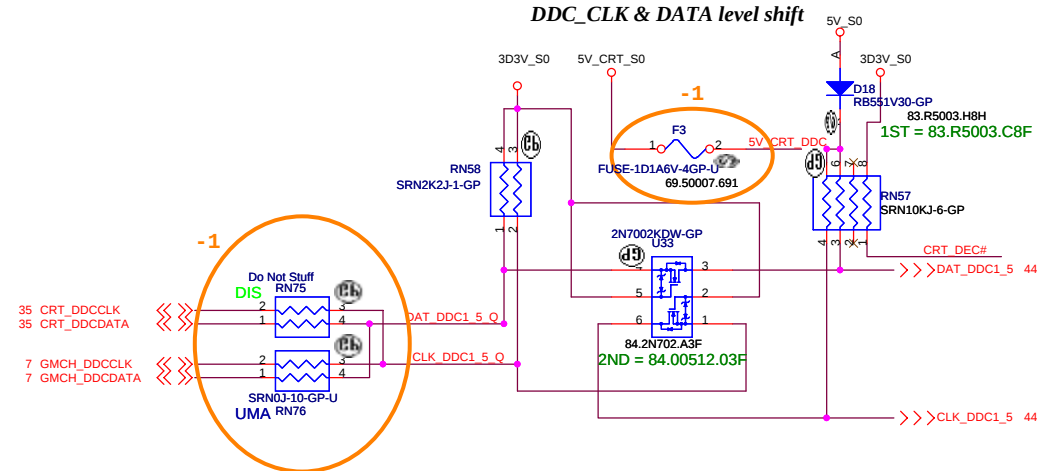
CRT I/F & CONNECTOR

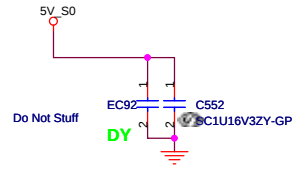
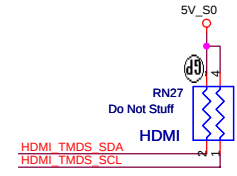
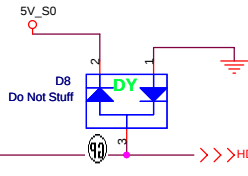
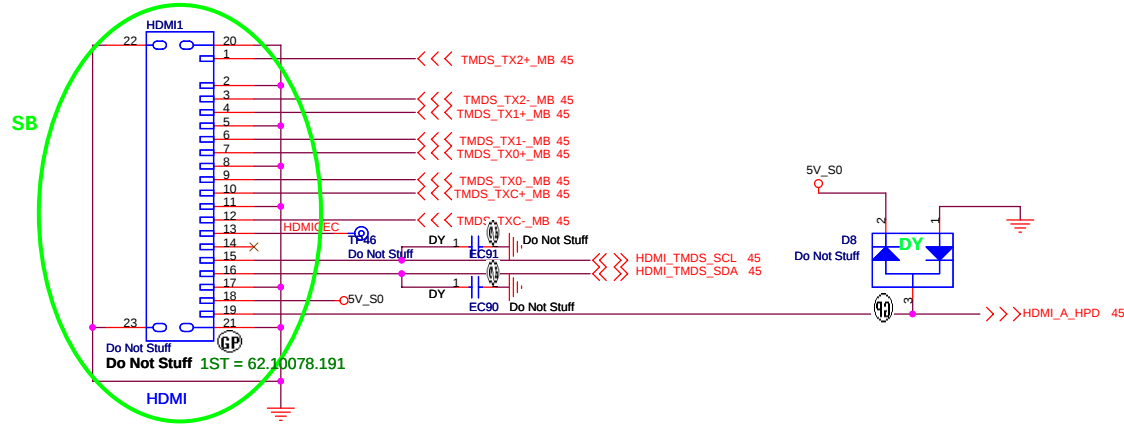


Hsync & Vsync level shift

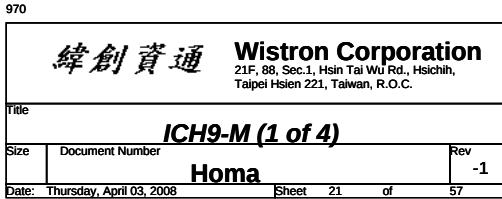


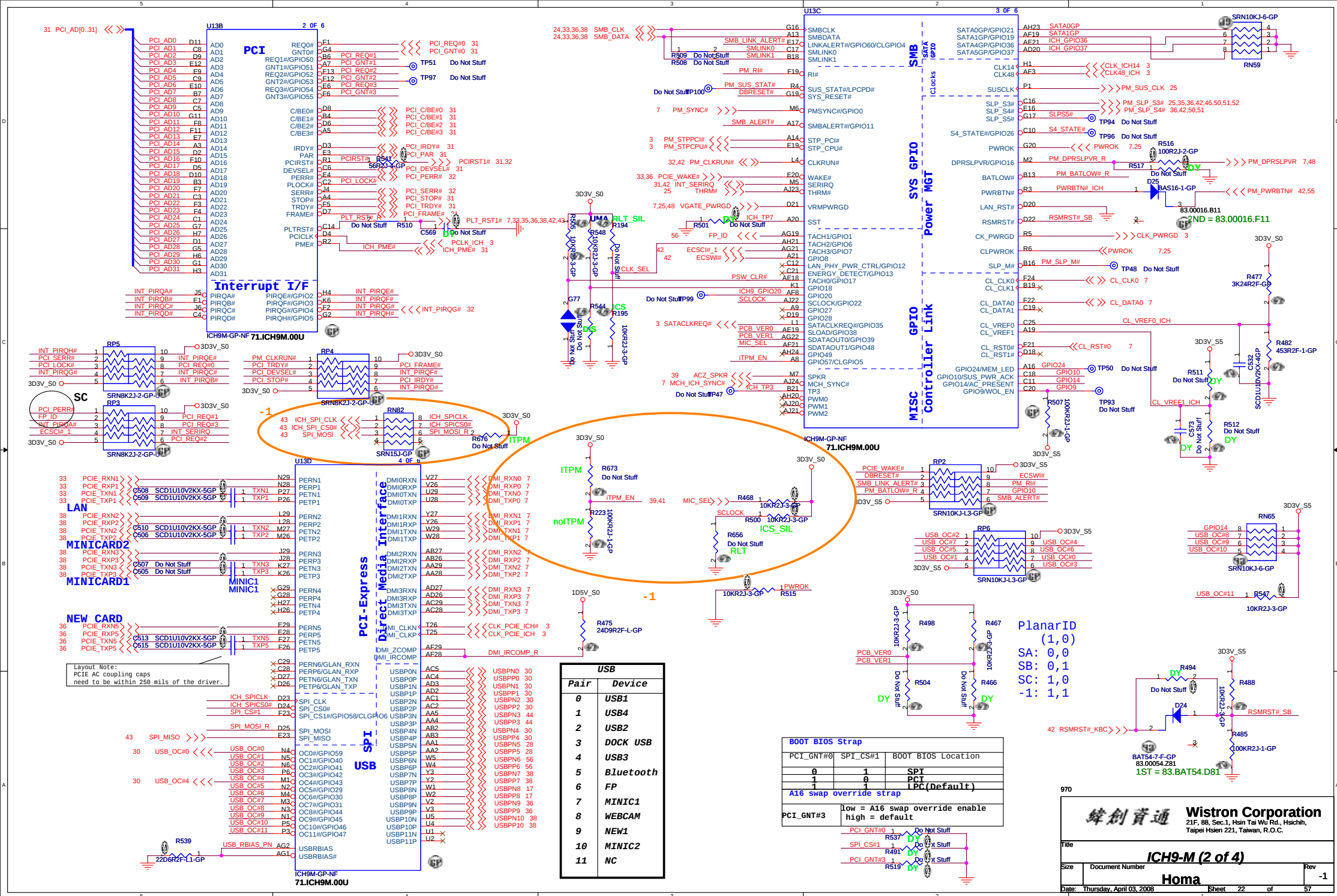
DDC_CLK & DATA level shift

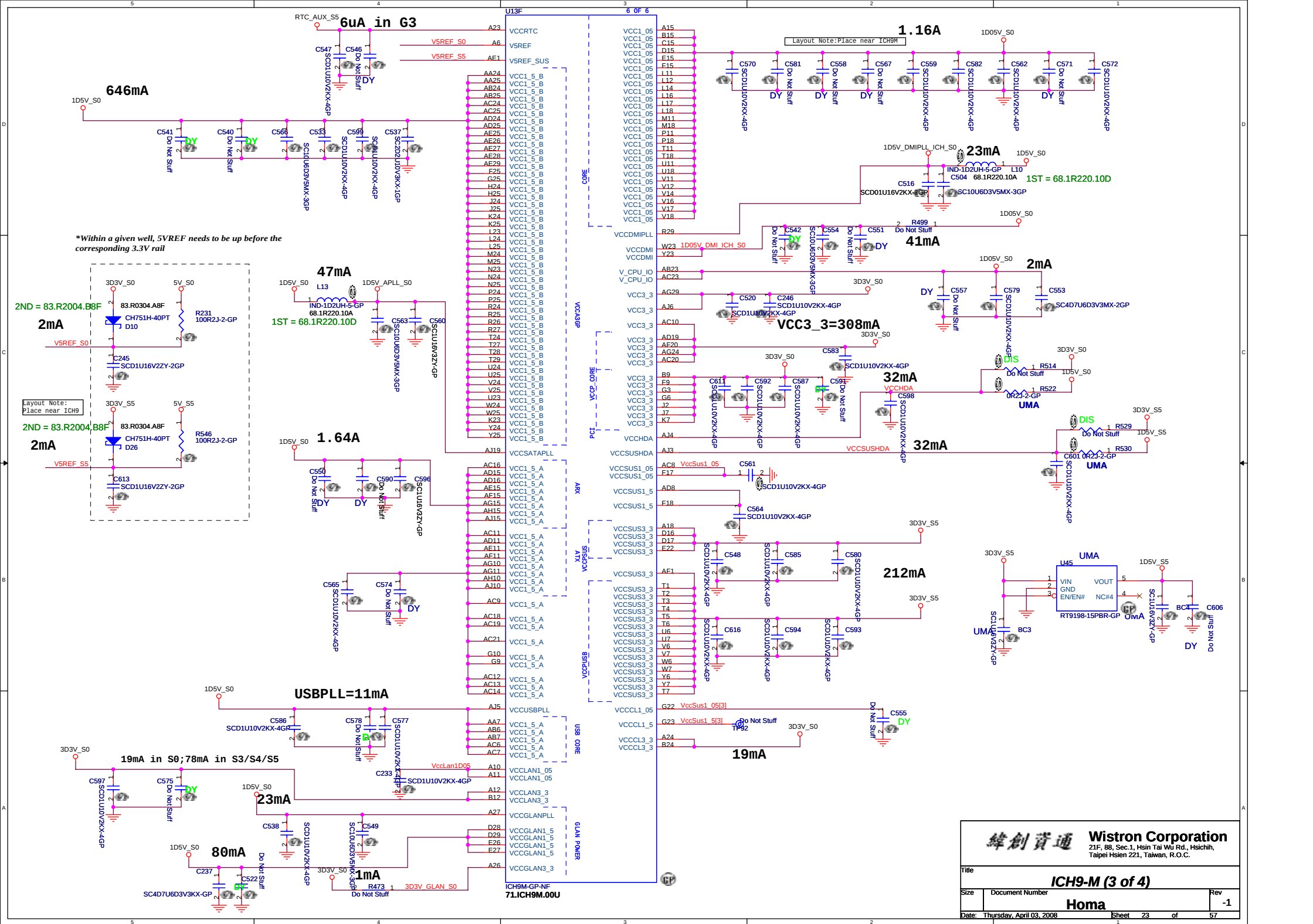


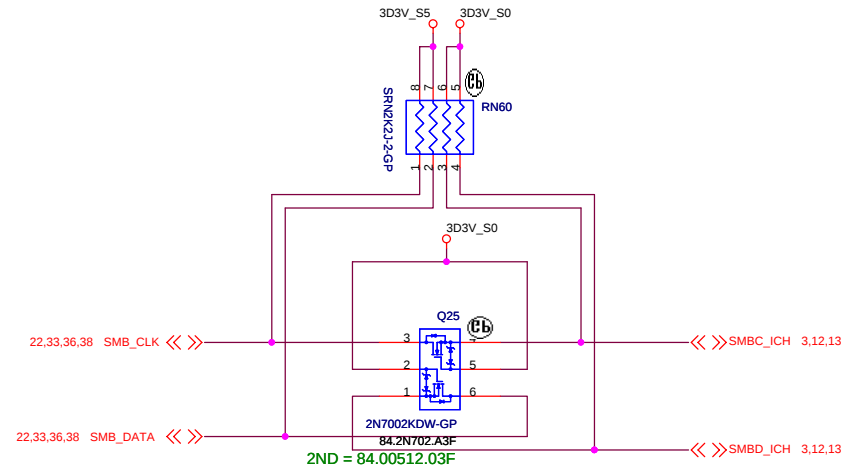


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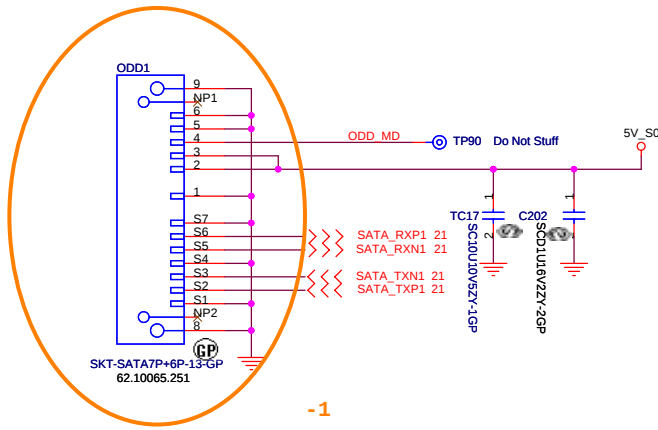






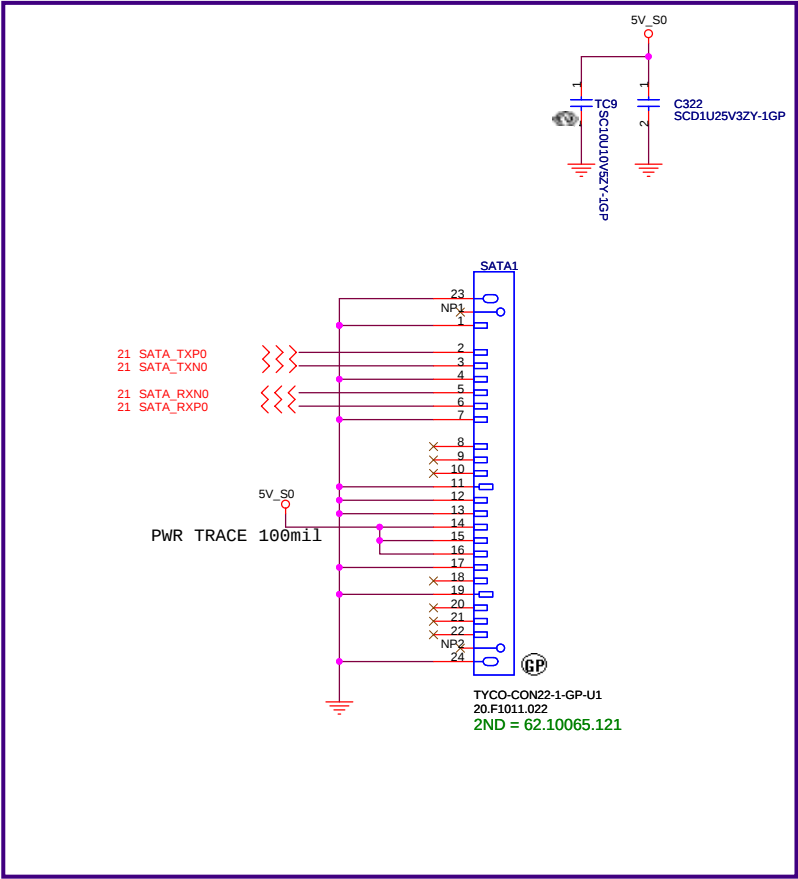
SMBUS

ODD Connector



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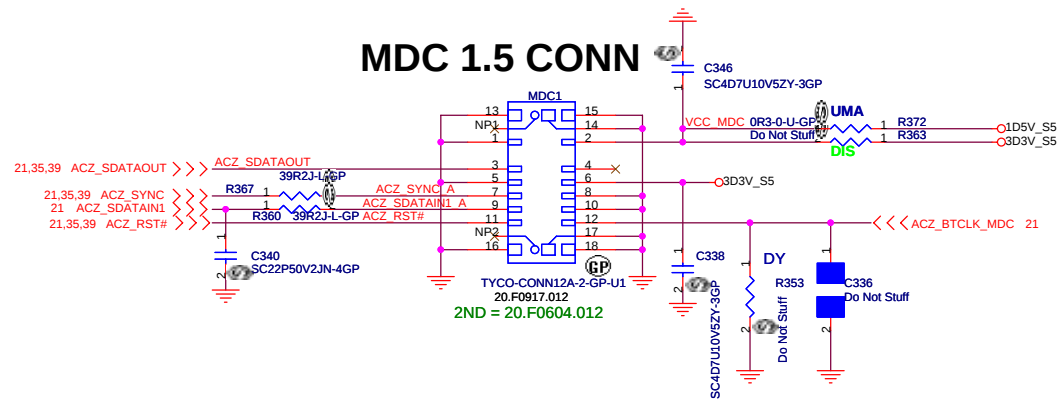
SATA Connector



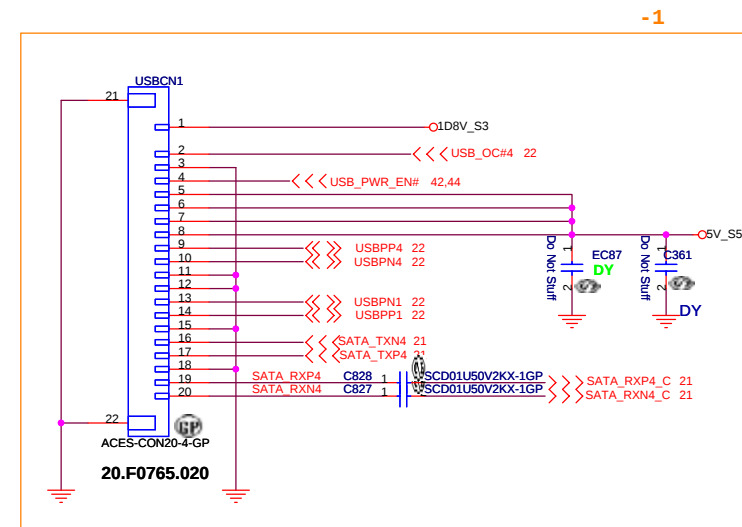
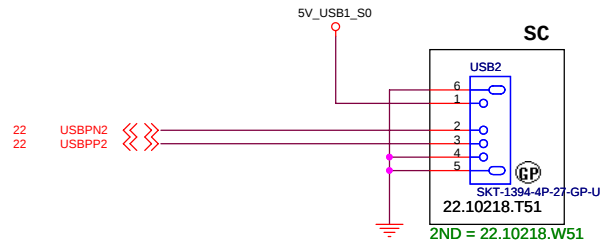
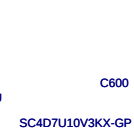
[illegible]

The diagram shows a USB to UART bridge IC (20.D0197.104) connected to a USB cable and a 3.3V BT module. The IC is a small blue component with pins labeled 1 through 5. Pin 1 is connected to the 3.3V BT module. Pin 2 is connected to the USB D+ line (labeled USBPN5). Pin 3 is connected to the USB D- line (labeled USBPP5). Pin 4 is connected to the USB VCC line (labeled 3D3V_BT S0). Pin 5 is connected to the USB GND line. The IC is also connected to a 3.3V BT module (labeled 20.F0984.004) via a 10k pull-up resistor (labeled ACES-CON4-1-GP-U2) connected to pin 1. The 3.3V BT module is connected to the USB D+ and D- lines (labeled 22).

Device	Port	TP	Notes
3D3V BT S0	1	TP139	Do Not Stuff
USBPN5	1	TP212	Do Not Stuff
USBPP5	1	TP213	Do Not Stuff



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22 PCI_AD[0..31]

<<<

- PCI_AD0 64
- PCI_AD1 63
- PCI_AD2 62
- PCI_AD3 61
- PCI_AD4 60
- PCI_AD5 59
- PCI_AD6 58
- PCI_AD7 57
- PCI_AD8 54
- PCI_AD9 53
- PCI_AD10 52
- PCI_AD11 51
- PCI_AD12 50
- PCI_AD13 49
- PCI_AD14 47
- PCI_AD15 46
- PCI_AD16 37
- PCI_AD17 36
- PCI_AD18 35
- PCI_AD19 34
- PCI_AD20 32
- PCI_AD21 31
- PCI_AD22 30
- PCI_AD23 29
- PCI_AD24 27
- PCI_AD25 25
- PCI_AD26 24
- PCI_AD27 23
- PCI_AD28 22
- PCI_AD29 21
- PCI_AD30 20
- PCI_AD31 19

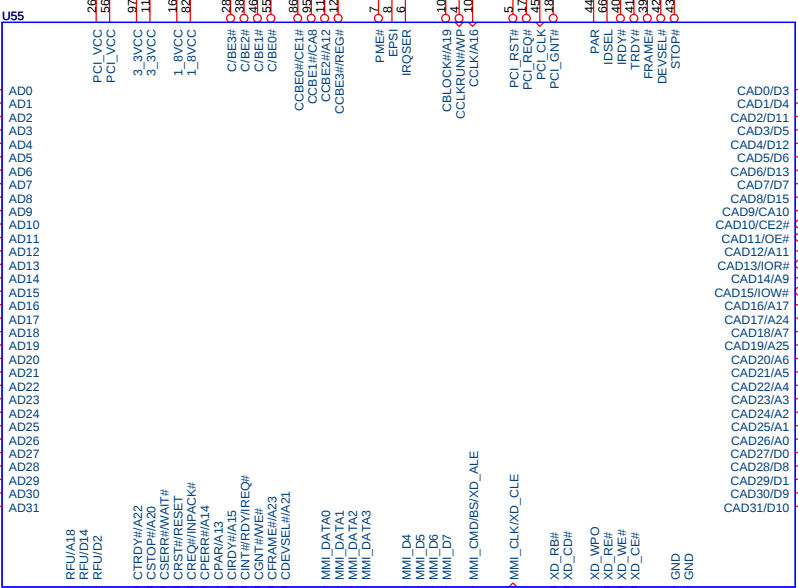
OZ711MZ0TN-GP-U1
71.00711.A0G

37 CBB_A18

37 CBB_D14

37 CBB_D2

- CBB_A22 37
- CBB_A20 37
- CBB_WAIT# 37
- CBB_RESET 37
- CBB_INPACK# 37
- CBB_A14 37
- CBB_A13 37
- CBB_A15 37
- CBB_RDY 37
- CBB_WE# 37
- CBB_A23 37
- CBB_A21 37
- MMI_D0 32
- MMI_D1 32
- MMI_D2 32
- MMI_D3 32

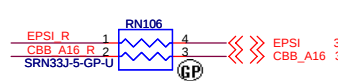


- CAD0/D3 76
- CAD1/D4 77
- CAD2/D11 78
- CAD3/D5 79
- CAD4/D12 80
- CAD5/D6 81
- CAD6/D13 83
- CAD7/D7 84
- CAD8/D15 87
- CAD9/CA10 88
- CAD10/CE2# 89
- CAD11/OE# 90
- CAD12/A11 91
- CAD13/IOR# 92
- CAD14/A9 93
- CAD15/IOW# 94
- CAD16/A17 96
- CAD17/A24 112
- CAD18/A7 113
- CAD19/A25 114
- CAD20/A6 115
- CAD21/A5 116
- CAD22/A4 118
- CAD23/A3 120
- CAD24/A2 122
- CAD25/A1 124
- CAD26/A0 125
- CAD27/D0 126
- CAD28/D8 127
- CAD29/D1 128
- CAD30/D9 1
- CAD31/D10 3

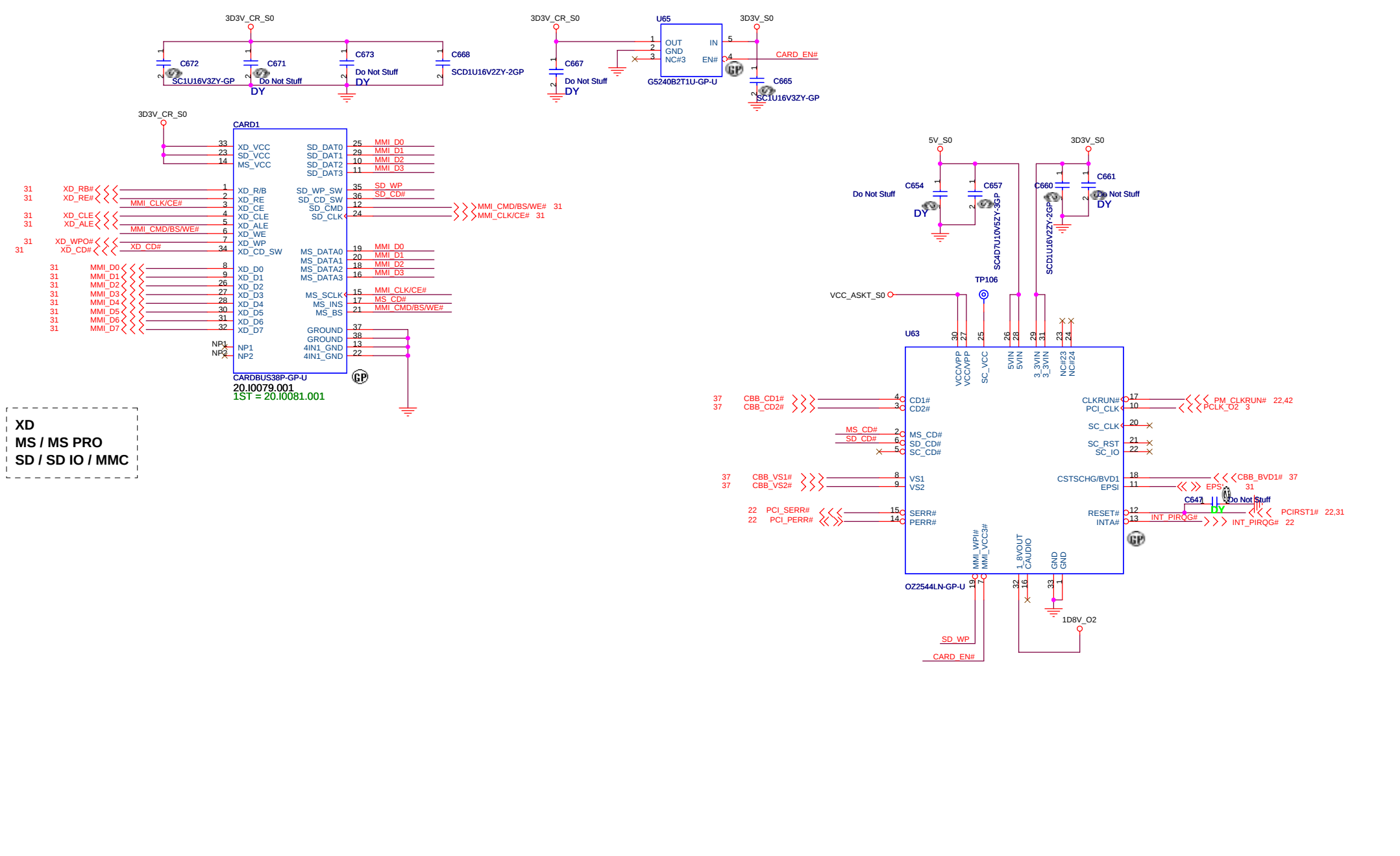
- CBB_D3 37
- CBB_D4 37
- CBB_D11 37
- CBB_D5 37
- CBB_D12 37
- CBB_D6 37
- CBB_D13 37
- CBB_D7 37
- CBB_D15 37
- CBB_A10 37
- CBB_CE2# 37
- CBB_OE# 37
- CBB_A11 37
- CBB_IORD# 37
- CBB_A9 37
- CBB_IOWR# 37
- CBB_A17 37
- CBB_A24 37
- CBB_A7 37
- CBB_A25 37
- CBB_A6 37
- CBB_A5 37
- CBB_A4 37
- CBB_A3 37
- CBB_A2 37
- CBB_A1 37
- CBB_A0 37
- CBB_D0 37
- CBB_D8 37
- CBB_D1 37
- CBB_D9 37
- CBB_D10 37

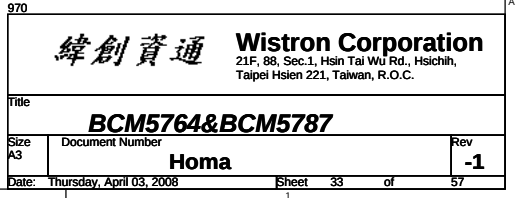
- MMI_DATA0 9
- MMI_DATA1 10
- MMI_DATA2 12
- MMI_DATA3 13
- MMI_D4 75
- MMI_D5 74
- MMI_D6 73
- MMI_D7 72
- MMI_CMD/BS/XD_ALE 14
- MMI_CLK/XD_CLE 15
- XD_RE# 68
- XD_CD# 66
- XD_WPO# 67
- XD_RE# 69
- XD_WE# 70
- XD_CE# 71
- GND 108
- GND 33

- <<< XD_ALE 32
- <<< XD_CLE 32
- <<< XD_RE# 32
- <<< XD_WPO# 32
- <<< XD_CD# 32
- <<< XD_RB# 32
- <<< MMI_CLK/CE# 32
- <<< MMI_CMD/BS/WE# 32
- <<< MMI_D7 32
- <<< MMI_D6 32
- <<< MMI_D5 32
- <<< MMI_D4 32



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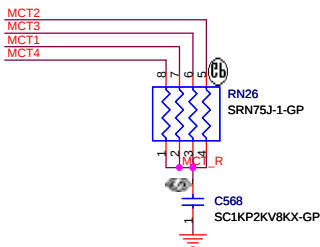
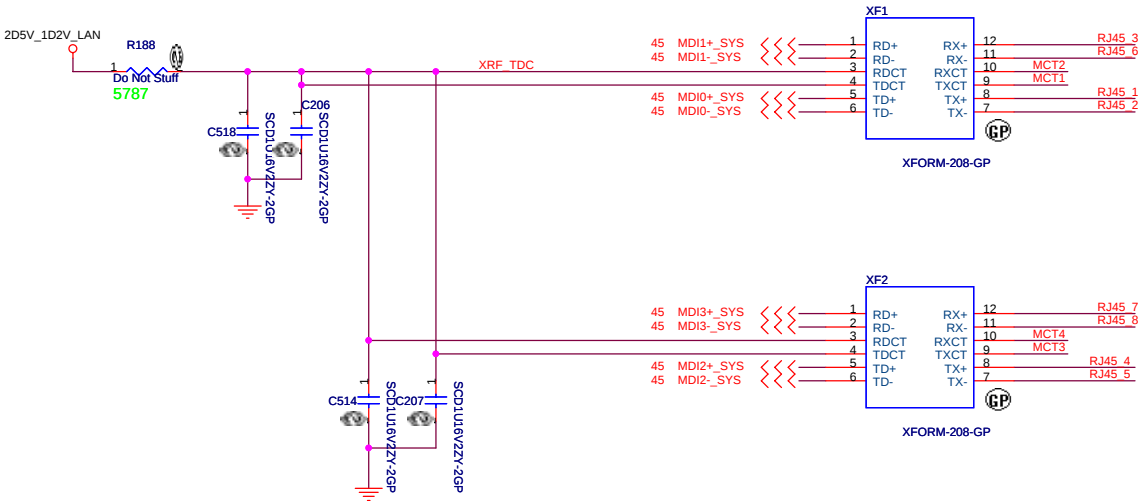




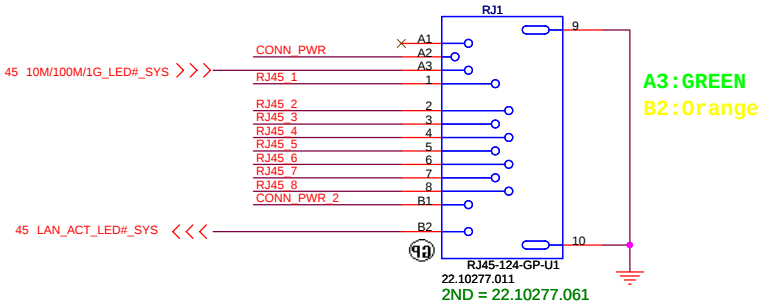
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

LAN Connector

GIGA Lan Transformer

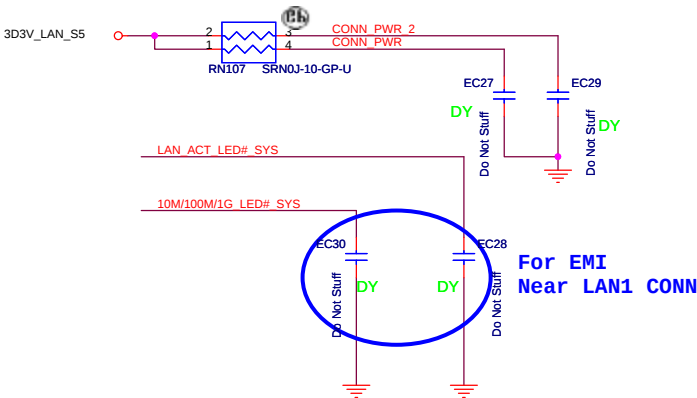


LAN Connector

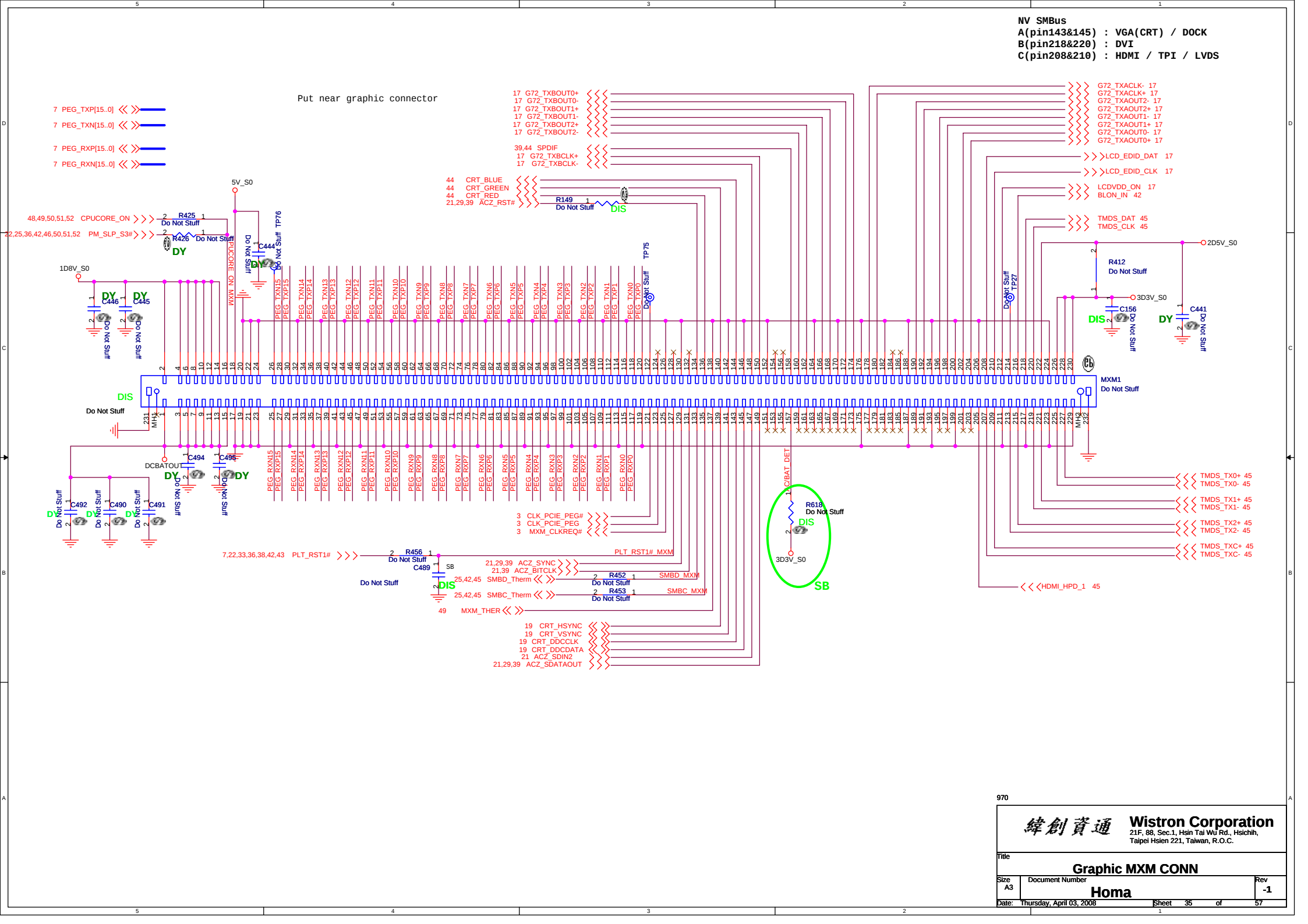


LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transferring data.

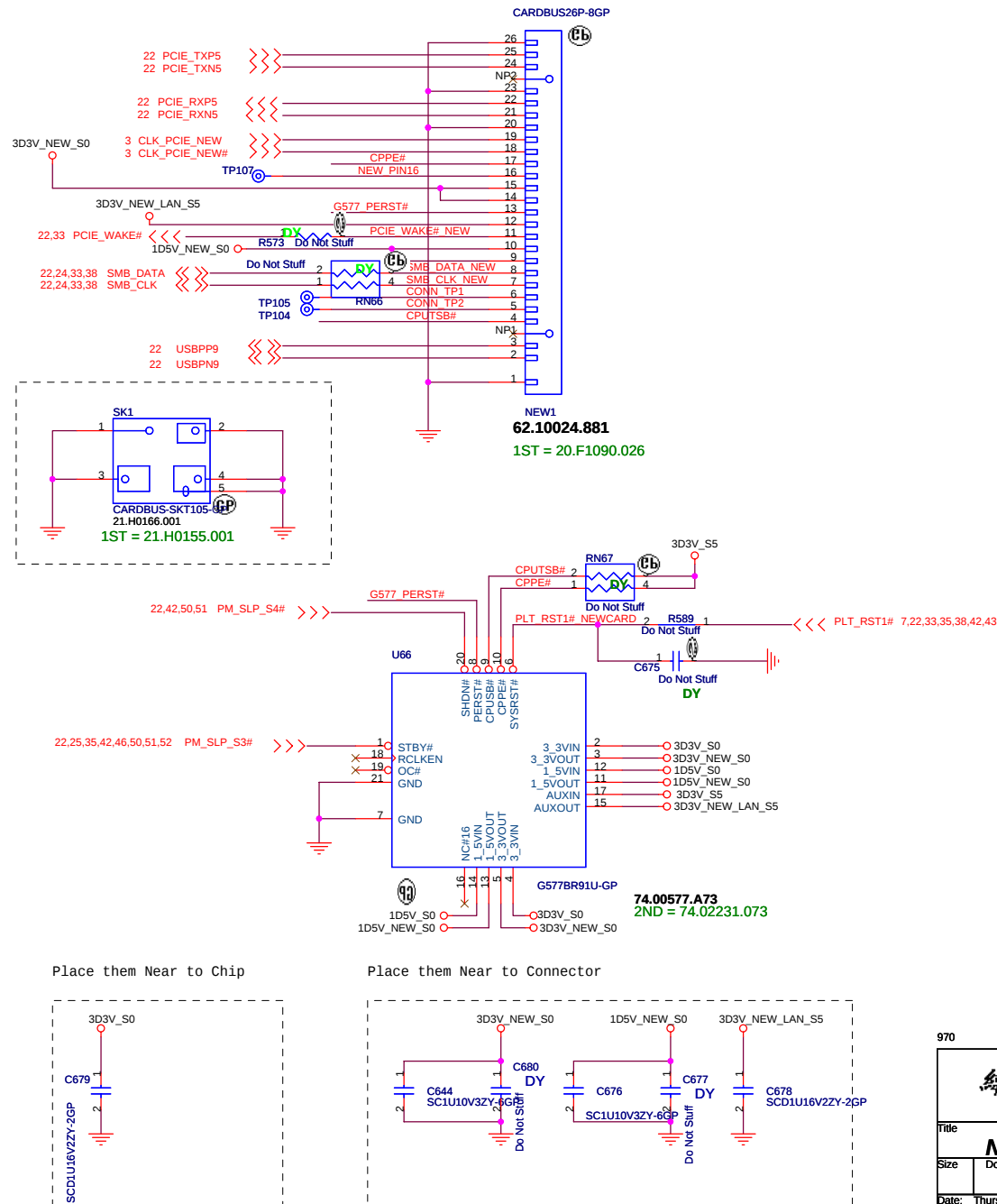


For EMI Near LAN1 CONN



NEWCARD Connector

Reserve the symbol
for bottom side
connector



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PCMCIA Socket

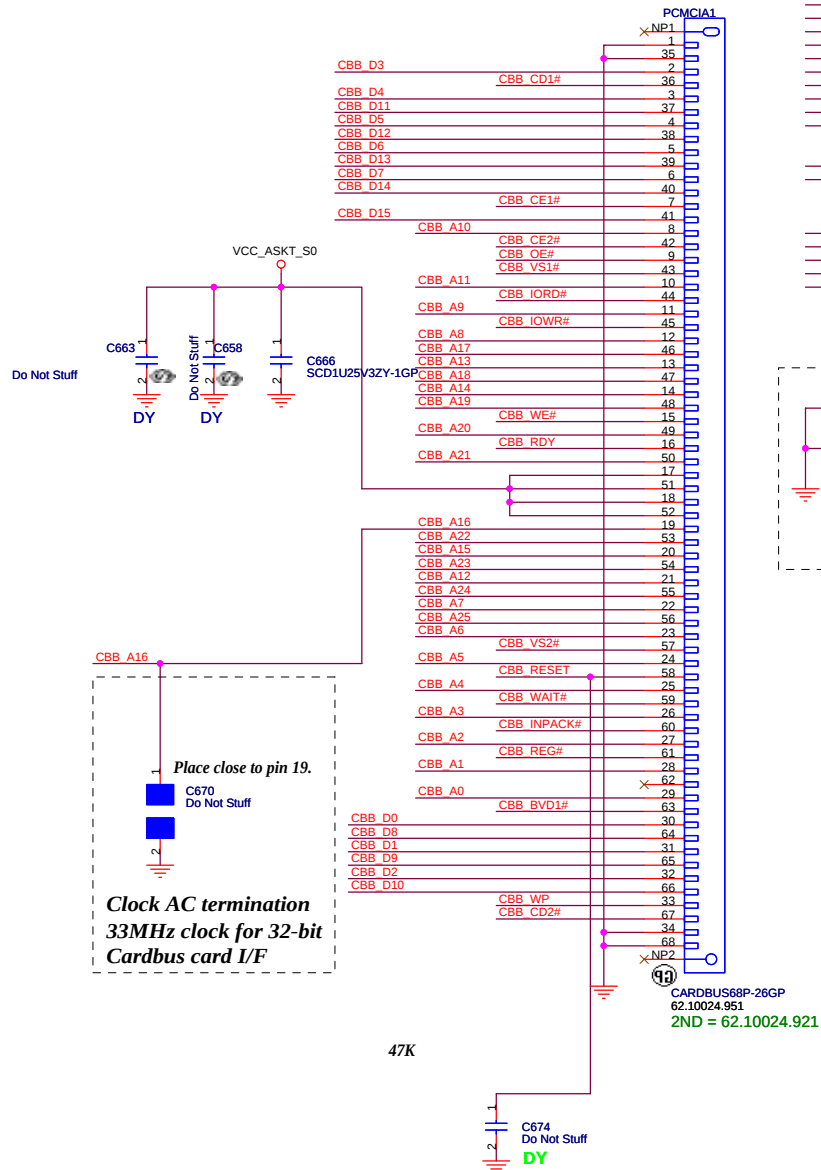
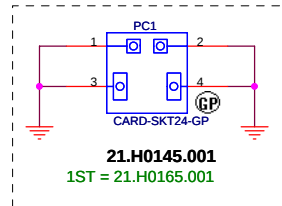
Cardbus I/F

CBB_D[15..0] << CBB_D[15..0] 31
CBB_A[25..0] << CBB_A[25..0] 31

CBB_IORD# 31
CBB_IOWR# 31
CBB_OE# 31
CBB_WE# 31
CBB_REG# 31
CBB_RDY 31
CBB_WP 31
CBB_RESET# 31
CBB_WAIT# 31
CBB_INPACK# 31

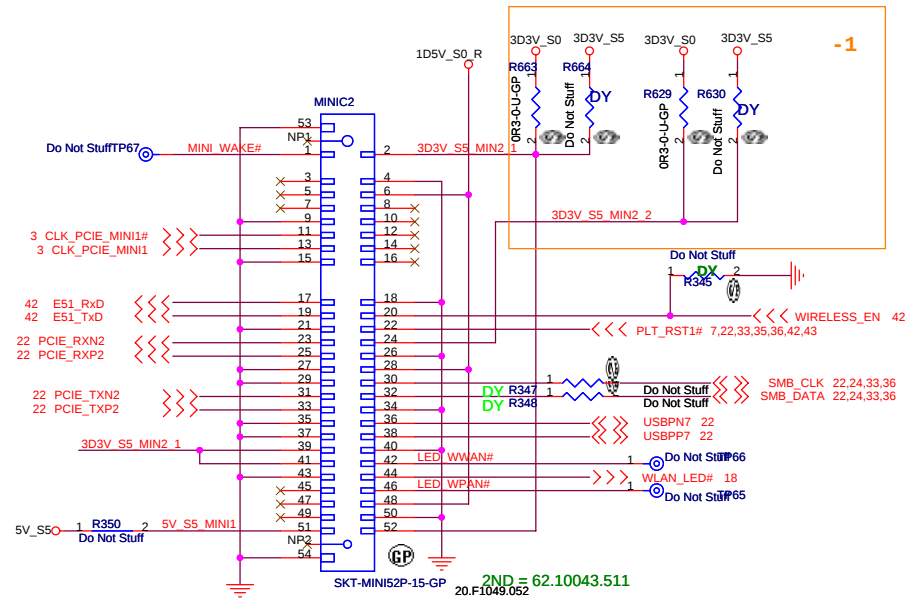
CBB_CE1# 31
CBB_CE2# 31

CBB_CD1# 32
CBB_CD2# 32
CBB_VS1# 32
CBB_VS2# 32
CBB_BVD1# 32

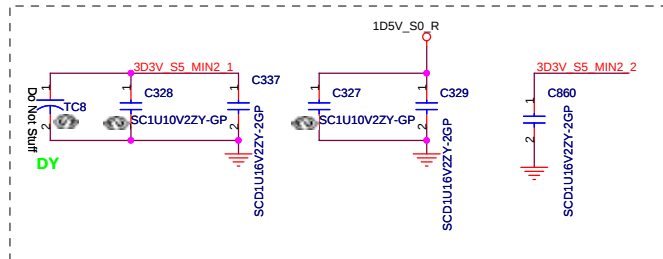


970

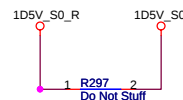
Mini Card Connector(WLAN)



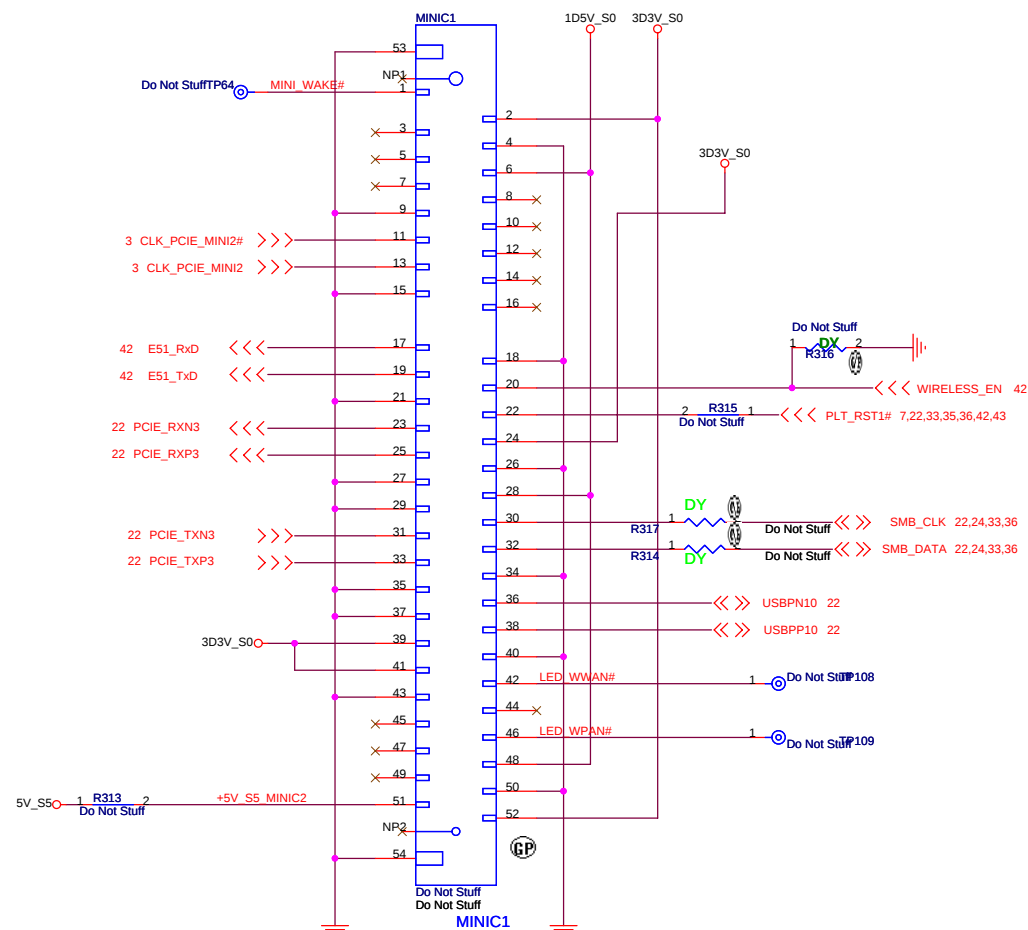
Place near MINIC2



Vo(cal.)=1.5024V OCP>3.2A

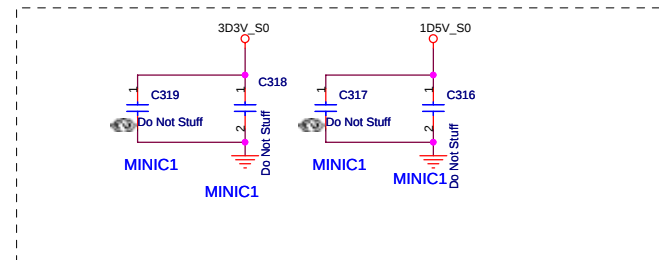


Mini Card Connector



1ST = 20.F1084.052

Place near MINIC1



970

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Title

MINI CARD

Size

	Document Number
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Homa

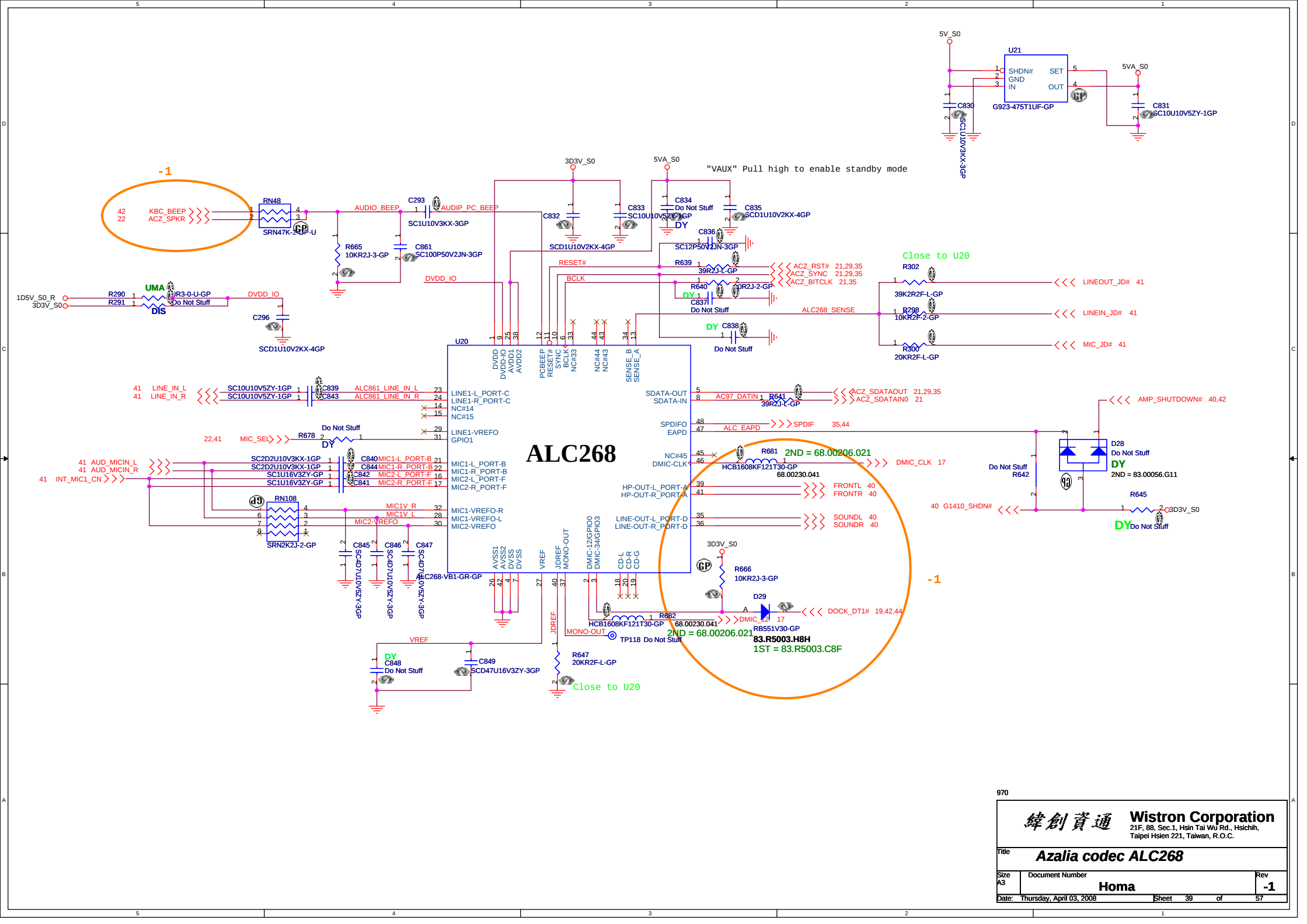
Date: Thursday, April 03, 2008

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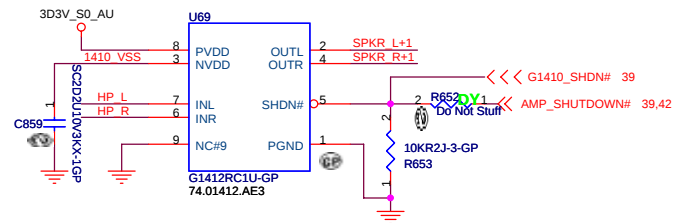
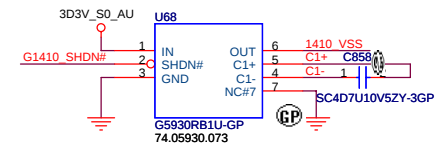
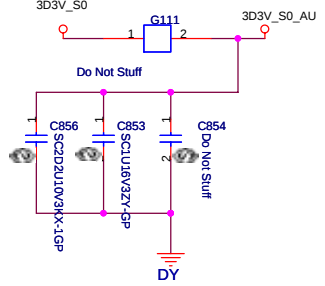
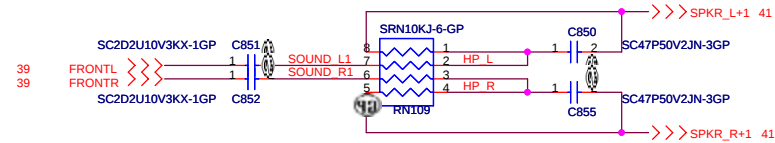
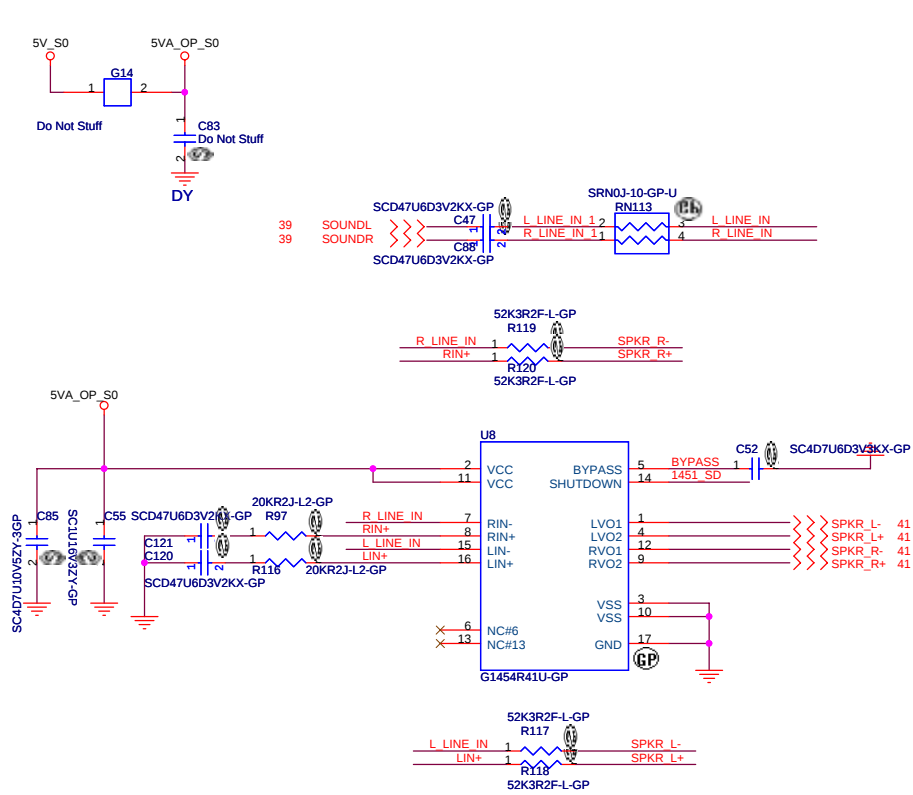
Rev

1

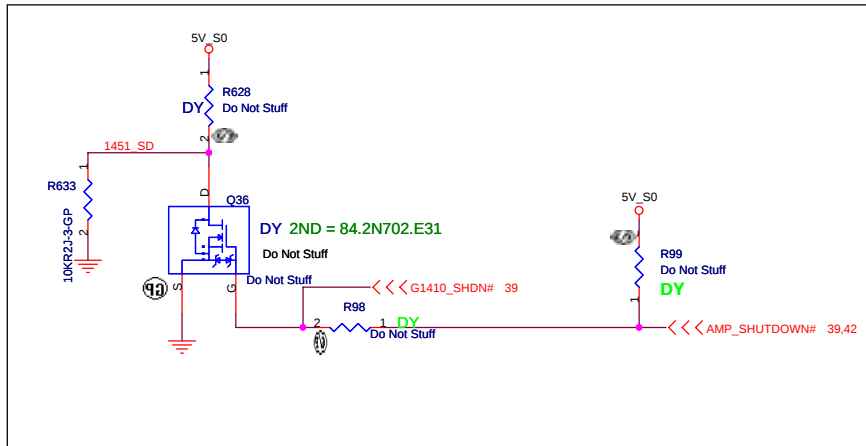
57



AUDIO OP AMPLIFIER

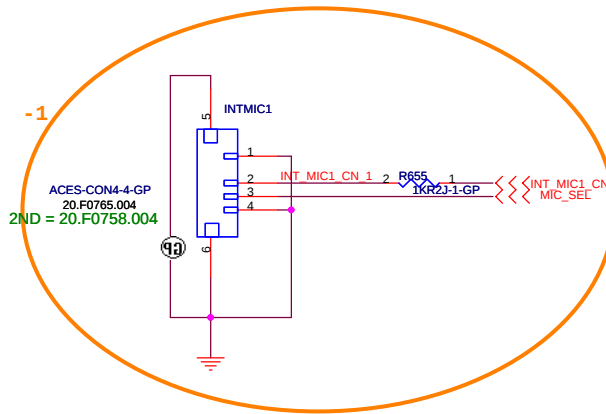
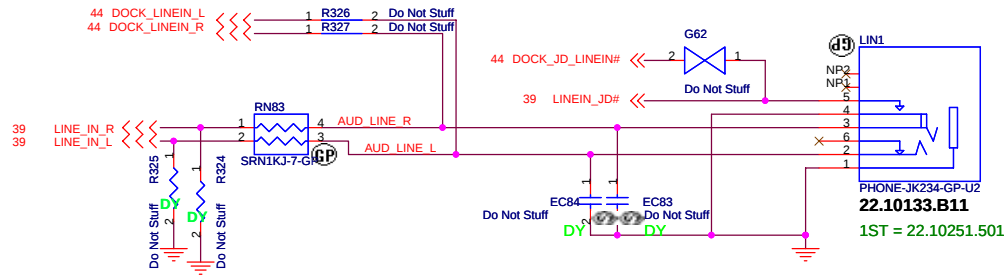


SC

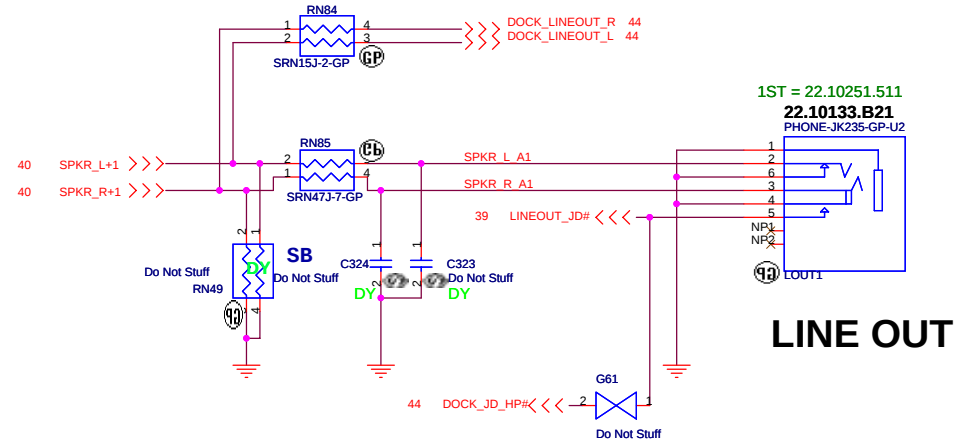
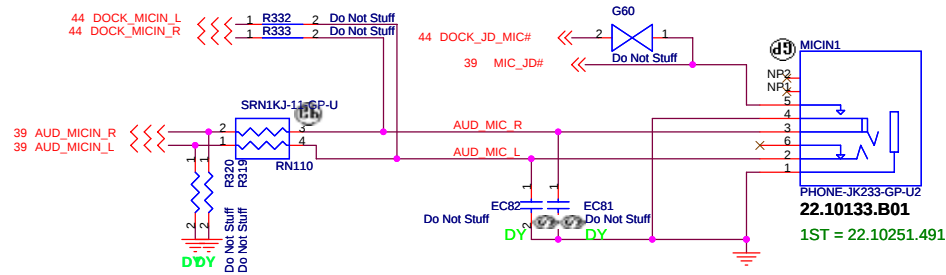


970

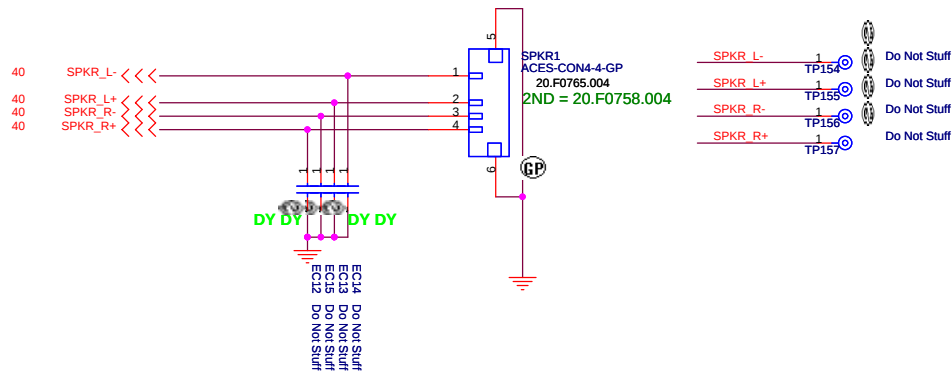
LINE IN



MIC IN



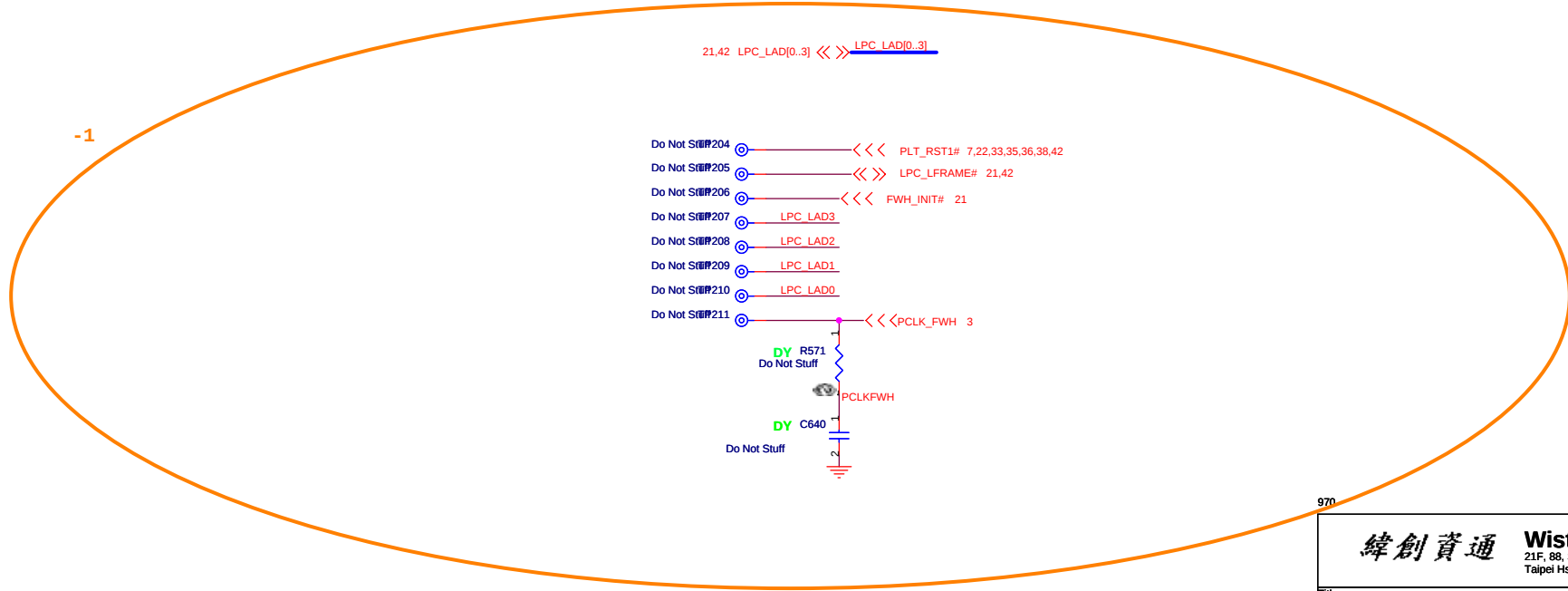
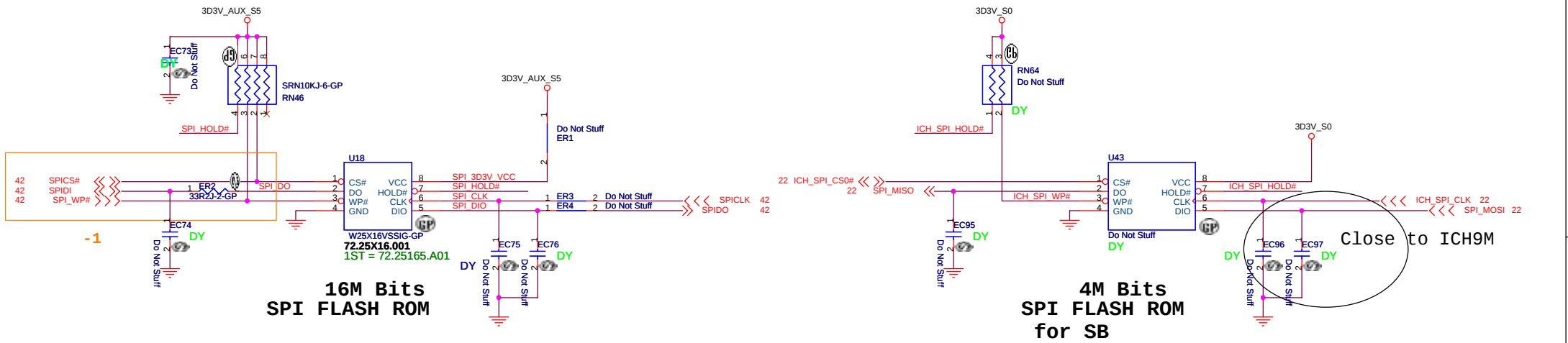
Internal Speaker



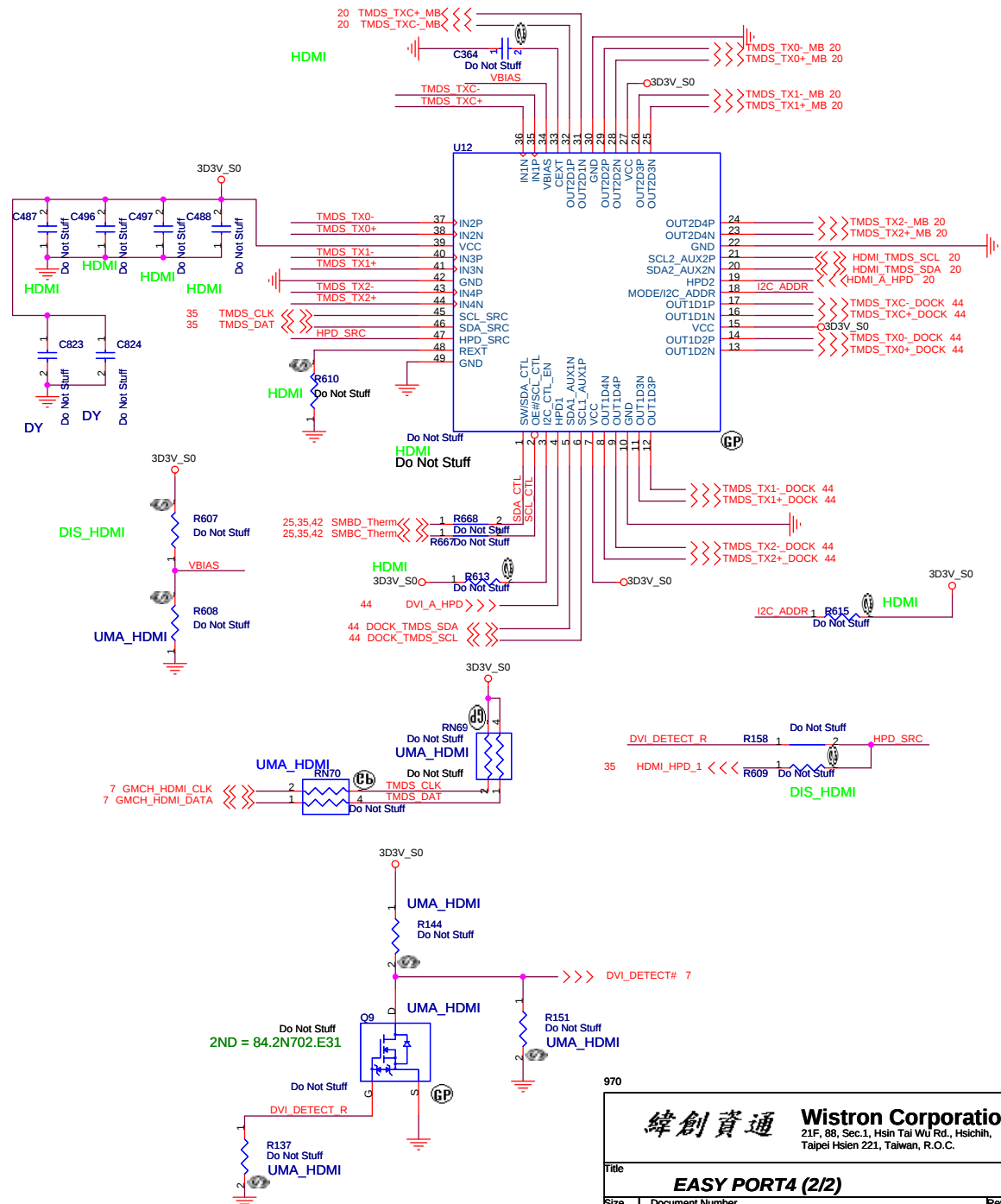
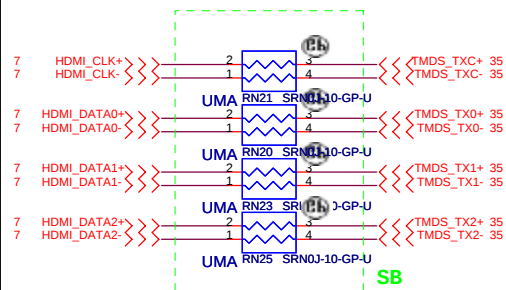
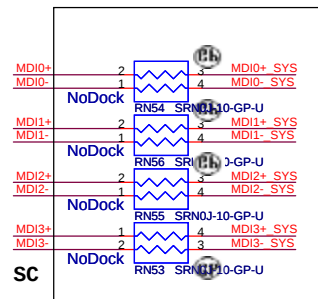
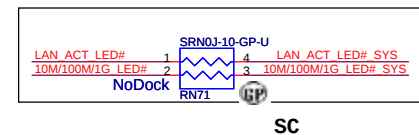
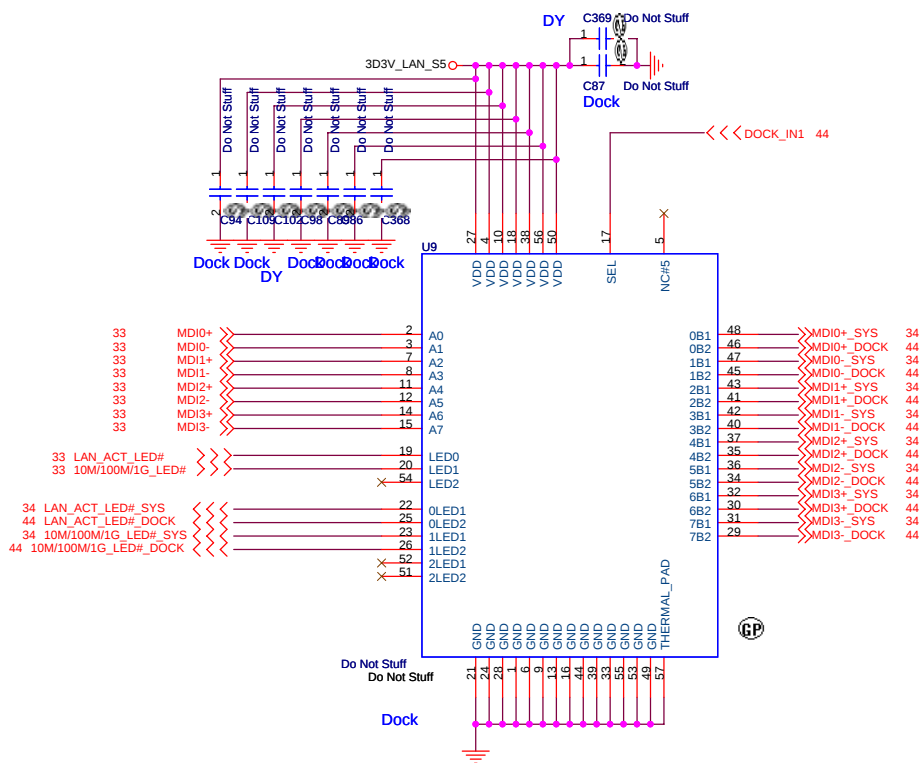
970

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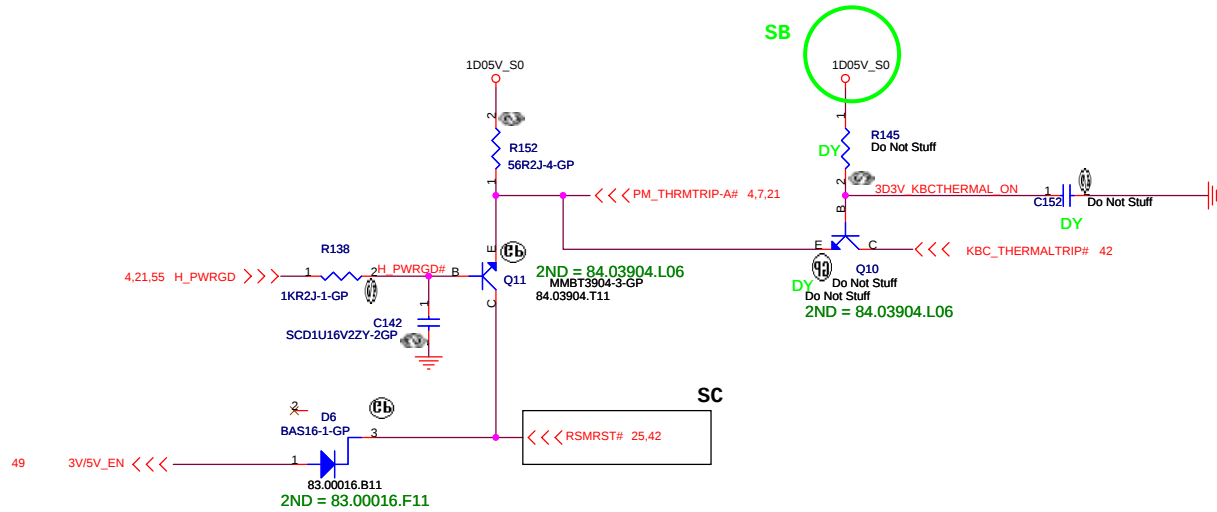
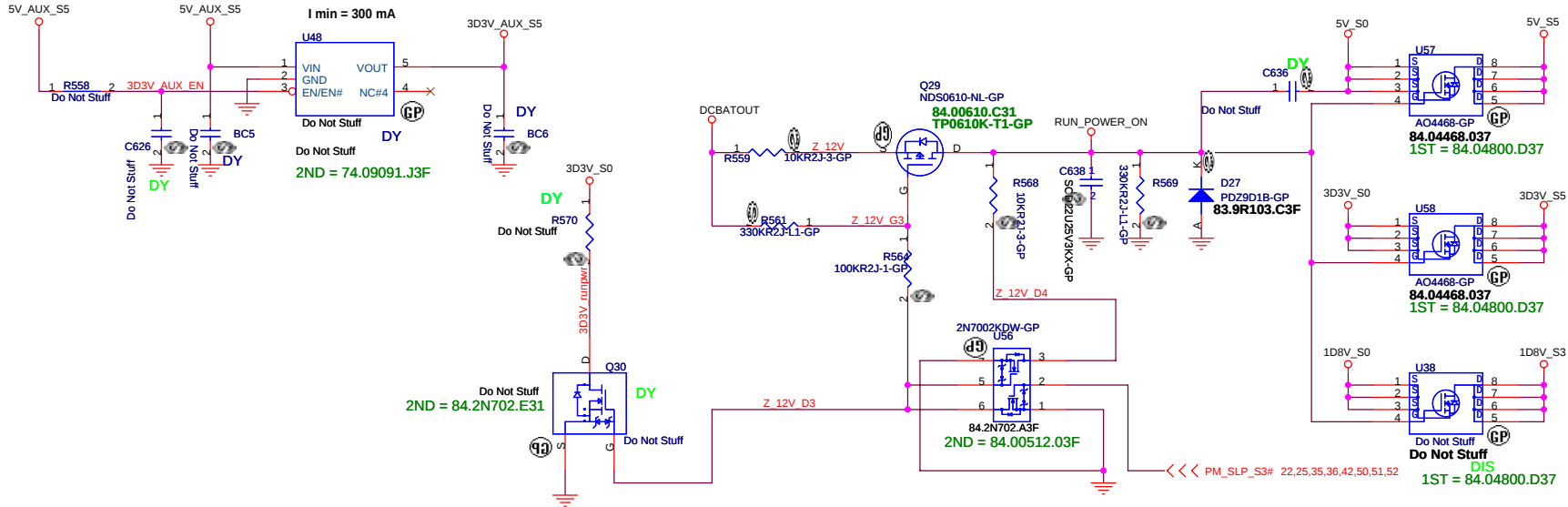
LAN switch



Aux Power

3D3V_AUX_S5

Run Power



970

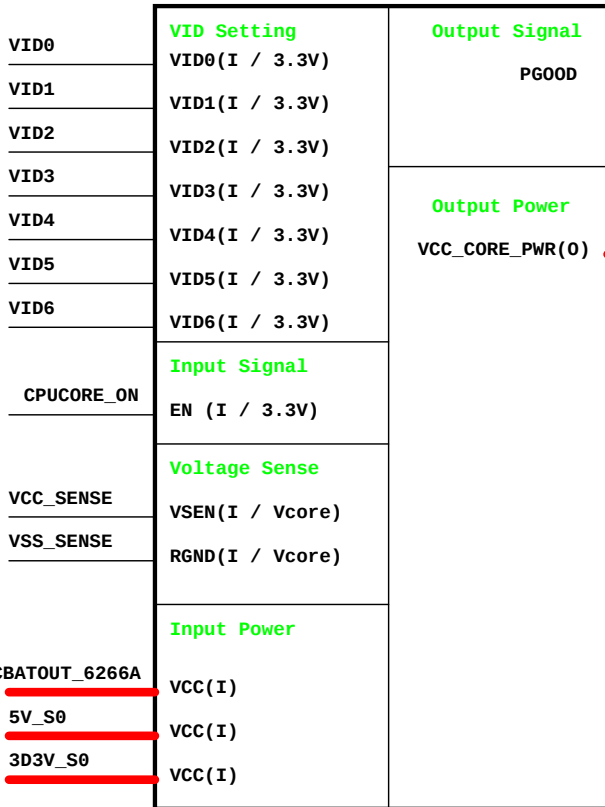
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Taipei Hsien 221, Taiwan, R.O.C.

Title	<i>RUN POWER and 3D3V_AUX_S5</i>
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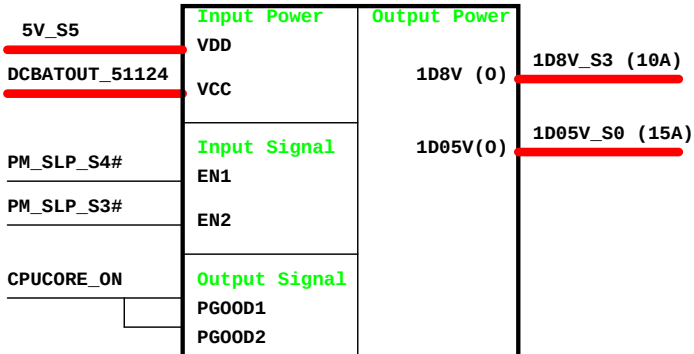
Size	Document Number	Rev
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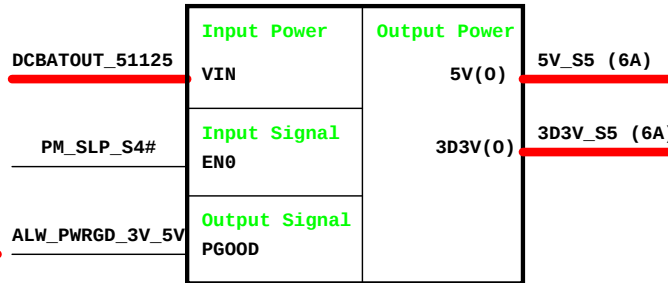
CPU_CORE
ISL6266A



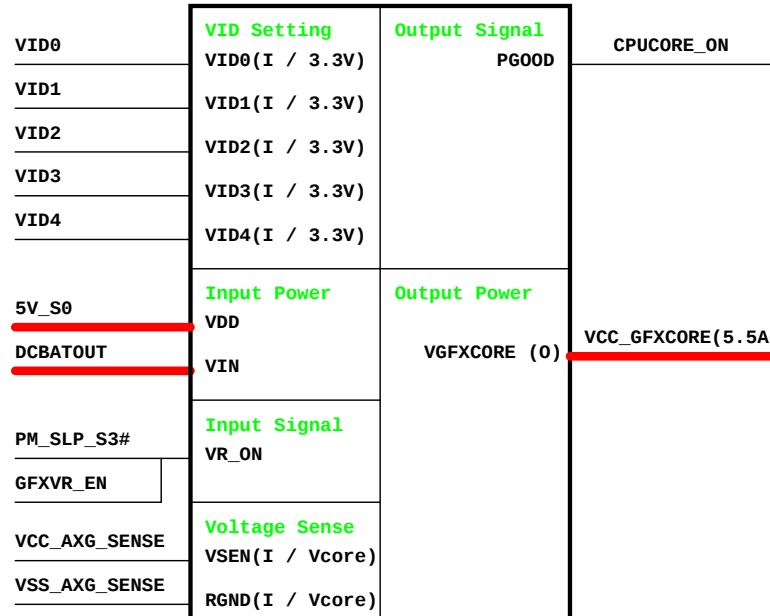
TPS51124
1D8V/1D05V



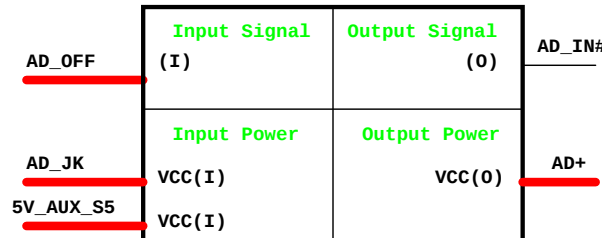
TPS51125
5V/3D3V



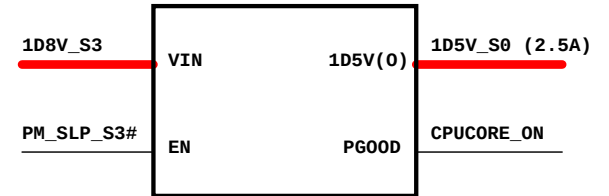
GFX_CORE
ISL6263A



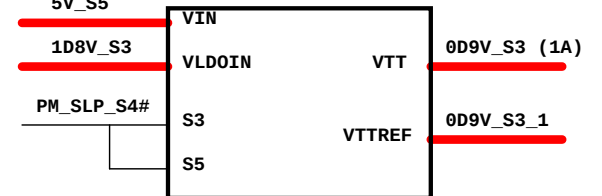
Adapter



RT9018A
1D5V_S0



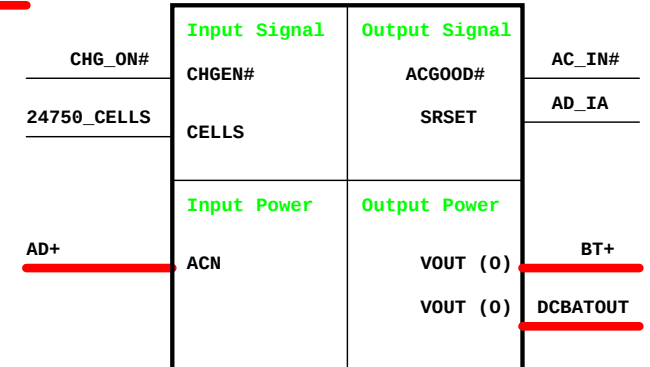
RT9026 0D9V_S0

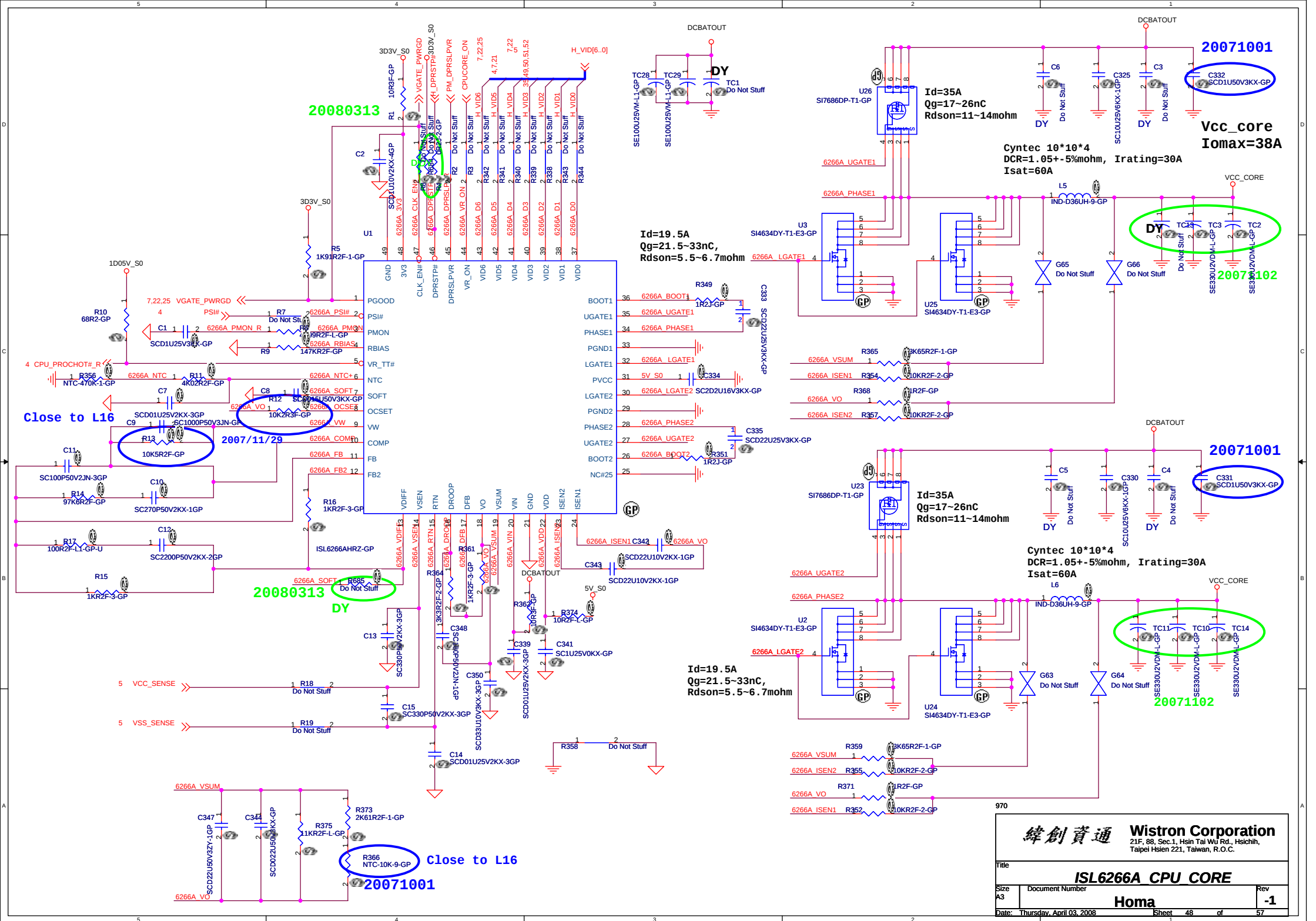


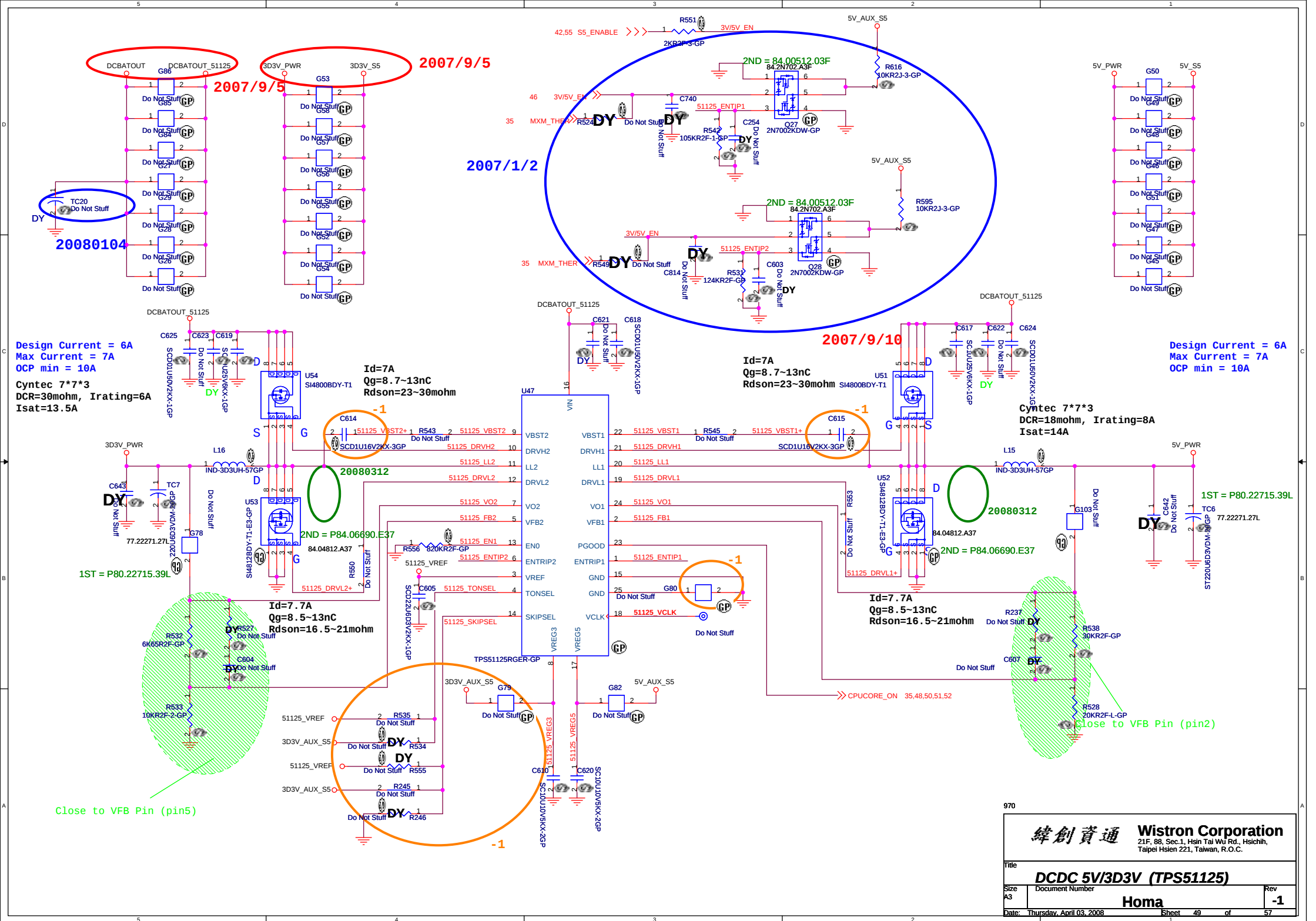
G9131 2D5V_S0



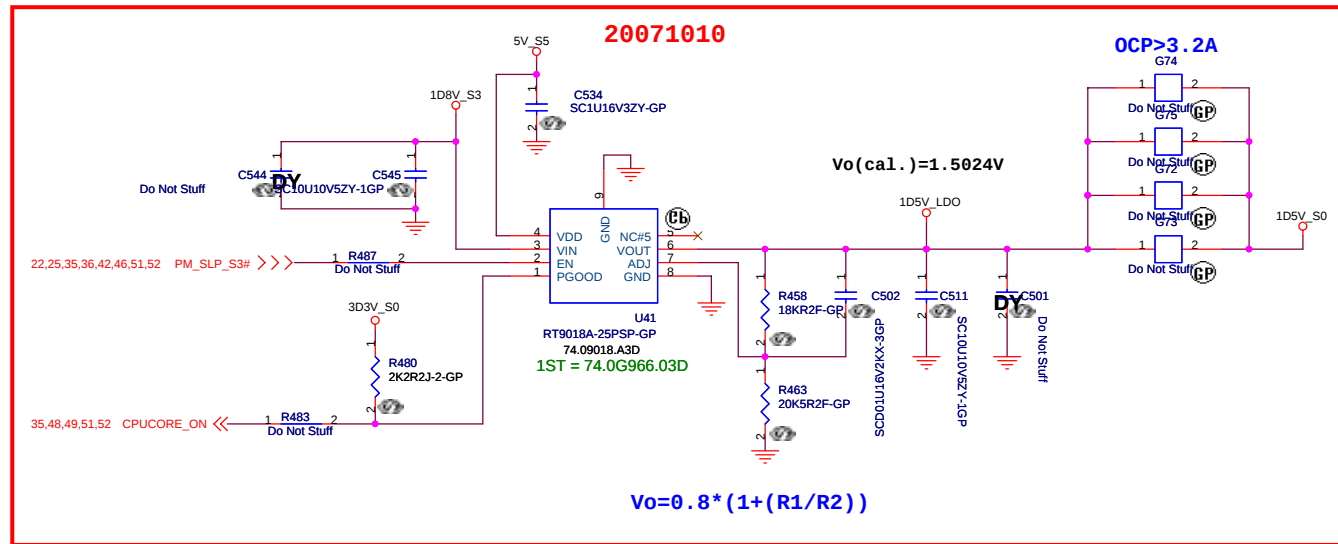
Charger BQ24750





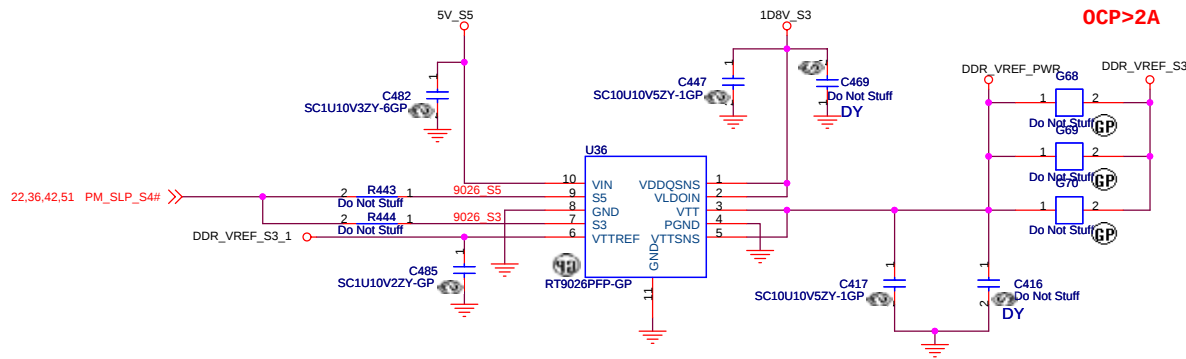


1D5V_S0 Iomax=2.5A

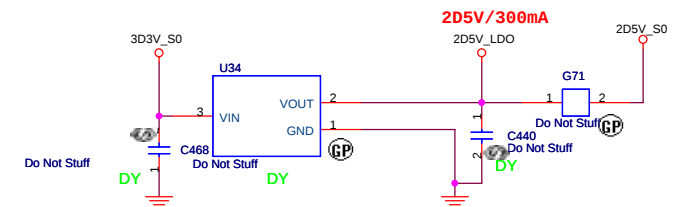


20071001

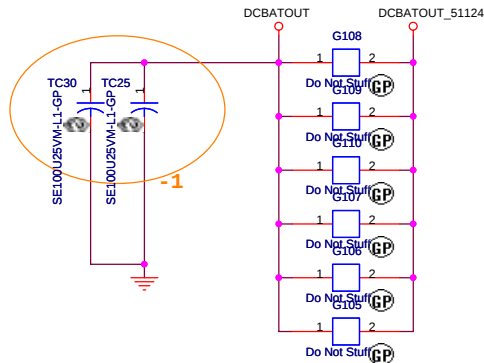
Iomax=1A
OCP>2A



2D5V_S0 Iomax=0.3A



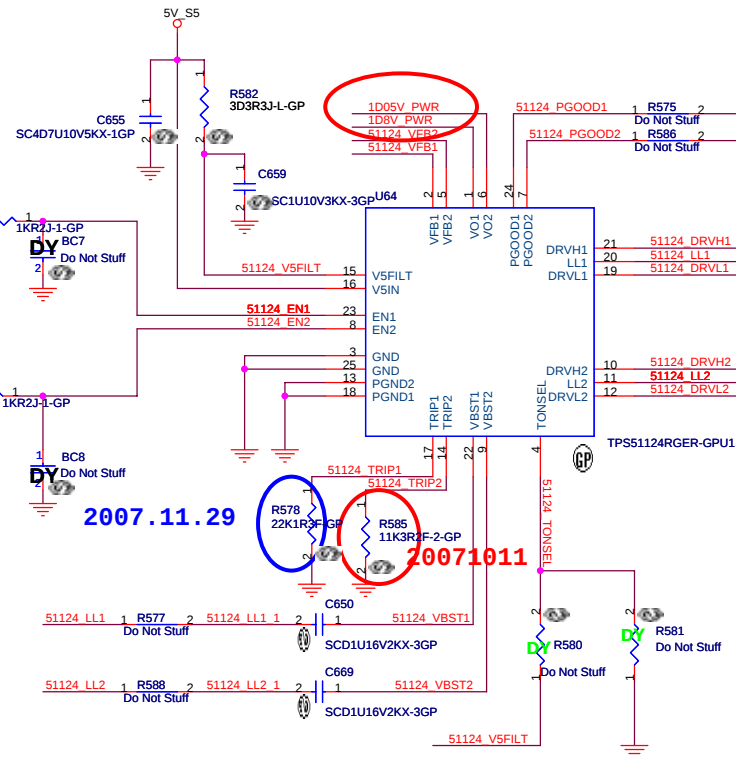
970



$$V_{trip}(mV) = R_{trip}(Kohm) * I_{uA}$$

$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in} - V_{out}) * V_{out}) / V_{in})$$

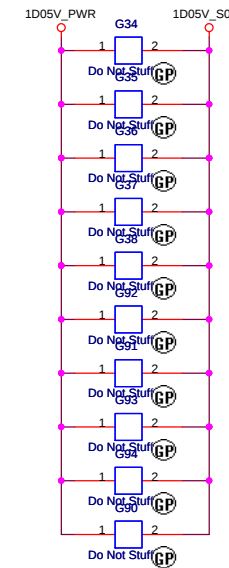
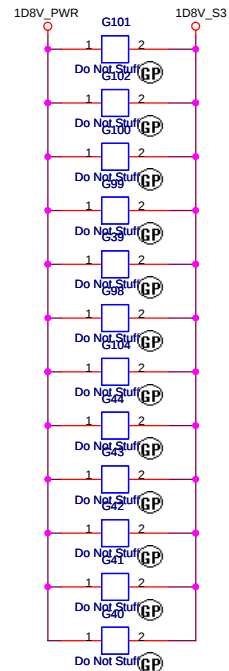
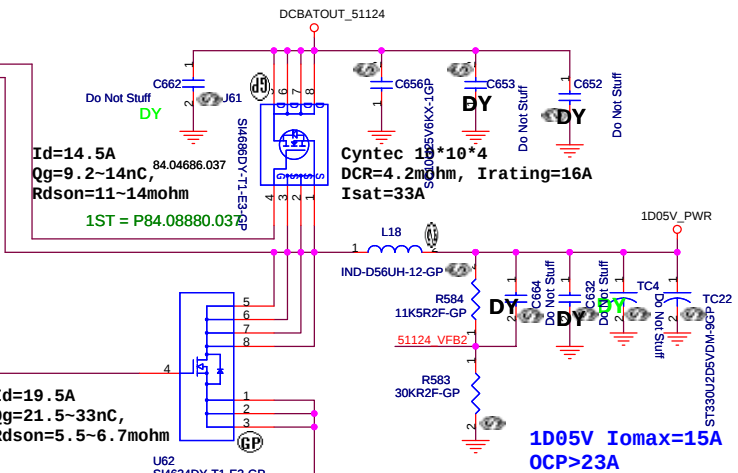
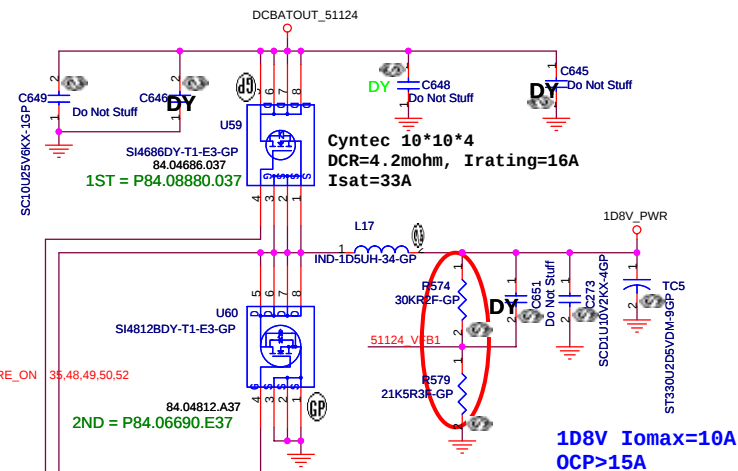
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L



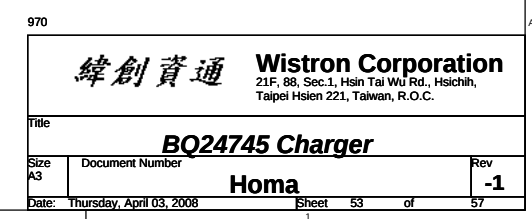
	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$$V_{out} = 0.758V * (R1 + R2) / R2 \rightarrow \text{PWM mode}$$

$$V_{out} = 0.764V * (R1 + R2) / R2 \rightarrow \text{Skip Mode}$$

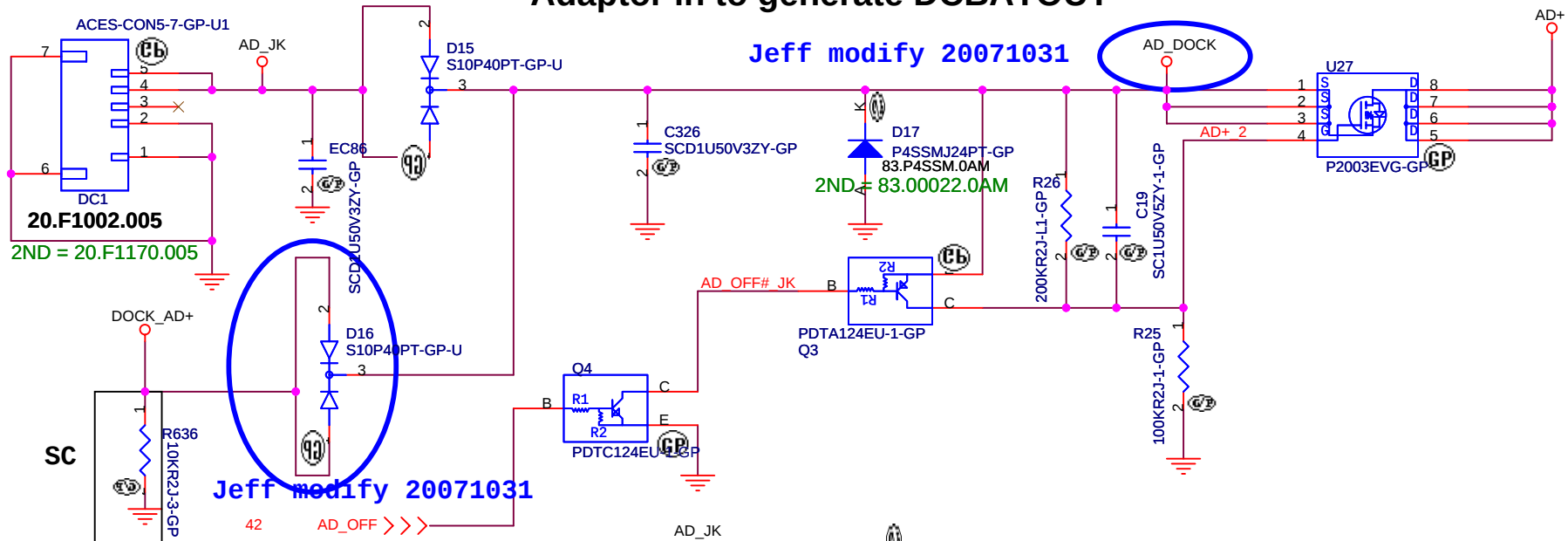


970

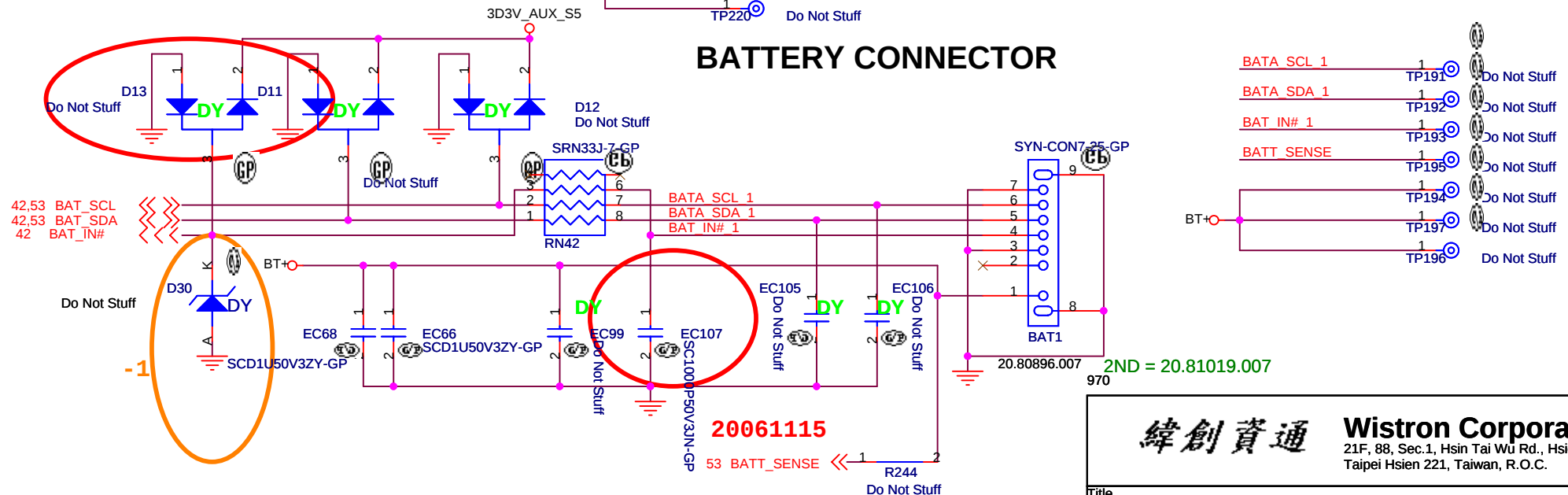


Adaptor in to generate DCBATOUT

Jeff modify 20071031



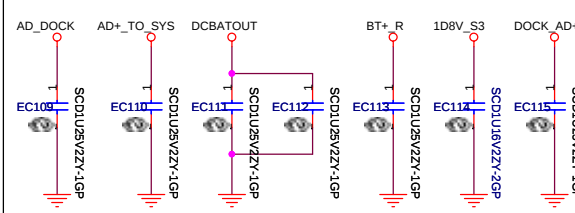
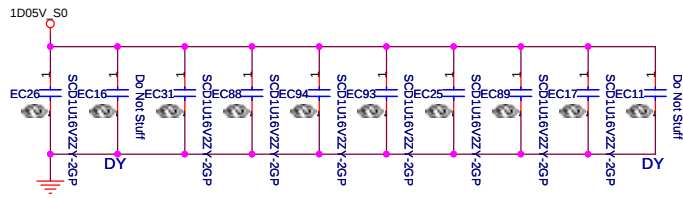
BATTERY CONNECTOR



緯創資通

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AD/BATT CONN		
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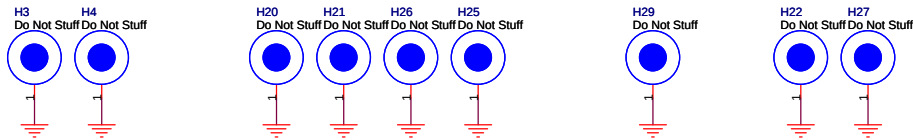
Check test point

- 3D3V_S0 <<< TP110 Do Not Stuff
- 3D3V_AUX_S5 <<< TP111 Do Not Stuff
- 3D3V_S5 <<< TP112 Do Not Stuff
- 5V_S5 <<< TP113 Do Not Stuff
- 22.42 PM_PWRBTN# <<< TP114 Do Not Stuff
- 4.21.46 H_PWRGD <<< TP115 Do Not Stuff
- 42.49 SS_ENABLE <<< TP116 Do Not Stuff
- 4.6 H_CPURST# <<< TP117 Do Not Stuff

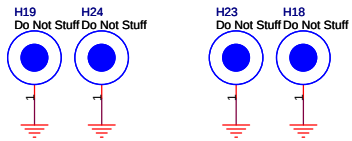
Test Point 放在 Dimm Door 打開可量測處

Stand off Location

34.42Y01.031



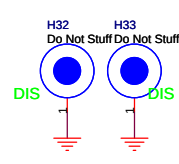
34.46502.021



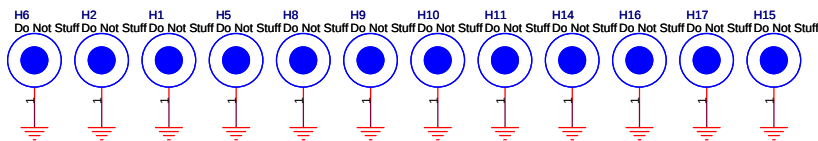
34.4Z402.011



34.4Z401.011



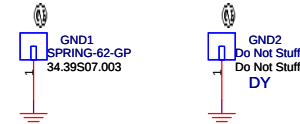
**DELETE MXM
STAND-OFF
H7;H28;H30;H31**



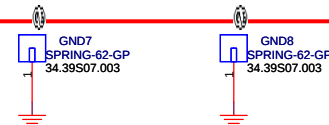
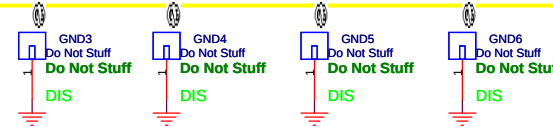
SC

SPRING ON BOTTOM

DIMM Heat Sink



MXM SPRING -1 20080307



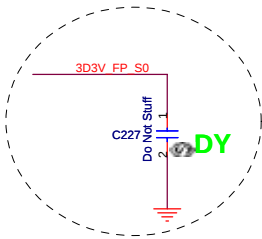
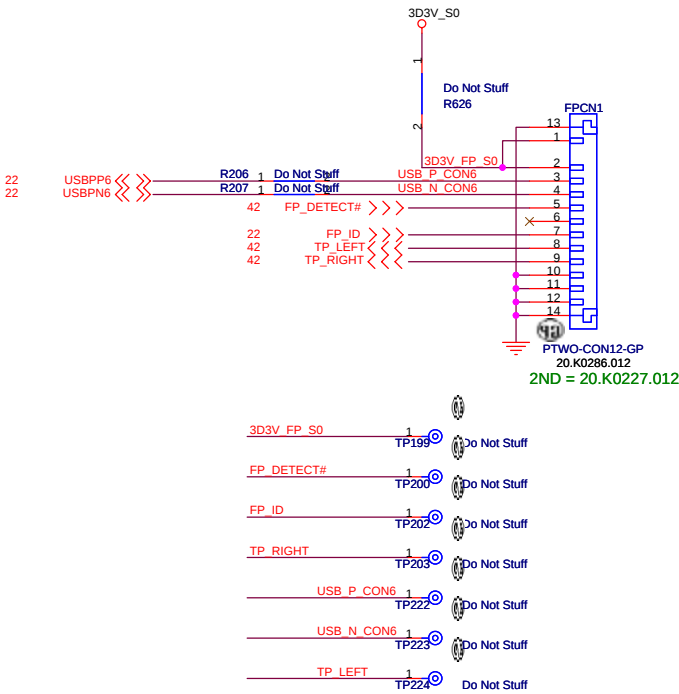
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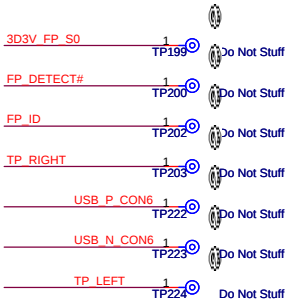
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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Finger printer



For EMI



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- 1.page25,Change Q24 and Q5 Pin_C and Pin_E net, Swap H_THERMDA and H_THERMDC(only close to C95)
- 2.page46,Change R145_Pin1 pull hige power to 1D05V_S0
- 3.page42,Add the Net let link U17_Pin101 and RN45_Pin3
- 4.page16,SWITCHCN1 pin12 connect to 3D3V_AUX_S5 and pin 11 connect to LID_CLOSE#
- 5.page20,HDMI1 change to 62.10078.171
- 6.page44,DOCK1 pin51 connect to CRT_DEC#
- 7.page53,R214 change to connect BQ24745_VREF as charger modify
- 8.page26,change ODD1 to 22.10300.141
- 9.page45,change U12 to PS8122QFN48G-GP and add some components
- 10.page44,Del U5
- 11.page20,Del U11,U42,Q9...
- 12.del G1-G8
- 13.page45,R614 changed to "DOCK_DT1#" and U12 output port1 and port2 swap,RN68 pin1&2 change to KBC SMBUS, RN69 pin3&4 change to connect"3D3V_S0",R615 change to 4K7R2F-GP
- 14.page49,change Q27&Q28 to 2N7002SPT ,add R595 R616
- 15.page48,change R12 to 10K2R3F-GP ,R13 to 16K5R2F-1-GP
- 16.page51,R578 change to 22K1R3-GP
- 17.page52,R257 change to 2K87R2F-1-GP ,C259 change to SCD033U50V
- 18.page40,change U8 to G1454R41U-GP
- 19.page42,Del R29 R27 C20 EC5
- 20.page41,LID1 change to INTMIC1 and connect to "MIC_L_CN"&"MIC_R_CN"
- 21.page39,add R619 C815 R621 R620 C816 C817
- 22.page38,Del C355 C320
- 23.page56,Del F4 addR626
- 24.page3,R204 change to connect"3D3V_CLKPLL_S0"
- 25.page52,add R622-R625
- 26.page44,add C818-C822 and L19 L20 L21
- 27.page35,Del TP77-TP82 TP84 TP86 TP87 TP24 TP25 TP26 TP28,add R618 pull up to 3D3V_S0
- 28.page25,add R617 Q35 del R115
- 29.page30,change C600 to 4.7U10V
- 30.page45, swap U12 output port1&pot2
- 31.page48-52, change power GAPS to close GAPS
- 32.page49,L15 change to 1ND-3D3UH by power modify
- 33.page16,add R627 EC108
- 34.page45,add C823 C824 and R144 R151 Q9 R137

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緯創資通

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