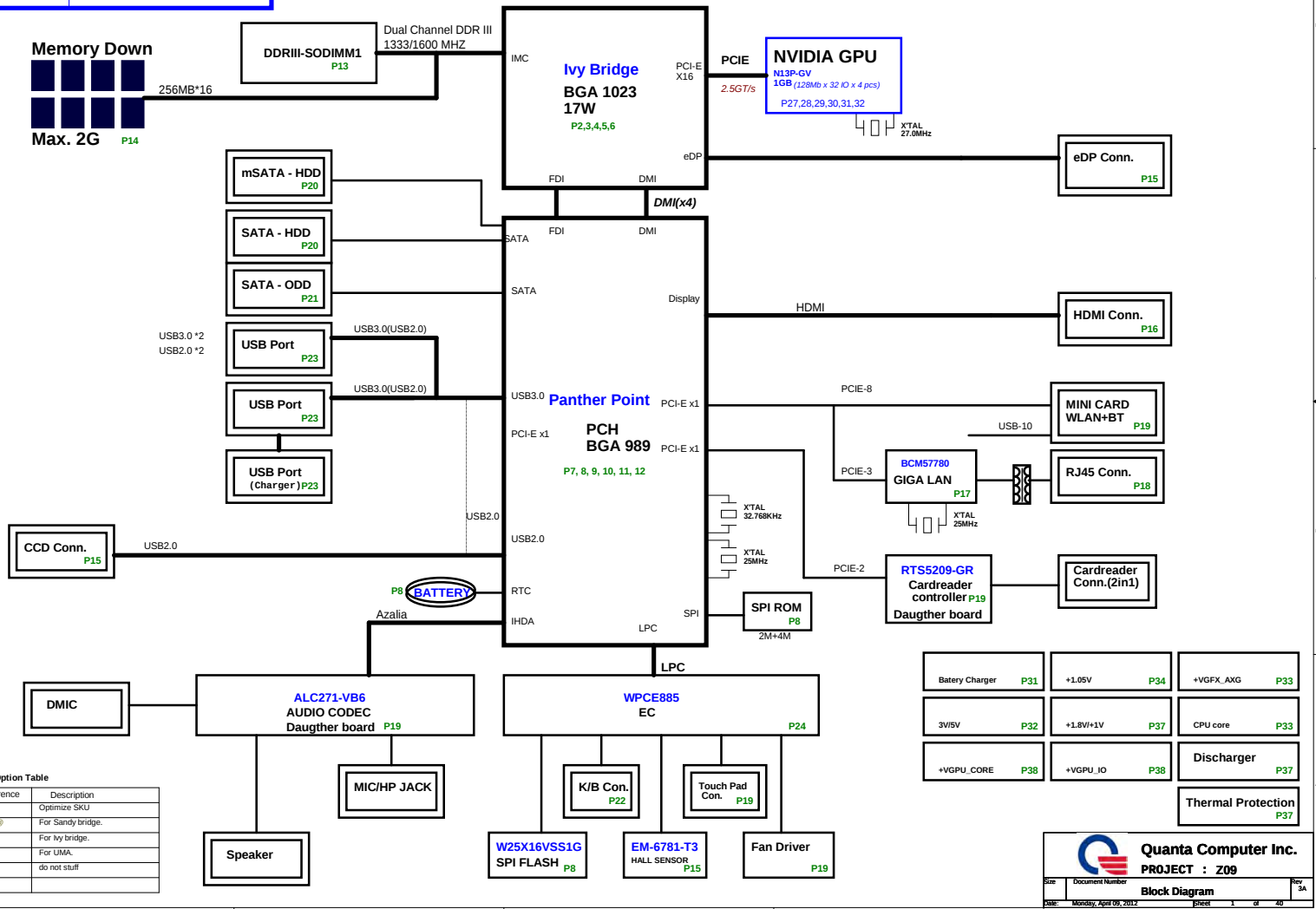


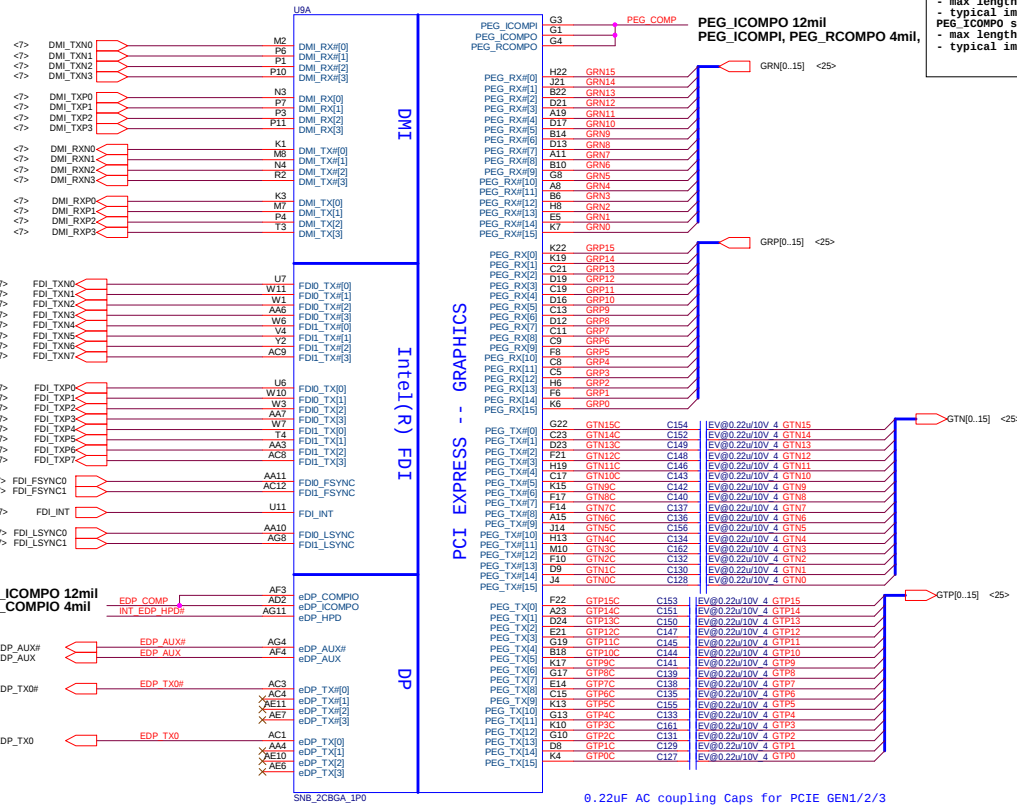
BOM P/N	Description
---------	-------------

Z09 SYSTEM BLOCK DIAGRAM



Ivy Bridge Processor (DMI, PEG, FDI)

PEG_ICOMPI and RCOMPO signals should be shorted and routed with
 - max length = 500 mils
 - typical impedance = 43 mohms
 PEG_ICOMPO signals should be routed with
 - max length = 500 mils
 - typical impedance = 14.5 mohms

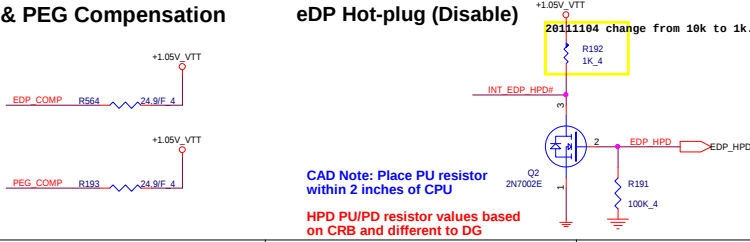


DP_COMPIO and ICOMPO signals should be shorted near balls and routed with
 - typical impedance < 25 mohms

UG 1.8:
 The recommended AC cap value is changed to 220nF for compatibility with PCIe Gen3 on future platforms.
 For Gen2 only designs, it is acceptable to continue to use the 100nF capacitor.

DP & PEG Compensation

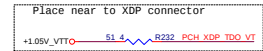
eDP Hot-plug (Disable)



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Size	Document Number	Rev
	Ivy Bridge 1/5	3A
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6. If motherboard only supports external graphics or if it supports Processor Graphics but without eDP:
 Connect **DRL_REF_SCLKL** on Processor to **GND** through **1K +/- 5% resistor**
 Connect **DPL_REF_SCLKL** on Processor to **VCCP** through **1K +/- 5% resistor**



20121218 change net to PCI_PLTRST#

PCI_PLTRST#

IN

GNDOUT

74VLC1G07FVW_NC

5K/F 4

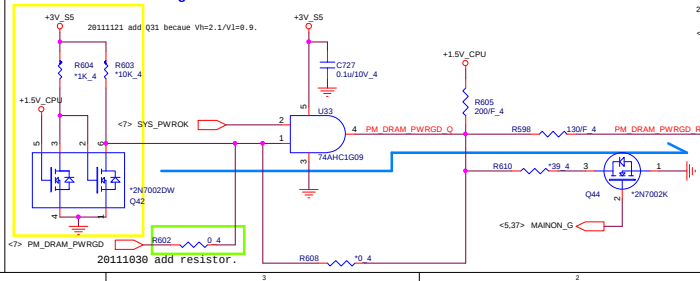
CPU_PLTRST#_R

+3V

C190

0.1uF/0V_4X

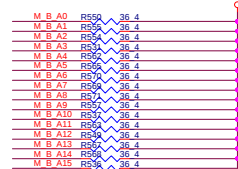
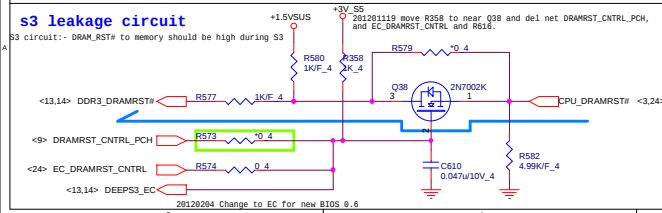
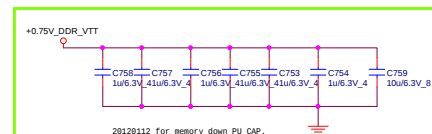
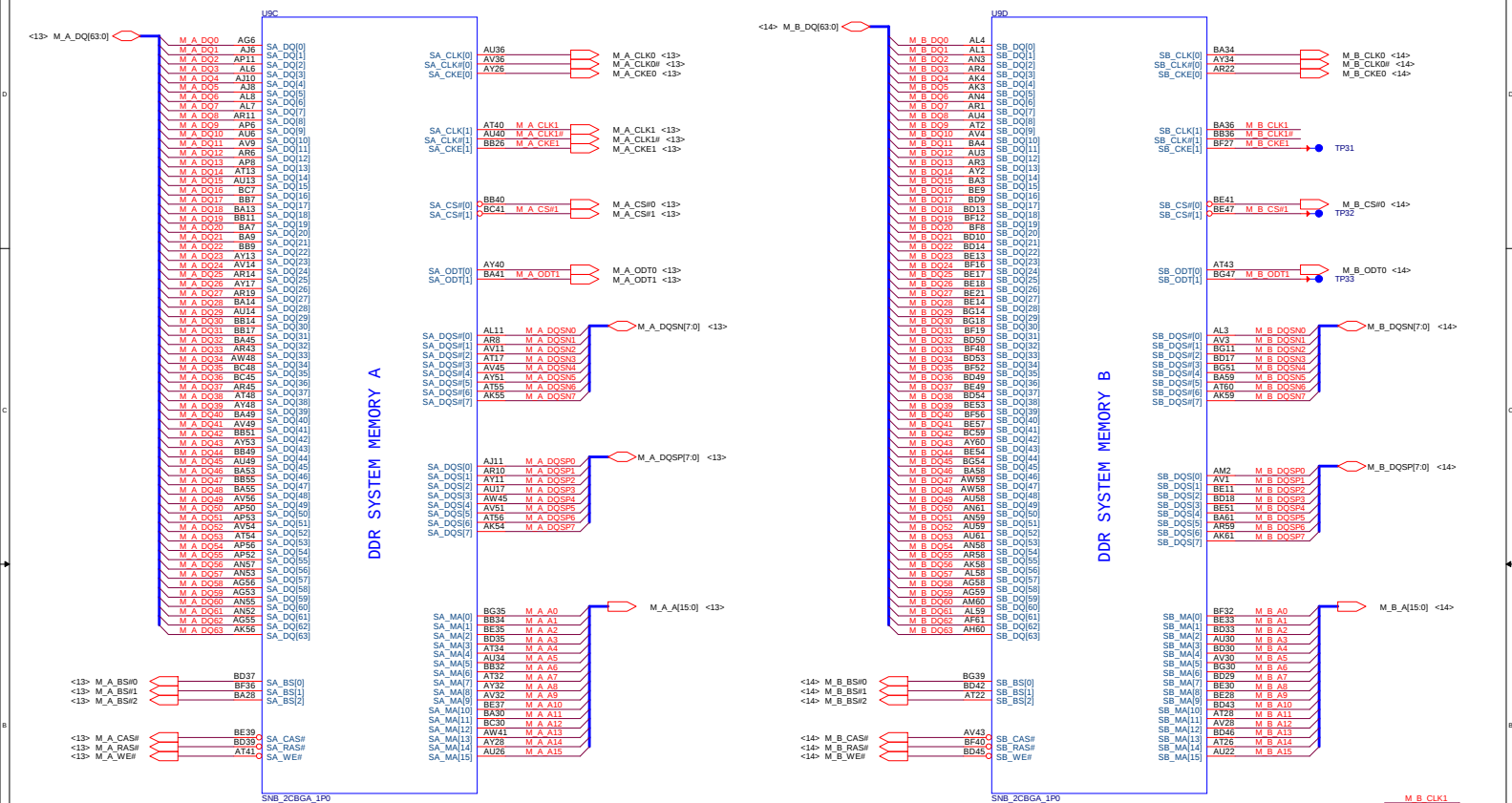
IN	OUT
L	
H	High-Z



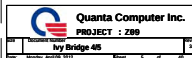
IN	OUT
L	L
H	High-Z

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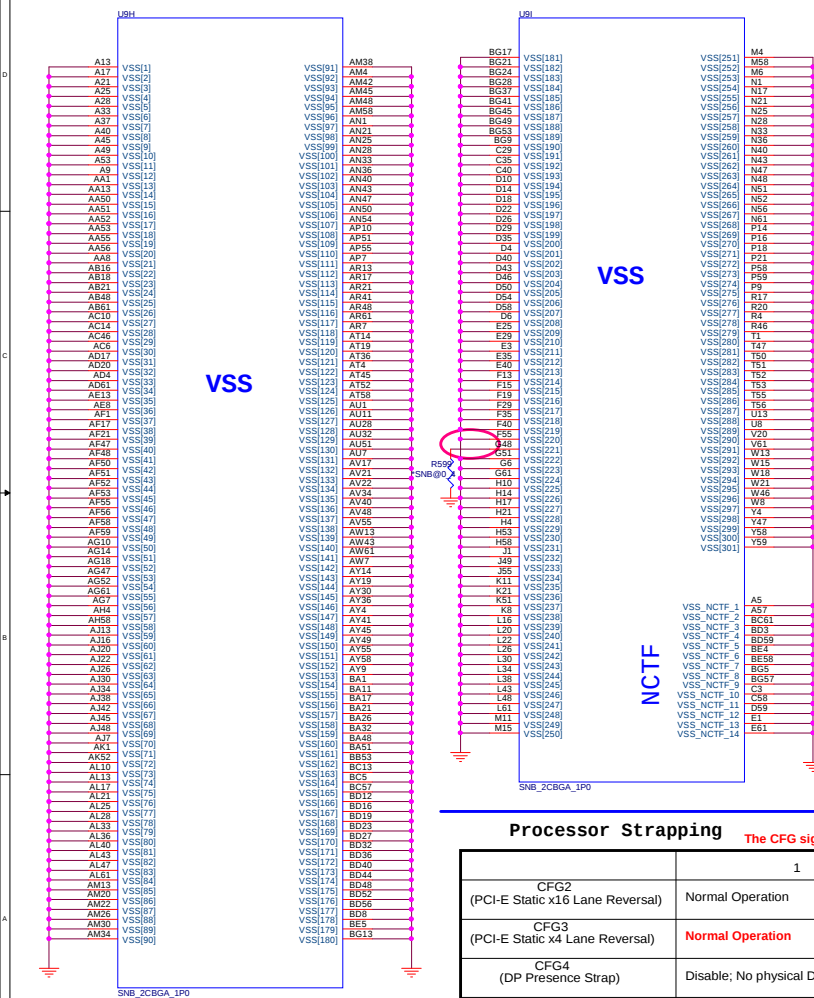
Sandy Bridge Processor (DDR3)



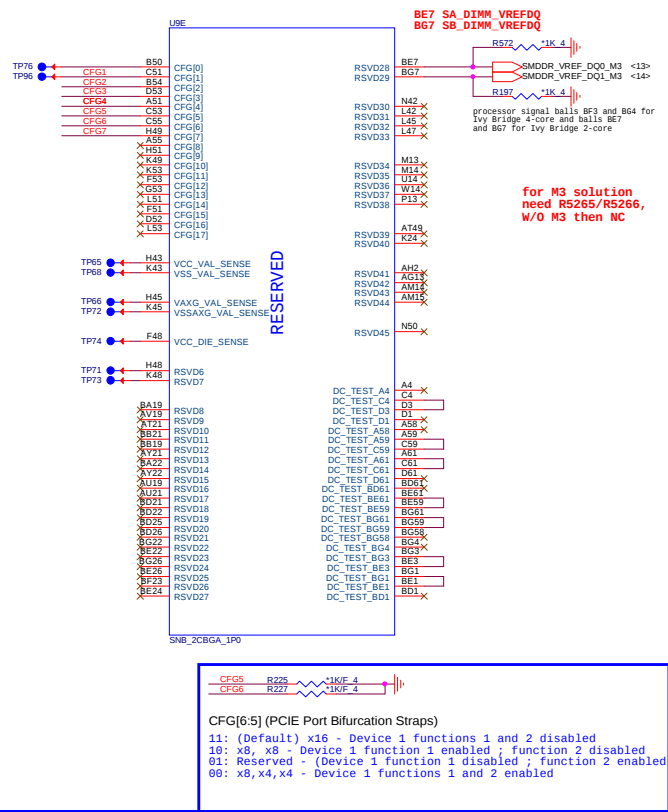
Sandy Bridge Processor (GRAPHIC POWER)



Sandy Bridge Processor (GND)



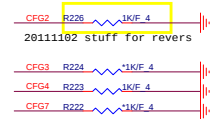
Sandy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



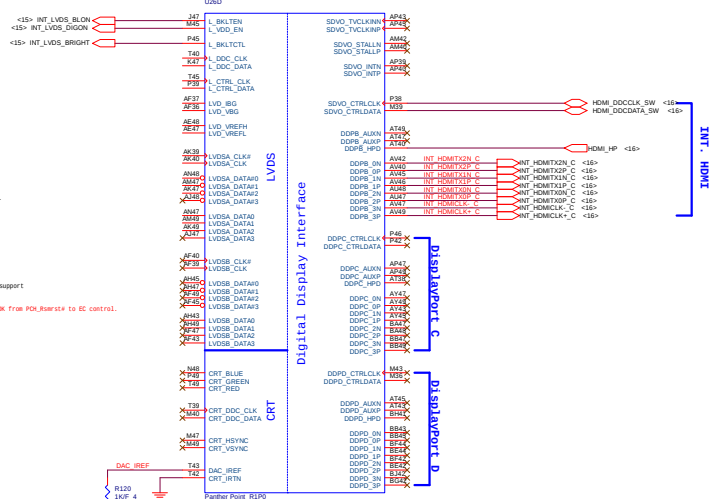
Quanta Computer Inc.

PROJECT : Z09

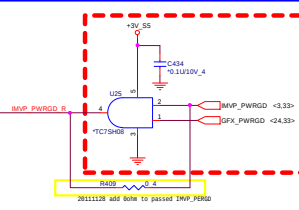
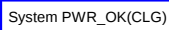
Size: Document Number: Ivy Bridge 5/5 Rev 3A

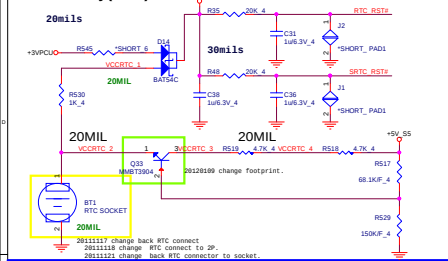
Date: Monday, April 09, 2012 Sheet 6 of 40

U26C



CRB 1.0 change R5196 to 1K

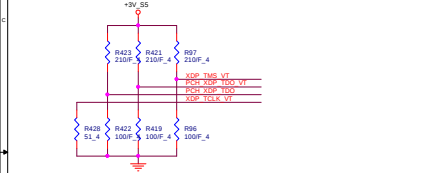




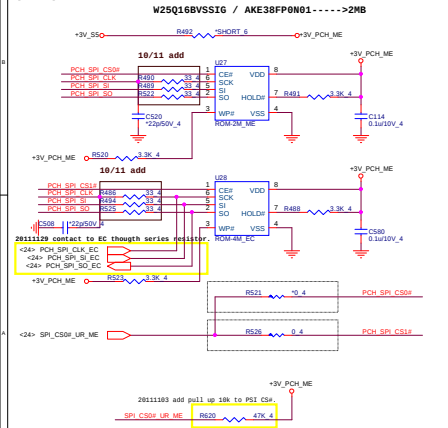
HDA Bus(CLG)



PCH JTAG Debug (CLG)



PCH Dual SPI (CLG)



PCH Strap Table

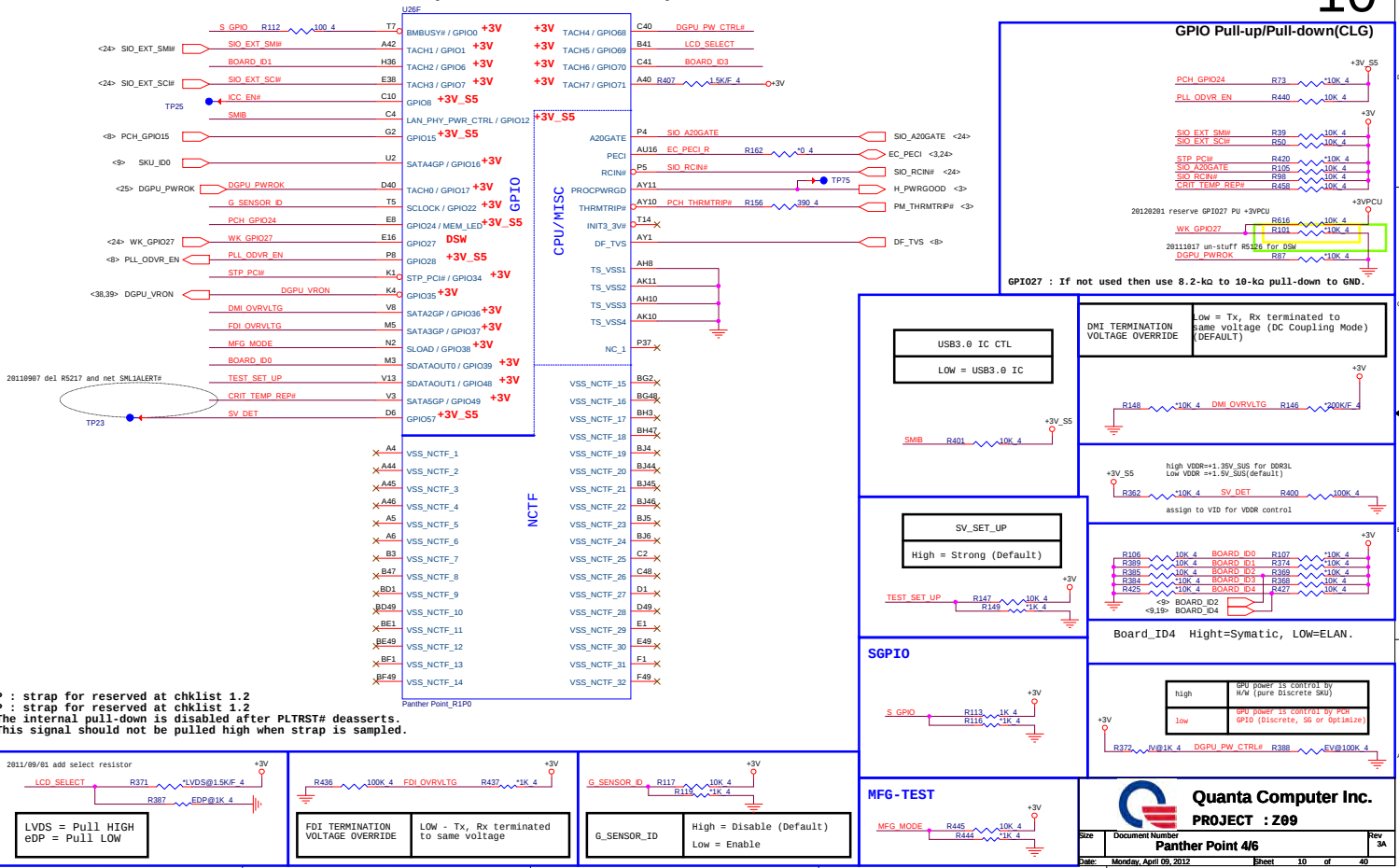
Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V0 R460 20K 4 SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R418 20K 4 PC1_GNT3# <0>
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R391 200K 4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK		
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SDO	Flash Descriptor Security	RSMRST	0 = effect (default)(weak pull-down 20K) 1 = overridden	+24 ME_WREN R377 20K 4 ACZ_SDOOUT_R
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss (weak pull-down 20K) 1 = Set to Vcc	R463 20K 4 DF_TVS <10> R464 20K 4 PL_SMB_NREF <3>
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K) 1 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	R439 20K 4 PLL_OVR_EN <10>
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Disable (Default) 1 = Enable	+3V_SS R390 10K 4 ACZ_SYNC_R
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite internal PD	RSMRST	0 = Disable (Default) 1 = Enable	+3V_SS R413 10K 4 PCH_GPIO15 <10>
DSWVREN	DEEP S4/S5 well On Die DSW VR Enable	DSW	High = Enable (Default) Low = Disable	+3V_RTC R469 200K 4 R59 200K 4 DSWVREN <7>
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V0 R473 10K 4 NV_ALE <0>

Used as GPIO only. at chikist 1.2

Default weak pull-up on GNT0/1#
(Need external pull-down for LPC BIOS)

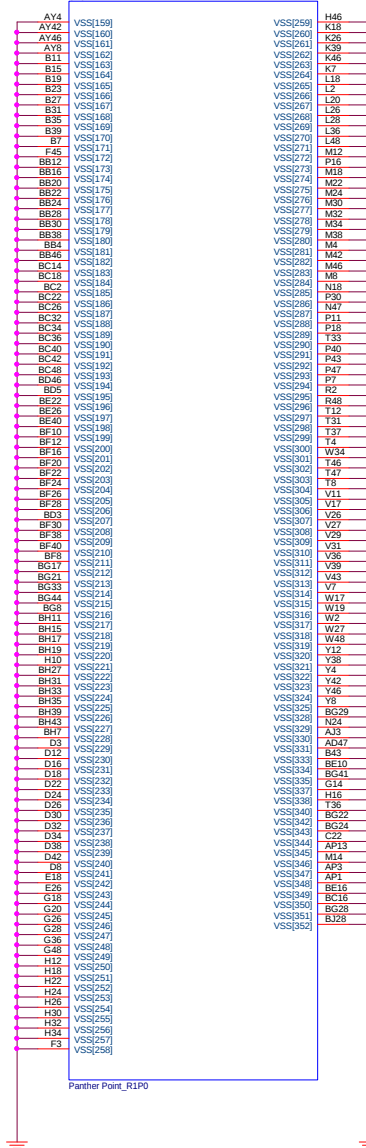
ME_WR default EC setting folating

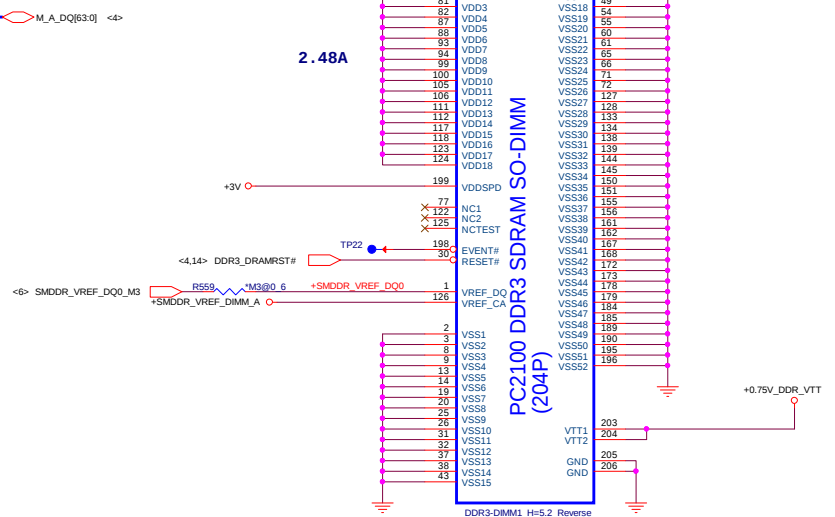
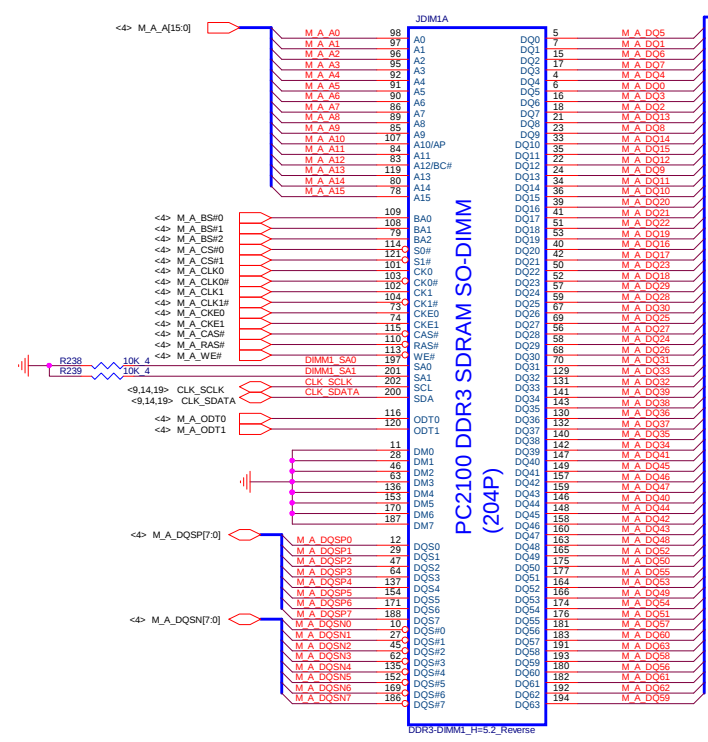
for future CPU, Sandy Bridge MC
DF_TVS needs to be pulled up to VccOPTERN power rail
through 2.2 kOhm 15% - R393 change to 0 or not??Needs to be pulled High for Huron River platform.
chikist 1.2



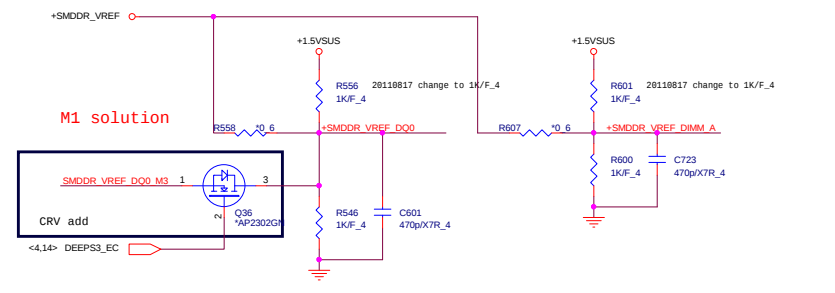
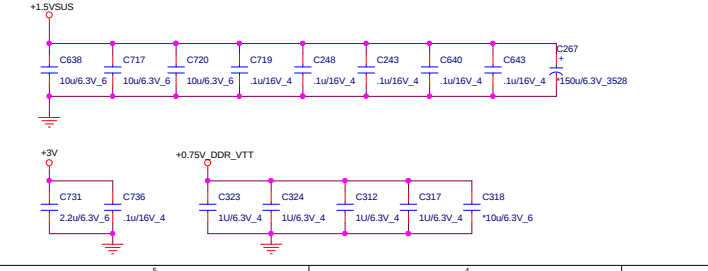


U261





Place these Caps near So-Dimm0.



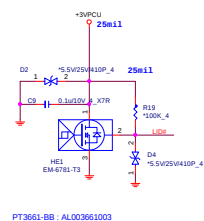
	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

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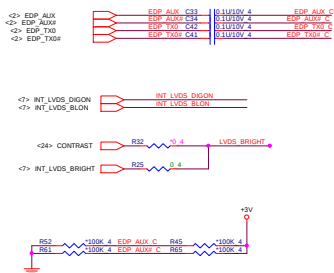
Size Document Number
DDR3 SO-DIMM-0

Date: Monday, April 09, 2012 Sheet 13 of 40 Rev 3A

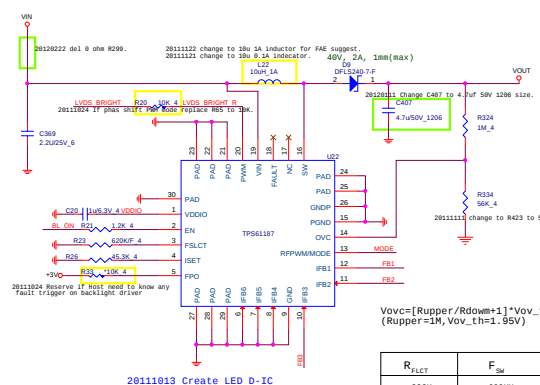
7/28 modify



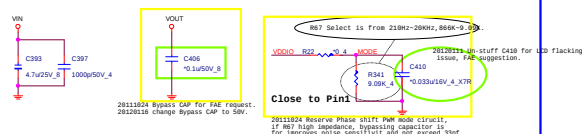
PT3661-BB : AL003661003



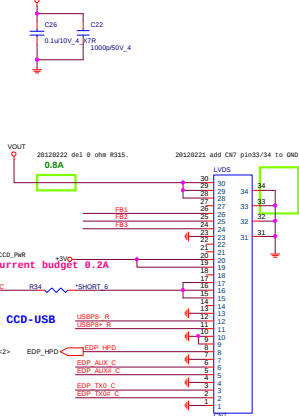
LED Driver-IC


$$V_{ovc} = [R_{upper} / R_{down} + 1] * V_{ov} \quad (R_{upper} = 1M, V_{ov} = 1.95V)$$

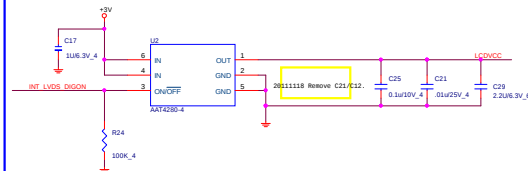
R_{FLCT}	F_{SM}
833K	600KHz
625K	800KHz
499K	1MHz



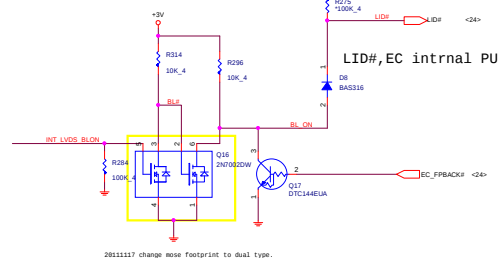
LCD CONNECTOR



LCD Power

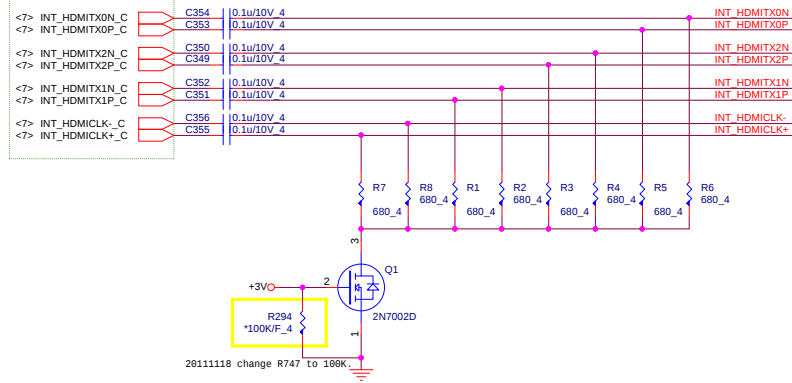


Backlight Control

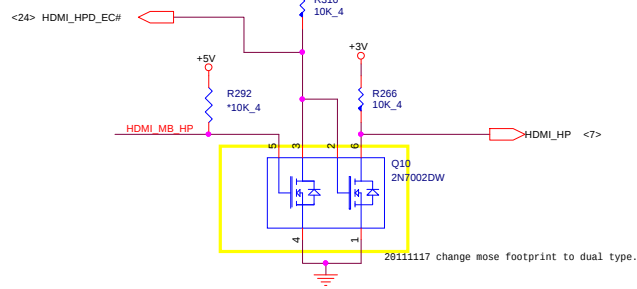


HDMI

from PCH

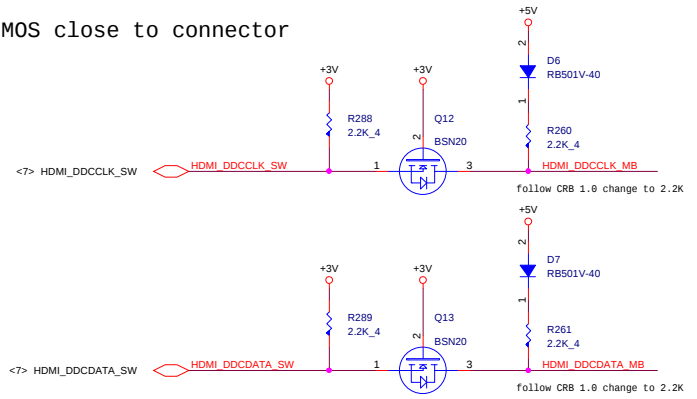


HDMI-detect

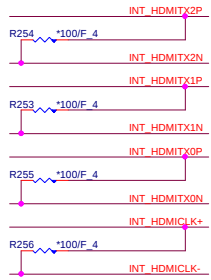


I2C

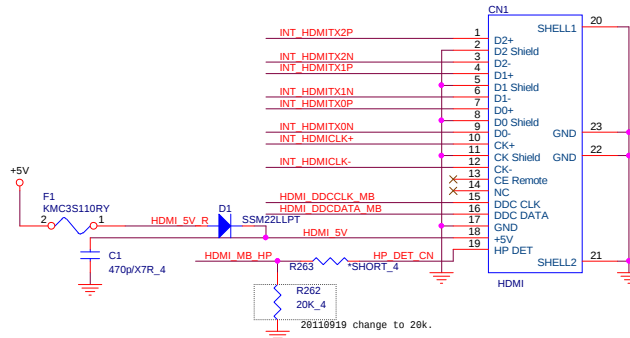
MOS close to connector

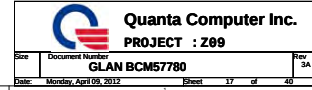


EMI

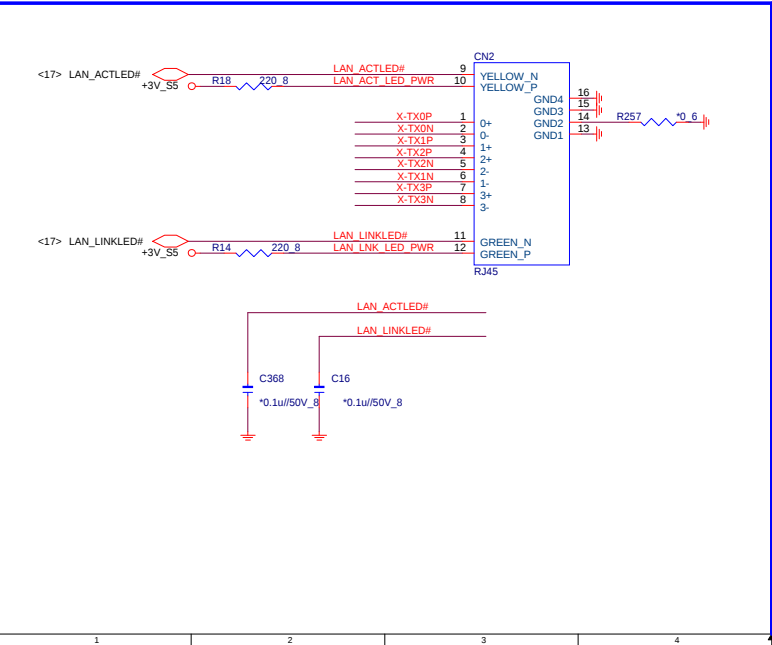
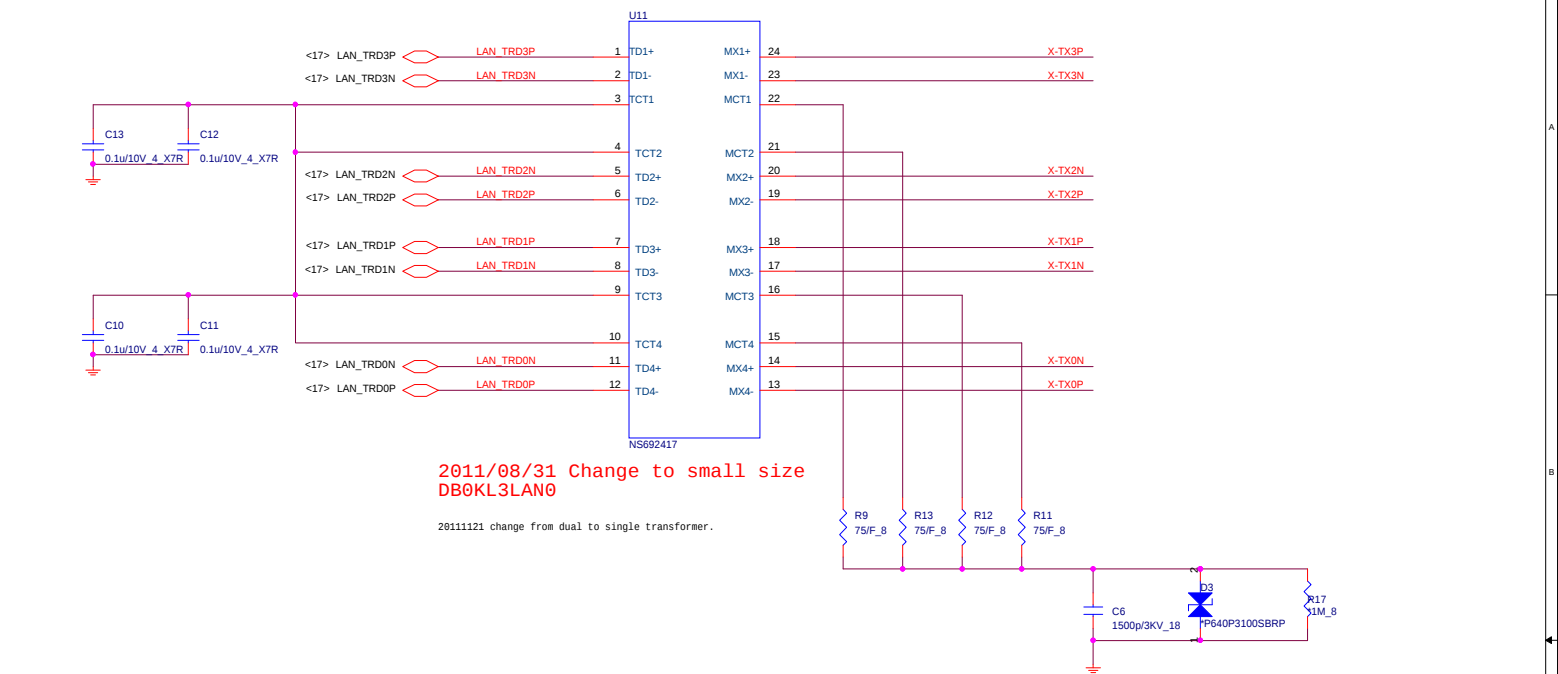


HDMI connector

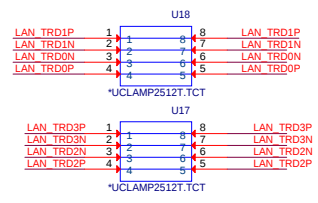




TRANSFORMER



For EMI



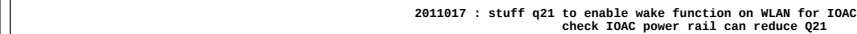


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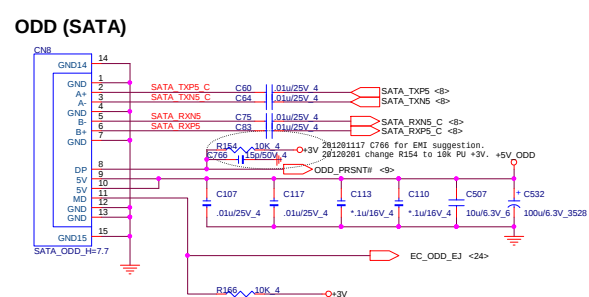
Size	Document Number	Rev 3A
LAN Transformer and RJ45		
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+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

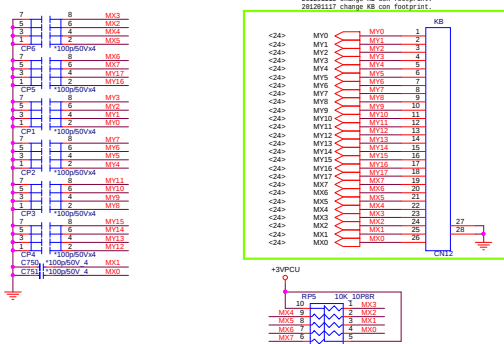


1

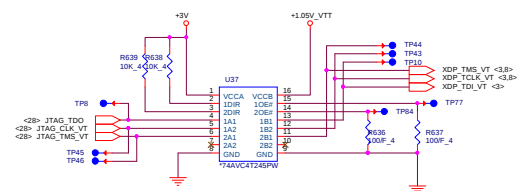


[illegible]

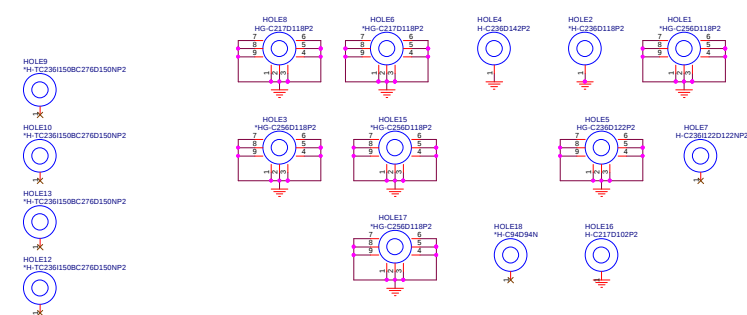
K/B



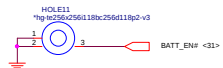
ICT TEST FIXTURE(VOLTAGE TRANSLATOR)



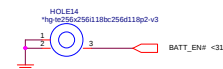
SCREW HOLE



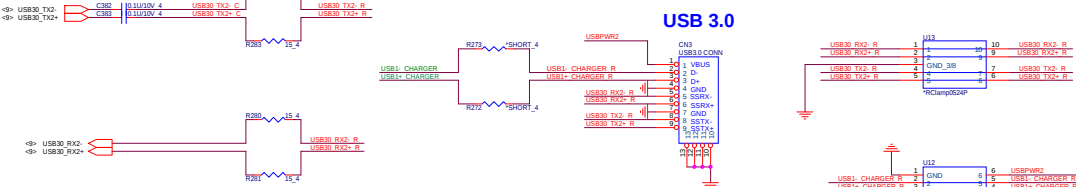
BATT Enable short pad



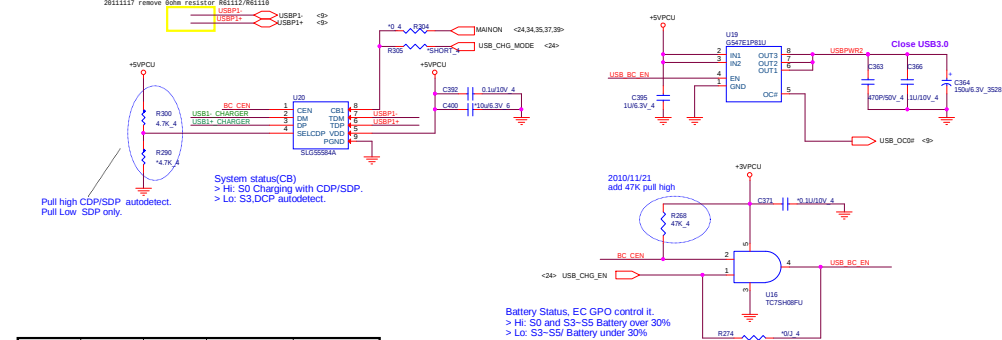
28111208 Change Hole8 to BATT short pad.



USB3.0 CONN

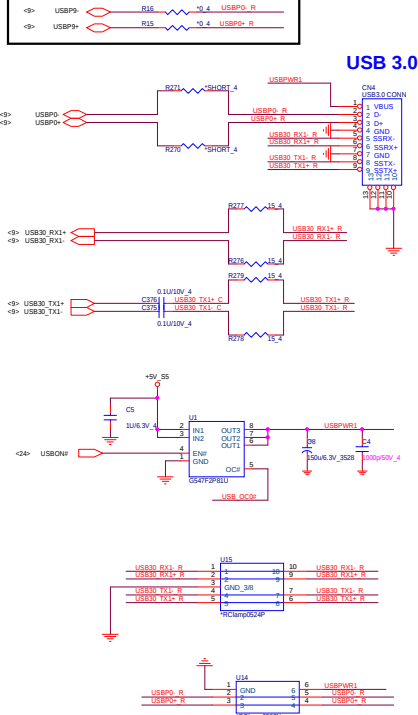


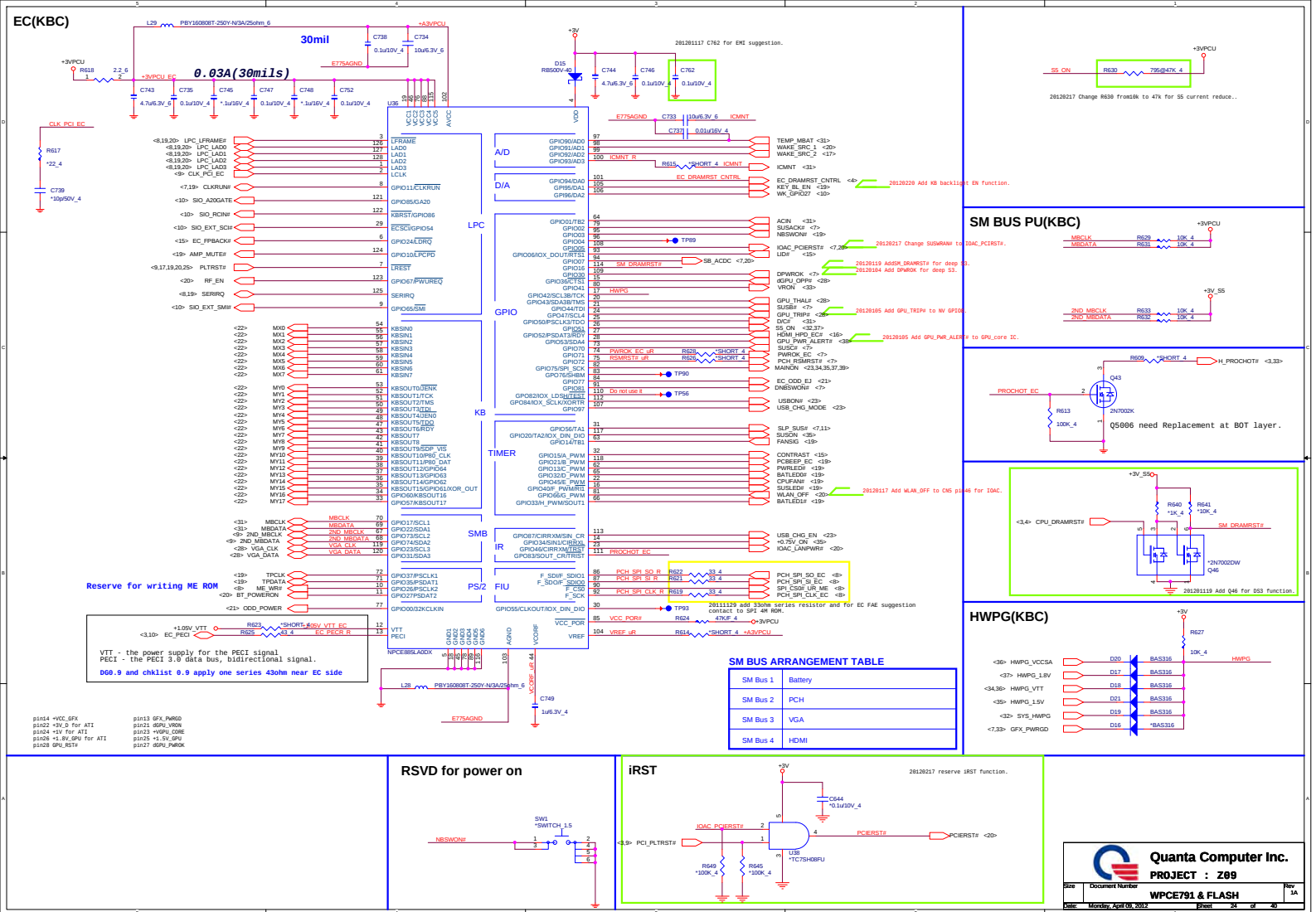
USB charger



Name	USB data	State	Max Current	Apple Device
SDP	YES	S0-S3	500mA	500mA
CDP	YES	S0-S3	1500mA	500mA
DCP_Auto	NO	S4-S5	1800mA	1800mA

Reserve for Debug





<30> VMA_DQ[63..0]
 <30> FBA_D[63..0]
 <30> FBA_EDC[7..0]

<30> VMB_DQ[63..0]
 <30> FBC_D[63..0]
 <30> FBC_EDC[7..0]

5500mA

UMC

318 FBB

VMB_DQ0

VMB_DQ1

VMB_DQ2

VMB_DQ3

VMB_DQ4

VMB_DQ5

VMB_DQ6

VMB_DQ7

VMB_DQ8

VMB_DQ9

VMB_DQ10

VMB_DQ11

VMB_DQ12

VMB_DQ13

VMB_DQ14

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VMB_DQ161

VMB_DQ162

VMB_DQ163

VMB_DQ164

VMB_DQ165

VMB_DQ166

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VMB_DQ196

VMB_DQ197

VMB_DQ198

VMB_DQ199

VMB_DQ200

VMB_DQ201

VMB_DQ202

VMB_DQ203

VMB_DQ204

VMB_DQ205

VMB_DQ206

VMB_DQ207

VMB_DQ208

VMB_DQ209

VMB_DQ210

VMB_DQ211

VMB_DQ212

VMB_DQ213

VMB_DQ214

VMB_DQ215

VMB_DQ216

VMB_DQ217

VMB_DQ218

VMB_DQ219

VMB_DQ220

VMB_DQ221

VMB_DQ222

VMB_DQ223

VMB_DQ224

VMB_DQ225

VMB_DQ226

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VMB_DQ230

VMB_DQ231

VMB_DQ232

VMB_DQ233

VMB_DQ234

VMB_DQ235

VMB_DQ236

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VMB_DQ319

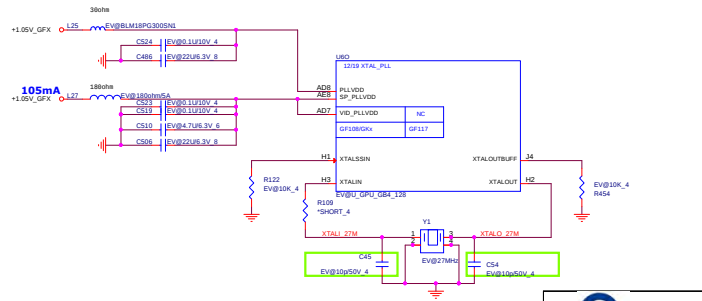
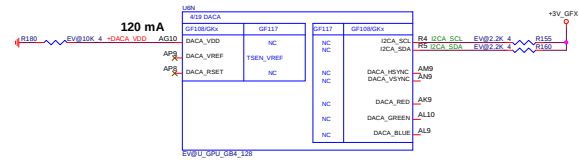
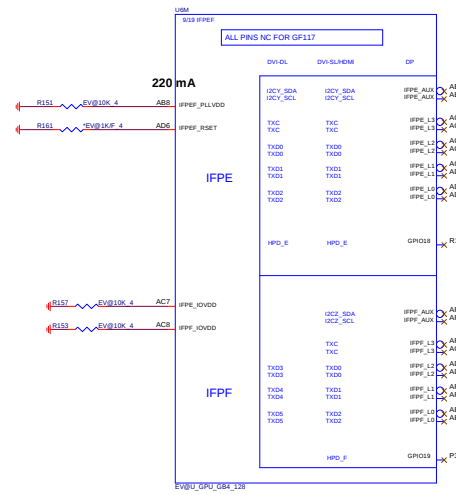
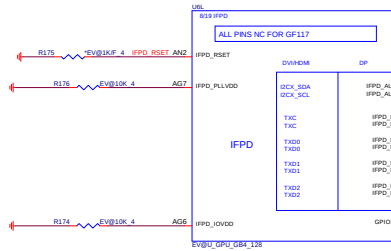
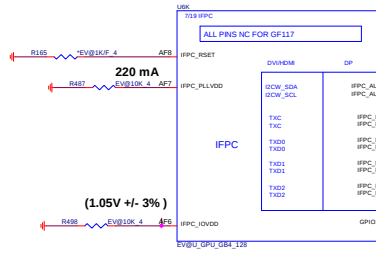
VMB_DQ320

VMB_DQ321

VMB_DQ322

VMB_DQ3

IFPAB ONLY: NO STUFF RSET is default
Required when external reference is used



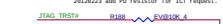
20120201 Change CAP from 27P to 10P

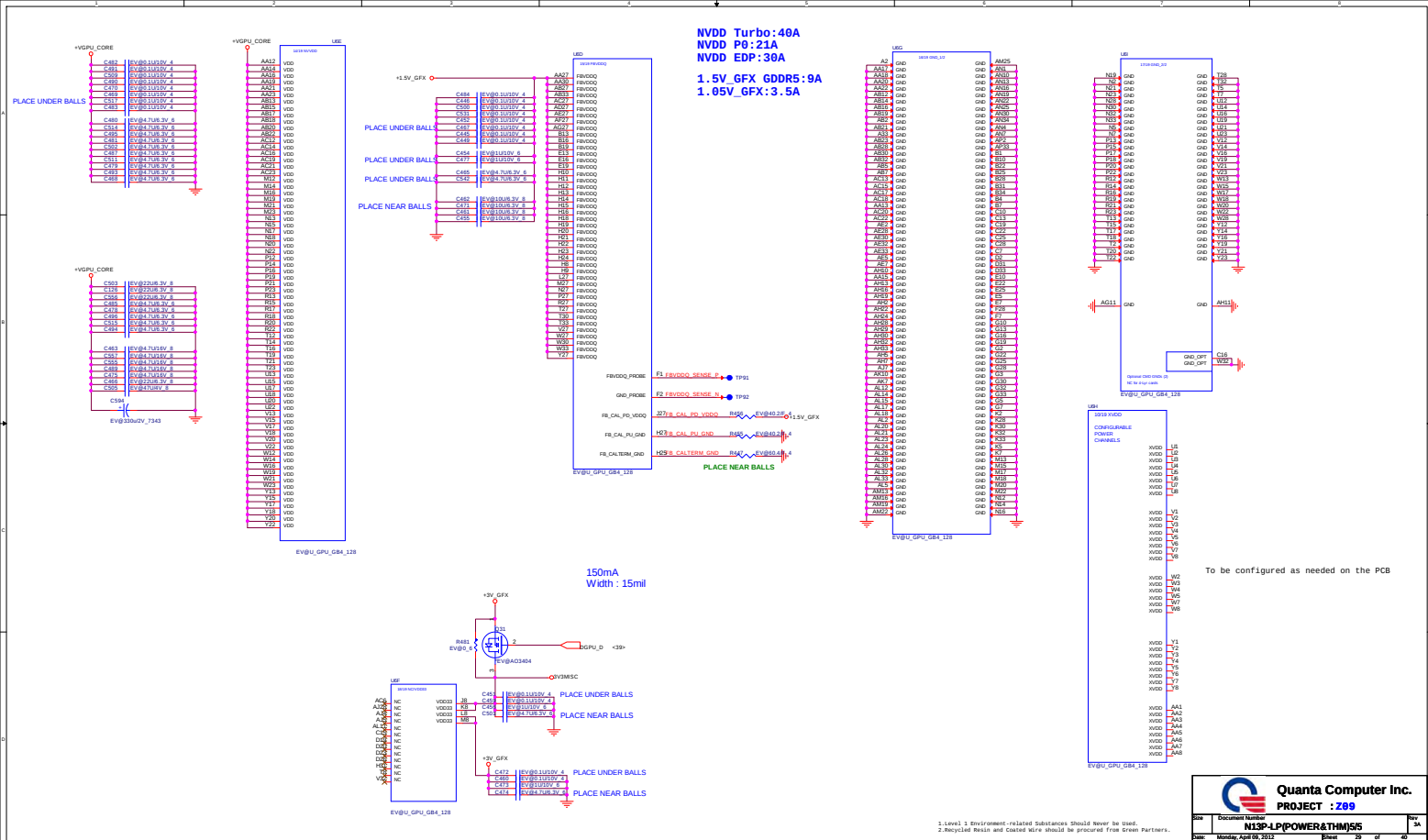


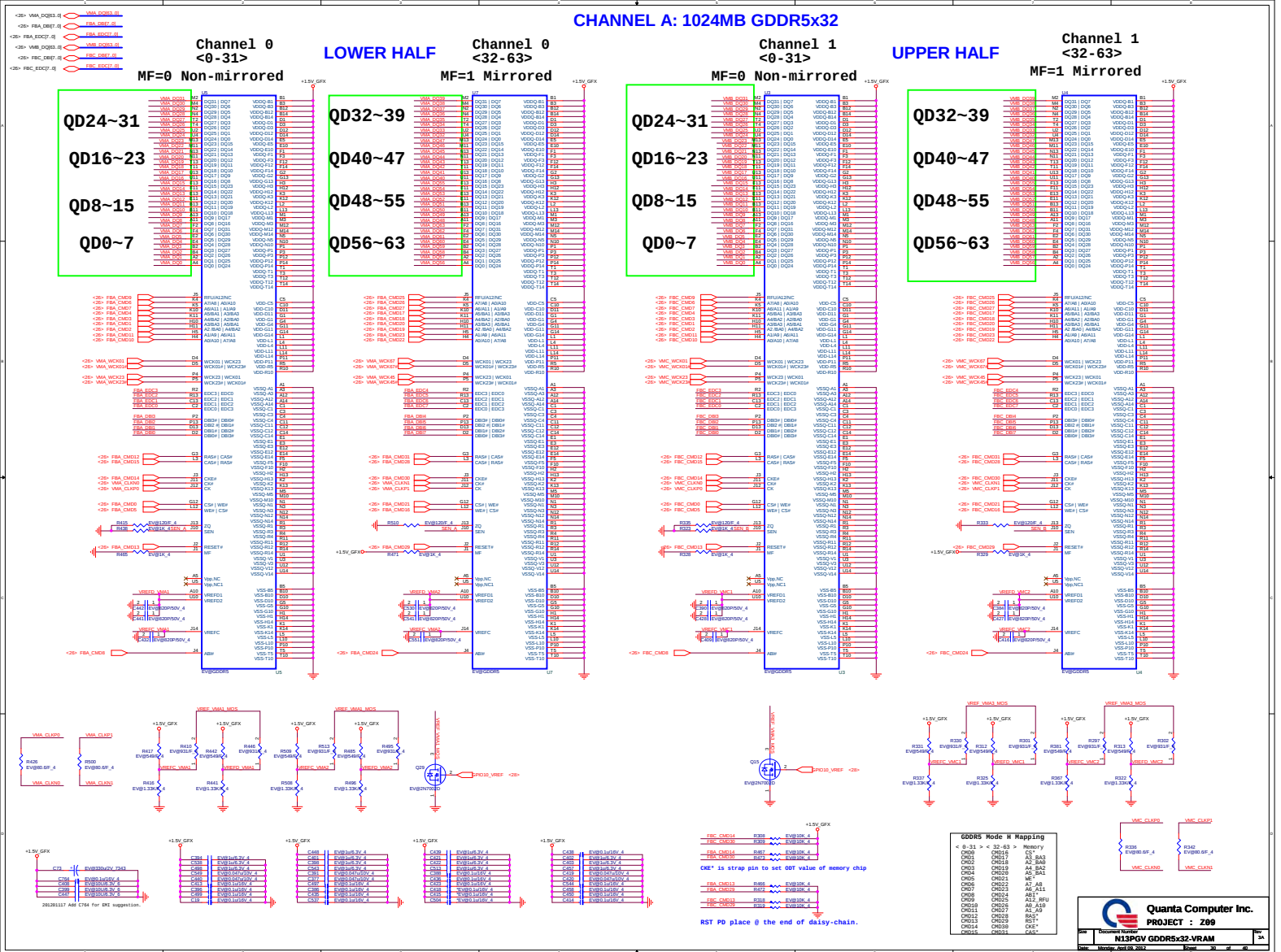
N13P-LP DID => 0X0FD3

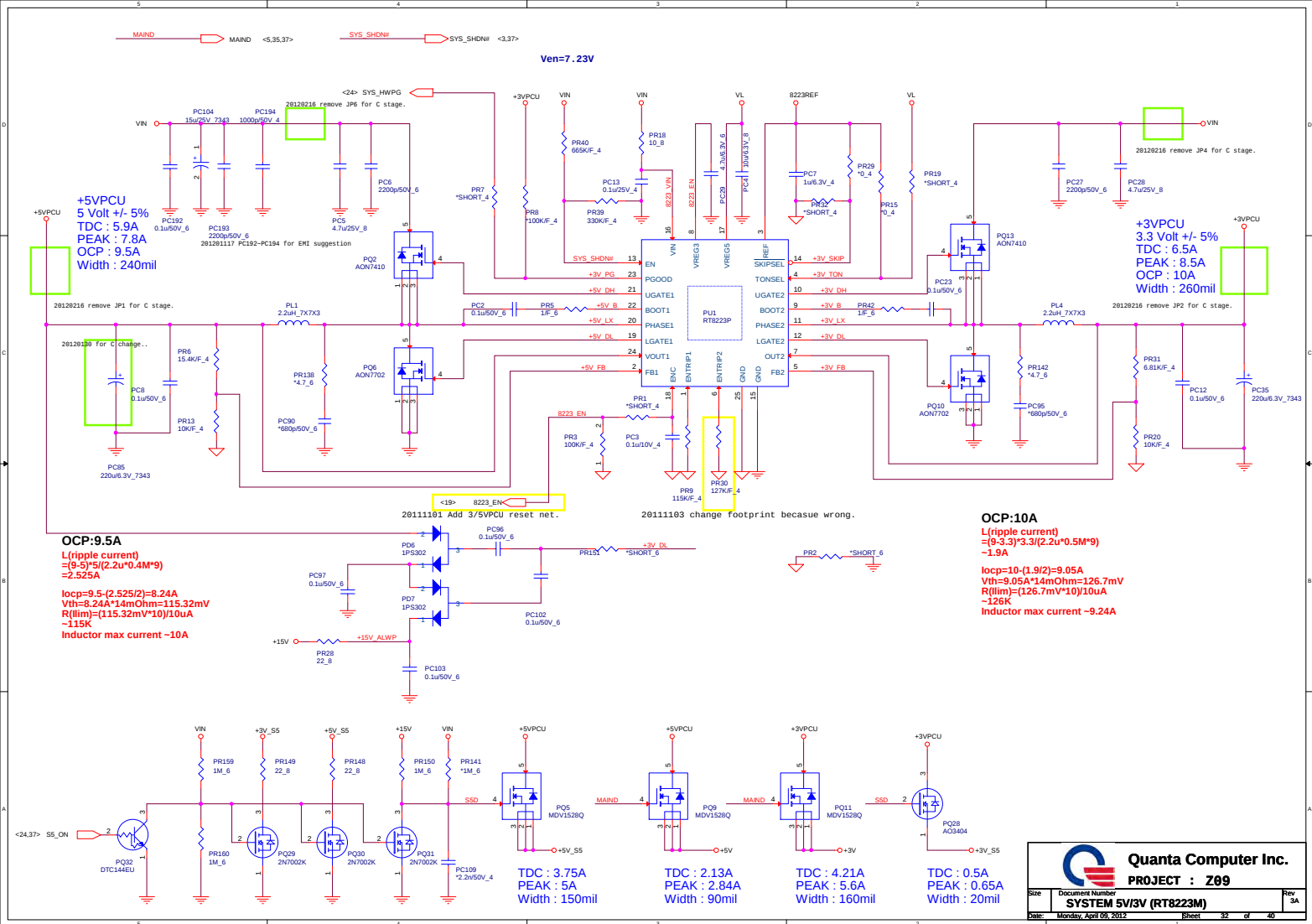
GK107:N13F

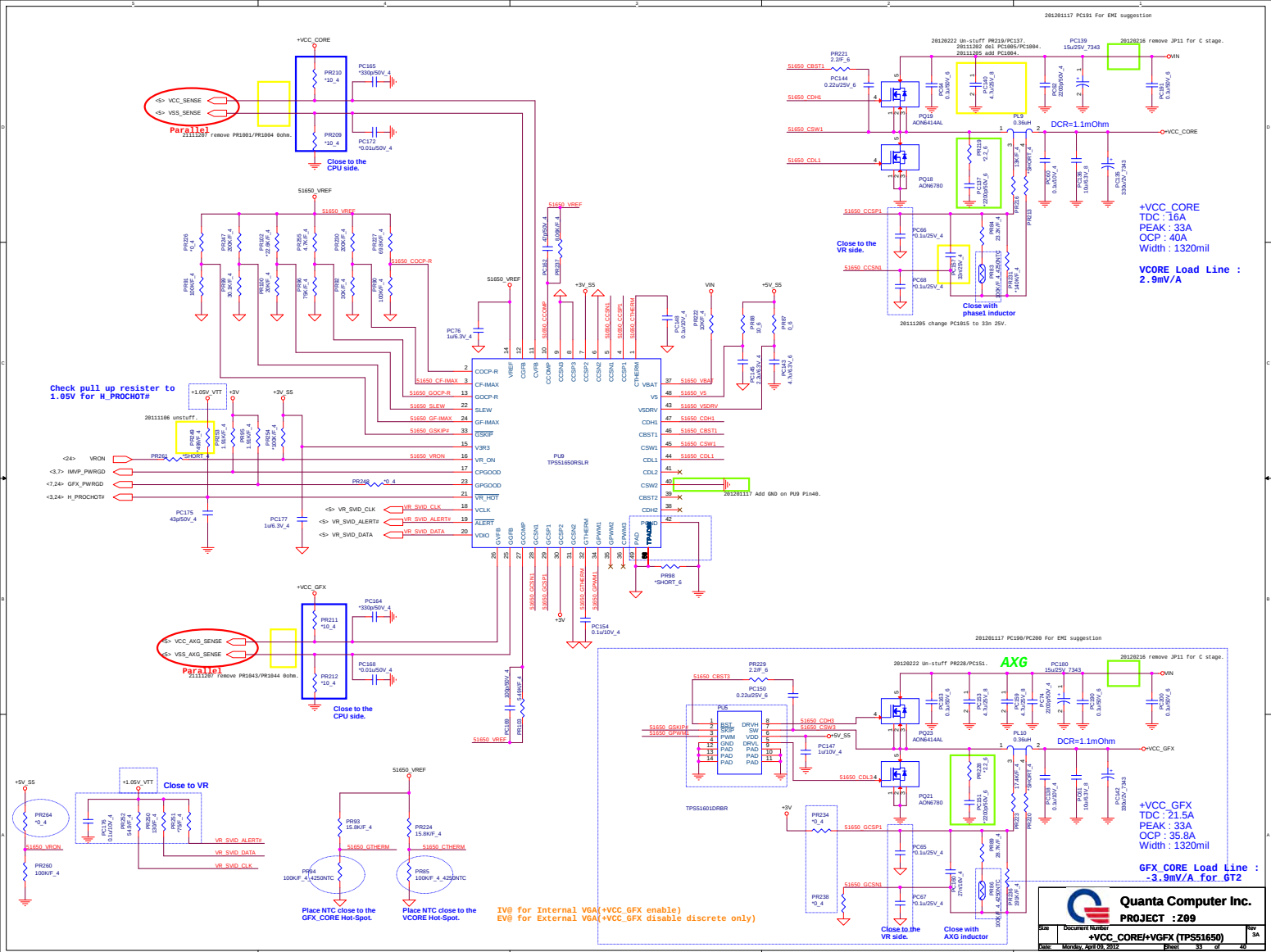
GPIO ASSIGNMENTS

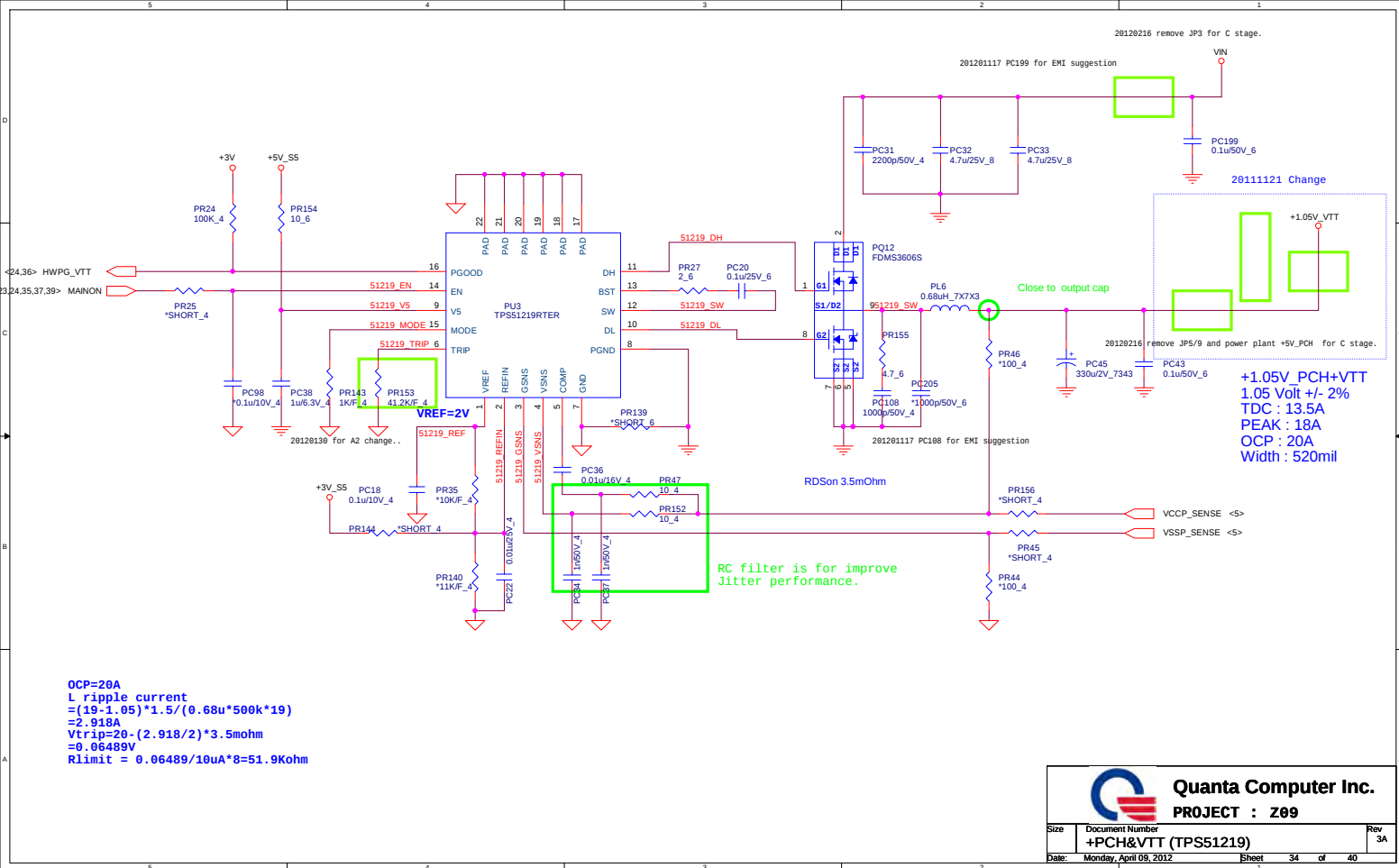












TDC : 0.75A
PEAK : 1A
Width : 40mil

TDC : 0.38A
PEAK : 0.5A
Width : 20mil

+SMDR_VREF

PC181
0.22u/10V_4

PR259
100K/F_4

20120130 for A2 change.. VREF=1.8V

PC174
0.1u/10V_4

PR104
10K/F_4

20120130 for A2 change..

PC171
0.01u/25V_4

PC184
10u/6.3V_8

PC185
10u/6.3V_8

20111109 remove PC2002

20111116 Add PC2002

Close to IC

Greater than or equal 40mil

+5VPCU

20120209 change power plant from +5V_S5 to +5VPCU.

PC161
1u/10V_4

20111109 remove Jump.

VIN

PC149
4.7u/25V_8

20111109 remove Jump.

+1.5V_SUS
1.5 Volt +/- 5%
TDC : 15A
PEAK : 18A
OCP : 20A
Width : 600mil

PC141
330u/2V_7343

PC146
1000p/50V_4

PC147
1000p/50V_4

PC148
1000p/50V_4

PC149
1000p/50V_4

PC150
1000p/50V_4

PC151
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PC152
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PC338
1000p/50V_4

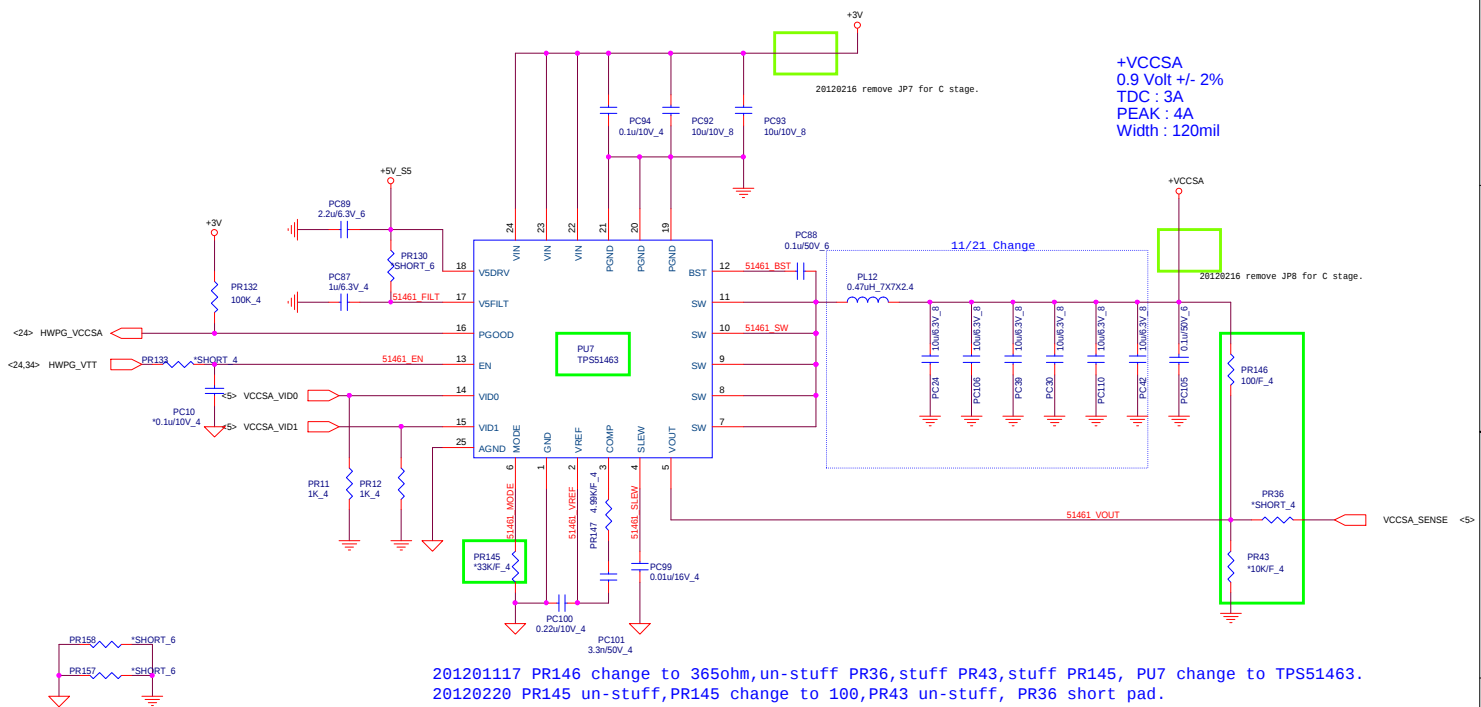
PC339
1000p/50V_4

PC340
1000p/50V_4

PC341
1000p/50V_4

PC342
1000p/50V_4

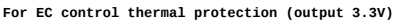
PC343
1000p/5

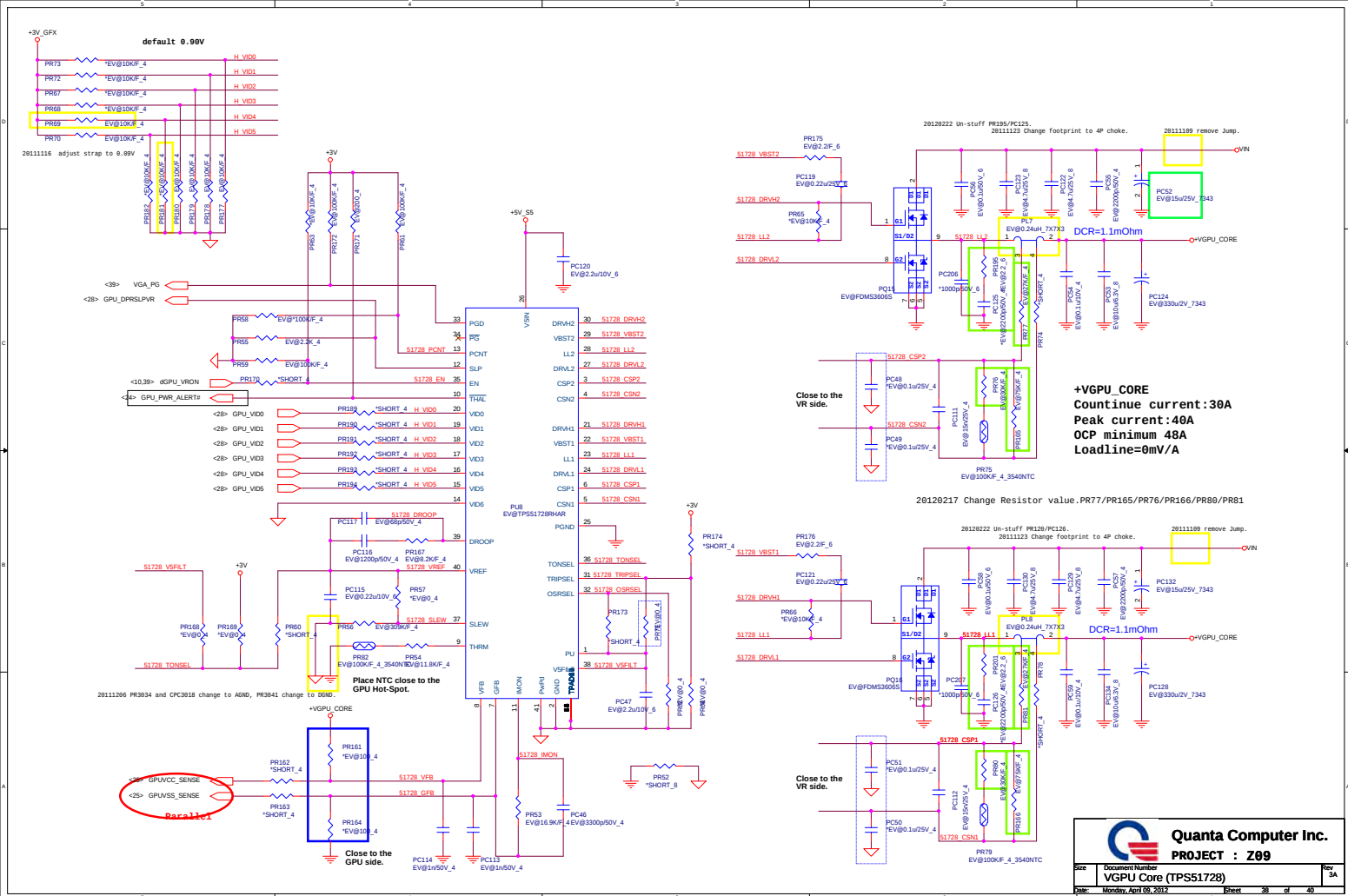


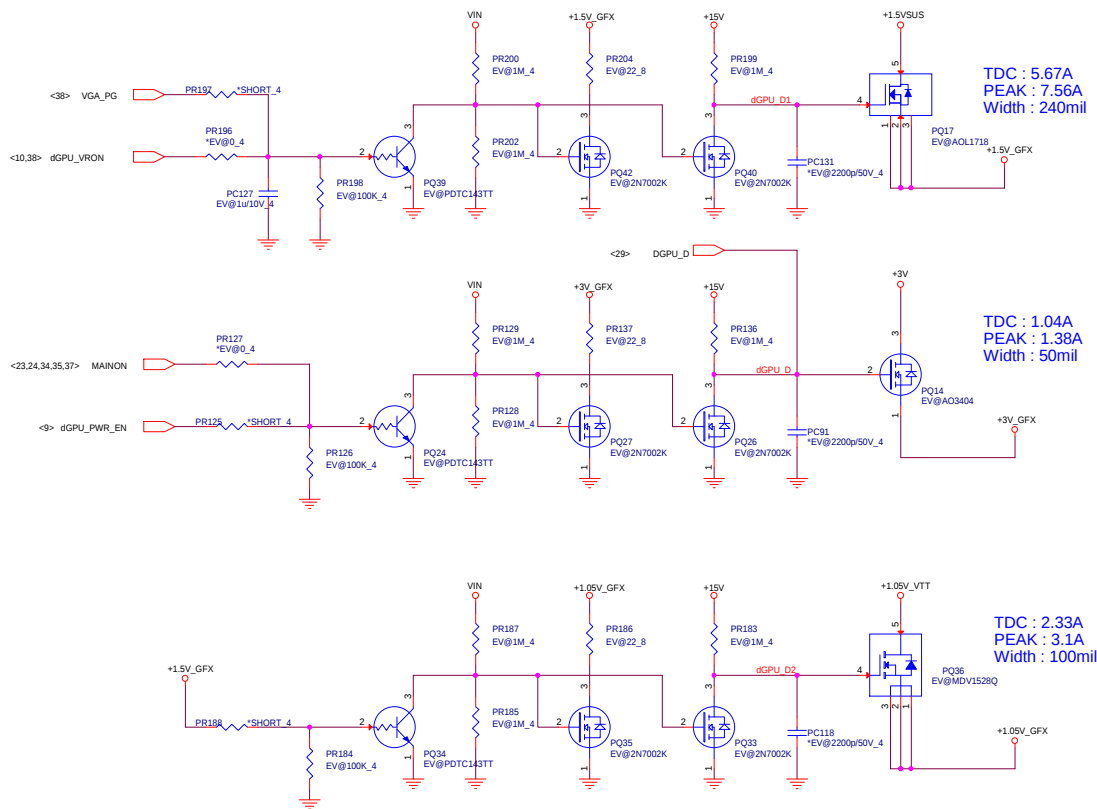
VID0	VID1	+VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

default 0.9V

PR145 33kohm
PR146 change to 365ohm
PR36 nc
PR43 10kohm
PU7 Change to 51463







[illegible]