PCB P/N AND DESCRIPTION

PCB ED5 MB(8L,309X218, REVA)
P/N: DA0ED5MB8A8

PCB ED5 MB(8L,309X218,REVB)
P/N: DA0ED5MB8B6

PCB ED5 USB/B(8L, 47.5X16.8, REVA)
P/N: DA0ED5SB8A5

PCB ED5 USB/B(8L,47.5X16.8,REVB)
P/N: DA0ED5SB8B3

ED5

SATA
ED5 SATA ASSY P/N
ED5 MB S/S ASSY P/N: 51ED5SS0018
ED5 MB C/S ASSY P/N: 41ED5CS0015
ED5 MB ASSY P/N: 31ED5MB0012

W/O ANT
ED5 USB/B S/S ASSY P/N: 4NED5SS0011
ED5 USB/B ASSY P/N: 3NED5UB0011

PATA
ED5 ASSY P/N
ED5 MB S/S ASSY P/N: 51ED5SS0000
ED5 MB C/S ASSY P/N: 41ED5CS0007
ED5 MB ASSY P/N: 31ED5MB0004

ANT
ED5 USB/B S/S ASSY P/N: 4NED5SS0002
ED5 USB/B ASSY P/N: 3NED5UB0003

VCC_CORE → **CPU VR** PG 30

+1.2V, +VCCP → **+1.2V +VCCP** PG 31

+1.8VSUS, +1.8V, SMDDR_VTERM → **+1.8VSUS SMDDR VTERM** PG 32

+3VPCU, +3V_S5, +3VSUS, +5VSUS, +5V, +12V → **3V/5V** PG 33

VIN → **CHARGER** PG 34

DDRII-SODIMM1 PG 7,8
DDRII-SODIMM2 PG 7,8
533/ 667 MHZ DDR II

AMD S1
Turion 64 Rev.F Dual-Core/ Sempron Rev.F Single-Core
Dual-Core 35W / Single-Core 25W
(638 S1g1 socket)
PG 3,4,5,6

HT_LINK

HOST 133/166MHz
PCIE 100MHz
VGA 96MHz
USB 48MHz
REF 14MHz

CLOCK GENERATOR
ICS951462
PG 13

Panel Connector PG 20 — LVDS
S-Video PG 20 — TVOUT
VGA PG 20 — VGA

RS485
465 FCBGA
PG 9,10,11,12

PG 19

PCI-E, 1X → **Express Card** PCIE1 & USB4 NEW CARD PG 24

PCI-E, 1X → **Mini PCI-E Card (WLAN)** PCIE2 PCI Express Mini Card PG 19

PCI-E, 1X → **Mini PCI-E Card (TV)** PCIE3 & USB5 PCI Express Mini Card PG 19

WIRE

PCI-E, 1X → **LAN RTL8111B-GR** PCIE0 PG 23 — **Magnetics** — **RJ45**

A_LINK

SATA - HDD PG 21
PATA - HDD PG 21
SATA0
PATA 100

Internal ODD CD-ROM PG 21

Azalia

SB460
549 BGA
PG 14,15,16,17

USB2.0 (P0~P7)

Bluetooth USB7 PG 22

B/B CN. USB2 & USB3 PG 22

USB2.0 I/O Ports USB0 & USB1 PG 22

DSC USB I/F USB6 PG 22

ANTENNA JACK

USB2.0 I/O

USB DAUGHTERBOARD

PCI Bus 33MHz

TI PCI8402
AD17
REQ3#, GNT3#
INTE#, INTG#, INTH#
PG 24,25

MINI PCI CN.
AD20
REQ2#, GNT2#
INTF#, INTG#
DEBUG PURPOSE ONLY PG 18

Card Reader PG 25

IEEE1394 CN. PG 25

Azalia Audio PG 26

Amplifier MAX9755A PG 27

Azalia MDC PG 26

MIC. PG 27
INT. S.P. PG 27
H.P PG 27
MODEM RJ 11 PG 23

LPC

KBC
NS97551
PG 28

SWITCH LED PG 29

X-Bus

K/B CONN. PG 29
Touch Pad PG 29
Flash ROM PG 28

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Quanta Computer Inc.

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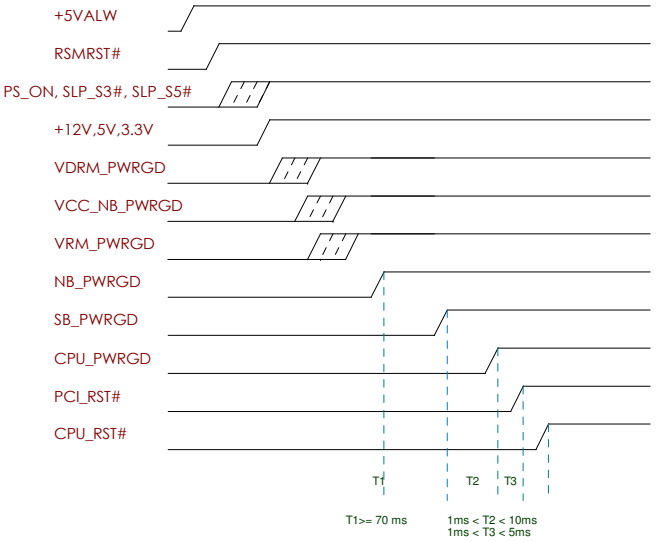
SYSTEM	+12V	+12V	OFF IN S3-S5	PLANE	41
	-12V	-12V	OFF IN S3-S5	TRACE 20 MIL	41
	+5V	+5V	OFF IN S3-S5	PLANE	41
	+3.3V	+3.3V	OFF IN S3-S5	PLANE	41
	+5VALW	+5V	S0-S5	PLANE/ 50 MIL	41
	+3.3VALW	+3.3V	S0-S5	TRACE 30 MIL	41
	+1.8VALW	+2.5V	S0-S5	TRACE 30 MIL	21
	+5V_DUAL	+5V	S0-S5	PLANE/ 100 MIL	41
	+3.3V_DUAL	+3.3V	S0-S5	PLANE/ 50 MIL	41
CPU	VCCCORE	VID[0..6]	OFF IN S3-S5	PLANE+COPER	37
	VCCP	+1.05V	OFF IN S3-S5	PLANE+COPER	38
	VCCA	+1.5V	OFF IN S3-S5	TRACE 20 MIL	38
RC485 NB	VCC_NB	+1.2V/1.0V	OFF IN S3-S5	PLANE+COPER	39
	VDD_CPU	+1.05V	OFF IN S3-S5	PLANE+COPER	38
	VDD_MEM	+1.8V	S0-S3	PLANE+COPER	40
	VDD18	+1.8V	OFF IN S3-S5	TRACE 20 MIL	12
	VDDA18	+1.8V	OFF IN S3-S5	COPPER	12
	VDDA12	+1.2V	OFF IN S3-S5	PLANE+COPPER	12
	AVDD	+3.3V	OFF IN S3-S5	TRACE 20 MIL	11
	AVDDQ	+1.8V	OFF IN S3-S5	TRACE 20 MIL	11
	PLVDD	+1.8V	OFF IN S3-S5	TRACE 20 MIL	11
	LPVDD	+1.8V	OFF IN S3-S5	TRACE 20 MIL	11
	LVDDR	+1.8V	OFF IN S3-S5	TRACE 30 MIL	11
	VDDR3	+3.3V	OFF IN S3-S5	TRACE 30 MIL	11
	VTT_DDR	+0.9V	OFF IN S3-S5	COPPER	40
	VDD_CLK	+3.3V	OFF IN S3-S5	COPPER	14
SB460 SB	+3.3V_SB	+3.3V	OFF IN S3-S5	PLANE	21
	+1.8V_SB	+1.8V	OFF IN S3-S5	PLANE	21
	+3.3VALW_SB	+3.3V	S0-S5	PLANE	21
	+1.8VALW_SB	+1.8V	S0-S5	PLANE	21
	+1.8V_SUB_PHY	+1.8V	S0-S5	TRACE 30 MIL	21
	AVDD_CK	+1.8V	OFF IN S3-S5	TRACE 10 MIL	21
	V5_REF	+5V	OFF IN S3-S5	TRACE 10 MIL	21
	CPU-PWR	+1.05V	OFF IN S3-S5	TRACE 20 MIL	21
	PCIE_PVDD	+1.8V	OFF IN S3-S5	TRACE 20 MIL	18
	PCIE_VDDR	+1.8V	OFF IN S3-S5	PLANE+COPER	18
	+1.8V_ATA	+1.8V	OFF IN S3-S5	PLANE	20
	PLLVDD_ATA	+1.8V	OFF IN S3-S5	TRACE 20 MIL	20
	XTLVDD_ATA	+1.8V	OFF IN S3-S5	TRACE 20 MIL	20
	AVDD_USB_TX	+1.8V	S0-S5	PLANE+COPER	19
	AVDD_USB_RX	+1.8V	S0-S5	PLANE+COPER	19
	+3.3V_AVDDC	+3.3V	S0-S5	TRACE 20 MIL	19
	V_BAT	+3.0V	--	TRACE 10 MIL	18

BONEFISH POWER UP SEQUENCE



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Quanta Computer Inc.

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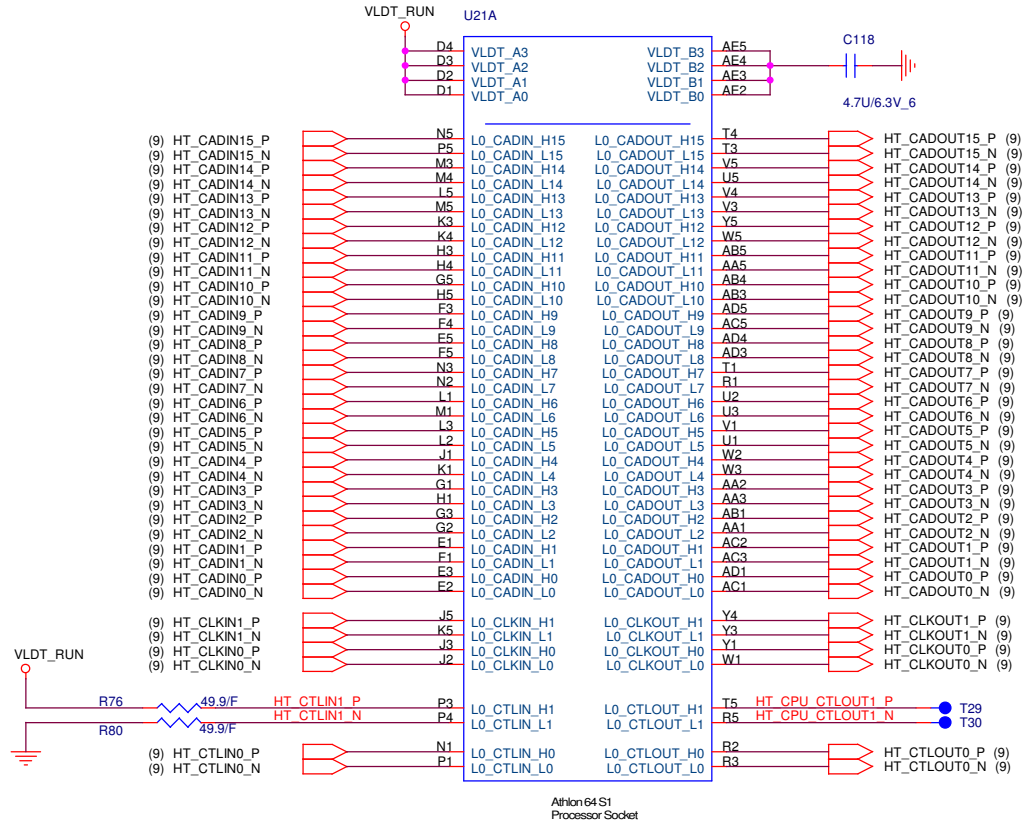
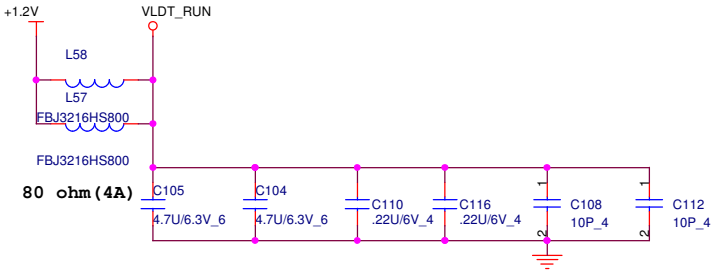
PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE





LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

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Quanta Computer Inc.

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Processor DDR2 Memory Interface

VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

PLACE THEM CLOSE TO CPU WITHIN 1"

+1.8VSUS

R140 2K/F

CPU_M_VREF

C180 .1U_4

C181 1000p/50V_4

R141 2K/F

+1.8VSUS

R363 39.2F

R365 39.2F

T45

VTT_SENSE

M_ZN

M_ZP

+0.9V_VTER

U21B

W17 MEMVREF

Y10 VTT_SENSE

AE10 MEMZN

AF10 MEMZP

VTT1 D10
VTT2 C10
VTT3 B10
VTT4 AD10
VTT5 W10
VTT6 AC10
VTT7 AB10
VTT8 AA10
VTT9 A10

(7,8) M_A_CS#3 V19 MA0_CS_L3
(7,8) M_A_CS#2 J22 MA0_CS_L2
(7,8) M_A_CS#1 V22 MA0_CS_L1
(7,8) M_A_CS#0 T19 MA0_CS_L0

MA0_CLK_H2 Y16 M_CLKOUT1 (7)
MA0_CLK_L2 AA16 M_CLKOUT1# (7)
MA0_CLK_H1 E16 M_CLKOUT0 (7)
MA0_CLK_L1 E16 M_CLKOUT0# (7)

(7,8) M_B_CS#3 Y26 MB0_CS_L3
(7,8) M_B_CS#2 J24 MB0_CS_L2
(7,8) M_B_CS#1 W24 MB0_CS_L1
(7,8) M_B_CS#0 U23 MB0_CS_L0

MB0_CLK_H2 AF18 M_CLKOUT4 (7)
MB0_CLK_L2 AF17 M_CLKOUT4# (7)
MB0_CLK_H1 A17 M_CLKOUT3 (7)
MB0_CLK_L1 A18 M_CLKOUT3# (7)

(7,8) M_CKE3 H26 MB_CKE1
(7,8) M_CKE2 J23 MB_CKE0
(7,8) M_CKE1 J20 MA_CKE1
(7,8) M_CKE0 J21 MA_CKE0

MB0_ODT1 W23 M_ODT3 (7,8)
MB0_ODT0 W26 M_ODT2 (7,8)
MA0_ODT1 V20 M_ODT1 (7,8)
MA0_ODT0 U19 M_ODT0 (7,8)

(7,8) M_A_A[0..15]

M_A_A15 K19 MA_ADD15
M_A_A14 K20 MA_ADD14
M_A_A13 V24 MA_ADD13
M_A_A12 K24 MA_ADD12
M_A_A11 L20 MA_ADD11
M_A_A10 R19 MA_ADD10
M_A_A9 L19 MA_ADD9
M_A_A8 L22 MA_ADD8
M_A_A7 L21 MA_ADD7
M_A_A6 M19 MA_ADD6
M_A_A5 M20 MA_ADD5
M_A_A4 M24 MA_ADD4
M_A_A3 M22 MA_ADD3
M_A_A2 N22 MA_ADD2
M_A_A1 N21 MA_ADD1
M_A_A0 R21 MA_ADD0

MB_ADD15 J25 M_B_A15
MB_ADD14 J26 M_B_A14
MB_ADD13 W25 M_B_A13
MB_ADD12 L23 M_B_A12
MB_ADD11 L25 M_B_A11
MB_ADD10 U25 M_B_A10
MB_ADD9 L24 M_B_A9
MB_ADD8 M26 M_B_A8
MB_ADD7 L26 M_B_A7
MB_ADD6 N23 M_B_A6
MB_ADD5 N24 M_B_A5
MB_ADD4 N25 M_B_A4
MB_ADD3 N26 M_B_A3
MB_ADD2 P24 M_B_A2
MB_ADD1 P26 M_B_A1
MB_ADD0 T24 M_B_A0

M_B_A[0..15] (7,8)

(7,8) M_A_BS#2 K22 MA_BANK2
(7,8) M_A_BS#1 R20 MA_BANK1
(7,8) M_A_BS#0 T22 MA_BANK0

MB_BANK2 K26 M_B_BS#2 (7,8)
MB_BANK1 T26 M_B_BS#1 (7,8)
MB_BANK0 U26 M_B_BS#0 (7,8)

(7,8) M_A_RAS# T20 MA_RAS_L
(7,8) M_A_CAS# U20 MA_CAS_L
(7,8) M_A_WE# U21 MA_WE_L

MB_RAS_L U24 M_B_RAS# (7,8)
MB_CAS_L V26 M_B_CAS# (7,8)
MB_WE_L U22 M_B_WE# (7,8)

DDR II: CMD/CTRL/CLK

Athlon 64 S1
Processor Socket

+0.9V_VTER

C150 4.7U/6.3V_6
C157 4.7U/6.3V_6
C132 4.7U/6.3V_6
C151 4.7U/6.3V_6
C133 .22U/6V_4
C145 .22U/6V_4
C148 .22U/6V_4
C135 .22U/6V_4
C137 1000p/50V_4
C153 1000p/50V_4
C154 1000p/50V_4
C144 1000p/50V_4
C136 180P_4
C134 180P_4
C147 180P_4
C138 180P_4

To SODIMM socket B (Far)

To SODIMM socket A (near)

U21C

(7) M_B_DQ[0..63]

M_B_DQ63 AD11 MB_DATA63
M_B_DQ62 AF11 MB_DATA62
M_B_DQ61 AE14 MB_DATA61
M_B_DQ60 AE14 MB_DATA60
M_B_DQ59 Y11 MB_DATA59
M_B_DQ58 AB11 MB_DATA58
M_B_DQ57 AC12 MB_DATA57
M_B_DQ56 AF13 MB_DATA56
M_B_DQ55 AF15 MB_DATA55
M_B_DQ54 AF16 MB_DATA54
M_B_DQ53 AC18 MB_DATA53
M_B_DQ52 AF19 MB_DATA52
M_B_DQ51 AD14 MB_DATA51
M_B_DQ50 AC14 MB_DATA50
M_B_DQ49 AE18 MB_DATA49
M_B_DQ48 AD18 MB_DATA48
M_B_DQ47 AD20 MB_DATA47
M_B_DQ46 AC20 MB_DATA46
M_B_DQ45 AF23 MB_DATA45
M_B_DQ44 AF24 MB_DATA44
M_B_DQ43 AF20 MB_DATA43
M_B_DQ42 AE20 MB_DATA42
M_B_DQ41 AD22 MB_DATA41
M_B_DQ40 AC22 MB_DATA40
M_B_DQ39 AE25 MB_DATA39
M_B_DQ38 AD26 MB_DATA38
M_B_DQ37 AA25 MB_DATA37
M_B_DQ36 AA26 MB_DATA36
M_B_DQ35 AE24 MB_DATA35
M_B_DQ34 AD24 MB_DATA34
M_B_DQ33 AA23 MB_DATA33
M_B_DQ32 AA24 MB_DATA32
M_B_DQ31 G24 MB_DATA31
M_B_DQ30 G23 MB_DATA30
M_B_DQ29 D26 MB_DATA29
M_B_DQ28 C26 MB_DATA28
M_B_DQ27 G26 MB_DATA27
M_B_DQ26 G25 MB_DATA26
M_B_DQ25 E24 MB_DATA25
M_B_DQ24 E23 MB_DATA24
M_B_DQ23 C24 MB_DATA23
M_B_DQ22 B24 MB_DATA22
M_B_DQ21 C20 MB_DATA21
M_B_DQ20 B20 MB_DATA20
M_B_DQ19 C25 MB_DATA19
M_B_DQ18 D24 MB_DATA18
M_B_DQ17 A21 MB_DATA17
M_B_DQ16 D20 MB_DATA16
M_B_DQ15 D18 MB_DATA15
M_B_DQ14 C18 MB_DATA14
M_B_DQ13 D14 MB_DATA13
M_B_DQ12 C14 MB_DATA12
M_B_DQ11 A20 MB_DATA11
M_B_DQ10 A19 MB_DATA10
M_B_DQ9 A16 MB_DATA9
M_B_DQ8 A15 MB_DATA8
M_B_DQ7 A13 MB_DATA7
M_B_DQ6 D12 MB_DATA6
M_B_DQ5 E11 MB_DATA5
M_B_DQ4 G11 MB_DATA4
M_B_DQ3 B14 MB_DATA3
M_B_DQ2 A14 MB_DATA2
M_B_DQ1 A11 MB_DATA1
M_B_DQ0 C11 MB_DATA0

MA_DATA63 AA12 M_A_DQ63
MA_DATA62 AB12 M_A_DQ62
MA_DATA61 AA14 M_A_DQ61
MA_DATA60 AB14 M_A_DQ60
MA_DATA59 W11 M_A_DQ59
MA_DATA58 Y12 M_A_DQ58
MA_DATA57 AD13 M_A_DQ57
MA_DATA56 AB13 M_A_DQ56
MA_DATA55 AD15 M_A_DQ55
MA_DATA54 AB15 M_A_DQ54
MA_DATA53 AB17 M_A_DQ53
MA_DATA52 Y17 M_A_DQ52
MA_DATA51 Y14 M_A_DQ51
MA_DATA50 W14 M_A_DQ50
MA_DATA49 W16 M_A_DQ49
MA_DATA48 AD17 M_A_DQ48
MA_DATA47 Y18 M_A_DQ47
MA_DATA46 AD19 M_A_DQ46
MA_DATA45 AD21 M_A_DQ45
MA_DATA44 AB21 M_A_DQ44
MA_DATA43 AB18 M_A_DQ43
MA_DATA42 AA18 M_A_DQ42
MA_DATA41 AA20 M_A_DQ41
MA_DATA40 Y20 M_A_DQ40
MA_DATA39 AA22 M_A_DQ39
MA_DATA38 Y22 M_A_DQ38
MA_DATA37 W21 M_A_DQ37
MA_DATA36 W22 M_A_DQ36
MA_DATA35 AA21 M_A_DQ35
MA_DATA34 AB22 M_A_DQ34
MA_DATA33 AB24 M_A_DQ33
MA_DATA32 Y24 M_A_DQ32
MA_DATA31 H22 M_A_DQ31
MA_DATA30 H20 M_A_DQ30
MA_DATA29 E22 M_A_DQ29
MA_DATA28 E21 M_A_DQ28
MA_DATA27 J19 M_A_DQ27
MA_DATA26 H24 M_A_DQ26
MA_DATA25 F22 M_A_DQ25
MA_DATA24 F20 M_A_DQ24
MA_DATA23 C23 M_A_DQ23
MA_DATA22 B22 M_A_DQ22
MA_DATA21 F18 M_A_DQ21
MA_DATA20 E18 M_A_DQ20
MA_DATA19 E20 M_A_DQ19
MA_DATA18 D22 M_A_DQ18
MA_DATA17 C19 M_A_DQ17
MA_DATA16 B18 M_A_DQ16
MA_DATA15 G17 M_A_DQ15
MA_DATA14 C17 M_A_DQ14
MA_DATA13 F14 M_A_DQ13
MA_DATA12 E14 M_A_DQ12
MA_DATA11 H17 M_A_DQ11
MA_DATA10 E17 M_A_DQ10
MA_DATA9 E15 M_A_DQ9
MA_DATA8 H15 M_A_DQ8
MA_DATA7 E13 M_A_DQ7
MA_DATA6 C13 M_A_DQ6
MA_DATA5 H12 M_A_DQ5
MA_DATA4 H11 M_A_DQ4
MA_DATA3 G14 M_A_DQ3
MA_DATA2 H14 M_A_DQ2
MA_DATA1 F12 M_A_DQ1
MA_DATA0 G12 M_A_DQ0

M_A_DQ[0..63] (7)

(7) M_B_DM[0..7]

M_B_DM7 AD12 MB_DM7
M_B_DM6 AC16 MB_DM6
M_B_DM5 AE22 MB_DM5
M_B_DM4 AB26 MB_DM4
M_B_DM3 E25 MB_DM3
M_B_DM2 A22 MB_DM2
M_B_DM1 B16 MB_DM1
M_B_DM0 A12 MB_DM0

MA_DM7 Y13 M_A_DM7
MA_DM6 AB16 M_A_DM6
MA_DM5 Y19 M_A_DM5
MA_DM4 AC24 M_A_DM4
MA_DM3 F24 M_A_DM3
MA_DM2 E19 M_A_DM2
MA_DM1 C15 M_A_DM1
MA_DM0 E12 M_A_DM0

M_A_DM[0..7] (7)

M_B_DQS7 AE12 MB_DQS_H7
M_B_DQS#7 AE12 MB_DQS_L7
M_B_DQS6 AE16 MB_DQS_H6
M_B_DQS#6 AD16 MB_DQS_L6
M_B_DQS5 AF21 MB_DQS_H5
M_B_DQS#5 AF22 MB_DQS_L5
M_B_DQS4 AC25 MB_DQS_H4
M_B_DQS#4 AC26 MB_DQS_L4
M_B_DQS3 F26 MB_DQS_H3
M_B_DQS#3 F26 MB_DQS_L3
M_B_DQS2 A24 MB_DQS_H2
M_B_DQS#2 A23 MB_DQS_L2
M_B_DQS1 D16 MB_DQS_H1
M_B_DQS#1 C16 MB_DQS_L1
M_B_DQS0 C12 MB_DQS_H0
M_B_DQS#0 B12 MB_DQS_L0

MA_DQS_H7 W12 M_A_DQS7
MA_DQS_L7 W13 M_A_DQS#7
MA_DQS_H6 Y15 M_A_DQS6
MA_DQS_L6 W15 M_A_DQS#6
MA_DQS_H5 AB19 M_A_DQS5
MA_DQS_L5 AB20 M_A_DQS#5
MA_DQS_H4 AD23 M_A_DQS4
MA_DQS_L4 AC23 M_A_DQS#4
MA_DQS_H3 G22 M_A_DQS3
MA_DQS_L3 G21 M_A_DQS#3
MA_DQS_H2 C22 M_A_DQS2
MA_DQS_L2 C21 M_A_DQS#2
MA_DQS_H1 G16 M_A_DQS1
MA_DQS_L1 G15 M_A_DQS#1
MA_DQS_H0 G13 M_A_DQS0
MA_DQS_L0 H13 M_A_DQS#0

DDR: DATA

Athlon 64 S1
Processor Socket

(7) M_B_DQS[0..7]

M_B_DQS0
M_B_DQS1
M_B_DQS2
M_B_DQS3
M_B_DQS4
M_B_DQS5
M_B_DQS6
M_B_DQS7

(7) M_B_DQS#[0..7]

M_B_DQS#0
M_B_DQS#1
M_B_DQS#2
M_B_DQS#3
M_B_DQS#4
M_B_DQS#5
M_B_DQS#6
M_B_DQS#7

(7) M_A_DQS[0..7]

M_A_DQS0
M_A_DQS1
M_A_DQS2
M_A_DQS3
M_A_DQS4
M_A_DQS5
M_A_DQS6
M_A_DQS7

(7) M_A_DQS#[0..7]

M_A_DQS#0
M_A_DQS#1
M_A_DQS#2
M_A_DQS#3
M_A_DQS#4
M_A_DQS#5
M_A_DQS#6
M_A_DQS#7

PROJECT : ED5
Quanta Computer Inc.

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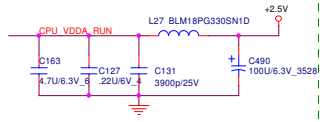
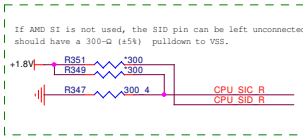
ATHLON Control and Debug

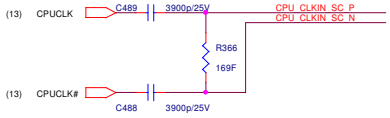
LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

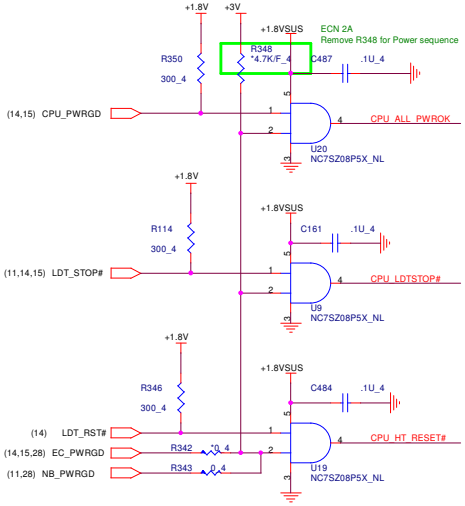
CPU_VDDA_RUN



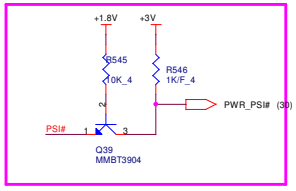
If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pulldown to VSS.

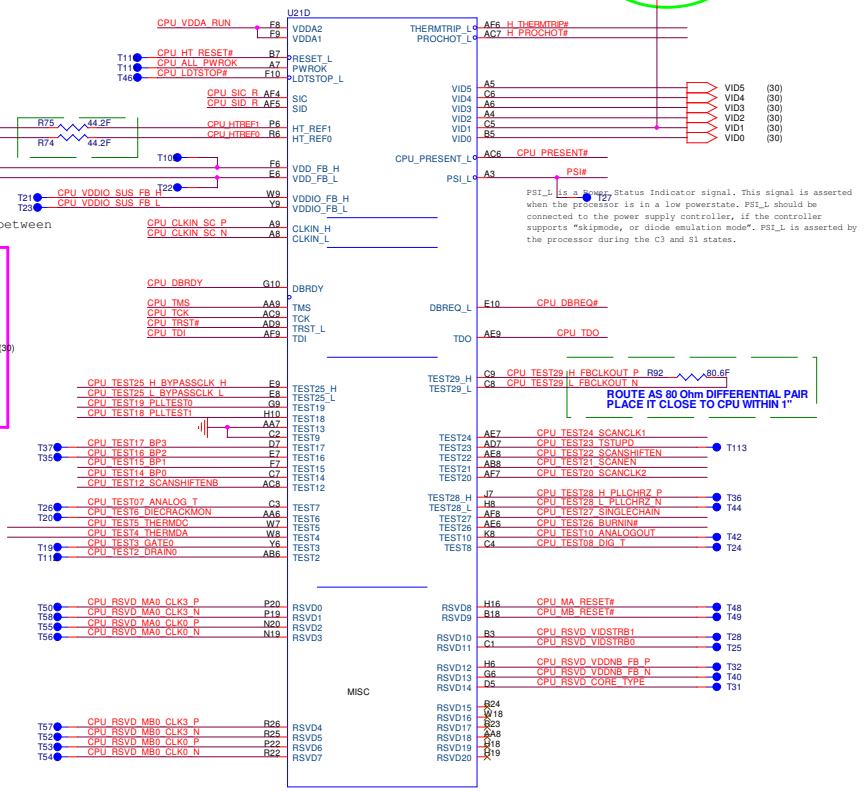


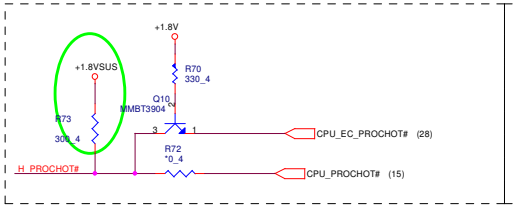


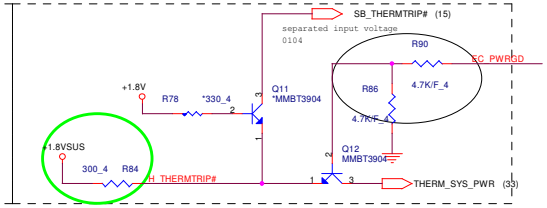


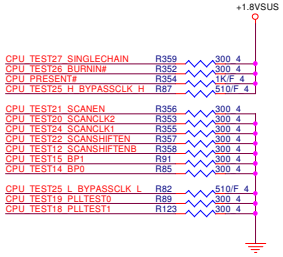
D3A:Add LEVEL-SHIFT circuit on PSI# that between CPU and POWER



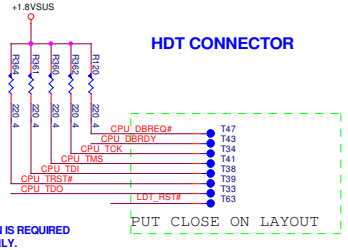






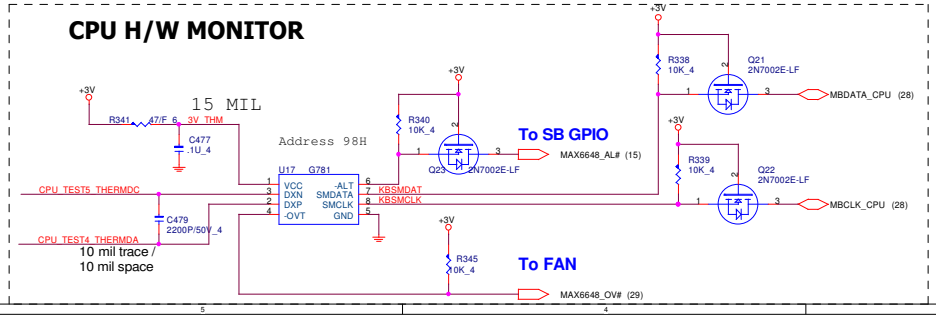


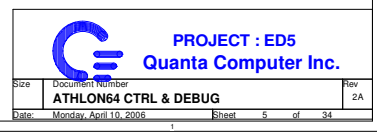
IF no use which Net need pull-up or down

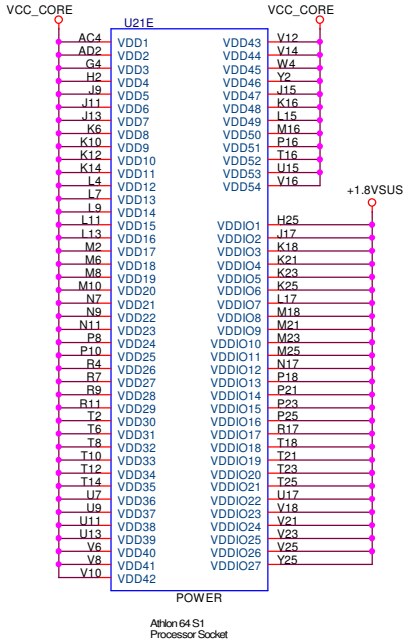


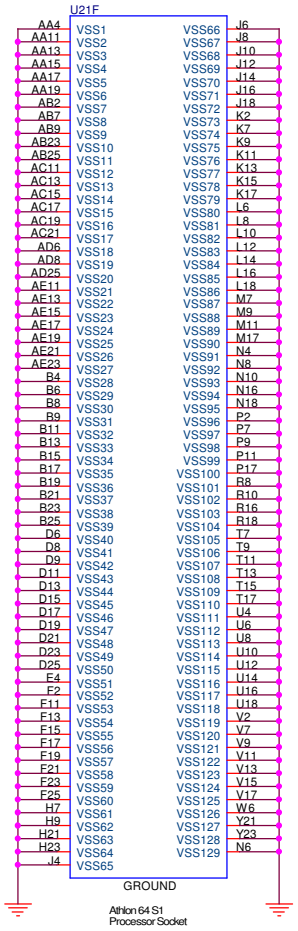
NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.

CPU H/W MONITOR

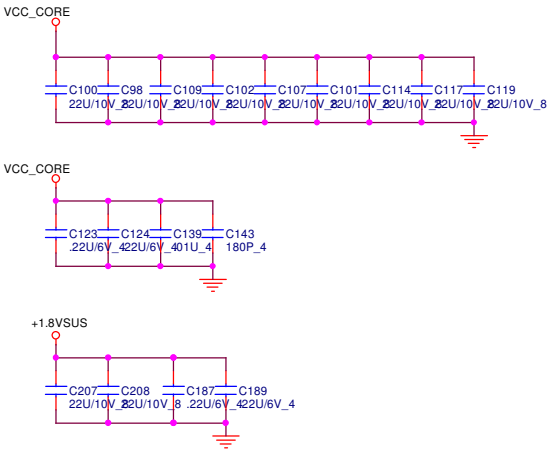




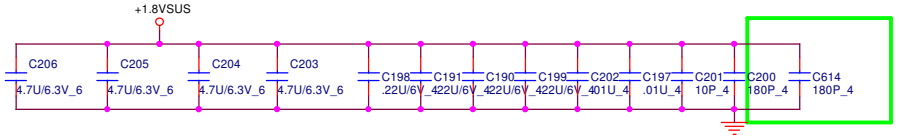


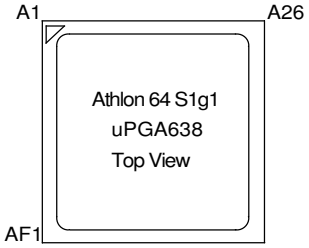


BOTTOMSIDE DECOUPLING



DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE





PROCESSOR POWER AND GROUND

PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
	ATHLON64 PWR & GND	1A
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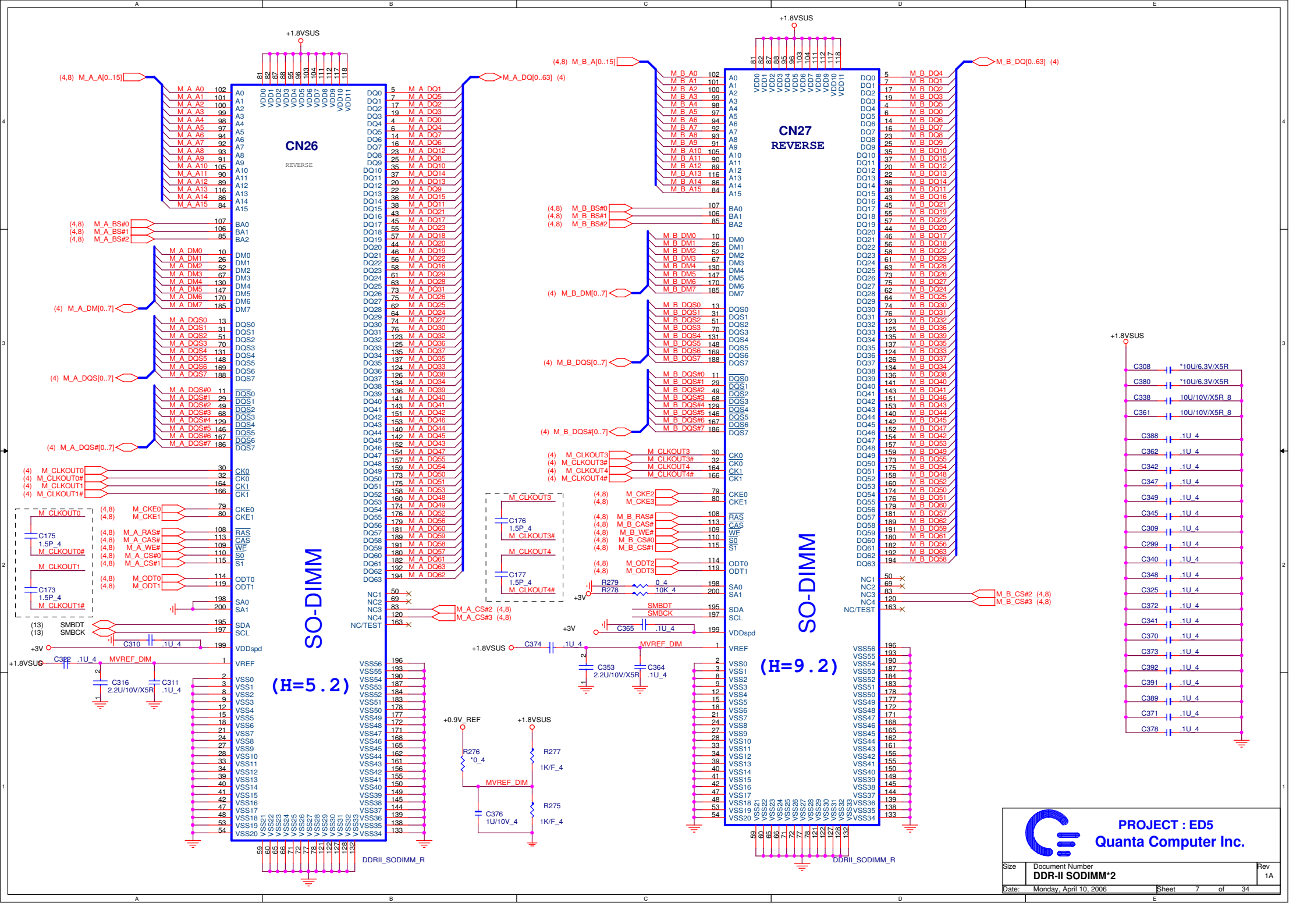
CN26
REVERSE
SO-DIMM
(H=5.2)
CN27
REVERSE
SO-DIMM
(H=9.2)
+1.8VSUS
+3V
+0.9V_REF
M_A_A[0..15]
M_A_DQ[0..63]
M_A_BS#0
M_A_BS#1
M_A_BS#2
M_A_DM[0..7]
M_A_DQS[0..7]
M_A_DQS#[0..7]
M_CLKOUT0
M_CLKOUT0#
M_CLKOUT1
M_CLKOUT1#
M_CLKOUT3
M_CLKOUT3#
M_CLKOUT4
M_CLKOUT4#
M_CKE0
M_CKE1
M_A_RAS#
M_A_CAS#
M_A_WE#
M_A_CS#0
M_A_CS#1
M_ODT0
M_ODT1
SMBDT
SMBCK
MVREF_DIM
M_A_CS#2 (4,8)
M_A_CS#3 (4,8)
M_B_A[0..15]
M_B_DQ[0..63]
M_B_BS#0
M_B_BS#1
M_B_BS#2
M_B_DM[0..7]
M_B_DQS[0..7]
M_B_DQS#[0..7]
M_CKE2
M_CKE3
M_B_RAS#
M_B_CAS#
M_B_WE#
M_B_CS#0
M_B_CS#1
M_ODT2
M_ODT3
M_B_CS#2 (4,8)
M_B_CS#3 (4,8)
C175 1.5P_4
C173 1.5P_4
C310 .1U_4
C309 .1U_4
C316 2.2U/10V/X5R
C311 .1U_4
C176 1.5P_4
C177 1.5P_4
C374 .1U_4
C353 2.2U/10V/X5R
C364 .1U_4
C365 .1U_4
C376 1U/10V_4
R276 *0_4
R277 1K/F_4
R275 1K/F_4
R279 0_4
R278 10K_4
C308 *10U/6.3V/X5R
C380 *10U/6.3V/X5R
C338 10U/10V/X5R_8
C361 10U/10V/X5R_8
C388 .1U_4
C362 .1U_4
C342 .1U_4
C347 .1U_4
C349 .1U_4
C345 .1U_4
C309 .1U_4
C299 .1U_4
C340 .1U_4
C348 .1U_4
C325 .1U_4
C372 .1U_4
C341 .1U_4
C370 .1U_4
C373 .1U_4
C392 .1U_4
C391 .1U_4
C389 .1U_4
C371 .1U_4
C378 .1U_4
DDRII_SODIMM_R
PROJECT : ED5
Quanta Computer Inc.
Size
Document Number
DDR-II SODIMM*2
Rev
1A
Date: Monday, April 10, 2006
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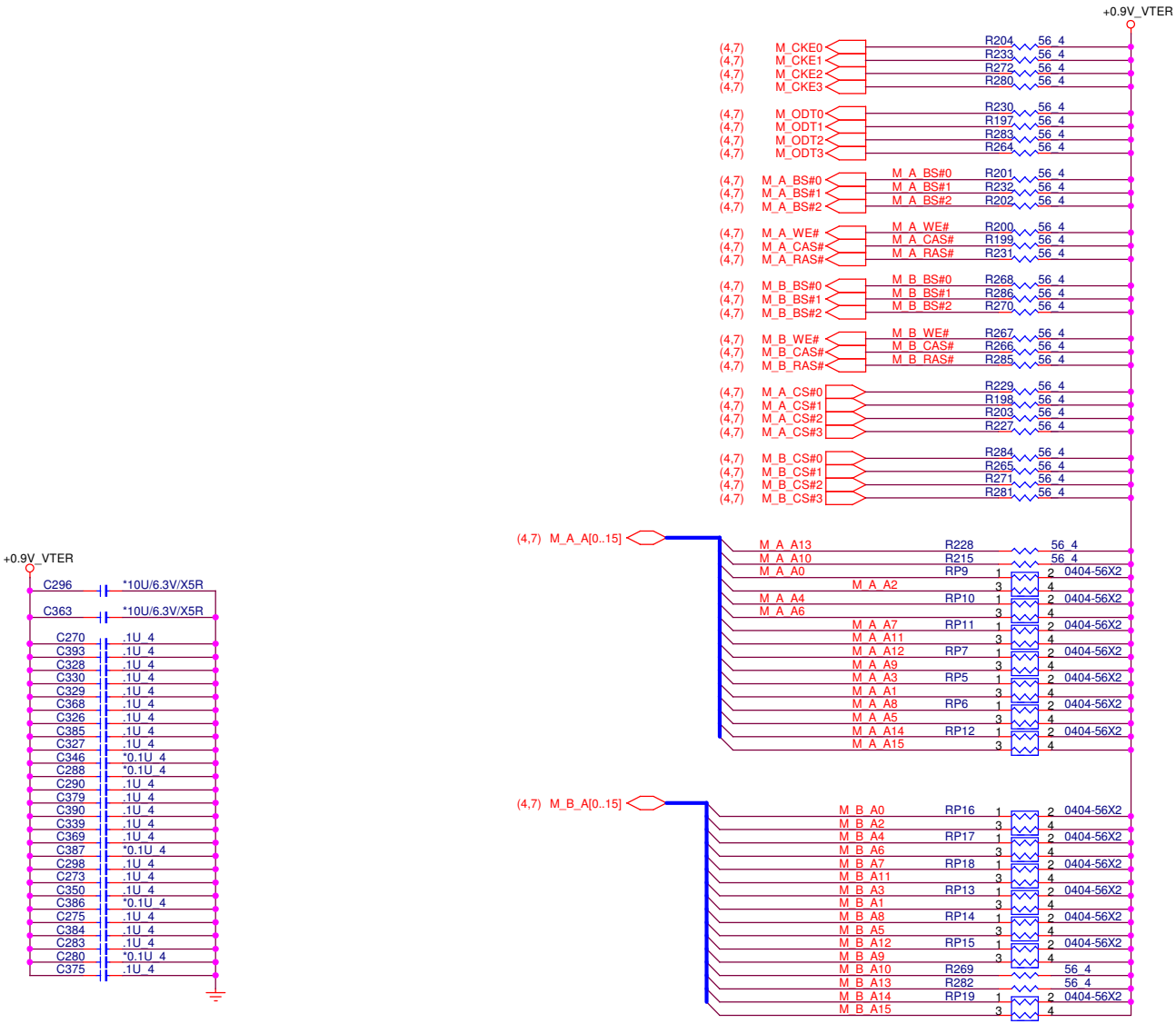

PROJECT : ED5

Quanta Computer Inc.

Size	Document Number	Rev
	DDR-II TERMINATION	1A
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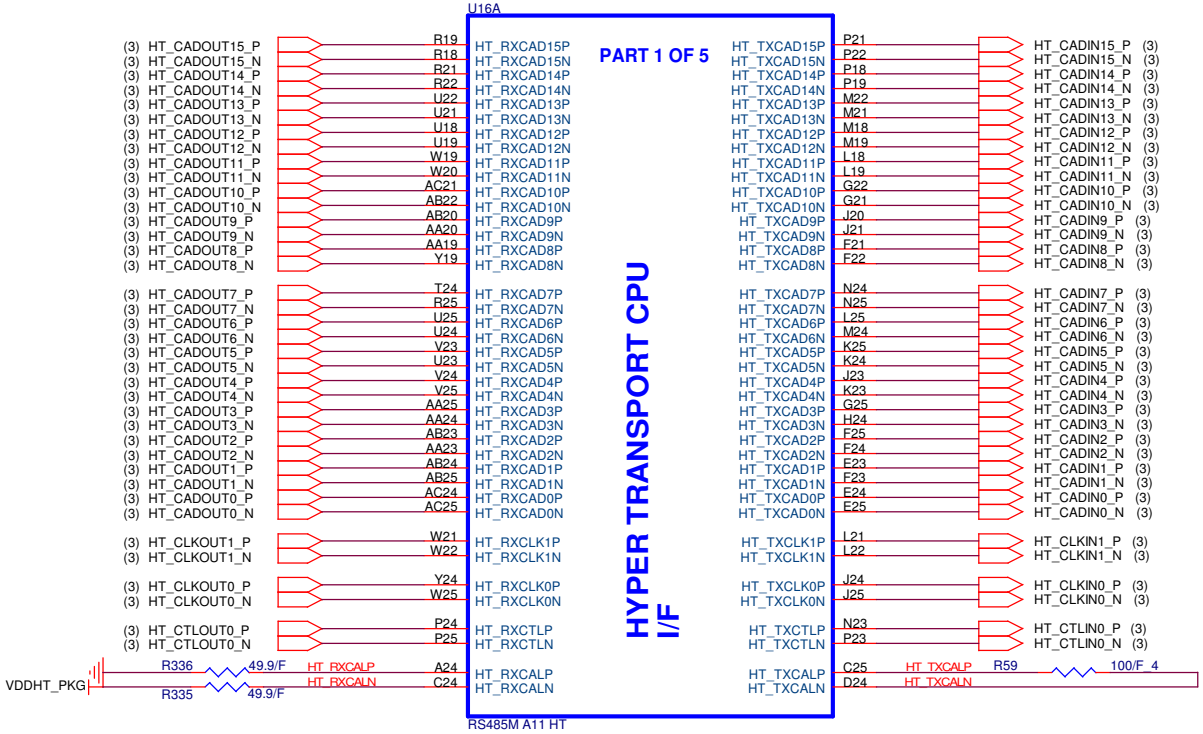
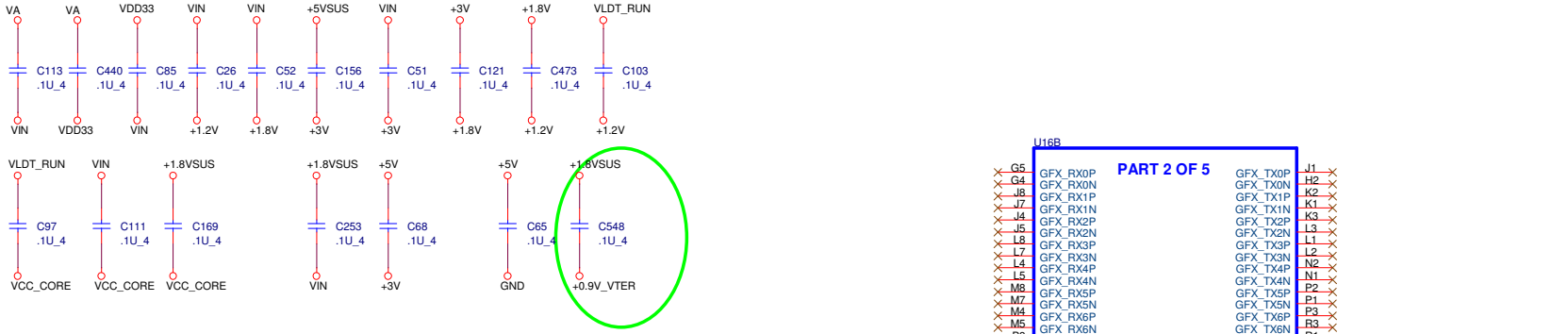
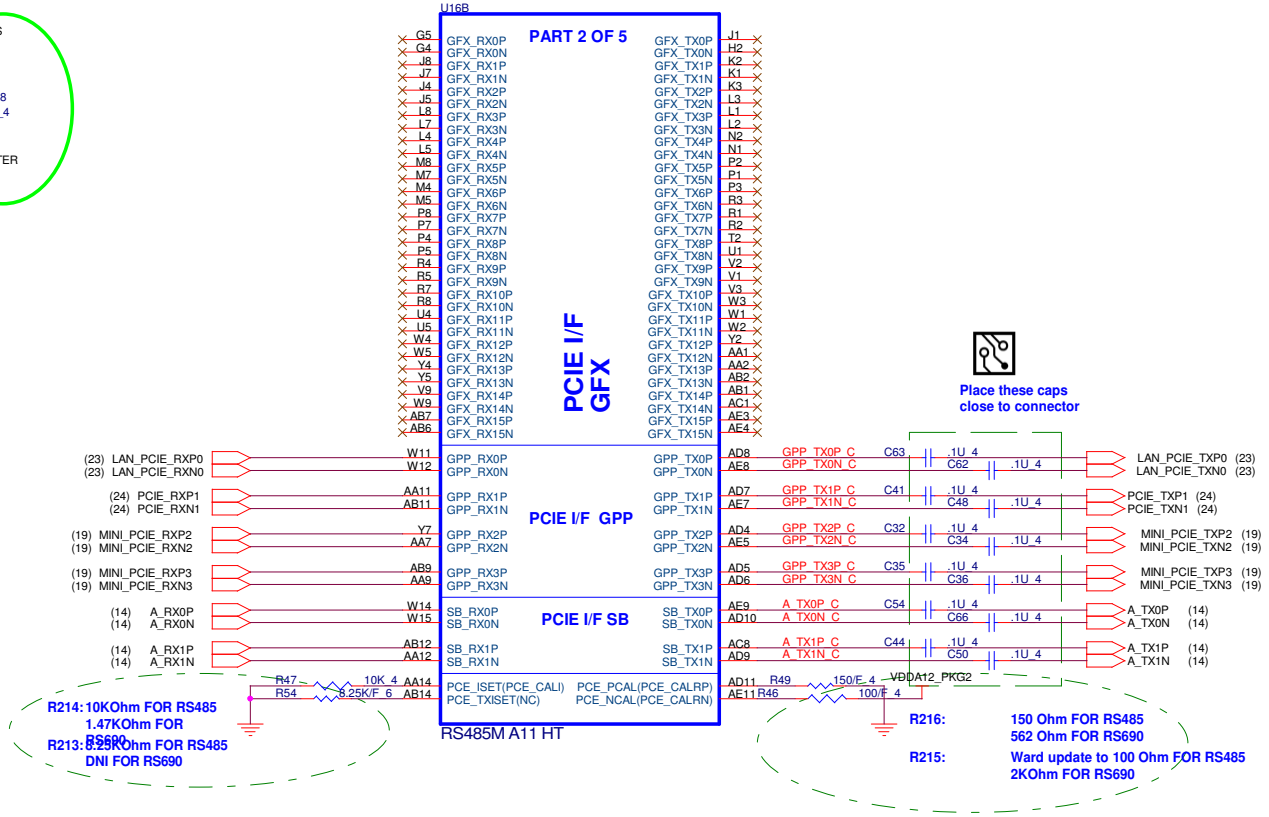


PROJECT : ED5

Quanta Computer Inc.

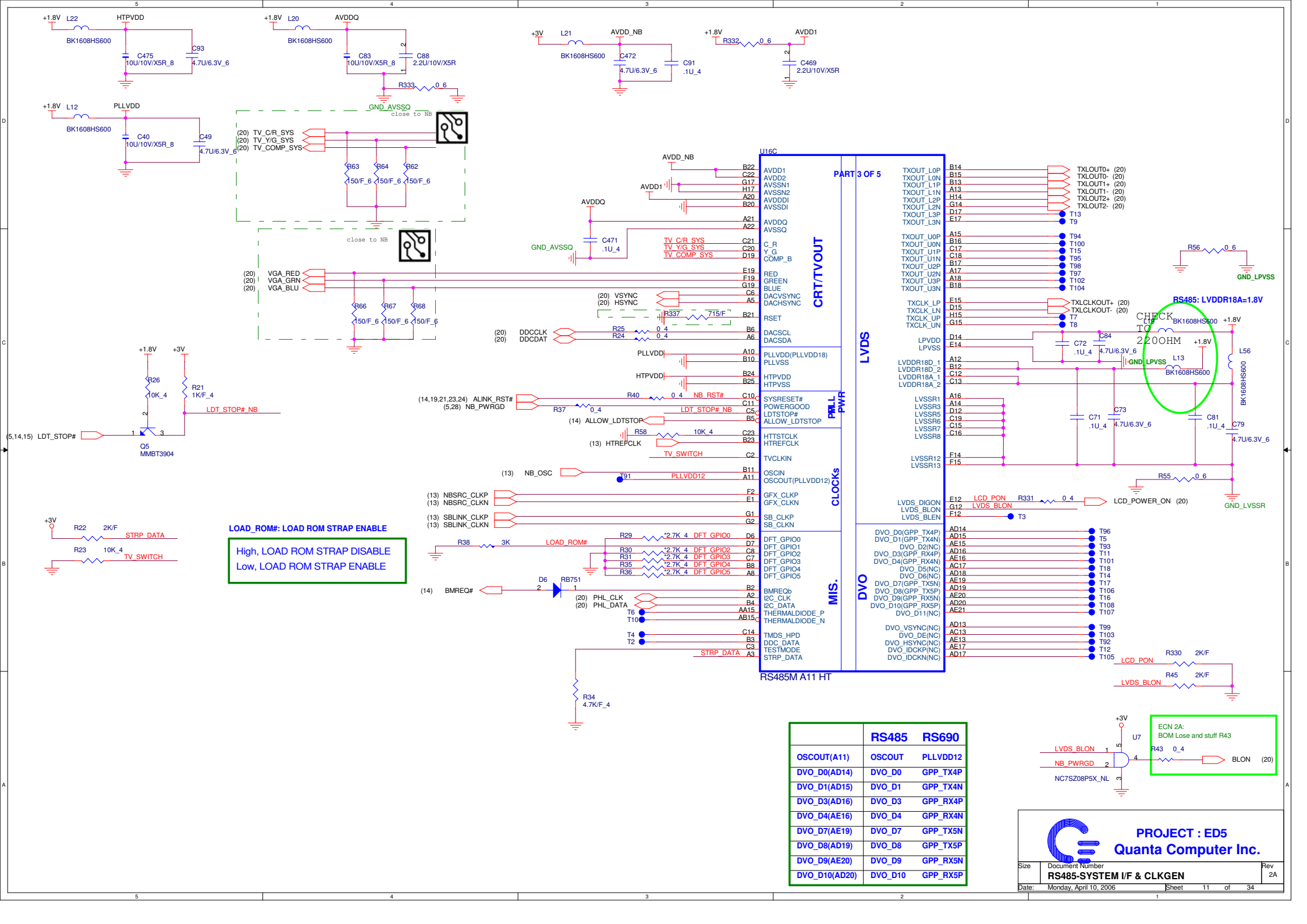
Size	Document Number	Rev
	RS485-HT LINK0 I/F	1A
Date: Monday, April 10, 2006	Sheet 9 of 34	





PROJECT : ED5
Quanta Computer Inc.

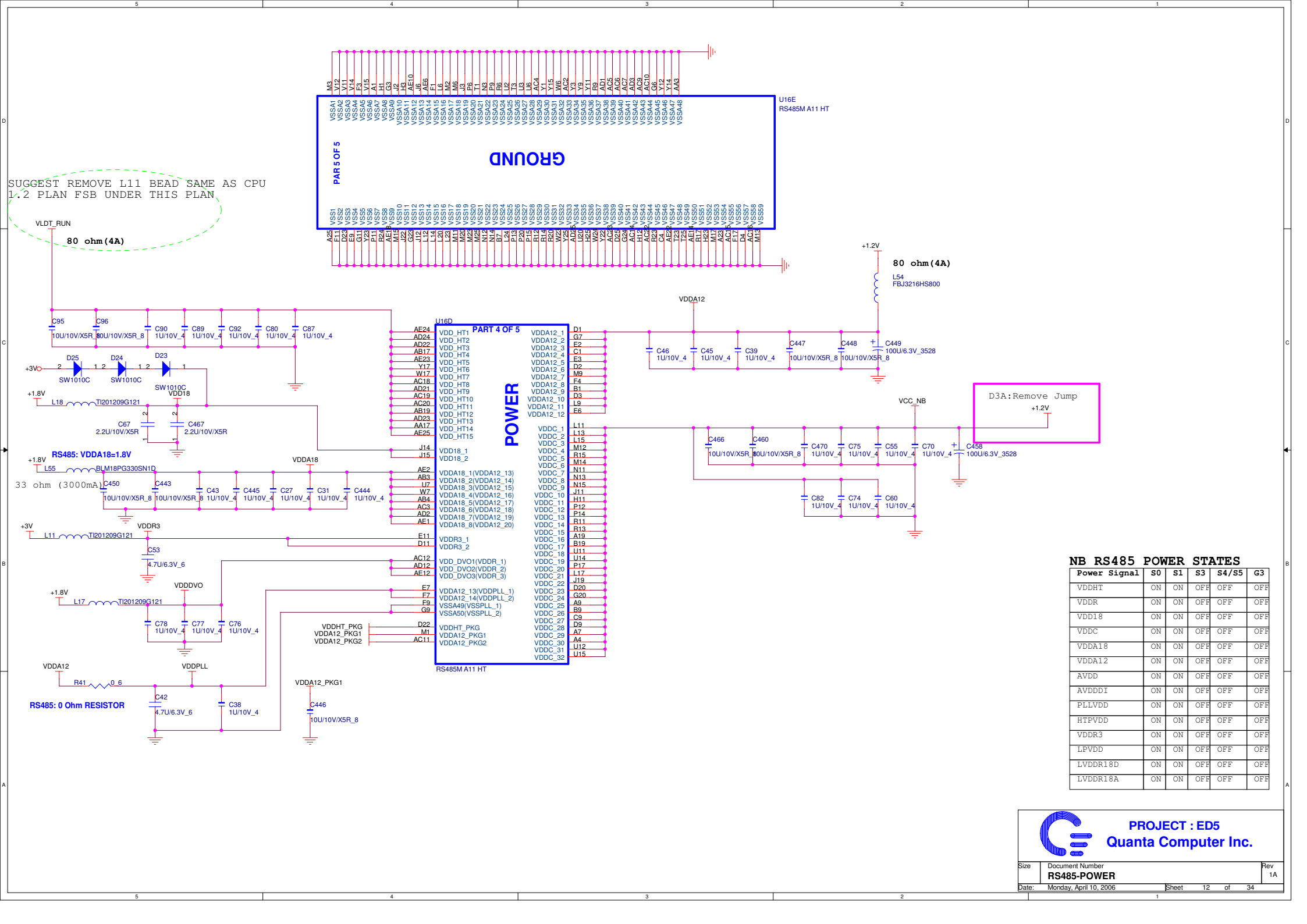
Size	Document Number	Rev
	RS485-PCIE LINK I/F	1A
Date: Monday, April 10, 2006	Sheet 10 of 34	



	RS485	RS690
OSCOUT(A11)	OSCOUT	PLLVDD12
DVO_D0(AD14)	DVO_D0	GPP_TX4P
DVO_D1(AD15)	DVO_D1	GPP_TX4N
DVO_D3(AD16)	DVO_D3	GPP_RX4P
DVO_D4(AE16)	DVO_D4	GPP_RX4N
DVO_D7(AE19)	DVO_D7	GPP_TX5N
DVO_D8(AD19)	DVO_D8	GPP_TX5P
DVO_D9(AE20)	DVO_D9	GPP_RX5N
DVO_D10(AD20)	DVO_D10	GPP_RX5P

PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
	RS485-SYSTEM I/F & CLKGEN	2A
Date: Monday, April 10, 2006	Sheet 11 of 34	


SUGGEST REMOVE L11 BEAD SAME AS CPU
1.2 PLAN FSB UNDER THIS PLAN
VLDT_RUN
80 ohm(4A)
U16E
RS485M A11 HT
PAR 5 OF 5
GROUND
U16D
PART 4 OF 5
POWER
RS485M A11 HT
80 ohm(4A)
L54
FBJ3216HS800
+1.2V
VDDA12
VCC_NB
D3A:Remove Jump
RS485: VDDA18=1.8V
33 ohm (3000mA)
RS485: 0 Ohm RESISTOR
SW1010C
TI201209G121
BLM18PG330SN1D
0_6
C95
C96
C90
C89
C92
C80
C87
C46
C45
C39
C447
C448
C449
100U/6.3V_3528
C466
C460
C470
C75
C55
C70
C458
C82
C74
C60
C67
C467
C450
C443
C43
C445
C27
C31
C444
C53
C78
C77
C76
R41
C42
C38
C446
VDDHT_PKG
VDDA12_PKG1
VDDA12_PKG2
NB RS485 POWER STATES
Power Signal | S0 | S1 | S3 | S4/S5 | G3
VDDHT | ON | ON | OFF | OFF | OFF
VDDR | ON | ON | OFF | OFF | OFF
VDD18 | ON | ON | OFF | OFF | OFF
VDDC | ON | ON | OFF | OFF | OFF
VDDA18 | ON | ON | OFF | OFF | OFF
VDDA12 | ON | ON | OFF | OFF | OFF
AVDD | ON | ON | OFF | OFF | OFF
AVDDDI | ON | ON | OFF | OFF | OFF
PLLVDD | ON | ON | OFF | OFF | OFF
HTPVDD | ON | ON | OFF | OFF | OFF
VDDR3 | ON | ON | OFF | OFF | OFF
LPVDD | ON | ON | OFF | OFF | OFF
LVDDR18D | ON | ON | OFF | OFF | OFF
LVDDR18A | ON | ON | OFF | OFF | OFF
PROJECT : ED5
Quanta Computer Inc.
Size
Document Number
RS485-POWER
Rev
1A
Date: Monday, April 10, 2006
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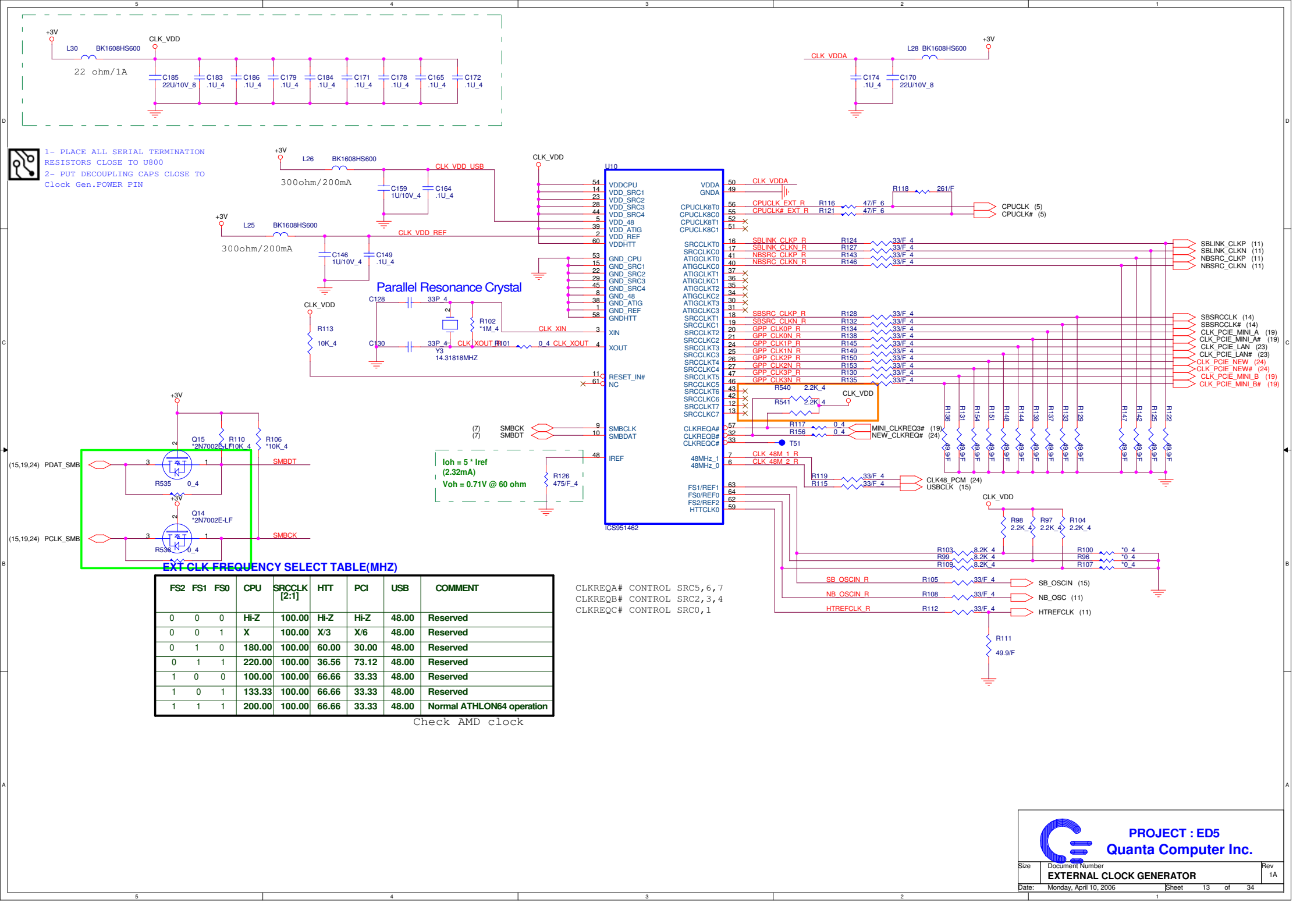

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

CLKREQA# CONTROL SRC5,6,7
CLKREQB# CONTROL SRC2,3,4
CLKREQC# CONTROL SRC0,1

Check AMD clock

PROJECT : ED5
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Size	Document Number	Rev
	EXTERNAL CLOCK GENERATOR	1A
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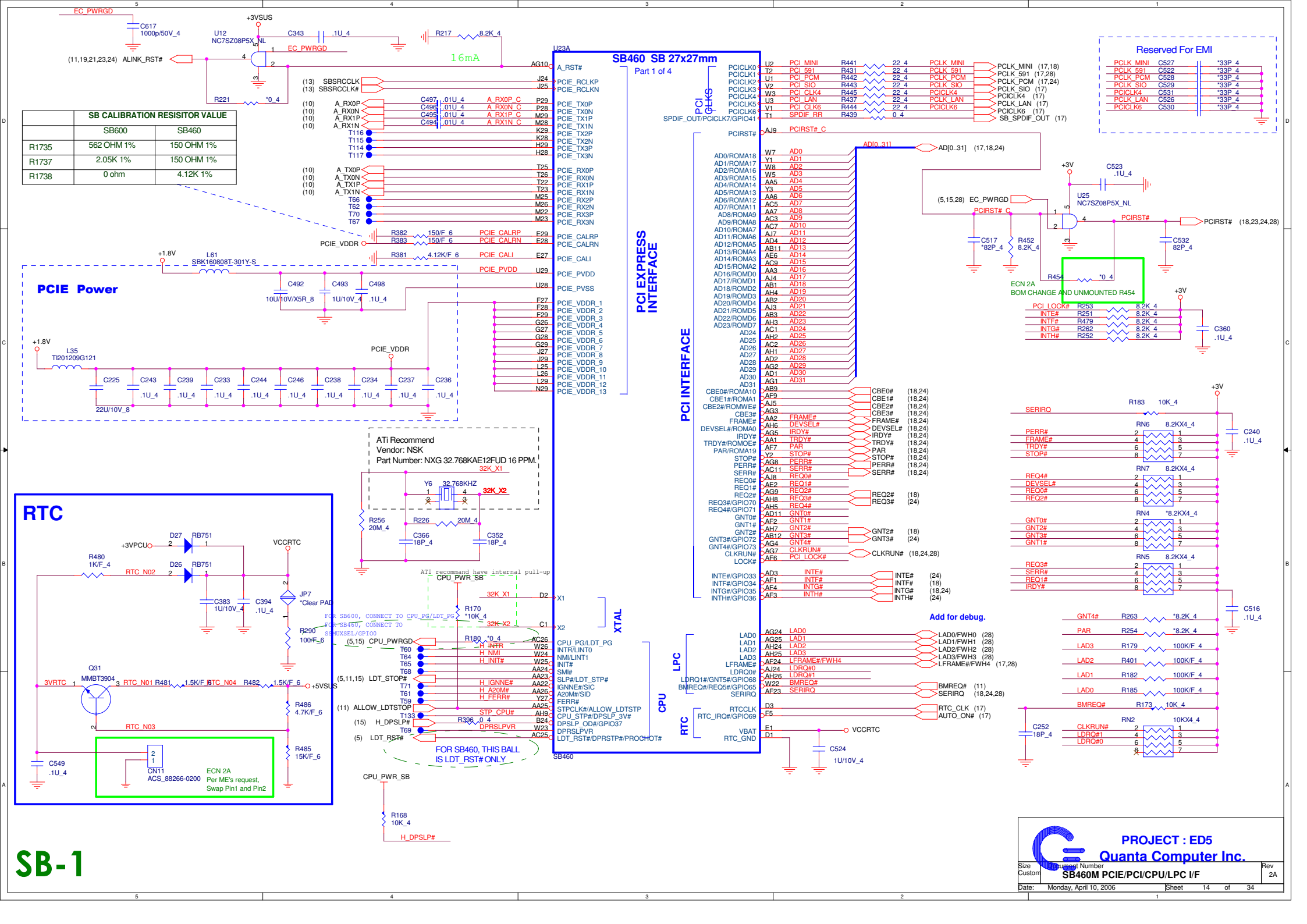
SB460 SB 27x27mm
Part 1 of 4
PCI EXPRESS INTERFACE
PCI INTERFACE
PCIE Power
RTC
XTAL
CPU
LPC
RTC
SB460
SB-1
SB CALIBRATION RESISITOR VALUE
SB600
SB460
R1735 562 OHM 1% 150 OHM 1%
R1737 2.05K 1% 150 OHM 1%
R1738 0 ohm 4.12K 1%
ATi Recommend
Vendor: NSK
Part Number: NXG 32.768KAE12FUD 16 PPM.
Reserved For EMI
ECN 2A
BOM CHANGE AND UNMOUNTED R454
ECN 2A
Per ME's request,
Swap Pin1 and Pin2
Add for debug.
FOR SB460, THIS BALL
IS LDT_RST# ONLY
PROJECT : ED5
Quanta Computer Inc.
SB460M PCIE/PCI/CPU/LPC I/F
Monday, April 10, 2006
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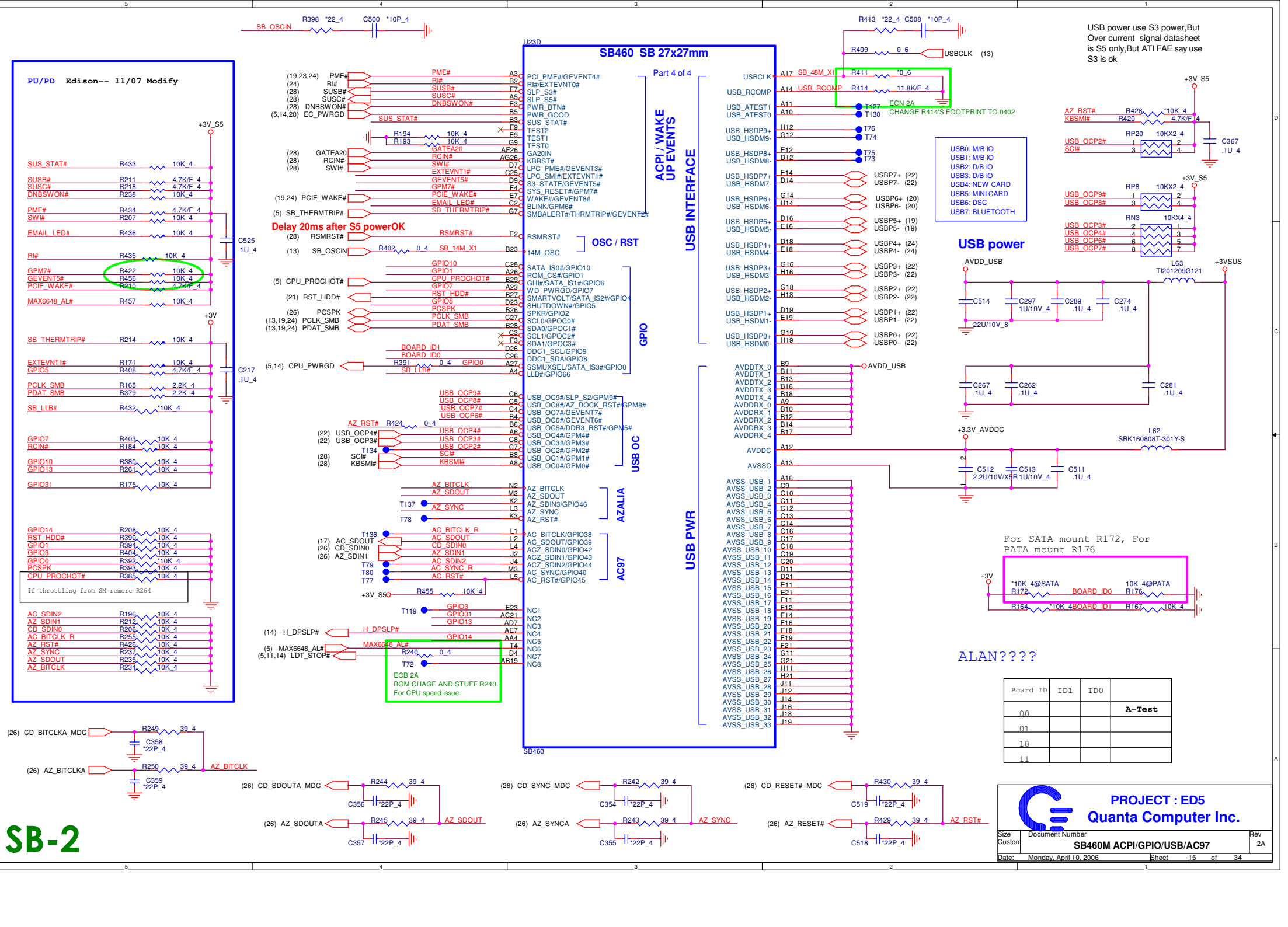
PU/PD Edison-- 11/07 Modify
SB460 SB 27x27mm
Part 4 of 4
USB INTERFACE
ACPI / WAKE UP EVENTS
GPIO
OSC / RST
USB OC
AZALIA
AC97
USB PWR
Delay 20ms after S5 powerOK
If throttling from SM remore R264
ECB 2A
BOM CHAGE AND STUFF R240.
For CPU speed issue.
USB power use S3 power,But Over current signal datasheet is S5 only,But ATI FAE say use S3 is ok
USB0: M/B IO
USB1: M/B IO
USB2: D/B IO
USB3: D/B IO
USB4: NEW CARD
USB5: MINI CARD
USB6: DSC
USB7: BLUETOOTH
USB power
ECN 2A
CHANGE R414'S FOOTPRINT TO 0402
For SATA mount R172, For PATA mount R176
ALAN????
Board ID | ID1 | ID0
00
01
10
11
A-Test
SB-2
PROJECT : ED5
Quanta Computer Inc.
SB460M ACPI/GPIO/USB/AC97
Rev 2A
Monday, April 10, 2006
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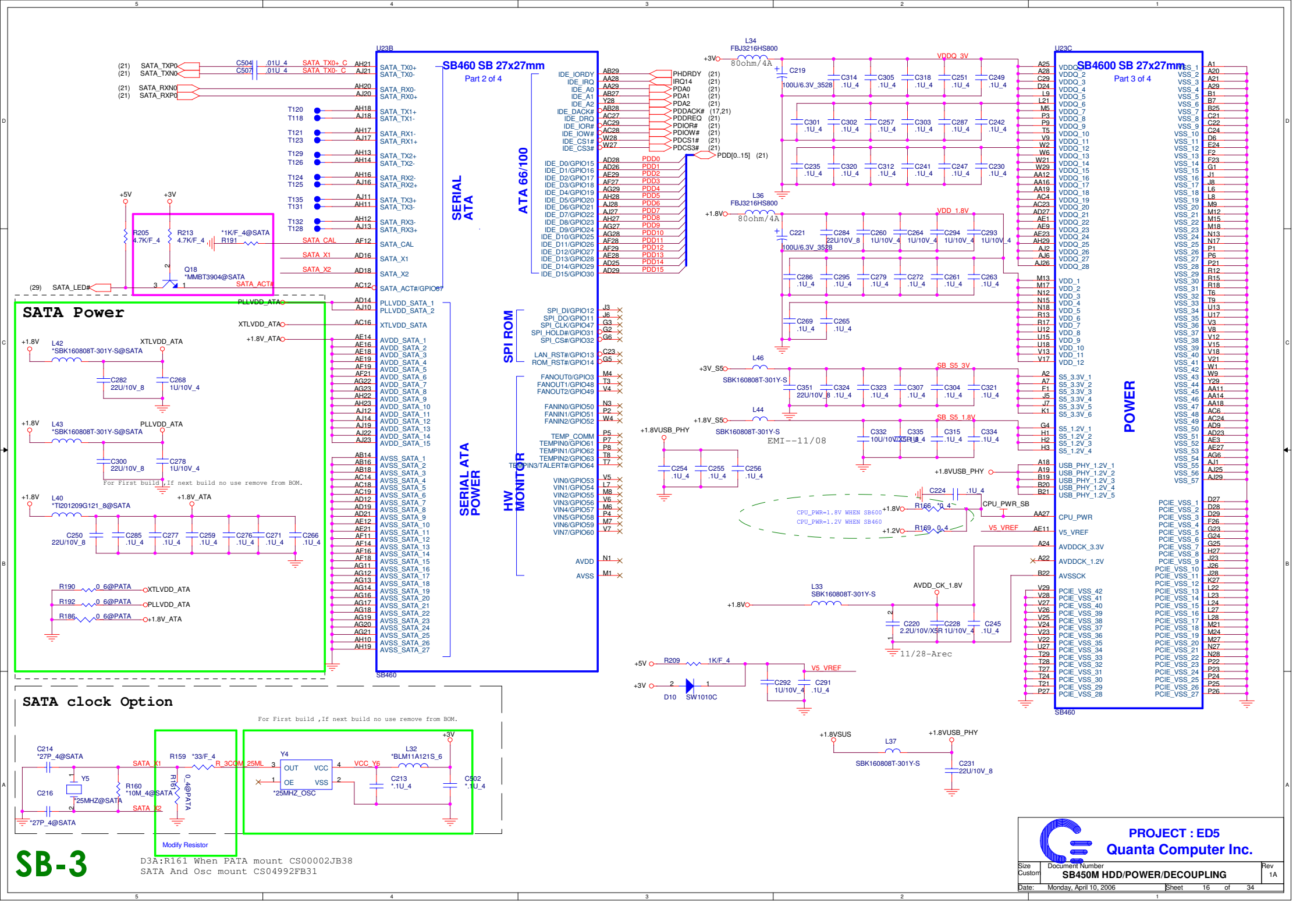
SB460 SB 27x27mm
Part 2 of 4
SERIAL ATA
ATA 66/100
SPI ROM
SERIAL ATA POWER
HW MONITOR
SATA Power
SATA clock Option
For First build ,If next build no use remove from BOM.
Modify Resistor
SB4600 SB 27x27mm
Part 3 of 4
POWER
SB460
EMI--11/08
11/28-Arec
CPU_PWR=1.8V WHEN SB600
CPU_PWR=1.2V WHEN SB460
SB-3
D3A:R161 When PATA mount CS00002JB38
SATA And Osc mount CS04992FB31
PROJECT : ED5
Quanta Computer Inc.
SB450M HDD/POWER/DECOUPLING
Monday, April 10, 2006
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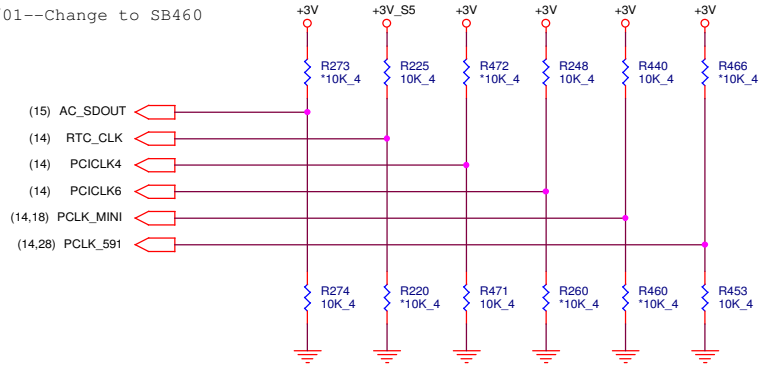
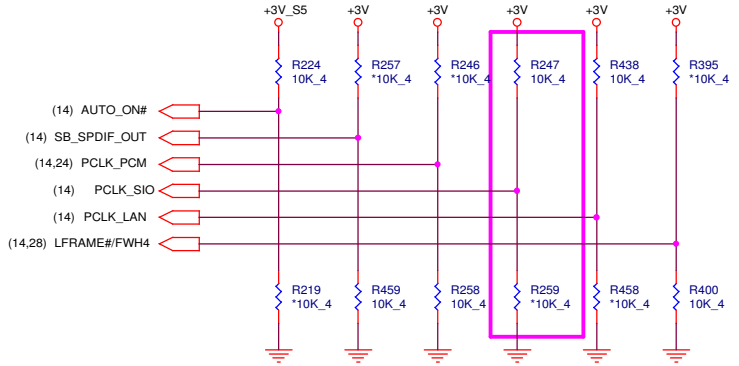
Edison-11/01--Change to SB460



D3A:BOM change. R247: Stuff, R259: Un-stuff. Disable USB PHY POWERDOWN.

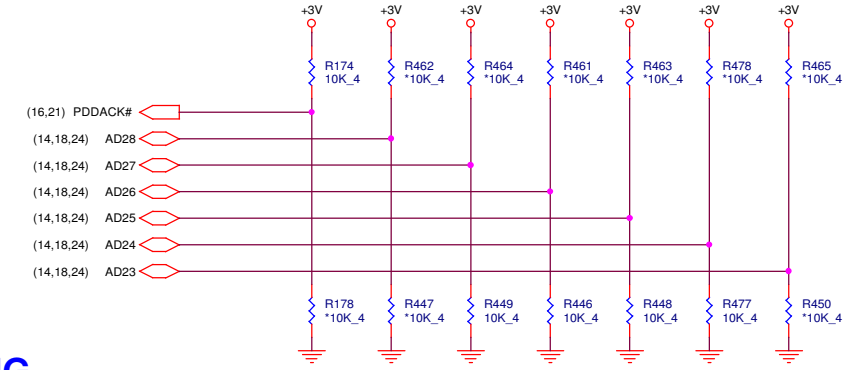


REQUIRED STRAPS

	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCLK_MINI PCLK_591
					PCI_CLK0 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM H, L = LPC TYPE I ROM L, H = LPC TYPE II ROM DEFAULT L, L = FWH ROM
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4 DEFAULT	NOTE:FOR SB460,PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]

	AUTO_ON#	SB_SPDIF_OUT	PCLK_PCM	PCLK_SIO	PCLK_LAN	LFRAME#
	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

BIOS ENABLE AFTER STARTUP



DEBUG STRAPS

	PDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET		USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

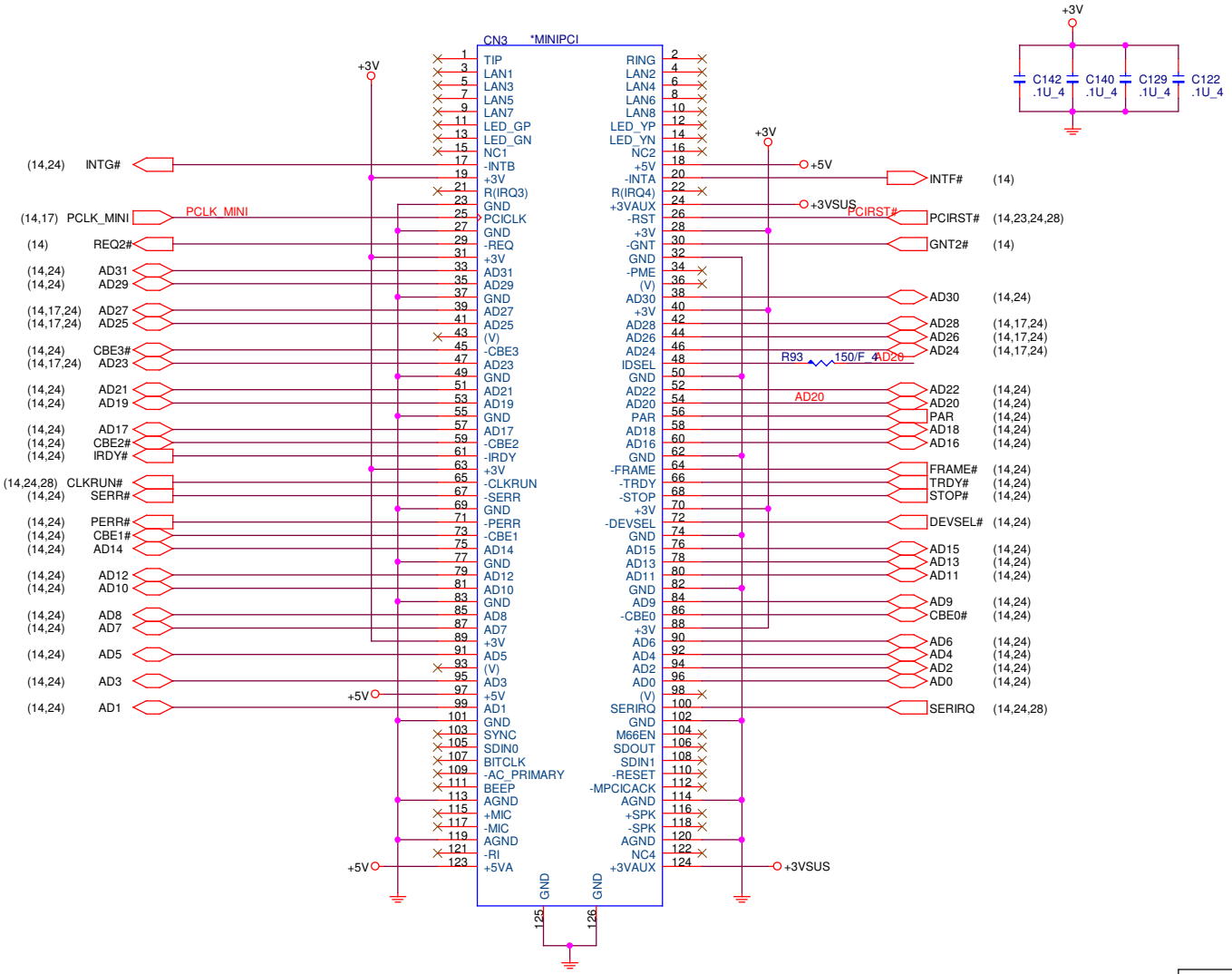
SB-4

PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB460M STRAPS	1A
Date: Monday, April 10, 2006	Sheet 17 of 34	

ID Select : AD20
Interrupt Pin : INTG# , INTF#
Request Indicate : REQ2#
Grant Indicate : GNT2#

DEBUG PURPOSE ONLY



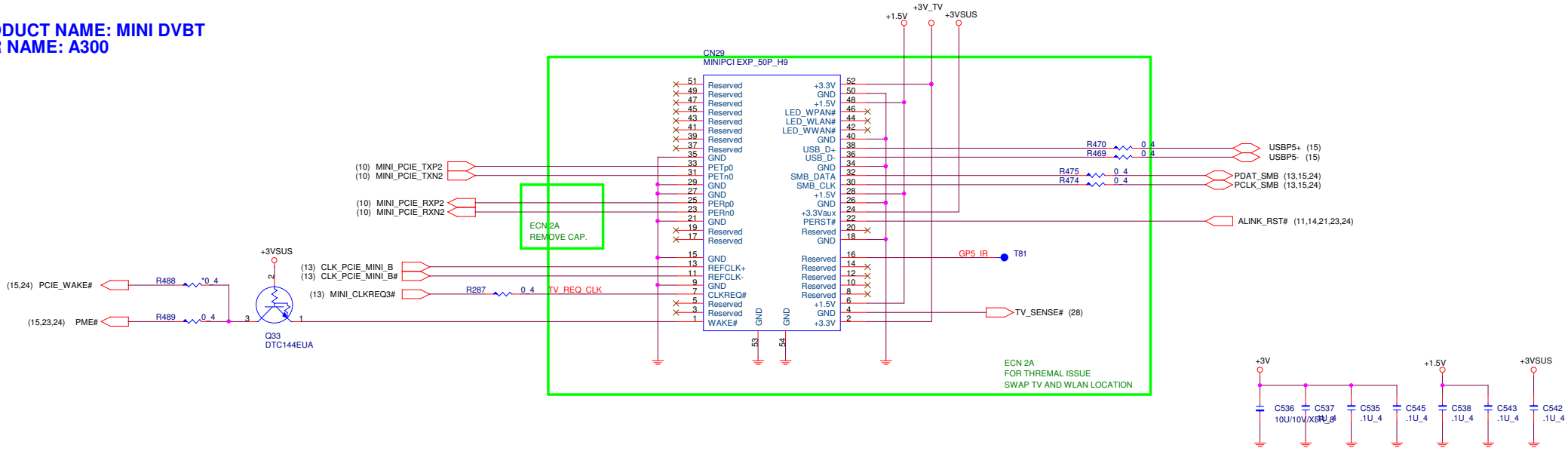
MPC

PROJECT : ED5
Quanta Computer Inc.

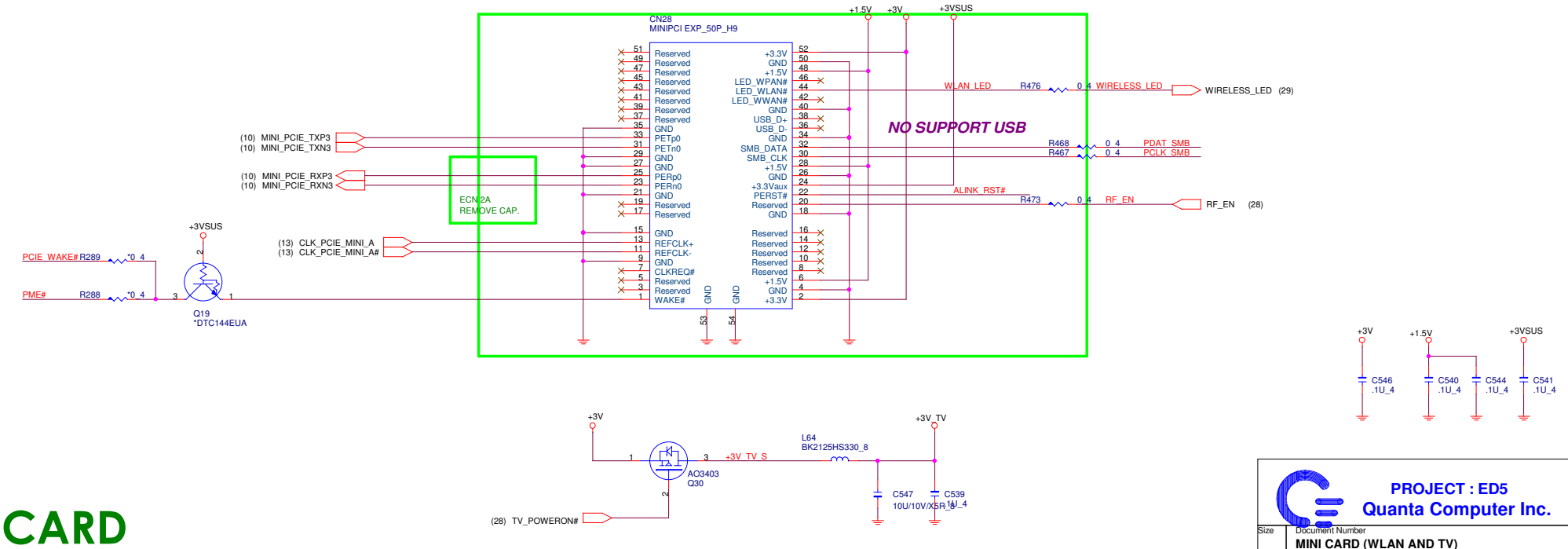
Size	Document Number	Rev
	MINI PCI CONNECTOR (DEBUG ONLY)	1A
Date: Monday, April 10, 2006	Sheet 18 of 34	

TV MINI CARD

PRODUCT NAME: MINI DVBT
MFR NAME: A300



WLAN MINI CARD

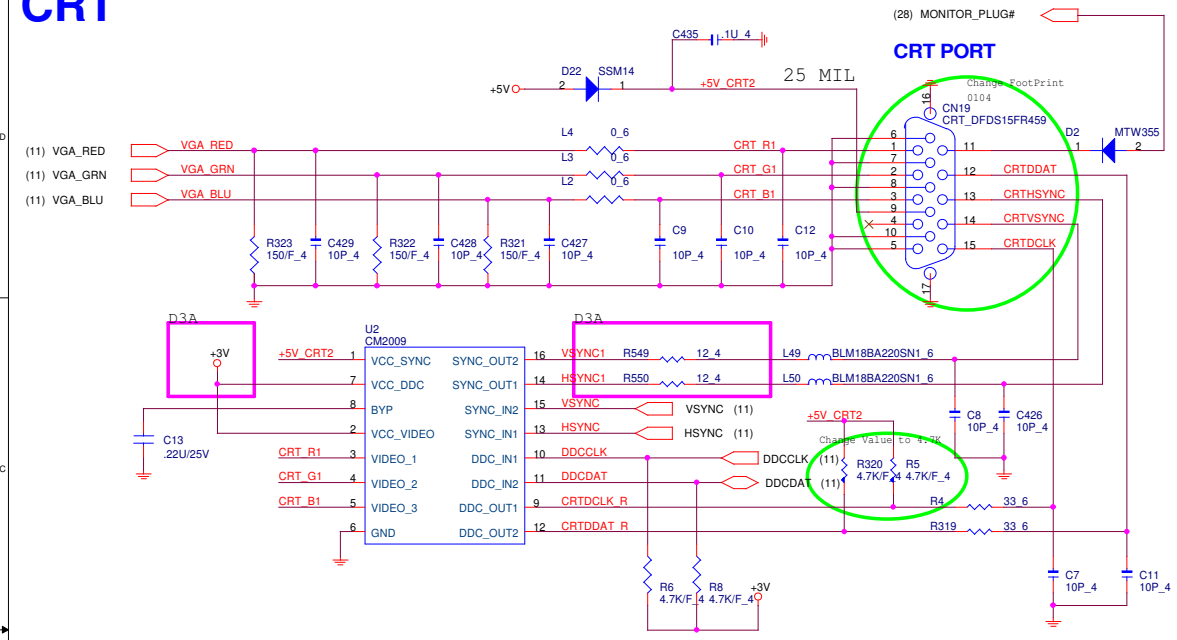


MINI CARD

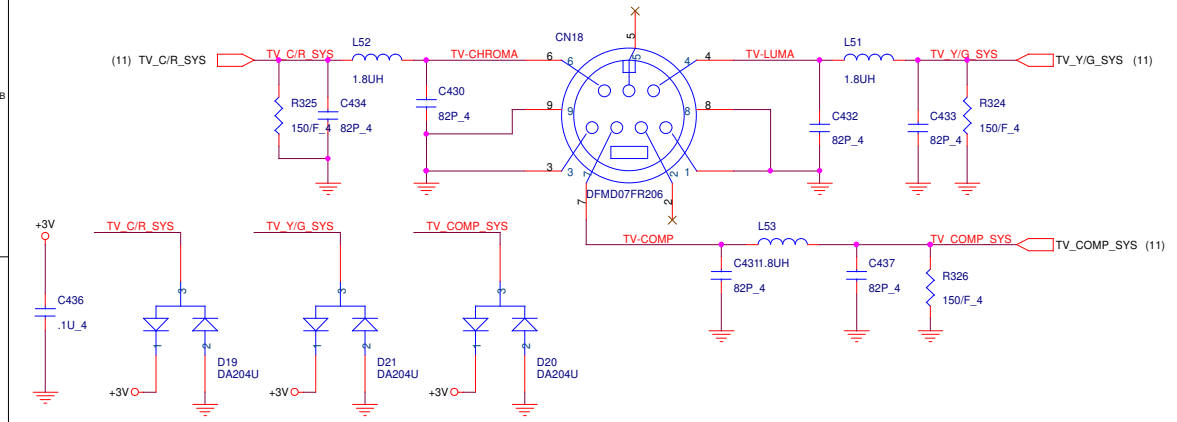
PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
	MINI CARD (WLAN AND TV)	2A
Date: Monday, April 10, 2006	Sheet 19 of 34	

CRT

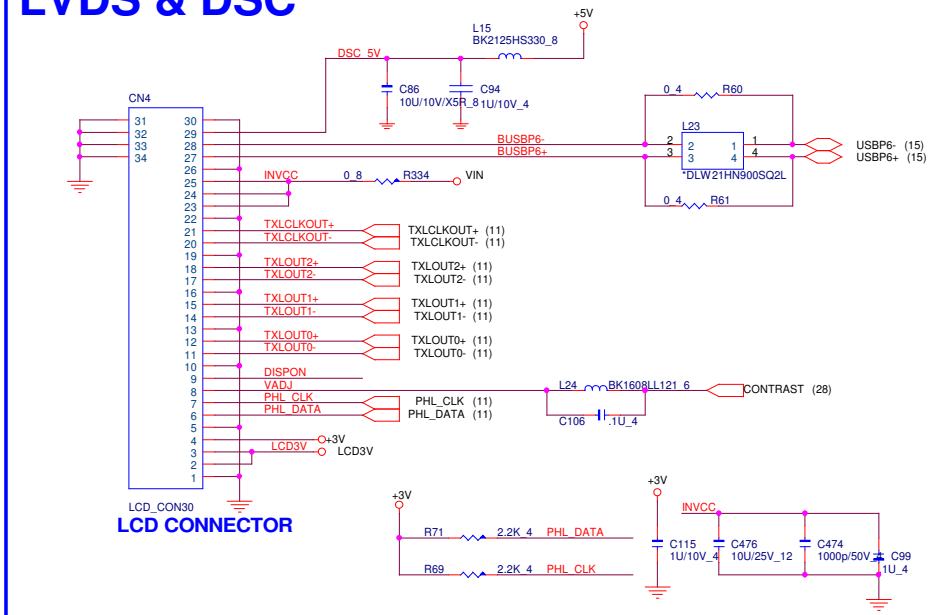


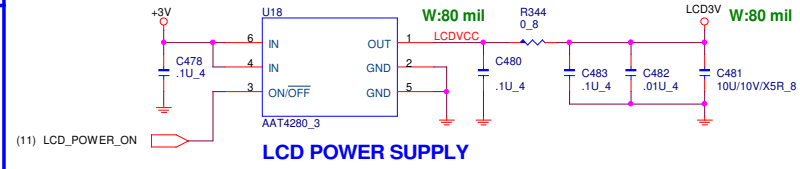
TV

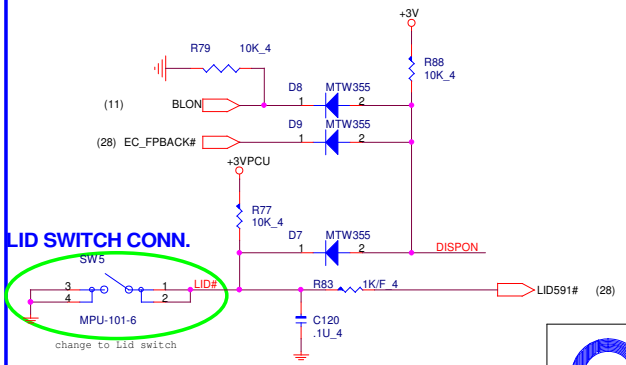


CRT, LVDS, TV, DSC

LVDS & DSC







PROJECT : ED5		
Quanta Computer Inc.		
Size	Document Number	Rev
	VGA Ports, LID, S-VIDEO, DSC	1A
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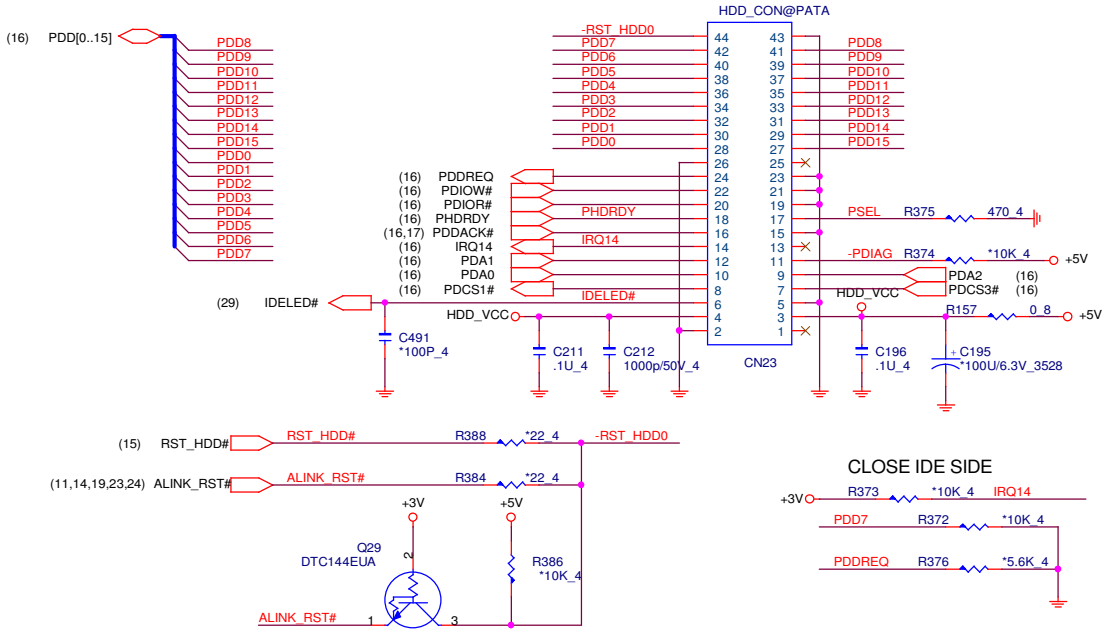
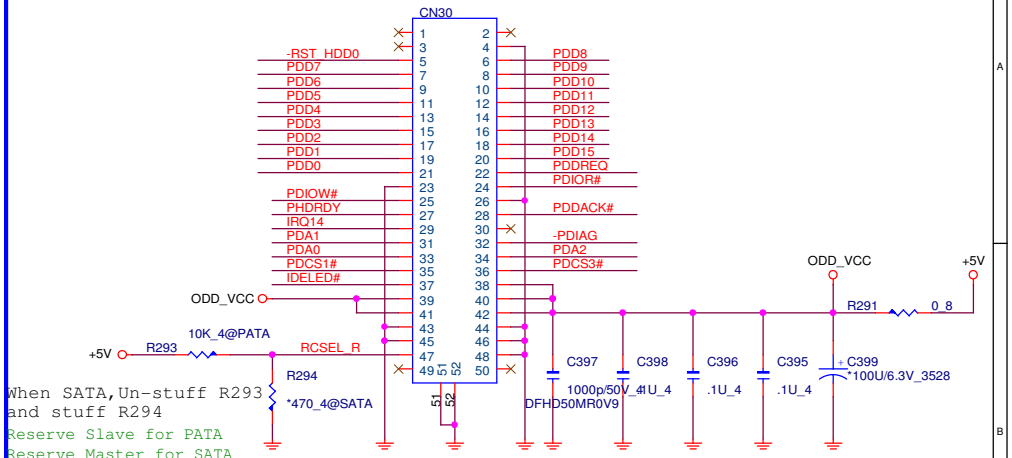
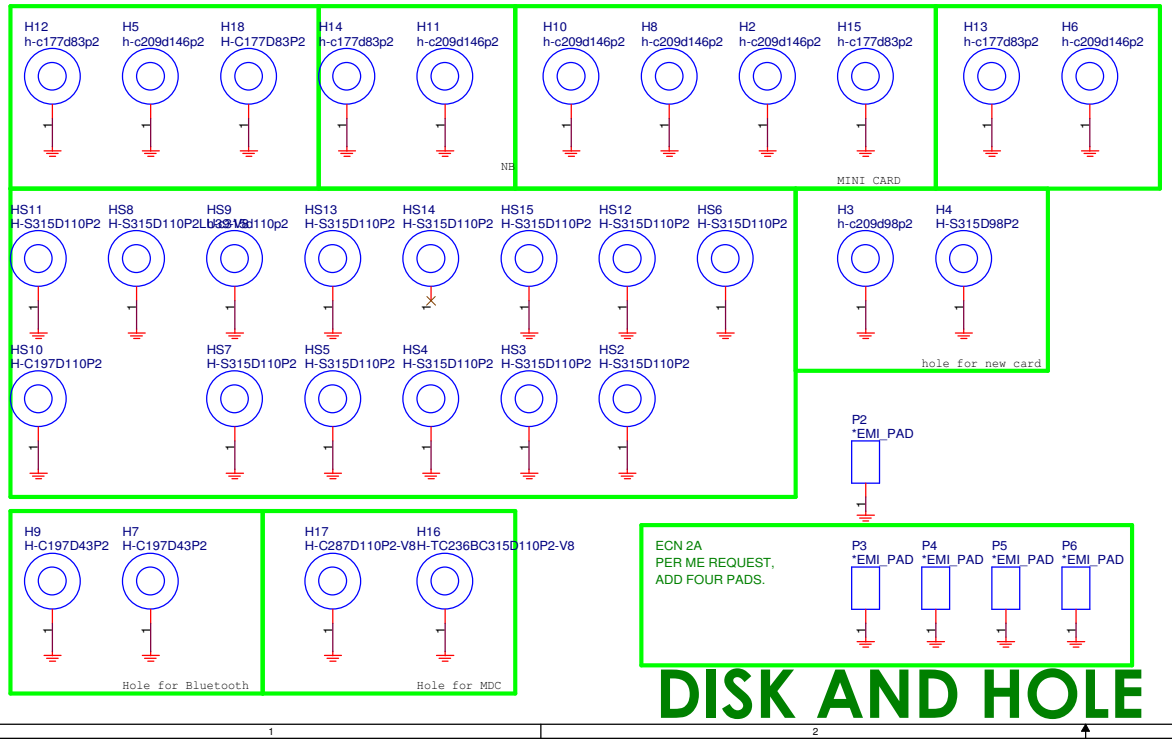
PATA HDD



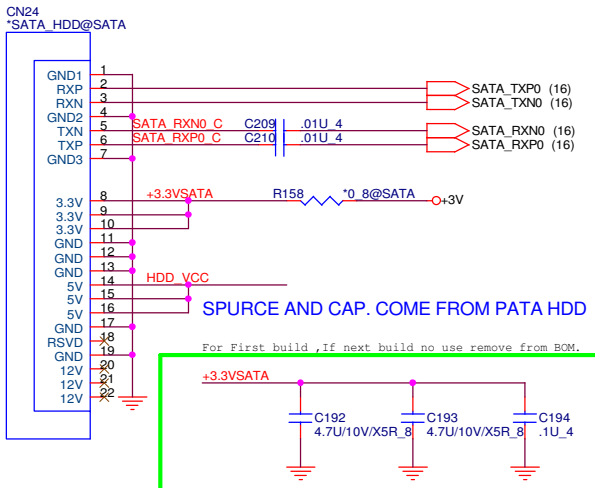
PATA ODD

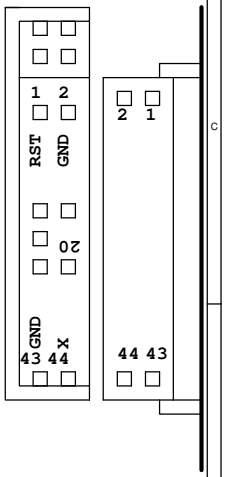




DISK AND HOLE

SATA HDD





PROJECT : ED5

Quanta Computer Inc.

Size	Document Number	Rev
	HDD & CDROM , HOLES	2A
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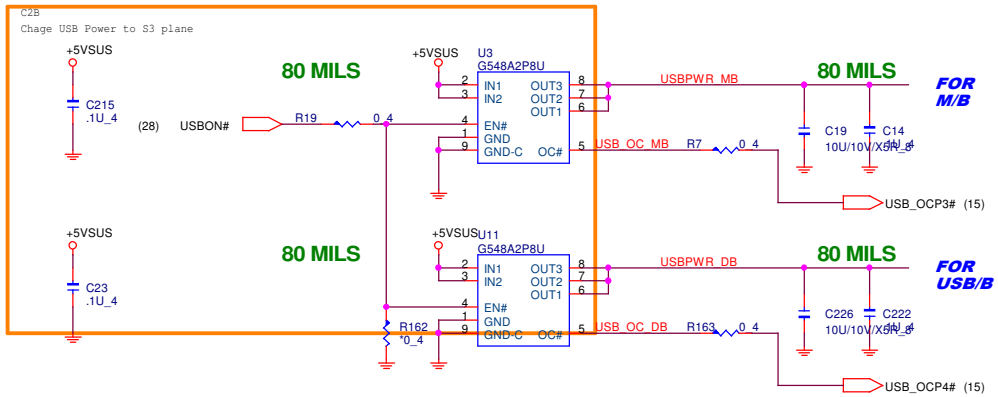
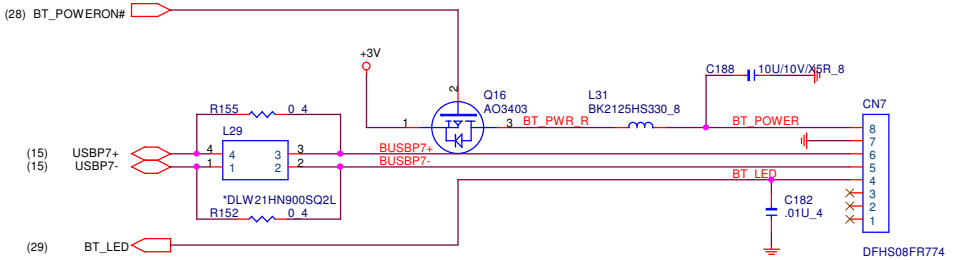
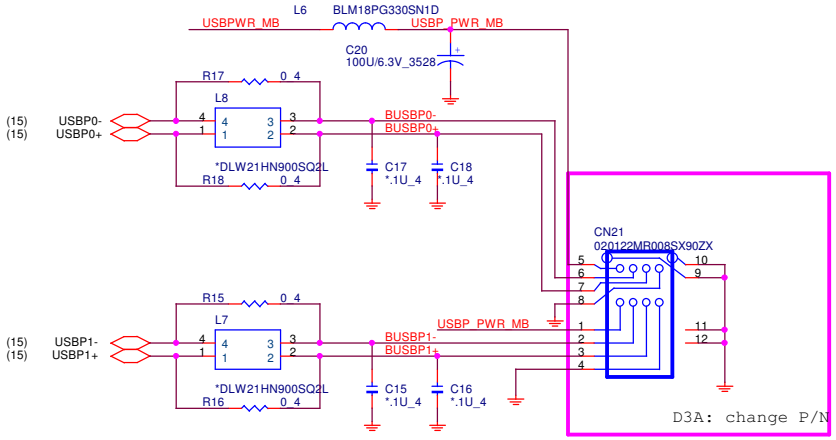
USB POWER SUPPLY



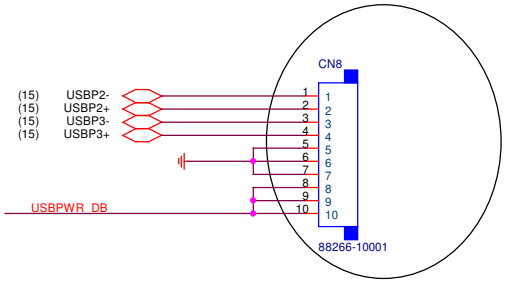
BLUETOOTH



USB I/O CONNECTORS



USB BAORD WIRE CONNECTOR



USB, BT, USB/B COONECTOR

PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
	MINI PCI & USB PORT & BT	1A
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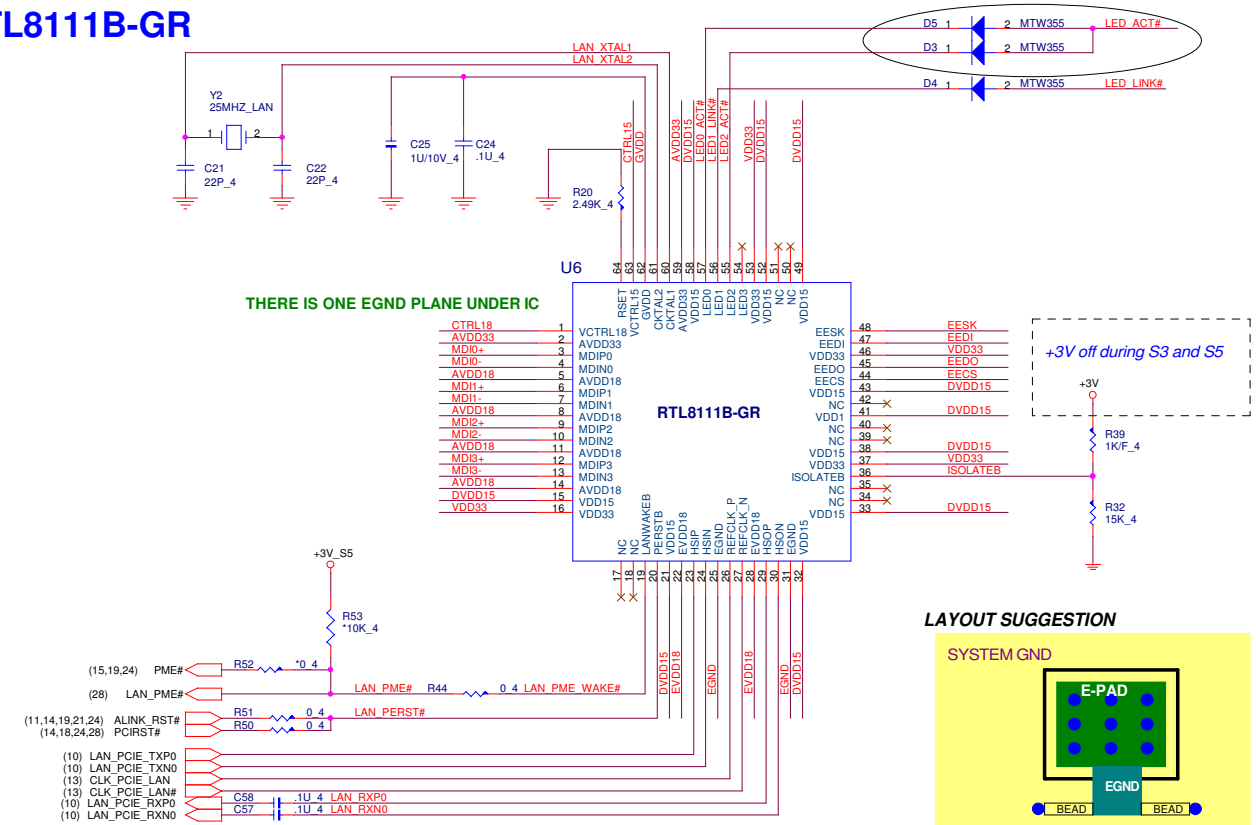
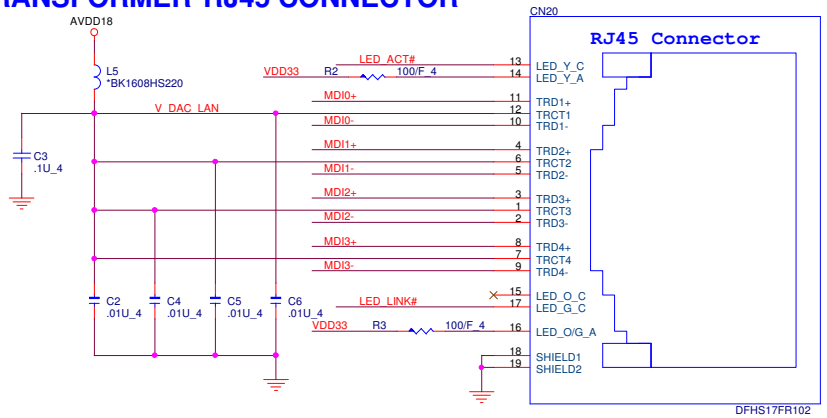
RTL8111B-GR

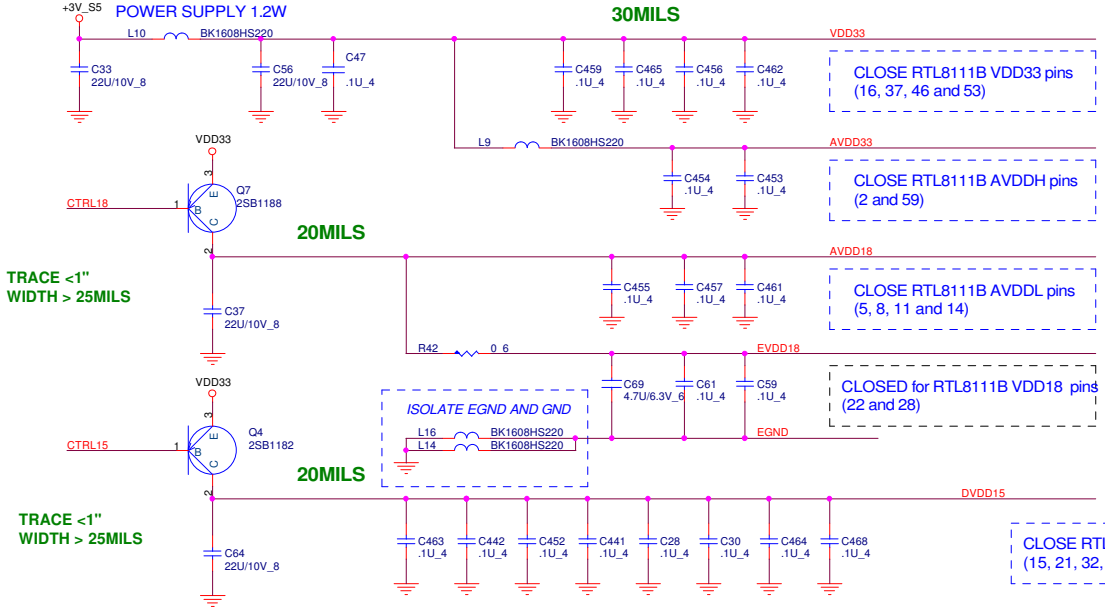


LAYOUT SUGGESTION

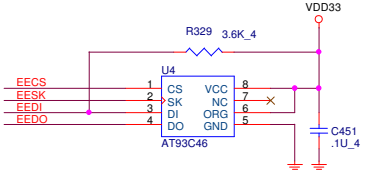
TRANSFORMER RJ45 CONNECTOR



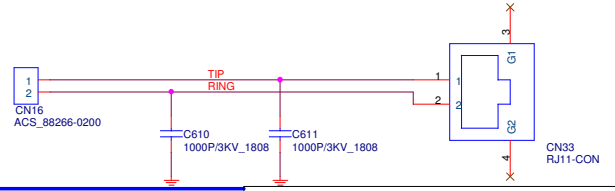
POWER SUPPLY



EEPROM



RJ11



LAN

PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
	LAN RTL8111B-GR PCI-E & RJ11	1A

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PCI8402 PCI I/F

ID Select : AD17
Interrupt Pin : INTE# , INTG#, INTH#
Request Indicate : REQ3#
Grant Indicate : GNT3#

AD17 R405 150/F_4 PCM_IDSEL

ECN 2A
BOM CHANGE
REMOVE Y7 AND C509
STUFF R407

R407 0_4 CLK48_PCM (13)

Y7 *48MHz C509 *.1U_4 +3V

(14,17,18) AD[0..31] AD[0..31]

U24A PCIXX12_0

CLK48 E1 CLK48M
GRST K5 GRST#_8412
SUSPEND J5 8402_SUS# R415 10K_4 +3V

MFUNC0 G1 INTE# R416 0_4 INTE# (14)
MFUNC1 H5 INTH# INTG# (14,18)
MFUNC2 H2 SERIRQ INTH# (14)
MFUNC3 H1 3VSP R406 4.7K/F_4 SERIRQ (14,18,28)
MFUNC4 J1 FM_LED +3V
MFUNC5 J2 CLKRUN# FM_LED (25)
MFUNC6 J3 CLKRUN# (14,18,28)

PCLK L1 PCLK_PCM PCLK_PCM (14,17)
PRST K3 PCIRST# PCIRST# (14,18,23,28)
SPKROUT H3 PCMSPK PCMSPK (26)
RI_OUT/PME L5 PCM_PME# R189 *0_4 RI# (15)

SDA G3 SDA_CARD
SCL G2 SCL_CARD

LATCH C9
DATA B9
CLOCK A9

USB_EN E10 USB_EN# R427 *10K_4 +3V

PHY_TEST_MA P17 TEST_MA R216 4.7K/F_4 1394_AVDD
TEST0 P12
RSVD // VD0 // VCCD1# C4 PSMODE R417 10K_4 +3V
TRDY NC E5

Q17 DTC144EUA +3V
R188 0_4
PME# (15,19,23)

CBE0# (14,18) W10 C/BE0
CBE1# (14,18) V7 C/BE1
CBE2# (14,18) U5 C/BE2
CBE3# (14,18) P2 C/BE3

PAR (14,18) U7 PAR
DEVSEL# (14,18) U6 DEVSEL
FRAME# (14,18) R6 FRAME
GNT3# (14) L2 GNT
PCM_IDSEL N5 IDSEL
IRDY# (14,18) V5 IRDY
PERR# (14,18) R7 PERR
REQ3# (14) L3 REQ
SERR# (14,18) W6 SERR
STOP# (14,18) V6 STOP
TRDY# (14,18) W5 TRDY

AD0 R11 AD1 P11 AD2 U11 AD3 V11 AD4 W11 AD5 R10 AD6 U10 AD7 V10 AD8 R9 AD9 U9 AD10 V9 AD11 W9 AD12 V8 AD13 U8 AD14 R8 AD15 W7 AD16 W4 AD17 T2 AD18 T1 AD19 R3 AD20 P5 AD21 R2 AD22 R1 AD23 P3 AD24 N3 AD25 N2 AD26 N1 AD27 M5 AD28 M6 AD29 M3 AD30 M2 AD31 M1

PCLK_PCM R397 *22_4 PCLK_PCM_R C499 *10p_4
CLK48_PCM R399 *22_4 CLK48_PCM_R C501 *10p_4

U24B PCIXX12_0

VCCB A15 VCCB U19
CAD31 // D10 C10 CAD30 // D9 A10 CAD29 // D1 C11 CAD28 // D8 E11 CAD27 // D0 C11 CAD26 // A0 B13 CAD25 // A1 C13 CAD24 // A2 A14 CAD23 // A3 B14 CAD22 // A4 B15 CAD21 // A5 E14 CAD20 // A6 A16 CAD19 // A25 D19 CAD18 // A7 C17 CAD17 // A24 E15 CAD16 // A17 H19 CAD15 // IOWR# H17 CAD14 // A9 J15 CAD13 // IORD# J18 CAD12 // A11 K15 CAD11 // OE# K17 CAD10 // CE2# K18 CAD9 // A10 L15 CAD8 // D15 L18 CAD7 // D7 L19 CAD6 // D13 M17 CAD5 // D6 M18 CAD4 // D12 N19 CAD3 // D5 M15 CAD2 // D11 N17 CAD1 // D4 N18 CAD0 // D3 R19
CC/BE3# // REG# E13 CC/BE2# // A12 E18 CC/BE1# // A8 H18 CC/BE0# // CE1# L17
CPAR // A13 H14 CDEVSEL# // A21 K19 CFRAME# // A23 E19 CGNT# // WE# G17 CINT# // READY(IREQ#) E12 CIRDY# // A15 E17 CPERR# // A14 G19 CREQ# // INPACK# C14 CSERR# // WAIT# C12 CSTOP# // A20 G18 CTRDY# // A22 G15
CCLK // A16 E18 CCLKRUN# // WP(IOIS16#) A11 CSTSCHG // BVD1(STSCHG#/RI#) A12 CBLOCK# // A19 H15 CRST# // RESET C15 CAUDIO // BVD2(SPKR#) B12
CCD1# // CD1# N15 CCD2# // CD2# B11 CVS1 // VS1# A13 CVS2 // VS2# B16
RSVD // A18 H17 RSVD // D2 B10 RSVD // D14 M19

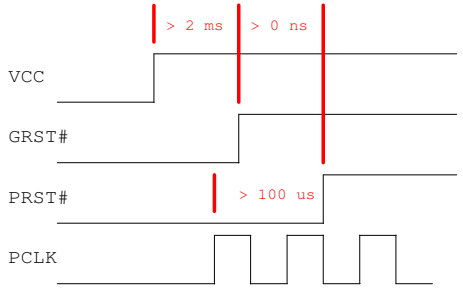
PCMCIA PORT

IEEE1394 EEPROM

+3V R389 2.2K_4 R387 2.2K_4 SDA_CARD SCL_CARD

U22 24LC08
SDA 5 SCL 6 WP 7 GND 4 VCC 8 A0 1 A1 2 A2 3
+3V C506 .1U_4

+3V R181 22K/F_4 GRST#_8412 C232 .22U/6V_4



IEEE1394 & NEW CARD

NEW CARD

NEW CARD HEADER: DFHD26MR074 (13081-1)
NEW CARD EJECTER: FBZF1026019 (130851-3)

CN6 FOXCONN_NEW_CARD

(10) PCIE_TXP1 (10) PCIE_TXN1
(10) PCIE_RXP1 (10) PCIE_RXN1
C126 .1U_4 PERP1
C125 .1U_4 PERN1
(13) CLK_PCIE_NEW (13) CLK_PCIE_NEW#
CPPE#
(13) NEW_CLKREQ#
+NEW_3V
NEW_PERST#
+NEW_3VAUX
NEWCARD_PCIE_WAKE#
+NEW_1.5V
(13,15,19) PDAT_SMB (13,15,19) PCLK_SMB
CPUSB#
(15) USBP4+ (15) USBP4-
R95 0_4 BUSBP4+
R94 0_4 BUSBP4-

GND5 29 GND1 26 PETp0 25 PETn0 24 GND2 23 PERp0 22 PERn0 21 GND3 20 REFCLK+ 19 REFCLK- 18 CPPE# 17 CLKREQ# 16 +3.3V1 15 +3.3V2 14 PERST# 13 +3.3VAUX 12 WAKE# 11 +1.5V1 10 +1.5V2 9 SMB_DATA 8 SMB_CLK 7 RESERVED1 6 RESERVED2 5 CPUSB# 4 USB_D+ 3 USB_D- 2 GND4 1 GND6 30

+3V_S5 Q13 DTC144EUA
(15,19) PCIE_WAKE# NEWCARD_PCIE_WAKE#

NEW CARD'S POWER SWITCH

U8 TPS2231PWG4

+3V 4 5 3.3VIN 3.3VOUT 6 7 +NEW_3V
+3V_S5 18 AUXIN AUXOUT 17 +NEW_3VAUX
+1.5V 16 15 1.5VIN 1.5VOUT 14 13 +NEW_1.5V
(11,14,19,21,23) ALINK_RST# 1 SYSRST# STBY# 3
2 SHDN# CPPE# 12 CPPE#
CPUSB# 11 CPUSB#
19 RCLKEN
9 NC PERST# 8 NEW_PERST#
10 GND OC# 20

CPPE# : (Internal Pull Up , active low when card support PCIE)
CPUSB# : (Internal Pull Up , active low when card support USB)
SHDN# : (Internal Pull Up)

+3V C155 .1U_4 +3V_S5 C141 .1U_4 +1.5V C158 .1U_4
+NEW_3VAUX C152 .1U_4
+NEW_3V C168 10U/10V/X5R_8 C160 .1U_4 C166 .1U_4
+NEW_1.5V C167 10U/10V/X5R_8 C162 .1U_4

PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
	PCI8402-1 & NEW CARD	2A
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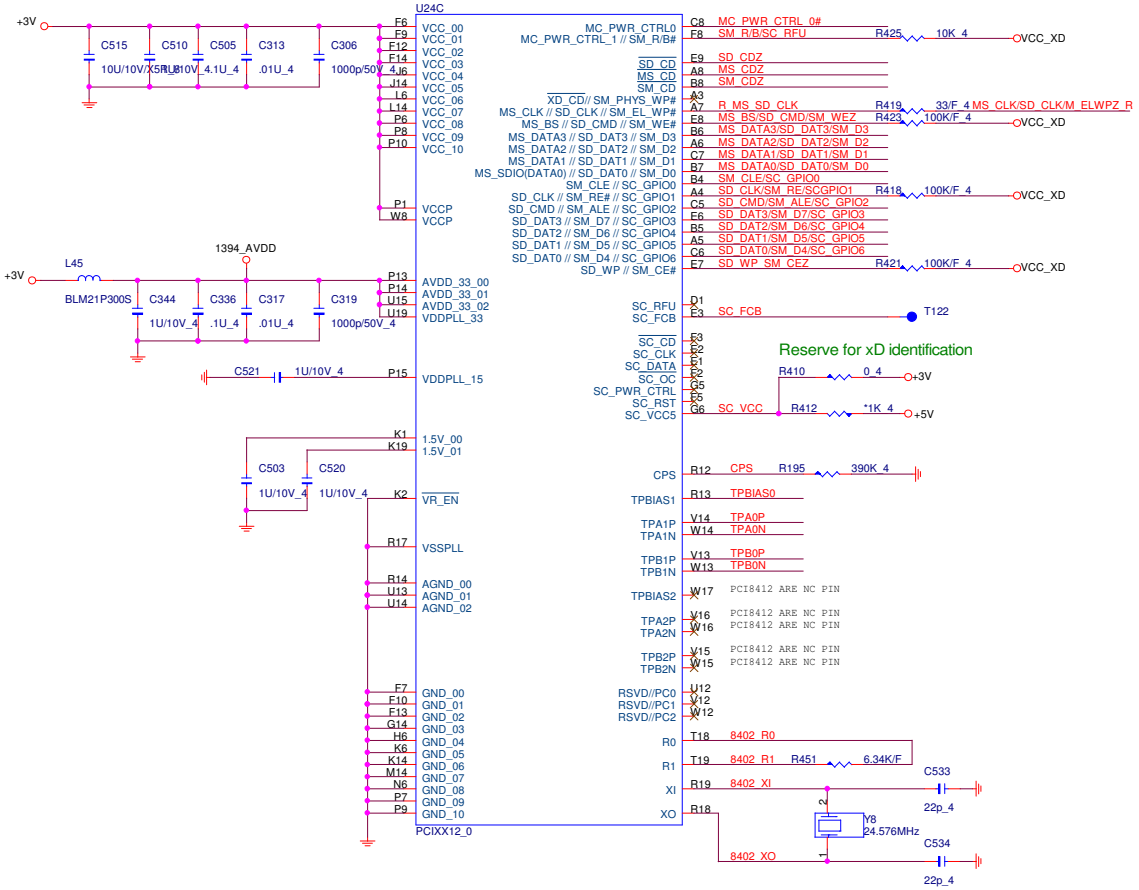
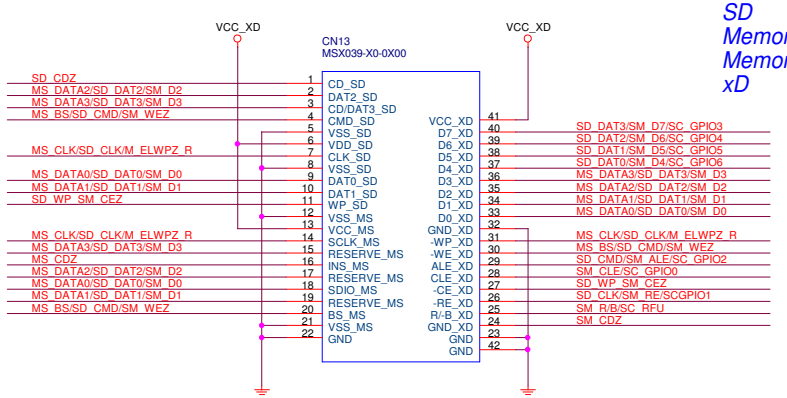
PCI8402 I/F OF 1394 & CARD READER



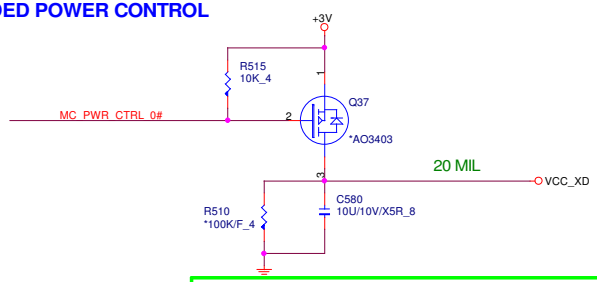
5 IN 1 MEMORY CARD READER

Support :

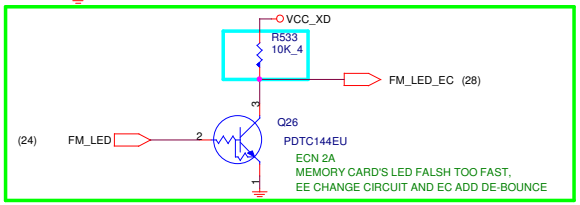
MMC
SD
Memory Stick
Memory Stick Pro
xD



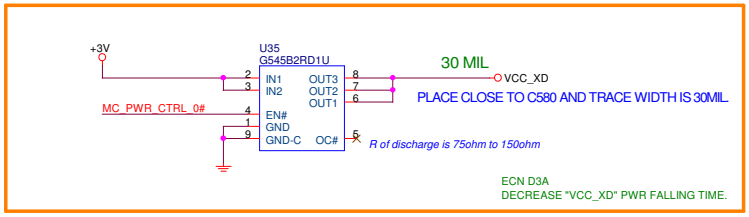
MEMORY CARD READED POWER CONTROL



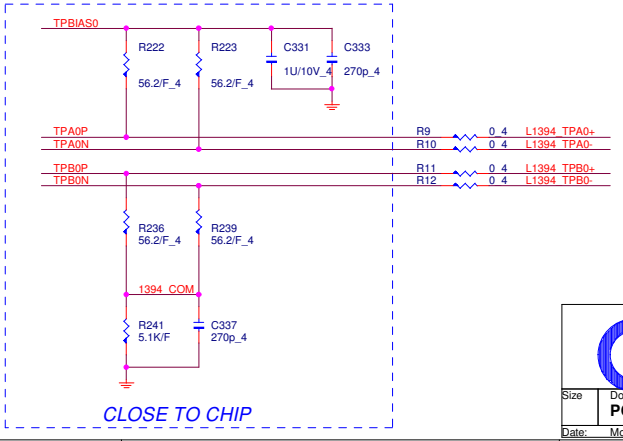
MEMORY CARD READED LED INDICATE

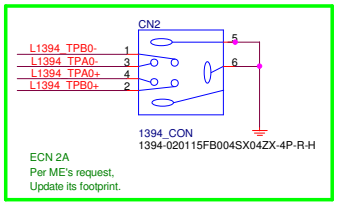


MEMORY CARD READED POWER CONTROL (IC SOLUTION FOR C-TEST)



IEEE1394 CONNECTOR





IEEE1394 & CARD REDER

PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
	PCI8402-2 (1394 & 5 IN 1)	2A
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AUDIO CODEC ALC262

ALC262 GPIO TABLE

GPIO 0	SRS	LO: SRS OFF (EC) HI: SRS ON (EC)
GPIO 1	H.P.	LO: NO PLUG-IN HI: PLUG-IN

D3A In order to Vista's request,
EAPD force MUTE,Remove Q34,R490

60 mils

RESERVE BYPASS PATH

ECN C2B
ADD CODEC_JD

ECN C2B
PER VISTA REQUEST,
MODIFY MIC PATH

ECN C2B
PER VISTA REQUEST,
ADD PWR FOR MIC.

Layout note:

CD_GND	5mil	5mil
CD_L	5mil	10mil
CD_GND	5mil	5mil
CD_R	5mil	10mil
CD_GND	5mil	5mil

AUDIO POWER AND GND

20 mil

20 mil

Vout=Vset(1+R(4,5)/R(5,gnd))
Vset=1.25V

Vout=1.25(1+29.4K/10K)=4.925V
Vout=1.25(1+28.7K/10K)=4.8375V
Vout=1.25(1+27K/10K)=4.625V

SPRAY THE BRIDGE ON THE GAP OF A/DGND UNIFORMLY.

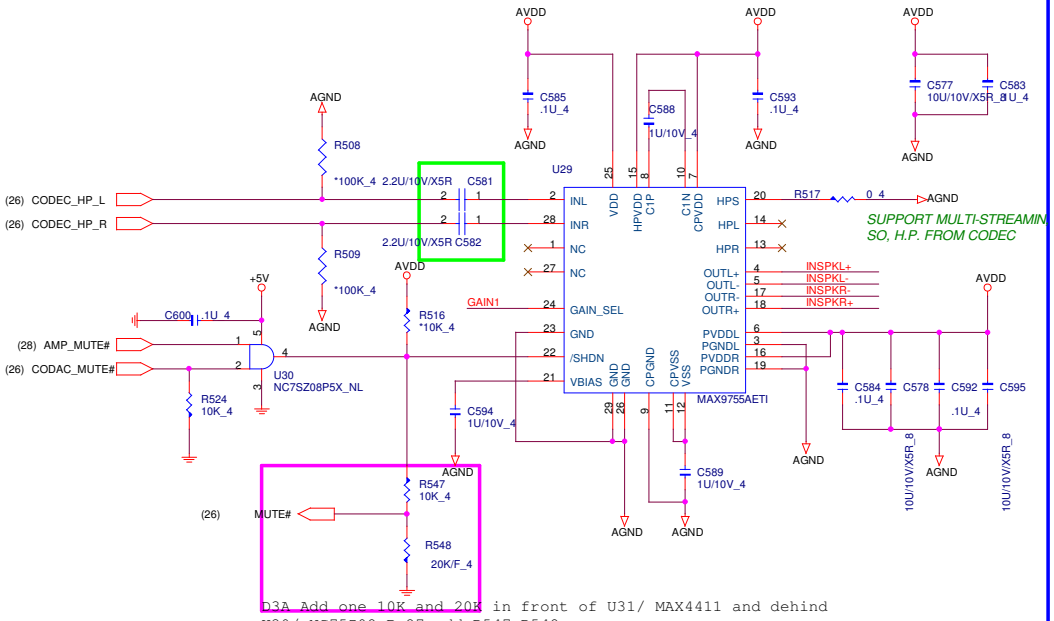
AZALIA MDC INTERFACE

AUDIO CODEC & MDC

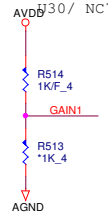
PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
	AUDIO CODEC ALC262 AND MDC	2A
Date: Monday, April 10, 2006	Sheet 26 of 34	

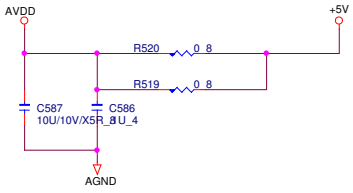
AUDIO AMP. (MAX9755)

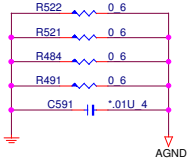


D3A Add one 10K and 20K in front of U31/ MAX4411 and dehind U30/ NC75Z08 P.27 add R547,R548



GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0

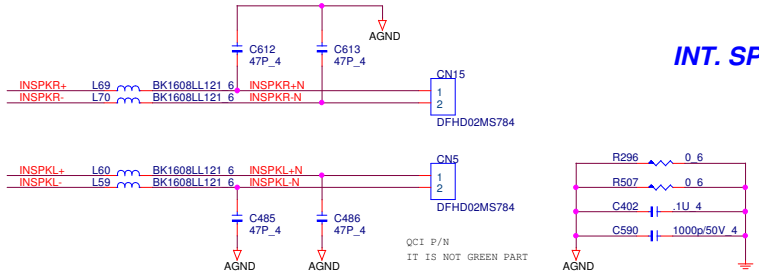




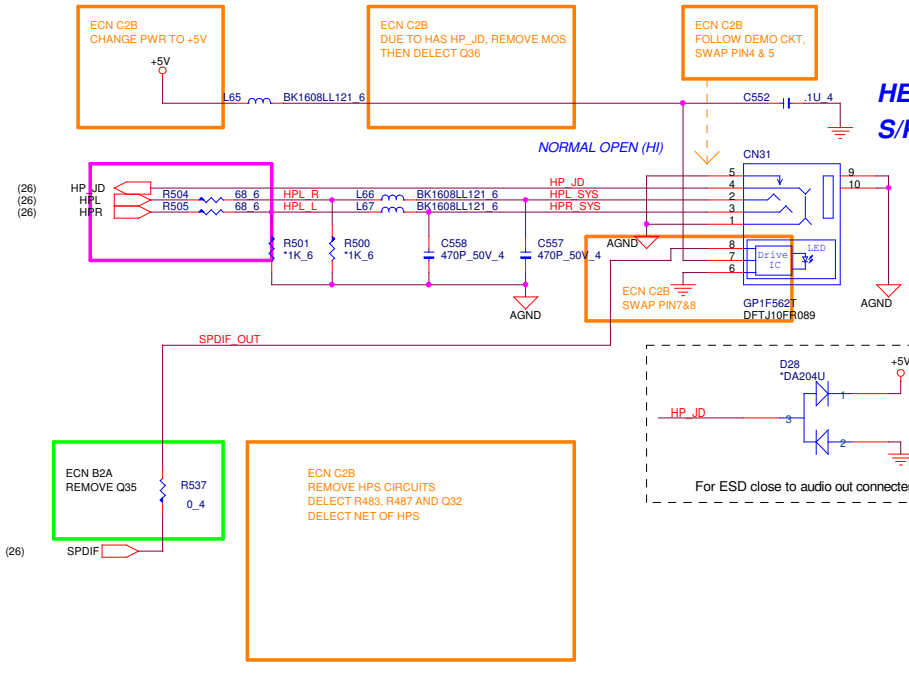
AMP. POWER SUPPLY

AUDIO JACK

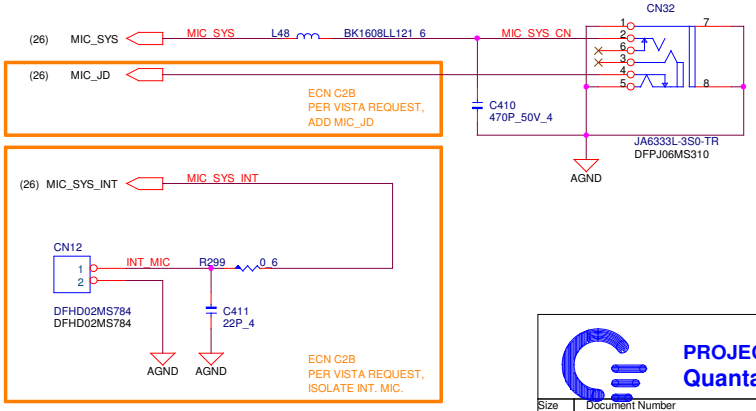
INT. SPEAKER



HEADPHONE OUT S/PDIF



MICROPHONE IN



AUDIO AMP. & JACK

PROJECT : ED5
Quanta Computer Inc.

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	AMP. & JACK	1A
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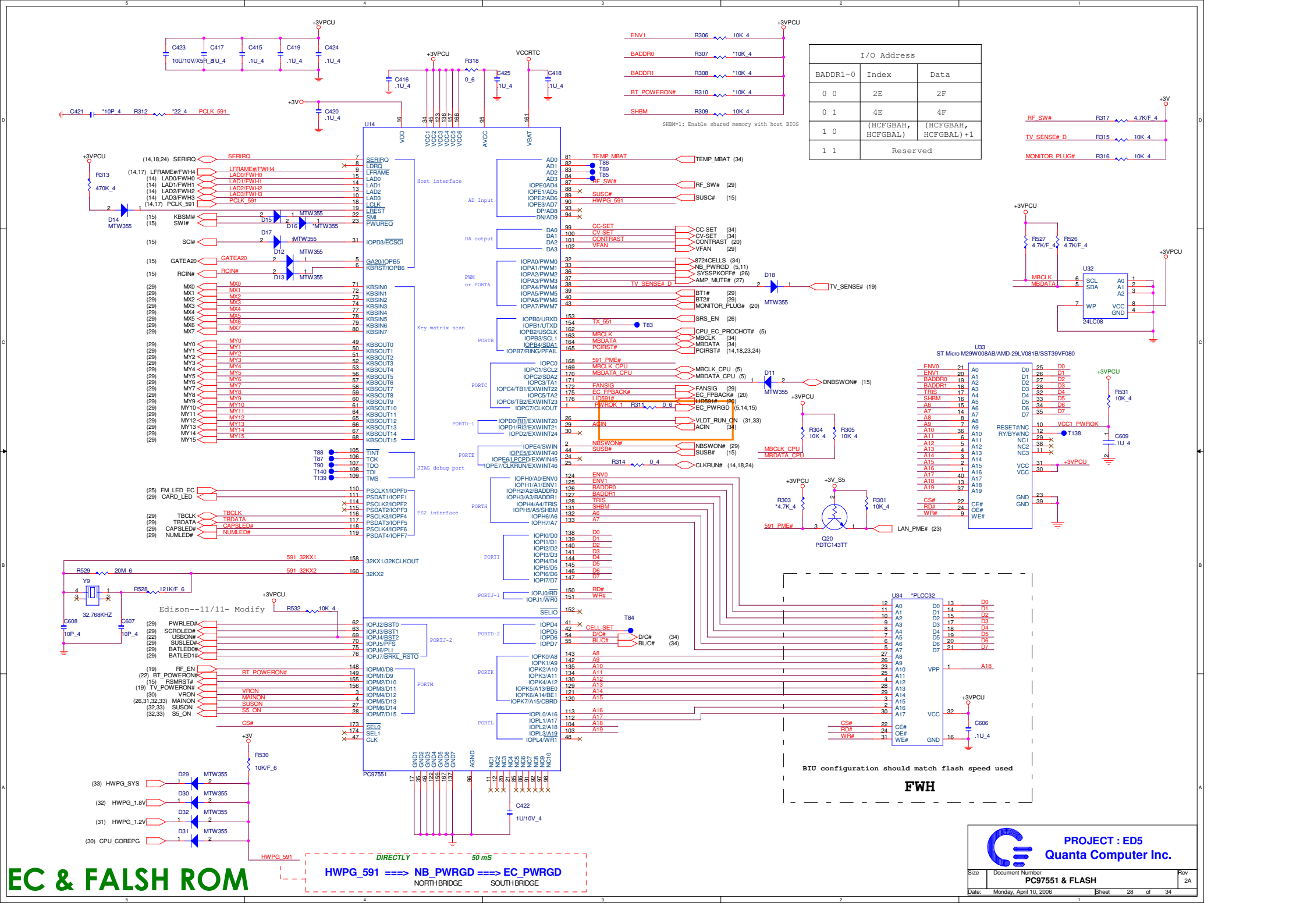
U14
PC97551
Host interface
AD Input
DA output
PWM or PORTA
Key matrix scan
PORTB
PORTC
PORTD-1
PORTE
JTAG debug port
PS2 interface
PORTH
PORTI
PORTJ-1
PORTD-2
PORTJ-2
PORTK
PORTM
PORTL
SERIRQ
LFRAME#/FWH4
LAD0/FWH0
LAD1/FWH1
LAD2/FWH2
LAD3/FWH3
PCLK_591
KBSMI#
SWI#
SCI#
GATEA20
RCIN#
MX0
MX1
MX2
MX3
MX4
MX5
MX6
MX7
MY0
MY1
MY2
MY3
MY4
MY5
MY6
MY7
MY8
MY9
MY10
MY11
MY12
MY13
MY14
MY15
FM_LED_EC
CARD_LED
TBCLK
TBDATA
CAPSLED#
NUMLED#
PWRLED#
SCROLED#
USBON#
SUSLED#
BATLED0#
BATLED1#
RF_EN
BT_POWERON#
RSMRST#
TV_POWERON#
VRON
MAINON
SUSON
S5_ON
CS#
SEL0
SEL1
CLK
TEMP_MBAT
SUSC#
HWPG_591
CC-SET
CV-SET
CONTRAST
VFAN
TV_SENSE# D
TX_551
MBCLK
MBDATA
PCIRST#
591_PME#
MBCLK_CPU
MBDATA_CPU
FANSIG
EC_FPBACK#
LID591#
PWROK_1
EC_PWRGD
ACIN
NBSWON#
SUSB#
CLKRUN#
ENV0
ENV1
BADDR0
BADDR1
TRIS
SHBM
A6
A7
D/C#
BL/C#
CELL-SET
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
591_32KX1
591_32KX2
32KX1/32KCLKOUT
32KX2
32.768KHZ
Edison--11/11- Modify
SELIO
+3VPCU
+3V
VCCRTC
VDD
VCC1
VCC2
VCC3
VCC4
VCC5
VCC6
AVCC
VBAT
AGND
GND1
GND2
GND3
GND4
GND5
GND6
GND7
NC1
NC2
NC3
NC4
NC5
NC6
NC7
NC8
NC9
NC10
ENV1 R306 10K_4
BADDR0 R307 *10K_4
BADDR1 R308 *10K_4
BT_POWERON# R310 *10K_4
SHBM R309 10K_4
SHBM=1: Enable shared memory with host BIOS
I/O Address
BADDR1-0 | Index | Data
0 0 | 2E | 2F
0 1 | 4E | 4F
1 0 | (HCFGBAH, HCFGBAL) | (HCFGBAH, HCFGBAL)+1
1 1 | Reserved
RF_SW# R317 4.7K/F_4
TV_SENSE# D R315 10K_4
MONITOR_PLUG# R316 10K_4
U32
24LC08
SCL
SDA
WP
U33
ST Micro M29W008AB/AMD-29LV081B/SST39VF080
RESET#/NC
RY/BY#/NC
VCC1_PWROK
U34 *PLCC32
VPP
BIU configuration should match flash speed used
FWH
HWPG_591 ===> NB_PWRGD ===> EC_PWRGD
DIRECTLY
50 mS
NORTH BRIDGE
SOUTH BRIDGE
EC & FALSH ROM
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Quanta Computer Inc.
PC97551 & FLASH
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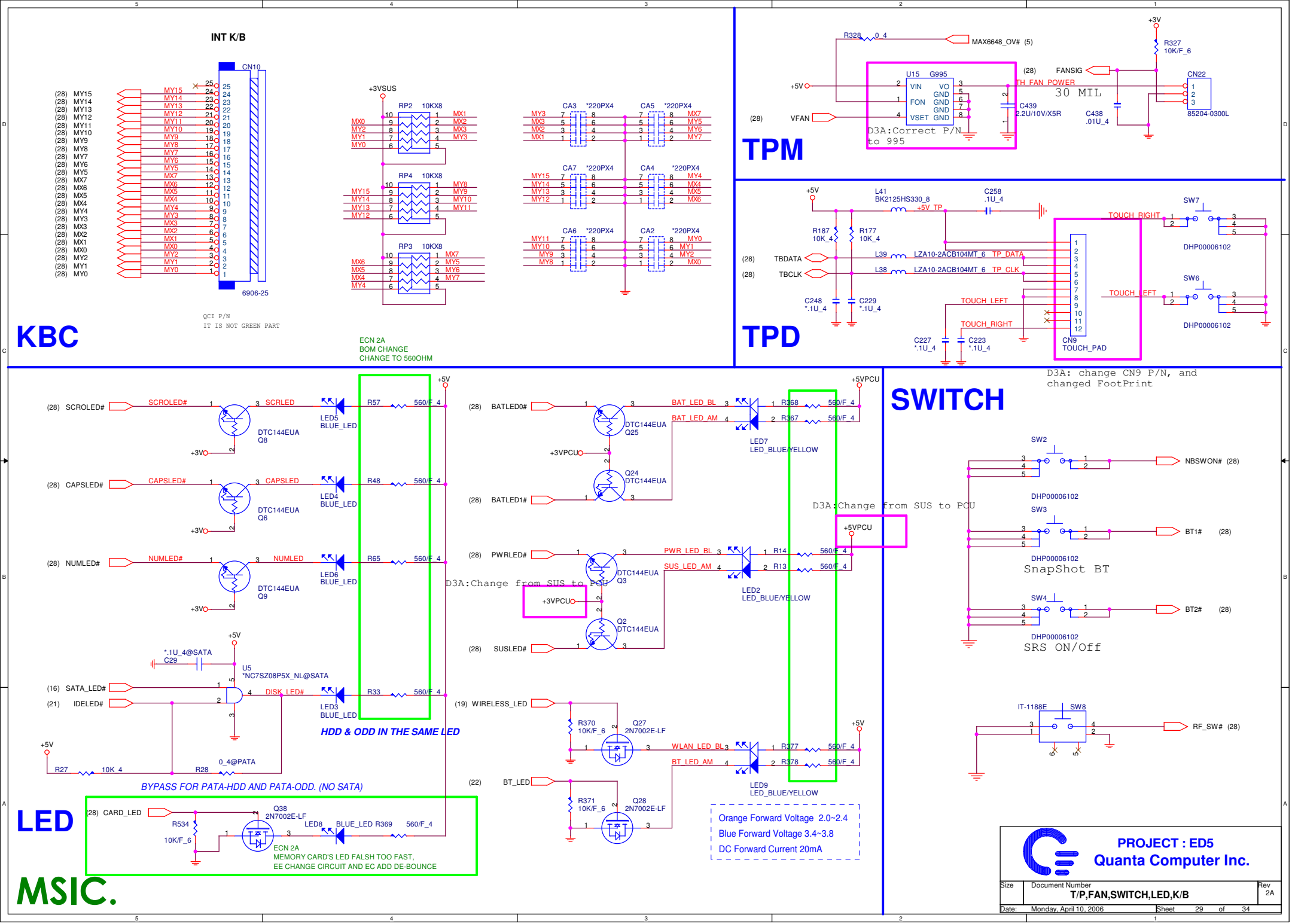
INT K/B
CN10
6906-25
QCI P/N
IT IS NOT GREEN PART
KBC
+3VSUS
RP2 10KX8
RP4 10KX8
RP3 10KX8
ECN 2A
BOM CHANGE
CHANGE TO 560OHM
TPM
R328 0_4
MAX6648_OV# (5)
U15 G995
D3A:Correct P/N to 995
FANSIG
TH_FAN_POWER
30 MIL
R327 10K/F_6
CN22
85204-0300L
C439 2.2U/10V/X5R
C438 .01U_4
TPD
L41 BK2125HS330_8
+5V_TP
C258 .1U_4
R187 10K_4
R177 10K_4
TBDATA
TBCLK
L39 LZA10-2ACB104MT_6 TP_DATA
L38 LZA10-2ACB104MT_6 TP_CLK
C248 *.1U_4
C229 *.1U_4
TOUCH_LEFT
TOUCH_RIGHT
SW7
SW6
DHP00006102
C227 *.1U_4
C223 *.1U_4
CN9
TOUCH_PAD
D3A: change CN9 P/N, and changed FootPrint
SWITCH
SW2
NBSWON# (28)
SW3
BT1# (28)
SnapShot BT
SW4
BT2# (28)
SRS ON/Off
IT-1188E SW8
RF_SW# (28)
LED
SCROLED#
CAPSLED#
NUMLED#
DTC144EUA
LED5 BLUE_LED
LED4 BLUE_LED
LED6 BLUE_LED
R57 560/F_4
R48 560/F_4
R65 560/F_4
SATA_LED#
IDELED#
U5 *NC7SZ08P5X_NL@SATA
LED3 BLUE_LED
R33 560/F_4
HDD & ODD IN THE SAME LED
BYPASS FOR PATA-HDD AND PATA-ODD. (NO SATA)
CARD_LED
Q38 2N7002E-LF
LED8 BLUE_LED R369 560/F_4
ECN 2A
MEMORY CARD'S LED FALSH TOO FAST,
EE CHANGE CIRCUIT AND EC ADD DE-BOUNCE
BATLED0#
BATLED1#
BAT_LED_BL
BAT_LED_AM
LED7 LED_BLUE/YELLOW
PWRLED#
SUSLED#
PWR_LED_BL
SUS_LED_AM
LED2 LED_BLUE/YELLOW
D3A:Change from SUS to PCU
WIRELESS_LED
BT_LED
WLAN_LED_BL
BT_LED_AM
LED9 LED_BLUE/YELLOW
Orange Forward Voltage 2.0~2.4
Blue Forward Voltage 3.4~3.8
DC Forward Current 20mA
MSIC.
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Quanta Computer Inc.
Size
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T/P,FAN,SWITCH,LED,K/B
Rev 2A
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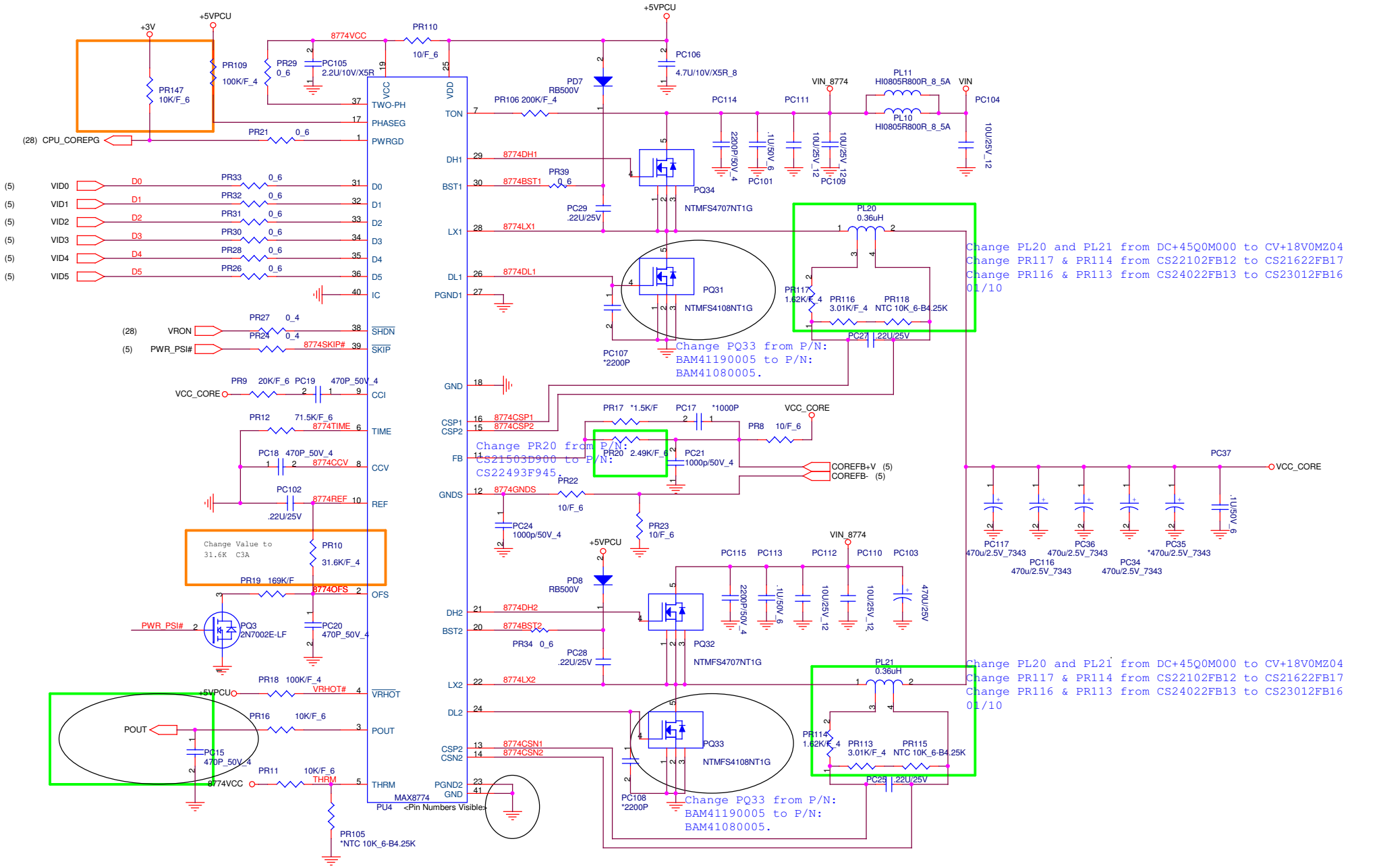

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Size	Document Number	Rev
	CPU CORE MAX8760	2A
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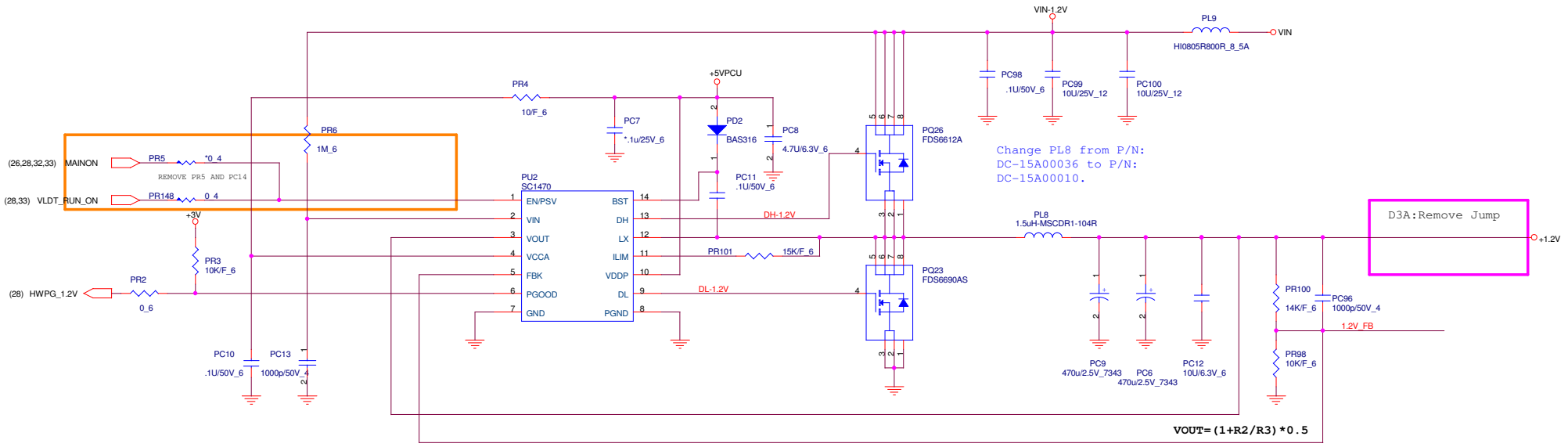
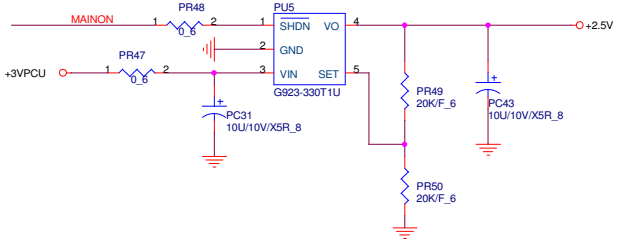
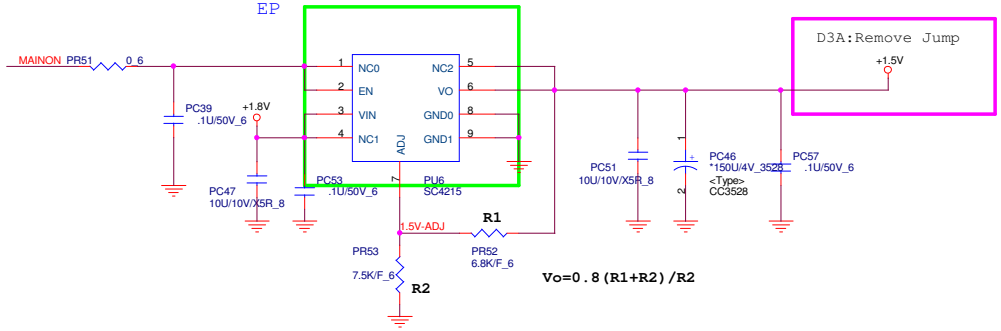


Change PL8 from P/N: DC-15A00036 to P/N: DC-15A00010.



Change PU6 from P/N: AL004215003 to P/N: AL004215011 . BOM typo. Lead -> EP



Vout =1.25(1+R1/R2)
= 1.25 (1+20K/20K)
= 2.5V

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Custom	+1.2V & NBRUN	2A
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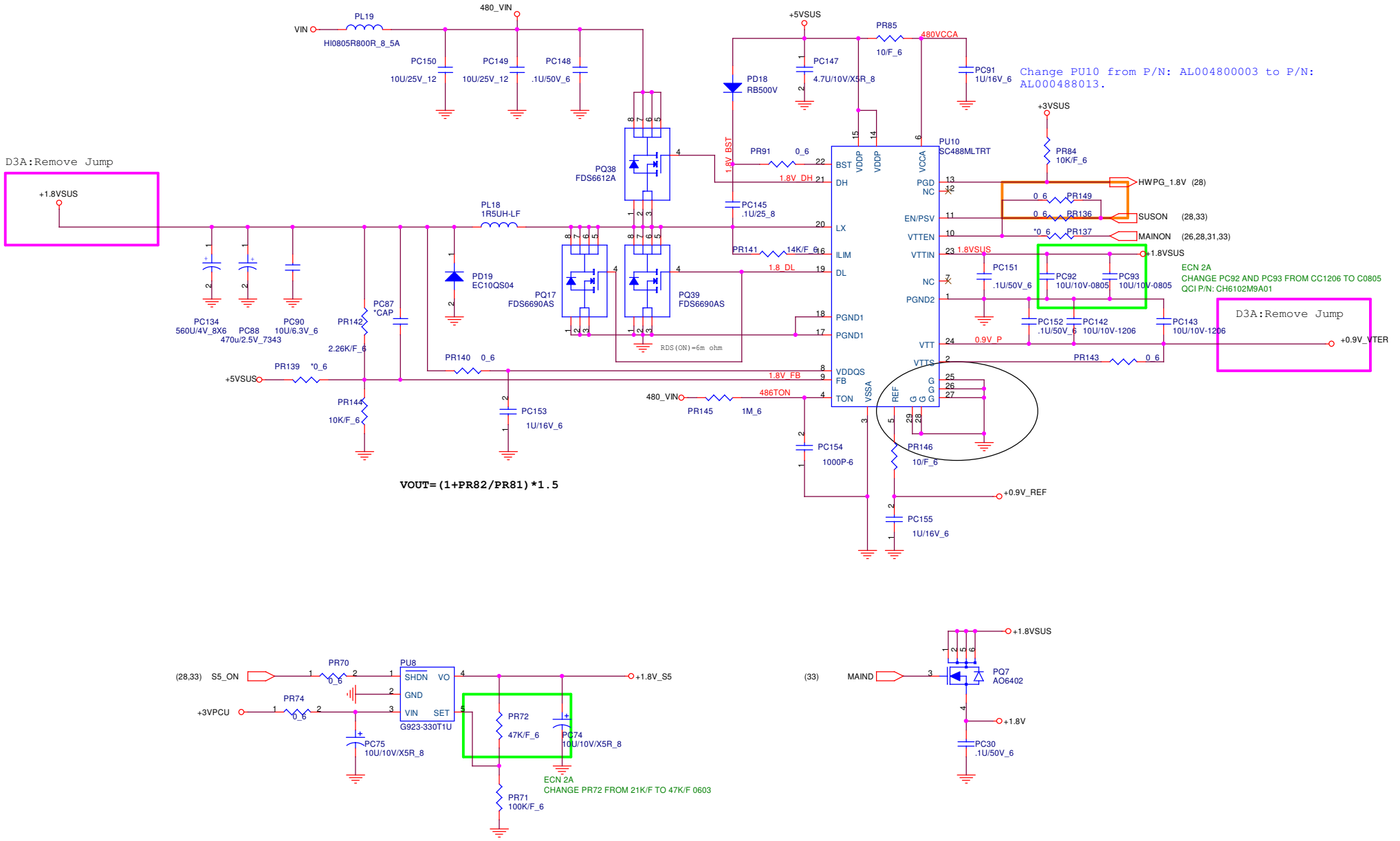

PROJECT : ED5

Quanta Computer Inc.

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Custom	1.8V&DDR	2A
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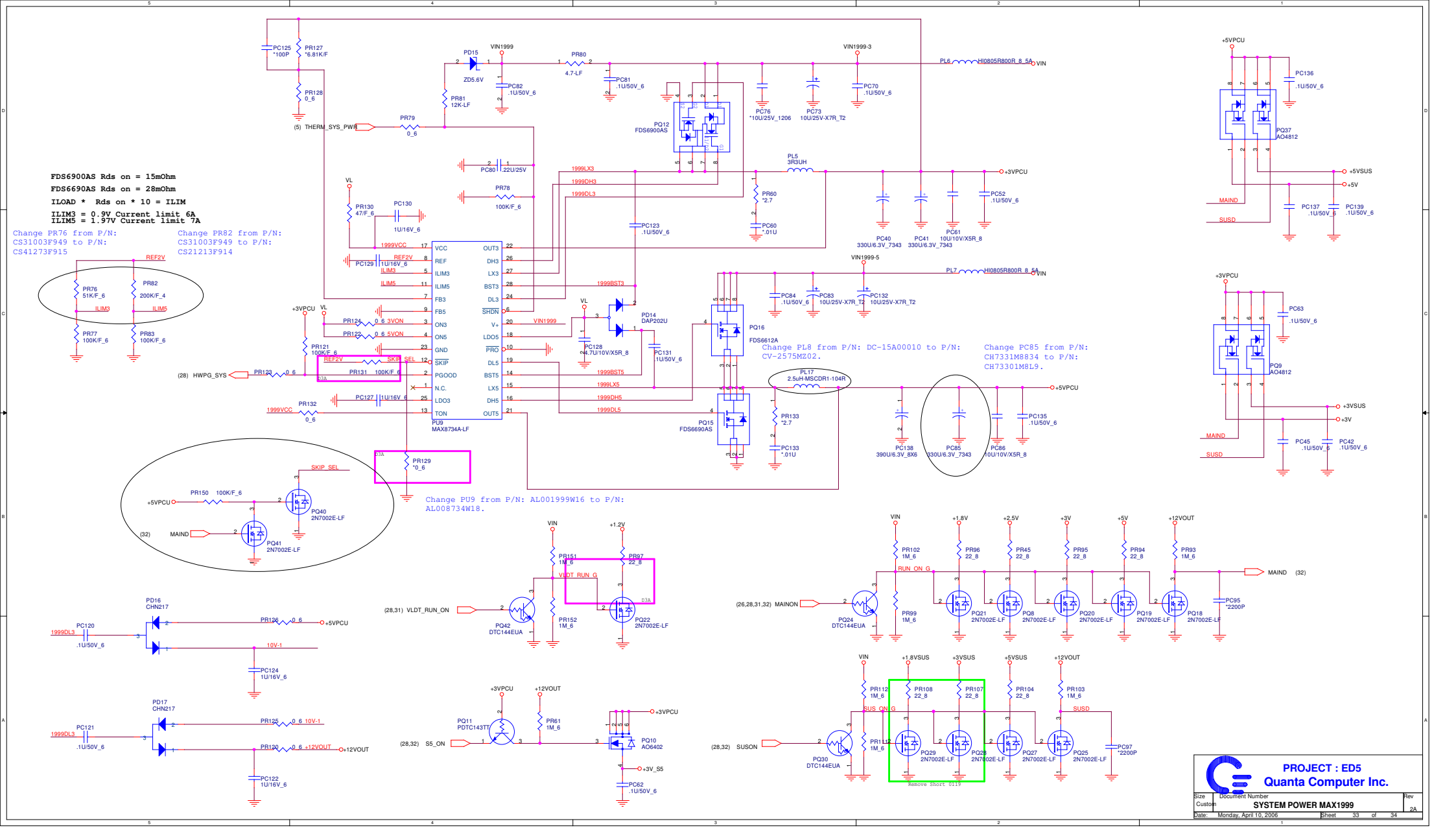
FDS6900AS Rds on = 15mOhm
FDS6690AS Rds on = 28mOhm
ILOAD * Rds on * 10 = ILIM
ILIM3 = 0.9V Current limit 6A
ILIM5 = 1.97V Current limit 7A
Change PR76 from P/N: CS31003F949 to P/N: CS41273F915
Change PR82 from P/N: CS31003F949 to P/N: CS21213F914
Change PL8 from P/N: DC-15A00010 to P/N: CV-2575MZ02.
Change PC85 from P/N: CH7331M8834 to P/N: CH73301M8L9.
Change PU9 from P/N: AL001999W16 to P/N: AL008734W18.
PU9 MAX8734A-LF
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Quanta Computer Inc.
SYSTEM POWER MAX1999
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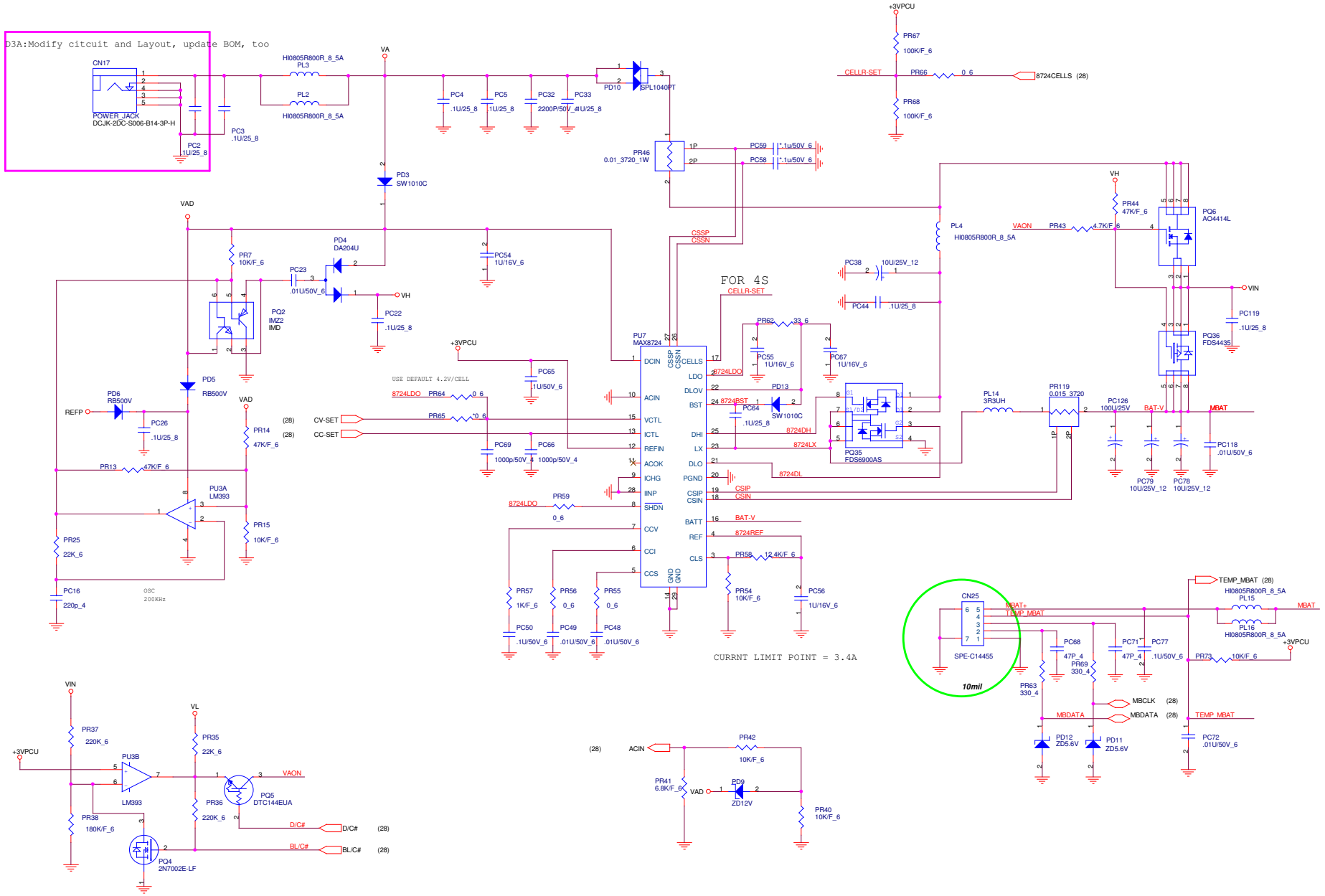

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C	BATTERY CHARGER	2A

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