TW3A- DESIGN

1

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

RUN POWER SW PG 43

AC/BATT CONNECTOR PG 40

BATT CHARGER PG 40

Yonah/Merom
31W/35W
(478 Micro-FCPGA)
PG 4,5

CPU VR PG 37

DC/DC +3VSUS +5VSUS PG43

DC/DC +3VPCU +5VPCU PG38

DC/DC +1.05V +1.5V PG37

CLOCKS
ICS954206
PG 3

FSB 133MHZ

DDRII VR PG 39

DDRII-SODIMM1 PG 16,17

DDRII-SODIMM2 PG 16,17

DDRII 667mhz

DDRII 667mhz

Calistoga PM
945PM
Integraded VGA Function
1466 BGA
PG 6,7,8,9,10,11

PCI-Express 16X

nVIDIA
NV72M/MV
(64 Bit B/W)

DDRII
16M*16(128MB)
32M*16(256MB)
(Bank*4)

PG 18~21

DC/DC VGA CORE PG42

LVDS(2 Channel)

Panel Connector PG 22

TVOUT

S-Video PG 35

VGA

VGA,DVI PG 23

DMI interface

USB2.0 (P5)

Bluetooth PG 33

USB2.0 (P0~P7)

USB2.0 (P0~P1,P4)

USB2.0 I/O Ports PG 26

SATA - HDD PG 29

PATA - HDD PG 29

Internal ODD CD-ROM PG 29

SATA0

PATA 100

ICH7-M

652 BGA

PG 12,13,14,15

PCI-E, 1X

LAN
88E8038/88E8055
PG 24

Magnetics PG 25

RJ45 PG 25

PCI-E, 1X

Mini PCI-E Card
PCI Express Mini Card
PG 33

PCI-E, 1X

Express Card x1
NEW CARD
PG 33

Azalia

PCI Bus 33MHz

Conexant Audio
CX20549-12
PG 30

LPC

TI PC7402
PG 27

IEEE1394 CONN
3 in 1 Card reader
PG28

AUDIO Amplifier PG 31

MDC DAA CX20548-A PG 32

TPM1.2 PG 44

KBC
PC87541V
PG 36

X-Bus

Jack to Speaker PG 31

Audio Jacks PG 30

MODEM RJ 11 PG 32

Key Matrix PG 34

Touch Pad PG 34

Flash PG 36

- Power Input
- LPT PORT
- COM PORT
- LAN
- VGA
- Headphone
- 1394
- USB X 2

RQ6

Replicator Daughter Board

USB

PG 35

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ2# / GNT2#	AD17	INTC#,INTD#	TI 7402

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram	B1A

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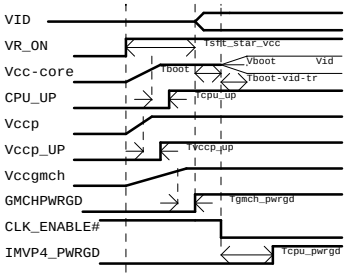
Board Stack up Description

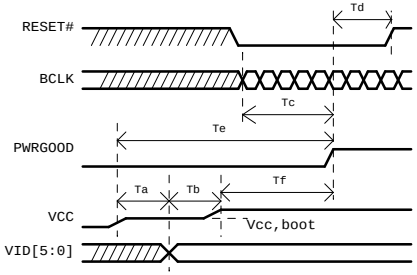
PCB Layers

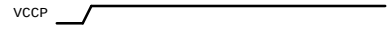
Layer 1		TOP(Component,Other)
Layer 2		Ground Plane
Layer 3		IN1
Layer 4		IN2
Layer 5		Power Plane
Layer 6		IN3
Layer 7		Ground Plane
Layer 8		BOTTOM

Power On Sequencing Timing Diagram



Dothan Power-up Timing Specifications



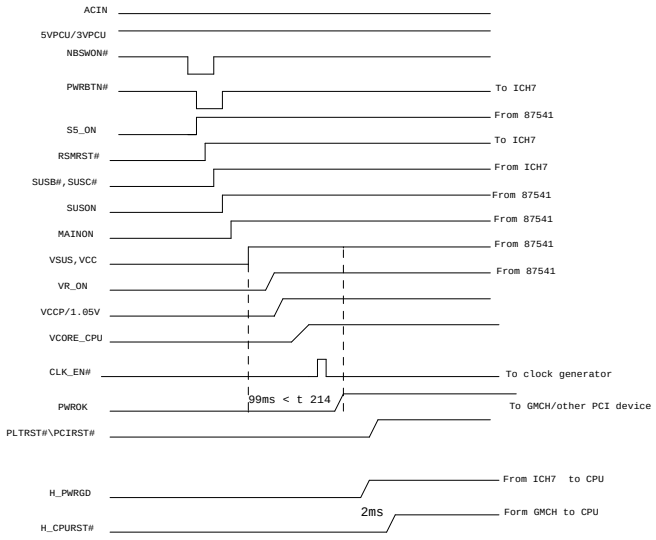


Ta=VCC and VCCP asseration to VID[5:0] vaild
Tb=VID[5:0] stable to VCC vaild
Tc=BCLK stable to PWRGOOD assertion
Td=PWRGOOD to RESET# de-assertion time
Te=Vcc,boot vaild to PWRGOOD assertion time

Voltage Rails

Voltage Rails		ON S0~S2	ON S3	ON S4	ON S5	Control signal
VCC_CORE	Core voltage for Processor	X				VR_ON 0.726V~0.94V
VCCP	Core voltage for CPU / NB	X				VR_ON
SMDDR_VTERM	0.9V for DDR2 Termination voltage	X				MAINON
RVCC1.5		X	X	X		RVCC_ON
RVCC3		X	X	X		RVCCD
VCC1.5		X				MAIND
VCC2.5		X				MAINON
VCC3		X				MAIND
VCC5		X				MAIND
1.8VSUS		X	X			SUSON
3VSUS		X	X			SUSD
5VSUS		X	X			SUSD
3VPCU		X	X	X	X	VL
5VPCU		X	X	X	X	VL
9VPCU		X	X	X	X	5VPCU

ACIN POWER ON TIMING



Voltage Rails		ON S0~S1	ON S3	ON S4	ON S5	Control signal
VCC_CORE	Core voltage for Processor	X				VRON
GMCH_VTT	Core voltage for GMCH 1.05V	X				MAINON
SMDDR_VTERM	0.9V for DDR II Termination voltage	X				MAINON
SMDDR_VREF	0.9V for DDR II Reference Voltage	X				MAINON
GMCH_1.5V		X				MAINON
1.8VSUS	1.8V for DDR II voltage	X	X			SUSON
+2.5V		X				MAINON
3VPCU		X	X	X	X	VL
3VSUS		X	X			SUSON
+3V		X				MAINON
5VPCU		X	X	X	X	VL
5VSUS		X	X			SUSON
+5V		X				MAINON
VIN	POWER SOURCE	X	X	X	X	

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI7402	AD17	REQ2# / GNT2#	PIRQ C/D

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	System Information	81A

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FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

Place these termination to close CK410M. Cause those Pin-out is for Current-Mode.

R135 49.9/F
R131 49.9/F
R133 49.9/F
R134 49.9/F

C419 33p/50V
C434 33p/50V
Y1 14.318MHZ
<500mil
XIN
XOUT

U13
CK-410M
XTAL_IN
XTAL_OUT
VTT_PWRGD#/PD#
PCI_STOP#
CPU_STOP#
SCLK
SDATA
FSA/USB_48
FSB/TEST_MODE
FSC/TEST_SEL
VDD_REF
VDD_CPU
VDD_PCI_1
VDD_PCI_2
VDD_SRC0
VDD_SRC1
VDD_SRC2
VDD_48
IREF
DOT96
DOT96#
VDDA
VSSA
REF
CPU0
CPU0#
CPU1
CPU1#
CPU2_ITP/SRC7
CPU2#_ITP/SRC7#
SRC6
SRC6#
SRC5
SRC5#
SRC4
SRC4#
SRC3
SRC3#
SRC2
SRC2#
SRC1
SRC1#
SRC0
SRC0#
PCI5
PCI4
PCI3
PCI2
PCIF1
PCIF0/ITP_EN
GND_48
GND_REF
GND_PCI_1
GND_PCI_2
GND_SRC
GND_CPU

14,37 CLK_EN#
14 PM_STPPCI#
14 PM_STPCPU#
28 TI_CLK48M
14 CLKUSB_48
CLK_EN#
PM_STPPCI#
PM_STPCPU#
TI_CLK48M
CLKUSB_48
R181 10
R180 10
CGCLK_SMB
CGDAT_SMB

SMbus address D2

4,7 CPU_MCH_BSEL0
4,7 CPU_MCH_BSEL1
4,7 CPU_MCH_BSEL2
R426 8.2K/F
R408 8.2K/F
FSA
FSC

VDDREF_CR
CLKVDD
CLKVDD1
VDD48_CR
R132 475/F
IREF

Iref=5mA,
Ioh=4*Iref

R145 33/F
14M_ICH 14
C405 *10p

RP33 RP34 RP35 RP31 RP32 RP40 RP39 RP38 RP37 33x2

R_HCLK_CPU
R_HCLK_CPU#
R_HCLK_MCH
R_HCLK_MCH#
R_PCIE_VGA
R_PCIE_VGA#
R_PCIE_LAN
R_PCIE_LAN#
R_MCH_3GPLL
R_MCH_3GPLL#
R_PCIE_SATA
R_PCIE_SATA#
R_PCIE_ICH
R_PCIE_ICH#
R_PCIE_MINI
R_PCIE_MINI#
R_PCIE_NEW
R_PCIE_NEW#

CLK_CPU_BCLK 4
CLK_CPU_BCLK# 4
CLK_MCH_BCLK 6
CLK_MCH_BCLK# 6
CLK_PCIE_VGA 18
CLK_PCIE_VGA# 18
CLK_PCIE_LAN 24
CLK_PCIE_LAN# 24
CLK_PCIE_3GPLL 7
CLK_PCIE_3GPLL# 7
CLK_PCIE_SATA 12
CLK_PCIE_SATA# 12
CLK_PCIE_ICH 13
CLK_PCIE_ICH# 13
CLK_PCIE_MINI 33
CLK_PCIE_MINI# 33
CLK_PCIE_NEW_C 33
CLK_PCIE_NEW_C# 33

R_PCLK_SIO
R_PCLK_PCM
R_PCLK_LPC_DEBUG
R_PCLK_TPM
R_PCLK_ICH
PCIF0
R169 33/F
R176 33/F
R173 33/F
R144 *33_4
R179 33/F
R177 10K
R170 *10K
R178 10K
+3VRUN

PCLK_541 36
PCLK_PCM 27
PCLK_LPC_DEBUG 33
PCLK_TPM 44
PCLK_ICH 13

PCIF1
1:100 Mhz
0:96 Mhz

0816a

ICS954206AGLFT
250mA (MAX.)

CT_0505: Change footprint to TSSOP56-8_1-5 from TSSOP56-240

Bypass CAPs need to follow Bypass CAP. Routing Rule, no vias between CAP to CHIPSET VCC Pin or GND.

Tie to VCC (Logic 1) is for ITP using.
Tie to GND (Logic 0) is for PCIE using.

+3VRUN
L21 HB-1T2012-121JT
120 ohms@100Mhz
C438 C408 C445 C406 C432
0.047u/10V 0.047u/10V 0.047u/10V 0.047u/10V 4.7u/10V_8
CLKVDD
R149 2.2_6
VDDA_CR
C409 0.047u/10V
C388 4.7u/10V_8

+3VRUN
L22 HB-1T2012-121JT
120 ohms@100Mhz
C446 C443 C441
0.047u/10V 0.047u/10V 4.7u/10V_8
CLKVDD1
R175 2.2_6
VDD48_CR
C444 0.047u/10V
C454 4.7u/10V_8
R146 1/F_6
VDDREF_CR
C407 0.047u/10V

Connect ICH6 SMB
14,33 PDAT_SMB
PDAT_SMB
Q22
RHU002N06
RP27 2.2Kx2
CGDAT_SMB
CGDAT_SMB 16
Connect DDR Module's SMB

These are for backdrive issue

CT_0229: Change MOS to RHU002N06 due to layout concern.

+3VRUN
Q23
14,33 PCLK_SMB
PCLK_SMB
RHU002N06
CGCLK_SMB
CGCLK_SMB 16

CLK_PCIE_VGA
CLK_PCIE_VGA# RP28
CLK_PCIE_LAN
CLK_PCIE_LAN# RP29
CLK_PCIE_MINI
CLK_PCIE_MINI# RP42
CLK_PCIE_NEW_C
CLK_PCIE_NEW_C# RP41
CLK_MCH_3GPLL
CLK_MCH_3GPLL# RP30
CLK_PCIE_SATA
CLK_PCIE_SATA# RP44
CLK_PCIE_ICH
CLK_PCIE_ICH# RP43
49.9x2

Place these termination to close CK410M. Cause those Pin-out is for Current-Mode.

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	CLOCK GENERATOR	B1A

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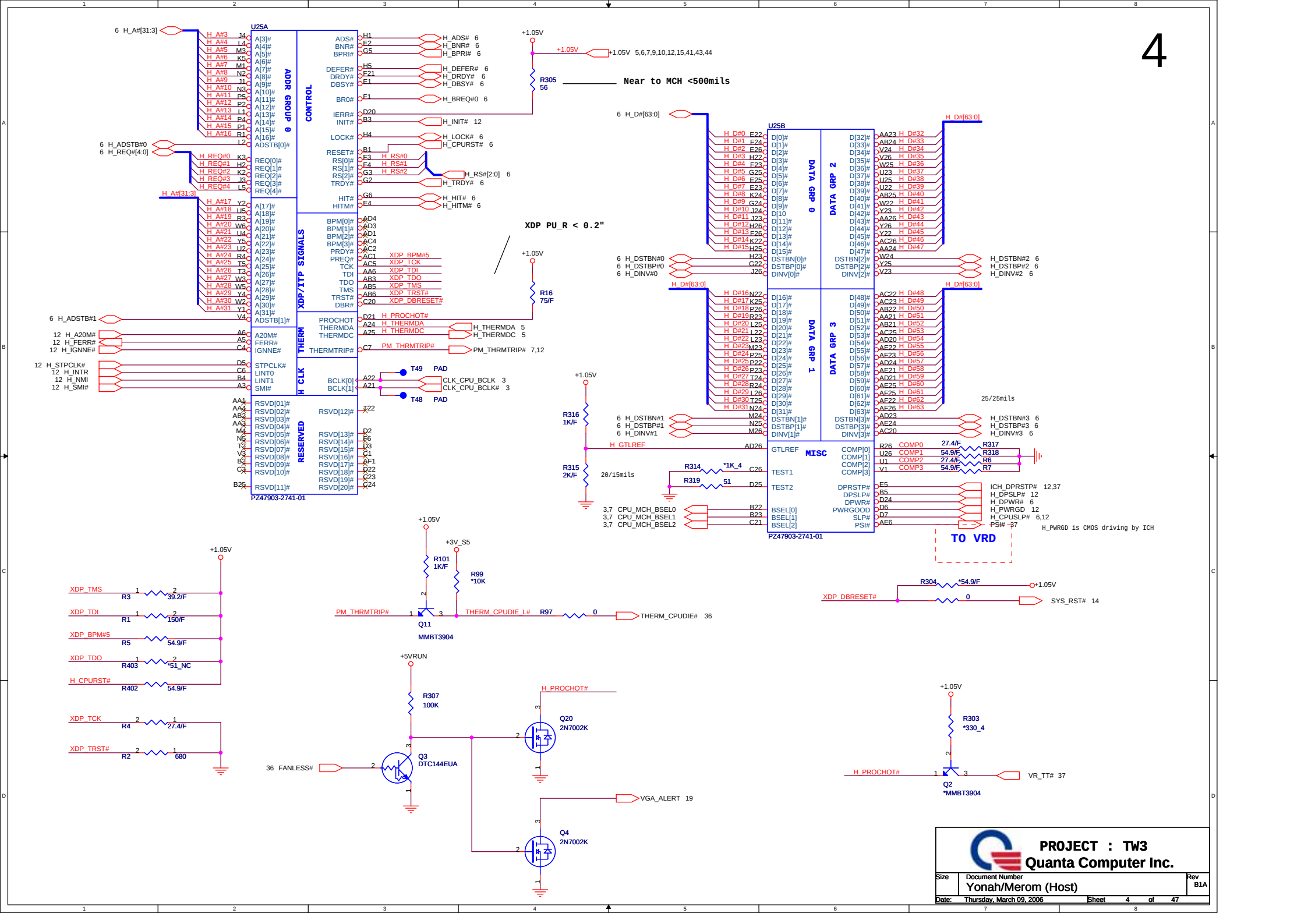
U25A
ADDR GROUP 0
CONTROL
XDP/ITP SIGNALS
THERM
H CLK
RESERVED
PZ47903-2741-01
U25B
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
MISC
PZ47903-2741-01
Near to MCH <500mils
XDP PU_R < 0.2"
TO VRD
H_PWRGD is CMOS driving by ICH
25/25mils
Q11
MMBT3904
Q3
DTC144EUA
Q20
2N7002K
Q4
2N7002K
Q2
*MMBT3904
PROJECT : TW3
Quanta Computer Inc.
Yonah/Merom (Host)
Thursday, March 09, 2006
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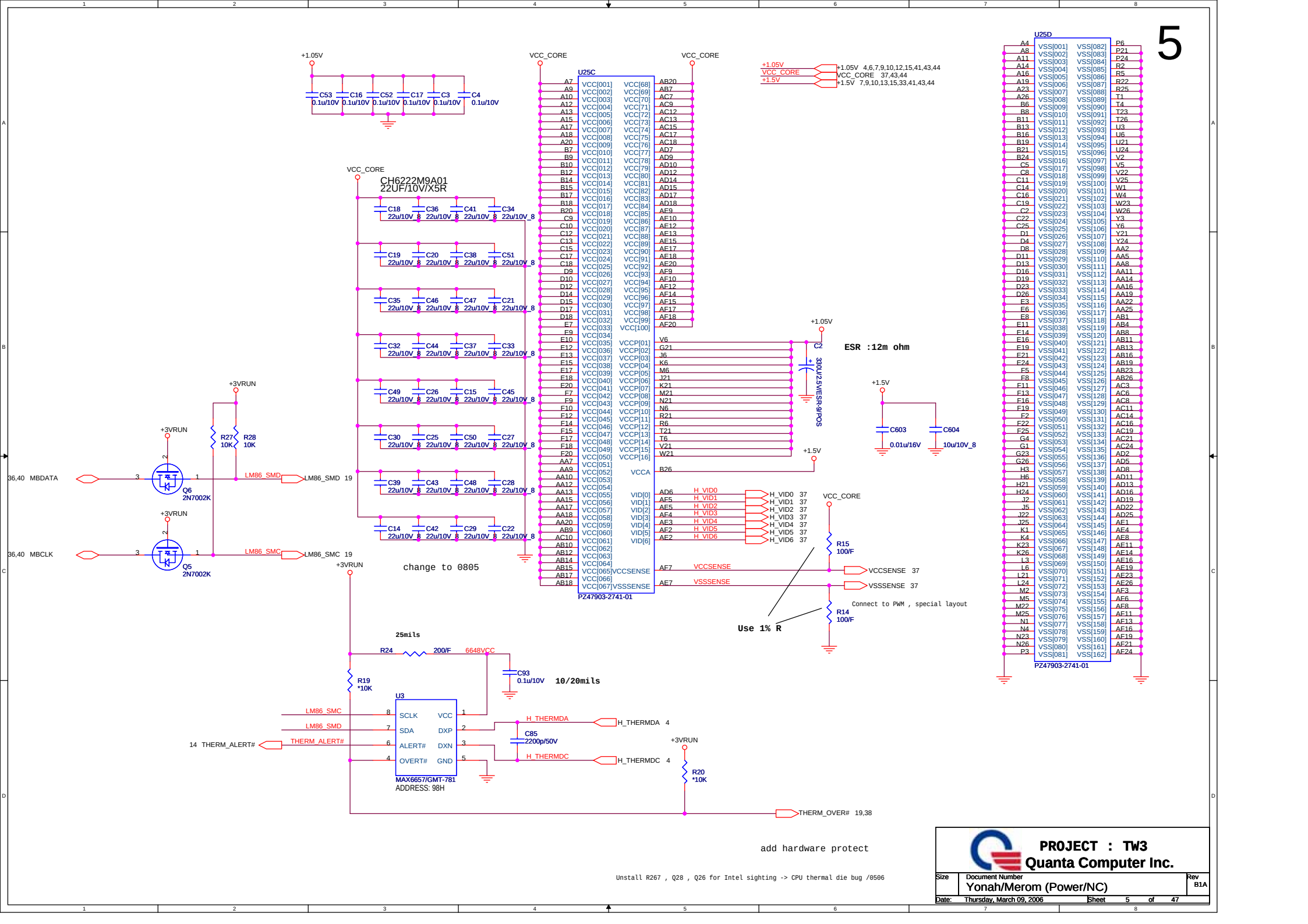
5
+1.05V
VCC_CORE
C53 0.1u/10V
C16 0.1u/10V
C52 0.1u/10V
C17 0.1u/10V
C3 0.1u/10V
C4 0.1u/10V
U25C
PZ47903-2741-01
+1.05V 4,6,7,9,10,12,15,41,43,44
VCC_CORE 37,43,44
+1.5V 7,9,10,13,15,33,41,43,44
U25D
PZ47903-2741-01
CH6222M9A01
22UF/10V/X5R
C18 22u/10V_8
C36 22u/10V_8
C41 22u/10V_8
C34 22u/10V_8
C19 22u/10V_8
C20 22u/10V_8
C38 22u/10V_8
C51 22u/10V_8
C35 22u/10V_8
C46 22u/10V_8
C47 22u/10V_8
C21 22u/10V_8
C32 22u/10V_8
C44 22u/10V_8
C37 22u/10V_8
C33 22u/10V_8
C49 22u/10V_8
C26 22u/10V_8
C15 22u/10V_8
C45 22u/10V_8
C30 22u/10V_8
C25 22u/10V_8
C50 22u/10V_8
C27 22u/10V_8
C39 22u/10V_8
C43 22u/10V_8
C48 22u/10V_8
C28 22u/10V_8
C14 22u/10V_8
C42 22u/10V_8
C29 22u/10V_8
C22 22u/10V_8
C2 330U/2.5V/ESR-9/POS
ESR :12m ohm
C603 0.01u/16V
C604 10u/10V_8
+3VRUN
R27 10K
R28 10K
Q6 2N7002K
Q5 2N7002K
36,40 MBDATA
36,40 MBCLK
LM86_SMD
LM86_SMC
change to 0805
H_VID0 37
H_VID1 37
H_VID2 37
H_VID3 37
H_VID4 37
H_VID5 37
H_VID6 37
VCCSENSE 37
VSSSENSE 37
R15 100/F
R14 100/F
Use 1% R
Connect to PWM , special layout
25mils
R24 200/F 6648VCC
C93 0.1u/10V
10/20mils
R19 *10K
U3
MAX6657/GMT-781
ADDRESS: 98H
SCLK
SDA
ALERT#
OVERT#
VCC
DXP
DXN
GND
THERM_ALERT#
H_THERMDA 4
H_THERMDC 4
C85 2200p/50V
R20 *10K
THERM_OVER# 19,38
add hardware protect
Unstall R267 , Q28 , Q26 for Intel sighting -> CPU thermal die bug /0506
PROJECT : TW3
Quanta Computer Inc.
Size
Document Number
Yonah/Merom (Power/NC)
Rev B1A
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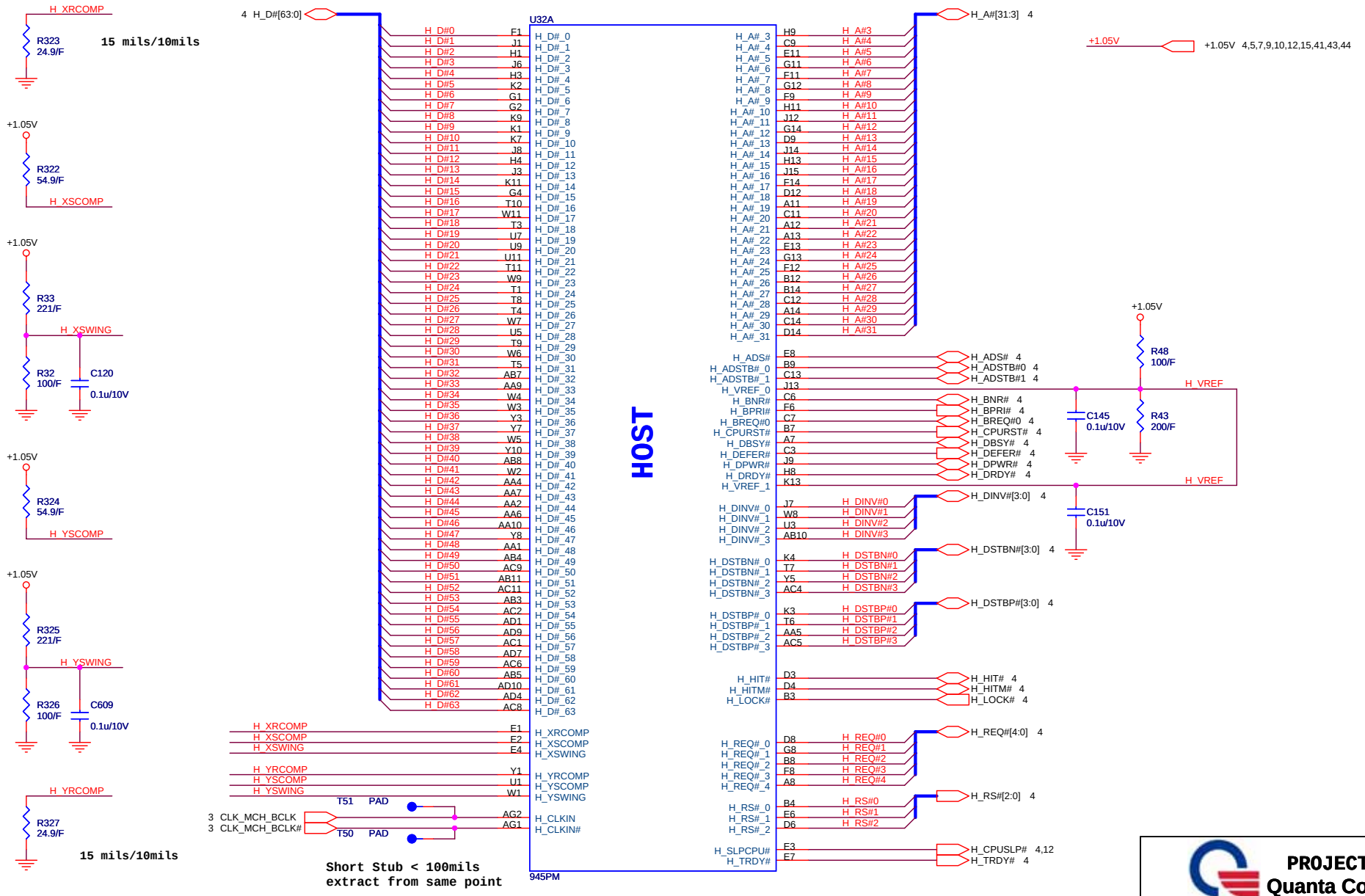
H_XRCOMP
R323 24.9/F
15 mils/10mils
+1.05V
R322 54.9/F
H_XSCOMP
+1.05V
R33 221/F
H_XSWING
R32 100/F
C120 0.1u/10V
+1.05V
R324 54.9/F
H_YSCOMP
+1.05V
R325 221/F
H_YSWING
R326 100/F
C609 0.1u/10V
H_YRCOMP
R327 24.9/F
15 mils/10mils
4 H_D#[63:0]
U32A
HOST
H_D#0 F1 H_D#_0
H_D#1 J1 H_D#_1
H_D#2 H1 H_D#_2
H_D#3 J6 H_D#_3
H_D#4 H3 H_D#_4
H_D#5 K2 H_D#_5
H_D#6 G1 H_D#_6
H_D#7 G2 H_D#_7
H_D#8 K9 H_D#_8
H_D#9 K1 H_D#_9
H_D#10 K7 H_D#_10
H_D#11 J8 H_D#_11
H_D#12 H4 H_D#_12
H_D#13 J3 H_D#_13
H_D#14 K11 H_D#_14
H_D#15 G4 H_D#_15
H_D#16 T10 H_D#_16
H_D#17 W11 H_D#_17
H_D#18 T3 H_D#_18
H_D#19 U7 H_D#_19
H_D#20 U9 H_D#_20
H_D#21 U11 H_D#_21
H_D#22 T11 H_D#_22
H_D#23 W9 H_D#_23
H_D#24 T1 H_D#_24
H_D#25 T8 H_D#_25
H_D#26 T4 H_D#_26
H_D#27 W7 H_D#_27
H_D#28 U5 H_D#_28
H_D#29 T9 H_D#_29
H_D#30 W6 H_D#_30
H_D#31 T5 H_D#_31
H_D#32 AB7 H_D#_32
H_D#33 AA9 H_D#_33
H_D#34 W4 H_D#_34
H_D#35 W3 H_D#_35
H_D#36 Y3 H_D#_36
H_D#37 Y7 H_D#_37
H_D#38 W5 H_D#_38
H_D#39 Y10 H_D#_39
H_D#40 AB8 H_D#_40
H_D#41 W2 H_D#_41
H_D#42 AA4 H_D#_42
H_D#43 AA7 H_D#_43
H_D#44 AA2 H_D#_44
H_D#45 AA6 H_D#_45
H_D#46 AA10 H_D#_46
H_D#47 Y8 H_D#_47
H_D#48 AA1 H_D#_48
H_D#49 AB4 H_D#_49
H_D#50 AC9 H_D#_50
H_D#51 AB11 H_D#_51
H_D#52 AC11 H_D#_52
H_D#53 AB3 H_D#_53
H_D#54 AC2 H_D#_54
H_D#55 AD1 H_D#_55
H_D#56 AD9 H_D#_56
H_D#57 AC1 H_D#_57
H_D#58 AD7 H_D#_58
H_D#59 AC6 H_D#_59
H_D#60 AB5 H_D#_60
H_D#61 AD10 H_D#_61
H_D#62 AD4 H_D#_62
H_D#63 AC8 H_D#_63
H_XRCOMP F1 H_XRCOMP
H_XSCOMP F2 H_XSCOMP
H_XSWING E4 H_XSWING
H_YRCOMP Y1 H_YRCOMP
H_YSCOMP U1 H_YSCOMP
H_YSWING W1 H_YSWING
T51 PAD
3 CLK_MCH_BCLK AG2 H_CLKIN
3 CLK_MCH_BCLK# AG1 H_CLKIN#
T50 PAD
Short Stub < 100mils
extract from same point
945PM
H_A#_3 H9 H_A#3
H_A#_4 C9 H_A#4
H_A#_5 E11 H_A#5
H_A#_6 G11 H_A#6
H_A#_7 F11 H_A#7
H_A#_8 G12 H_A#8
H_A#_9 F9 H_A#9
H_A#_10 H11 H_A#10
H_A#_11 J12 H_A#11
H_A#_12 G14 H_A#12
H_A#_13 D9 H_A#13
H_A#_14 J14 H_A#14
H_A#_15 H13 H_A#15
H_A#_16 J15 H_A#16
H_A#_17 F14 H_A#17
H_A#_18 D12 H_A#18
H_A#_19 A11 H_A#19
H_A#_20 C11 H_A#20
H_A#_21 A12 H_A#21
H_A#_22 A13 H_A#22
H_A#_23 E13 H_A#23
H_A#_24 G13 H_A#24
H_A#_25 F12 H_A#25
H_A#_26 B12 H_A#26
H_A#_27 B14 H_A#27
H_A#_28 C12 H_A#28
H_A#_29 A14 H_A#29
H_A#_30 C14 H_A#30
H_A#_31 D14 H_A#31
H_A#[31:3] 4
+1.05V
+1.05V 4,5,7,9,10,12,15,41,43,44
H_ADS# E8 H_ADS# 4
H_ADSTB#_0 B9 H_ADSTB#0 4
H_ADSTB#_1 C13 H_ADSTB#1 4
H_VREF_0 J13
H_BNR# C6 H_BNR# 4
H_BPRI# F6 H_BPRI# 4
H_BREQ#0 C7 H_BREQ#0 4
H_CPURST# B7 H_CPURST# 4
H_DBSY# A7 H_DBSY# 4
H_DEFER# C3 H_DEFER# 4
H_DPWR# J9 H_DPWR# 4
H_DRDY# H8 H_DRDY# 4
H_VREF_1 K13
+1.05V
R48 100/F
H_VREF
C145 0.1u/10V
R43 200/F
H_VREF
C151 0.1u/10V
H_DINV#_0 J7 H_DINV#0
H_DINV#_1 W8 H_DINV#1
H_DINV#_2 U3 H_DINV#2
H_DINV#_3 AB10 H_DINV#3
H_DINV#[3:0] 4
H_DSTBN#_0 K4 H_DSTBN#0
H_DSTBN#_1 T7 H_DSTBN#1
H_DSTBN#_2 Y5 H_DSTBN#2
H_DSTBN#_3 AC4 H_DSTBN#3
H_DSTBN#[3:0] 4
H_DSTBP#_0 K3 H_DSTBP#0
H_DSTBP#_1 T6 H_DSTBP#1
H_DSTBP#_2 AA5 H_DSTBP#2
H_DSTBP#_3 AC5 H_DSTBP#3
H_DSTBP#[3:0] 4
H_HIT# D3 H_HIT# 4
H_HITM# D4 H_HITM# 4
H_LOCK# B3 H_LOCK# 4
H_REQ#_0 D8 H_REQ#0
H_REQ#_1 G8 H_REQ#1
H_REQ#_2 B8 H_REQ#2
H_REQ#_3 F8 H_REQ#3
H_REQ#_4 A8 H_REQ#4
H_REQ#[4:0] 4
H_RS#_0 B4 H_RS#0
H_RS#_1 E6 H_RS#1
H_RS#_2 D6 H_RS#2
H_RS#[2:0] 4
H_SLPCPU# E3 H_CPUSLP# 4,12
H_TRDY# E7 H_TRDY# 4
PROJECT : TW3
Quanta Computer Inc.
Size
Document Number
Calistoga_A(Host)
Rev B1A
Date: Thursday, March 09, 2006
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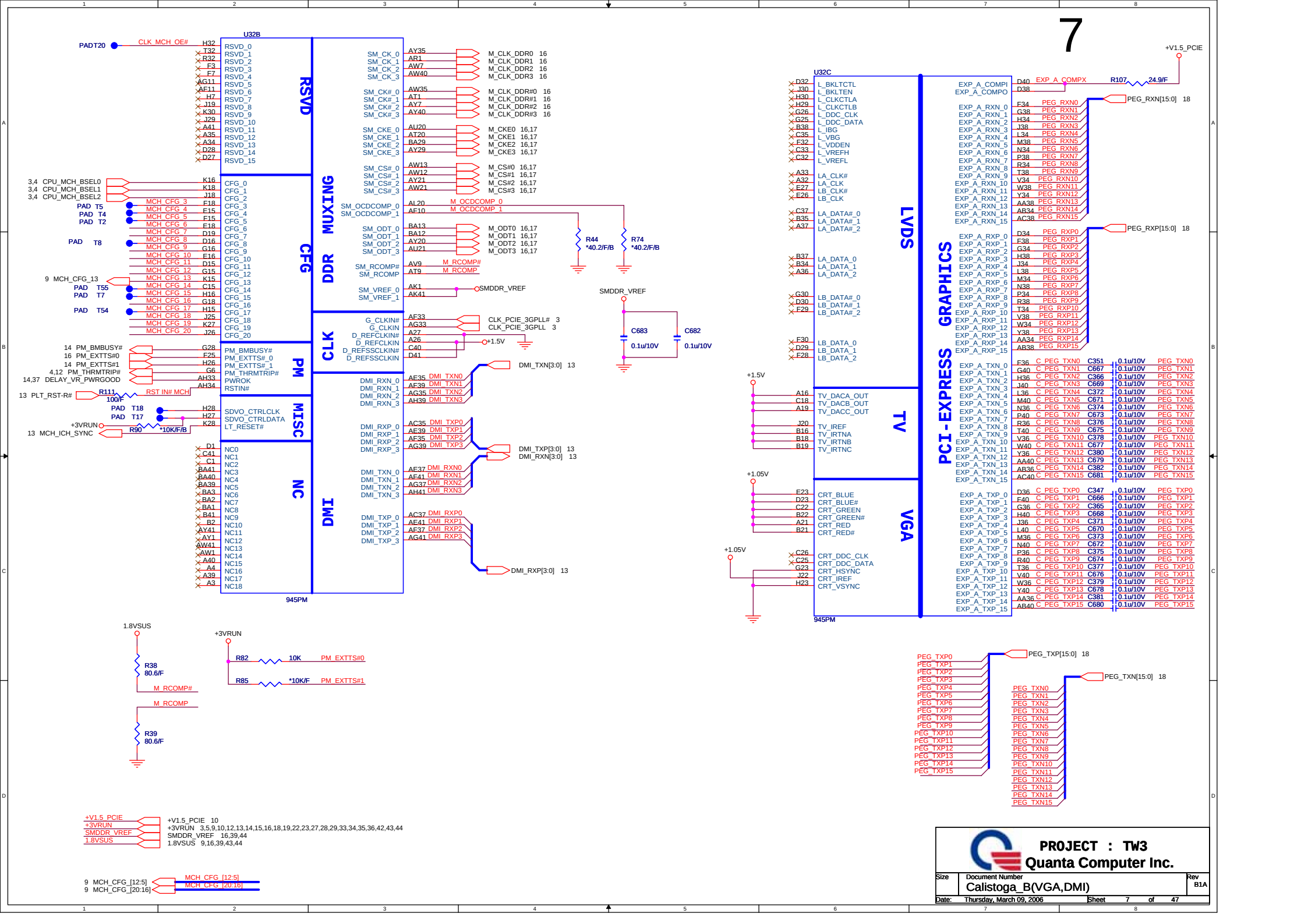
U32B
RSVD
CFG
PM
MISC
NC
DDR MUXING
CLK
DMI
945PM
U32C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
945PM
PADT20
CLK_MCH_OE#
MCH_CFG_3
MCH_CFG_4
MCH_CFG_5
MCH_CFG_6
MCH_CFG_7
MCH_CFG_8
MCH_CFG_9
MCH_CFG_10
MCH_CFG_11
MCH_CFG_12
MCH_CFG_13
MCH_CFG_14
MCH_CFG_15
MCH_CFG_16
MCH_CFG_17
MCH_CFG_18
MCH_CFG_19
MCH_CFG_20
PM_BMBUSY#
PM_EXTTS#0
PM_EXTTS#1
PM_THRMTRIP#
PWROK
RSTIN#
PLT_RST-R#
RST IN# MCH
SDVO_CTRLCLK
SDVO_CTRLDATA
LT_RESET#
MCH_ICH_SYNC
R90
*10K/F/B
R44
*40.2/F/B
R74
*40.2/F/B
SMDDR_VREF
C683
C682
0.1u/10V
+1.5V
+1.05V
DMI_TXN[3:0] 13
DMI_RXN[3:0] 13
DMI_TXP[3:0] 13
DMI_RXP[3:0] 13
+V1.5_PCIE
EXP_A_COMPX
R107
24.9/F
PEG_RXN[15:0] 18
PEG_RXP[15:0] 18
PEG_TXP[15:0] 18
PEG_TXN[15:0] 18
1.8VSUS
+3VRUN
R38
80.6/F
R39
80.6/F
R82
10K
PM_EXTTS#0
R85
*10K/F
PM_EXTTS#1
M_RCOMP#
M_RCOMP
+V1.5_PCIE 10
+3VRUN 3,5,9,10,12,13,14,15,16,18,19,22,23,27,28,29,33,34,35,36,42,43,44
SMDDR_VREF 16,39,44
1.8VSUS 9,16,39,43,44
MCH_CFG_[12:5]
MCH_CFG_[20:16]
PROJECT : TW3
Quanta Computer Inc.
Size
Document Number
Calistoga_B(VGA,DMI)
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B1A
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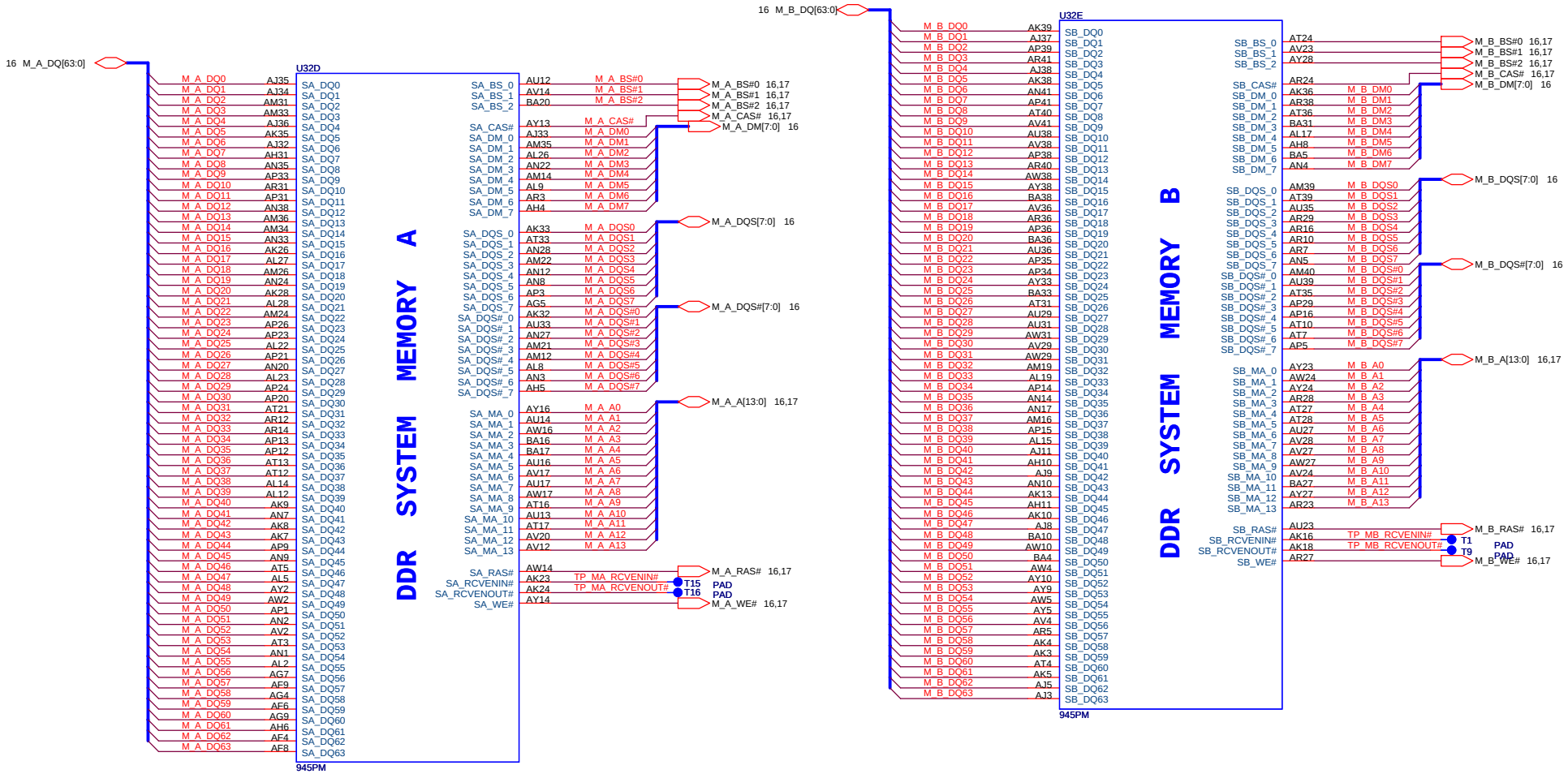

PROJECT : TW3
Quanta Computer Inc.

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	Calistoga_C(DDR)	B1A

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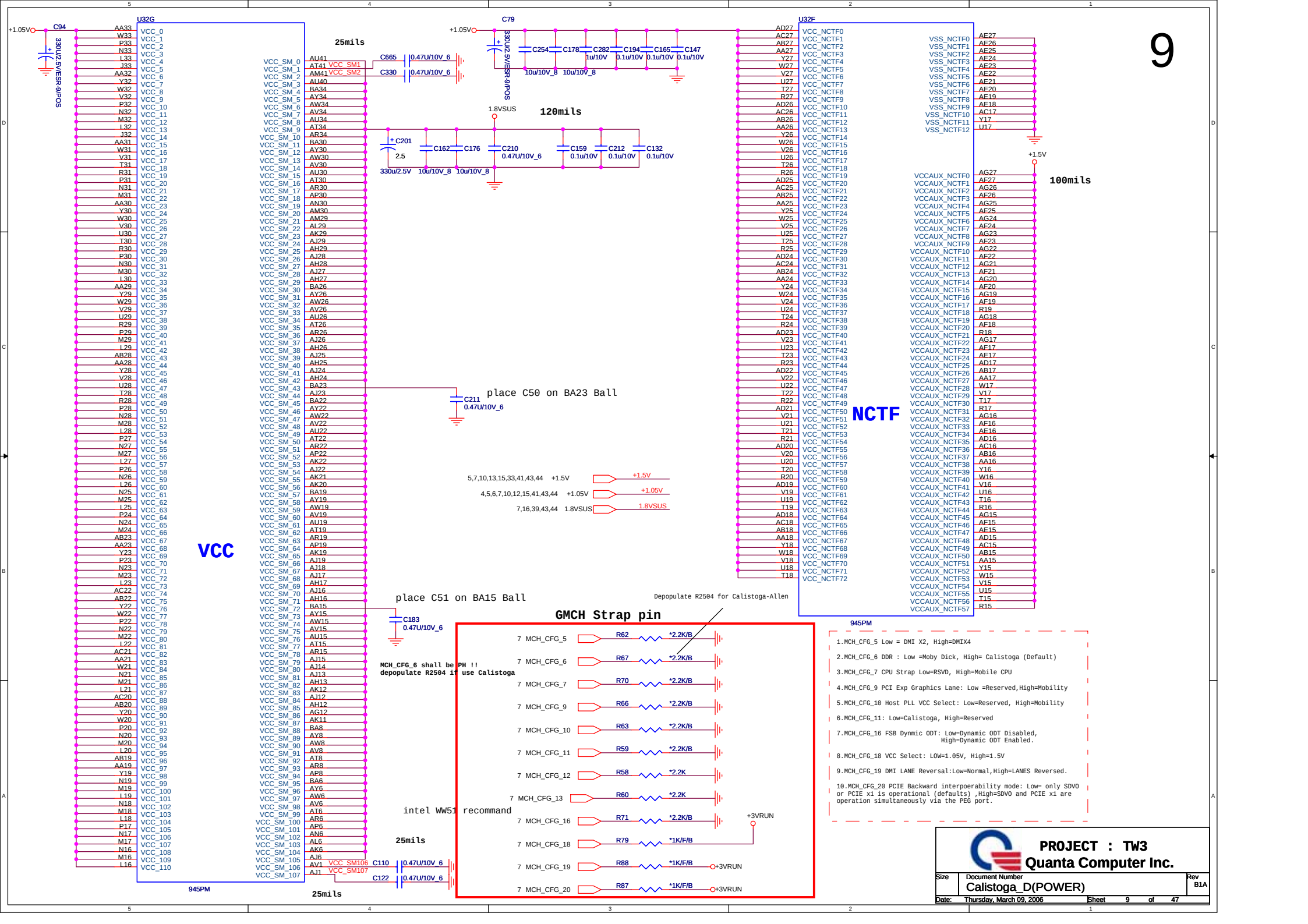
U32G
VCC
945PM
U32F
NCTF
945PM
C94
330U/2.5V/ESR-9/POS
C79
330U/2.5V/ESR-9/POS
C254
C178
C282
C194
C165
C147
10u/10V_8
10u/10V_8
1u/10V
0.1u/10V
0.1u/10V
0.1u/10V
+1.05V
1.8VSUS
120mils
C201
330u/2.5V
2.5
C162
C176
C210
0.47U/10V_6
C159
0.1u/10V
C212
0.1u/10V
C132
0.1u/10V
10u/10V_8
10u/10V_8
25mils
C665
C330
0.47U/10V_6
0.47U/10V_6
AU41
AT41 VCC_SM1
AM41 VCC_SM2
AU40
BA34
AY34
AW34
AV34
AU34
AT34
AR34
BA30
AY30
AW30
AV30
AU30
AT30
AR30
AP30
AN30
AM30
AM29
AL29
AK29
AJ29
AH29
AJ28
AH28
AH27
BA26
AY26
AW26
AV26
AU26
AT26
AR26
AJ26
AH26
AJ25
AH25
AJ24
AH24
BA23
AJ23
BA22
AY22
AW22
AV22
AU22
AT22
AR22
AP22
AK22
AJ22
AK21
AK20
BA19
AY19
AW19
AV19
AU19
AT19
AR19
AP19
AK19
AJ19
AJ18
AJ17
AH17
AJ16
AH16
BA15
AY15
AW15
AV15
AU15
AT15
AR15
AJ15
AJ14
AJ13
AH13
AK12
AJ12
AH12
AG12
AK11
BA8
AY8
AW8
AV8
AT8
AR8
AP8
BA6
AY6
AW6
AV6
AT6
AR6
AP6
AN6
AL6
AK6
AJ6
AV1 VCC_SM106
AJ1 VCC_SM107
C110
C122
0.47U/10V_6
0.47U/10V_6
25mils
C211
0.47U/10V_6
place C50 on BA23 Ball
place C51 on BA15 Ball
C183
0.47U/10V_6
MCH_CFG_6 shall be PH !!
depopulate R2504 if use Calistoga
5,7,10,13,15,33,41,43,44 +1.5V
4,5,6,7,10,12,15,41,43,44 +1.05V
7,16,39,43,44 1.8VSUS
+1.5V
+1.05V
1.8VSUS
GMCH Strap pin
Depopulate R2504 for Calistoga-Allen
7 MCH_CFG_5 R62 *2.2K/B
7 MCH_CFG_6 R67 *2.2K/B
7 MCH_CFG_7 R70 *2.2K/B
7 MCH_CFG_9 R66 *2.2K/B
7 MCH_CFG_10 R63 *2.2K/B
7 MCH_CFG_11 R59 *2.2K/B
7 MCH_CFG_12 R58 *2.2K
7 MCH_CFG_13 R60 *2.2K
7 MCH_CFG_16 R71 *2.2K/B
7 MCH_CFG_18 R79 *1K/F/B
7 MCH_CFG_19 R88 *1K/F/B
7 MCH_CFG_20 R87 *1K/F/B
+3VRUN
+3VRUN
+3VRUN
intel WW51 recommand
1.MCH_CFG_5 Low = DMI X2, High=DMIX4
2.MCH_CFG_6 DDR : Low =Moby Dick, High= Calistoga (Default)
3.MCH_CFG_7 CPU Strap Low=RSVD, High=Mobile CPU
4.MCH_CFG_9 PCI Exp Graphics Lane: Low =Reserved,High=Mobility
5.MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility
6.MCH_CFG_11: Low=Calistoga, High=Reserved
7.MCH_CFG_16 FSB Dynmic ODT: Low=Dynamic ODT Disabled, High=Dynamic ODT Enabled.
8.MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V
9.MCH_CFG_19 DMI LANE Reversal:Low=Normal,High=LANES Reversed.
10.MCH_CFG_20 PCIE Backward interpoerability mode: Low= only SDVO or PCIE x1 is operational (defaults) ,High=SDVO and PCIE x1 are operation simultaneously via the PEG port.
+1.5V
100mils
PROJECT : TW3
Quanta Computer Inc.
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Calistoga_D(POWER)
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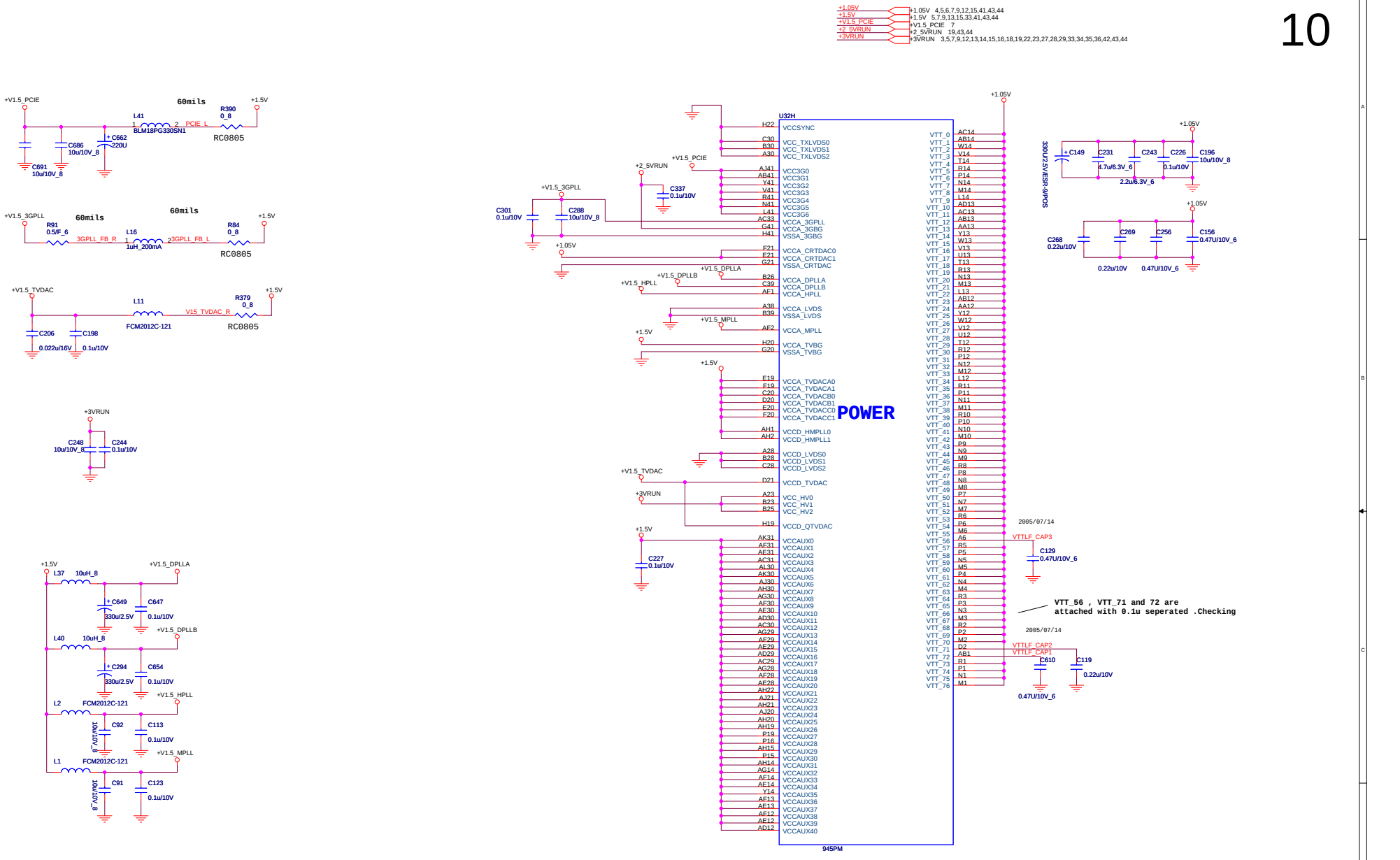

	PROJECT : TW3 Quanta Computer Inc.		
Size	Document Number Calistoga_E(POWER2)		Rev B1A
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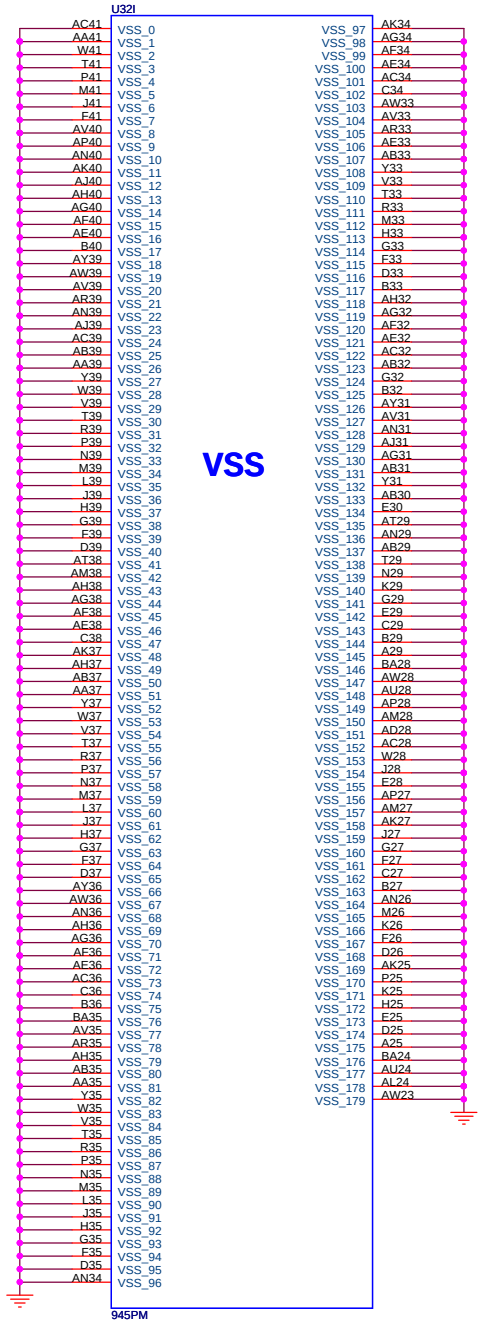

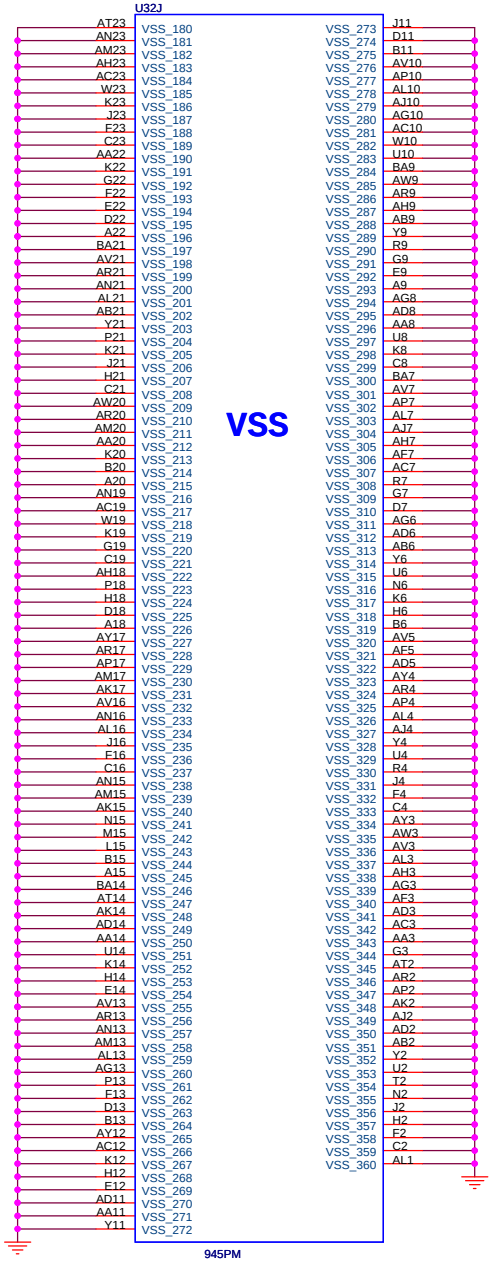

PROJECT : TW3		
Quanta Computer Inc.		
Size	Document Number	Rev
	Calistoga_F(VSS, NCTF)	B1A
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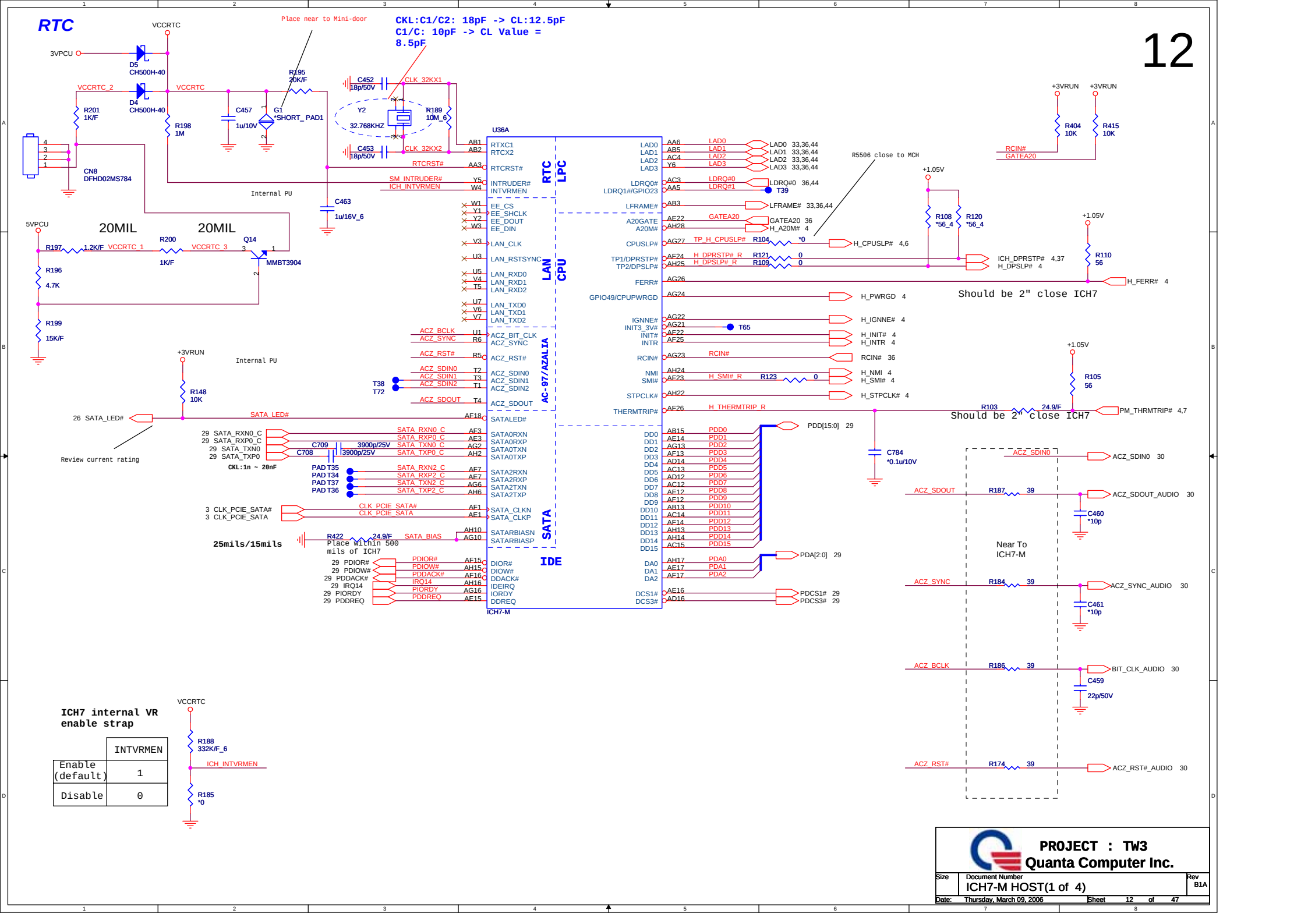
RTC
12
Place near to Mini-door
CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF
VCCRTC
3VPCU
D5 CH500H-40
D4 CH500H-40
VCCRTC_2
R195 20K/F
C452 18p/50V
CLK_32KX1
C453 18p/50V
CLK_32KX2
Y2 32.768KHZ
R189 10M_6
R201 1K/F
R198 1M
C457 1u/10V
G1 *SHORT_ PAD1
CN8 DFHD02MS784
Internal PU
C463 1u/16V_6
U36A
RTXC1
RTXC2
RTCRST#
INTRUDER#
INTVRMEN
SM_INTRUDER#
ICH_INTVRMEN
RTC
LPC
EE_CS
EE_SHCLK
EE_DOUT
EE_DIN
LAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
LAN
CPU
ACZ_BCLK
ACZ_SYNC
ACZ_RST#
ACZ_SDIN0
ACZ_SDIN1
ACZ_SDIN2
ACZ_SDOUT
ACZ_BIT_CLK
AC-97/AZALIA
T38
T72
5VPCU
20MIL
20MIL
R197 1.2K/F
VCCRTC_1
R200 1K/F
VCCRTC_3
Q14 MMBT3904
R196 4.7K
R199 15K/F
+3VRUN
R148 10K
Internal PU
26 SATA_LED#
SATA_LED#
Review current rating
29 SATA_RXN0_C
29 SATA_RXP0_C
29 SATA_TXN0
29 SATA_TXP0
C709 3900p/25V
C708 3900p/25V
CKL:1n ~ 20nF
SATA_RXN0_C
SATA_RXP0_C
SATA_TXN0_C
SATA_TXP0_C
PAD T35
PAD T34
PAD T37
PAD T36
SATA_RXN2_C
SATA_RXP2_C
SATA_TXN2_C
SATA_TXP2_C
3 CLK_PCIE_SATA#
3 CLK_PCIE_SATA
CLK_PCIE_SATA#
CLK_PCIE_SATA
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATALED#
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATA
25mils/15mils
R422 24.9/F
SATA_BIAS
Place within 500 mils of ICH7
SATARBIASN
SATARBIASP
29 PDIOR#
29 PDIOW#
29 PDDACK#
29 IRQ14
29 PIORDY
29 PDDREQ
PDIOR#
PDIOW#
PDDACK#
IRQ14
PIORDY
PDDREQ
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
IDE
ICH7-M
LAD0
LAD1
LAD2
LAD3
LDRQ0#
LDRQ1#/GPIO23
LFRAME#
A20GATE
A20M#
CPUSLP#
TP1/DPRSTP#
TP2/DPSLP#
FERR#
GPIO49/CPUPWRGD
IGNNE#
INIT3_3V#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THERMTRIP#
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
LAD0 33,36,44
LAD1 33,36,44
LAD2 33,36,44
LAD3 33,36,44
LDRQ#0 36,44
LDRQ#1
T39
LFRAME# 33,36,44
GATEA20
GATEA20 36
H_A20M# 4
TP_H_CPUSLP#
R104 *0
H_CPUSLP# 4,6
H_DPRSTP# R
H_DPSLP# R
R121 0
R109 0
R5506 close to MCH
+1.05V
R108 *56_4
R120 *56_4
ICH_DPRSTP# 4,37
H_DPSLP# 4
+1.05V
R110 56
H_FERR# 4
Should be 2" close ICH7
H_PWRGD 4
T65
H_IGNNE# 4
H_INIT# 4
H_INTR 4
RCIN#
RCIN# 36
H_SMI# R
R123 0
H_NMI 4
H_SMI# 4
H_STPCLK# 4
H_THERMTRIP_R
R103 24.9/F
PM_THRMTRIP# 4,7
Should be 2" close ICH7
+1.05V
R105 56
C784 *0.1u/10V
PDD[15:0] 29
PDA[2:0] 29
PDCS1# 29
PDCS3# 29
+3VRUN
+3VRUN
R404 10K
R415 10K
RCIN#
GATEA20
ACZ_SDIN0
ACZ_SDOUT
R187 39
ACZ_SDOUT_AUDIO 30
C460 *10p
Near To ICH7-M
ACZ_SYNC
R184 39
ACZ_SYNC_AUDIO 30
C461 *10p
ACZ_BCLK
R186 39
BIT_CLK_AUDIO 30
C459 22p/50V
ACZ_RST#
R174 39
ACZ_RST#_AUDIO 30
ICH7 internal VR enable strap
INTVRMEN
Enable (default) 1
Disable 0
VCCRTC
R188 332K/F_6
ICH_INTVRMEN
R185 *0
PROJECT : TW3
Quanta Computer Inc.
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ICH7-M HOST(1 of 4)
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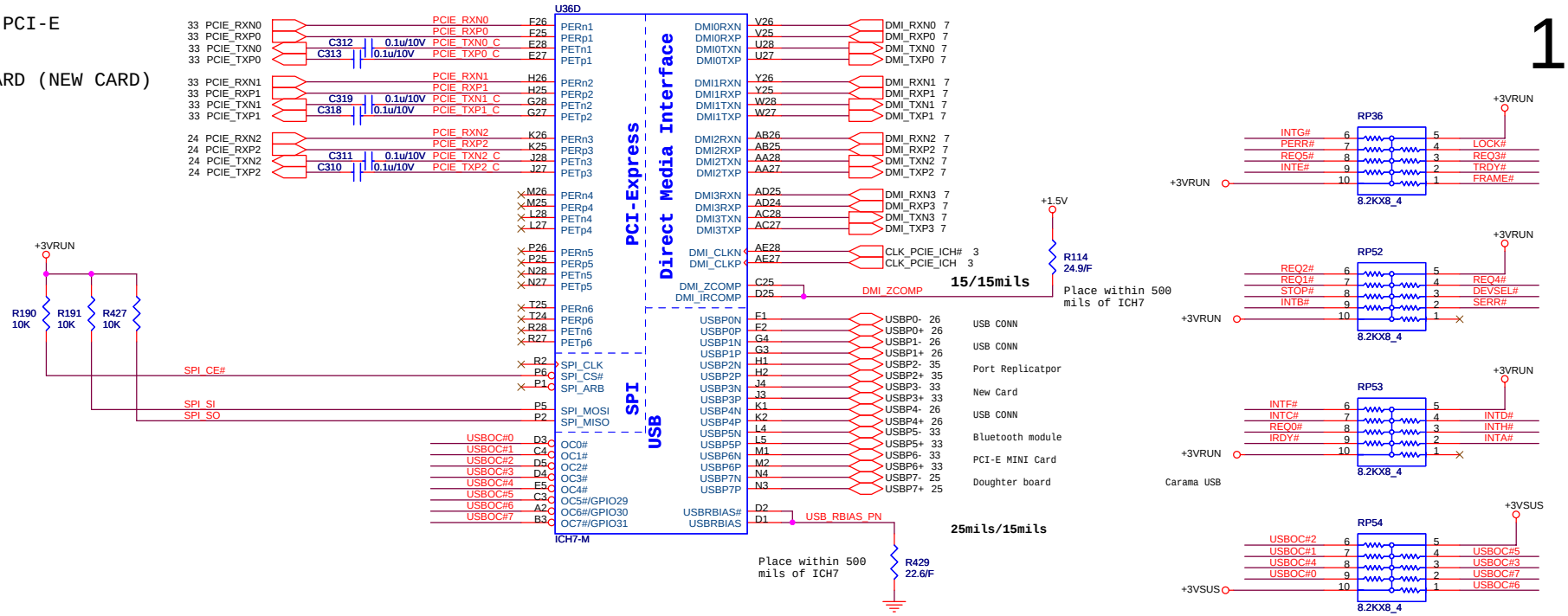
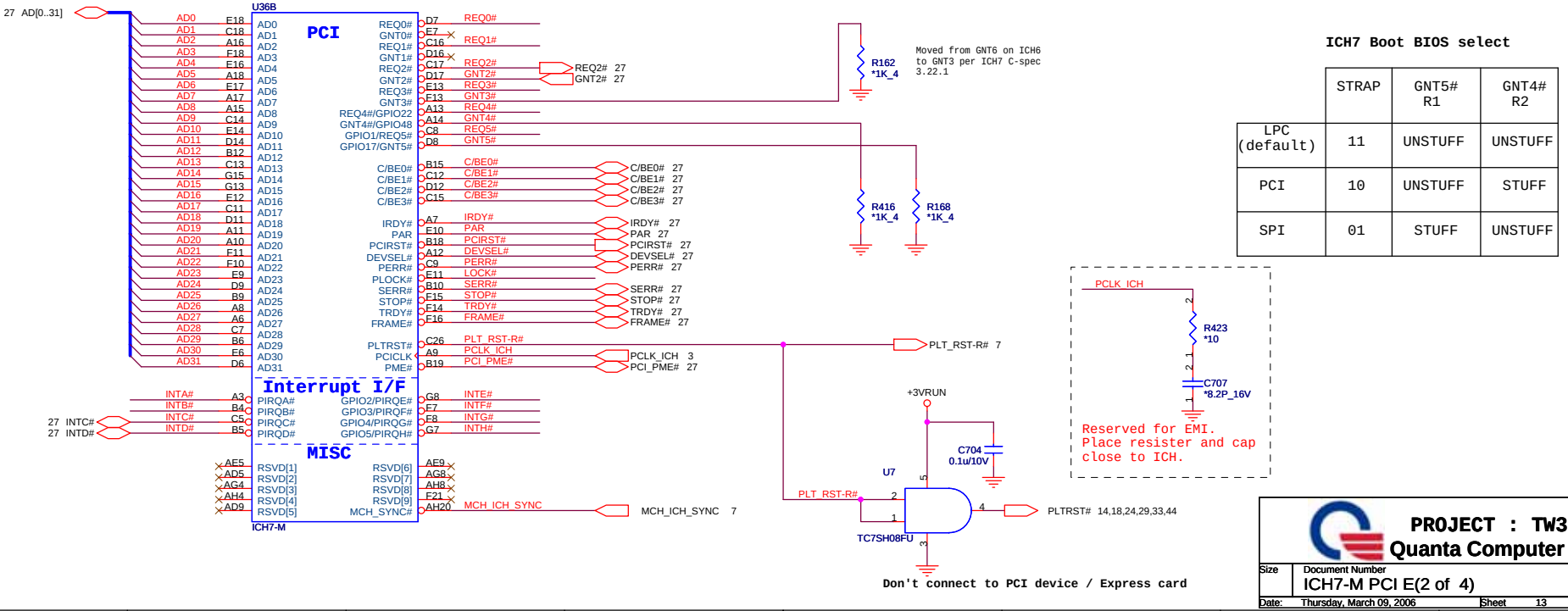
MINI CARD PCI-E

EXPRESS CARD (NEW CARD)





ICH7 Boot BIOS select

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

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Quanta Computer Inc.

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R376

No stuff-->boot
Stuff-->No boot

+3V_S5
PCLK_SMB R124 2.2K
PDAT_SMB R128 2.2K
PCIE_WAKE# R156 680

+3V_S5
RI# R389 10K
SMB_LINK_ALERT# R391 10K
SMLINK0 R392 10K
SMLINK1 R394 10K
EXTSMI# R R153 *10K
WAKE_SCI# R R95 10K
SMBALERT# R395 10K

+3V_S5
SWI# R409 10K
DNBSWON# R117 10K
SYS_RST# R396 10K
PM_BATLOW# R401 8.2K/F

+3VRUN
SYS_RST# R399 *10K
CLKRUN# R420 8.2K/F
SERIRQ R412 8.2K/F
RUNTIME_SCI# R R140 10K

SYS_RST is suspend rail

RSMRST# R424 10K

+3VRUN
R411 *1K_4
30 ACZ_SPKR

U36C
ICH7-M

SMB
SMBCLK C22
SMBDATA B22
LINKALERT# A26
SMLINK0 B25
SMLINK1 A25
RI# A28
SPKR A19
SUS_STAT# A27
SYS_RST# A22
GPIO0/BM_BUSY# AB18
GPIO11/SMBALERT# B23
GPIO18/STPPCI# AC20
GPIO20/STPCPU# AE21
GPIO26 A21
GPIO27 B21
GPIO28 E23
GPIO32/CLKRUN# AG18
GPIO33/AZ_DOCK_EN# AC19
GPIO34/AZ_DOCK_RST# U2
WAKE# F20
SERIRQ AH21
THRM# AE20
VRMPWRGD AD22
GPIO6 AC21
GPIO7 AC18
GPIO8 F21

SATA GPIO
GPIO21/SATA0GP AE19 BOARD_ID1
GPIO19/SATA1GP AH18 BOARD_ID0
GPIO36/SATA2GP AH19 BOARD_ID3
GPIO37/SATA3GP AE19 BOARD_ID4

Clocks
CLK14 AC1 14M_ICH
CLK48 B2 CLKUSB_48
SUSCLK C20 ICH_SUSCLK

Power MGT
SLP_S3# B24 R115 100/F SUSB# 36
SLP_S4# D23 R122 100/F SUSC# 36
SLP_S5# F22 T21
PWROK AA4 ICH_PWROK
GPIO16/DPRSLPVR AC22 PM_DPRSLPVR_R R113 100/F
TP0/BATLOW# C21 PM_BATLOW# R R400 100/F
PWRBTN# C23 DNBSWON# R158 100K DNBSWON# 36
LAN_RST# C19 R98 0 PLTRST# 13,18,24,29,33,44
RSMRST# Y4 PM_RSMRST# R R425 100/F RSMRST#

GPIO
GPIO9 E20 SWI#
GPIO10 A20 T67
GPIO12 F19 T27
GPIO13 E19 WAKE_SCI# R
GPIO14 R4 T19
GPIO15 E22 T40
GPIO24 R3 T25
GPIO25 D20 T29
GPIO35 AD21
GPIO38 AD20 GPIO38
GPIO39 AE20 T30

3,33 PCLK_SMB
3,33 PDAT_SMB
27 RI#
27,44 SUS_STAT#
4 SYS_RST#
7 PM_BMBUSY#
T24
No ASF support
3 PM_STPPCI#
3 PM_STPCPU#
T64
T66
T22
27,36,44 CLKRUN#
29 ICH_GPO33
24,33 PCIE_WAKE#
27,36,44 SERIRQ
5 THERM_ALERT#
VR_PWRGD_CK410
T28
36 SCI#
36 KBSMI#

+3VRUN
R126 *10K
R129 *10K
R418 8.2K/F

R166 0
R130 0
R127 0
R141 0
R143 0
RUNTIME_SCI# R
EXTSMI# R

+3VRUN
U14
3,37 CLK_EN#
VR_PWRGD_CK410
NL17SZ14DFT2G

Note: External pull-up 3V

R116 0
R112 *100K
PM_EXTTS#1 7
PM_DPRSLPVR 37
PM_BATLOW# 36
CKL :100Kohm PD

GPIO25 /Suspend rail is a HW strap , don't pull down .

3/9 Change to NI
PWM require 6.9K
Change to 6.8K
R193 *6.8K
+3VRUN
+3VSUS
C451 0.047u/10V
U15
TC7SH08FU
7,37 DELAY_VR_PWRGOOD
36 PWROK
R182 100K
ICH_PWROK
R183 10K

Level is incorrect !!

Place these close to ICH7.
CLKUSB_48
14M_ICH
R428 *10
C712 *4.7P_50V
R372 *10_NC
C637 *4.7P_50V_NC

+3VRUN
R421 *10K_4
BOARD_ID0
R167 10K
R147 *10K
BOARD_ID1
R139 10K
R371 *10K_NC
BOARD_ID2
R367 10K
R136 *10K
BOARD_ID3
R137 10K
R368 10K
BOARD_ID4
R366 *10K

+3VRUN
R482 10K
GPIO38
R483 *10K

GPIO38	Function
High	CRT
Low	DVI

Board ID	Function
ID [1:0]	00: TW3 01: DW1
ID2	0: SATA HDD 1: PATA HDD
ID3	Reserve
ID4	0: No docking. 1: w/ docking

PROJECT : TW3
Quanta Computer Inc.

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	ICH7-M GPIO(3 of 4)	B1A
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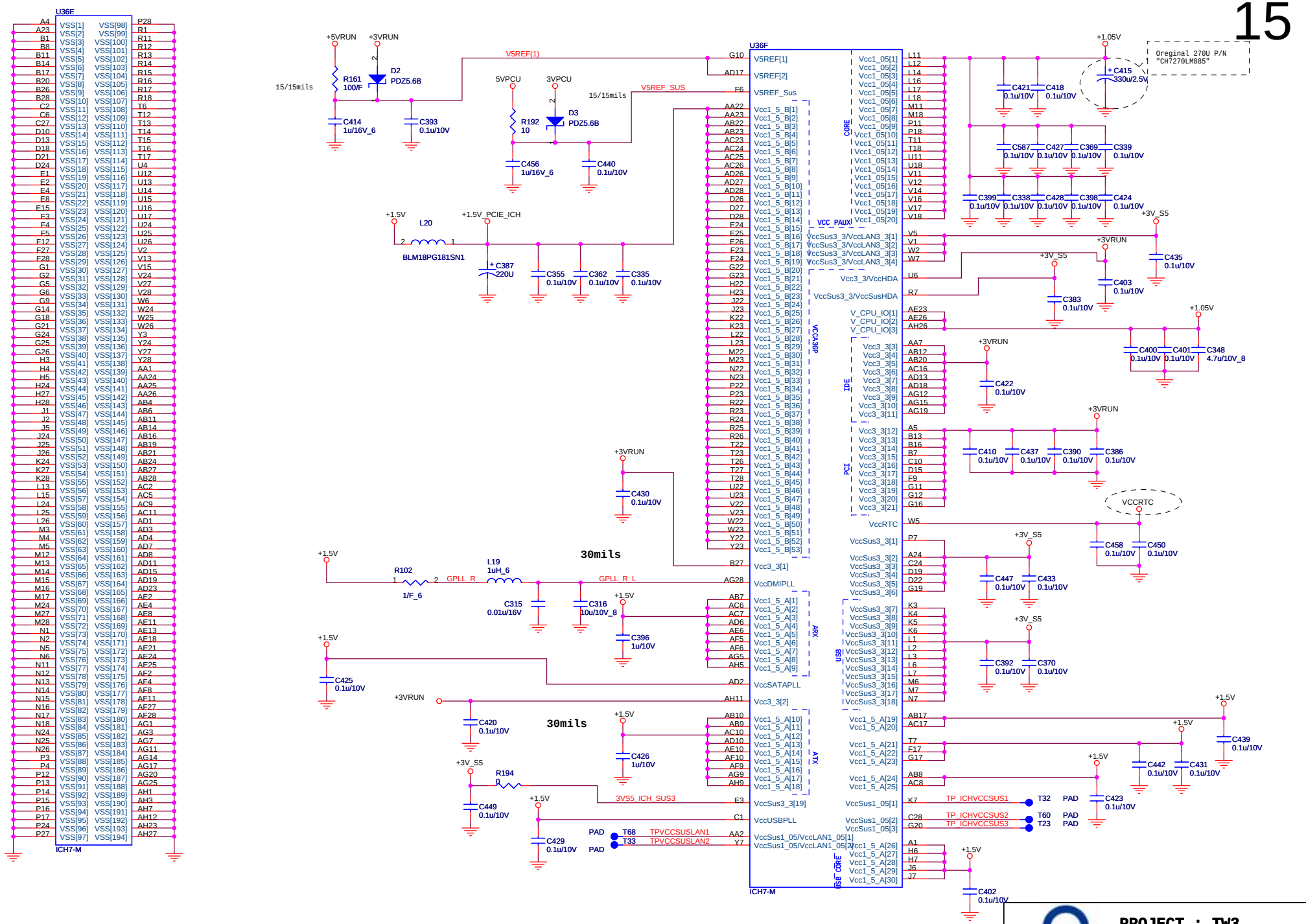

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M POWER(4 of 4)	B1A

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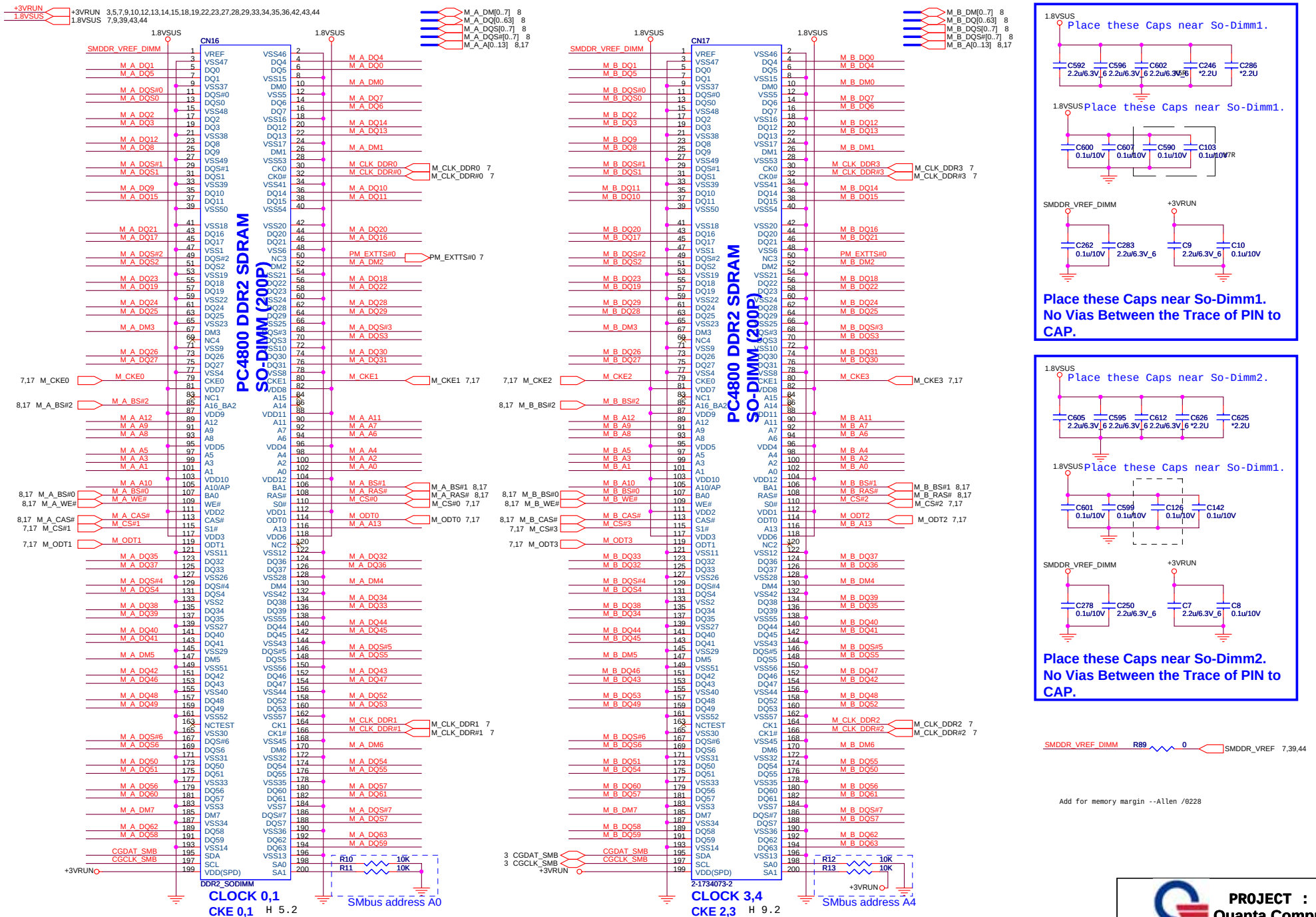
+3VRUN
1.8VSUS
+3VRUN 3,5,7,9,10,12,13,14,15,18,19,22,23,27,28,29,33,34,35,36,42,43,44
1.8VSUS 7,9,39,43,44
M_A_DM[0..7] 8
M_A_DQ[0..63] 8
M_A_DQS[0..7] 8
M_A_DQS#[0..7] 8
M_A_A[0..13] 8,17
CN16
SMDDR_VREF_DIMM
PC4800 DDR2 SDRAM
SO-DIMM (200P)
DDR2_SODIMM
M_CLK_DDR0 7
M_CLK_DDR#0 7
PM_EXTTS#0 7
M_CLK_DDR1 7
M_CLK_DDR#1 7
7,17 M_CKE0
M_CKE1 7,17
8,17 M_A_BS#2
8,17 M_A_BS#0
8,17 M_A_WE#
8,17 M_A_CAS#
7,17 M_CS#1
7,17 M_ODT1
M_A_BS#1 8,17
M_A_RAS# 8,17
M_CS#0 7,17
M_ODT0 7,17
CGDAT_SMB
CGCLK_SMB
+3VRUN
R10 10K
R11 10K
CLOCK 0,1
CKE 0,1
H 5.2
SMbus address A0
M_B_DM[0..7] 8
M_B_DQ[0..63] 8
M_B_DQS[0..7] 8
M_B_DQS#[0..7] 8
M_B_A[0..13] 8,17
CN17
PC4800 DDR2 SDRAM
SO-DIMM (200P)
2-1734073-2
M_CLK_DDR3 7
M_CLK_DDR#3 7
M_CLK_DDR2 7
M_CLK_DDR#2 7
7,17 M_CKE2
M_CKE3 7,17
8,17 M_B_BS#2
8,17 M_B_BS#0
8,17 M_B_WE#
8,17 M_B_CAS#
7,17 M_CS#3
7,17 M_ODT3
M_B_BS#1 8,17
M_B_RAS# 8,17
M_CS#2 7,17
M_ODT2 7,17
3 CGDAT_SMB
3 CGCLK_SMB
+3VRUN
R12 10K
R13 10K
CLOCK 3,4
CKE 2,3
H 9.2
SMbus address A4
1.8VSUS
Place these Caps near So-Dimm1.
C592 2.2u/6.3V_6
C596 2.2u/6.3V_6
C602 2.2u/6.3V_6
C246 *2.2U
C286 *2.2U
C600 0.1u/10V
C607 0.1u/10V
C590 0.1u/10V
C103 0.1u/10V
SMDDR_VREF_DIMM
+3VRUN
C262 0.1u/10V
C283 2.2u/6.3V_6
C9 2.2u/6.3V_6
C10 0.1u/10V
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.
Place these Caps near So-Dimm2.
C605 2.2u/6.3V_6
C595 2.2u/6.3V_6
C612 2.2u/6.3V_6
C626 *2.2U
C625 *2.2U
C601 0.1u/10V
C599 0.1u/10V
C126 0.1u/10V
C142 0.1u/10V
C278 0.1u/10V
C250 2.2u/6.3V_6
C7 2.2u/6.3V_6
C8 0.1u/10V
Place these Caps near So-Dimm2.
No Vias Between the Trace of PIN to CAP.
SMDDR_VREF_DIMM
R89 0
SMDDR_VREF 7,39,44
Add for memory margin --Allen /0228
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Quanta Computer Inc.
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DDRII SO-DIMM(200P)
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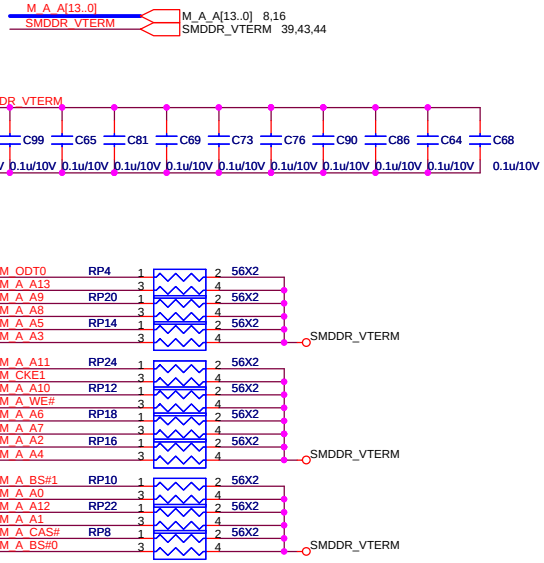
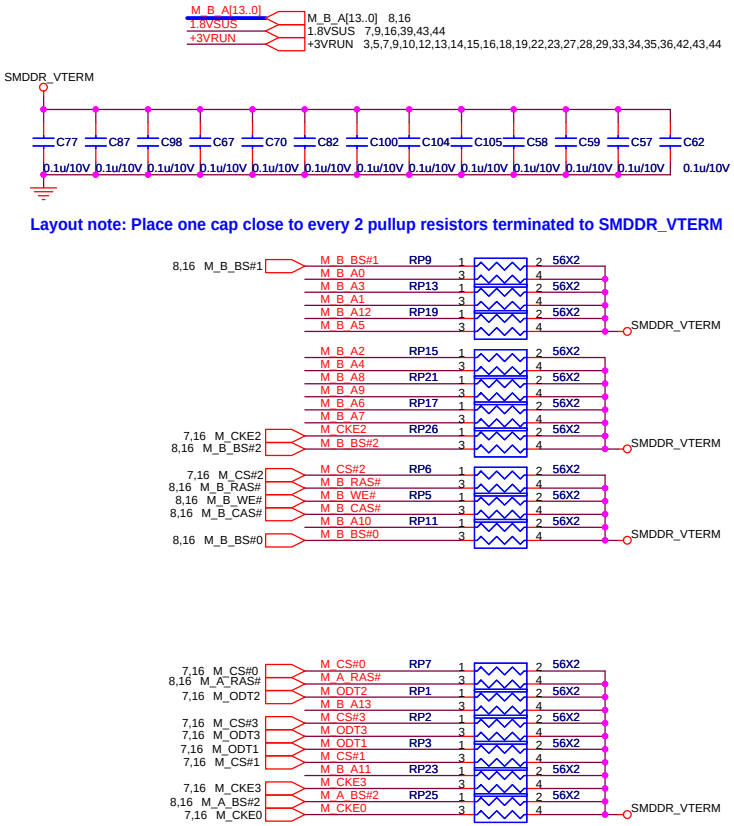
DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL



DDRII B CHANNEL



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Quanta Computer Inc.		
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7 PEG_RXP[15:0]
7 PEG_RXN[15:0]
7 PEG_TXP[15:0]
7 PEG_TXN[15:0]

U31A
PART 1 OF 4
PCI-EXPRESS INTERFACE
Clock
PCIE Power
G72M

PEG_TXP0 AF1 PEX_RX0P
PEG_TXN0 AG2 PEX_RX0N
PEG_TXP1 AG3 PEX_RX1P
PEG_TXN1 AG4 PEX_RX1N
PEG_TXP2 AF4 PEX_RX2P
PEG_TXN2 AF5 PEX_RX2N
PEG_TXP3 AG6 PEX_RX3P
PEG_TXN3 AG7 PEX_RX3N
PEG_TXP4 AF7 PEX_RX4P
PEG_TXN4 AF8 PEX_RX4N
PEG_TXP5 AG9 PEX_RX5P
PEG_TXN5 AG10 PEX_RX5N
PEG_TXP6 AF10 PEX_RX6P
PEG_TXN6 AF11 PEX_RX6N
PEG_TXP7 AG12 PEX_RX7P
PEG_TXN7 AG13 PEX_RX7N
PEG_TXP8 AG15 PEX_RX8P
PEG_TXN8 AG16 PEX_RX8N
PEG_TXP9 AF16 PEX_RX9P
PEG_TXN9 AF17 PEX_RX9N
PEG_TXP10 AG18 PEX_RX10P
PEG_TXN10 AG19 PEX_RX10N
PEG_TXP11 AF19 PEX_RX11P
PEG_TXN11 AF20 PEX_RX11N
PEG_TXP12 AG21 PEX_RX12P
PEG_TXN12 AG22 PEX_RX12N
PEG_TXP13 AF22 PEX_RX13P
PEG_TXN13 AF23 PEX_RX13N
PEG_TXP14 AG24 PEX_RX14P
PEG_TXN14 AG25 PEX_RX14N
PEG_TXP15 AG26 PEX_RX15P
PEG_TXN15 AF27 PEX_RX15N

PEX_TX0P AD5 V_GMCHEXP_RXP0
PEX_TX0N AD6 V_GMCHEXP_RXN0
PEX_TX1P AE6 V_GMCHEXP_RXP1
PEX_TX1N AE7 V_GMCHEXP_RXN1
PEX_TX2P AD7 V_GMCHEXP_RXP2
PEX_TX2N AC7 V_GMCHEXP_RXN2
PEX_TX3P AE9 V_GMCHEXP_RXP3
PEX_TX3N AE10 V_GMCHEXP_RXN3
PEX_TX4P AD10 V_GMCHEXP_RXP4
PEX_TX4N AC10 V_GMCHEXP_RXN4
PEX_TX5P AE12 V_GMCHEXP_RXP5
PEX_TX5N AE13 V_GMCHEXP_RXN5
PEX_TX6P AD13 V_GMCHEXP_RXP6
PEX_TX6N AC13 V_GMCHEXP_RXN6
PEX_TX7P AC15 V_GMCHEXP_RXP7
PEX_TX7N AD15 V_GMCHEXP_RXN7
PEX_TX8P AE15 V_GMCHEXP_RXP8
PEX_TX8N AE16 V_GMCHEXP_RXN8
PEX_TX9P AC18 V_GMCHEXP_RXP9
PEX_TX9N AD18 V_GMCHEXP_RXN9
PEX_TX10P AE18 V_GMCHEXP_RXP10
PEX_TX10N AE19 V_GMCHEXP_RXN10
PEX_TX11P AC21 V_GMCHEXP_RXP11
PEX_TX11N AD21 V_GMCHEXP_RXN11
PEX_TX12P AE21 V_GMCHEXP_RXP12
PEX_TX12N AE22 V_GMCHEXP_RXN12
PEX_TX13P AD22 V_GMCHEXP_RXP13
PEX_TX13N AD23 V_GMCHEXP_RXN13
PEX_TX14P AE25 V_GMCHEXP_RXP14
PEX_TX14N AE25 V_GMCHEXP_RXN14
PEX_TX15P AE24 V_GMCHEXP_RXP15
PEX_TX15N AD24 V_GMCHEXP_RXN15

3 CLK_PCIE_VGA AE3 PEX_REFCLK
3 CLK_PCIE_VGA# AE4 PEX_REFCLK#
PEX_TSTCLK_OUT AF13 PEX_TSTCLK
PEX_TSTCLK_OUT# AF14 PEX_TSTCLK#
PEX_RST# AC6

J9 VDD_01
M9 VDD_02
N9 VDD_03
R9 VDD_04
T9 VDD_05
J10 VDD_06
J11 VDD_07
M11 VDD_08
N11 VDD_09
R11 VDD_10
T11 VDD_11
L12 VDD_12
M12 VDD_13
T12 VDD_14
U12 VDD_15
L13 VDD_16
M13 VDD_17
T13 VDD_18
U13 VDD_19
W13 VDD_20
M14 VDD_21
T14 VDD_22
L15 VDD_23
M15 VDD_24
T15 VDD_25
U15 VDD_26
W15 VDD_27
L16 VDD_28
M16 VDD_29
T16 VDD_30
U16 VDD_31
W16 VDD_32
M17 VDD_33
N17 VDD_34
R17 VDD_35
T17 VDD_36

PEX_IOVDD_01 AB10
PEX_IOVDD_02 AB11
PEX_IOVDD_03 AB14
PEX_IOVDD_04 AB15
PEX_IOVDD_05 W17
PEX_IOVDD_06 W18
PEX_IOVDD_07 AB20
PEX_IOVDD_08 AB21

PEX_IOVDDQ_01 AA4
PEX_IOVDDQ_02 AB5
PEX_IOVDDQ_03 AB6
PEX_IOVDDQ_04 AB7
PEX_IOVDDQ_05 AB8
PEX_IOVDDQ_06 AB9
PEX_IOVDDQ_07 AC9
PEX_IOVDDQ_08 AC11
PEX_IOVDDQ_09 AB12
PEX_IOVDDQ_10 AC12
PEX_IOVDDQ_11 AB13
PEX_IOVDDQ_12 AB16
PEX_IOVDDQ_13 AC16
PEX_IOVDDQ_14 AB17
PEX_IOVDDQ_15 AC17
PEX_IOVDDQ_16 AB18
PEX_IOVDDQ_17 AB19
PEX_IOVDDQ_18 AC19
PEX_IOVDDQ_19 AC20

VDD_LP_01 W9
VDD_LP_02 W10
VDD_LP_03 W11
VDD_LP_04 W12

VDD33_01 J12
VDD33_02 F13
VDD33_03 J13
VDD33_04 F14
VDD33_05 J15
VDD33_06 J16

NC_01 D12
NC_02 E12
NC_03 F12
NC_04 C13

PEX_PLL_AVDD Y6 PEX_PLLAVDD
PEX_PLL_DVDD AA5 PEX_PLLDVDD
AA6 PEX_PLLGND

C304 0.1u/10V PEG_RXP0 V_GMCHEXP_RXP0
C656 0.1u/10V PEG_RXN0 V_GMCHEXP_RXN0
C314 0.1u/10V PEG_RXP1 V_GMCHEXP_RXP1
C664 0.1u/10V PEG_RXN1 V_GMCHEXP_RXN1
C326 0.1u/10V PEG_RXP2 V_GMCHEXP_RXP2
C684 0.1u/10V PEG_RXN2 V_GMCHEXP_RXN2
C368 0.1u/10V PEG_RXP3 V_GMCHEXP_RXP3
C688 0.1u/10V PEG_RXN3 V_GMCHEXP_RXN3
C385 0.1u/10V PEG_RXP4 V_GMCHEXP_RXP4
C690 0.1u/10V PEG_RXN4 V_GMCHEXP_RXN4
C353 0.1u/10V PEG_RXP5 V_GMCHEXP_RXP5
C693 0.1u/10V PEG_RXN5 V_GMCHEXP_RXN5
C361 0.1u/10V PEG_RXP6 V_GMCHEXP_RXP6
C696 0.1u/10V PEG_RXN6 V_GMCHEXP_RXN6
C364 0.1u/10V PEG_RXP7 V_GMCHEXP_RXP7
C699 0.1u/10V PEG_RXN7 V_GMCHEXP_RXN7
PEG_RXP8 V_GMCHEXP_RXP8
PEG_RXN8 V_GMCHEXP_RXN8
PEG_RXP9 V_GMCHEXP_RXP9
PEG_RXN9 V_GMCHEXP_RXN9
PEG_RXP10 V_GMCHEXP_RXP10
PEG_RXN10 V_GMCHEXP_RXN10
PEG_RXP11 V_GMCHEXP_RXP11
PEG_RXN11 V_GMCHEXP_RXN11
PEG_RXP12 V_GMCHEXP_RXP12
PEG_RXN12 V_GMCHEXP_RXN12
PEG_RXP13 V_GMCHEXP_RXP13
PEG_RXN13 V_GMCHEXP_RXN13
PEG_RXP14 V_GMCHEXP_RXP14
PEG_RXN14 V_GMCHEXP_RXN14
PEG_RXP15 V_GMCHEXP_RXP15
PEG_RXN15 V_GMCHEXP_RXN15

C309 0.1u/10V PEG_RXN0 V_GMCHEXP_RXN0
C657 0.1u/10V PEG_RXN1 V_GMCHEXP_RXN1
C323 0.1u/10V PEG_RXN2 V_GMCHEXP_RXN2
C663 0.1u/10V PEG_RXN3 V_GMCHEXP_RXN3
C332 0.1u/10V PEG_RXN4 V_GMCHEXP_RXN4
C685 0.1u/10V PEG_RXN5 V_GMCHEXP_RXN5
C367 0.1u/10V PEG_RXN6 V_GMCHEXP_RXN6
C687 0.1u/10V PEG_RXN7 V_GMCHEXP_RXN7
C384 0.1u/10V PEG_RXN8 V_GMCHEXP_RXN8
C689 0.1u/10V PEG_RXN9 V_GMCHEXP_RXN9
C352 0.1u/10V PEG_RXN10 V_GMCHEXP_RXN10
C692 0.1u/10V PEG_RXN11 V_GMCHEXP_RXN11
C360 0.1u/10V PEG_RXN12 V_GMCHEXP_RXN12
C695 0.1u/10V PEG_RXN13 V_GMCHEXP_RXN13
C363 0.1u/10V PEG_RXN14 V_GMCHEXP_RXN14
C698 0.1u/10V PEG_RXN15 V_GMCHEXP_RXN15

+1.2V_GFX_PCIE
L14 BLM11A121S
G72_PLLAVDD
C242 4.7u/6.3V_6
C192 0.1u/10V

+3VRUN
C651 *0.1u/10V
U33 *TC7SH08FU
PLTRST# 13,14,24,29,33,44
R93 *200/F
R386 0

+VCC_GFX_CORE
C247 100p/50V
C189 0.01u/16V
C197 0.01u/16V
C168 100p/50V
C181 0.01u/16V
C228 220p/50V
C240 100p/50V
C223 220p/50V
C205 100p/50V
C170 1u/10V
C224 220p/50V
C185 0.01u/16V
C238 220p/50V
C225 220p/50V
C219 10u/6.3V_6
C245 10u/6.3V_6
C188 10u/6.3V_6

+1.2V_GFX_PCIE
C266 0.022u/16V
C274 0.022u/16V
C273 0.022u/16V
C258 10u/6.3V_6
C261 1u/10V
C277 4.7u/6.3V_6
PLACE NEAR BALLS
PLACE NEAR GPU

+1.2V_GFX_PCIE
C259 10u/6.3V_6
C271 0.022u/16V
C276 0.1u/10V
C272 0.1u/10V
C260 1u/10V
C606 4.7u/6.3V_6
PLACE NEAR BALLS

+VCC_GFX_CORE
C209 220p/50V
C193 0.01u/16V
C249 0.1u/10V

+1.2V_GFX_PCIE
L17 BLM11A121S
C285 4.7u/6.3V_6
C281 1u/10V
C280 1u/10V
C241 0.1u/10V
C255 0.01u/16V

+3VRUN
C169 0.1u/10V
C173 4700p/25V
C230 0.022u/16V
C155 1u/10V
PLACE NEAR BALLS

PROJECT : TW3
Quanta Computer Inc.

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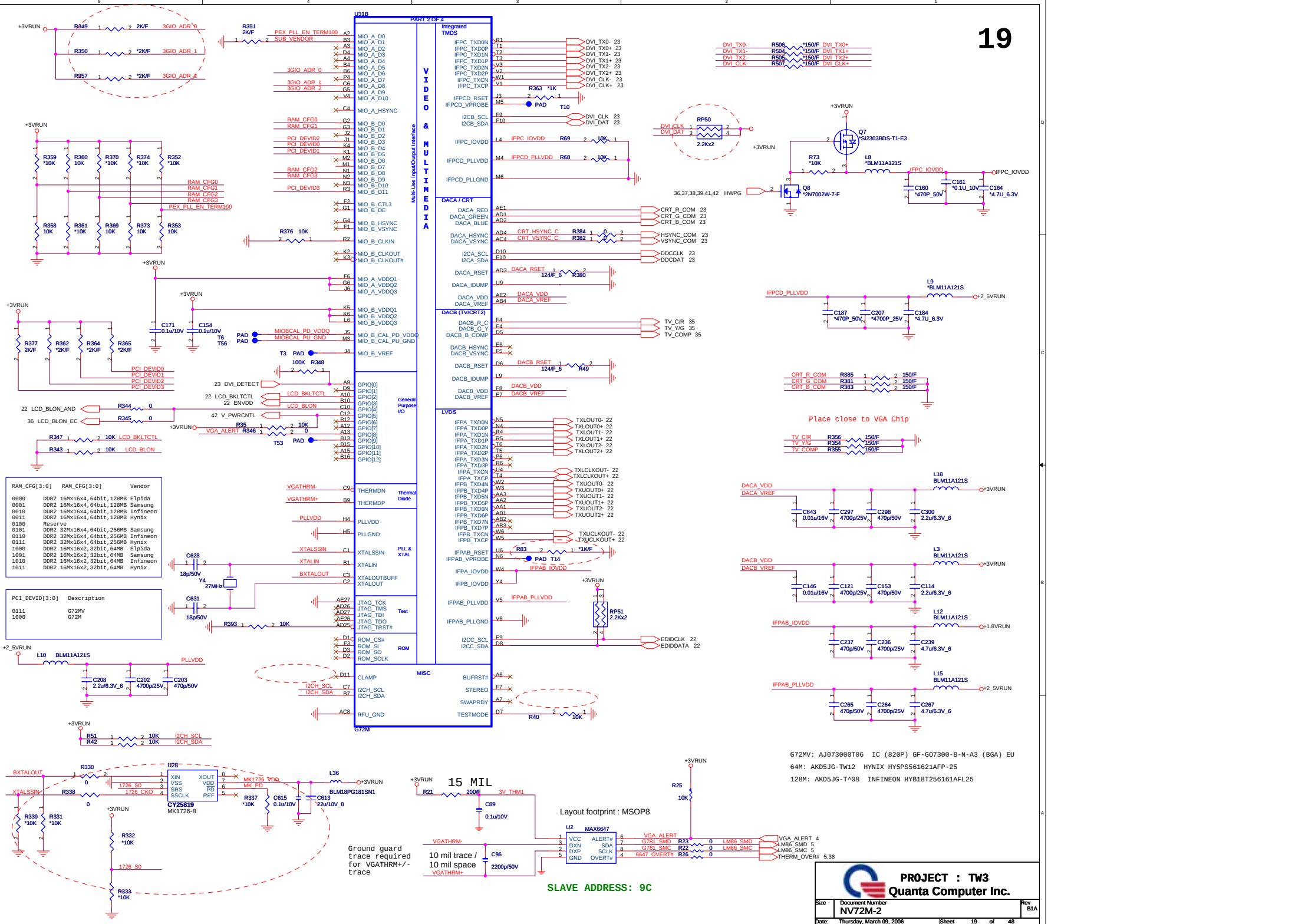
U31B
PART 2 OF 4
VIDEO & MULTIMEDIA
Multi-Use Input/Output interface
Integrated TMDS
DACA / CRT
DACB (TV/CRT2)
LVDS
General Purpose I/O
Thermal Diode
PLL & XTAL
Test
ROM
MISC
G72M
+3VRUN
+2_5VRUN
+1.8VRUN
Place close to VGA Chip
15 MIL
Layout footprint : MSOP8
Ground guard trace required for VGATHRM+/- trace
10 mil trace / 10 mil space
SLAVE ADDRESS: 9C
G72MV: AJ073000T06 IC (820P) GF-GO7300-B-N-A3 (BGA) EU
64M: AKD5JG-TW12 HYNIX HY5PS561621AFP-25
128M: AKD5JG-T^08 INFINEON HYB18T256161AFL25
PROJECT : TW3
Quanta Computer Inc.
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FB_CMD[0..26] 21
FBD[0..63] 21
FBDQM[0..7] 21
FBDQS[0..7] 21
FBDQS#[0..7] 21

U31C

Part 3 of 4

MEMORY INTERFACE

FBD0	A26	FB_DQ0	FB_CMD0	G27	FB_CMD0
FBD1	C24	FB_DQ1	FB_CMD1	D25	FB_CMD1
FBD2	B24	FB_DQ2	FB_CMD2	F26	FB_CMD2
FBD3	A24	FB_DQ3	FB_CMD3	F25	FB_CMD3
FBD4	C22	FB_DQ4	FB_CMD4	G25	FB_CMD4
FBD5	A25	FB_DQ5	FB_CMD5	J25	FB_CMD5
FBD6	B25	FB_DQ6	FB_CMD6	J27	FB_CMD6
FBD7	D23	FB_DQ7	FB_CMD7	M26	FB_CMD7
FBD8	G22	FB_DQ8	FB_CMD8	C27	FB_CMD8
FBD9	J23	FB_DQ9	FB_CMD9	C25	FB_CMD9
FBD10	E24	FB_DQ10	FB_CMD10	D24	FB_CMD10
FBD11	F23	FB_DQ11	FB_CMD11	N27	FB_CMD11
FBD12	J24	FB_DQ12	FB_CMD12	G24	FB_CMD12
FBD13	F24	FB_DQ13	FB_CMD13	J26	FB_CMD13
FBD14	G23	FB_DQ14	FB_CMD14	M27	FB_CMD14
FBD15	H24	FB_DQ15	FB_CMD15	C26	FB_CMD15
FBD16	D16	FB_DQ16	FB_CMD16	M25	FB_CMD16
FBD17	E16	FB_DQ17	FB_CMD17	D26	FB_CMD17
FBD18	D17	FB_DQ18	FB_CMD18	D27	FB_CMD18
FBD19	F18	FB_DQ19	FB_CMD19	K26	FB_CMD19
FBD20	E19	FB_DQ20	FB_CMD20	K25	FB_CMD20
FBD21	E18	FB_DQ21	FB_CMD21	K24	FB_CMD21
FBD22	D20	FB_DQ22	FB_CMD22	F27	FB_CMD22
FBD23	D19	FB_DQ23	FB_CMD23	K27	FB_CMD23
FBD24	A18	FB_DQ24	FB_CMD24	G26	FB_CMD24
FBD25	B18	FB_DQ25	FB_CMD25	B27	FB_CMD25
FBD26	A19	FB_DQ26	FB_CMD26	N24	FB_CMD26
FBD27	B19	FB_DQ27			
FBD28	D18	FB_DQ28			
FBD29	C19	FB_DQ29			
FBD30	C16	FB_DQ30	FB_DQM0	D21	FBDQM0
FBD31	C18	FB_DQ31	FB_DQM1	F22	FBDQM1
FBD32	N26	FB_DQ32	FB_DQM2	F20	FBDQM2
FBD33	N25	FB_DQ33	FB_DQM3	A21	FBDQM3
FBD34	R25	FB_DQ34	FB_DQM4	V27	FBDQM4
FBD35	R26	FB_DQ35	FB_DQM5	W22	FBDQM5
FBD36	R27	FB_DQ36	FB_DQM6	V22	FBDQM6
FBD37	T25	FB_DQ37	FB_DQM7	V24	FBDQM7
FBD38	T27	FB_DQ38			
FBD39	T26	FB_DQ39			
FBD40	AB23	FB_DQ40	read strobe		
FBD41	Y24	FB_DQ41	FB_DQS_RN0	A22	FBDQS#0
FBD42	AB24	FB_DQ42	FB_DQS_RN1	E22	FBDQS#1
FBD43	AB22	FB_DQ43	FB_DQS_RN2	F21	FBDQS#2
FBD44	AC24	FB_DQ44	FB_DQS_RN3	B21	FBDQS#3
FBD45	AC22	FB_DQ45	FB_DQS_RN4	V26	FBDQS#4
FBD46	AA23	FB_DQ46	FB_DQS_RN5	W23	FBDQS#5
FBD47	AA22	FB_DQ47	FB_DQS_RN6	V23	FBDQS#6
FBD48	T24	FB_DQ48	FB_DQS_RN7	W27	FBDQS#7
FBD49	T23	FB_DQ49	write strobe		
FBD50	R24	FB_DQ50	FB_DQS_WP0	B22	FBDQS0
FBD51	R23	FB_DQ51	FB_DQS_WP1	D22	FBDQS1
FBD52	R22	FB_DQ52	FB_DQS_WP2	E21	FBDQS2
FBD53	T22	FB_DQ53	FB_DQS_WP3	C21	FBDQS3
FBD54	N23	FB_DQ54	FB_DQS_WP4	V25	FBDQS4
FBD55	P24	FB_DQ55	FB_DQS_WP5	W24	FBDQS5
FBD56	AA24	FB_DQ56	FB_DQS_WP6	U24	FBDQS6
FBD57	AA27	FB_DQ57	FB_DQS_WP7	W26	FBDQS7
FBD58	AA26	FB_DQ58			
FBD59	AB25	FB_DQ59			
FBD60	AB26	FB_DQ60			
FBD61	AB27	FB_DQ61			
FBD62	AA25	FB_DQ62			
FBD63	W25	FB_DQ63			

		FBVTT_01	E15		
		FBVTT_02	F15		
		FBVTT_03	F16		
		FBVTT_04	J17		
		FBVTT_05	J18		
		FBVTT_06	L19		
		FBVTT_07	N19		
		FBVTT_08	R19		
		FBVTT_09	U19		
		FBVTT_10	W19		
		FBVDDQ_01	F17		
		FBVDDQ_02	F19		
		FBVDDQ_03	J19		
		FBVDDQ_04	M19		
		FBVDDQ_05	T19		
		FBVDDQ_06	J22		
		FBVDDQ_07	L22		
		FBVDDQ_08	P22		
		FBVDDQ_09	U22		
		FBVDDQ_10	Y22		
21 FB_CLK0	L24	FB_CLK0			
21 FB_CLK0#	K23	FB_CLK0#			
21 FB_CLK1	M22	FB_CLK1			
21 FB_CLK1#	N22	FB_CLK1#			
T11 PAD	M23	FB_REFCLK			
T12 PAD	M24	FB_REFCLK#			
T13 PAD	K22	FB_DEBUG			
FBVREF	A16	FB_VREF			
T52 PAD	D14	FB_PLLVDD	FBCAL_PD_VDDQ	D15	FBCAL_PD_VDDQ
FB_PLLAVDD	D13	FB_PLLAVDD	FBCAL_PU_GND	F13	FBCAL_PU_GND
	C15	FB_PLLAGND	FBCAL_TERM_GND	H22	FBCAL_TERM_GND

G72M

U31D

Part 4 of 4

GND

B2	GND_01	GND_48	P14
E2	GND_02	GND_49	R14
H2	GND_03	GND_50	U14
L2	GND_04	GND_51	W14
P2	GND_05	GND_52	AC14
U2	GND_06	GND_53	AD14
Y2	GND_07	GND_54	N15
AC2	GND_08	GND_55	P15
AF2	GND_09	GND_56	R15
AF3	GND_10	GND_57	AF15
B5	GND_11	GND_58	N16
E5	GND_12	GND_59	P16
L5	GND_13	GND_60	R16
P5	GND_14	GND_61	AD16
U5	GND_15	GND_62	B17
Y5	GND_16	GND_63	E17
AC5	GND_17	GND_64	L17
H6	GND_18	GND_65	P17
AF6	GND_19	GND_66	U17
B8	GND_20	GND_67	AD17
E8	GND_21	GND_68	AF18
AD8	GND_22	GND_69	K19
K9	GND_23	GND_70	P19
P9	GND_24	GND_71	V19
V9	GND_25	GND_72	AD19
AD9	GND_26	GND_73	B20
AF9	GND_27	GND_74	E20
B11	GND_28	GND_75	AD20
E11	GND_29	GND_76	AF21
F11	GND_30	GND_77	B23
L11	GND_31	GND_78	E23
P11	GND_32	GND_79	H23
U11	GND_33	GND_80	L23
AD11	GND_34	GND_81	P23
N12	GND_35	GND_82	U23
P12	GND_36	GND_83	Y23
R12	GND_37	GND_84	AC23
AD12	GND_38	GND_85	AF24
AF12	GND_39	GND_86	B26
N13	GND_40	GND_87	E26
P13	GND_41	GND_88	H26
R13	GND_42	GND_89	L26
B14	GND_43	GND_90	P26
E14	GND_44	GND_91	U26
J14	GND_45	GND_92	Y26
L14	GND_46	GND_93	AC26
N14	GND_47	GND_94	AF26

G72M

+1.8VRUN
R341 1K/F
FBVREF
R342 1K/F
C624 0.1u/10V

FBVREF = FBVDDQ * Rb/(Rt + Rb).
VREF = 0.5 * FBVDDQ.
DDR: 0.9V = 1.8V * 1K/(1K + 1K).

+1.2V_GFX_PCIE
L7 BLM11A121S
C135 4.7u/6.3V_6
C141 1u/10V
C138 0.01u/16V

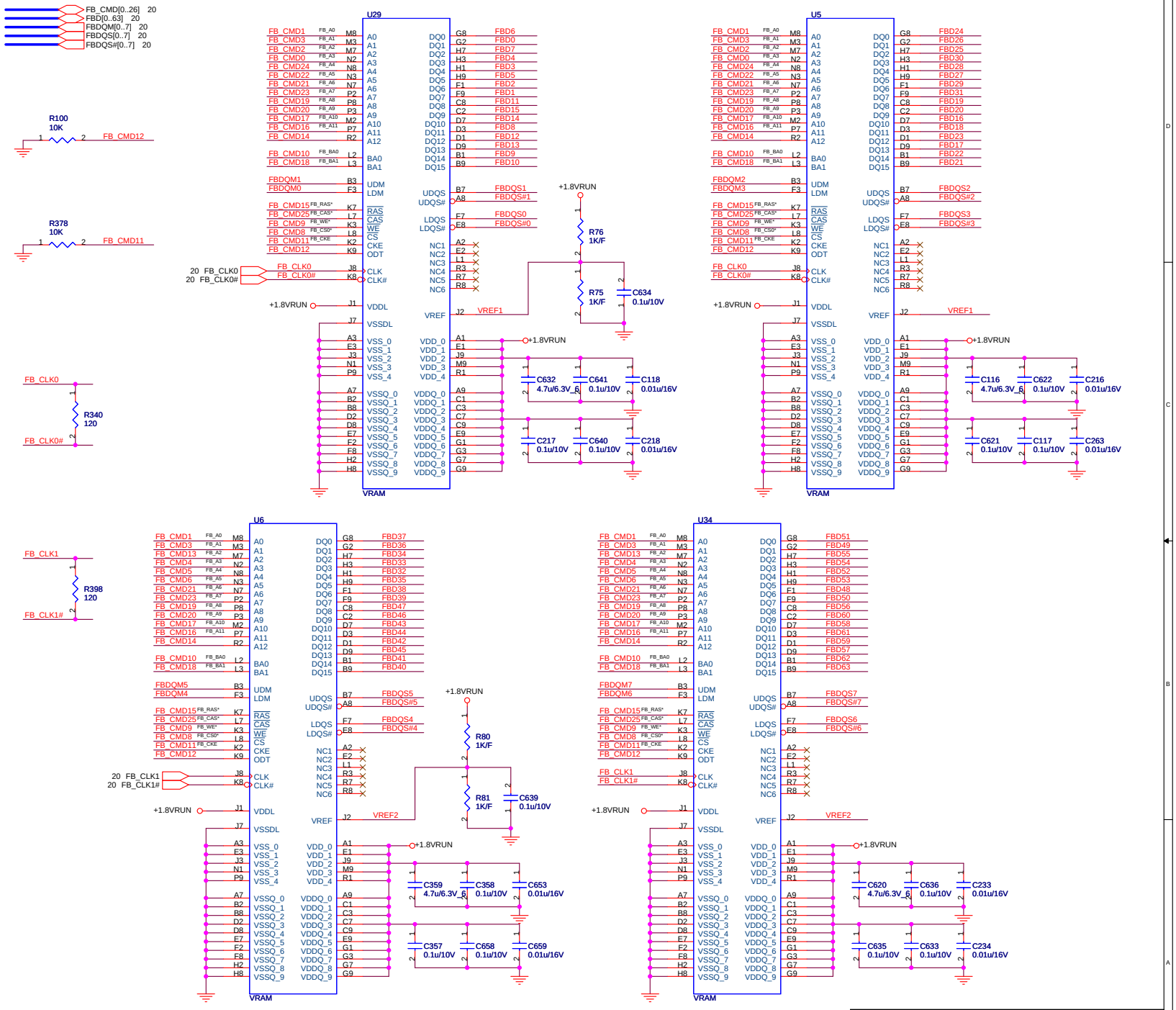
+1.8VRUN
R53 40.2/F
R57 *0
R52 30/F

PLACE BELOW GPU

+1.8VRUN
C179 4700p/25V
C213 0.022u/16V
C232 0.1u/10V
C130 4700p/25V
C638 0.1u/10V
C661 4.7u/6.3V_6
C650 1u/10V
C177 4700p/25V
C191 0.022u/16V
C251 0.1u/10V
C180 4700p/25V
C214 0.022u/16V
C252 0.1u/10V
C235 4.7u/6.3V_6
C157 4700p/25V
C166 0.022u/16V
C172 0.1u/10V
C190 0.022u/16V
C158 0.1u/10V
C630 1u/10V

PROJECT : TW3
Quanta Computer Inc.

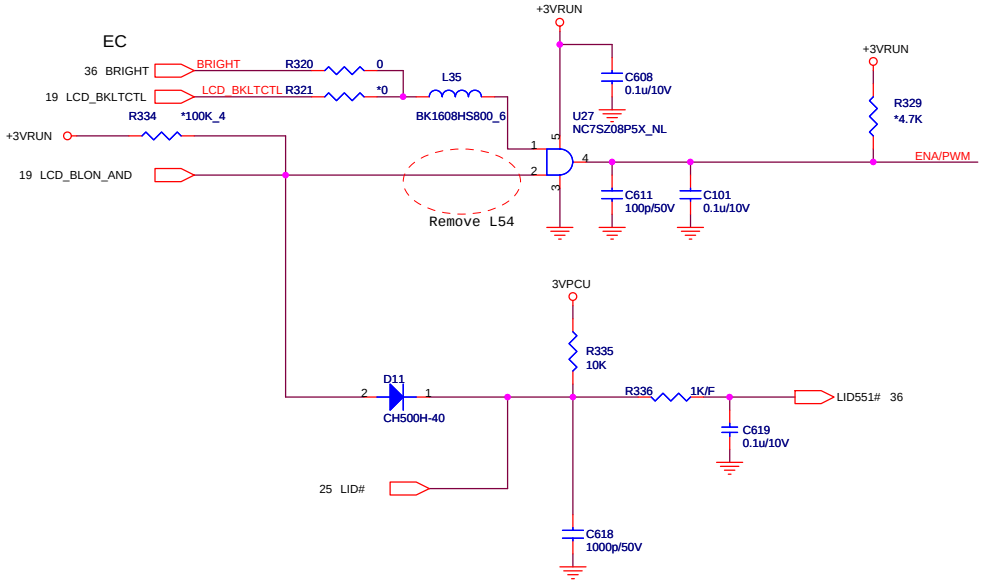
Size	Document Number	Rev
	NV72M-3	B1A
Date: Thursday, March 09, 2006	Sheet 20 of 47	

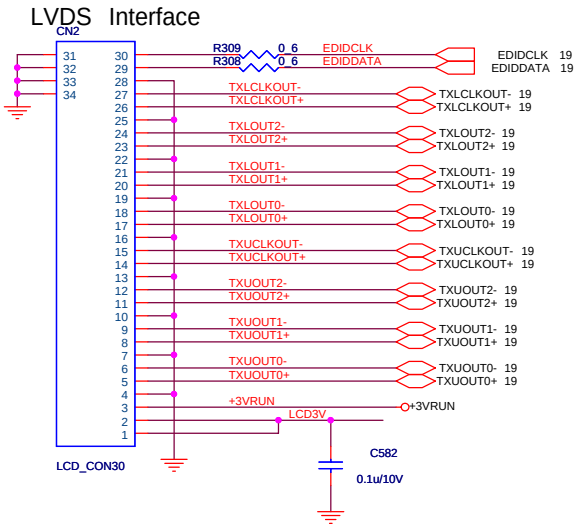


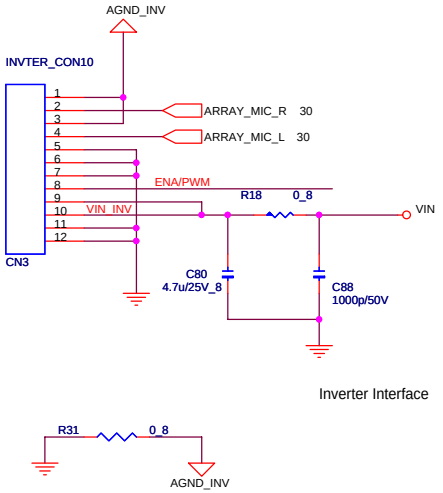
PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	NV72M-4	B1A

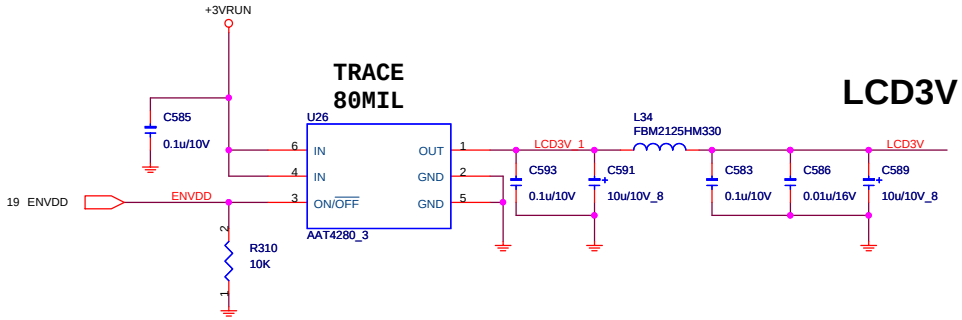
Date: Thursday, March 09, 2006 Sheet 21 of 47







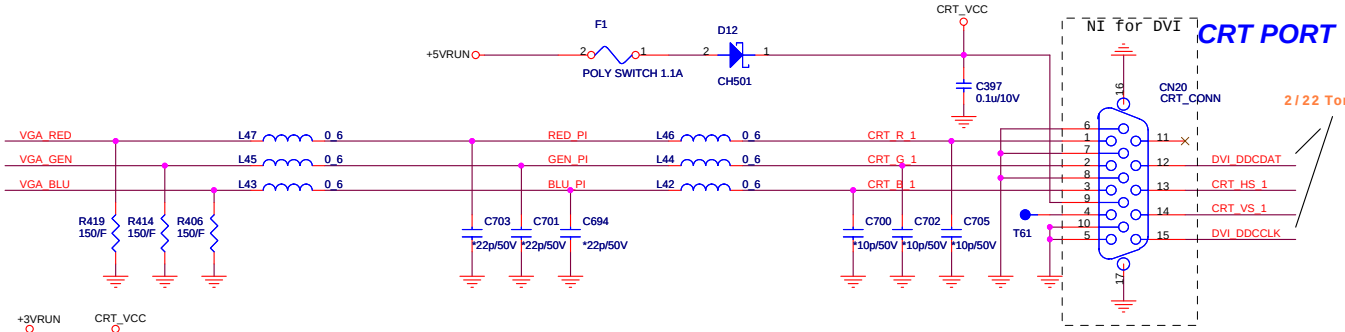
Inverter Interface



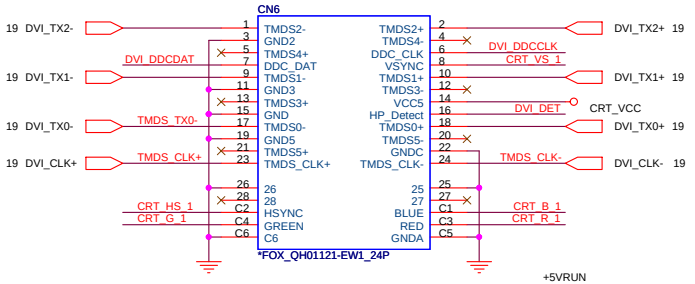
PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	LCD,INVERTER CONN	B1A
Date: Thursday, March 09, 2006	Sheet 22 of 47	

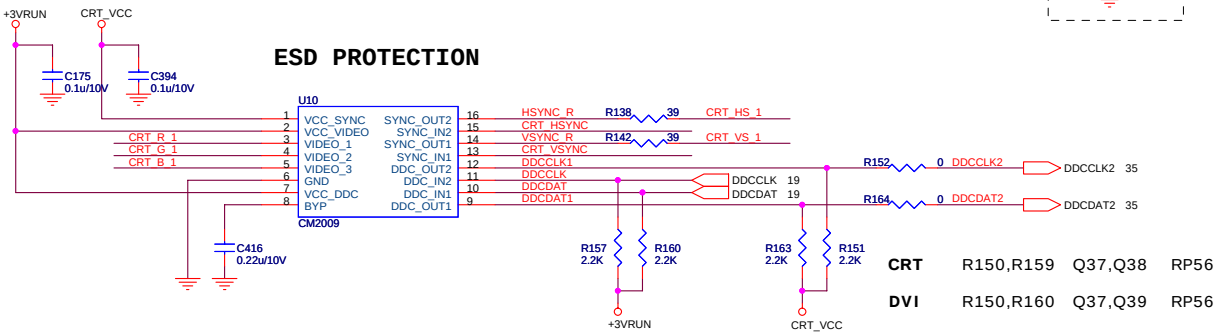
CRT PORT



2/22 Tony Huang



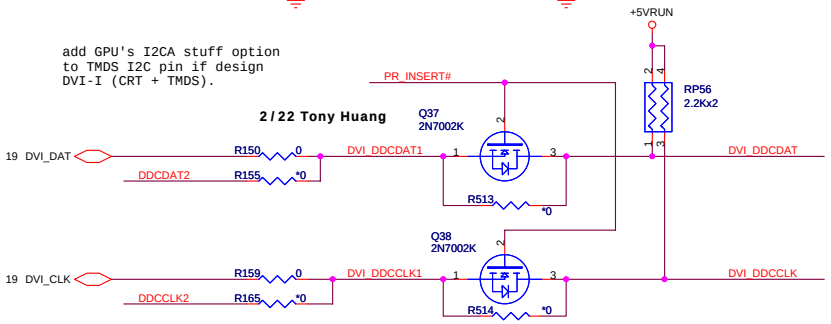
ESD PROTECTION



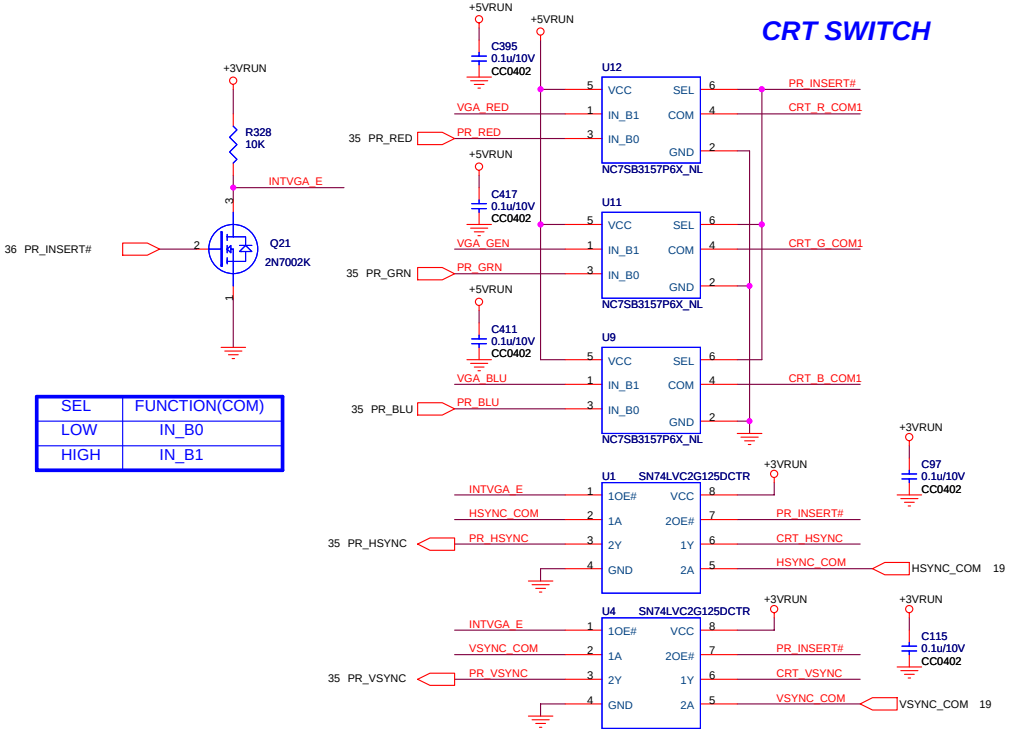
CRT	R150,R159	Q37,Q38	RP56
DVI	R150,R160	Q37,Q39	RP56

add GPU's I2CA stuff option
to TMDS I2C pin if design
DVI-I (CRT + TMDS).

2/22 Tony Huang

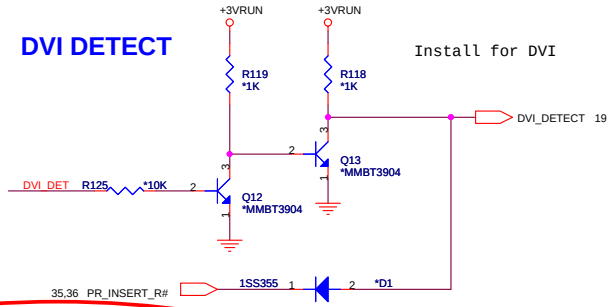


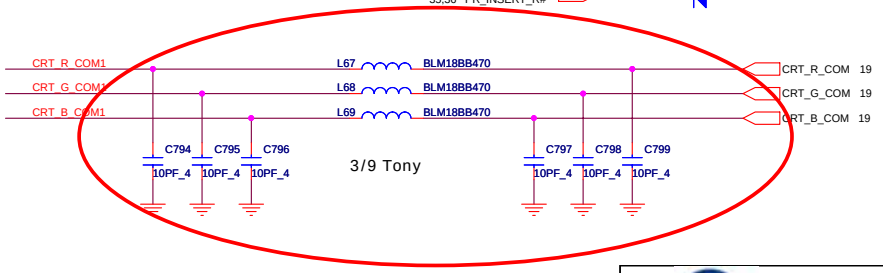
CRT SWITCH



SEL	FUNCTION(COM)
LOW	IN_B0
HIGH	IN_B1

DVI DETECT





PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	CRT,TV-OUT,DVI CONN.	B1A

Date: Thursday, March 09, 2006 Sheet 23 of 47

C: 88E8053 LF PN: AJ080530010 (20050414)

1Mbits

C: Add 9 X GND Pad for LAN controller. (20050411)

C: Add these GND pin for via hole to GND Plane.

C: Add RC (R37 change to 200K, Add C101) delay to control LOM_DISABLE#. (20050411)

C: Reserve R36. Change LANRST# to PCIRST# source from MB option modify.(2005/04/11)

CLOSE CHIP

DELAY PIN10 AT LEAST 150ms

88E8038/88E8055

FOR 8038	
R389	2K
R9	NC

Install for 8038

NI for 8038

LANVCC

PLACEMENT CLOSE TO EACH OTHER

C: Widen to 20 mils. AVDD25 to 20 mils.(20050411)

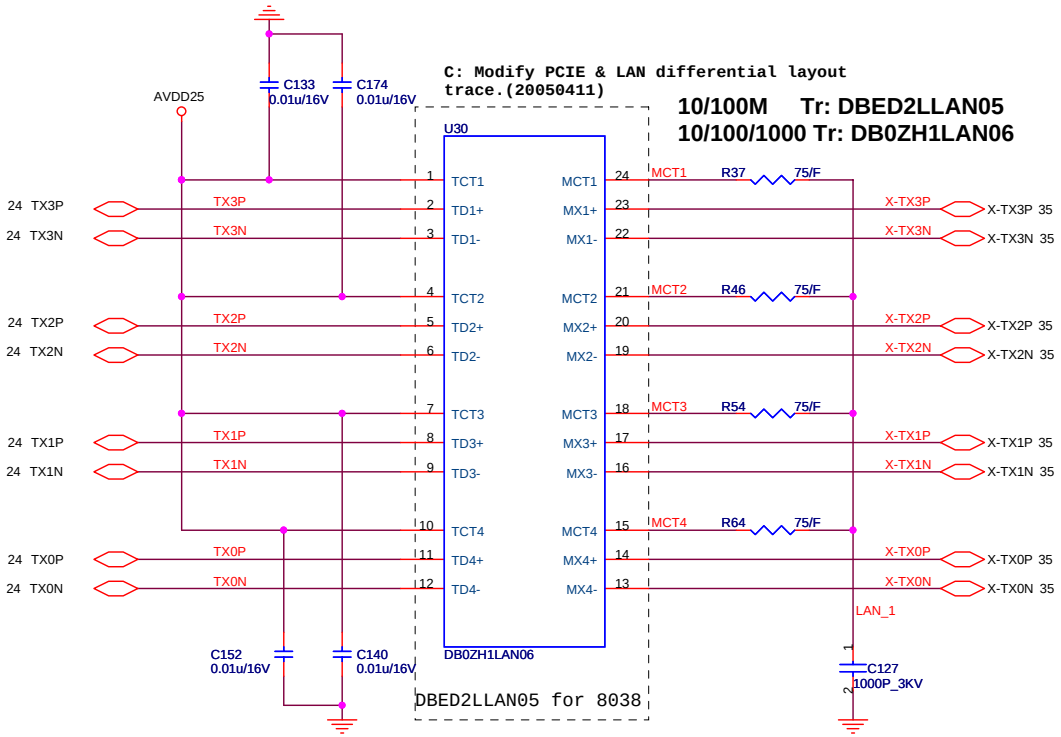
C: Widen to 20 mils. VDD to 20 mils.(20050411)

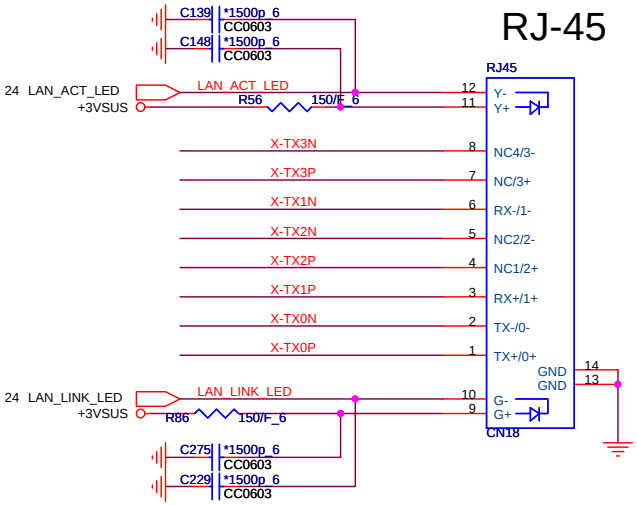
0804 REDUCING THE LANVCC NOISE

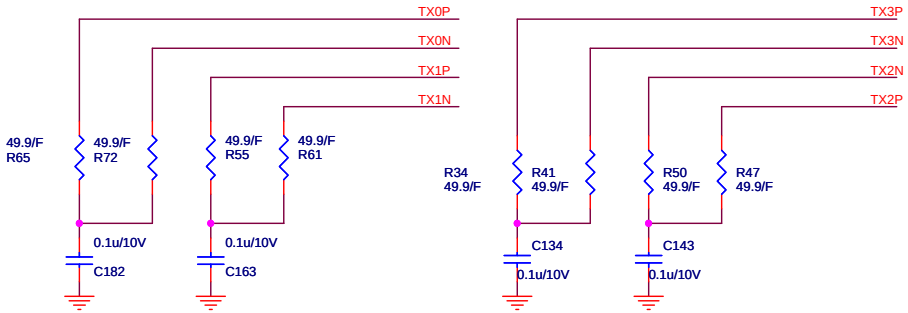
PROJECT : TW3
Quanta Computer Inc.

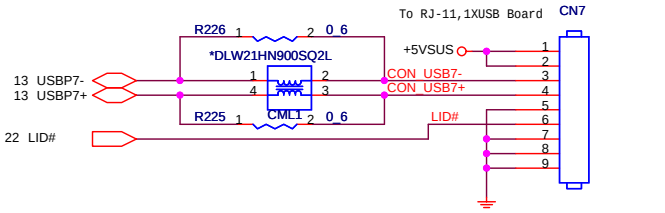
Size	Document Number	Rev
	Marvell 88E8036,88E8053	B1A

Date: Thursday, March 09, 2006 Sheet 24 of 47







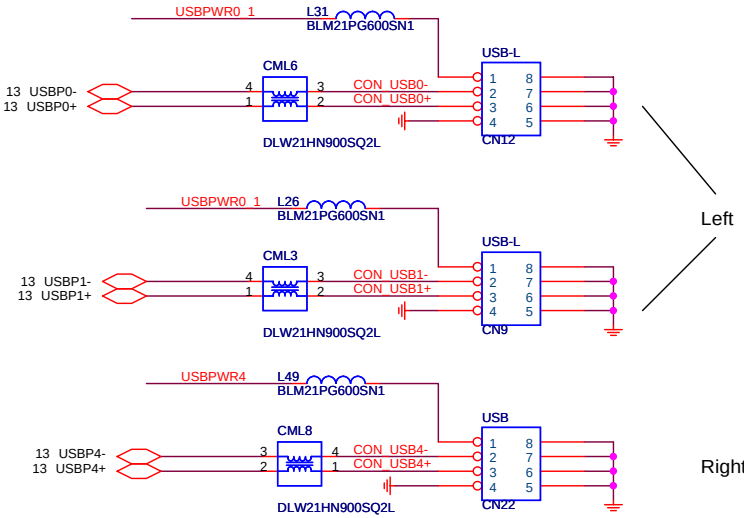


PROJECT : TW3
Quanta Computer Inc.

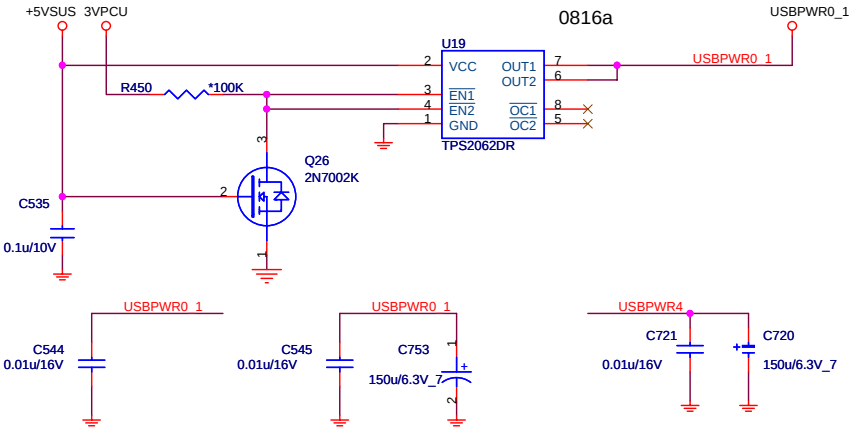
Size	Document Number	Rev
	LAN SW CONN& MDC CONN	B1A

Date: Thursday, March 09, 2006 Sheet 25 of 47

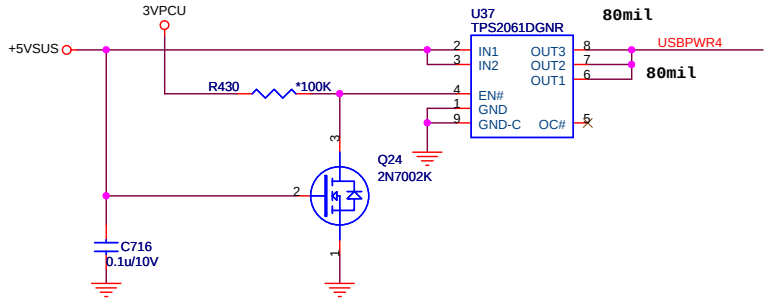
USB Port



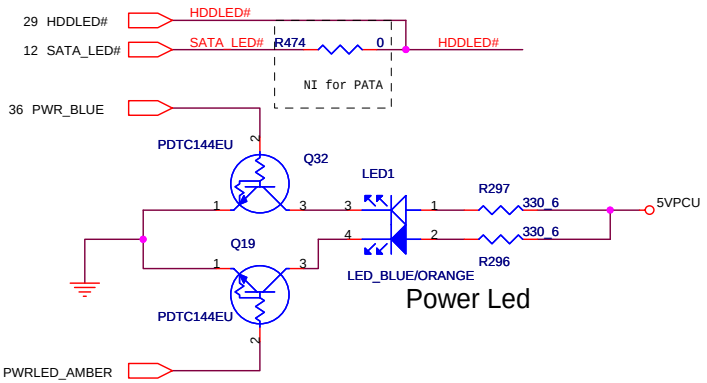
For Botton Board



C:Change U1 from G528 to TPS2061

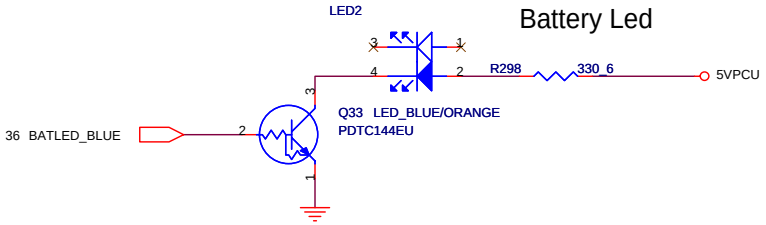


HDD,SATA Led

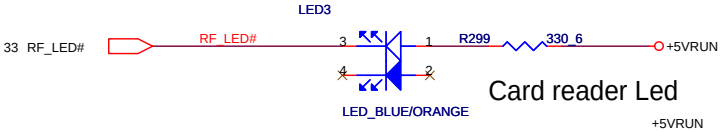


Power Led

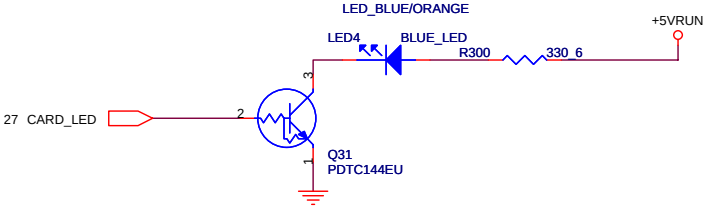
Battery Led

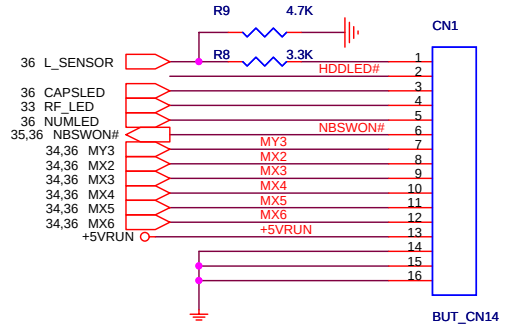


Wireless Led



Card reader Led

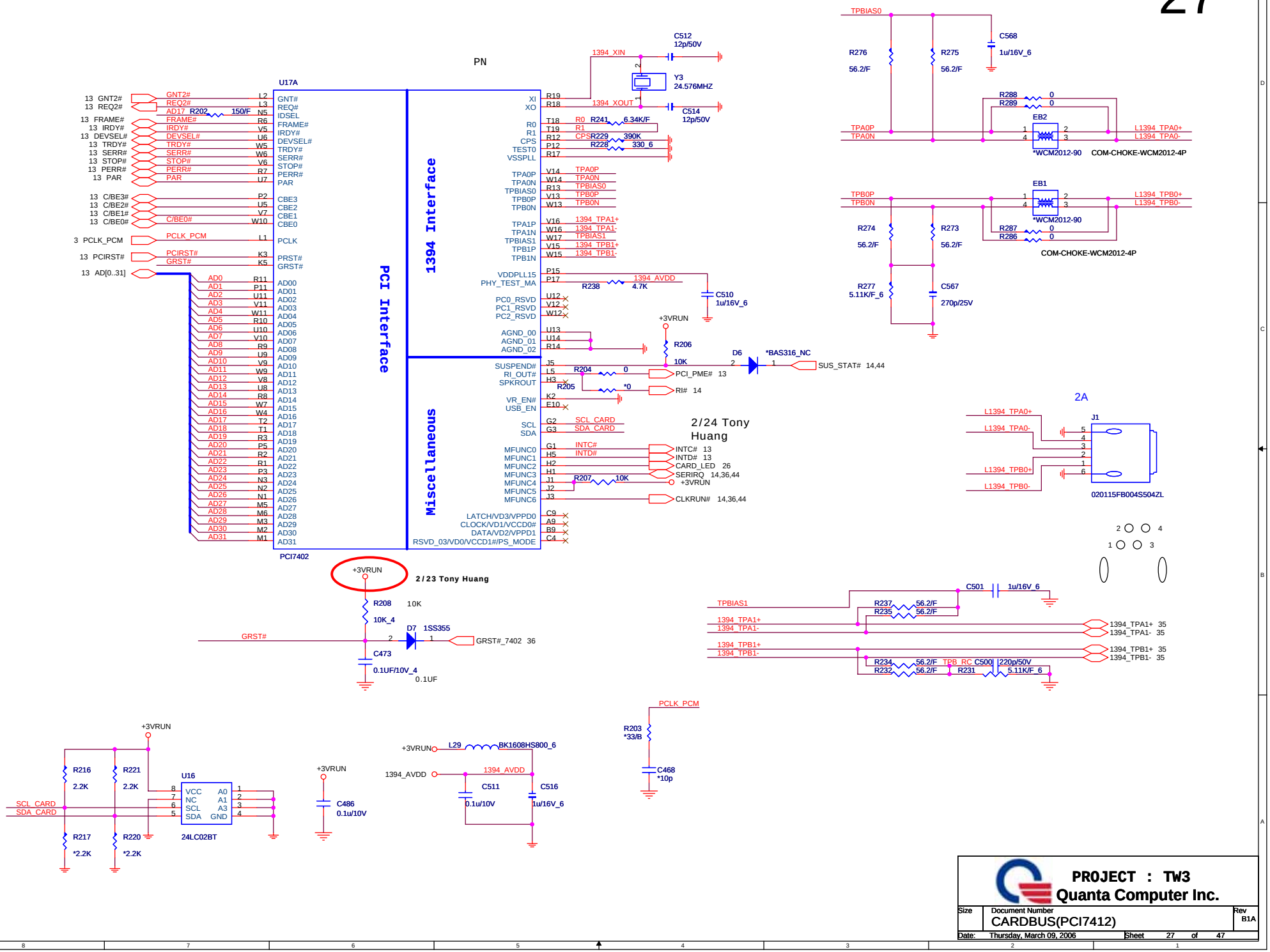




PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	USB,LED,Buttom/B	B1A

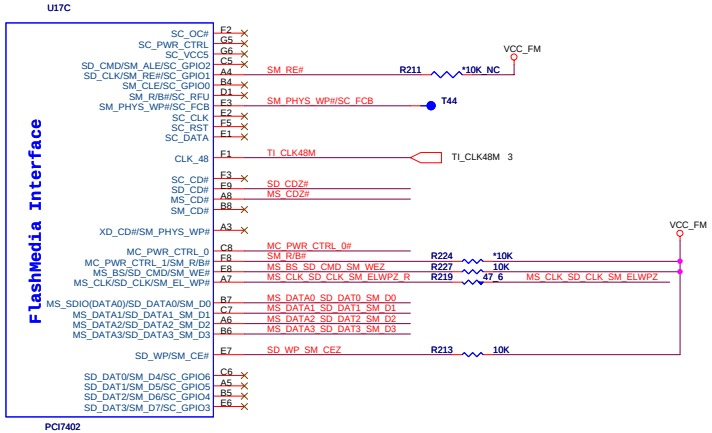
Date: Thursday, March 09, 2006 Sheet 26 of 47

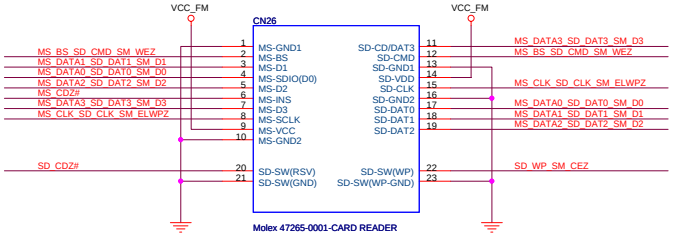


PROJECT : TW3		
Quanta Computer Inc.		
Size	Document Number	Rev
	CARDBUS(PCI7412)	B1A
Date: Thursday, March 09, 2006	Sheet 27 of 47	

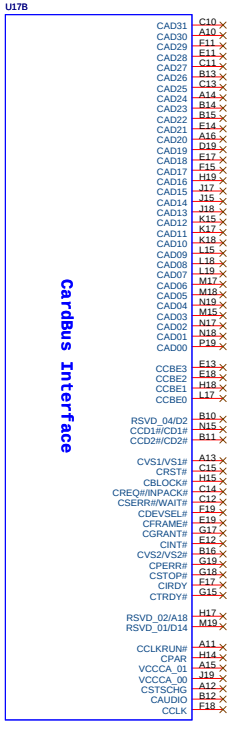
DO NOT INSERT SD/MMC, MEMORYSTICK AND XD SIMULTANEOUSLY.

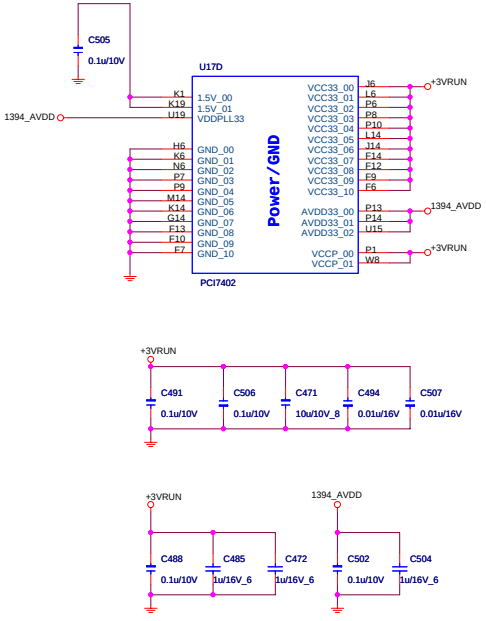
3 IN1 CARD READER (push-push)

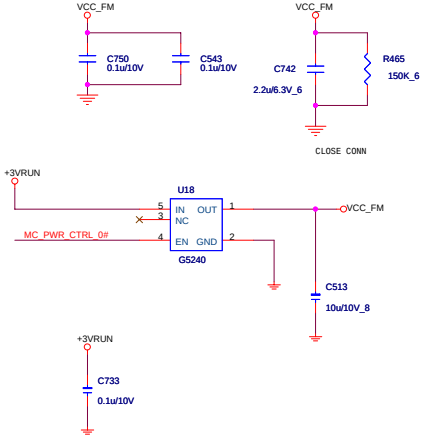




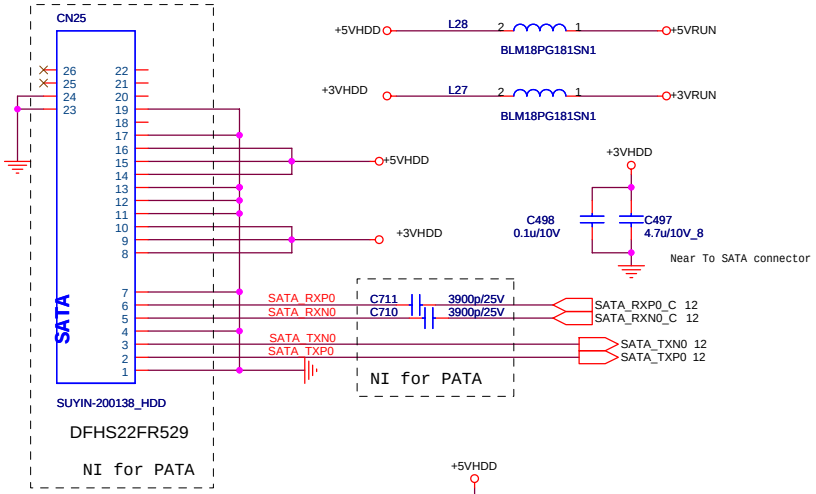
Supporting MMC/SD/MS Cards
Molex P/N:DFHD23MSBB6

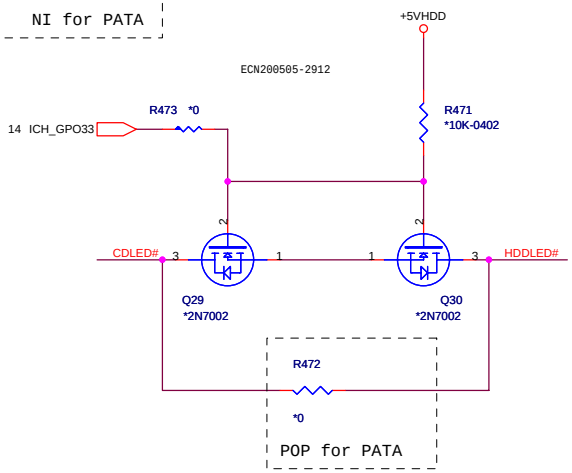




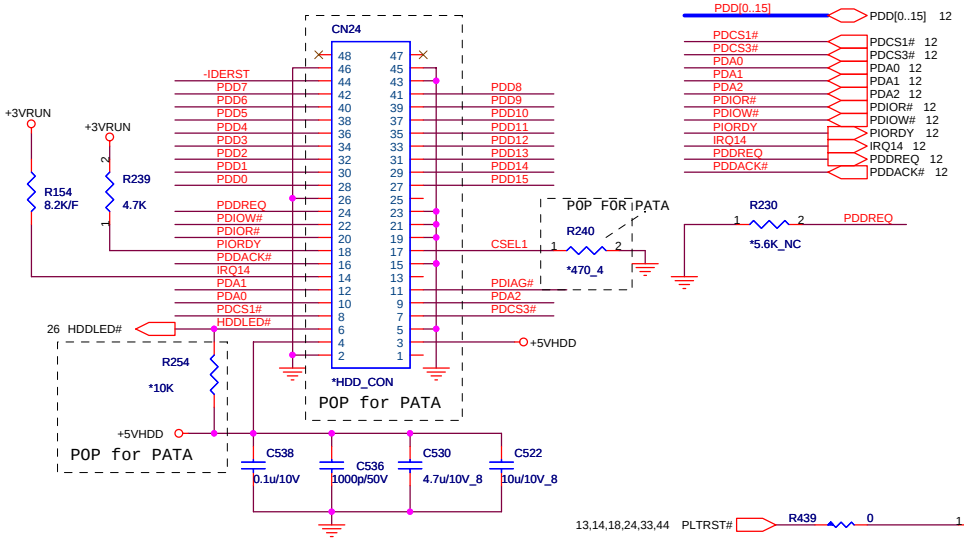


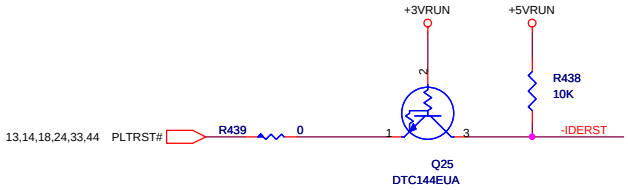
SATA HDD



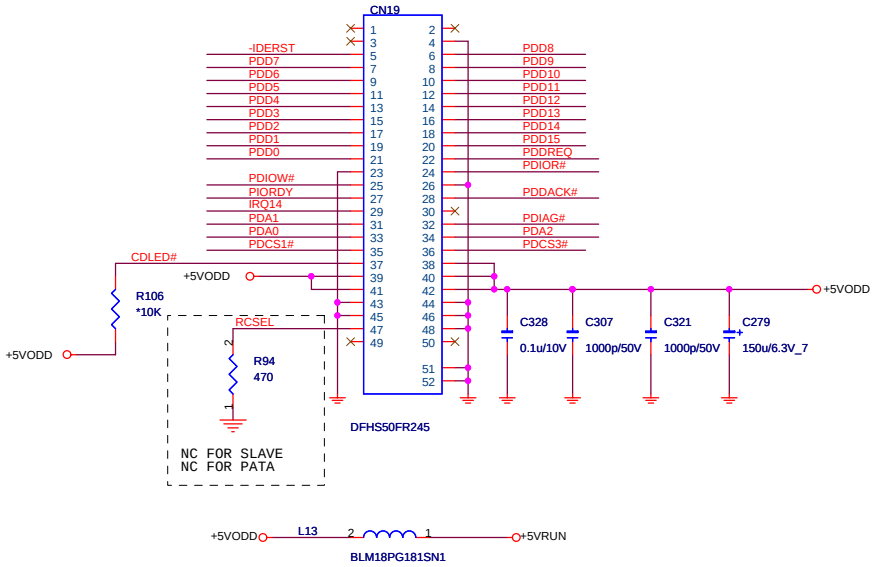


PATA HDD





ODD



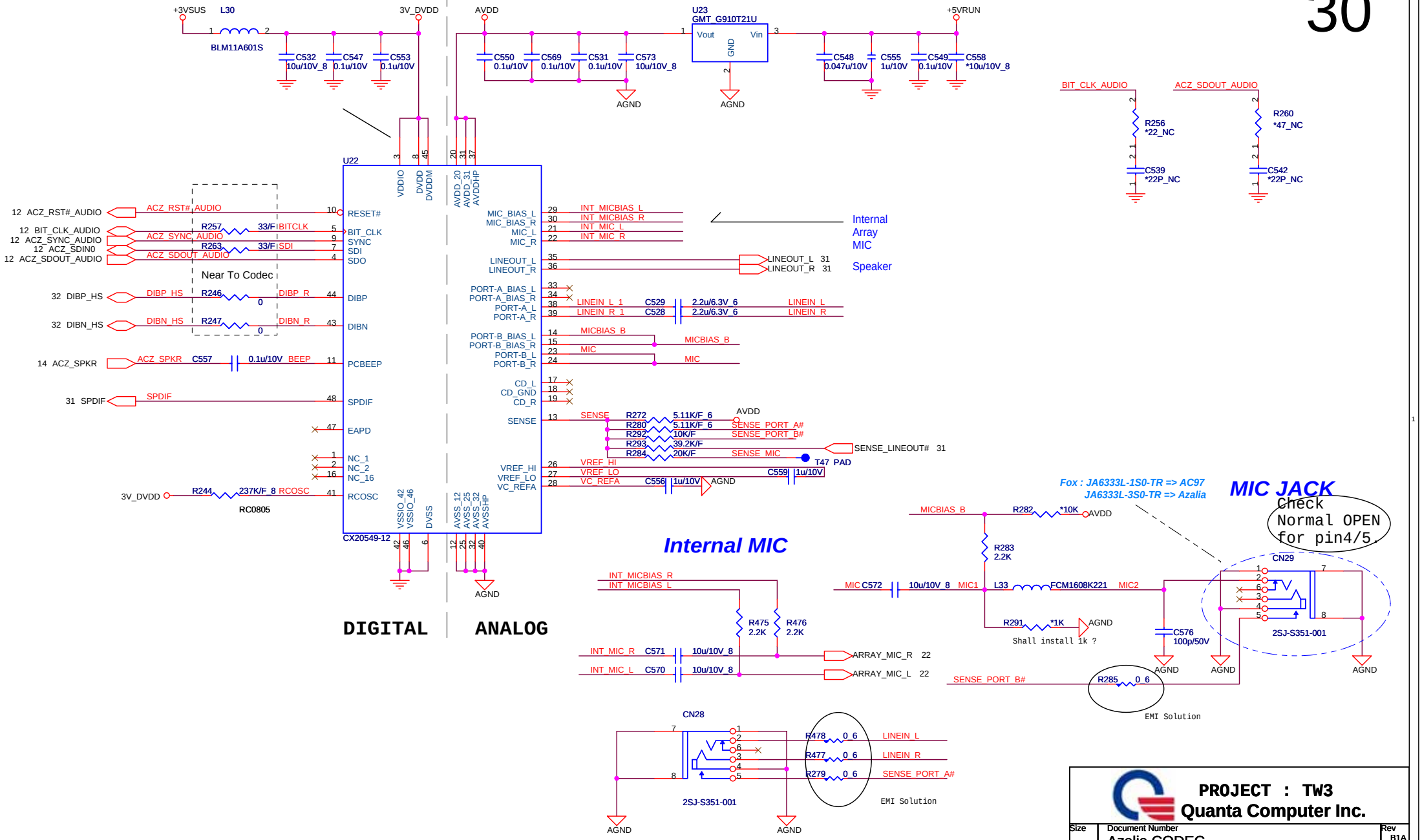
FOR PATA HDD

CN19	NI
C730	NI
C729	NI
CN18	HDD CON
R517	NI
Q25	2N7002
Q26	2N7002
R513	10K
R512	0
R168	470

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	SATA,PATA(HDD,ODD)	B1A

Date: Thursday, March 09, 2006 Sheet 29 of 47



PROJECT : TW3		
Quanta Computer Inc.		
Size	Document Number	Rev
	Azalia CODEC	B1A
Date: Thursday, March 09, 2006	Sheet 30 of 48	

0816a

EAPD
low:mute

HEADPHONE OUT/SPDIF

GAIN	SPKR MODE	HP MODE
0	10.5	3
1	9	0

Check
Normal OPEN
for pin4/5.

SPEAKER CON. BK1608HM121

3/9 Tony Huang

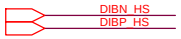
When Docking insert , disable BTL

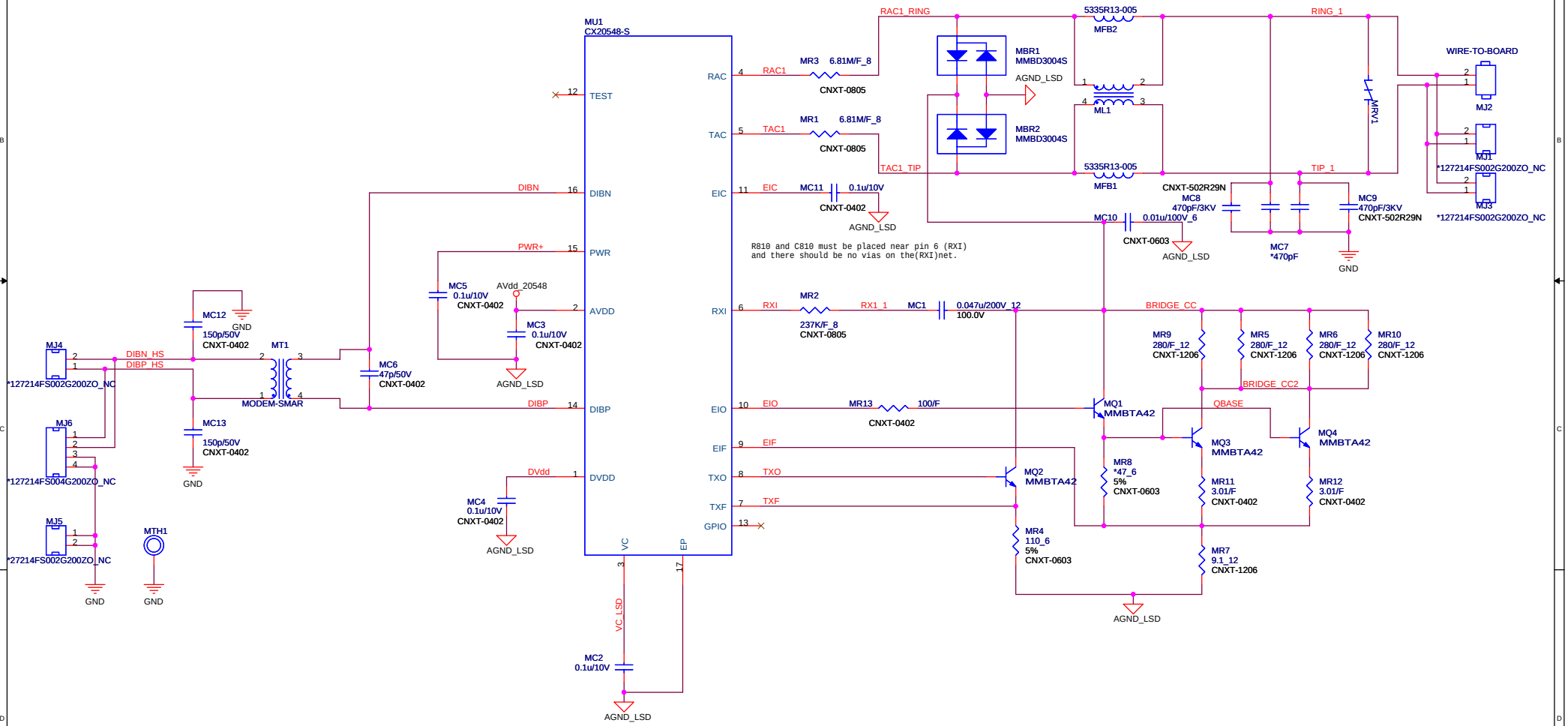
R189,R190
Modify to RC0603

PROJECT :	TW3
Quanta Computer Inc.	
Size	Document Number: AUDIO AMPLIFIER
Rev	A1A
Date:	Thursday, March 09, 2006
Sheet	31 of 47

Revision History		
REV	Description	Date
0	Initial Release	April 26, 2005

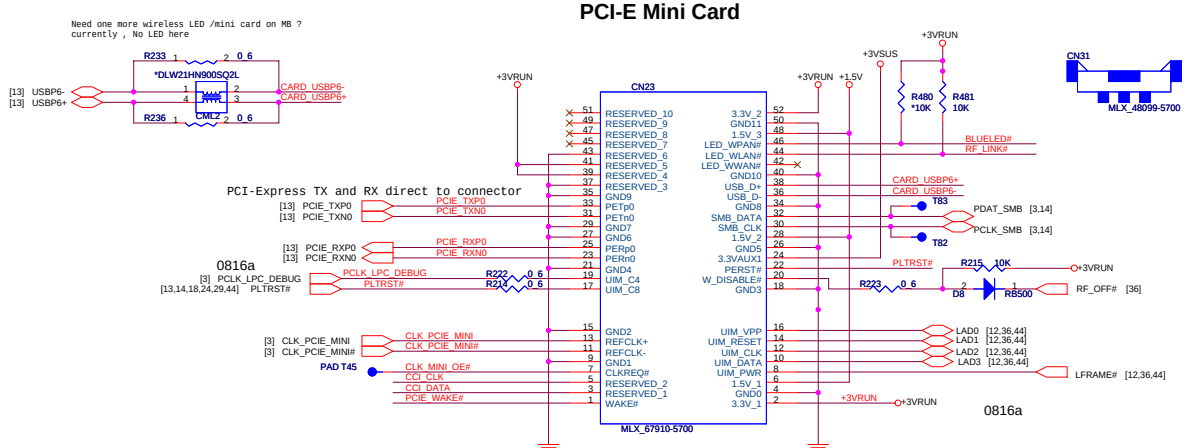
30 DIBN_HS
30 DIBP_HS



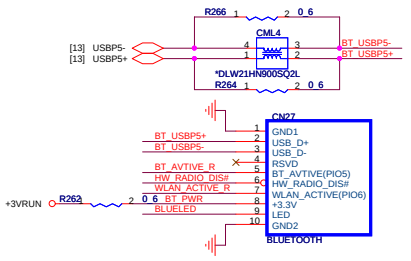


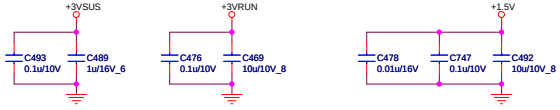
PROJECT : TW3			
Quanta Computer Inc.			
Size	Document Number		Rev
	Conexant Modem		B1A
Date:	Thursday, March 09, 2006	Sheet 32 of 47	

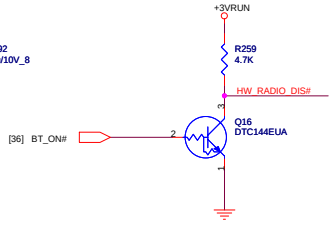
PCI-E Mini Card

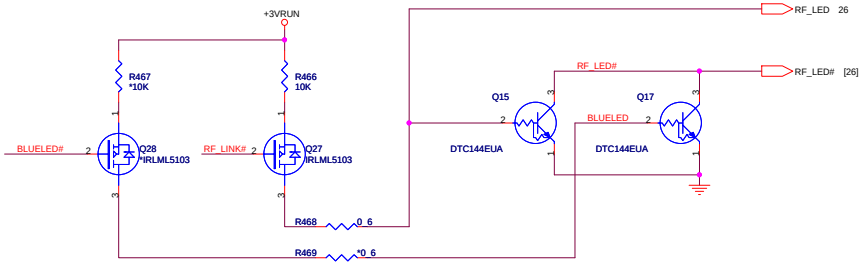


BLUETOOTH CONNECTOR

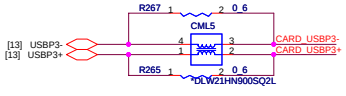


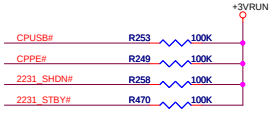


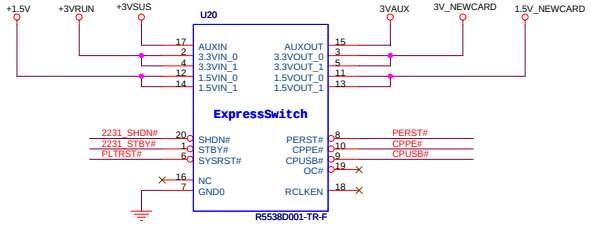


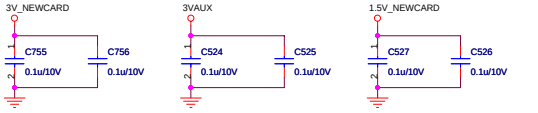


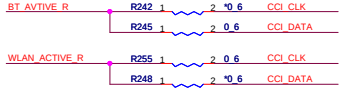
NEWCARD (PCIEXPRESS*1 + USB*1)

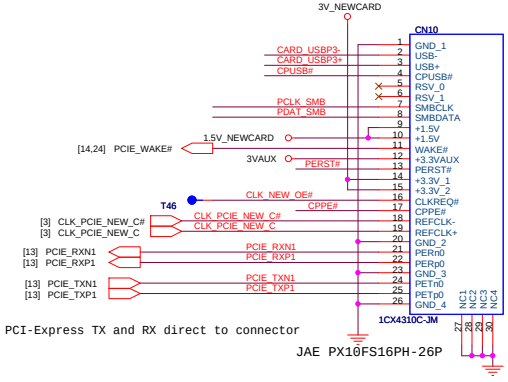






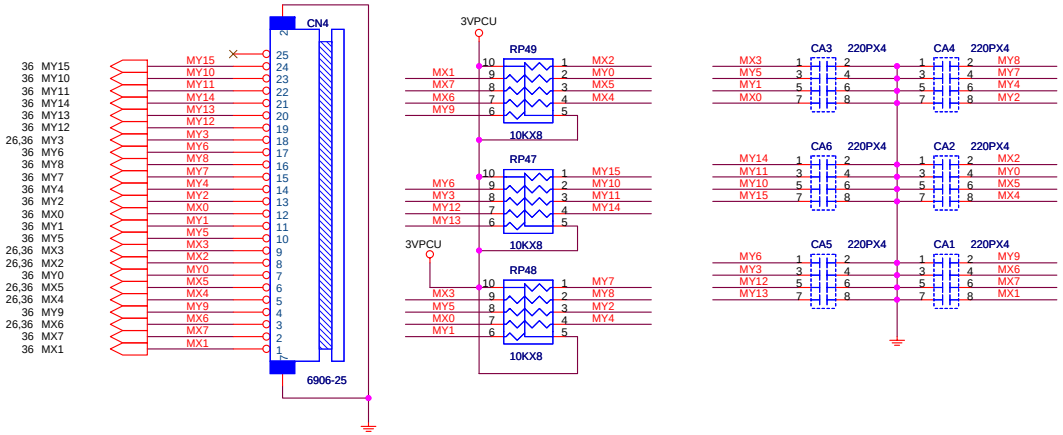


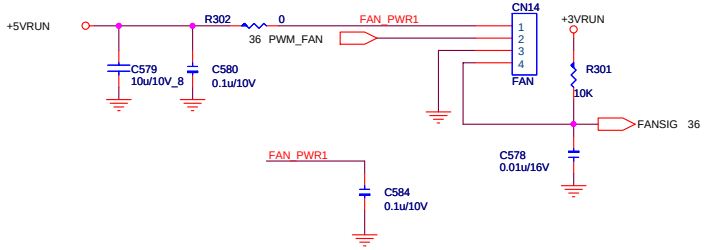


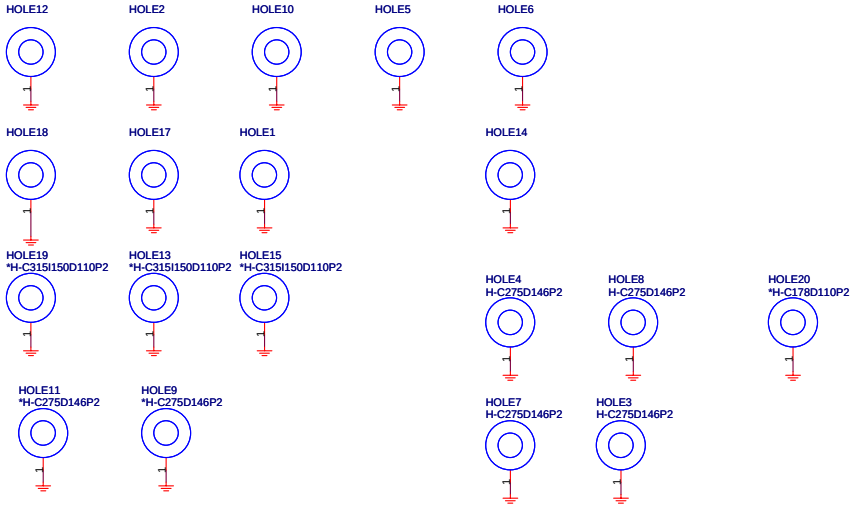


PROJECT : TW3		
Quanta Computer Inc.		
Size	Document Number	Rev
	BT,NEW CARD,MINI PCIE	B1A
Date: Thursday, March 09, 2006	Sheet 33 of 47	

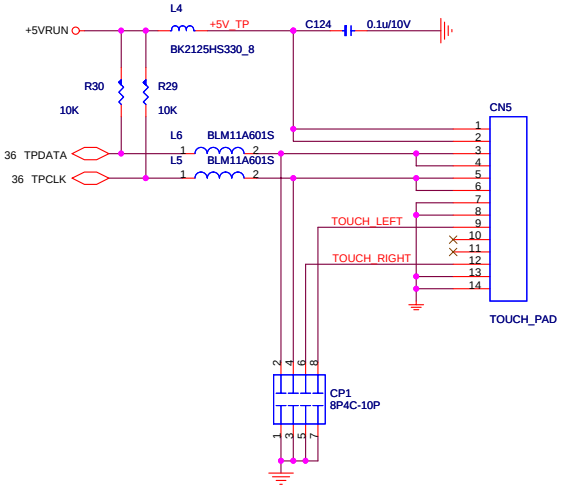
KeyBoard Interface

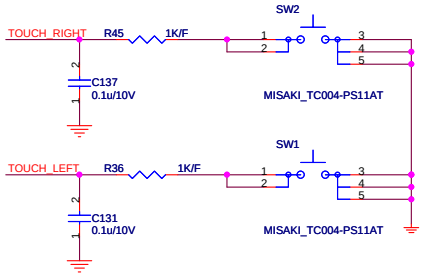






TOUCH PAD

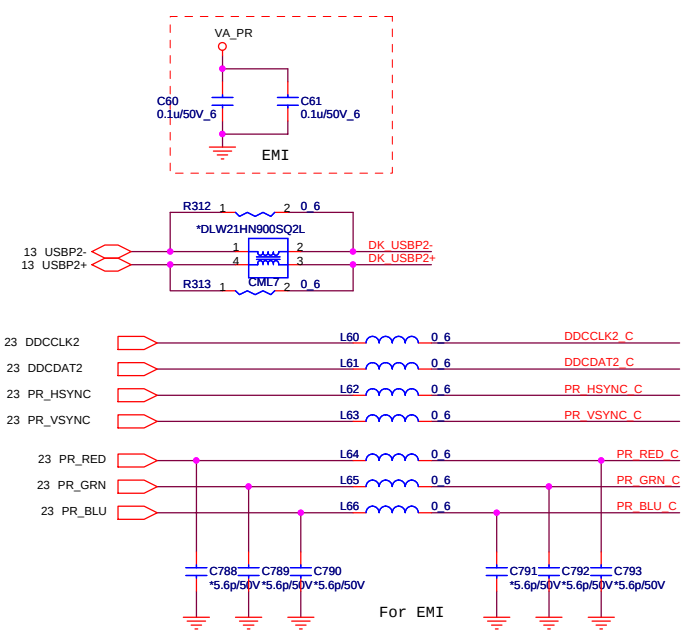


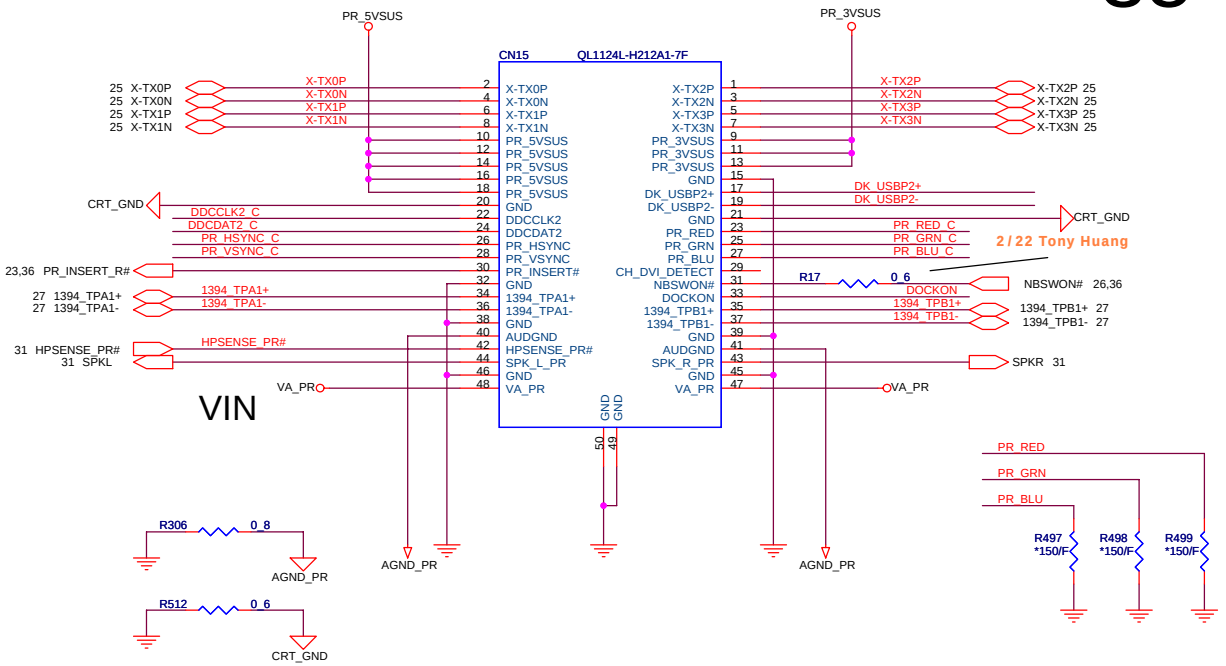


PROJECT : TW3
Quanta Computer Inc.

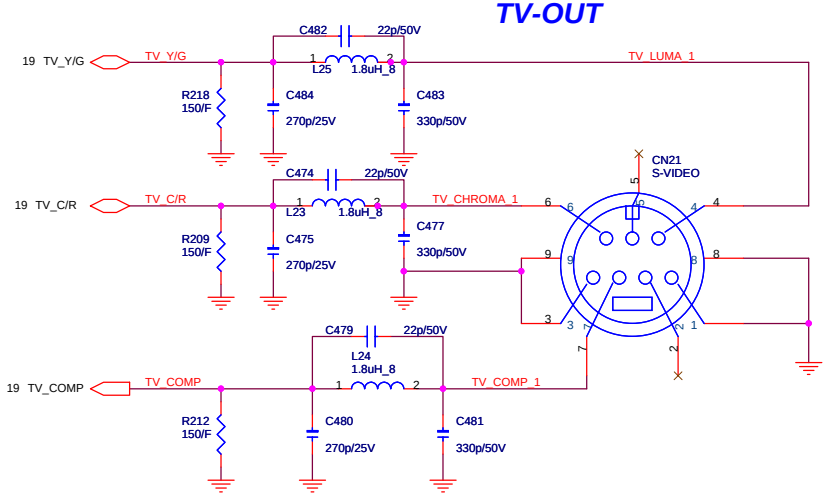
Size	Document Number	Rev
	T/P,FAN,KB	B1A
Date: Thursday, March 09, 2006	Sheet 34 of 47	

CABLE DOCKING CONNECTOR





TV-OUT



CX8PG181001 (180 ohm ,1.5A)

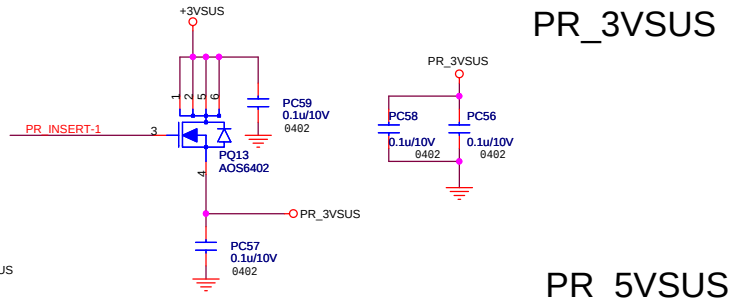
CH00606TB04 CH00606TB04

Intel CRB

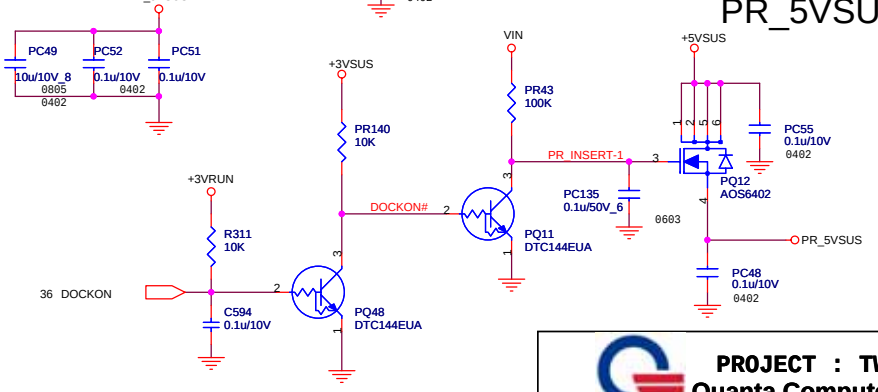
150 ohm@ 100MHZ
(100mA)

6pf 16V 6pf 16V

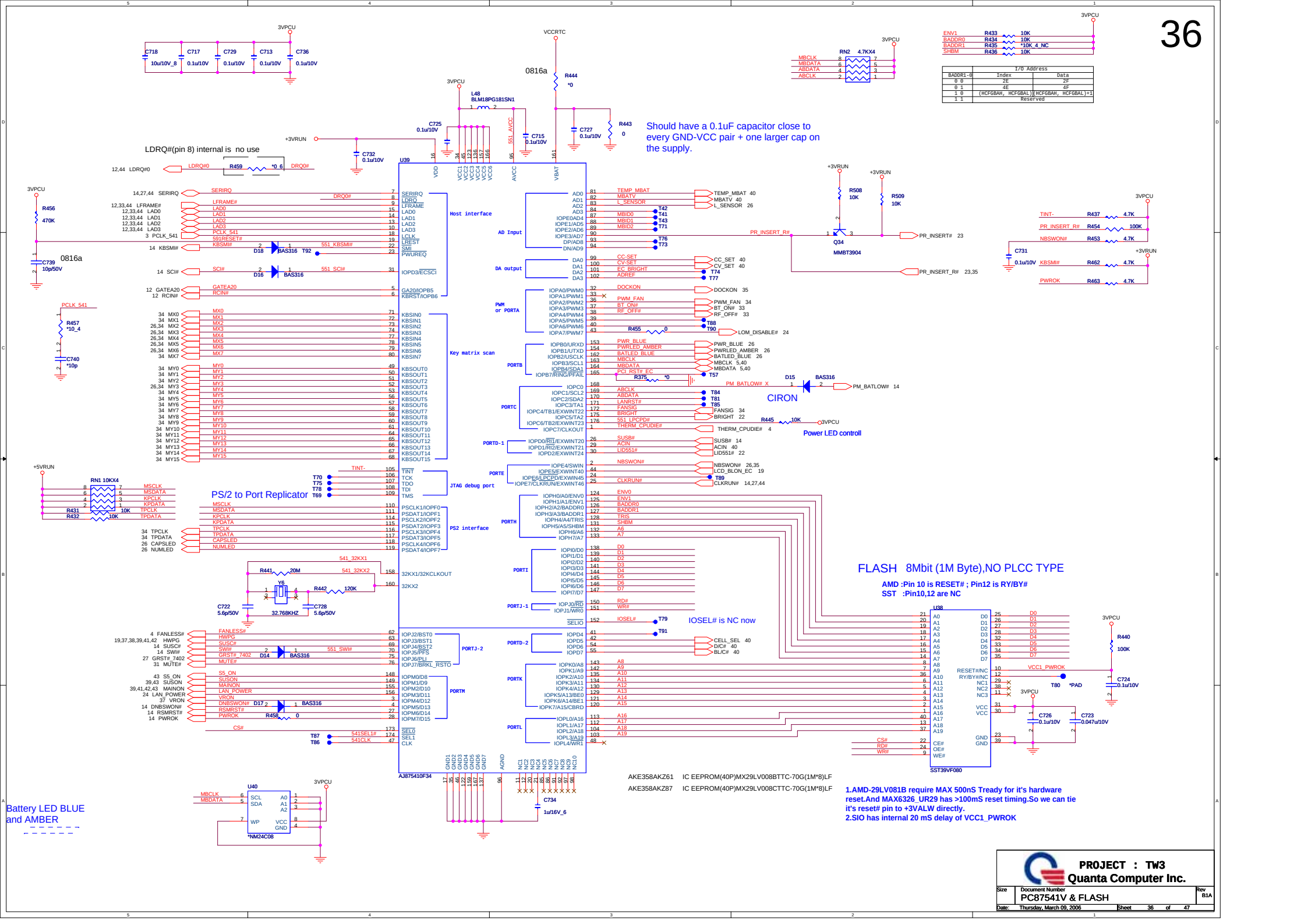
PR_3VSUS

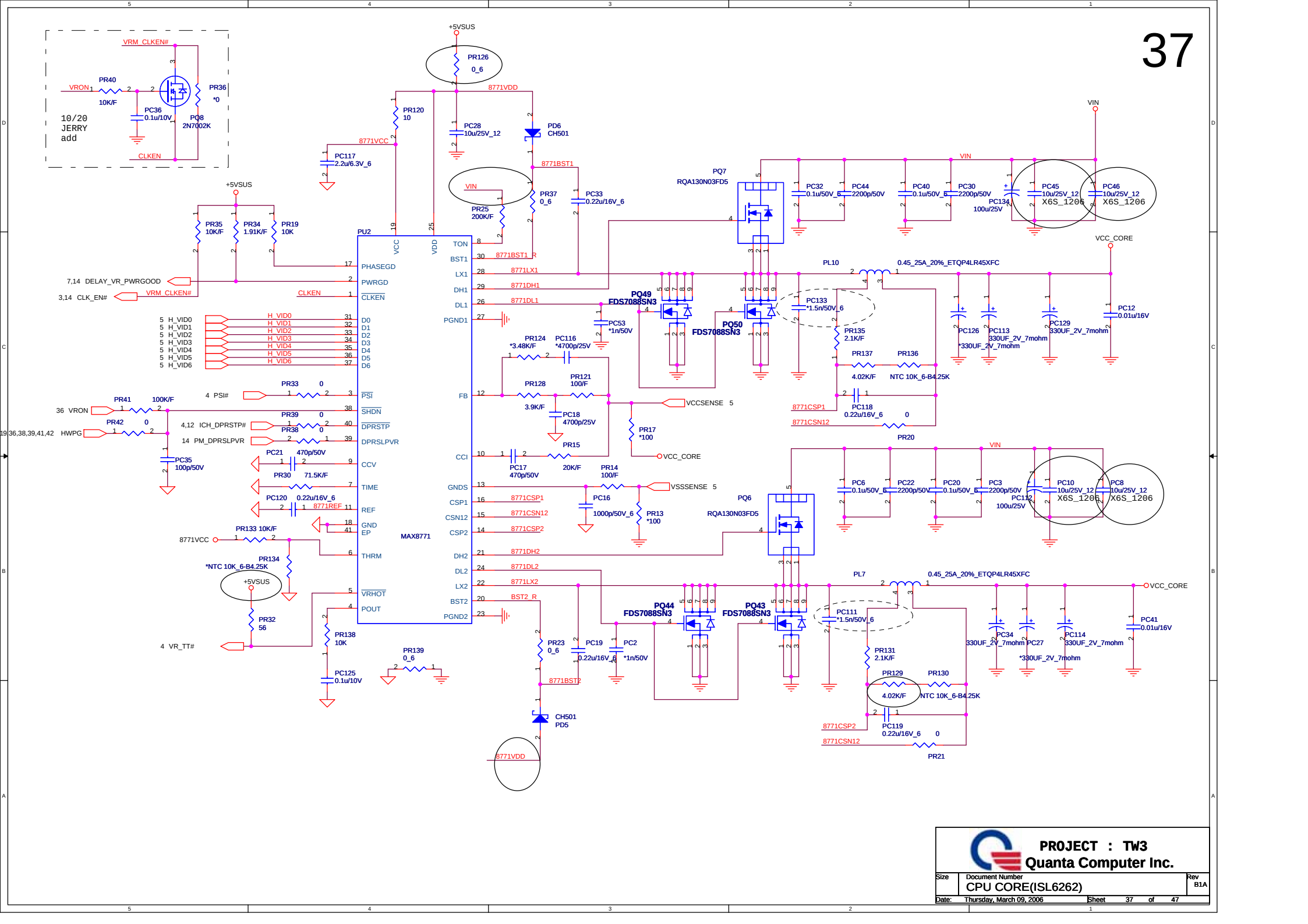


PR_5VSUS

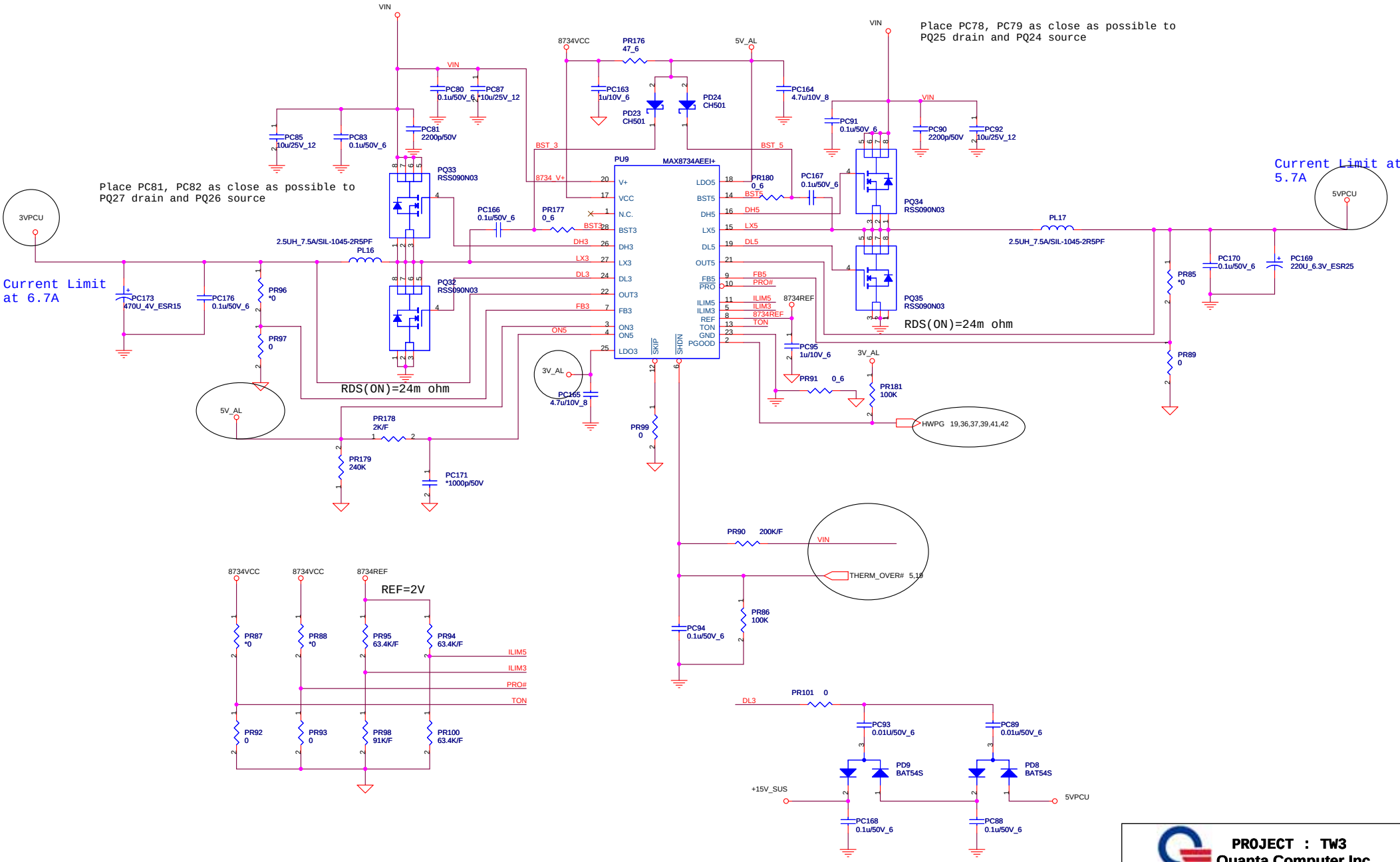


	PROJECT : TW3 Quanta Computer Inc.	
Size	Document Number PORT REPLICATOR	Rev B1A
Date: Thursday, March 09, 2006	Sheet 35 of 47	


Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.
LDRQ#(pin 8) internal is no use
Host interface
AD Input
DA output
PWM or PORTA
Key matrix scan
PORTB
PORTC
PORTD-1
PORTE
JTAG debug port
PS2 interface
PORTH
PORTI
PORTJ-1
PORTD-2
PORTJ-2
PORTK
PORTM
PORTL
CIRON
Power LED controll
PS/2 to Port Replicator
IOSEL# is NC now
FLASH 8Mbit (1M Byte),NO PLCC TYPE
AMD :Pin 10 is RESET# ; Pin12 is RY/BY#
SST :Pin10,12 are NC
Battery LED BLUE and AMBER
AKE358AKZ61 IC EEPROM(40P)MX29LV008BTTC-70G(1M*8)LF
AKE358AKZ87 IC EEPROM(40P)MX29LV008CTTC-70G(1M*8)LF
1.AMD-29LV081B require MAX 500nS Tready for it's hardware reset.And MAX6326_UR29 has >100mS reset timing.So we can tie it's reset# pin to +3VALW directly.
2.SIO has internal 20 mS delay of VCC1_PWROK
PROJECT : TW3
Quanta Computer Inc.
PC87541V & FLASH
Thursday, March 09, 2006



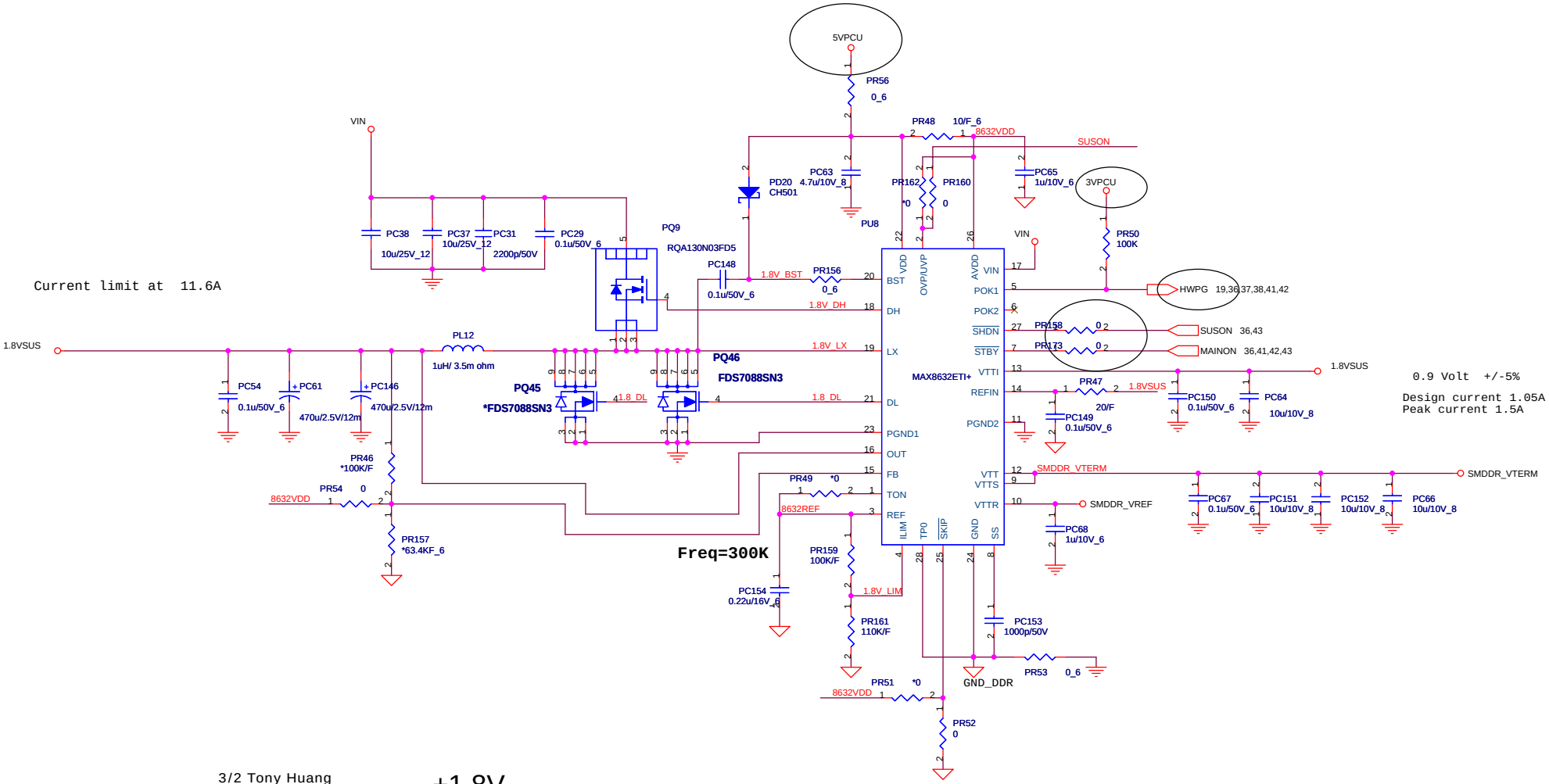
PROJECT : TW3		
Quanta Computer Inc.		
Size	Document Number: CPU CORE(ISL6262)	Rev: B1A
Date: Thursday, March 09, 2006	Sheet 37 of 47	

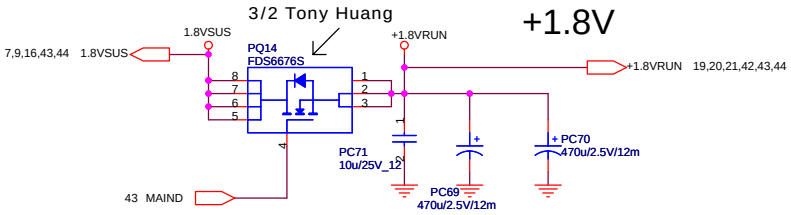


PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	5V/3.3V(TPS51120)	B1A

Date: Thursday, March 09, 2006 Sheet 38 of 47





PROJECT : TW3		
Quanta Computer Inc.		
Size	Document Number: 1.8VSUS/+0.9TERM/+2.5VSUS	Rev: B1A
Date: Thursday, March 09, 2006	Sheet 39 of 47	

Iinput =(V CLS / V REF)*(0.075/ RS1)

ICHG =(V ICTL / V REFIN)*(0.075/ RS2)

CELL-SET
0 = 4 CELL
1 = 3 CELL

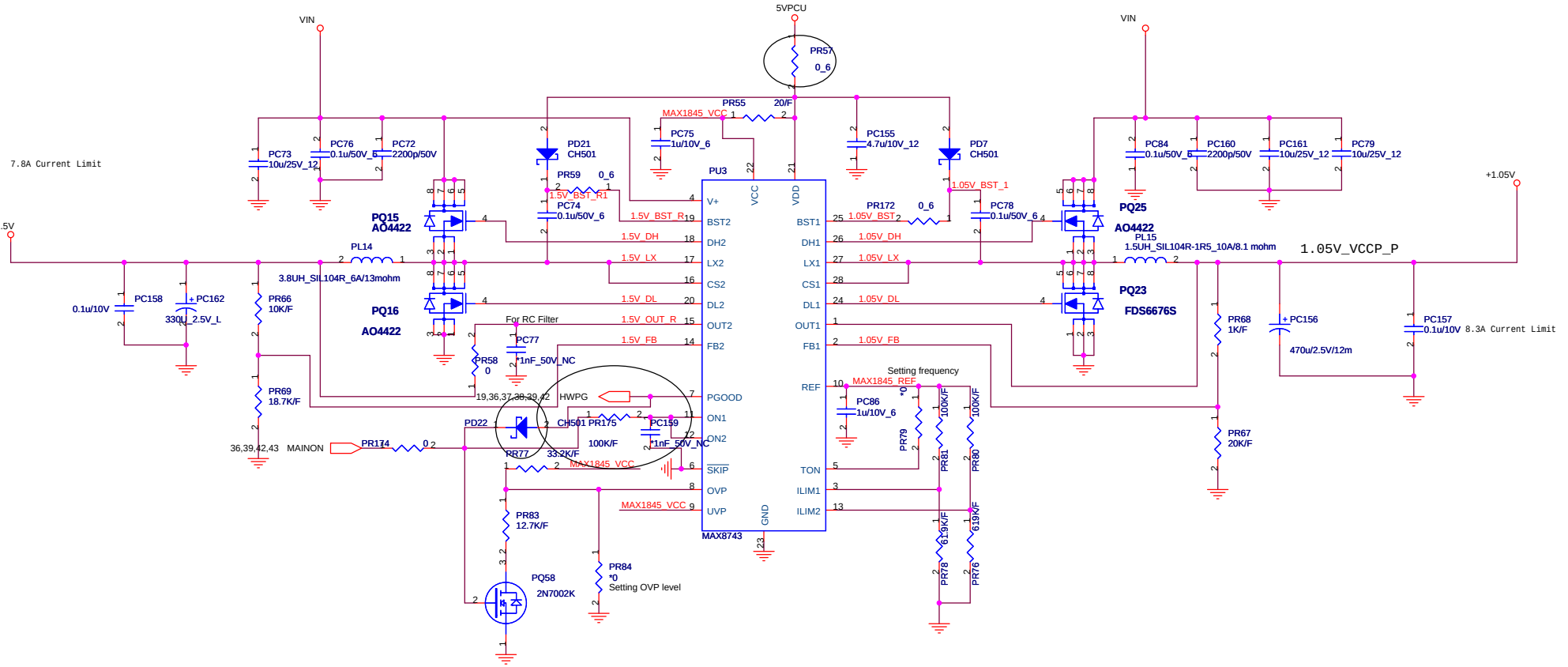
300mil

PU1 MAX8724

PROJECT : DW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CHARGER	B1A
Date: Thursday, March 09, 2006	Sheet 40 of 47	

AO4422: Id= 11A, Rdson= 24m ohm, Qg= 19.8nC
FDS6676S: Id= 14.5A, Rdson= 7.25m ohm, Qg= 43 nC



PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	1.05V&1.5V	B1A
Date: Thursday, March 09, 2006	Sheet 41 of 47	

13,14,25,27,30,33,35,43,44 +3VSUS +3VSUS
25,26,35,37,43,44 +5VSUS +5VSUS
22,24,35,37,38,39,40,41 VIN VIN

RQW130N03: Id= 13A, Rdson= 17.1m ohm, Qg= 12.6nC
RQW200N03: Id= 20A, Rdson= 5.6m ohm, Qg= 40 nC

CHOKE: 0.56U +-20% 15A(ETQP4LR56WFC) 1.6m ohm +/-5%

1.0V/ 9.3A/ OCP= 13A

+VCC_GFX_CORE

VIN, VIN_1993, PL2 HI0805R800R-10

PC42 10u/25V_12, PC47 10u/25V_12, PC50 0.1u/50V_6, PC39 2200p/50V

PC132 0.1u/50V_6

PC43 330U_2V_9m, PC130 330U_2V_9m

PL9 0.56uH/ 1.6m ohm

PR31 1.62K/F

PC138 0.22u/25V_6

PQ10 RQA130N03FD5

PQ47 RQW180N03

PC136 0.1u/50V_6

PD19 CH501

PC60 1u/10V_6

PR145 0_6

PR146 20_6

PC142 1u/10V_6

PR141 0_6

PR44 0_6

PU6 MAX1993ETG

VDD, VCC, V+, POK, BST, DH, LSAT, SHDN, LX, GATE, REFIN, DL, GND, CSP, CSN, OUT, FB, OVP/UVP, SKIP, FBLANK, ILIM, OD, TON, REF

VGA_BST, 1993_DH, 1993_LX, 1993_DL, 1993_CSP, VGA_P_VCC, VGA_REFIN, VGA_P_REF

+3VRUN

PR154 100K/F

HWPG 19,36,37,38,39,41

PC144 0.1u/50V_6 3/9 Tony

PR151 0

MAINON 36,39,41,43

PR147 *0

V_PWRCNTL 19

PR150 75K

PR45 75K

PC143 470p/50V

PR148 20K/F

PR152 *0

V_PWRCNTL:
High(3.3V) = 1.0V
Low(0V) = 1.1V

PR155 137K/F_6

PC62 1u/10V_6

PR144 0

PC147 470p/50V

PR153 20K/F

Iout_max = 13.4A

Tony Huang 3/2

	NV72M:1.1V G72M:	NV72MV:1.0V
PR150	75K	75 K
PR45	75K	75K
PR148	20K	0 ohm
PR147	NC	NC

+1.2V_VPCIE

1.2V/ 2A

+1.8VRUN, +5VRUN

PL13 HI0805R800R-10

PR149 0

PU7 APL5331

VIN, VOUT, VCNTL, NC, VREF, NC, GND1, NC, AGND, GND

VCNTL 1.2VA

PR142 10K/F

PR143 20K/F

PC137 10u/10V_8, PC145 1u/10V_6

PC141 1000p/50V_6, PC140 10u/10V_8, PC139 10u/10V_8

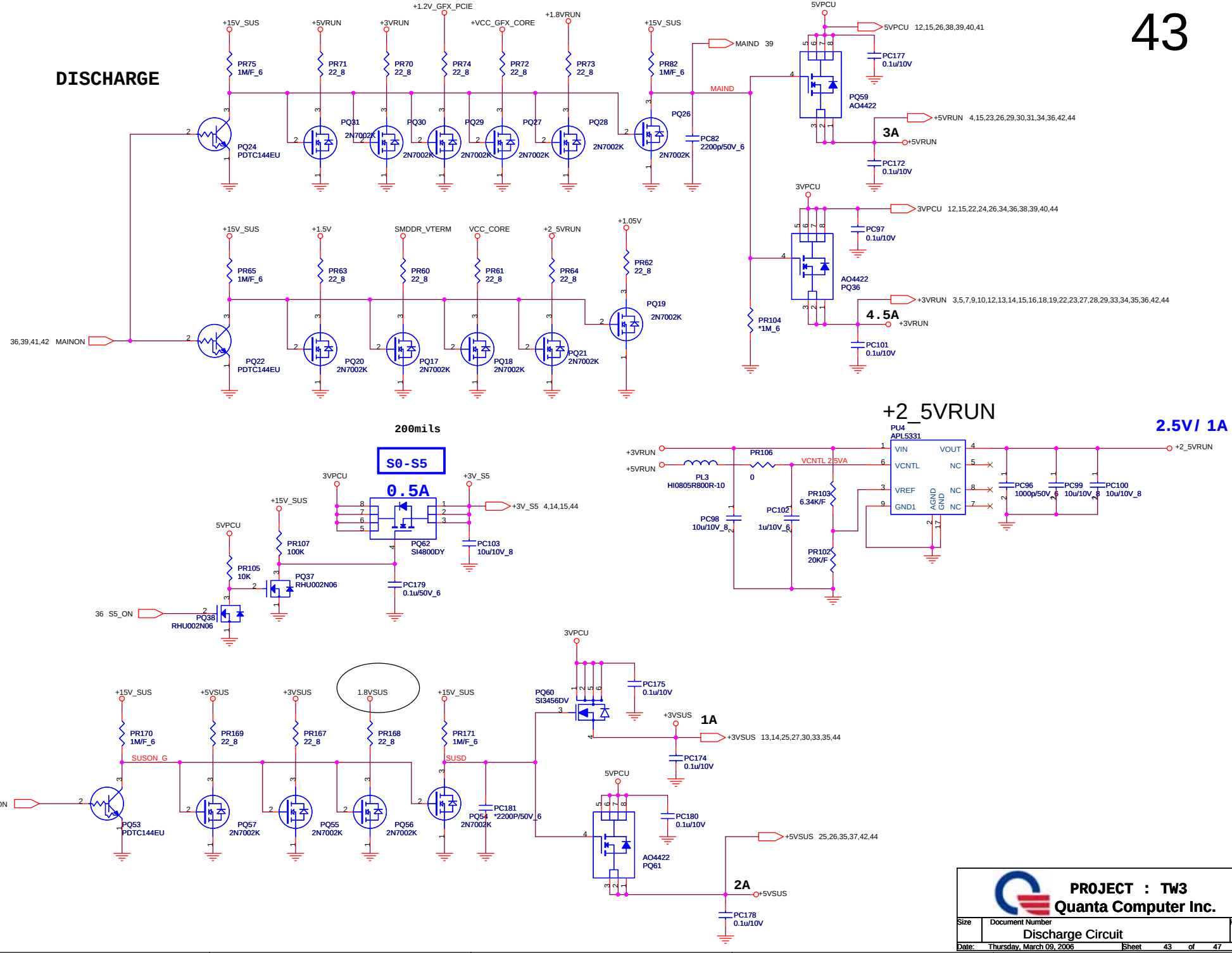
+1.2V_GFX_PCIE

PROJECT : TW3
Quanta Computer Inc.

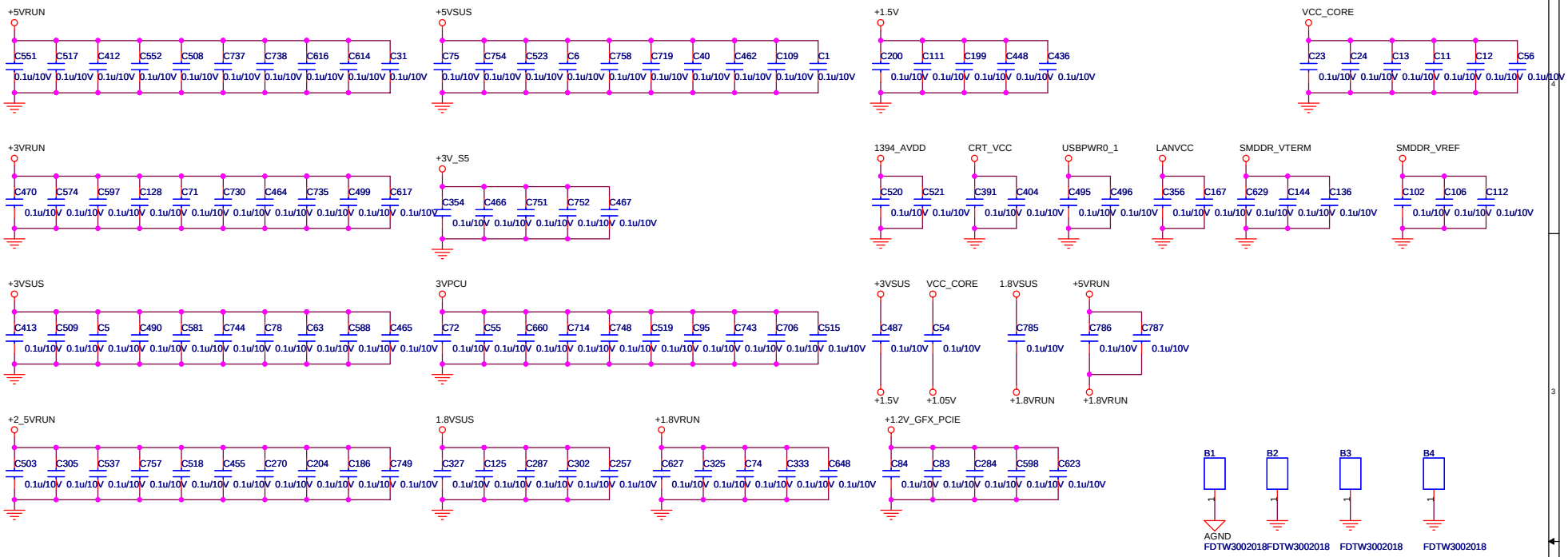
Size	Document Number	Rev
	VGA CORE	B1A

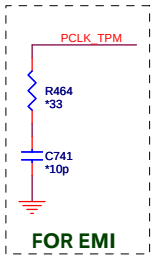
Date: Thursday, March 09, 2006 Sheet 42 of 48

DISCHARGE



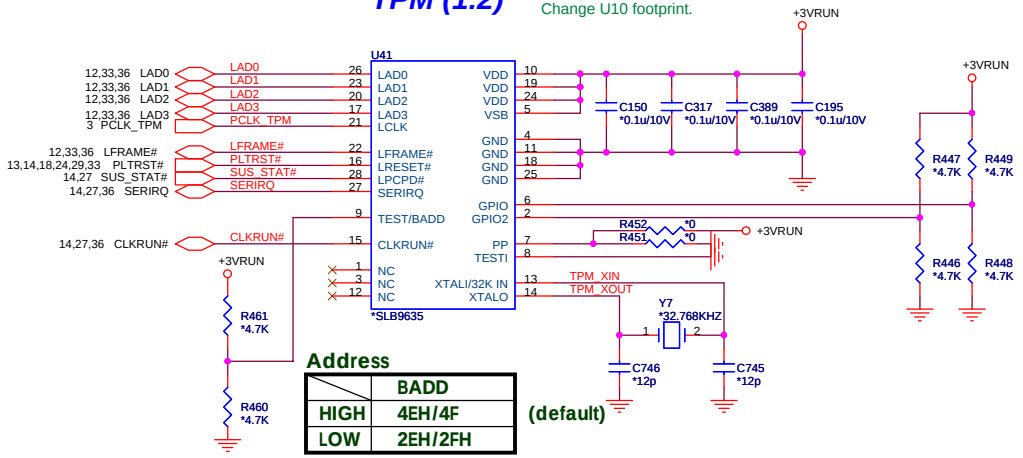
PROJECT : TW3		
Quanta Computer Inc.		
Size	Document Number	Rev
	Discharge Circuit	B1A
Date: Thursday, March 09, 2006	Sheet 43 of 47	





TPM (1.2)

B stage:
Change U10 footprint.



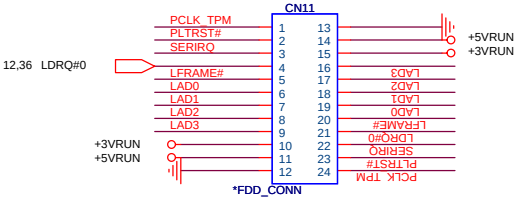
Address

	BADD
HIGH	4EH/4F
LOW	2EH/2FH

(default)

B stage:
Change U10 Footprint

Debug Conn.



PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	EMI & TPM & Debug Conn	B1A
Date: Thursday, March 09, 2006	Sheet 44 of 47	

MODEL	REV	CHANGE LIST		
TW3A		Page	Description	
	B to 1223	Page 29	Change R472 to NI for SATA,install for PATA to solve sometimes ODD can't be detected and slow boot..	
		Page 33	Add R481,R480 to solve WLAN LED light leakage.	
		Page 3	Change R177 to install and pull low to set VGA clock to 100MHz.	
		Page 19	Change R345 to install to solve back light can't enable.	
		Page 29	Change R245 to NI for SATA,install for PATA.	
		Page 14	Add R482,R483 for CRT/DVI option.	
		Page 24	Change C645 to 10uF for LAN 1.2V per Marvell recommendation.	
		Page 19	R377 to install,R362,R364,R365 to NI. (Set default to G72M)	
		Page 30	3V_DVDD connect to +3VSUS to solve WOR.	
	1223 to 1224	Page 32	Change MQ1,MQ2,MQ3,MQ4 to BA000420Z07 to solve MODEM low performance.	
		Page 37	Delete short pad.	
		Page 38	Delete short pad.PC92 change to install.	
		Page 39	Delete short pad.	
		Page 41	Delete short pad.	
		Page 42	Delete short pad.PR45,PR150 change to 75K(CS37502FB04).	
		Page 43	Delete short pad.	
		Page 5	R19 change to NI for solving power-on shutdown.	
		Page 34	HOLE,3,HOLE4,HOLE7,HOLE8 change to MBRW1003011.	
		Page 40	PR110 change to CS+0158JL11.PR132 change to 24.9K.	
		Page 37	PC34,PC113,PC114,PC129 change to CH733RM8831.	
		Page 23	F1 change to DK100TPU028.	
		Page 33	Q17 change to install for BT LED control.	
		Page 34	Change CN4 footprint to "afn250-a2g1t-25p-l" for SMT issue.	
		Page 26	Change CN1.4 connection to RF_LED.	
		Page 33	Add NET RF_LED.	
		Page 36	Delete NET TUCHLED.	
		Page 31	Change C541,C546 to X7R for audio precision.	
	1223 to 1226	Page 38	Change PC93,PD9,PC168 to install. Delete NET 10V.	
		Page 41	Change NET 10V to +15V_SUS.	
		Page 26	LED2,LED3 change to dual color type(cost down and unify brightness and color).	
		Page 12	Reserve C784 on THERMTRIP for ESD.	
		Page 35	Reserve R497,R498,R499 for TW2 PR.	
		Page 33	Delete RP45,RP46,R210 for layout problem.	
	1226 to 1227	Page 33	Change CN23 to Molex (same as SW1). Add CN31 PCIE latch.	
		Page 44	Add EMI spring B1,B2,B3.	
		Page 32	Install MC8,MC9 for EMI.	
		Page 12	Change C459 TO 22pF for EMI.	
		Page 31	R479,R281,R295 change to install for EMI.	
	1227 to 1228	Page 44	Add B4,C785,C786,C787 for EMI.	
		Page 19	Reserve R504,R505,R506,R507 for DVI EMI.	
		Page 3	Change Y1 P/N to BG614318081(CL=20pF) for solving system time delay issue.	
		Page 23	Change C694,C701,C703 to NI for signal quality.	
		Page 36	RN2 change to 4.7K for IIC signal quality.	
		Page 30	C528,C529 change to 1uF/10V X5R for audio precision.	
		Page 35	Add L60~L66,C788~C793 for EMI.	
	1227 to 1230	Page 26	Change CN9,CN12 P/N to DFHS04FRE80.	
		Page 36	Delete D13, add R508,R509,Q34 for PR leakage current. R454 change to 100K.	

Model	TW3 M/B	
Page	From	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	
16	1A	
17	1A	
18	1A	
19	1A	
20	1A	
21	1A	
22	1A	
23	1A	
24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	
31	1A	
32	1A	
33	1A	
34	1A	
35	1A	
36	1A	
37	1A	
38	1A	
39	1A	
40	1A	
41	1A	
42	1A	
43	1A	
44	1A	
45	1A	

PROJECT : TW3
Quanta Computer Inc.

Size	Document Number	Rev
	Change List (B2A)	B1A
Date: Thursday, March 09, 2006	Sheet 45 of 47	

PROJECT: TW3	PCBA NO.	REV: 2B	DOC. NO :	
APPROVED BY : Johnson Hsu	CHECK BY : Titan Chiang	DRAWING BY : Tony Huang	DATE :05/05/2005	SHEET 1

MODEL	REV	CHANGE LIST		
		Page	Description	
TW3A				
	1230 to 0102	Page 38	PC173 change to 470uF.	
		Page 39	PC66 change to install.	
		Page 42	PR153 change to 20K.	
		Page 41	PD7,PD21,PD22 change to CH501.	
		Page 37	PD6,PD5 change to CH501.	
		Page 42	PQ47 change to RQW180N03.	
		Page 26	CN12,CN9 USB connector change to DIP type.	
		Page 29	CN25 pin25,26 and CN24 pin47,48 disconnect to GND.	
		Page 23	CN6 pin27,28 disconnect to GND.	
		Page 34	SW1,SW2 P/N change to DHP00FC1G16.	
		Page 36	Change R454 to 100K,R508,R509 to 10K.	
	0102 to 0103	Page 4	R101,R97,Q11 change to install.	
		Page 6,7,8,9,10,11	Change U32 P/N to AJSL8Z40T26.(945PM)	
		Page 12,13,14,15	Change U36 P/N to AJSL8YB0T12.(ICH7M)	
		Page 37	PR128 change to 3.9K.	
	0103 to 0105	Page 45,46	Update change list.	
		Page 27	Change J1 P/N to DFHS04FRE47.	
		Page 35	Change CN15 to install and P/N to DFHS48FR001	
		Page 44	Change B1,B2,B4 P/N to FDTW3002018.	
		Page 36	U38 P/N change to AKE35ZAKK17.	
		Page 42	PR45,PR150 P/N change to CS37502FB12.	
	0105 to 0111	Page 30	Change C528,C529 to 2.2uF/6.3V for audio precision.	
C1 TO C2				
	0111 to 0119	Page 19	Change R26 to 0 ohm and change connection to THERM_OVER#.	
		Page 23	Q21 mirror vertical.	
		Page 23	Add C794~C799, L67~L69 for EMI.	
		Page 23	L46,L44,L42 change to 0 ohm. C700,C702,C705 change to NI for EMI.	
		Page 32	Change MR5,MR6,MR,MR10 to 280ohm. Add MR11,MR12,MR13. Change MR8 to NI.	
		Page 35	R17 change to install.	
		Page 35	CN15.21,22 change to CRT_GND. Add R512 for EMI.	
		Page 35	Change D1 to page23 and its connection and to NI.	
		Page 41	PL14 P/N change to DC-38600001.	
		Page 43	PQ59,PQ61,PQ36 P/N change to BAM44220002.	
		Page 36	RN2 P/N change to CJ247084N25.	
		Page 26	LED4 P/N change to BEBL0002Z62. LED1~3 P/N change to BEAB0013ZA1.	
		Page 33	CN10 P/N change to DFHS26FR489.	
	0119 to 0120	Page 14	Change R368 to install,R366 to NI to set w/ docking.	
		Page 27	Change D7 to install to solve 7402 does not work.	
		Page 19	Delete R410,R413,R417 for EMI layout.	
		Page 23	Correct CN6 C1~C4 pin define.	
		Page 23	Reserve Q37,Q38,RP56,R513,R514 for DVI disable when docking attach.	
		Page 29	CN25 footprint change to "SATA-C16647-122A4-B-22P-R-V" for SMT issue.	
C2 TO C3	0120 to 0209A	Page 25	LAN active/link LED change to +3VSUS.	

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Page	From	To
1	1A	
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	Change List (B2A)	B1A
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APPROVED BY : Johnson Hsu	CHECK BY : Titan Chiang	DRAWING BY : Tony Huang	DATE :05/05/2005	SHEET 1

A. G72M to G72MV

1. change P/N to G72MV (AJ073000T14)
2. Set VGA core to 1.0V fix.
3. Change PCI_DEVID.

B. VRAM 128MB to 64MB

1.follow config table to set RAM_CFG.
2.Change VRAM P/N to HYNIX.
3.VRAMx2

C. LAN GIGA to 10/100.

1.Change LAN chip to 8038(AJ080380000).
2.Change Rset resistor.
3.Change transformer.

D. SATA to PATA

1.Set ODD to slave.
2.Set HDD to master.
3. Remove SATA conn.
4. Add PATA conn.
5. Change board ID to PATA.
6. Install resistor to connect ODD and HDD LED.
7. NI resistor of SATA LED.

E. docking to no docking.

1.Set board ID4 to low.

MODEL	REV
TW3A **C2 to C3**	0209 to 0222A

CHANGE LIST

Page	Description
Page 23	**(1)** CN20 pin 12,15 change connect to DVI_DDCDAT,DVI_DDCCLK **(In C1 was connect to DDCCLK2,DDCDAT2)**
	(2) R150,R159,Q37,Q38,RP56 Change to install for DVI,CRT I2C,D1 change to NI
	(3) Change L67,L68,L69 P/N from CX8BB121002 to CX8BB470007
	(4) Change C794,C795,C796 P/N from CH01806JB07 to CH01006JB08
Page 27	**(1)** Change R208 pin1 contact to +3VRUN
	Change R208 P/N to CS31002JB28,C473 change to CH4102K1B03 ,D7 change to NI.
Page 31	**(1)** Change L50,L51,L52,L53 P/N from CS00003J951 to CX0HM121008
	(2) Add C759,C760,C761,C762 to install (CH02206GB02)
Page 34	**(1)** RP47,RP48,RP49 change to CJ3100A8N21(meet Rohs)
Page 42	**(1)** Change PR147 to NI

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APPROVED BY : Johnson Hsu	CHECK BY : Titan Chiang	DRAWING BY : Tony Huang	DATE :05/05/2005	SHEET 1