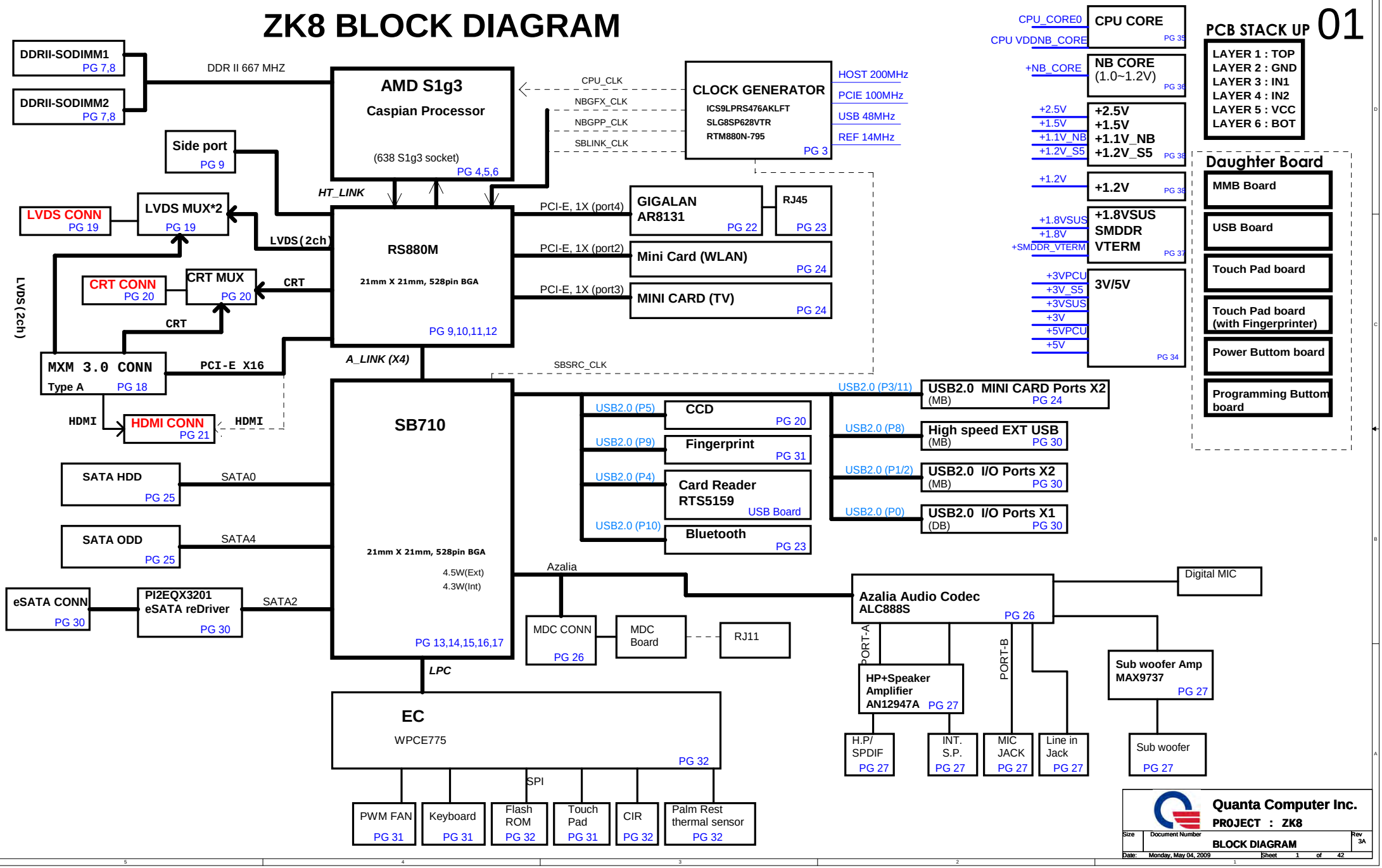
ZK8 BLOCK DIAGRAM

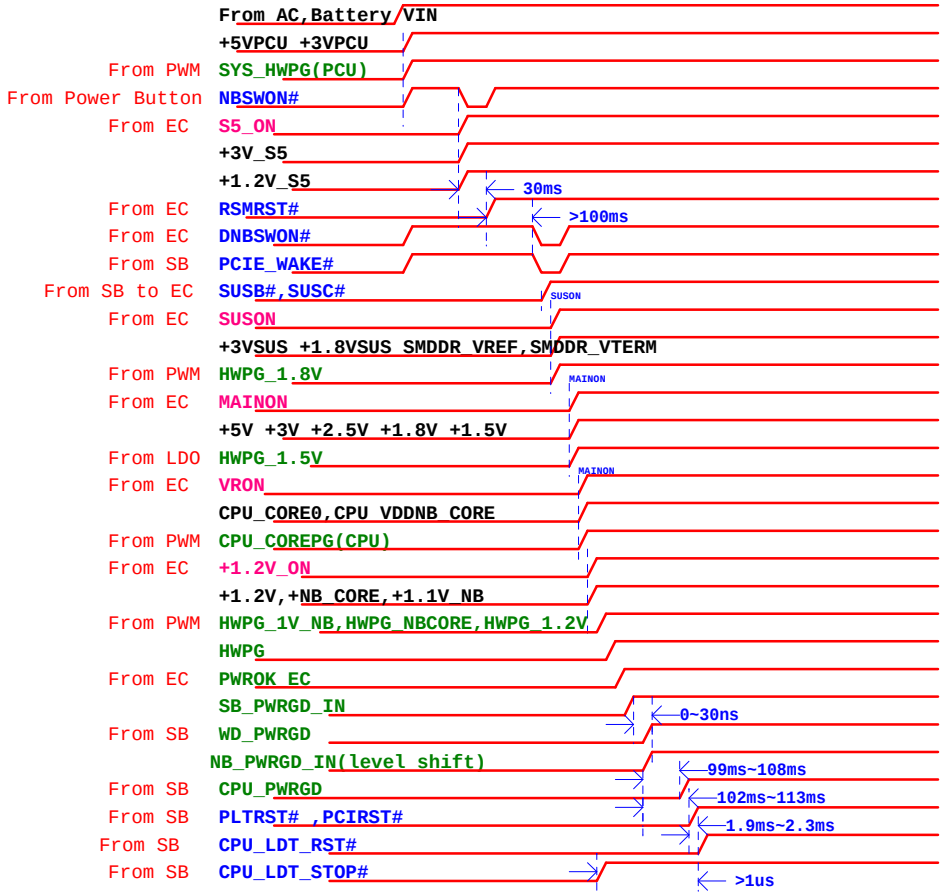


Quanta Computer Inc.
PROJECT : ZK8

Size	Document Number	Rev
	BLOCK DIAGRAM	3A

Date: Monday, May 04, 2009 Sheet 1 of 42

ZK8 Power On Sequence



BOM naming rule

Items	Function	BTO	Name	Description
1	CIR	v	CIR@	
2	HDMI port	v	HDM@	
3	HDMI transmitter	v	SI@	Silicon image SiI 1392/1932
4	HDMI-CEC	v	CEC@	Renesas R8C/1B
5	Discrete VGA		EV@	External VGA stuff
6	UMA		IV@	Internal VGA stuff
7	New Card		NEW@	
8	RJ11	v	MD@	Modem
9	RJ45-10/100		40@	Marvell 8040T(10/100)
10	RJ45-1000		55@	Marvell 8055(Giga)
11	Option for RJ45-10/100 and RJ45-1000		40@55@	Option for 8040/8055
12	TV	v	TV@	
13	Cardbus		CB@	
14	FM transmitter	v	FM@	
15	Mainstream ID LED		MID@	
16	Low cost ID LED		LID@	
17	CCD	v	CCD@	
18	INT MIC	v	I_MIC@	
19	AMD Hyper Flash		HF@	Only for AMD platform
20	North bridge(690MC/RS780MC)		MC@	Only for AMD platform
21	North bridge(RX780)		RX@	Only for AMD platform
22	PowerXpress		PX@	Only for AMD platform
23	PowerXpress with UMA SKU		PX@IV@	Only for AMD platform
24	PowerXpress with Discrete VGA SKU		PX@EV@	Only for AMD platform
25	Power player/Power Shift		PP@	Only for AMD platform

***Note: EC will sampling SUSB# & SUSC# every 5ms.**

AMD SB710 SMBUS Table

	CLK GEN	RAM	Mini Card TV)	Mini-card(WL)	LAN
SB710 SDATA0/SCLK0(+3V)	V	V	V	V	V
SB710 SDATA1/SCLK1(+3V_S5)					
SB710 SDATA2/SCLK2(+3V_S5)					
Power	+3V	+3V	+3V	+3V	+3V (Atheros)
Reserve MOS ckt	V	X	V	V	X

EC SMBUS Table

	Battery	CPU thermal Sensor	EC EEPROM	VGA thermal Sensor	MMB
EC775 SDATA1/SCLK1(+3VPCU)	V				
EC775 SDATA2/SCLK2(+3VPCU)		V		V	
EC775 SDATA3/SCLK3(+3VPCU)			V		V
EC775 SDATA4/SCLK4(+3VPCU)					
Power	+3VPCU	+3V	+3VPCU	+3V	+3VPCU
Reserve MOS ckt	X	X	X	X	X

Quanta Computer Inc.
PROJECT : ZK8
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CLK_GEN_SLG8SP628(CLK)

ICS9LPRS480 P/N : ALPRS480000

SLG8SP628 P/N : AL8SP628000

RTM880N-796 P/N : AL000880000

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

Add 0216

Add 0226

Add 0216

Add 0217 14.318M for SB

RS780/RX780 for VGA

B2A to C3A

QFN64

SLG8SP628

10/17 Add 10p for EMI issue (Suggestion by Seligo)

CLOCKS name	RX780	RS780	Clock pin function
NBGFX_CLKP NBGFX_CLKN	RP1001 STUFF	RP1001 STUFF	to NB for VGA reference clock
MXM_REFCLKP MXM_REFCLKN	RP66 STUFF	RP66 NC	to M82-S external reference clock -RX780 only
NBGPP_CLKP NBGPP_CLKN	RP1005 STUFF	RP1005 NC	to NB for RX780 for PCIEX2 interface reference clock only RS780 is internal share with AC-LINK clock,RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP1003 STUFF	RP1003 STUFF	to NB for AC-LINK reference clock

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

* default

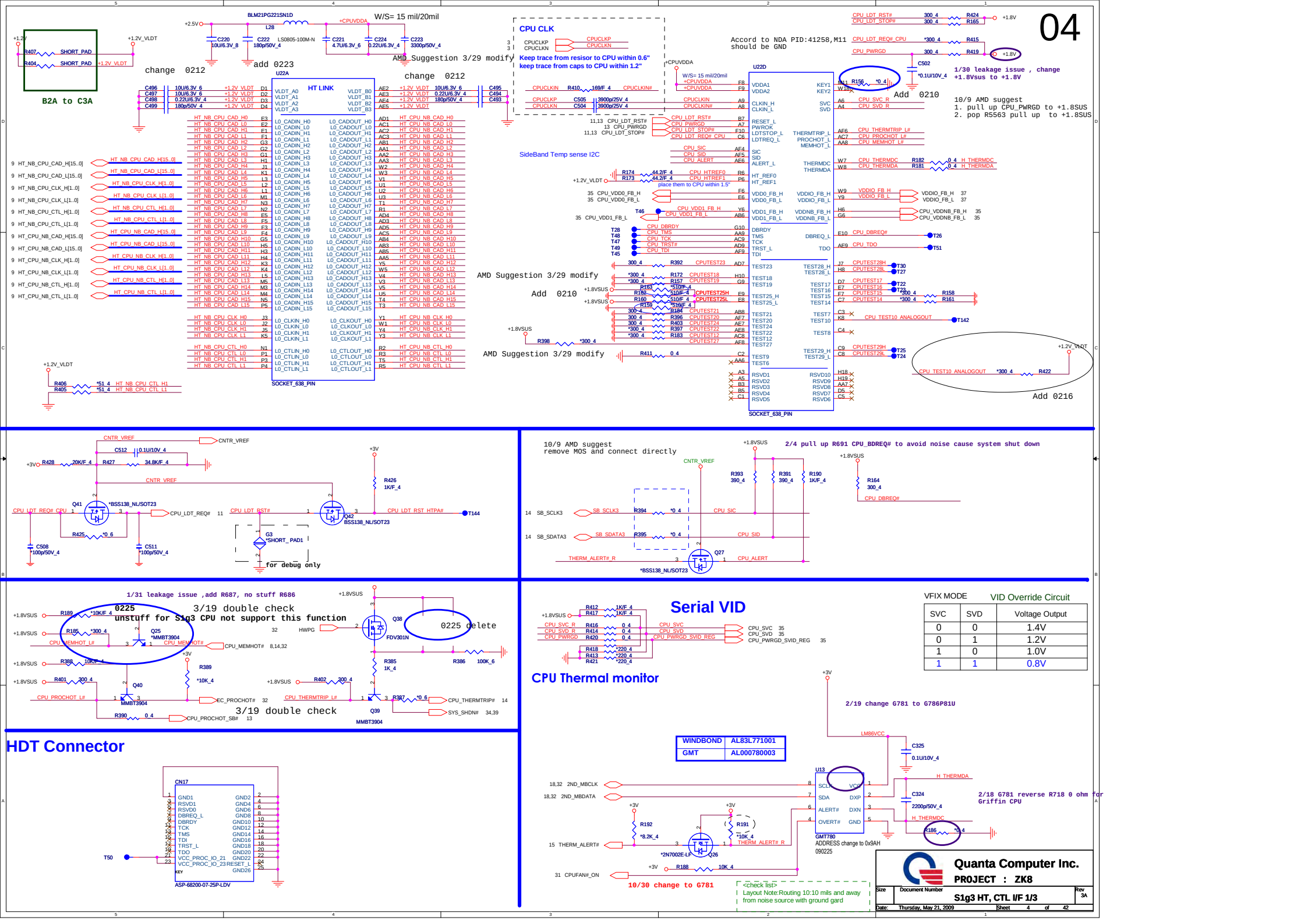
	RX780 1.8V	RS780 1.1V
Ra	82.5R	158R
Rb	130R	90.9R

RES CHIP 130 1/16W +-1%(0402)L-F -->CS11302FB15
RES CHIP 158 1/16W +-1%(0402) -->CS11582FB00
RES CHIP 90.9 1/16W +-1%(0402) -->CS09092FB15
RES CHIP 82.5 1/16W +-1%(0402) -->CS08252FB11

NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

Quanta Computer Inc.
PROJECT : ZK8
Size | Document Number: CLOCK GENERATOR_SLG8SP628 | Rev 3A
Date: Thursday, May 21, 2009 | Sheet 3 of 42


04
B2A to C3A
change 0212
add 0223
W/S= 15 mil/20mil
AMD Suggestion 3/29 modify
change 0212
CPU CLK
Keep trace from resisor to CPU within 0.6"
keep trace from caps to CPU within 1.2"
Accord to NDA PID:41258,M11 should be GND
1/30 leakage issue , change +1.8Vsus to +1.8V
Add 0210
10/9 AMD suggest
1. pull up CPU_PWRGD to +1.8SUS
2. pop R5563 pull up to +1.8SUS
SideBand Temp sense I2C
place them to CPU within 1.5"
AMD Suggestion 3/29 modify
Add 0210
AMD Suggestion 3/29 modify
Add 0216
10/9 AMD suggest
remove MOS and connect directly
2/4 pull up R691 CPU_BDREQ# to avoid noise cause system shut down
for debug only
1/31 leakage issue ,add R687, no stuff R686
0225
3/19 double check
unstuff for S1g3 CPU not support this function
0225 delete
3/19 double check
Serial VID
CPU Thermal monitor
VFIX MODE
VID Override Circuit
SVC SVD Voltage Output
0 0 1.4V
0 1 1.2V
1 0 1.0V
1 1 0.8V
2/19 change G781 to G786P81U
WINDBOND AL83L771001
GMT AL000780003
GMT780
ADDRESS change to 0x9AH
090225
2/18 G781 reverse R718 0 ohm for Griffin CPU
10/30 change to G781
HDT Connector
ASP-68200-07-25P-LDV
<check list>
Layout Note:Routing 10:10 mils and away from noise source with ground gard
Quanta Computer Inc.
PROJECT : ZK8
S1g3 HT, CTL I/F 1/3
Size Document Number Rev 3A
Date: Thursday, May 21, 2009 Sheet 4 of 42

Processor Memory Interface

05

PLACE THEM CLOSE TO CPU WITHIN 1"

750 mA

U22B

MEM:CMD/CTRL/CLK

SOCKET_638_PIN

U22C

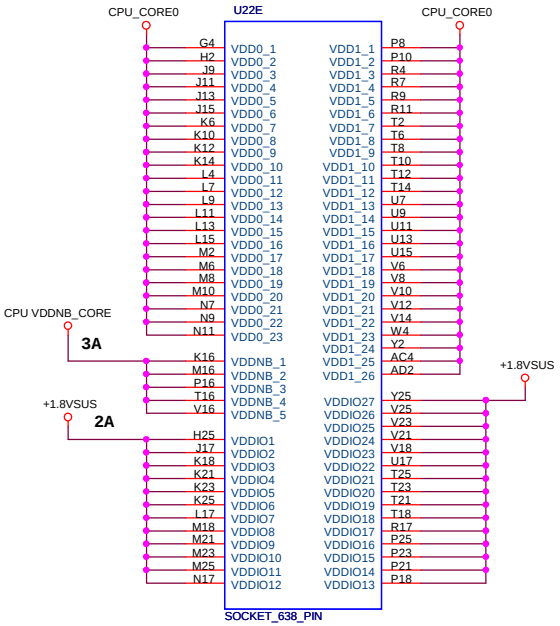
MEM:DATA

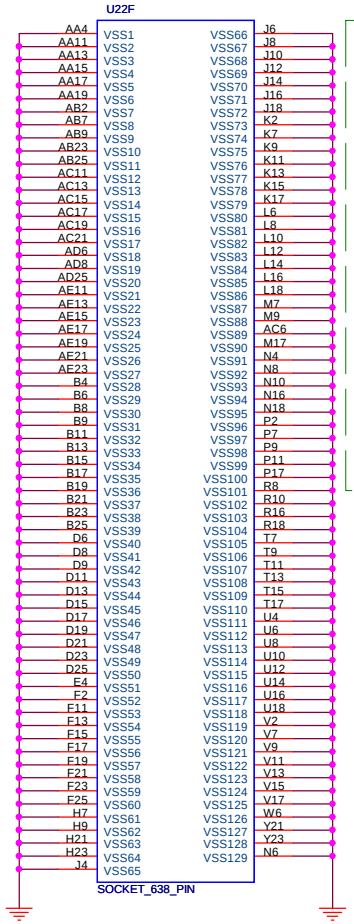
SOCKET_638_PIN

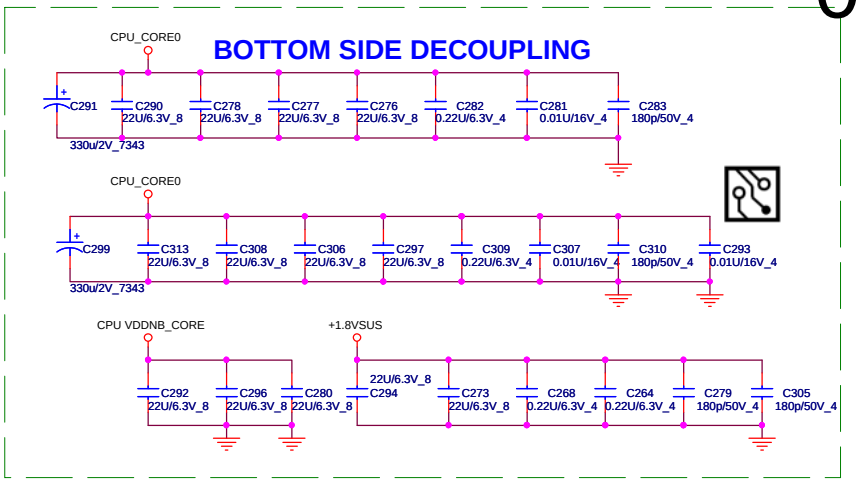
Place close to socket

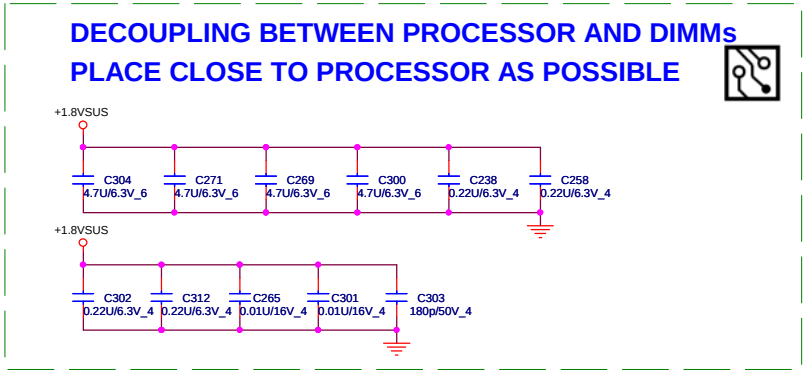
Close to CPU within 1500 mils

Quanta Computer Inc.	
PROJECT : ZK8	
Size	Document Number: S1G3 DDRII MEMORY I/F 2/3 — Rev: 3A
Date: Thursday, May 21, 2009	Sheet 5 of 42



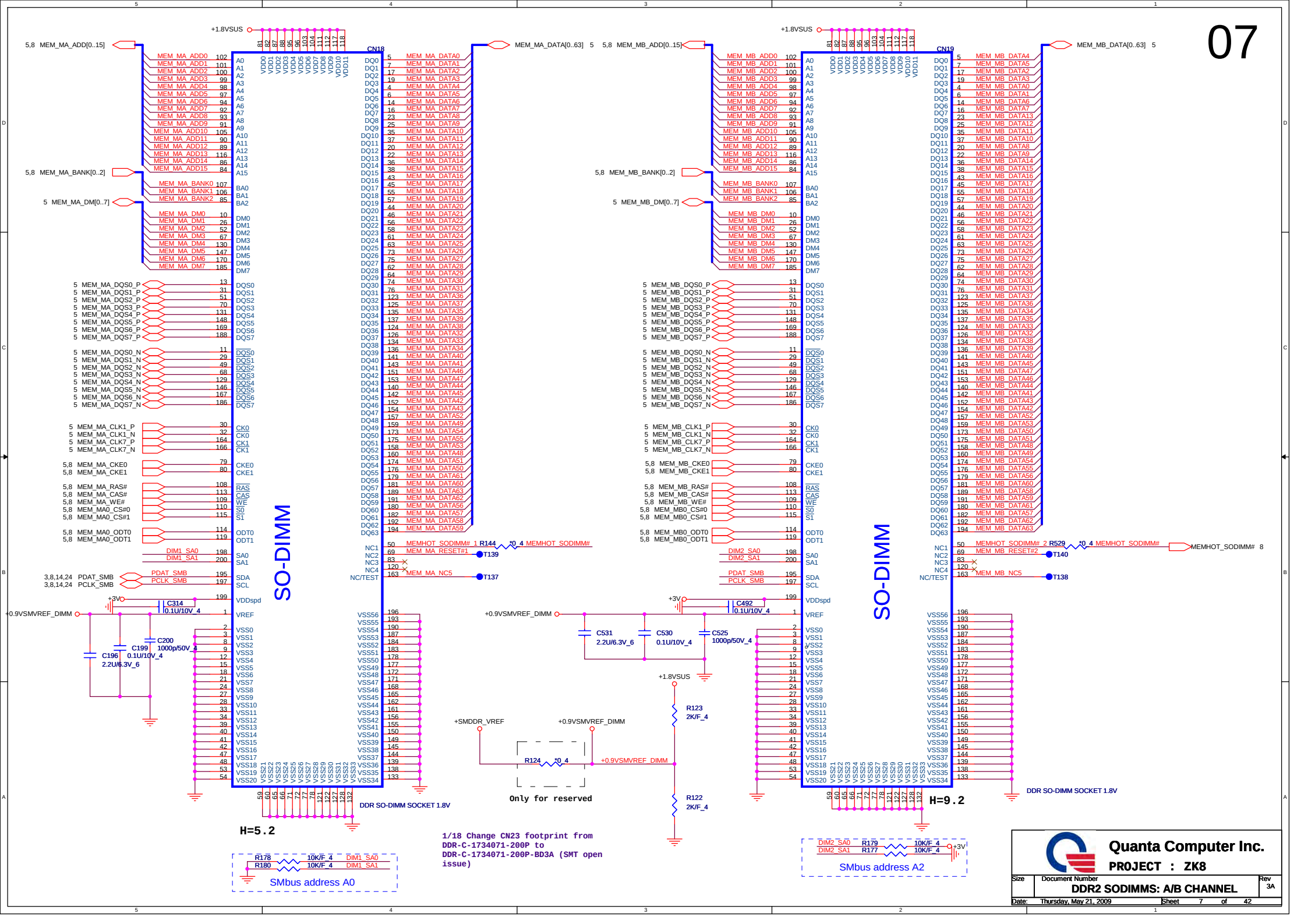






PROCESSOR POWER AND GROUND

Quanta Computer Inc.		
PROJECT : ZK8		
Size	Document Number: S1G3 PWR & GND 3/3	Rev: 3A
Date: Monday, May 04, 2009	Sheet 6 of 42	


+1.8VSUS
CN18
SO-DIMM
5,8 MEM_MA_ADD[0..15]
MEM_MA_ADD0 102
MEM_MA_ADD1 101
MEM_MA_ADD2 100
MEM_MA_ADD3 99
MEM_MA_ADD4 98
MEM_MA_ADD5 97
MEM_MA_ADD6 94
MEM_MA_ADD7 92
MEM_MA_ADD8 93
MEM_MA_ADD9 91
MEM_MA_ADD10 105
MEM_MA_ADD11 90
MEM_MA_ADD12 89
MEM_MA_ADD13 116
MEM_MA_ADD14 86
MEM_MA_ADD15 84
5,8 MEM_MA_BANK[0..2]
MEM_MA_BANK0 107
MEM_MA_BANK1 106
MEM_MA_BANK2 85
5 MEM_MA_DM[0..7]
MEM_MA_DM0 10
MEM_MA_DM1 26
MEM_MA_DM2 52
MEM_MA_DM3 67
MEM_MA_DM4 130
MEM_MA_DM5 147
MEM_MA_DM6 170
MEM_MA_DM7 185
5 MEM_MA_DQS0_P 13
5 MEM_MA_DQS1_P 31
5 MEM_MA_DQS2_P 51
5 MEM_MA_DQS3_P 70
5 MEM_MA_DQS4_P 131
5 MEM_MA_DQS5_P 148
5 MEM_MA_DQS6_P 169
5 MEM_MA_DQS7_P 188
5 MEM_MA_DQS0_N 11
5 MEM_MA_DQS1_N 29
5 MEM_MA_DQS2_N 49
5 MEM_MA_DQS3_N 68
5 MEM_MA_DQS4_N 129
5 MEM_MA_DQS5_N 146
5 MEM_MA_DQS6_N 167
5 MEM_MA_DQS7_N 186
5 MEM_MA_CLK1_P 30
5 MEM_MA_CLK1_N 32
5 MEM_MA_CLK7_P 164
5 MEM_MA_CLK7_N 166
5,8 MEM_MA_CKE0 79
5,8 MEM_MA_CKE1 80
5,8 MEM_MA_RAS# 108
5,8 MEM_MA_CAS# 113
5,8 MEM_MA_WE# 109
5,8 MEM_MA_CS#0 110
5,8 MEM_MA_CS#1 115
5,8 MEM_MA_ODT0 114
5,8 MEM_MA_ODT1 119
DIM1_SA0 198
DIM1_SA1 200
3,8,14,24 PDAT_SMB 195
3,8,14,24 PCLK_SMB 197
199 VDDspd
1 VREF
MEM_MA_DATA0
MEM_MA_DATA1
MEM_MA_DATA2
MEM_MA_DATA3
MEM_MA_DATA4
MEM_MA_DATA5
MEM_MA_DATA6
MEM_MA_DATA7
MEM_MA_DATA8
MEM_MA_DATA9
MEM_MA_DATA10
MEM_MA_DATA11
MEM_MA_DATA12
MEM_MA_DATA13
MEM_MA_DATA14
MEM_MA_DATA15
MEM_MA_DATA16
MEM_MA_DATA17
MEM_MA_DATA18
MEM_MA_DATA19
MEM_MA_DATA20
MEM_MA_DATA21
MEM_MA_DATA22
MEM_MA_DATA23
MEM_MA_DATA24
MEM_MA_DATA25
MEM_MA_DATA26
MEM_MA_DATA27
MEM_MA_DATA28
MEM_MA_DATA29
MEM_MA_DATA30
MEM_MA_DATA31
MEM_MA_DATA36
MEM_MA_DATA37
MEM_MA_DATA35
MEM_MA_DATA39
MEM_MA_DATA38
MEM_MA_DATA32
MEM_MA_DATA33
MEM_MA_DATA34
MEM_MA_DATA40
MEM_MA_DATA41
MEM_MA_DATA46
MEM_MA_DATA47
MEM_MA_DATA44
MEM_MA_DATA45
MEM_MA_DATA42
MEM_MA_DATA43
MEM_MA_DATA52
MEM_MA_DATA49
MEM_MA_DATA54
MEM_MA_DATA55
MEM_MA_DATA53
MEM_MA_DATA48
MEM_MA_DATA51
MEM_MA_DATA50
MEM_MA_DATA60
MEM_MA_DATA63
MEM_MA_DATA62
MEM_MA_DATA56
MEM_MA_DATA57
MEM_MA_DATA58
MEM_MA_DATA59
MEMHOT_SODIMM# 1
R144 *0_4 MEMHOT_SODIMM#
MEM_MA_RESET#1
T139
MEM_MA_NC5
T137
MEM_MA_DATA[0..63] 5
+3V
C314 0.1U/10V_4
+0.9VSMVREF_DIMM
C200 1000p/50V_4
C199 0.1U/10V_4
C196 2.2U/6.3V_6
VSS0
VSS1
VSS2
VSS3
VSS4
VSS5
VSS6
VSS7
VSS8
VSS9
VSS10
VSS11
VSS12
VSS13
VSS14
VSS15
VSS16
VSS17
VSS18
VSS19
VSS20
VSS21
VSS22
VSS23
VSS24
VSS25
VSS26
VSS27
VSS28
VSS29
VSS30
VSS31
VSS32
VSS33
VSS34
VSS35
VSS36
VSS37
VSS38
VSS39
VSS40
VSS41
VSS42
VSS43
VSS44
VSS45
VSS46
VSS47
VSS48
VSS49
VSS50
VSS51
VSS52
VSS53
VSS54
VSS55
VSS56
DDR SO-DIMM SOCKET 1.8V
H=5.2
R178 10K/F_4 DIM1_SA0
R180 10K/F_4 DIM1_SA1
SMbus address A0
+1.8VSUS
CN19
SO-DIMM
5,8 MEM_MB_ADD[0..15]
MEM_MB_ADD0 102
MEM_MB_ADD1 101
MEM_MB_ADD2 100
MEM_MB_ADD3 99
MEM_MB_ADD4 98
MEM_MB_ADD5 97
MEM_MB_ADD6 94
MEM_MB_ADD7 92
MEM_MB_ADD8 93
MEM_MB_ADD9 91
MEM_MB_ADD10 105
MEM_MB_ADD11 90
MEM_MB_ADD12 89
MEM_MB_ADD13 116
MEM_MB_ADD14 86
MEM_MB_ADD15 84
5,8 MEM_MB_BANK[0..2]
MEM_MB_BANK0 107
MEM_MB_BANK1 106
MEM_MB_BANK2 85
5 MEM_MB_DM[0..7]
MEM_MB_DM0 10
MEM_MB_DM1 26
MEM_MB_DM2 52
MEM_MB_DM3 67
MEM_MB_DM4 130
MEM_MB_DM5 147
MEM_MB_DM6 170
MEM_MB_DM7 185
5 MEM_MB_DQS0_P 13
5 MEM_MB_DQS1_P 31
5 MEM_MB_DQS2_P 51
5 MEM_MB_DQS3_P 70
5 MEM_MB_DQS4_P 131
5 MEM_MB_DQS5_P 148
5 MEM_MB_DQS6_P 169
5 MEM_MB_DQS7_P 188
5 MEM_MB_DQS0_N 11
5 MEM_MB_DQS1_N 29
5 MEM_MB_DQS2_N 49
5 MEM_MB_DQS3_N 68
5 MEM_MB_DQS4_N 129
5 MEM_MB_DQS5_N 146
5 MEM_MB_DQS6_N 167
5 MEM_MB_DQS7_N 186
5 MEM_MB_CLK1_P 30
5 MEM_MB_CLK1_N 32
5 MEM_MB_CLK7_P 164
5 MEM_MB_CLK7_N 166
5,8 MEM_MB_CKE0 79
5,8 MEM_MB_CKE1 80
5,8 MEM_MB_RAS# 108
5,8 MEM_MB_CAS# 113
5,8 MEM_MB_WE# 109
5,8 MEM_MB0_CS#0 110
5,8 MEM_MB0_CS#1 115
5,8 MEM_MB0_ODT0 114
5,8 MEM_MB0_ODT1 119
DIM2_SA0 198
DIM2_SA1 200
PDAT_SMB 195
PCLK_SMB 197
199 VDDspd
1 VREF
MEM_MB_DATA0
MEM_MB_DATA1
MEM_MB_DATA2
MEM_MB_DATA3
MEM_MB_DATA4
MEM_MB_DATA5
MEM_MB_DATA6
MEM_MB_DATA7
MEM_MB_DATA8
MEM_MB_DATA9
MEM_MB_DATA10
MEM_MB_DATA11
MEM_MB_DATA12
MEM_MB_DATA13
MEM_MB_DATA14
MEM_MB_DATA15
MEM_MB_DATA16
MEM_MB_DATA17
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MEM_MB_DATA22
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MEM_MB_DATA26
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MEM_MB_DATA30
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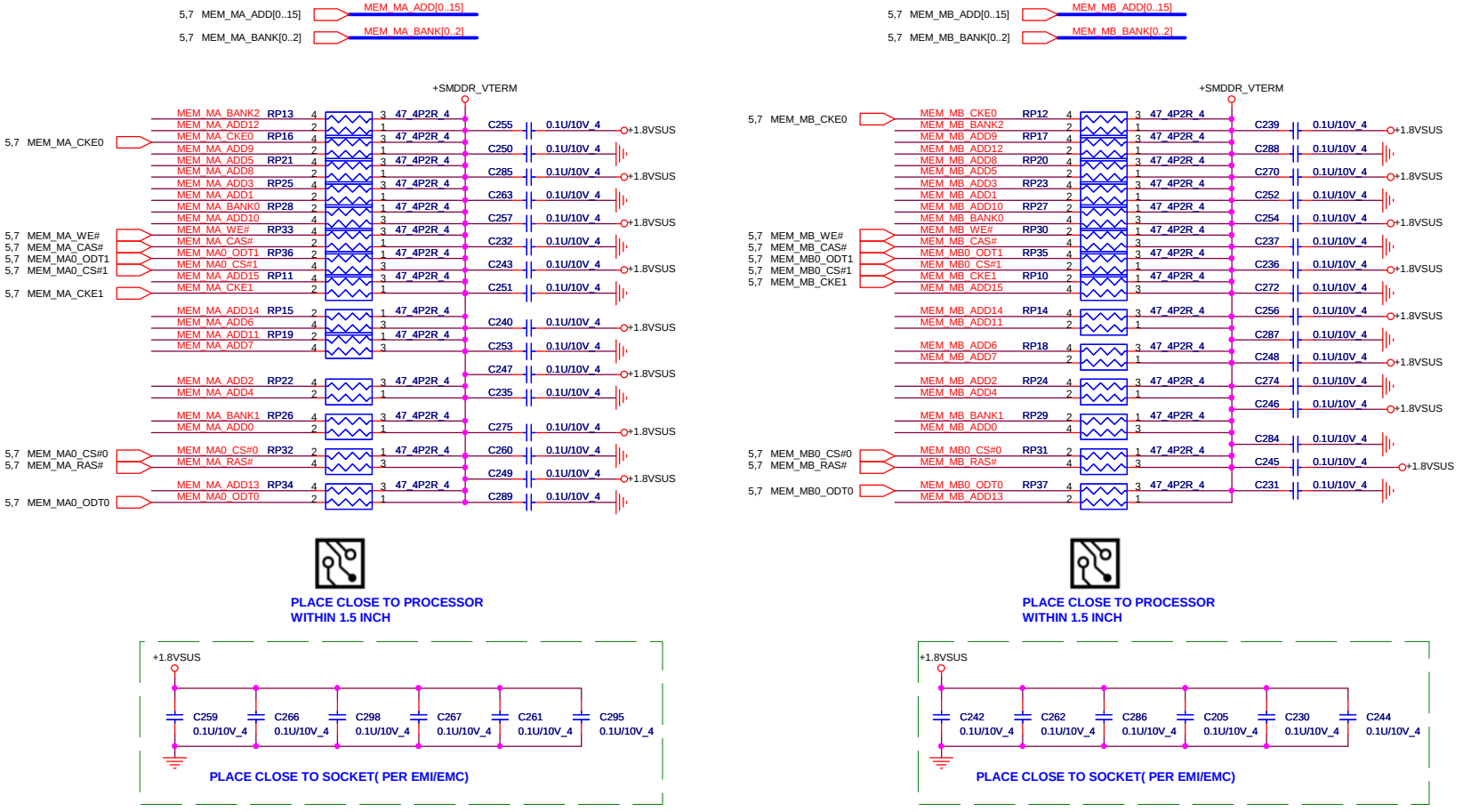
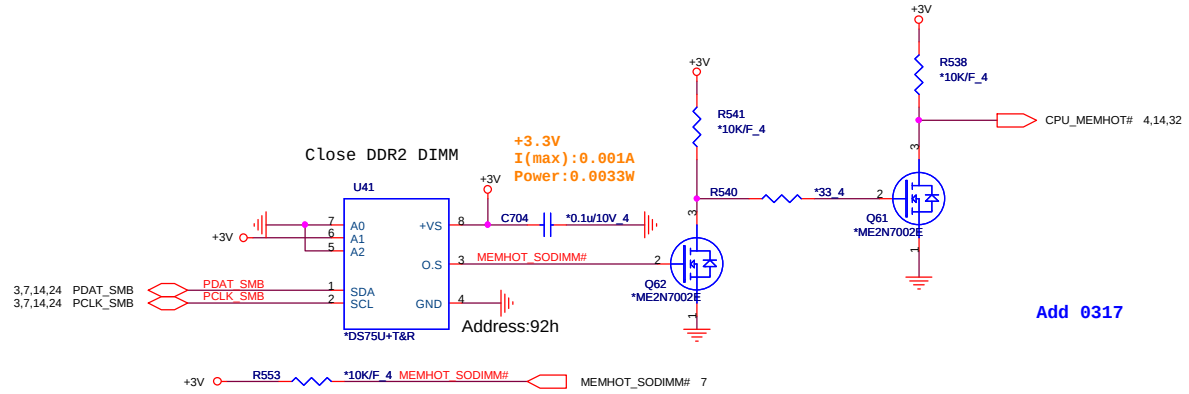
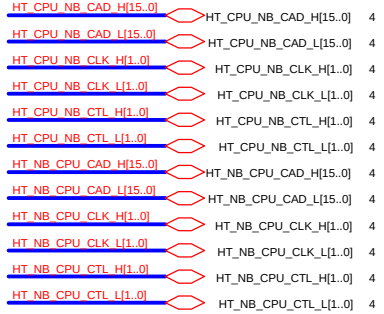
MEM_MB_DATA37
MEM_MB_DATA36
MEM_MB_DATA34
MEM_MB_DATA35
MEM_MB_DATA33
MEM_MB_DATA32
MEM_MB_DATA38
MEM_MB_DATA39
MEM_MB_DATA40
MEM_MB_DATA45
MEM_MB_DATA47
MEM_MB_DATA46
MEM_MB_DATA44
MEM_MB_DATA41
MEM_MB_DATA43
MEM_MB_DATA42
MEM_MB_DATA52
MEM_MB_DATA53
MEM_MB_DATA50
MEM_MB_DATA51
MEM_MB_DATA48
MEM_MB_DATA49
MEM_MB_DATA54
MEM_MB_DATA55
MEM_MB_DATA56
MEM_MB_DATA60
MEM_MB_DATA58
MEM_MB_DATA59
MEM_MB_DATA61
MEM_MB_DATA57
MEM_MB_DATA62
MEM_MB_DATA63
MEMHOT_SODIMM# 2
R529 *0_4 MEMHOT_SODIMM#
MEM_MB_RESET#2
T140
MEM_MB_NC5
T138
MEMHOT_SODIMM# 8
MEM_MB_DATA[0..63] 5
+3V
C492 0.1U/10V_4
+0.9VSMVREF_DIMM
C531 2.2U/6.3V_6
C530 0.1U/10V_4
C525 1000p/50V_4
VSS0
VSS1
VSS2
VSS3
VSS4
VSS5
VSS6
VSS7
VSS8
VSS9
VSS10
VSS11
VSS12
VSS13
VSS14
VSS15
VSS16
VSS17
VSS18
VSS19
VSS20
VSS21
VSS22
VSS23
VSS24
VSS25
VSS26
VSS27
VSS28
VSS29
VSS30
VSS31
VSS32
VSS33
VSS34
VSS35
VSS36
VSS37
VSS38
VSS39
VSS40
VSS41
VSS42
VSS43
VSS44
VSS45
VSS46
VSS47
VSS48
VSS49
VSS50
VSS51
VSS52
VSS53
VSS54
VSS55
VSS56
DDR SO-DIMM SOCKET 1.8V
H=9.2
+1.8VSUS
R123 2K/F_4
R122 2K/F_4
+SMDDR_VREF
+0.9VSMVREF_DIMM
R124 *0_4
+0.9VSMVREF_DIMM
Only for reserved
1/18 Change CN23 footprint from DDR-C-1734071-200P to DDR-C-1734071-200P-BD3A (SMT open issue)
DIM2_SA0 R179 10K/F_4 +3V
DIM2_SA1 R177 10K/F_4
SMbus address A2
Quanta Computer Inc.
PROJECT : ZK8
Size
Document Number
DDR2 SODIMMS: A/B CHANNEL
Rev 3A
Date: Thursday, May 21, 2009
Sheet 7 of 42



stuff for S1G3 CPU



Quanta Computer Inc.		
PROJECT : ZK8		
Size	Document Number: DDR2 SODIMMS TERMINATIONS	Rev: 3A
Date: Thursday, May 21, 2009	Sheet 8 of 42	



11/4 modify

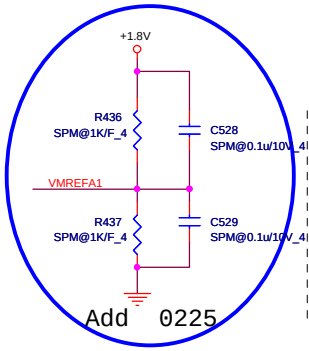
signals	RS780	RX780
HT_TXCALP	R641 300 ohm 1%	R641 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R655 300 ohm 1%	R655 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

RES CHIP 300 1/16W +-1%(0402)
P/N : CS13002FB00

A12 version
RS780M AJ067400T05 100-CK2612(216-0674008-00)
RS780MC AJ067400T06 100-CK2613(216-0674010-00)
RX781 AJ067400T10 100-CK2642(215-0674024)
SB700 AJA12FG0T18 100-CK2614(218S7EALA12FG)

A13 version
RS780M AJ067400T18 100-CK2699(216-0674022)
RS780MC AJ067400T20 100-CK2704(216-0674024)
RX781 AJ067400T21 100-CK2706(215-0674034)
A12 version
SB700 AJA12FG0T18

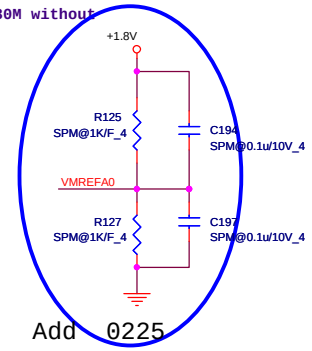


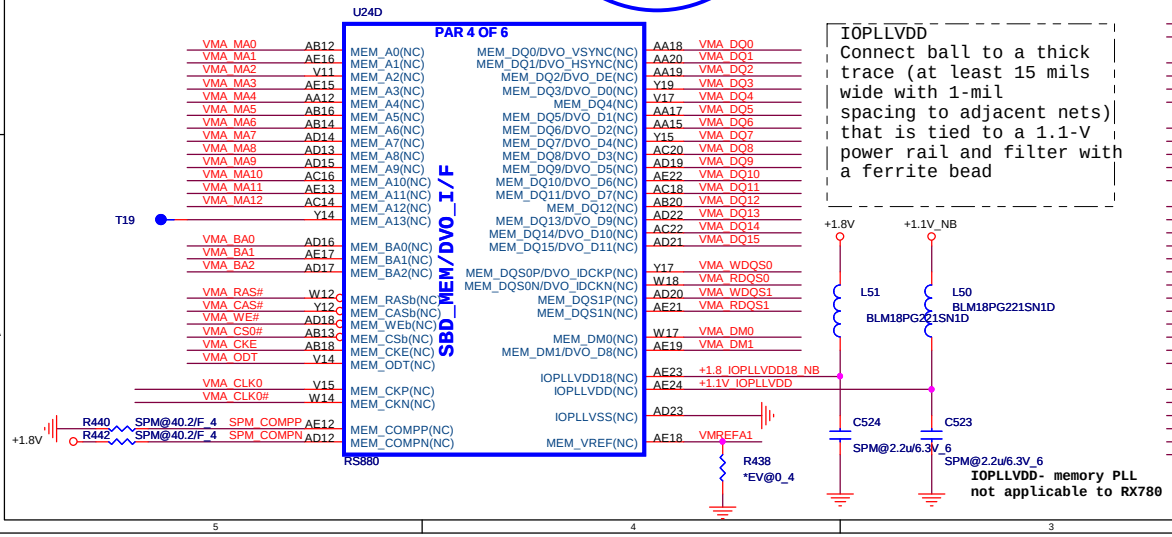
This block is for UMA RS780 only , RX780 can remove all component

IOPLLVDD18
Connect ball to a thick trace (at least 15 mils wide with 10-mil spacing from adjacent nets) tied to a 1.8-V power rail and filter with a ferrite bead.

IOPLLVDD
Connect ball to a thick trace (at least 15 mils wide with 1-mil spacing to adjacent nets) that is tied to a 1.1-V power rail and filter with a ferrite bead

2/1 R480,R479 no stuff when RS780M without side port / RX781





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Size	Document Number	Rev
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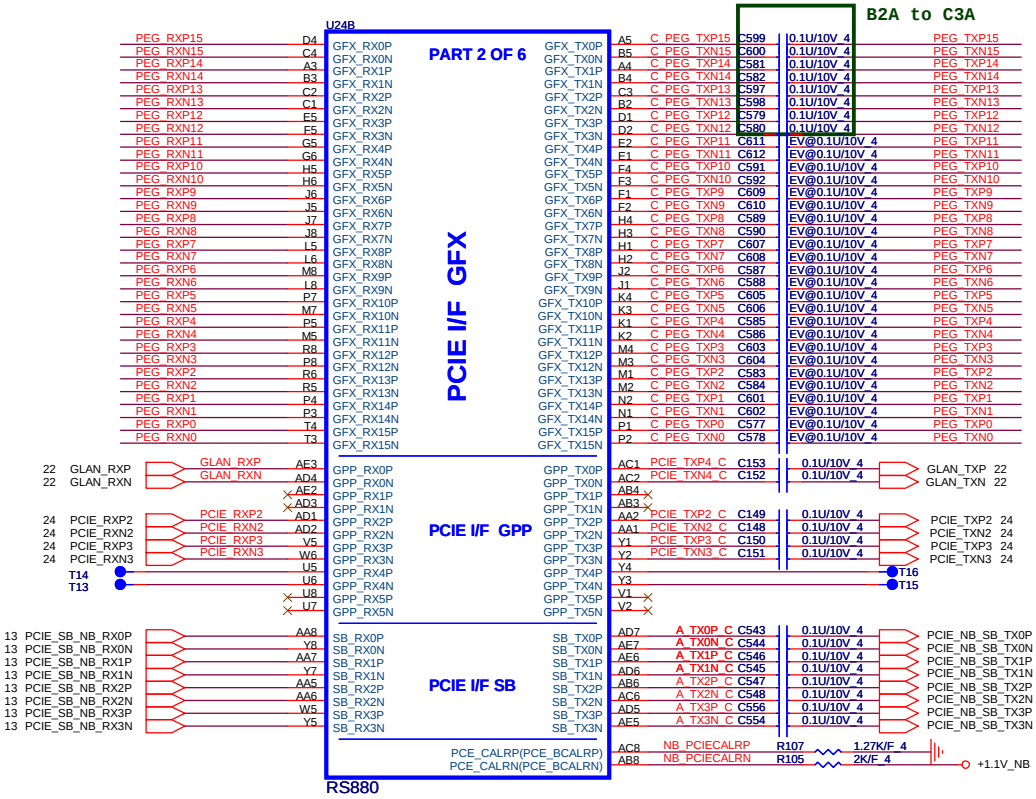
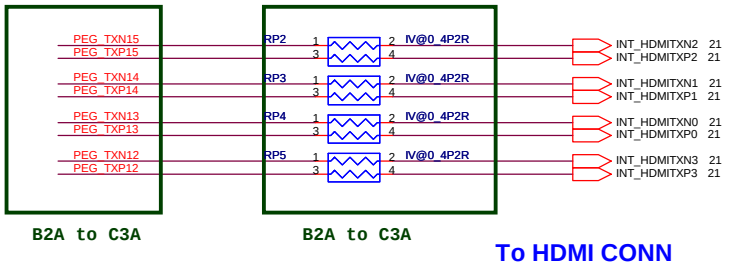


Close to North Bridge



To HDMI CONN

TO PCIE-LAN

TO TV CARD

TO WLAN

NOTE:
RS780MC no support Graphic / HDMI

11/4 modify

RX780/RS740/RS780 difference table (PCIE LINK)

	RS740	RX780/RS780
NB_PCIECALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

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RX780: Powered from the 1.8-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.
RS780: Powered from the 3.3-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.

RS780

4,13 CPU_LDT_RST# R459 *0_4
13 NB_PLTRST# R100 0_4 NB_PLTRST#_NB

North Bridge RESET

Power Xpress

+3V R460 EV@4.7K_4 R461 *EV@0_4 +3V R88 *10K_4
D27 *EV@CH501H-40PT HDTV_DET LVDS_SW Q45 EV@BSS138_NL/SOT23 PX_LVDS_SW 19,20
D28 EV@CH501H-40PT PX_EN 13 R462 *IV@10K_4
+3V R458 *4.7K_4 HDTV_DET

RX780
+1.1V_NB R106 *2.2K_4 INT_CRT_DDCDAT
R103 *2.2K_4 INT_CRT_DDCCLK
10/9 add 2K pull up to DDCDAT /DDCCLK for RX780

11/4 no stuff for RS780M/MC/RX781

12/22 stuff R48 2.2K for power play

STRP_DATA R455 *10K/F_4 +3V
R454 2.2K_4

U24C — RS880 — PART 3 OF 6

CRT/TVOUT
+3V_AVDD_NB F12 AVDD1(NC)
+1.8V_AVDDDI_NB F14 AVDD2(NC)
+1.8V_AVDDQ_NB G15 AVDDDI(NC)
H15 AVSSDI(NC)
H14 AVDDQ(NC)
INT_TV_C/R F17 AVSSQ(NC)
F17 C_Pr(DFT_GPIO5)
F15 Y(DFT_GPIO2)
COMP_Pb(DFT_GPIO4)

20 INT_CRT_RED R128 140/F_4 INT_CRT_RED G18 RED(DFT_GPIO0)
20 INT_CRT_GRN R130 150/F_4 INT_CRT_GRN G17 REDN(NC)
20 INT_CRT_BLU R133 150/F_4 INT_CRT_BLU E18 GREEN(DFT_GPIO1)
E18 GREENb(NC)
E19 BLUE(DFT_GPIO3)
F19 BLUEb(NC)

20 INT_HSYNC A11 DAC_HSYNC(PWM_GPIO4)
20 INT_VSYNC B11 DAC_VSYNC(PWM_GPIO6)
20 INT_CRT_DDCDAT E8 DAC_SDA(PCE_TCALRN)
20 INT_CRT_DDCCLK F8 DAC_SCL(PCE_RCALRN)
R126 715/F_6 DAC_RSET_NB G14 DAC_RSET(PWM_GPIO1)

PLL PWR
+1.1V_PLLVDD A12 PLLVDD(NC)
+1.8V_PLLVDD18 D14 PLLVDD18(NC)
B12 PLLVSS(NC)
+1.8V_VDDA18HTPLL H17 VDDA18HTPLL
+1.8V_VDDA18PCIEPLL D7 VDDA18PCIEPLL1
E7 VDDA18PCIEPLL2

LVTM
TXOUT_L0P(NC) A22 INT_TXLOUT0+ 19
TXOUT_L0N(NC) B22 INT_TXLOUT0- 19
TXOUT_L1P(NC) A21 INT_TXLOUT1+ 19
TXOUT_L1N(NC) B21 INT_TXLOUT1- 19
TXOUT_L2P(NC) B20 INT_TXLOUT2+ 19
TXOUT_L2N(DBG_GPIO0) A20 INT_TXLOUT2- 19
TXOUT_L3P(NC) A19 T146
TXOUT_L3N(DBG_GPIO2) B19 T147

TXOUT_U0P(NC) B18 INT_TXUOUT0+ 19
TXOUT_U0N(NC) A18 INT_TXUOUT0- 19
TXOUT_U1P(PCIE_RESET_GPIO3) A17 INT_TXUOUT1+ 19
TXOUT_U1N(PCIE_RESET_GPIO2) B17 INT_TXUOUT1- 19
TXOUT_U2P(NC) D20 INT_TXUOUT2+ 19
TXOUT_U2N(NC) D21 INT_TXUOUT2- 19
TXOUT_U3P(PCIE_RESET_GPIO5) D18 T148
TXOUT_U3N(NC) D19 T145

TXCLK_LP(DBG_GPIO1) B16 INT_TXLCLKOUT+ 19
TXCLK_LN(DBG_GPIO3) A16 INT_TXLCLKOUT- 19
TXCLK_UP(PCIE_RESET_GPIO4) D16 INT_TXUCLKOUT+ 19
TXCLK_UN(PCIE_RESET_GPIO1) D17 INT_TXUCLKOUT- 19

VDDLTP18(NC) A13 +1.8V_VDDLTP18_NB
VSSLTP18(NC) B13
VDDLT18_1(NC) A15 +1.8V_VDDLT_18_NB
VDDLT18_2(NC) B15
VDDLT33_1(NC) A14 +3V_VDLT33_NB
VDDLT33_2(NC) B14

VSSLT1(VSS) C14
VSSLT2(VSS) D15
VSSLT3(VSS) C16
VSSLT4(VSS) C18
VSSLT5(VSS) C20
VSSLT6(VSS) E20
VSSLT7(VSS) C22

11/01 exchange LVDS_PWM /LVDS_BLON

PM
NB_PLTRST#_NB D8 SYSRESETb
NB_PWRGD_IN A10 POWERGOOD
NB_LDT_STOP# C10 LDTSTOPb
NB_ALLOW_LDTSTOP C12 ALLOW_LDTSTOP

17 NB_PWRGD_IN

CLOCKS
NBHT_REFCLKP C25 HT_REFCLKP
NBHT_REFCLKN C24 HT_REFCLKN
3 NBHT_REFCLKP
3 NBHT_REFCLKN
3 EXT_NB_OSC R114 0_4 NB_REFCLK_P E11 REFCLK_P/OSCIN(OSCIN)
R116 0_4 NB_REFCLK_N F11 REFCLK_N(PWM_GPIO3)
+1.1V_NB 4.7K_4 R111 4.7K_4 R112
NBGFX_CLKP T2 GFX_REFCLKP I/O
NBGFX_CLKN T1 GFX_REFCLKN
3 NBGFX_CLKP
3 NBGFX_CLKN
022409 remove for AMD suggest
N1 GPP_REFCLKP I/O
U1 GPP_REFCLKN
SBLINK_CLKP V4 GPPSB_REFCLKP(SB_REFCLKP)
SBLINK_CLKN V3 GPPSB_REFCLKN(SB_REFCLKN)
3 SBLINK_CLKP
3 SBLINK_CLKN

MIS.
19 INT_LVDS_EDIDDATA A9 I2C_DATA
19 INT_LVDS_EDIDCLK B9 I2C_CLK
INT_LVDS_EDIDDATA B8 DDC_DATA/AUX0N(NC)
INT_LVDS_EDIDCLK A8 DDC_CLK/AUX0P(NC)
HDTV_DET B7 AUX1P(NC)
A7 AUX1N(NC)
B2A to C3A
21 SDVO_CTRLCLK T152 SDVO_CTRLCLK
21 SDVO_CTRLDATA SDVO_CTRLDATA
36 +NB_CORE_ON R456 SHORT_PAD_4 STRP_DATA B10 STRP_DATA
G11 RSVD
B2A to C3A T151 RS780_AUX_CAL C8 AUX_CAL(NC)

LVDS_DIGON(PCE_TCALRP) E9 INT_LVDS_DIGON 19
LVDS_BLON(PCE_RCALRP) E7 L_BKLT_CTRL 19
LVDS_ENA_BL(PWM_GPIO2) G12 INT_LVDS_BLON 19
R91 *IV@1.27K/F_4
R90 *IV@1.27K/F_4
For RX780 only
9/25 Del R205

TMDS_HPD(NC) D9 TMDS_HPD0
HPD(NC) D10 TMDS_HPD1 T18 TMDS_HPD0 21
TVCLKIN(PWM_GPIO5) D12 SUS_STAT#_NB R451 0_4 SUS_STAT# 14
THERMALDIODE_P AE8 R_NB_THRMDA T149
THERMALDIODE_N AD8 R_NB_THRMDC T150
TESTMODE D13 TEST_EN R449 *3K_4
R447 1.82K/F_4

selects Loading of straps from EPROM
1 : use default vaule , default
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RX780 --RS780_AUX_CAL
RS780 -- SUS_ATAT

RX780
RS780_AUX_CAL R457 *3K_4

Enables Debug Bus acess through memory T/O pads and GPIO.
1 : Enable RX780 , Default
0 : Disable RX780

RX780
INT_TV_C/R R121 *1K_4

Reserved only

Enables Debug Bus acess through memory T/O pads and GPIO.
1 : Enable RS780 , Default
0 : Disable RS780
(RS780 use VSYNC#)

RS780
INT_VSYNC R450 3K_4 +3V
R453 *3K_4

Indicates if memory Side port is available or not
0: available RS780 , Default
1: Not available RS780
(RS780 use HSYNC#)

RS780
INT_HSYNC R445 3K_4 +3V
R446 SPM@3K_4

10/19 RS780M Databook rev 1.01 define High disable

1/17 RX781 connect to GND
C104,C110,C646,C98,C136,C103,C118 change to CS00003J951

+3V L18 BLM18PG221SN1D +3V_AVDD_NB C171 10U/6.3V_6
AVDD-DAC Analog not applicable to RX780

+1.1V_NB BLM18PG221SN1D L19 +1.1V_PLLVDD C185 2.2U/6.3V_6
PLLVDD - Graphics PLL not applicable to RX780

+1.8V L20 BLM18PG221SN1D +1.8V_PLLVDD18 C174 10U/6.3V_6 C186 10U/6.3V_6
PLLVDD18 - Graphics PLL not applicable to RX780

+1.8V R120 0_6 +1.8V_AVDDI_NB C180 2.2U/6.3V_6
AVDDI-DAC Digital not applicable to RX780

BLM18PG221SN1D L21 +1.8V_AVDDQ_NB C187 2.2U/6.3V_6
AVDDQ-DAC Bandgap Reference not applicable to RX780

11/4 no stuff for RS780M/MC

+1.8V L55 BLM18PG221SN1D +1.8V_VDDLTP18_NB C179 2.2U/6.3V_6
VDDLTP18 - LVDS or DVI/HDMI PLL not applicable to RX780

L52 BLM21PG221SN1D +1.8V_VDDLT_18_NB C533 4.7U/6.3V_6 C534 0.1U/10V_4
1/17 RX781 no stuff them L2,L12,C124,L52,R76,L17,L51,L10,C115

VDDLT18 - LVDS or DVI/HDMI digital not applicable to RX780

1/31 voltage leakage issue
remove Q5,Q3,R83,R80,R97
stuff R88,R77

+1.8V **VDDA18PCIEPLL -PCIE PLL**
L57 BLM18PG221SN1D 20mils width +1.8V_VDDA18PCIEPLL C165 2.2U/6.3V_6

VDDA18HTPLL -HT LINK PLL
L22 BLM18PG221SN1D 20mils width +1.8V_VDDA18HTPLL C195 2.2U/6.3V_6

Q43 *BSS138_NL/SOT23
4,13 CPU_LDT_STOP#
R431 *4.7K_4 RX780
R430 *4.7K_4 RS780
NB_LDT_STOP#
R433 0_4 RS780

Q44 *BSS138_NL/SOT23
4 CPU_LDT_REQ#
R441 *0_4
R434 *4.7K_4 RX780
R435 *4.7K_4 RS780
NB_ALLOW_LDTSTOP
13 ALLOW_LDTSTOP
R439 0_4 RS780

modify 0310

+3V L53 BLM21PG221SN1D +3V_VDLT33_NB C536 *2.2U/6.3V_6
VDDLT33 - LVDS or DVI/HDMI ANALOG RS740 only

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RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVDD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVDD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVDD18	NC	+1.8V	VDDLT33	NC	NC

U29F

PART 6/6

GROUND

VSSAPCIE1 VSSAPCIE2 VSSAPCIE3 VSSAPCIE4 VSSAPCIE5 VSSAPCIE6 VSSAPCIE7 VSSAPCIE8 VSSAPCIE9 VSSAPCIE10 VSSAPCIE11 VSSAPCIE12 VSSAPCIE13 VSSAPCIE14 VSSAPCIE15 VSSAPCIE16 VSSAPCIE17 VSSAPCIE18 VSSAPCIE19 VSSAPCIE20 VSSAPCIE21 VSSAPCIE22 VSSAPCIE23 VSSAPCIE24 VSSAPCIE25 VSSAPCIE26 VSSAPCIE27 VSSAPCIE28 VSSAPCIE29 VSSAPCIE30 VSSAPCIE31 VSSAPCIE32 VSSAPCIE33 VSSAPCIE34 VSSAPCIE35 VSSAPCIE36 VSSAPCIE37 VSSAPCIE38 VSSAPCIE39 VSSAPCIE40

VSSAHT1 VSSAHT2 VSSAHT3 VSSAHT4 VSSAHT5 VSSAHT6 VSSAHT7 VSSAHT8 VSSAHT9 VSSAHT10 VSSAHT11 VSSAHT12 VSSAHT13 VSSAHT14 VSSAHT15 VSSAHT16 VSSAHT17 VSSAHT18 VSSAHT19 VSSAHT20 VSSAHT21 VSSAHT22 VSSAHT23 VSSAHT24 VSSAHT25 VSSAHT26 VSSAHT27

VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34

+1.1V 2A for RS780M

VDDHT - HT LINK digital I/O for RX780/RS780

+1.1V_NB 0.6A L54 BLM21PG221SN1D

C535 4.7U/6.3V_6, C190 0.1U/10V_4, C188 0.1U/10V_4, C532 0.1U/10V_4

+1.1V_VDDHT

VDDHTRX - HT LINK RX I/O for RX780/RS780

0.45A L49 BLM21PG221SN1D

C519 4.7U/6.3V_6, C193 0.1U/10V_4, C517 0.1U/10V_4, C201 0.1U/10V_4

+1.1V_VDDHTRX

+1.2V 2A for RS780M+SB700

+1.2V 0.5A L48 BLM21PG221SN1D

C518 4.7U/6.3V_6, C189 0.1U/10V_4, C202 0.1U/10V_4, C521 0.1U/10V_4, C192 0.1U/10V_4

+1.2V_VDDHTTX

+1.35V for A1-1 chip bug , A1-2 can remove

VDDHTTX - HT LINK TX I/O for RX780/RS780

12/14 del L15 stuff L36 for A12

+1.8V 1A for RS780M+SB700

+1.8V 600mA L17 BLM21PG221SN1D

C176 4.7U/6.3V_6, C177 4.7U/6.3V_6, C184 0.1U/10V_4, C168 0.1U/10V_4, C173 0.1U/10V_4, C170 0.1U/10V_4

+1.8V_VDDA18PCIE

VDDA18PCIE - PCIE TX stage I/O for RX780/RS780

U24E

PART 5/6

POWER

RS880

VDDHT_1 VDDHT_2 VDDHT_3 VDDHT_4 VDDHT_5 VDDHT_6 VDDHT_7 — J17 K16 L16 M16 P16 R16 T16

VDDHTRX_1 VDDHTRX_2 VDDHTRX_3 VDDHTRX_4 VDDHTRX_5 VDDHTRX_6 VDDHTRX_7 — H18 G19 F20 E21 D22 B23 A23

VDDHTTX_1 VDDHTTX_2 VDDHTTX_3 VDDHTTX_4 VDDHTTX_5 VDDHTTX_6 VDDHTTX_7 VDDHTTX_8 VDDHTTX_9 VDDHTTX_10 VDDHTTX_11 VDDHTTX_12 VDDHTTX_13 — AE25 AD24 AC23 AB22 AA21 Y20 W19 V18 U17 T17 R17 P17 M17

VDDA18PCIE_1 VDDA18PCIE_2 VDDA18PCIE_3 VDDA18PCIE_4 VDDA18PCIE_5 VDDA18PCIE_6 VDDA18PCIE_7 VDDA18PCIE_8 VDDA18PCIE_9 VDDA18PCIE_10 VDDA18PCIE_11 VDDA18PCIE_12 VDDA18PCIE_13 VDDA18PCIE_14 VDDA18PCIE_15 — J10 P10 K10 M10 L10 W9 H9 T10 R10 Y9 AA9 AB9 AD9 AE9 U10

VDDG18_1(VDD18_1) VDDG18_2(VDD18_2) VDD18_MEM1(NC) VDD18_MEM2(NC) — F9 G9 AE11 AD11

VDDPCIE_1 VDDPCIE_2 VDDPCIE_3 VDDPCIE_4 VDDPCIE_5 VDDPCIE_6 VDDPCIE_7 VDDPCIE_8 VDDPCIE_9 VDDPCIE_10 VDDPCIE_11 VDDPCIE_12 VDDPCIE_13 VDDPCIE_14 VDDPCIE_15 VDDPCIE_16 VDDPCIE_17 — A6 B6 C6 D6 E6 F6 G7 H8 J9 K9 M9 L9 P9 R9 T9 V9 U9

VDDC_1 VDDC_2 VDDC_3 VDDC_4 VDDC_5 VDDC_6 VDDC_7 VDDC_8 VDDC_9 VDDC_10 VDDC_11 VDDC_12 VDDC_13 VDDC_14 VDDC_15 VDDC_16 VDDC_17 VDDC_18 VDDC_19 VDDC_20 VDDC_21 VDDC_22 — K12 J14 U16 J11 K15 M12 L14 L11 M13 M15 N12 N14 P11 P13 P14 R12 R15 T11 T15 U12 T14 J16

VDD_MEM1(NC) VDD_MEM2(NC) VDD_MEM3(NC) VDD_MEM4(NC) VDD_MEM5(NC) VDD_MEM6(NC) — AE10 AA11 Y11 AD10 AB10 AC10

VDDG33_1(NC) VDDG33_2(NC) — H11 H12

VDD18 - RS780 I/O transform

B2A to C3A

+1.8V R95 short0603 0.005A C169 1U/10V_4 +1.8V_VDDG18_NB

+1.8V R443 short0603 0.005A C538 1U/10V_4 +1.8V_VDD18_MEM

VDD18_MEM For UMA RS780 only
Not applicable to RX780
memory I/O transform

1/17 RX781 no stuff them R484

1/17 RX781 connect to GND C616 change to CS00002JB38

B2A to C3A

VDDPCIE - PCIE-E Main power

+1.1V_VDD_PCIE 0.7A R99 short0805 +1.1V_NB

C166 0.1U/10V_4, C159 0.1U/10V_4, C164 1U/10V_4, C157 1U/10V_4, C156 4.7U/6.3V_6

2/13 EMI
stuff C804~C807 for +NB_CORE

VDDC - Core Logic power

7A +NB_CORE

C191 0.1U/10V_4, C183 0.1U/10V_4, C514 0.1U/10V_4, C520 0.1U/10V_4, C522 10U/6.3V_8, C513 0.1U/10V_4, C526 0.1U/10V_4, C515 0.1U/10V_4, C516 0.1U/10V_4

C178 0.1U/10V_4, C182 0.1U/10V_4, C181 0.1U/10V_4, C527 10U/6.3V_8

10/18 follow AMD design guide 1.0

0.23A

R444 SPM@0_6 +1.8V

C167 SPM@4.7u/6.3V_6, C540 SPM@0.1u/10V_4, C542 SPM@0.1u/10V_4, C541 SPM@0.1u/10V_4, C161 SPM@0.1u/10V_4

Side port support

1.8V(0.15A) +1.8V_VDD_MEM

R448 0_6

+3V_VDDG33 C172 0.1U/10V_4, C154 0.1U/10V_4

R97 RS780 short0603 3.3V(0.03A) +3V

VDD33 - 3.3V I/O
Not applicable to RX780

VDD_MEM For UMA RS780 only
Not applicable to RX780
memory I/O transform

B2A to C3A

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2/4 reserve C800 PLTRST#

PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO U600

PCIE_PVDD-- PCIE PLL POWER

B test

9/22 Del T41

Add 0217 for SB710 only

1/31 voltage leakage remove R349

A11 default PCICLK5
A12 default GPIO41

All the PCI bus has build-in Pull-UP/Down resistors

Maybe can remove

RTC

R571+R667 = (5V - 0.2V-2V)/0.2mA = 14k

B2A to C3A

B2A to C3A

4/14
R527, change from 2k to 0.
R524 change from 2K to 16K
R529,change from 6.8k to 68.1k
R531 change form 15k to 150k

SB710
IC CTRL(528P) SB700 A11(218S7EALA11FG)
P/N : AJALA110T00

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NC only ,Can't be install

11/01 chagne +3VSUS to +3V_S5

10/31 add newcard DET#

SCL0/SDATA0 is 3V tolerance
AMD datasheet define it

Clock gen
/DDR2 /MINI CARD/NEW CARD

SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it

SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it

3/19 Without Side-port NU

0225
unstuff D6037 for S1g3 CPU not support this function

1/31 NEW_DET# change from GEVEN5# to GPM1#

B2A to C3A

9/22 Del T52

10/26 modify it

11/06 check it

0302
delete test point for layout

To Azalia

12/7 add D57,D58 to avoid voltage leakage

HD audio
interface is
3.3V voltage

9/25 Del R269, R623

12/21EMI
change R241from 33 to BK1005HM121-T
stff C309 22p

High : Main Strem
Low : Low Cost

AMD Suggestion 3/29 modify
From 20K change to 10K

9/22 Del T48

for EMI

To WLAN

To Bluetooth

To Finger Printer

To M/B H_S USB

To CCD

To CARD READER

To TV

To USB board

To M/B USB

To M/B USB/ESATA

SPI/LPC define

SB700 Part 4 of 5

SB710

Quanta Computer Inc.
PROJECT : ZK8

Size	Document Number	Rev
	SB710-ACPI/GPIO/USB 2/4	3A
Date: Thursday, May 21, 2009	Sheet 14 of 42	

PLACE SATA AC COUPLING CAPS CLOSE TO SB700

SATA PORT 0,1,2,3 can support AHCI mode

SATA PORT 4,5 are only support IDE mode

2/22 change SATA ODD from port3 to port4 (solve ODD post detect fail)

SATA

E-SATA

ODD

U14B

SB700

Part 2 of 5

SERIAL ATA

ATA 66/100/133

SPI ROM

SATA PWR

HW MONITOR

SB710

MB ID Selection Table

Board ID	ID4	ID3	ID2	ID1	ID0
Z08 ZK8					H L
CCFL Panel LED Panel				H L	
W/ MXM W/O MXM			H L		
W/ side_port W/O side_port		H L			
W/ HDMI W/O HDMI	H L				

MB ID

Mount R441 and Unmout R442 for non IR SKU

10/18 AMD suggest to connect to GND

B2A to C3A

0220 change from +3V to +3V_S5 follow AMD checklist

AVDD--H/W monitor Analog power

EMI FILTER CHIP BLM18PG221SN1D(220,1.4A)

2/13 EMI stuff C375,C366 for SB HW MONITOR

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB700

NOTE:
R361 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

PLVDD_SATA-- SATA PLL POWER

XTLVDD_SATA-- SATA crystal power

Place near ball

Quanta Computer Inc.	
PROJECT : ZK8	
Size	Document Number: SB710-SATA/IDE/HWM/SPI 3/4 — Rev 3A
Date: Thursday, May 21, 2009	Sheet 15 of 42

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

12/14 del R234 stuff R235 for A12

B2A to C3A

VDDQ--3.3V I/O power

+3V → R300 short0805 → +3.3V_SB_R, 0.8A
C383 100u/6.3V_3528
C378 10U/6.3V_8, C458 1U/10V_4, C450 1U/10V_4, C467 1U/10V_4, C462 1U/10V_4, C443 1U/10V_4, C444 1U/10V_4

1.8V : FLASH MEMORY MODE(DEFAULT)
3.3V: IDE MODE

U14C SB700 Part 3 of 5

VDDQ_1 VDDQ_2 VDDQ_3 VDDQ_4 VDDQ_5 VDDQ_6 VDDQ_7 VDDQ_8 VDDQ_9 VDDQ_10 VDDQ_11 VDDQ_12
L9 M9 T15 U9 U16 U17 V8 W7 Y6 AA4 AB5 AB21
PCI/GPIO I/O

VDD-- S/B CORE power

+1.2V_VCC_SB_R, 604mA
VDD_1 VDD_2 VDD_3 VDD_4 VDD_5 VDD_6 VDD_7 VDD_8 VDD_9
L15 M12 M14 N13 P12 P14 R11 R15 T16
CORE S0
C460 0.1U/10V_4, C463 0.1U/10V_4, C464 1U/10V_4, C465 1U/10V_4, C333 10U/6.3V_8
R199 short0805 → +1.2V

B2A to C3A

CKVDD_1.2V-- Internal clock Generator I/O power

+1.2V_CKVDD, 286mA
CKVDD_1.2V_1 CKVDD_1.2V_2 CKVDD_1.2V_3 CKVDD_1.2V_4
L21 L22 L24 L25
CLKGEN I/O
C469 *1U/10V_4, C472 *0.1U/50V_6, C471 0.1U/50V_6, C347 *10U/6.3V_8
L38 BLM18PG221SN1D → +1.2V

B2A to C3A B2A to C3A

+1.8V R259 1 *0_8 2
+3V R252 1 0_8 2
+VDD33_18, 0.45A
C373 *10U/6.3V_8, C445 *1U/10V_4, C452 *1U/10V_4, C448 *1U/10V_4, C442 *1U/10V_4
VDD33_18_1 VDD33_18_2 VDD33_18_3 VDD33_18_4
Y20 AA21 AA22 AE25
IDE/FLSH I/O

10/18 change to +1.8V

2008-MAR CHECK LIST CHANGE TO 3V because no IDE device

POWER

PCIE_VDDR--PCIE I/O power

+1.2V → L40 BLM18PG221SN1D → +1.2V_PCIE_VDDR, 844mA
C356 10U/6.3V_8, C455 1U/10V_4, C454 1U/10V_4, C456 1U/10V_4, C457 0.1U/10V_4, C461 0.1U/10V_4
PCIE_VDDR_1 PCIE_VDDR_2 PCIE_VDDR_3 PCIE_VDDR_4 PCIE_VDDR_5 PCIE_VDDR_6 PCIE_VDDR_7
P18 P19 P20 P21 R22 R24 R25
A-LINK I/O

S5_3.3--3.3v standby power

+3VALW_R, 0.01A
S5_3.3V_1 S5_3.3V_2 S5_3.3V_3 S5_3.3V_4 S5_3.3V_5 S5_3.3V_6 S5_3.3V_7
A17 A24 B17 J4 J5 L1 L2
3.3V_S5 I/O
C480 0.1U/10V_4, C470 0.1U/10V_4, C342 10U/6.3V_8
R201 short0603 → +3V_S5
Change to 0603

AVDD_SATA--SATA phy power

+1.2V → L45 BLM18PG221SN1D → +1.2V_AVDD_SATA, 0.2A
C214 10U/6.3V_6, C437 10U/6.3V_6, C447 0.1U/10V_4, C440 0.1U/10V_4, C438 1U/10V_4, C439 1U/10V_4
AVDD_SATA_1 AVDD_SATA_4 AVDD_SATA_2 AVDD_SATA_3 AVDD_SATA_5 AVDD_SATA_6 AVDD_SATA_7
AA14 AB18 AA15 AA17 AC18 AD17 AE17
SATA I/O

S5_1.2V--1.2V standby power

+1.2VALW_R, 0.22A
S5_1.2V_1 S5_1.2V_2
G2 G4
CORE S5
C476 1U/10V_4, C477 1U/10V_4
R377 short0603 → +1.2V_S5

0.2A
USB_PHY_1.2V_1 USB_PHY_1.2V_2
A10 B10
+1.2V_USB_PHY_R

B2A to C3A B2A to C3A

AVDDTX--USB Phy Analog I/O power

For support USB wakeup-->3V_S5
+3V_S5 → L37 BLM18PG221SN1D → +3V_AVDD_USB, 0.2A
C335 10U/6.3V_8, C334 10U/6.3V_8, C487 0.1U/10V_4, C483 0.1U/10V_4
C485 1U/10V_4, C484 1U/10V_4, C486 1U/10V_4, C336 0.1U/10V_4, C489 0.1U/10V_4, C339 0.1U/10V_4, C340 0.1U/10V_4
AVDDTX_0 AVDDTX_1 AVDDTX_2 AVDDTX_3 AVDDTX_4 AVDDTX_5 AVDDRX_0 AVDDRX_1 AVDDRX_2 AVDDRX_3 AVDDRX_4 AVDDRX_5
A16 B16 C16 D16 D17 E17 F15 F17 F18 G15 G17 G18
USB I/O

V5_VREF--PCI 5V TOLERANCE

V5_VREF AE7 +5V_VREF, 4mA
R286 1 2 1K/F_4 → +5V
AVDDCK_3.3V J16 +3V_AVDDCK, 7mA
AVDDCK_1.2V K17 +1.2V_AVDDCK, 44mA
AVDDC E9 +3V_AVDDC, 16mA
PLL
C441 1U/10V_4
D14 CH501H-40PT → +3V

U14E SB700 Part 5 of 5

GROUND
VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_32 VSS_33 VSS_34 VSS_35 VSS_36 VSS_37 VSS_38 VSS_39 VSS_40 VSS_41 VSS_42 VSS_43 VSS_44 VSS_45 VSS_46 VSS_47 VSS_48 VSS_49 VSS_50
A2 A25 B1 D7 F20 G19 H8 K9 K11 K16 L4 L7 L10 L11 L12 L14 L16 M6 M10 M11 M13 M15 N4 N12 N14 P6 P9 P10 P11 P13 P15 R1 R2 R4 R9 R10 R12 R14 T11 T12 T14 U4 U14 V6 Y21 AB1 AB19 AB25 AE1 AE24
AVSS_SATA_1 AVSS_SATA_2 AVSS_SATA_3 AVSS_SATA_4 AVSS_SATA_5 AVSS_SATA_6 AVSS_SATA_7 AVSS_SATA_8 AVSS_SATA_9 AVSS_SATA_10 AVSS_SATA_11 AVSS_SATA_12 AVSS_SATA_13 AVSS_SATA_14 AVSS_SATA_15 AVSS_SATA_16 AVSS_SATA_17 AVSS_SATA_18 AVSS_SATA_19 AVSS_SATA_20
T10 U10 U11 U12 V11 V14 W9 Y9 Y11 Y14 Y17 AA9 AB9 AB11 AB13 AB15 AB17 AC8 AD8 AE8
AVSS_USB_1 AVSS_USB_2 AVSS_USB_3 AVSS_USB_4 AVSS_USB_5 AVSS_USB_6 AVSS_USB_7 AVSS_USB_8 AVSS_USB_9 AVSS_USB_10 AVSS_USB_11 AVSS_USB_12 AVSS_USB_13 AVSS_USB_14 AVSS_USB_15 AVSS_USB_16 AVSS_USB_17 AVSS_USB_18 AVSS_USB_19 AVSS_USB_20 AVSS_USB_21 AVSS_USB_22 AVSS_USB_23 AVSS_USB_24
A15 B15 C14 D8 D9 D11 D13 D14 D15 E15 F12 F14 G9 H9 H17 J9 J11 J12 J14 J15 K10 K12 K14 K15
PCIE_CK_VSS_1 PCIE_CK_VSS_2 PCIE_CK_VSS_3 PCIE_CK_VSS_4 PCIE_CK_VSS_5 PCIE_CK_VSS_6 PCIE_CK_VSS_7 PCIE_CK_VSS_8 PCIE_CK_VSS_9 PCIE_CK_VSS_10 PCIE_CK_VSS_11 PCIE_CK_VSS_12 PCIE_CK_VSS_13 PCIE_CK_VSS_14 PCIE_CK_VSS_15 PCIE_CK_VSS_16 PCIE_CK_VSS_17 PCIE_CK_VSS_18 PCIE_CK_VSS_19 PCIE_CK_VSS_20 PCIE_CK_VSS_21
H18 J17 J22 K25 M16 M17 M21 P16
P23 R16 R19 T17 U18 U20 V18 V20 V21 W19 W22 W24 W25
AVSSC F9
AVSSCK L17

SB710

USB_PHY_1.2V--USB Phy digital power

+1.2V_S5 → R198 short0603 → +1.2V_USB_PHY_R
C338 0.1U/10V_4, C341 0.1U/10V_4, C330 10U/6.3V_8

B2A to C3A

AVDDC--USB Analog PLL power

+3V_S5 → L34 BLM18PG221SN1D → +3V_AVDDC
C475 0.1U/10V_4, C337 10U/6.3V_8

AVDDCK_1.2--USB Phy digital power

+1.2V → L36 BLM18PG221SN1D → +1.2V_AVDDCK
C468 2.2U/6.3V_6

AVDDCK_3.3--Analog system PLL power

+3V → L35 BLM18PG221SN1D → +3V_AVDDCK
C474 2.2U/6.3V_6

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	SB710-PWR/DECOUPLING 4/4	3A
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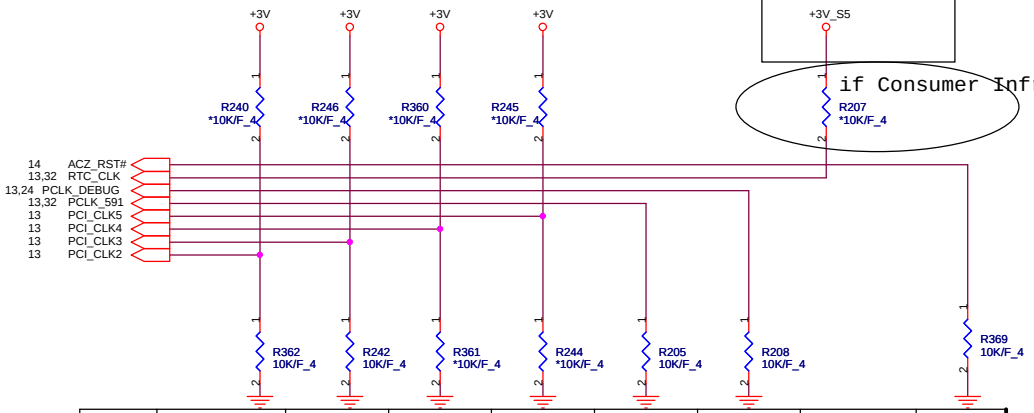
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

It must ready refore RSMRST#

if Consumer Infrared is implemented

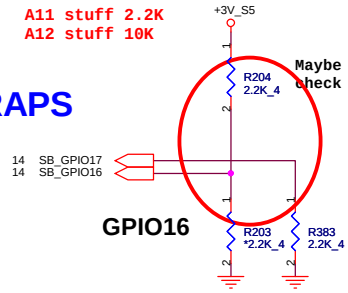
REQUIRED STRAPS



	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT
	EC ENABLED							ENABLE PCI MEM BOOT

A11 stuff 2.2K
A12 stuff 10K

Maybe can be remove -- internla pull up check AMD



GPIO16 GPIO17

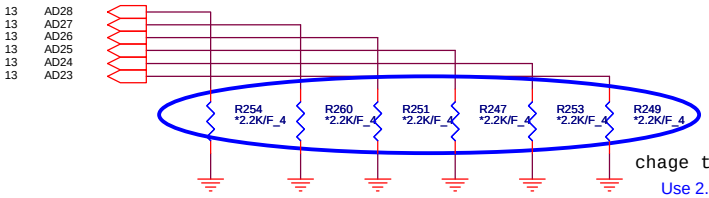
TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

SB_PWRGD
A11 use external ckt
A12 Asserting SYS_RESET# will de-assert SB PWRGOOD internally

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

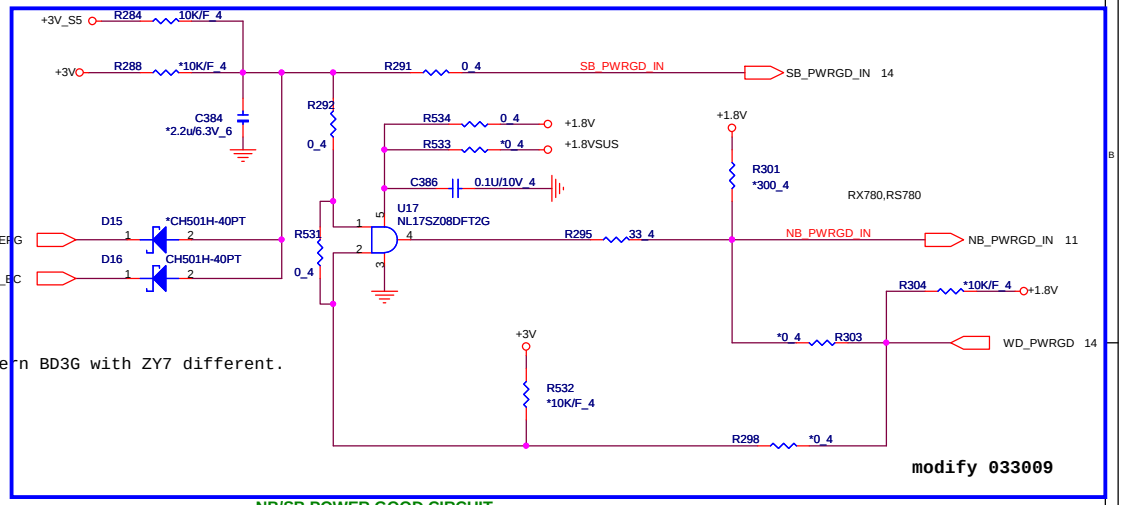
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



chage to 2.2k 0217
Use 2.2K PD.

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



Impotern BD3G with ZY7 different.

NB/SB POWER GOOD CIRCUIT

WD_PWRGD: Push/Pull when A11SB700, OD when A12SB700.

	U11	R230	R229	R245	R234
RX780 RS780M	V	V	V	X	X

AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

Quanta Computer Inc.
PROJECT : ZK8

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	SB710-STRAPS	3A
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(VGA)

R433 for PEX_Swing adjust
NC for default low swing mode
GND for standard(desktop) mode

Add 0211

PEX_Swing adjust

Add 0211

Close CN36 MXMconnector for Layout concern

HPD Pin : 100KR PD on module

(VGA)

PLTRST# from NB_RST# (A_RST#_SB)

(VGA)

EC SMBUS

delete 0225

MXM PWR_GOOD internal PU 100K to +3V

Add 0211

Same as AJ6

B2A to C3A

Add 0217

(VGA)

(VGA)

B2A to C3A

MXM 3V/5V Power switch

B2A to C3A

Add 0213

PE_GPIO1
1 : MXMPWR_EN
0 : Disable MXMPWR

Quanta Computer Inc.		
PROJECT : ZK8		
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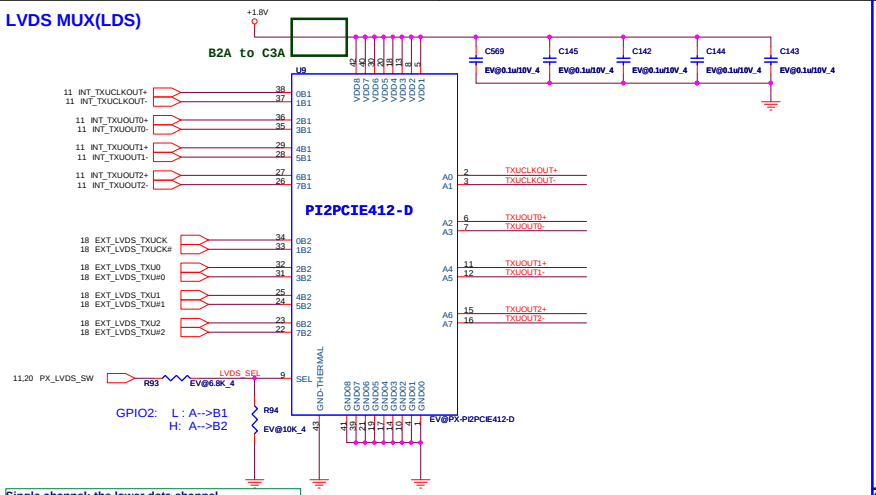
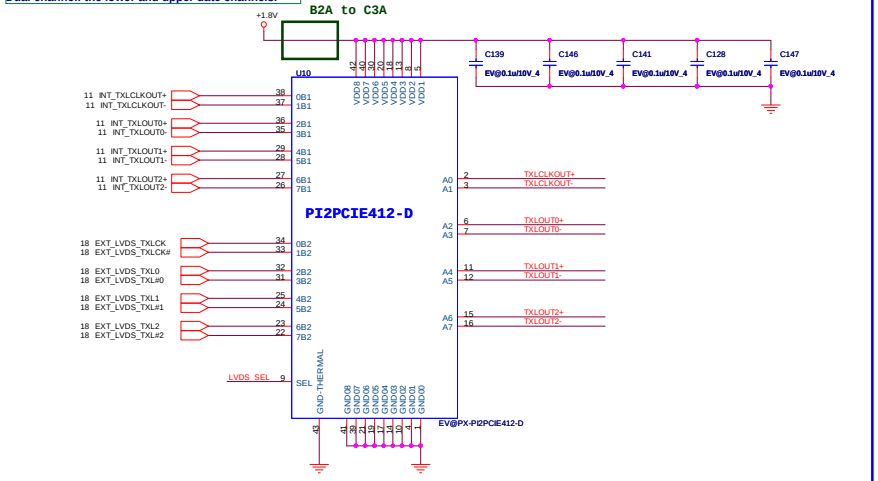
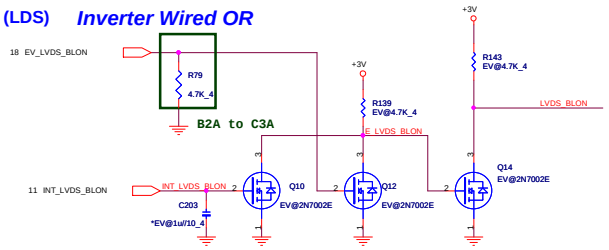
LVDS MUX(LDS)

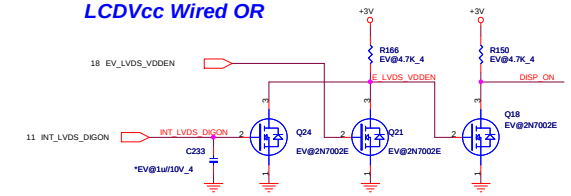




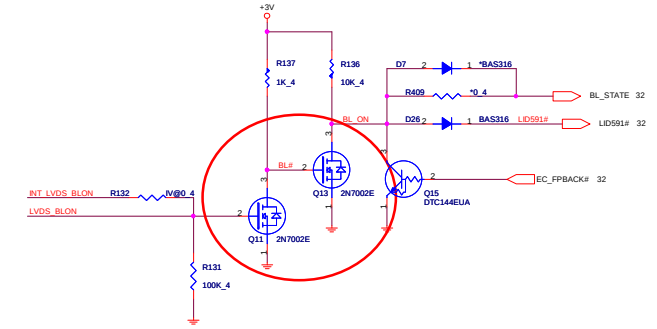
(LDS) Inverter Wired OR



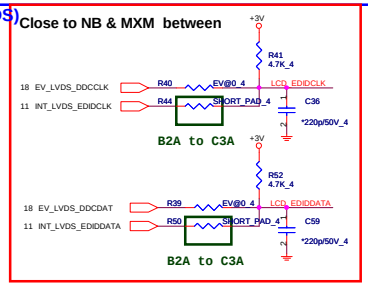
LCDVcc Wired OR

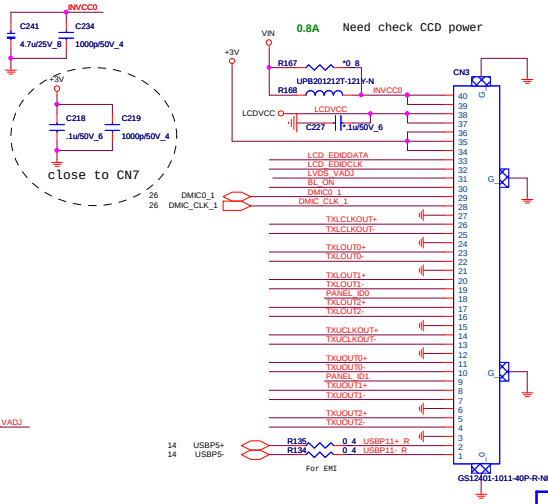


(LDS)



(LDS) Close to NB & MXM between



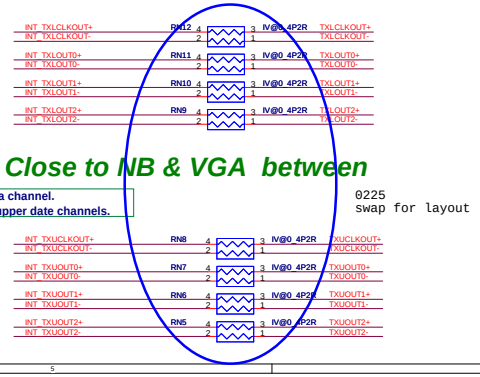


Panel ID

remove or !?

P_ID1	P_ID0	Resolution
0	0	DUAL CH
0	1	SINGLE CH
1	0	Reserved
1	1	Reserved

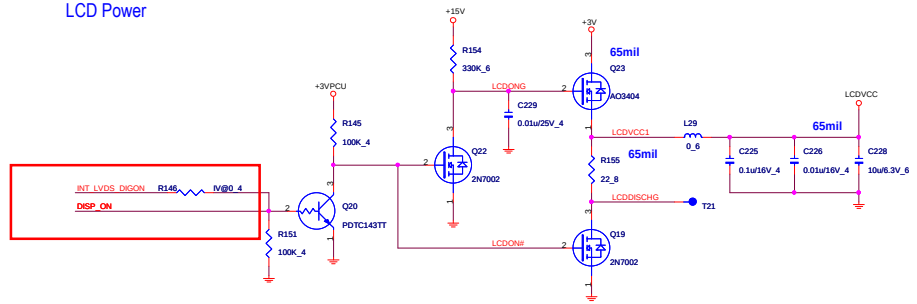
(LDS) Close to NB & VGA between



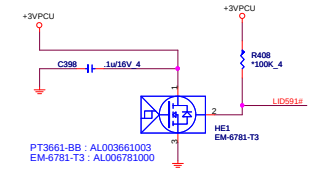
Single channel: the lower data channel.
Dual channel: the lower and upper date channels.

0225
swap for layout

(LDS) LCD Power



Hall sensor(HSR)



Lid Switch (Hall sensor)

Quanta Computer Inc.
PROJECT : ZK8

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	LVDS/LID/Hall IC	3A

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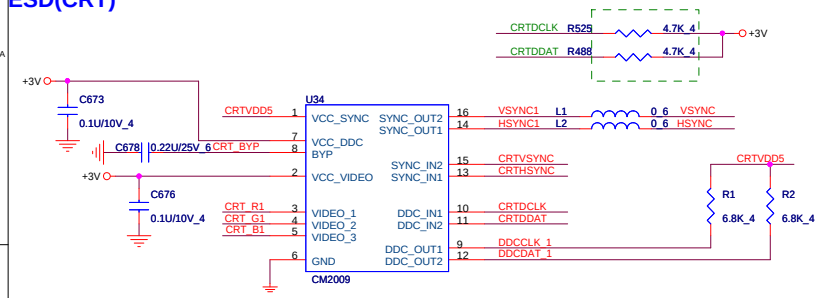
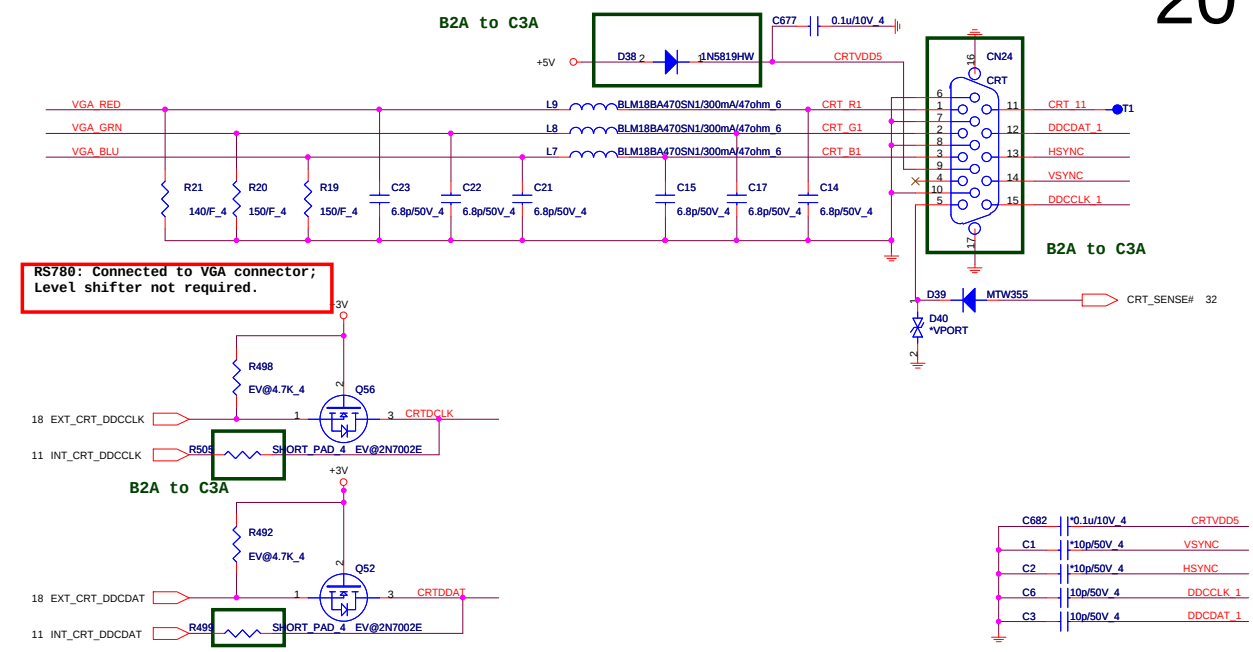
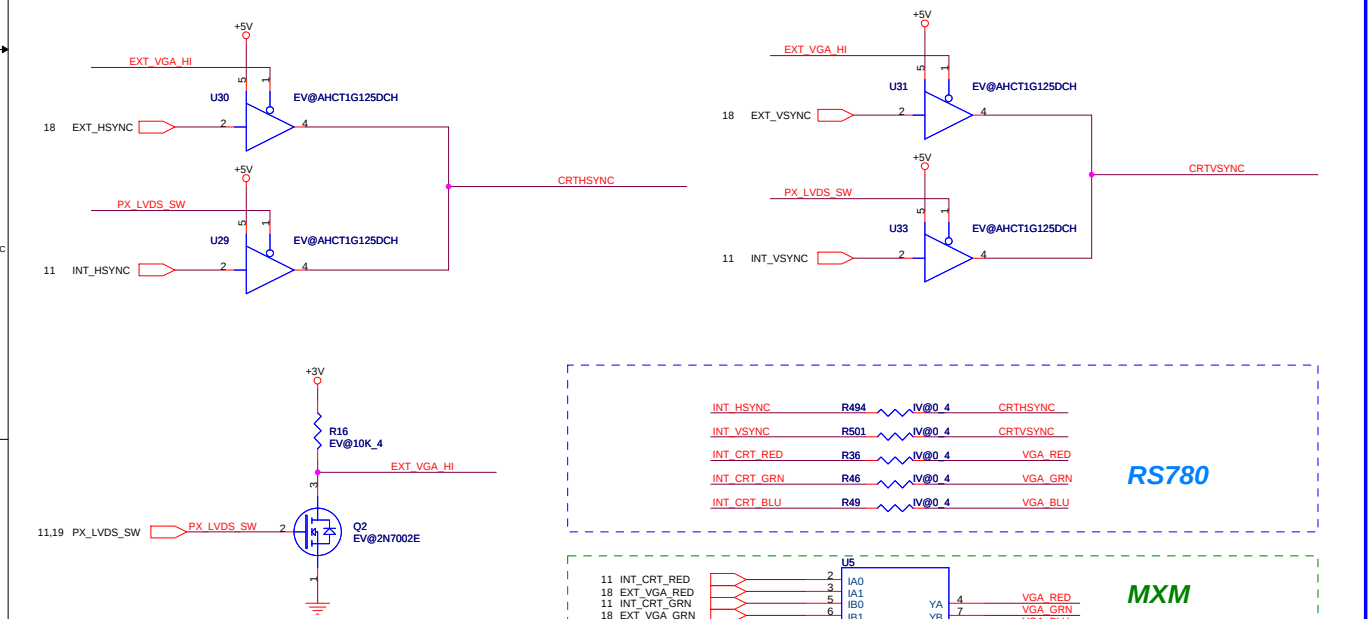
ESD(CRT)



CRT(CRT)



CRT MUX(CRT)



inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

DISPLAY SUPPORT TABLE

	PX_EN	PE_GPIO2_NB	INT_VGA_EN#	DISPLAY OUTPUT
IGP only mode	0	X	0	IGP(LVDS,VGA,HDMI,DP)
MXM only mode	0	X	1	MXM(LVDS,VGA,HDMI,DP)
Power Express mode	1	0/1	X	*MXM(VGA,HDMI,DP); MXM/IGP(LVDS)
IGP + MXM	0	X	0	IGP(LVDS,VGA,HDMI)

PX mode display device auto detection method:
VGA: I2C interface to NB
HDMI/DVI: HPD, I2C is optional
DP: HPD

Quanta Computer Inc.
PROJECT : ZK8

Size	Document Number	Rev
	CRT/CCD	3A
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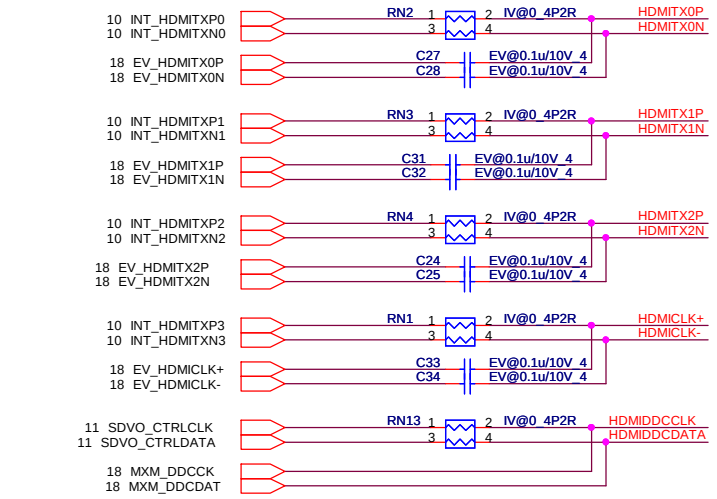
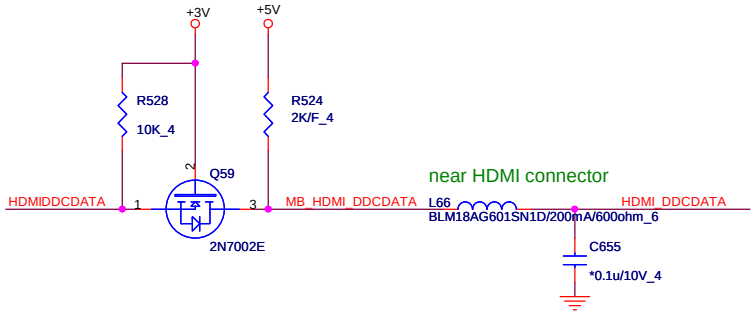
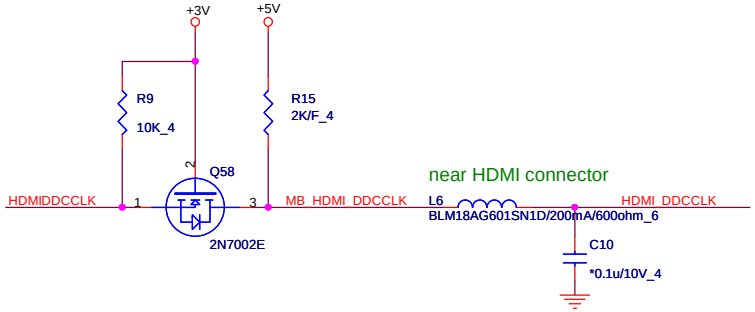
(HDM)

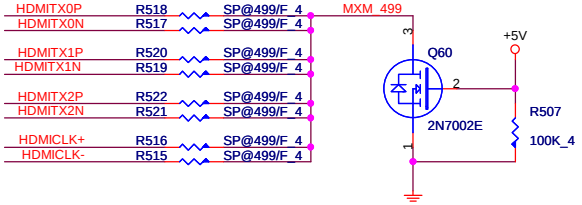




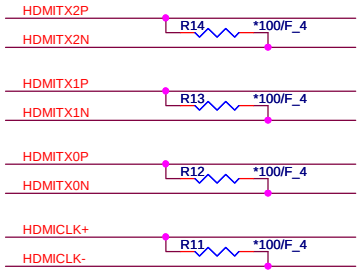


(HDM)

EV @ 499R/F CS14992FB24
IV @ 750R/F CS17502FB19



(HDM) for EMI



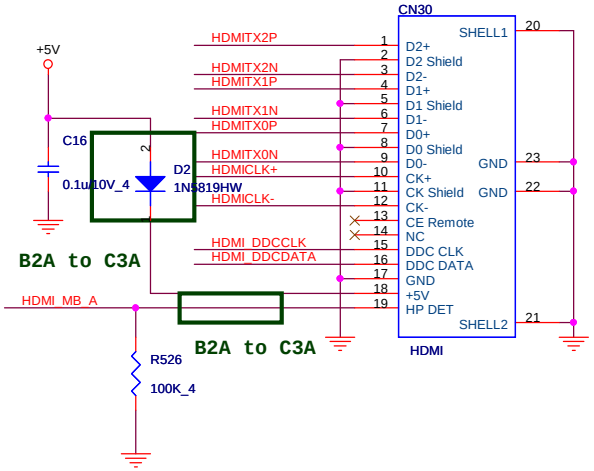
(HDM) CLOSE CN9

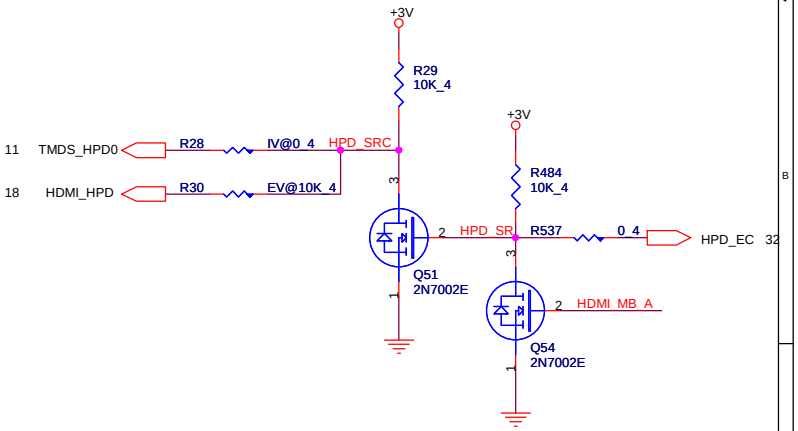
B2A to C3A

delete for UMA SI issue

(HDM)

HDMI connector





Quanta Computer Inc.
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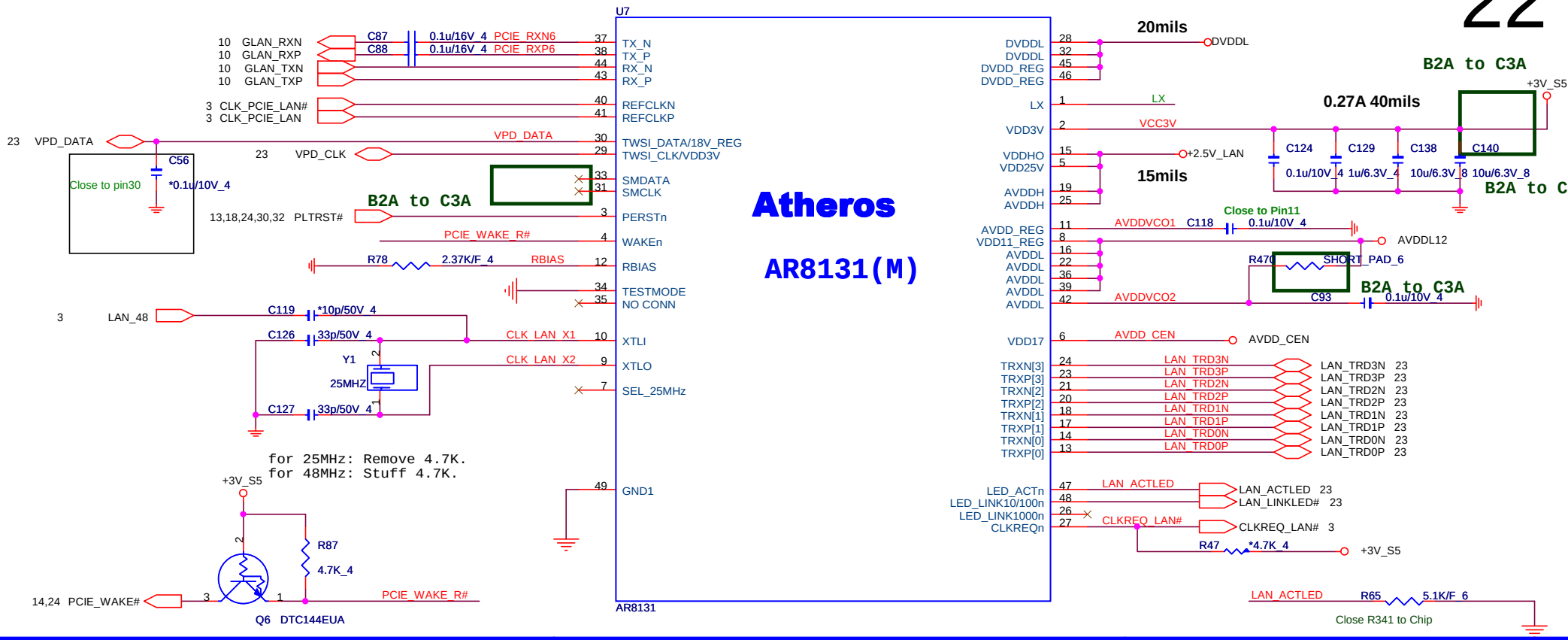
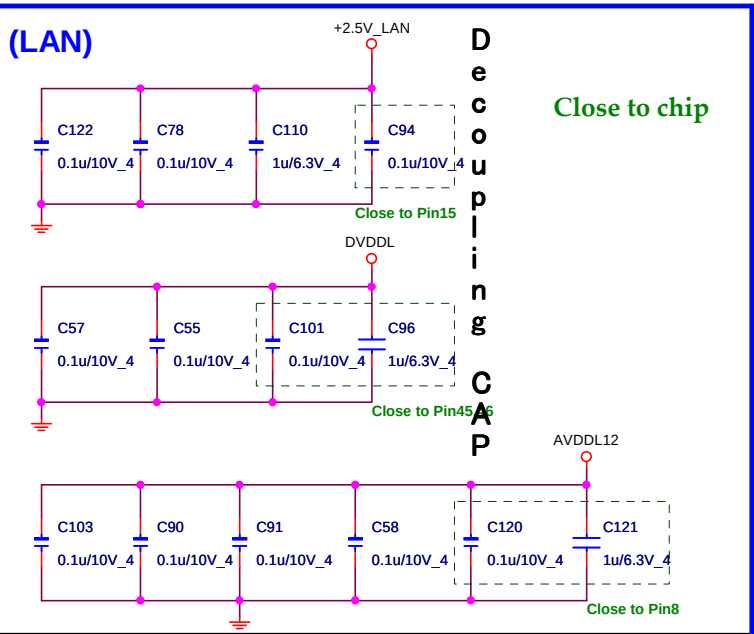
LAN(LAN)

22



(LAN)



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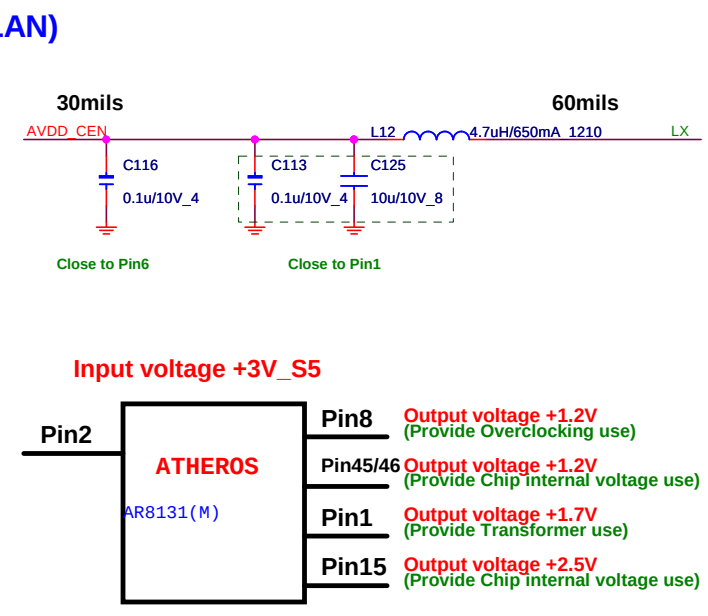
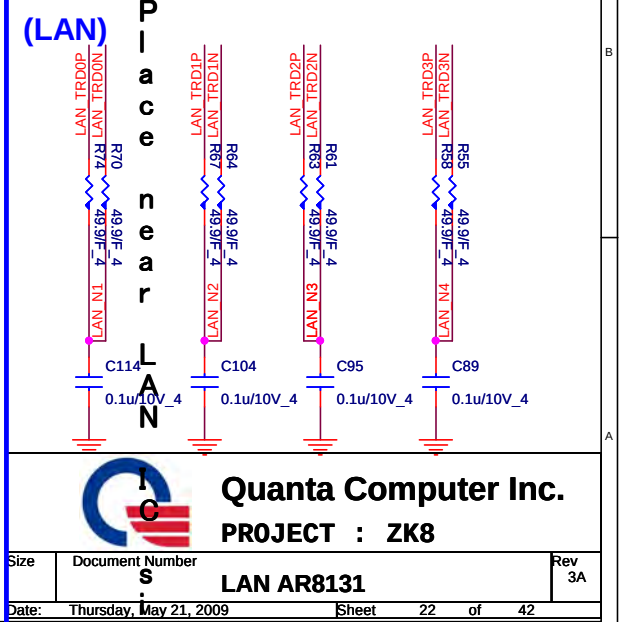


(LAN)



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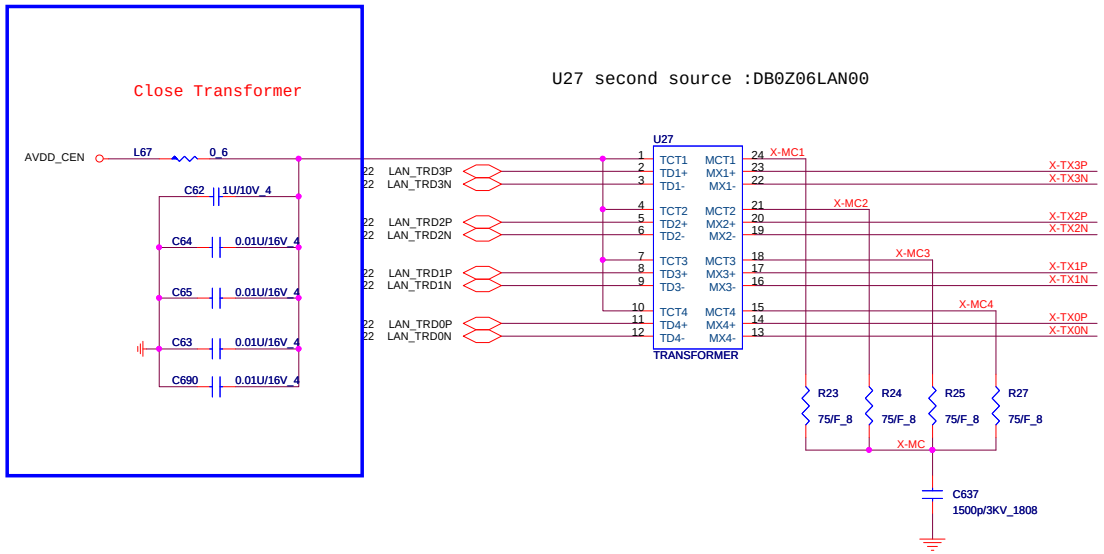
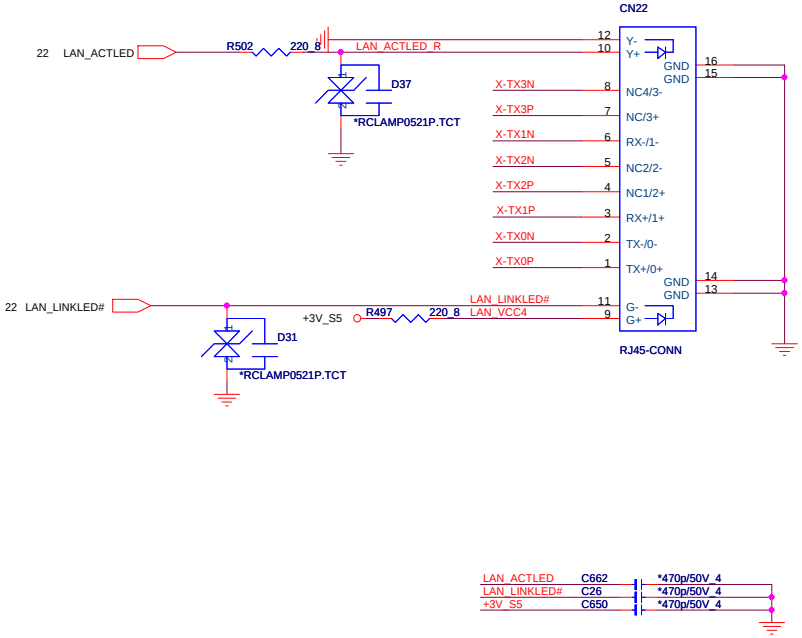
TRANSFORMER(LAN)

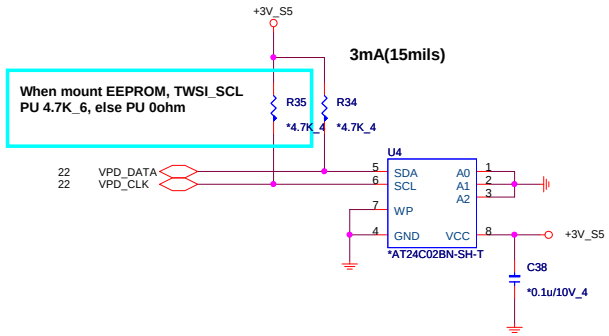


BOTHHAND GST-5009 (DBKN1NLAN03)
Delta LFE9291-R (DB0BD3LAN00)

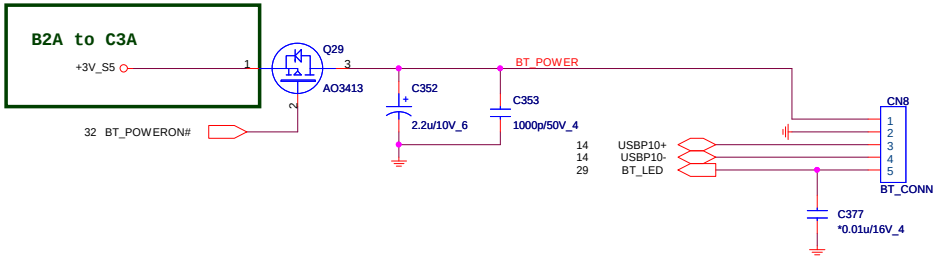
RJ45(LAN)



EEPROM(LAN)



BLUETOOTH MODULE CONNECTOR(BTM)



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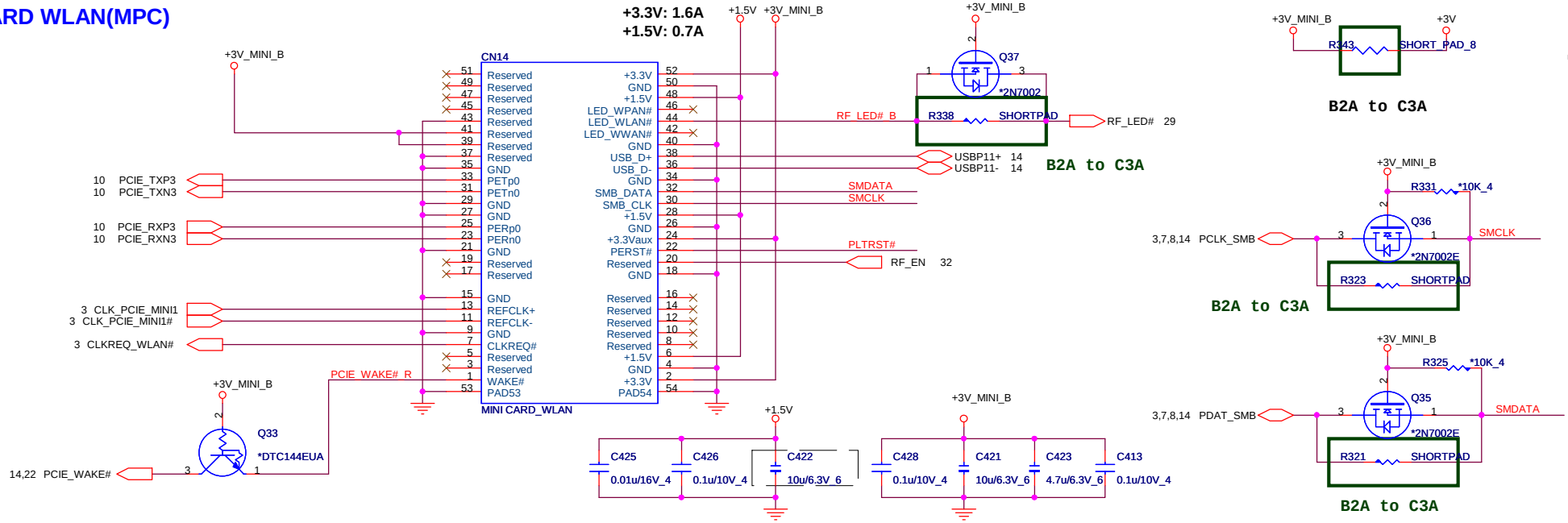
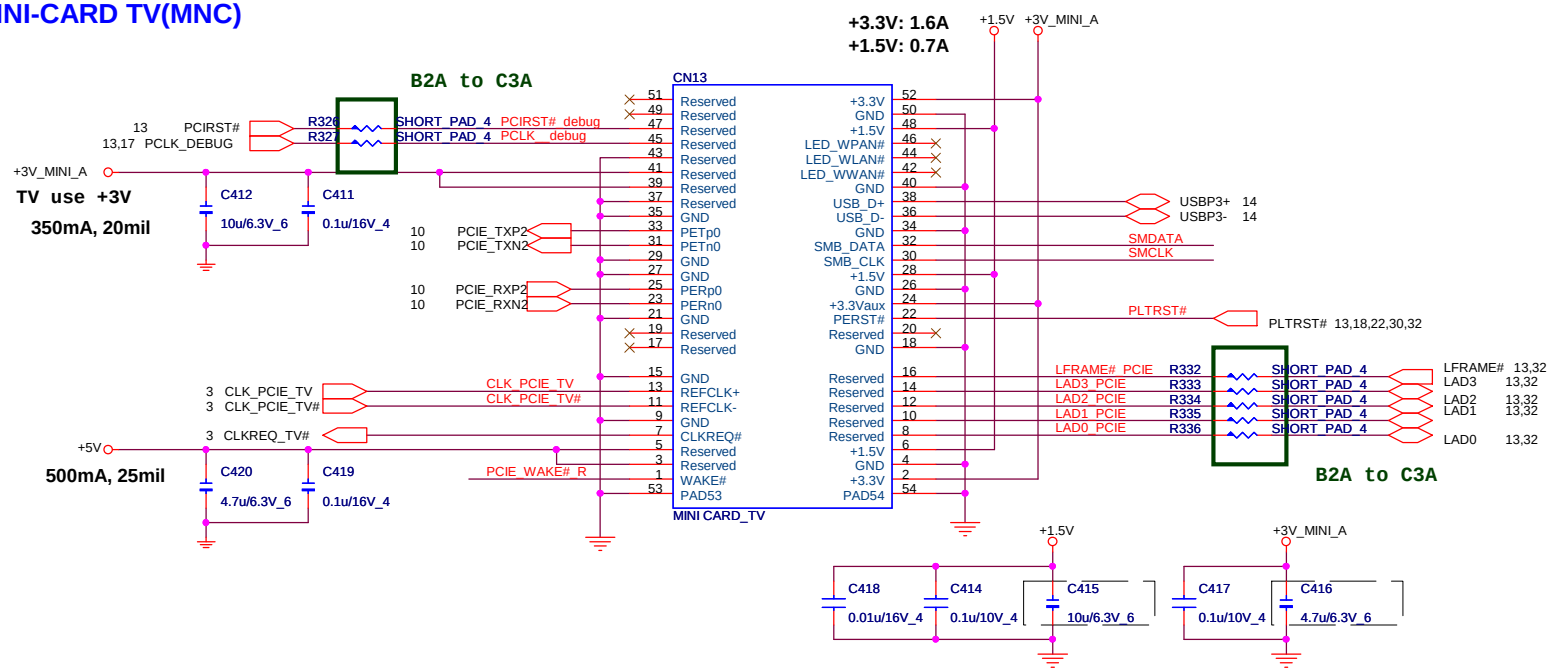
MINI-CARD WLAN(MPC)



MINI-CARD TV(MNC)



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Size	Document Number	Rev
	MINI PCI-E card/TV	3A
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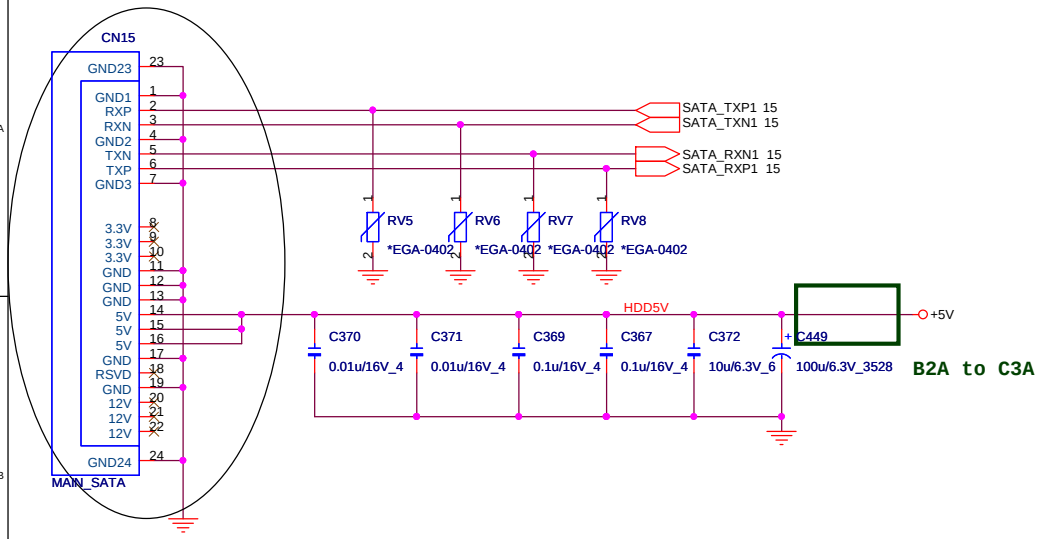
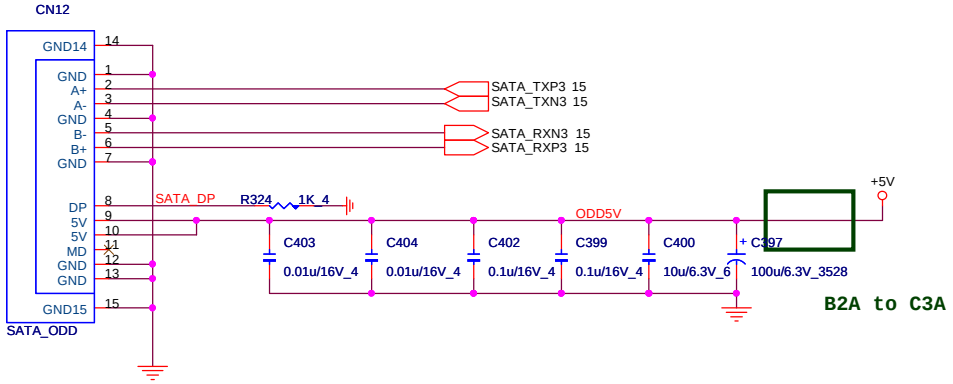
SATA HDD(HDD)



ODD (ODD)



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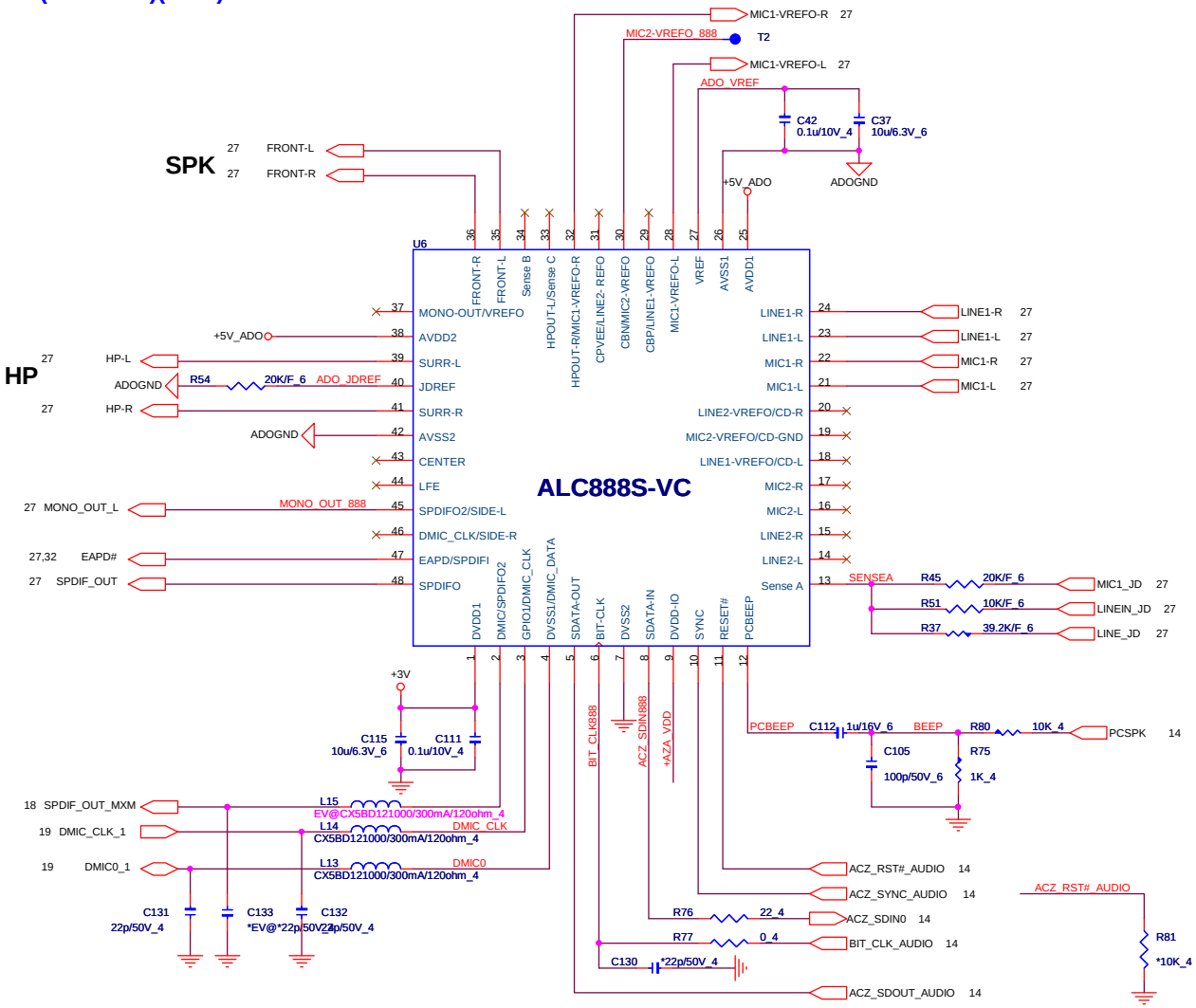
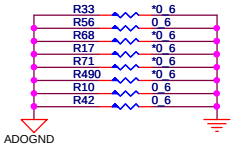
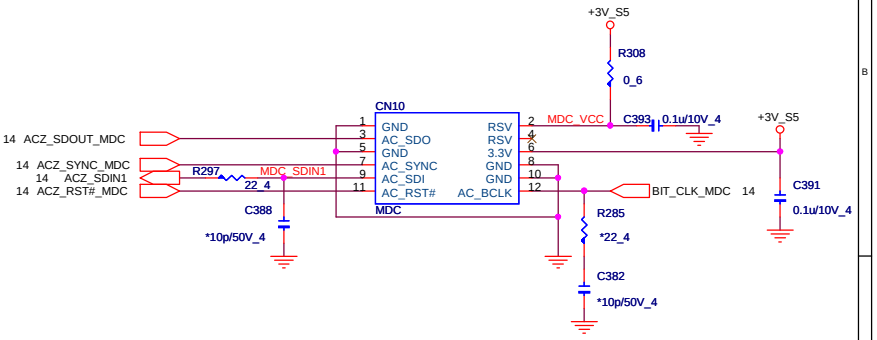
CODEC(ALC888S)(ADO)



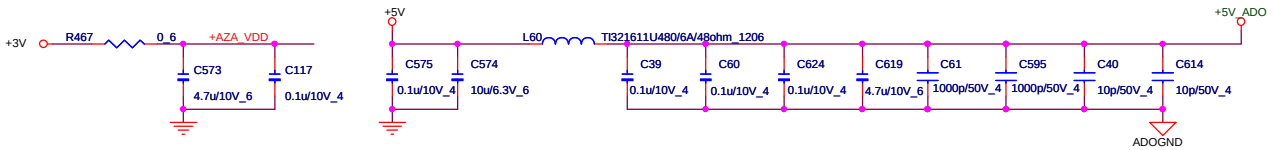
(ADO)



MDC(MDC)



Codec Power(ADO)



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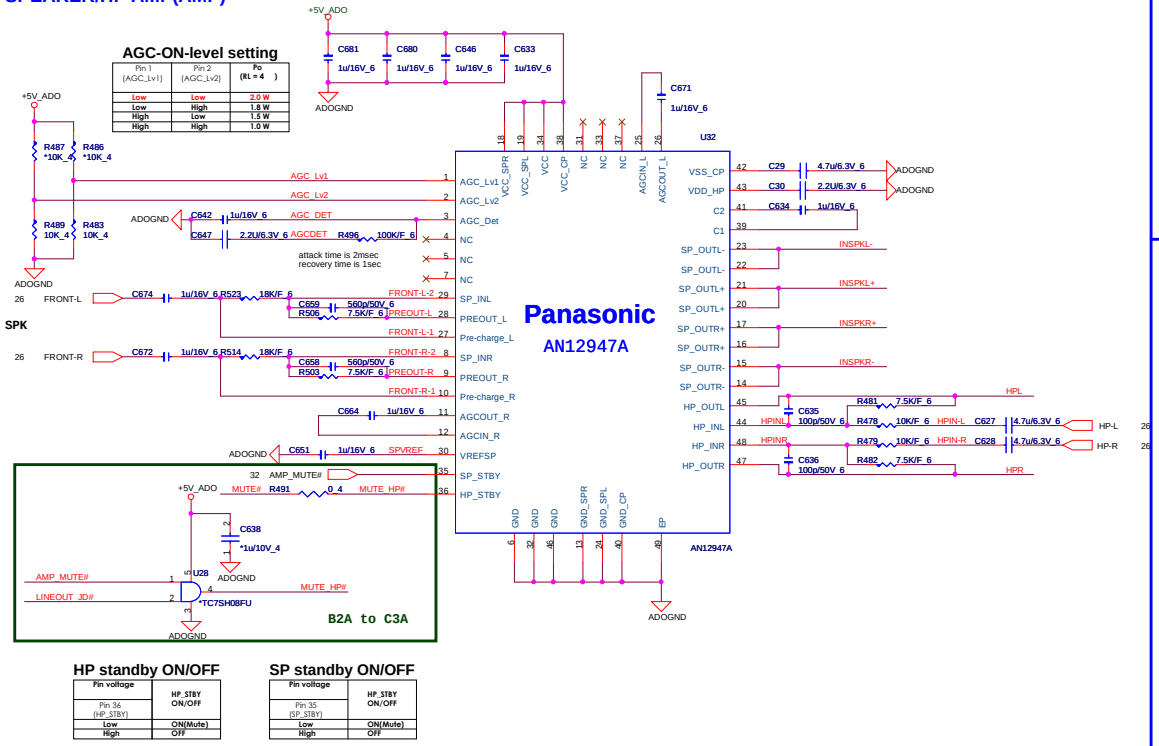
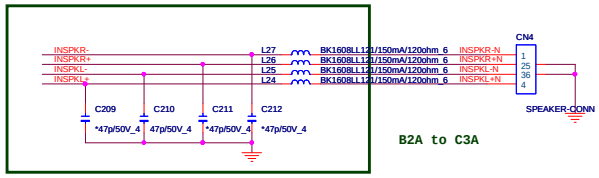
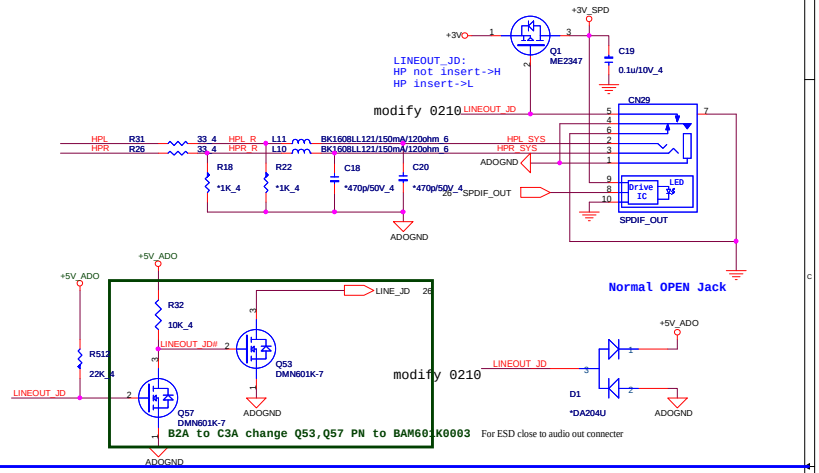
SPEAKER/HP AMP(AMP)



SPEAKER(AMP)

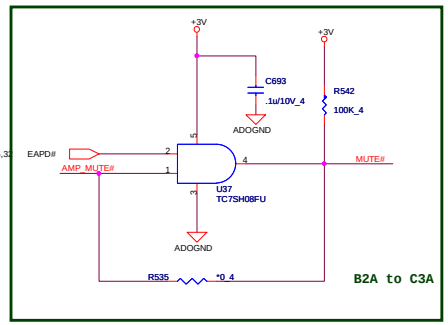


LINE-OUT/SPDIF(AMP)



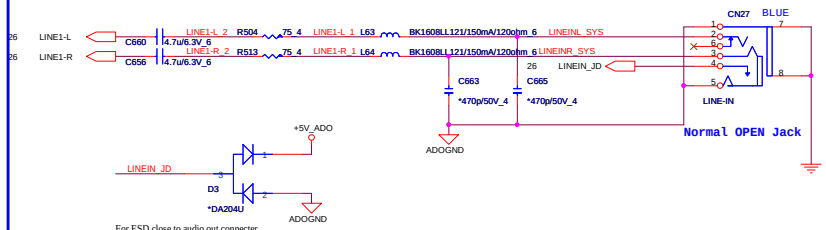
MUTE(AMP)

EAPD# (codec mute)
AMP_MUTE# (EC mute)
MUTE# (mute all AMP)
SUB_MUTE# (mute subwoofer)

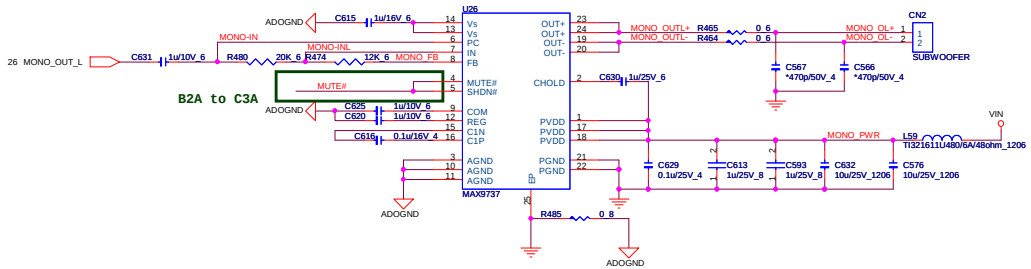


LINE IN(AMP)

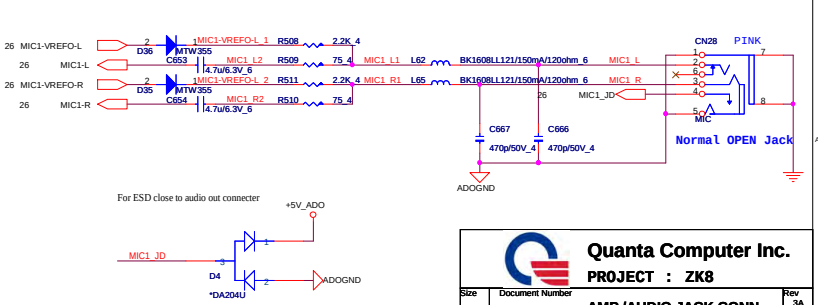
modify 0210



SUBWOOFER(AMP)



MIC(AMP)



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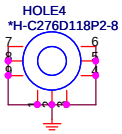
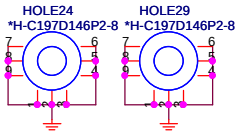
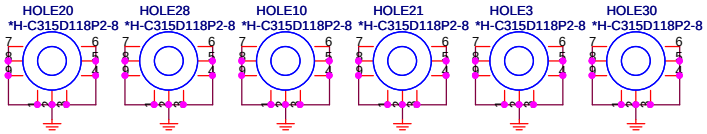
HOLES

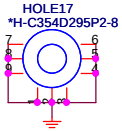
H-C276D118P2-8 -- 1 pcs

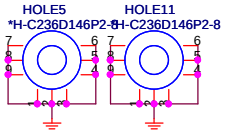


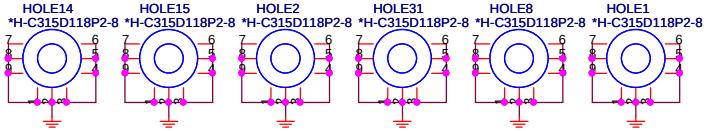


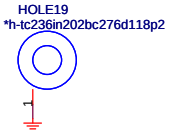


H-C354D295P2-8 -- 1 pcs

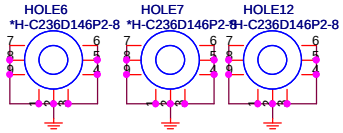




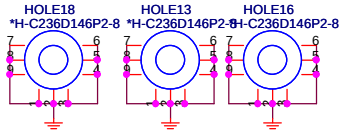




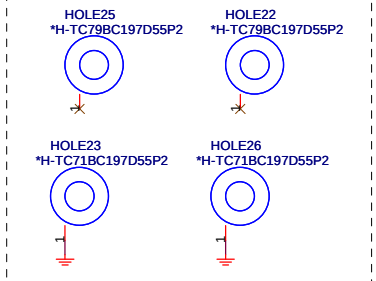
H-C236D146P2-8 -- 8 pcs



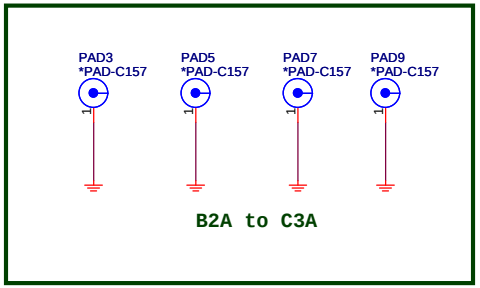
MXM



CPU



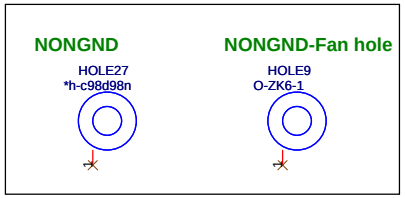
MINI CARD

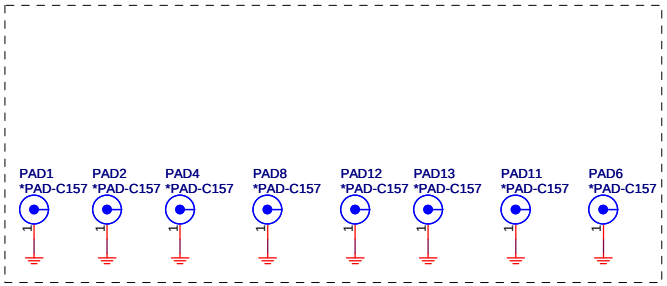


B2A to C3A

NONGND

NONGND-Fan hole





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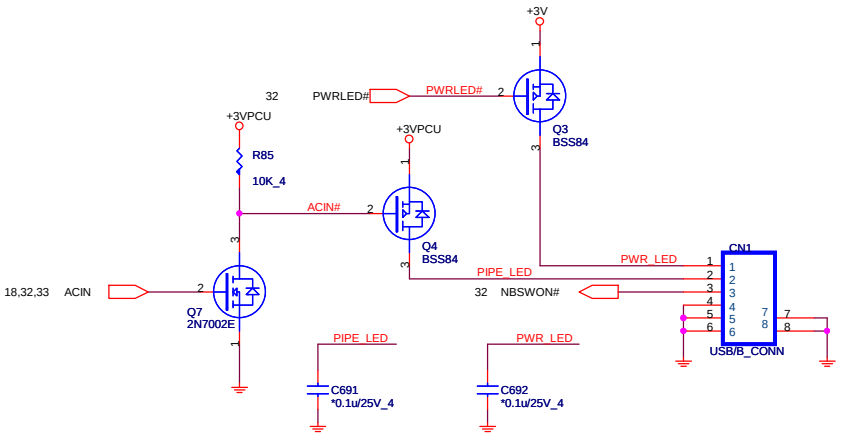
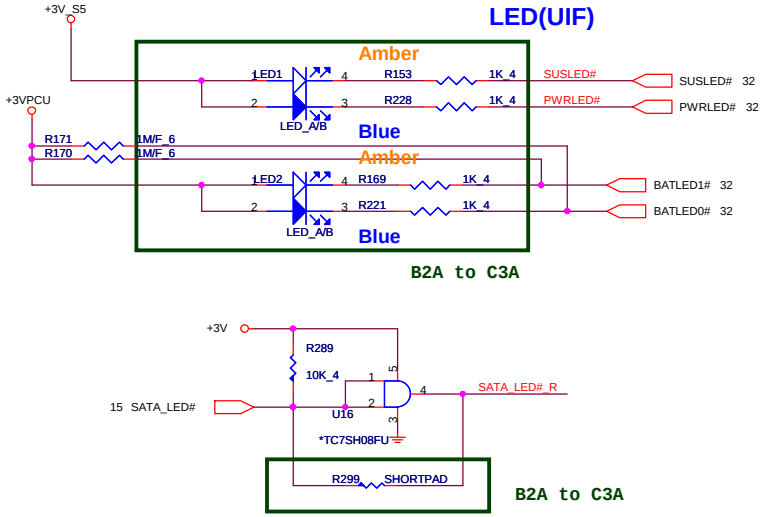
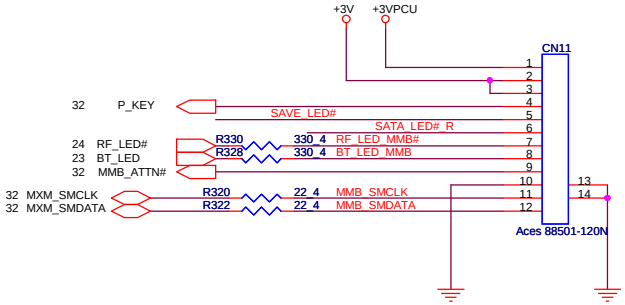
POWER BOARD(UIF)

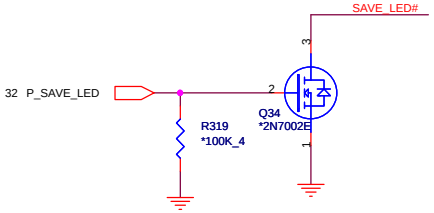


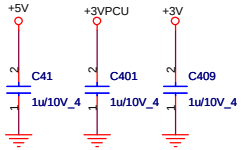
LED(UIF)



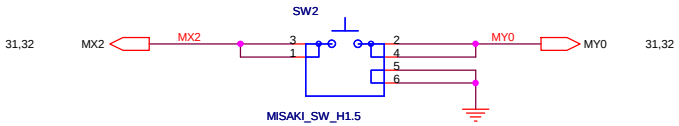
MMB(MMB)

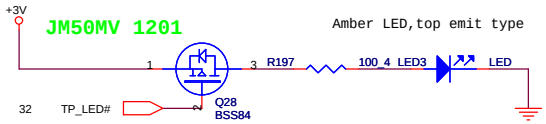






TP_LOCK BUTTON(UIF)





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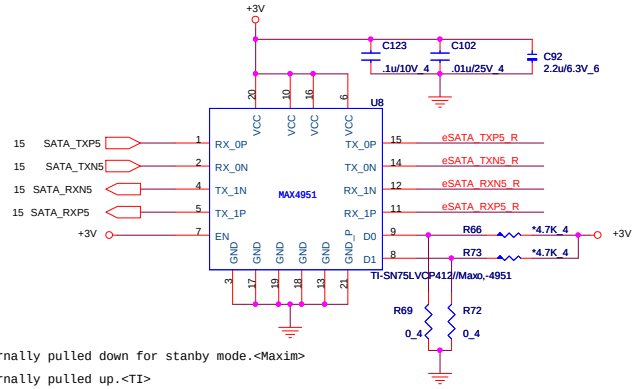
eSATA Redriver(ESA)



Pin-7 ::EN is internally pulled down for stanby mode.<Maxim>

Pin-7 ::EN is internally pulled up.<TI>

Pin-8 ::BB is internally pulled down.<TI/MAXIM>

Pin-9 ::BA is internally pulled down.<TI/MAXIM>

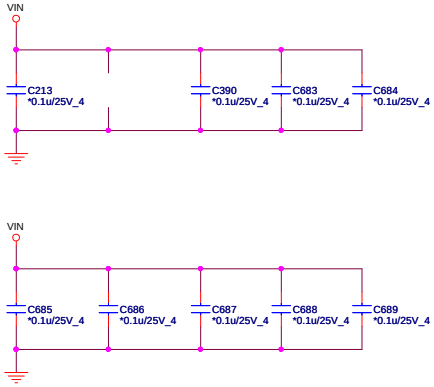
EN	BA/D0	BB/D1	CH-0/A	CH-1/B
0	X	X	Standby	Standby
1	0	0	0dB	0dB
1	1	0	Pre-emphasis (5dB)	0dB
1	0	1	0dB	Pre-emphasis (5dB)
1	1	1	Pre-emphasis (5dB)	Pre-emphasis (5dB)

X=don't care

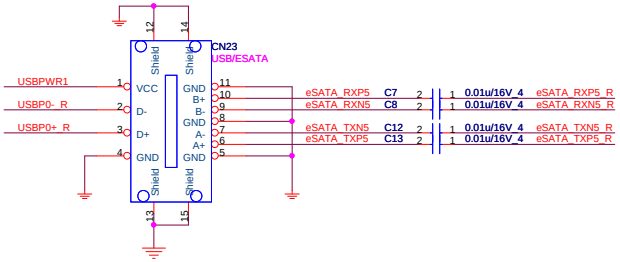
DG2.1 4.2.4 Terminating Unused SATA Interface

SATA[1:0]RXp/n, SATA[5:4]RXp/n connect to GND while SATA not be implemented

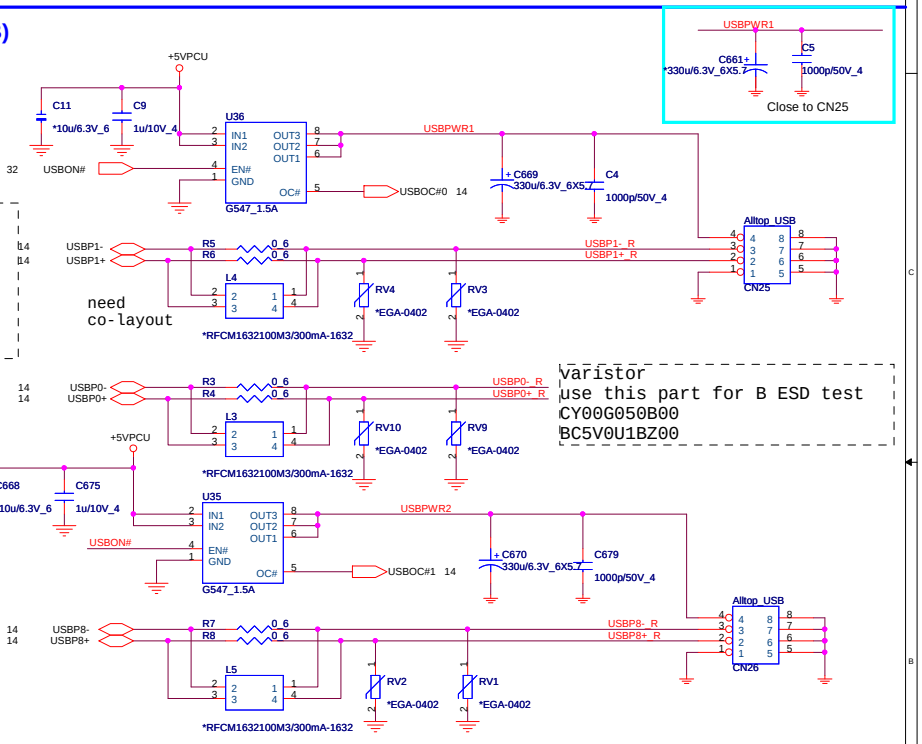
EMI CAPS



USB&ESATA(ESA)



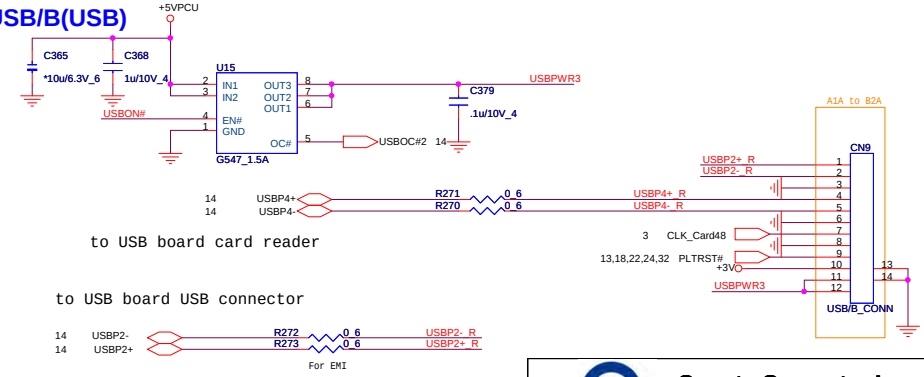
(USB)



USBPWR1
C661+ *330u/6.3V_6X5.7
C5 1000p/50V_4
Close to CN25

varistor
use this part for B ESD test
CY00G050B00
BC5V0U1BZ00

USB/B(USB)



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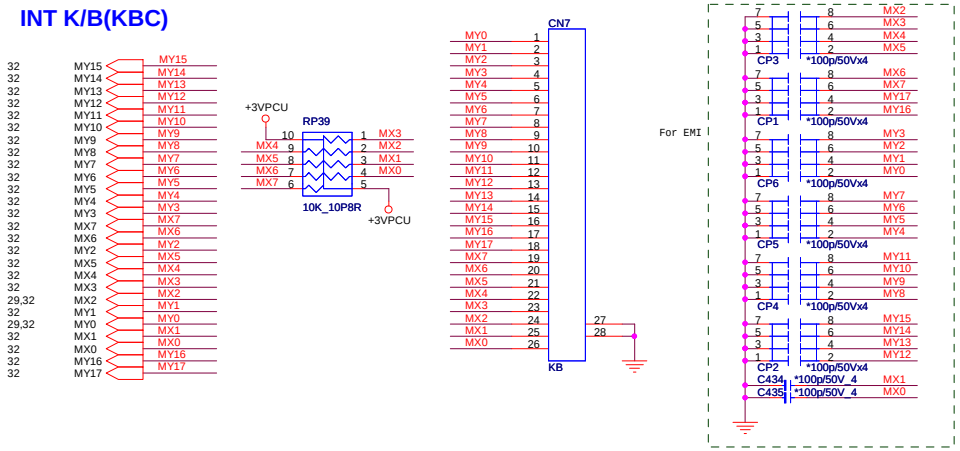
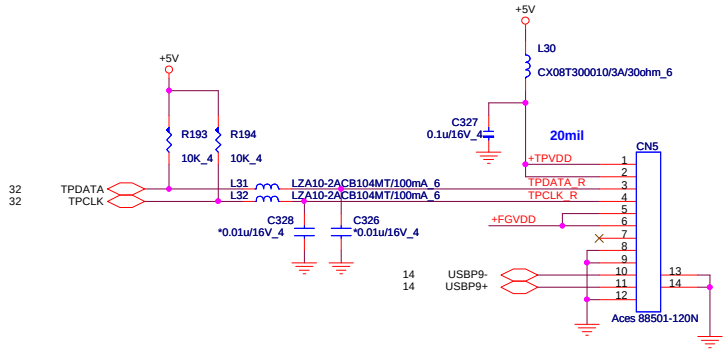
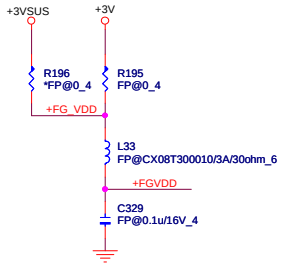
INT K/B(KBC)



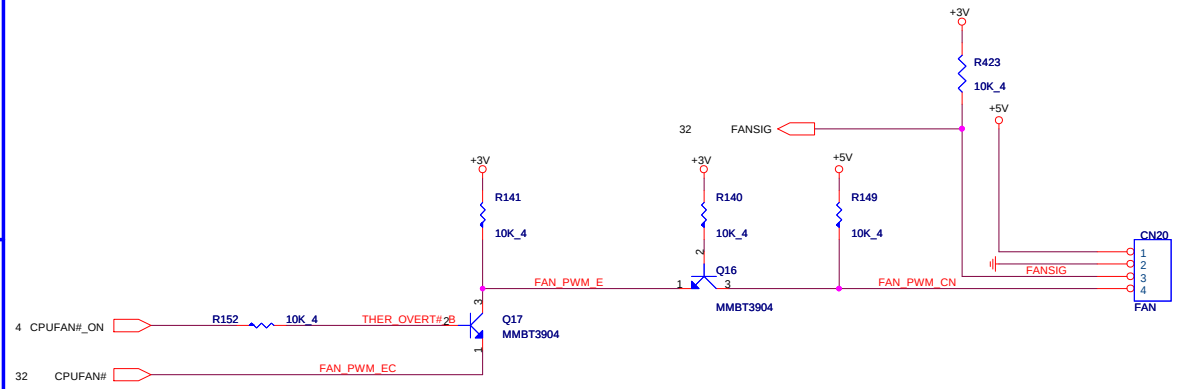
TOUCHPAD & Finger Printer CONN.(TPD)



(FPD)



CPU FAN(THM)



Quanta Computer Inc.	
PROJECT : ZK8	
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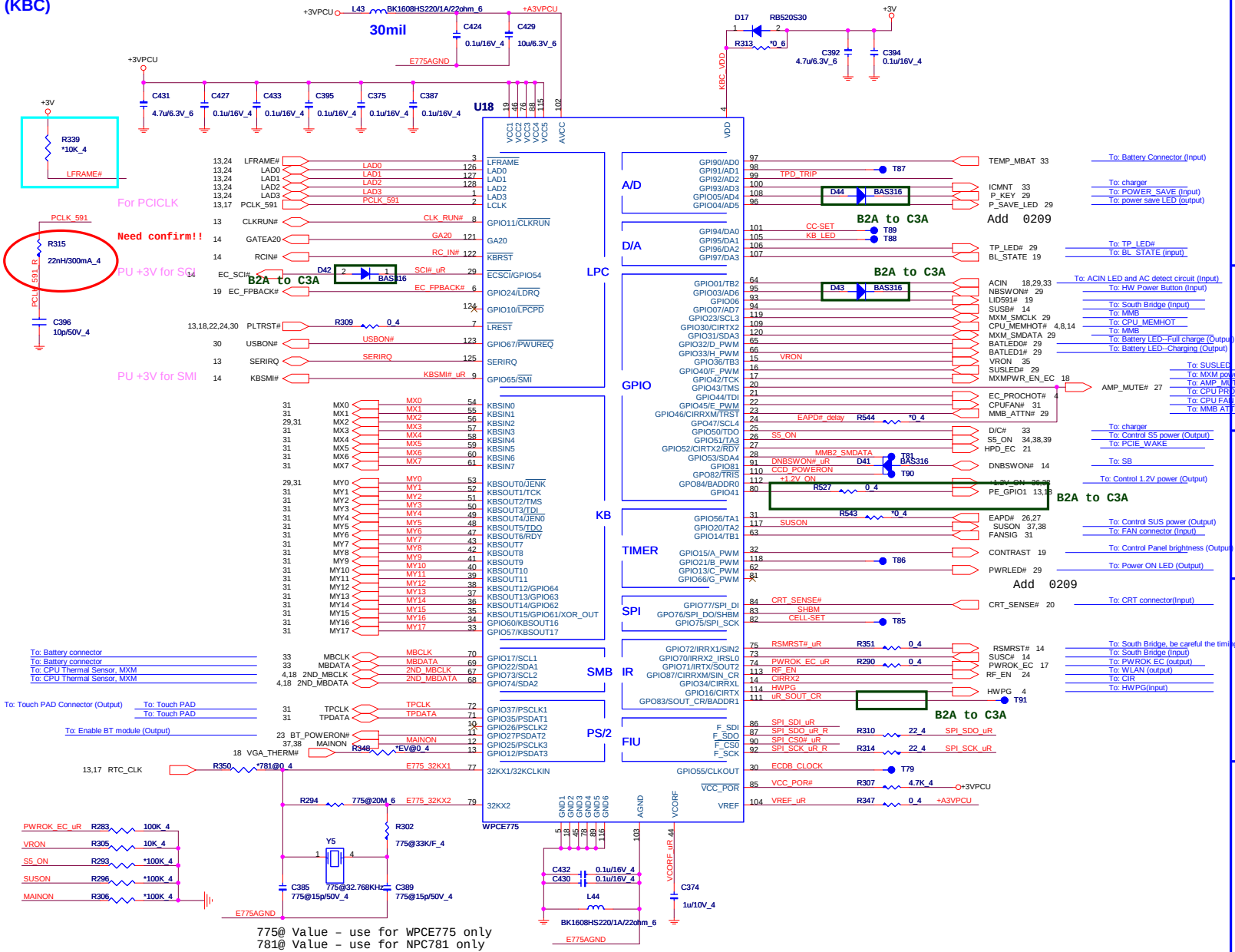
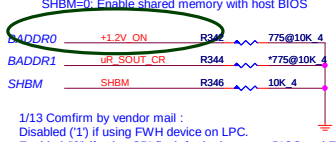
(KBC)



I/O ADDRESS SETTING(KBC)

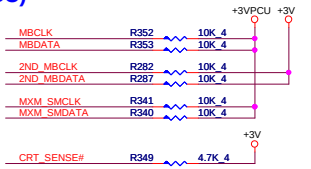
BADDR1-0	I/O Address	
	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

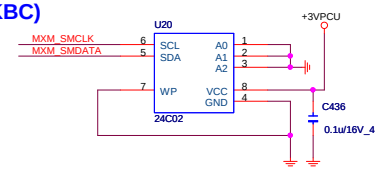


1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

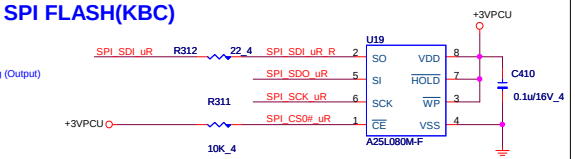
SM BUS PU(KBC)



ACER ID(KBC)

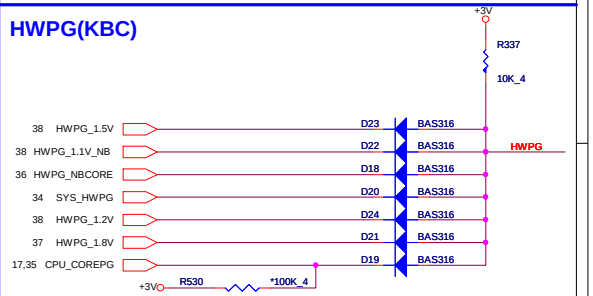


SPI FLASH(KBC)

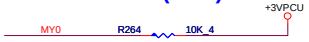


If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

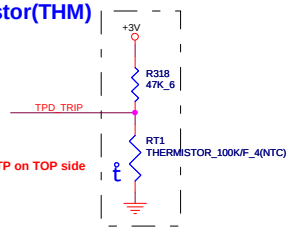
HWPG(KBC)



INTERNAL KEYBOARD STRIP SET(KBC)

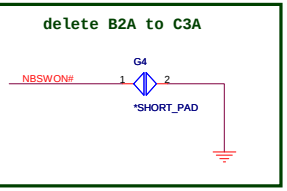


Thermistor(THM)

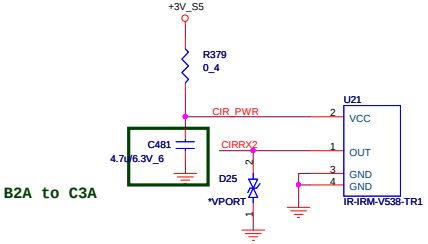


POWER SWITCH(KBC)

delete B2A to C3A



CIR(FIR)



B2A to C3A

Quanta Computer Inc.			
PROJECT : ZK8			
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	WPCE775C_0DG & FLASH		3A
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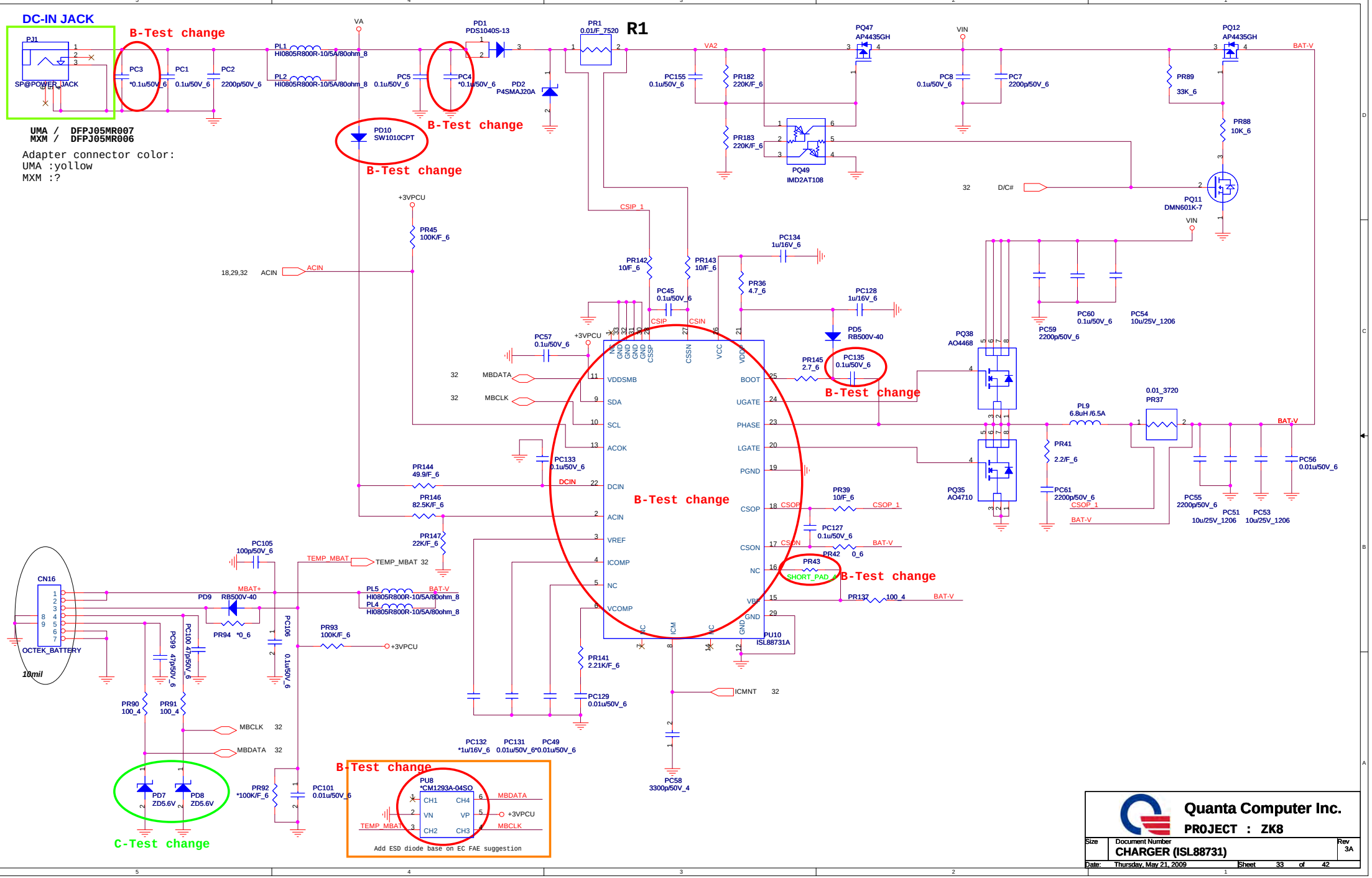
DC-IN JACK
B-Test change
R1
UMA / DFPJ05MR007
MXM / DFPJ05MR006
Adapter connector color:
UMA :yollow
MXM :?
B-Test change
B-Test change
B-Test change
B-Test change
B-Test change
B-Test change
C-Test change
Add ESD diode base on EC FAE suggestion
Quanta Computer Inc.
PROJECT : ZK8
CHARGER (ISL88731)
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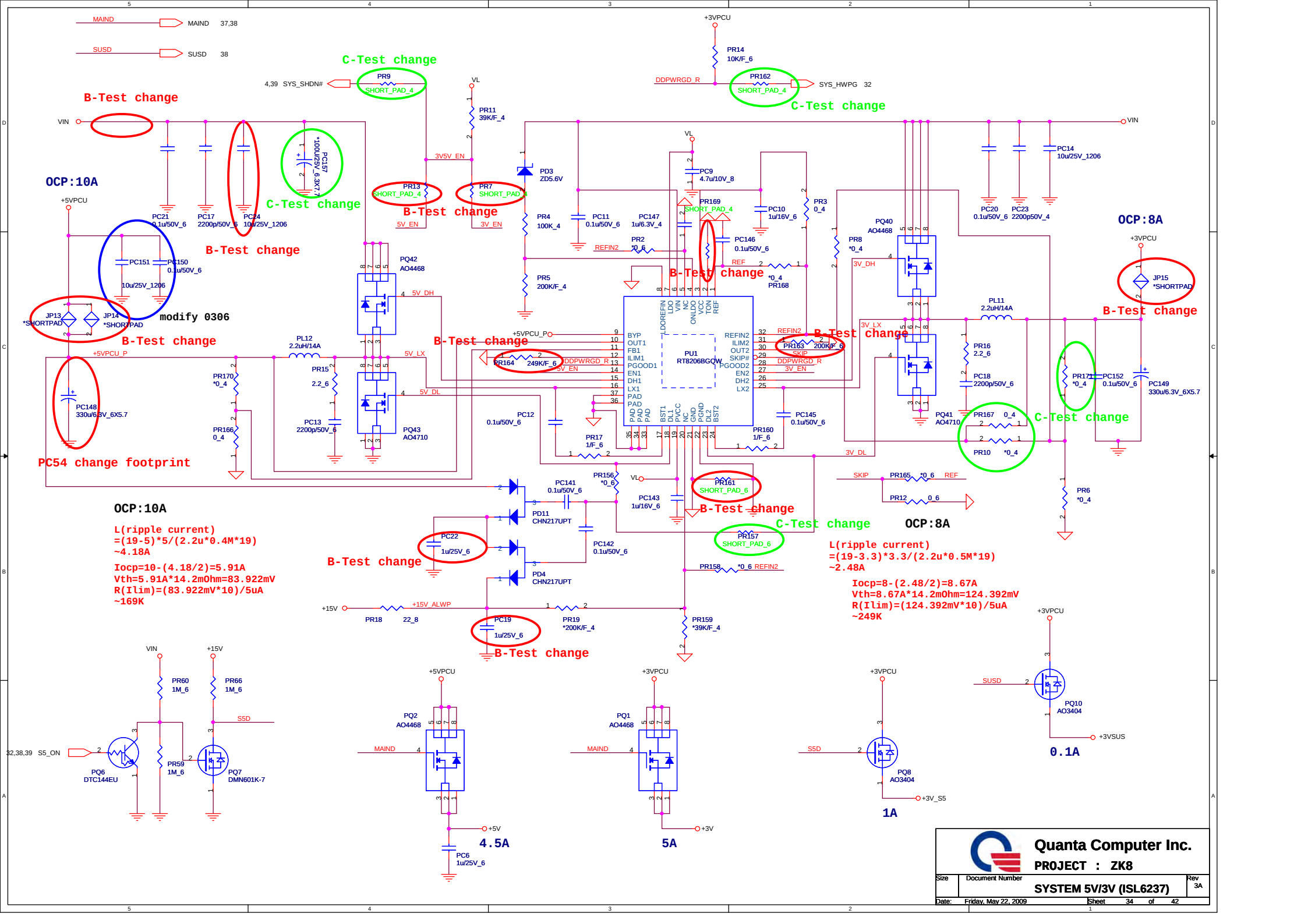
MAIND
MAIND 37,38
SUSD
SUSD 38
4,39 SYS_SHDN#
C-Test change
PR9
SHORT_PAD_4
B-Test change
VIN
OCP:10A
+5VPCU
PC21
0.1u/50V_6
PC17
2200p/50V_6
PC24
10u/25V_1206
PC157
100u/25V_6.3X7.7
C-Test change
PR13
SHORT_PAD_4
B-Test change
PR7
SHORT_PAD
5V_EN
3V_EN
VL
PR11
39K/F_4
3V5V_EN
PD3
ZD5.6V
PR4
100K_4
PC11
0.1u/50V_6
PC147
1u/6.3V_4
REFIN2
PR2
*0_6
PR5
200K/F_4
+3VPCU
PR14
10K/F_6
DDPWRGD_R
PR162
SHORT_PAD_4
SYS_HWPG 32
C-Test change
PC14
10u/25V_1206
PC20
0.1u/50V_6
PC23
2200p50V_4
OCP:8A
PC9
4.7u/10V_8
PR169
SHORT_PAD_4
PC10
1u/16V_6
PR3
0_4
PC146
0.1u/50V_6
REF
PR168
*0_4
B-Test change
PQ40
AO4468
PR8
*0_4
3V_DH
PQ42
AO4468
5V_DH
PC151
PC150
0.1u/50V_6
10u/25V_1206
JP13
*SHORTPAD
JP14
*SHORTPAD
modify 0306
B-Test change
+5VPCU_P
PC148
330u/6.3V_6X5.7
PC54 change footprint
PL12
2.2uH/14A
PR170
*0_4
PR166
0_4
PR15
2.2_6
PC13
2200p/50V_6
PQ43
AO4710
5V_LX
5V_DL
B-Test change
PU1
RT8206BGQW
LDOREFIN
LDO
VIN
NC
ONLDO
VCC
TON
REF
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
BST1
DL1
PVCC
NC
GND
DL2
BST2
PC12
0.1u/50V_6
PR17
1/F_6
PR164
249K/F_6
PR163
200K/F_6
SKIP
PR160
1/F_6
PC145
0.1u/50V_6
PR156
*0_6
PC141
0.1u/50V_6
PD11
CHN217UPT
PC143
1u/16V_6
PR161
SHORT_PAD_6
B-Test change
PC22
1u/25V_6
PC142
0.1u/50V_6
PD4
CHN217UPT
PR158
*0_6 REFIN2
PR157
SHORT_PAD_6
C-Test change
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=8.67A
Vth=8.67A*14.2mOhm=124.392mV
R(Ilim)=(124.392mV*10)/5uA
~249K
+15V
+15V_ALWP
PR18
22_8
PC19
1u/25V_6
PR19
*200K/F_4
PR159
*39K/F_4
B-Test change
OCP:10A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=10-(4.18/2)=5.91A
Vth=5.91A*14.2mOhm=83.922mV
R(Ilim)=(83.922mV*10)/5uA
~169K
PL11
2.2uH/14A
PR16
2.2_6
PC18
2200p/50V_6
PQ41
AO4710
PR167
0_4
PR10
*0_4
C-Test change
PR171
*0_4
PC152
0.1u/50V_6
PC149
330u/6.3V_6X5.7
JP15
*SHORTPAD
B-Test change
PR6
*0_4
SKIP
PR165
*0_6
REF
PR12
0_6
3V_DL
3V_LX
PR164
249K/F_6
DDPWRGD_R
5V_EN
PR60
1M_6
PR66
1M_6
S5D
32,38,39 S5_ON
PR59
1M_6
PQ6
DTC144EU
PQ7
DMN601K-7
PQ2
AO4468
MAIND
+5V
4.5A
PC6
1u/25V_6
PQ1
AO4468
MAIND
+3V
5A
PQ8
AO3404
+3V_S5
1A
PQ10
AO3404
SUSD
+3VSUS
0.1A
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PROJECT : ZK8
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SYSTEM 5V/3V (ISL6237)
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OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

3A

20A

20A

B-Test change

B-Test Modify

C-Test change

C-Test Modify

Change symber

Pin 49 is GND Pin

Delete PR89 and PR90

Delete PR104 and PR105

Close to CPU socket

Parallel

Add for Tigris

Chage PR113 value from 10 to 10K

Change from CPU_CORE1 to CPU_CORE0 for Tigris

Remove for Tigris only

Quanta Computer Inc.
PROJECT : ZK8
AMD CPU Core(ISL6265)
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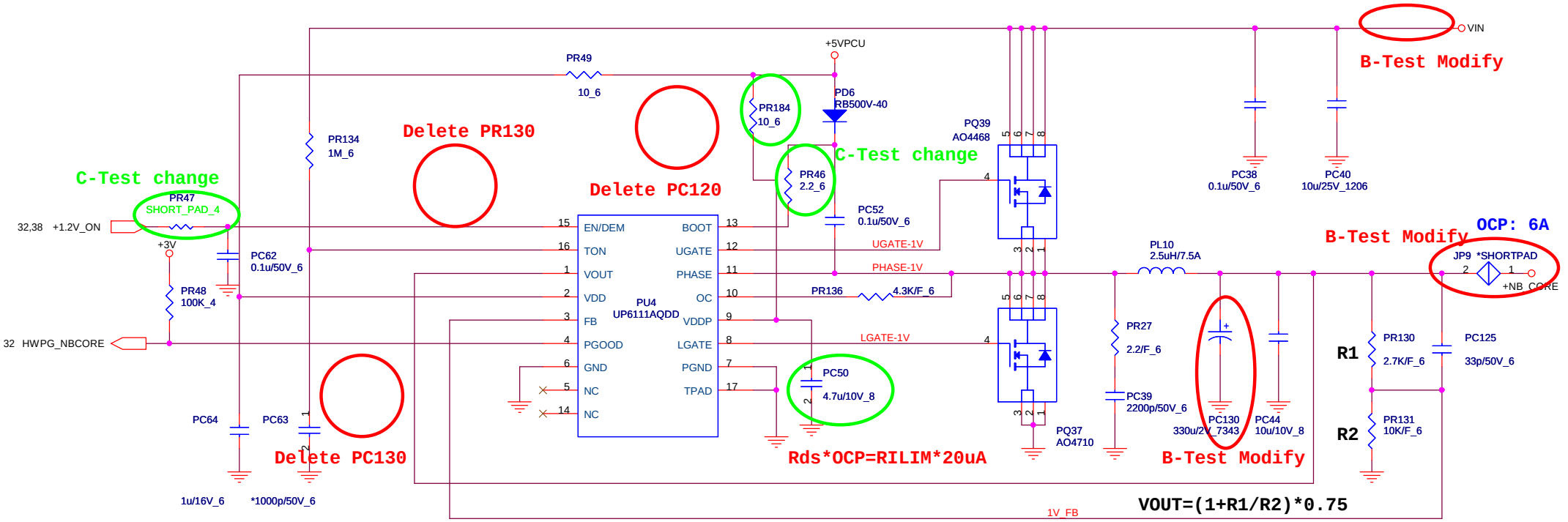
Date: Friday, May 22, 2009 Sheet 35 of 42

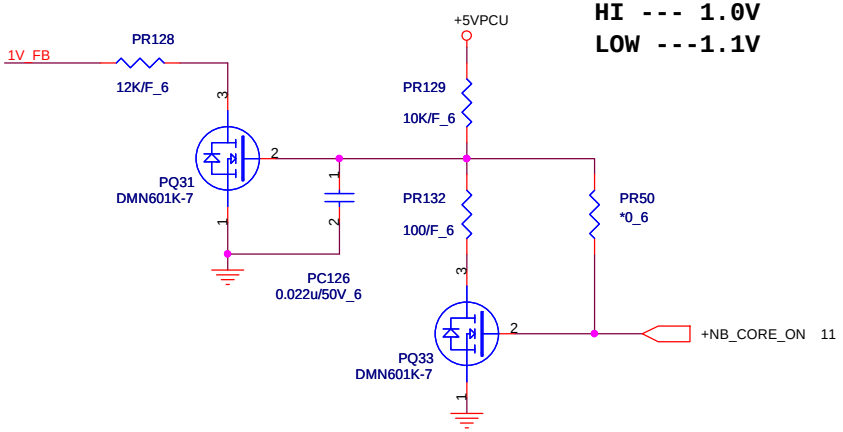


TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K



HI --- 1.0V
LOW ---1.1V

AO4710 Rdson=14.2mOhm
OCP=7.2-0.8A
L(ripple current)
=(19-1.05)*1.05/(2.2u*272k*19)
~1.63A

14.2m*6=RILIM*20uA
RILIM=4.3K

Quanta Computer Inc.		
PROJECT : ZK8		
Size	Document Number: +NB_CORE(UP6111AQDD)	Rev: 3A
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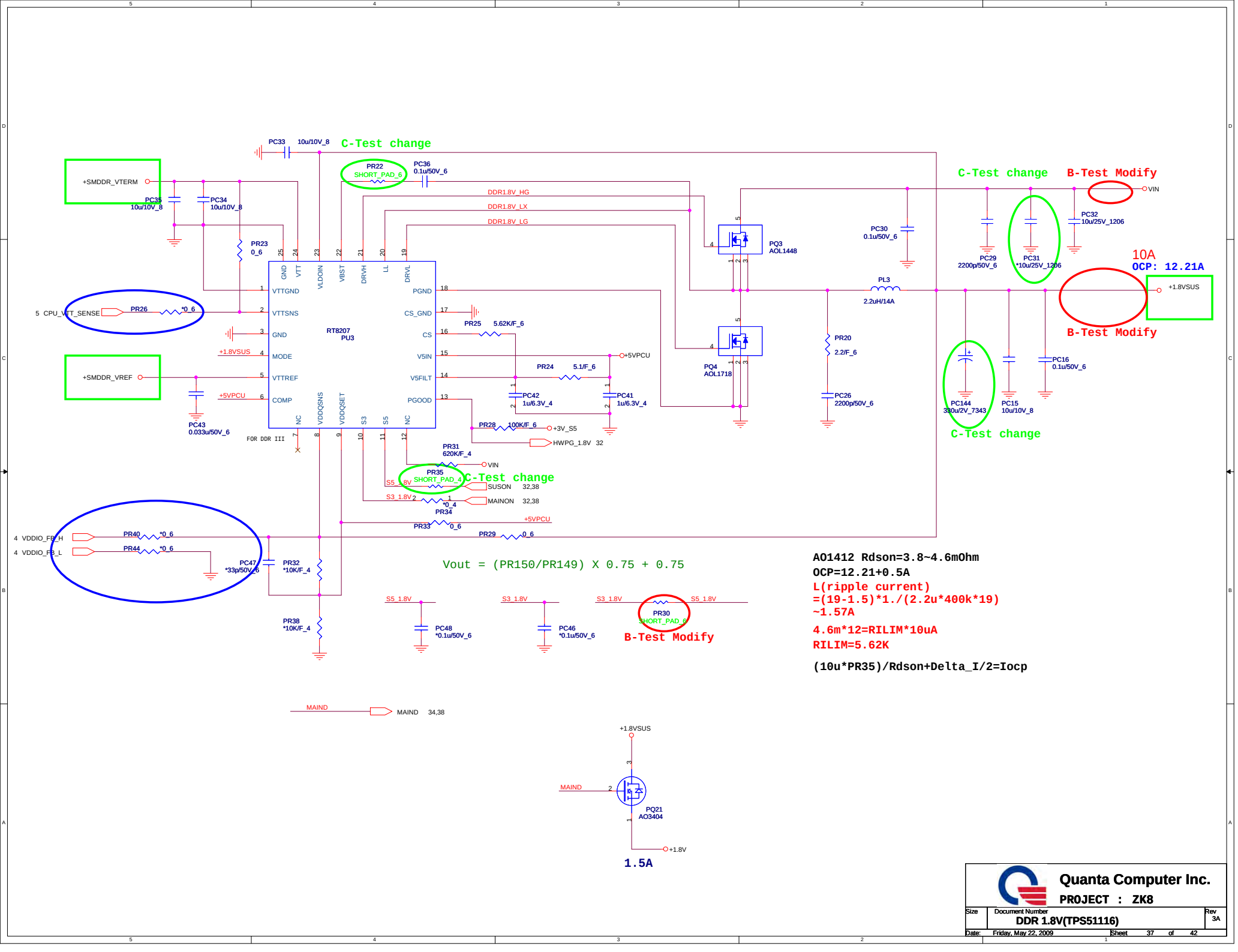
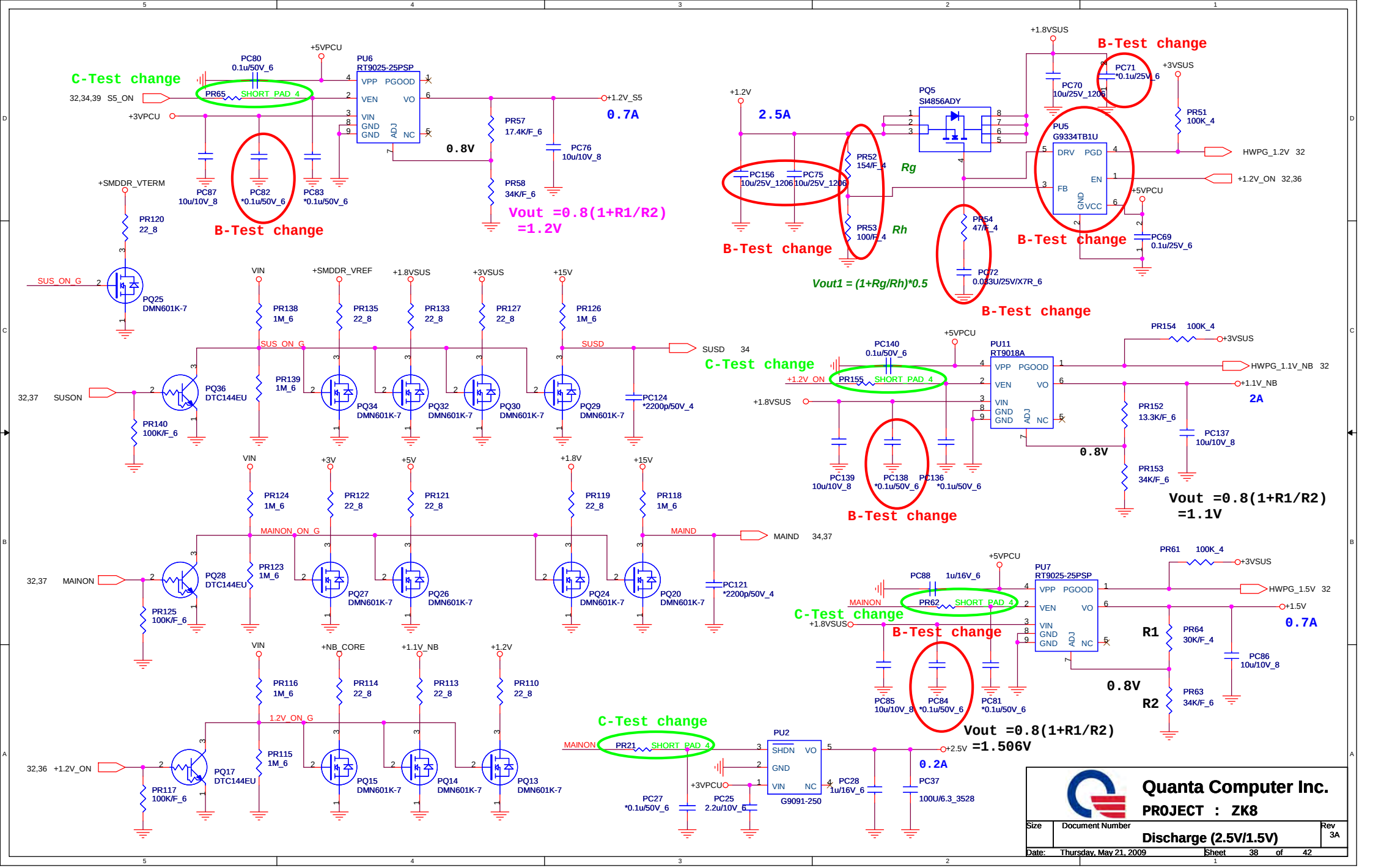


Quanta Computer Inc.			
PROJECT : ZK8			
Size	Document Number: DDR 1.8V(TPS51116)		Rev 3A
Date: Friday, May 22, 2009		Sheet 37 of 42	


C-Test change
B-Test change
0.7A
0.8V
Vout =0.8(1+R1/R2)
=1.2V
2.5A
Rg
Rh
Vout1 = (1+Rg/Rh)*0.5
2A
Vout =0.8(1+R1/R2)
=1.1V
0.2A
Vout =0.8(1+R1/R2)
=1.506V
R1
R2
Quanta Computer Inc.
PROJECT : ZK8
Discharge (2.5V/1.5V)
Size
Document Number
Rev
3A
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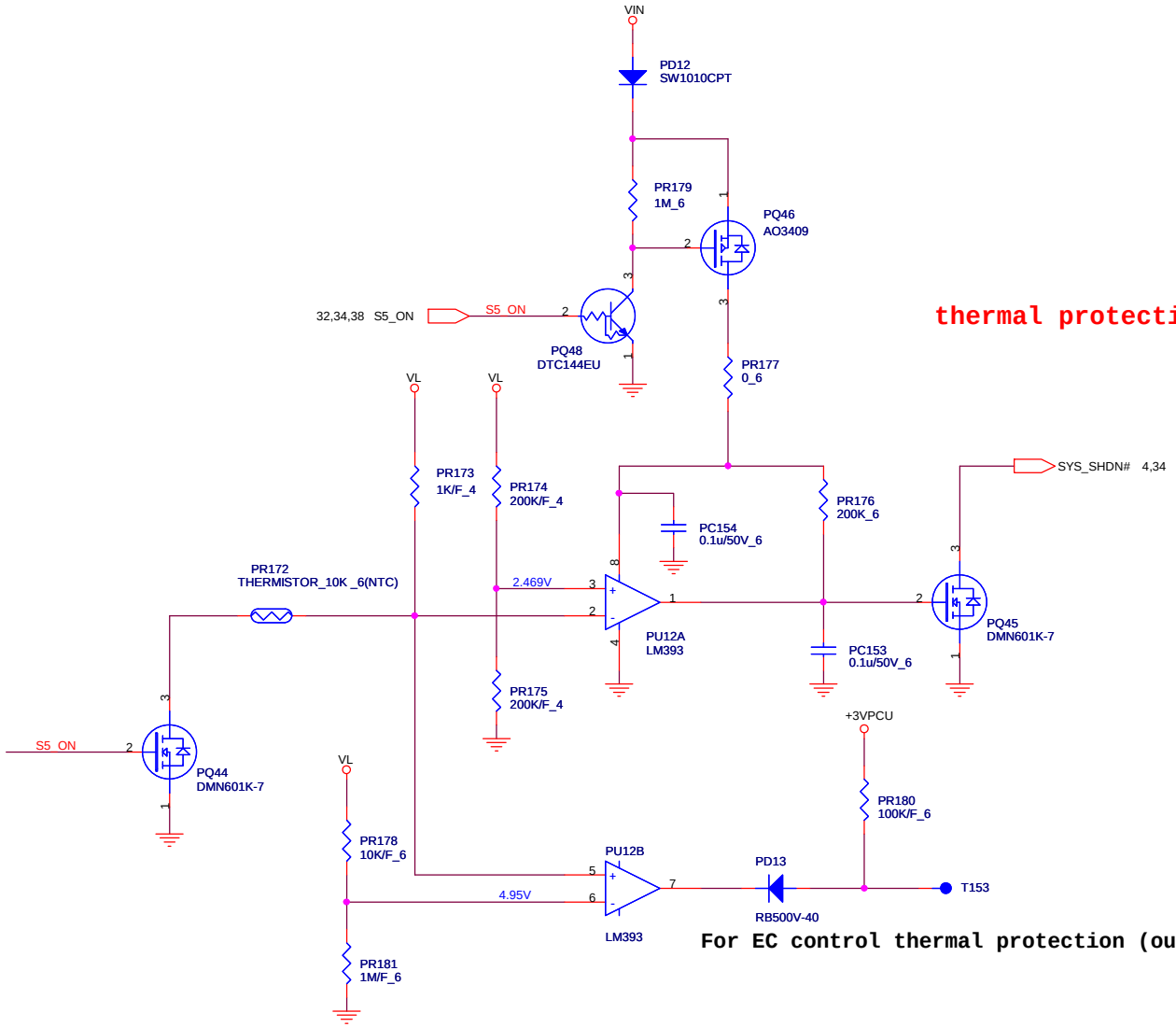

Quanta Computer Inc.		
PROJECT : ZK8		
Size	Document Number: Thermal protect	Rev: 3A
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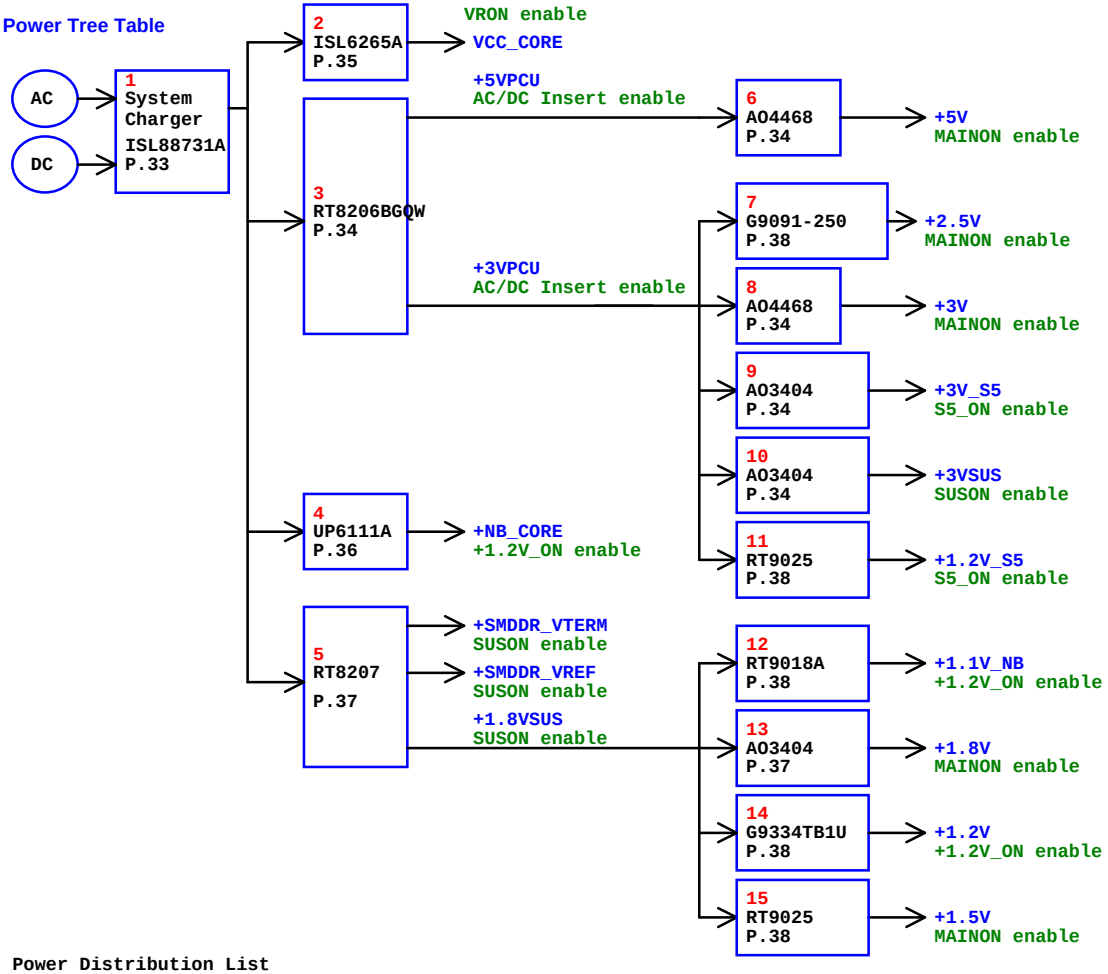
Power Tree Table



Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	RTC charge,USB,+5V
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash
+1.8V	RS880, SB710, LVDS switch
+SMDDR_VTERM	CPU, DDR
+SMDDR_VREF	CPU, DDR
+1.8VSUS	CPU, DDR
+NB_CORE	RS880
+1.2V_S5	SB710
+5V	SB710,MXM,CRT,HDMI,TV CARD,HDD,ODD,AUDIO,FAN,TP
+3V	CLK, CPU Thermal Monitor, FAN, RS880, DDR, SB710, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, MXM,ESATA Mini Card, KB, TP/FP/LED /B, RJ45/USB /B, Bluetooth, MMB, New Card, PC BEEP, EC, Codec (ALC889), VR, Headphone
+3V_S5	SB710, LAN, RJ45, MDC
+3VSUS	BT
+1.1V_NB	RS880
+2.5V	CPU
+1.2V	CPU,CLK,RS880,SB710
+1.5V	Mini Card,

Quanta Computer Inc.
PROJECT : ZK8
Size | Document Number: Power Tree Table | Rev 3A
Date: Monday, May 04, 2009 | Sheet 40 of 42

CHANGE LIST

Model	REV	CHANGE LIST	MODEL	ZK8 FROM	ZK8 To
ZK8 MB	1A	FIRST RELEASED: (PCB:A)		X	1A
	2A	20090317 page32 Add R530 for CPU_COREPG pull high.		1A	2A
		20090317 page08 Add MEMHOT circuit.		1A	2A
		20090330 page32 change SW1 footprint to SW-TC901-AA1G-A160T-6P.		1A	2A
		20090330 page38 change PU5 to G9334TB1U,PR52 to 140 Ohm ,PR53 to 100 Ohm.		1A	2A
		20090330 page17 modify NB/SB POWER GOOD circuit.		1A	2A
		20090401 page32 delete R316 ,add D41.		1A	2A
		20090402 modify AMP and SUBWOOFER MUTE circuit.		1A	2A
		20090407 page17 delete C390.		1A	2A
		20090408 page30 add C213, C214,C390,C683,C684,C685,C686,C687,C688,C689 for EMI.		1A	2A
		20090408 change PL3,PL9,PL11,PL12 footprint to CHOKE-ETQP4LR36WFC-NB4.		1A	2A
		20090408 page23 add L67 ,C690,change C62 to 1uF,C63,C64,C65 to 0.01uF for EMI.		1A	2A
		20090409 page29 add C691,C692 for EMI.		1A	2A
		20090409 page19 change R168 to 120 Ohm bead (CX12T121005).		1A	2A
				1A	2A
		20090411 page22 delete R79 for layout request.		1A	2A
		20090411 page30 delete C214 for layout request.		1A	2A
		20090415 page11 change Q45 from ZN7002 to BSS138.		1A	2A
		20090415 page27 change R524,R523 to 18K Ohm.		1A	2A
				1A	2A
		20090423 page29 R169 , R153 change from 330 Ohm to 1k Ohm（CS21002JB34）.		1A	2A
		20090423 page29 R197 change from 330 Ohm to 100 Ohm(CS11002JB32).		1A	2A
		20090423 page36 PR130 changes from CS23653F912 to CS22703F911,PR128 changes from CS33573F910 to CS31203F911.		1A	2A
		20090423 page38 PQ5 changes from BAM44680003 to BAM48560011,PR52 changes from CS11402FB19 to CS11542FB00.		1A	2A
	3A	20090428 page18 modify MXMPWR_EN circuit.		2A	3A
		20090428 page20 change CRT connector PN to DFDS15FR111.		2A	3A
		20090504 page32 delete SW1,add D42.		2A	3A
		20090504 page22 delete R38,R48.		2A	3A
		20090505 page19 add R79.		2A	3A
		20090507 page27 change Q53,Q57 PN to BAM601K0003.		2A	3A
		20090512 page03 delete PR2,PR3,PR4,PR5,PR6,PR7,PR8,PR9.		2A	3A
		20090512 page04 change R404,R407 to short pad.		2A	3A
		20090512 page10 delete C97,C98,C99,C100,C106,C107,C108,C109.		2A	3A
		20090512 page11 Move HDTV_DET from pin B7 to B8,Move HDMI EDID pair from EDID0 (pin B8 & A8) to EDID1 (pin B7 & A7),change R456 to short pad		2A	3A
		20090512 page12 change R95,R97,R99,R443 to short pad.		2A	3A
		20090512 page13 change R269 to short pad,delete R266.		2A	3A
		20090512 page14 delete R278.		2A	3A
		20090512 page15 change R384 to short pad.		2A	3A
		20090512 page16 change R300,R198,R199,R377,R201 to short pad ,change C437 to 10 uF,add C214,unstuff C469,C472,C347.		2A	3A
		20090512 page18 add R539,unstuff R53,D6,change C623 to o.1 uF.		2A	3A
		20090512 page19 delete R84,R89.add R79,change R44,R50 to short pad.		2A	3A
		20090512 page20 change R499,R505 to short pad.		2A	3A
		20090512 page21 delete R527.		2A	3A
		20090512 page22 delete R38,R48,R86,change R470 to short pad.		2A	3A
		20090512 page23 unstuff R34,R35,U4,C38 ,delete R221,R228.		2A	3A
		20090512 page24 change R326,R327,R332,R333,R334,R335,R336,R321,R323,R329,R338,R343 to short pad.		2A	3A
		20090512 page25 delete R265,R317.		2A	3A
		20090512 page27 change Q53,Q57 to DMN601K-7.		2A	3A
		20090512 page29 change R299 to short pad.		2A	3A
		20090512 page32 add D42,D43,D44,R527,change C481 to 4.7u/6.3V_6,delete R345.		2A	3A
		20090514 page24 change CN14 PN to DFHS52FR005.		2A	3A
		20090514 page33 change CN16 footfrint to bat-200045mr007g122-7p-l-v-nb4.		2A	3A
		20090518 page27 modify CN4 LC circuit for EMI request.		2A	3A
		20090519 change D2 ,D38 PN form BC0SSM14Z21 to BC005819Z40.		2A	3A
		20090529 page29 add R221,R228.		2A	3A
		20090529 page27 modify AMP and SUBWOOFER MUTE circuit.		2A	3A

Quanta Computer Inc. PROJECT : ZK8	DOC NO.	PROJECT MODEL :	ZK8	APPROVED BY:	
		DATE:	2009/04/07		
		PART NUMBER:		DRAWING BY:	
		REVISON:	3A		

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CHANGE LIST OF POWER

Model	REV		MODEL	ZK8
				FROM / To

ZK8 MB

1A

FIRST RELEASED: (PCB:A)

2A

Page33: PC3, PC4 change from CH41006K911 to *CH41006K911
Page33: PD10 changes from BC1N4148Z00 to BC001010Z17
Page33: PU10 changes from AL088731000 to AL088731001
Page33: PR43 changes from CS00002JB38 to SHORT0402
Page33: PD7, PD8 change from *BDDZS36BZ00 to *BDDZS56BZ09
Page34: PC24 change from *CH61004M291 to CH61004M291
Page34: PR7, PR13, PR169 change from CS00002JB38 to SHORT0402
Page34: PR164 changes from CS42003F919 to CS42493F914
Page34: PC19, PC22 change from CH41006K911 to CH5104K9906
Page34: PR161 changes from CS00003J951 to SHORT0603
Page34: PR163 changes from CS42493F914 to CS42003F919
Page35: PC66, PC68, PC123 change from CH733RM8802 to CH733RY8802
Page35: PC65, PC67 change from *CH733RM8802 to *CH733RY8802
Page35: PR75 changes from CS00004JA40 to SHORT0805
Page36: PC130 changes from CH733RM8802 to CH733RY8802
Page37: PR30 changes from CS00003J951 to SHORT0603
Page38: PC82, PC84, PC138 change from CH41006K911 to *CH41006K911
Page38: PC71 changes from CH41004K910 to *CH41004K910
Page38: PU5 changes from AL009338014 to AL009334000
Page38: PR54 changes from CS00003J951 to CS04702FB16
Page38: PC72 changes from CH31006K919 to CH33304K914
Page38: PR52 changes from CS32262FB15 to CS11402FB19
Page38: PR53 changes from CS31603F916 to CS11002FB22
Page35: PU9 changes from AL006265001 to AL006265002
Page33: PC135 changes from CH41006KE11 to CH41006K911
Page33: PU8 changes from AL001293000 to *AL001293000
Page38: PC75 changes from CH6222M9200 to CH61004M291
Page38: Add PC156 (10u/25V_1206, CH61004M291)

3A

Page33: PD7、PD8 change from *BDDZS56BZ09 to BDDZS56BZ09
Page34: PR9、PR162 change from CS00002JB38 to SHORT0402
Page34: PR157 changes from CS00003J951 to SHORT0603
Page34: Add PC157 (CC71004MZ81)
Page34: PR167 changes from *CS00002JB38 to CS00002JB38
Page34: PR10、PR171 change from CS00002JB38 to *CS00002JB38
Page35: PR70、PR107 change from CS23922FB13 to CS31822FB16
Page35: PR71、PR106 change from CS31822FB16 to CS23922FB13
Page35: PC113、PC114、PC115、PC116、PC117 change from CH61004M291 to *CH61004M291
Page35: PC119、PC120 change from *CC62704MZ00 to CC71004MZ81
Page35: PR70、PR107 change from CS23922FB13 to CS31822FB16
Page35: PR71、PR106 change from CS31822FB16 to CS23922FB13
Page35: PR79、PR97、PR99、PR101 change from CS00002JB38 to SHORT0402
Page35: PC65、PC67 change from *CH733RY8802 to CH733RY8802
Page35: PR74 changes from CS41072FB11 to CS32552FB11
Page35: PR76 change from CS31002FB26 to CS39102FB05
Page36: PR46 changes from CS00003J951 to CS-2203J913
Page36: Add PR184 (CS01003J953)
Page37: PC31 changes from CH61004M291 to *CH61004M291
Page37: PR22 changes from CS00003J951 to SHORT0603
Page37: PR35 changes from CS00002JB38 to SHORT0402
Page38: PR21、PR62、PR65、PR155 change from CS00002JB38 to SHORT0402
Page37: PC144 changes from CC7560JMZ15 to CH733RY8802

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FROM	To
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