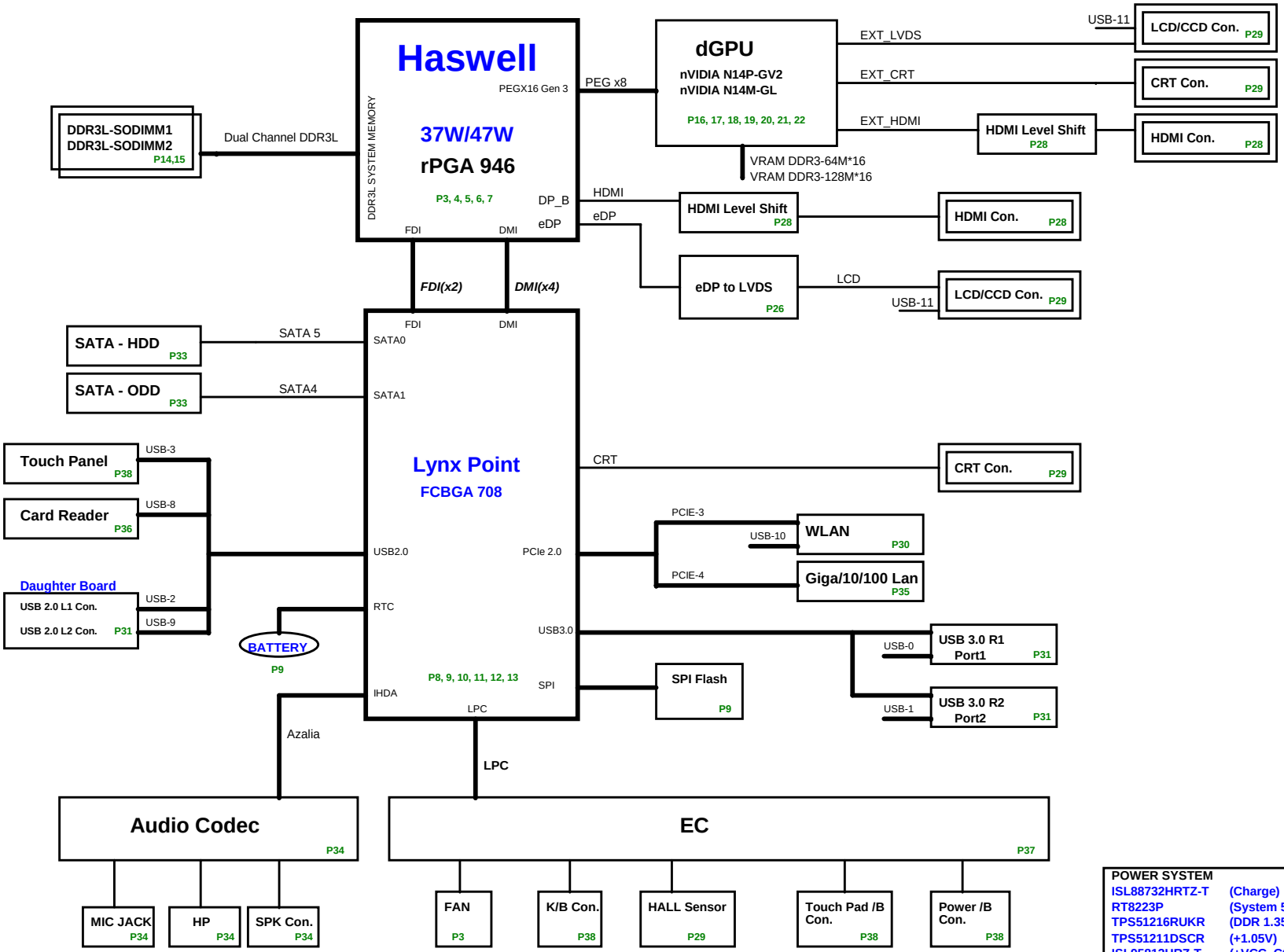
BD6 Shark Bay Block Diagram



POWER SYSTEM

ISL88732HRTZ-T	(Charge)	P40
RT8223P	(System 5V/3V)	P41
TPS51216RUKR	(DDR 1.35V)	P42
TPS51211DSCR	(+1.05V)	P43
ISL95812HRZ-T	(+VCC_CORE)	P44
RT8812A	(NV_VGPU_CORE)	P46
	(other GPU)	P47

Quanta Computer Inc.

PROJECT : BD6

Size	Document Number	Rev
	Block Diagram	1A

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25	PCH XDP	CLG
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28	HDMI comm part	HDM
29	VGA Connector	VGA
	LCD Panel	LDS
	CRT & CRT BUS SWITCH	CRT
	CCD	CCD
	HALL SENSOR&BACK LIGHT SWITCH	HSR
30	MINI Card (Wi-Fi & WIMAX)	MNW
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	USB Sleep Charger	SLC
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	ODD	ODD
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37	EC	KBC
38	KeyBoard	KBC
	TP&FP board	TPD,FPD
	Power SW	PSW
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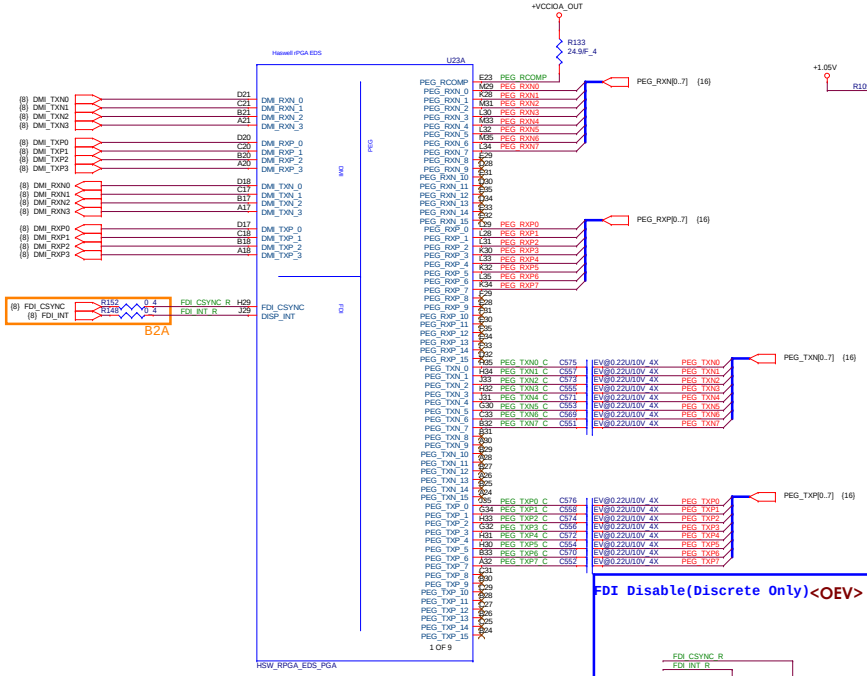
41	System 5V/3V	PWM
42	DDR 1.35V	PWM
43	+1.05V	PWM
45	+VCORE	PWM
46	Discharge	PWM
47	GPU_CORE	PWM
48	other GPU	PWM

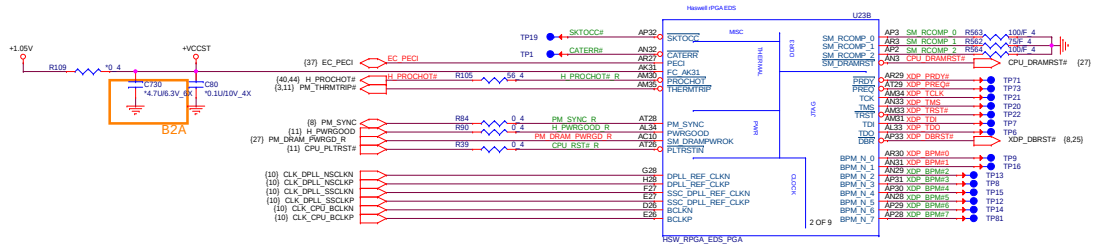
POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
+VIN	10V~+19V		S0~S5
+3V_RTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3VPCU	+3.3V	AC/DC Insert enable	S0~S5
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
+1.35VSUS	+1.5V	S5_ON	S0~S3
+1.5V	+1.5V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VCORE	~	MPWROK	S0
+3V_GPU	+3.3V	DGPU_PWR_EN_R	S0
+VGPU_CORE	~	DGPU_PWR_EN_RC	S0
+1.5V_GPU	+1.5V	GPU_PWR_GD	S0
+1.05V_GPU	+1.05V	GPU_PWR_GD	S0

GND PLANE	PAGE
GND_SIGNAL	32
8769GND	37
GND	ALL
ADOGND	34

Haswell Processor (DMI,PEG,FDI) <CPU/VGA>

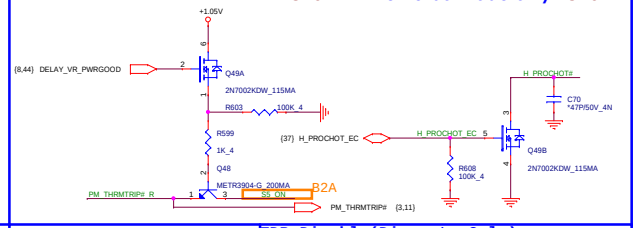


Haswell Processor (CLK,MISC,JTAG) <CPU>

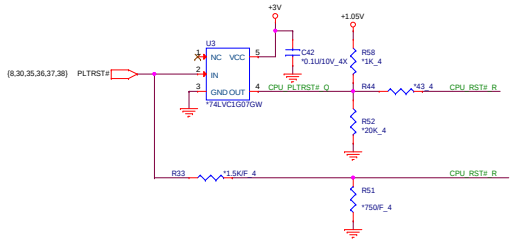


Thermal Trip & Process HOT <CPU>

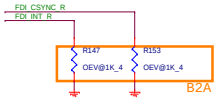
Intel Turbo mode only <CPU>



Reserved For buffer reset of PLTRSRIN# <CPU>

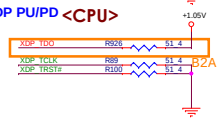


FDI Disable(Discrete Only) <OEV>

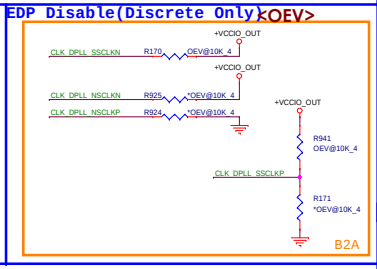


PU/PD of CPU <CPU>

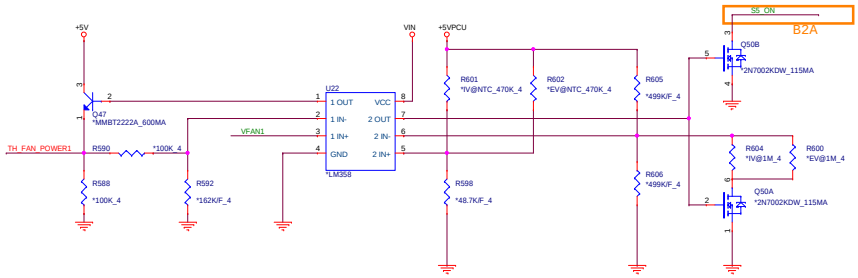
XDP PU/PD <CPU>



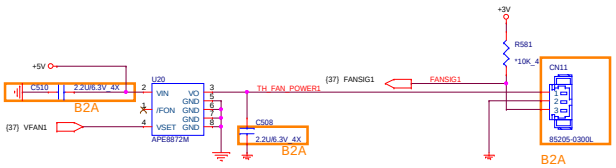
EDP Disable(Discrete Only) <OEV>



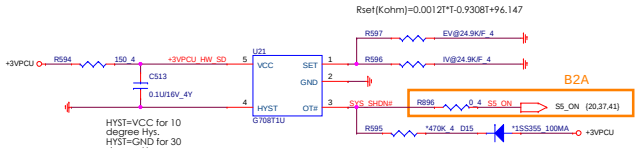
<THC>



FAN Control-->For one FAN solution <THC>



CPU Thermal sensor / MB Local TEMP <THP/UGA/VGA>



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PROJECT : BD6

Size	Document Number	Rev
	Haswell 1/5 (PEG/DMI/FDI)	1A

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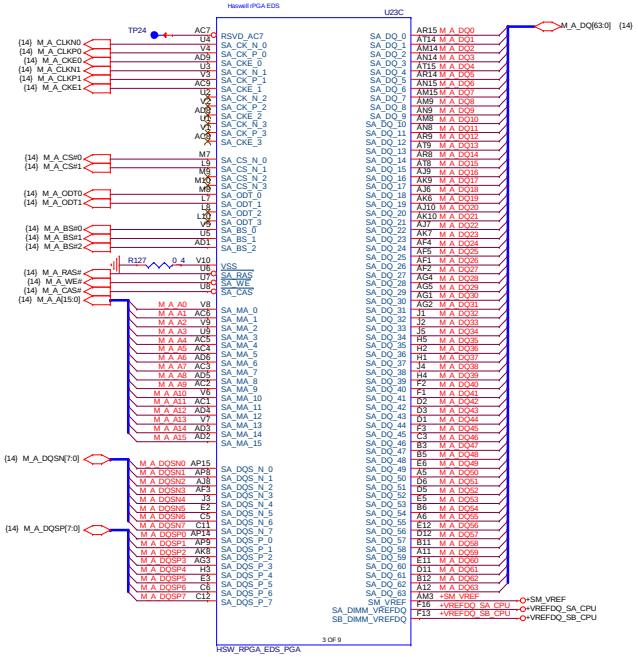
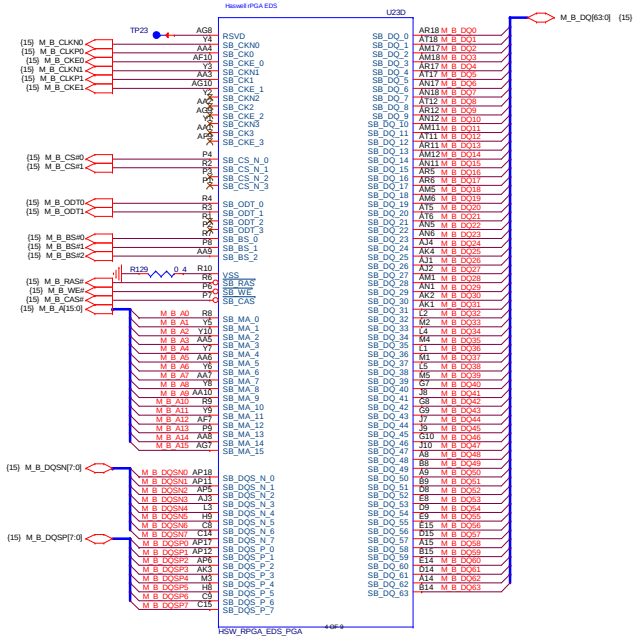
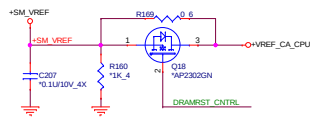
Haswell Processor (DDR3) <CPU>



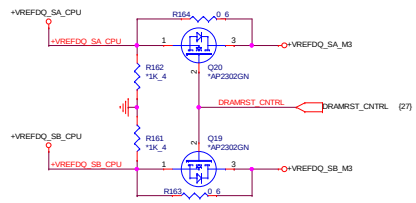
Haswell Processor (DDR3) <CPU>



CPU SM_VREF M3 <CPU>



CPU VREFDQ M3 <CPU>



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Size	Document Number	Rev
	Haswell 2/5 (DDR3 I/F)	1A

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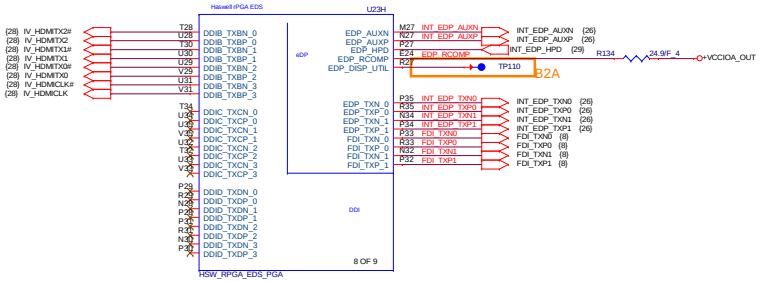
Haswell Processor (DDI,eDP,FDI) <CPU>



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PROJECT : BD6

Size	Document Number	Rev
	Haswell 3/5 (DDI/eDP)	1A

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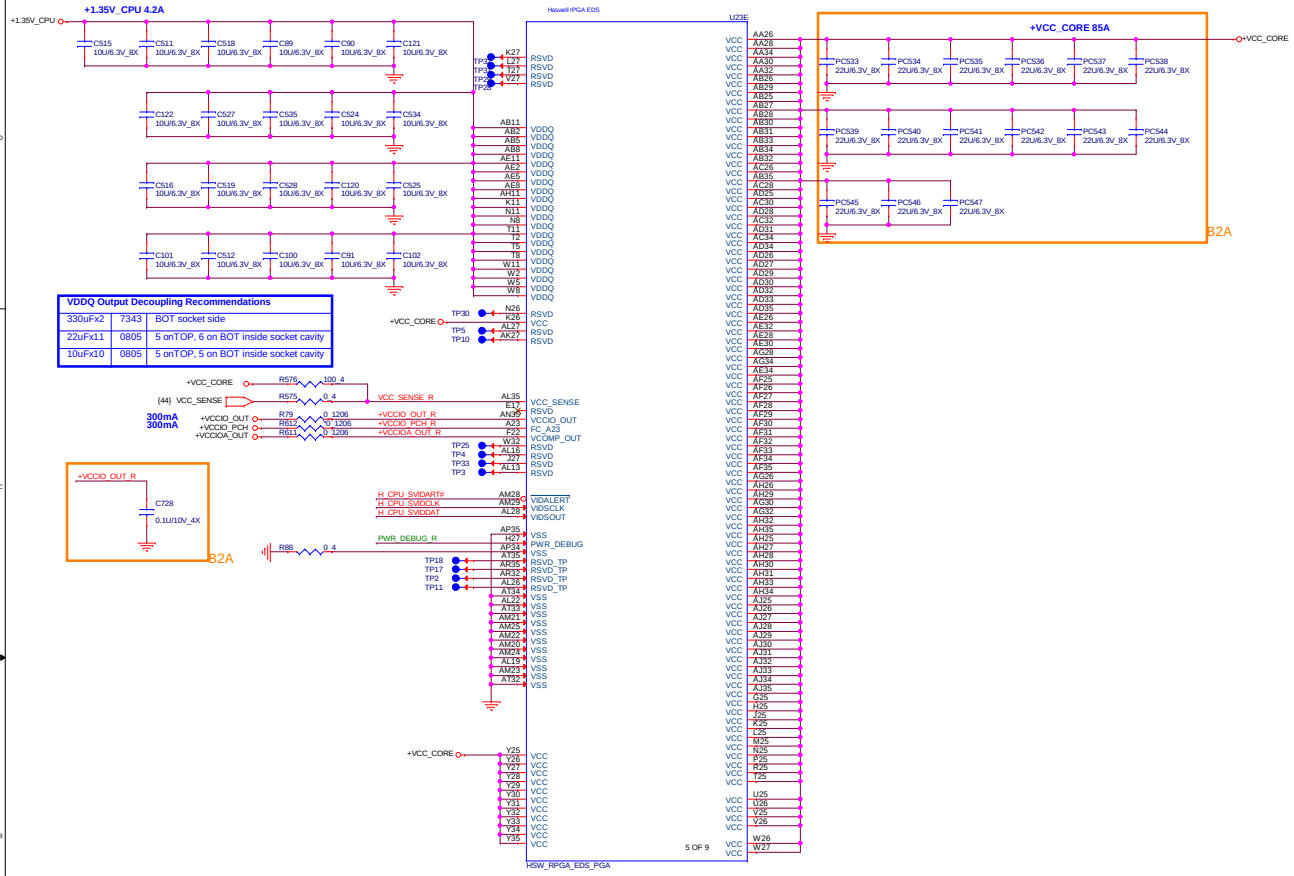
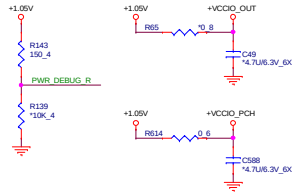
Haswell Processor (POWER) <CPU>

06

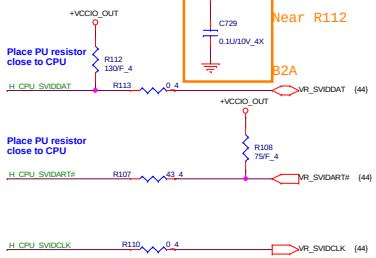


VDDQ Output Decoupling Recommendations		
330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

Power Test Propose <CPU>



SVID <CPU>



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PROJECT : BD6

Size	Document Number	Rev
	Haswell 4/5 (POWER)	1A

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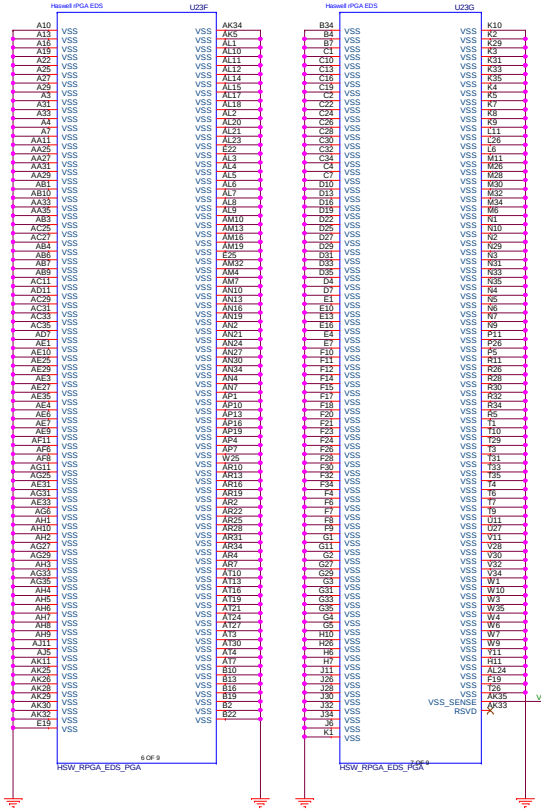
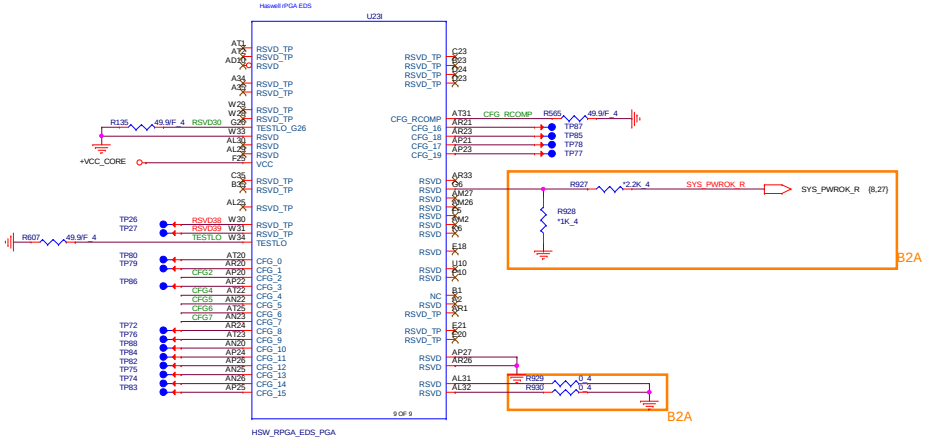
Haswell Processor (GND)<CPU>



Haswell Processor (CFG,RSVD)<CPU>



Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	CFG2 R82 *EV@1K_4 B2A
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	CFG4 R567 PIV@1K_4
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	CFG6 R566 *EV@1K_4 CFG5 R81 EV@1K_4 B2A
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asseted x0 = PEG wait for BIOS fro training	CFG7 R83 *1K_4

Quanta Computer Inc.
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	Haswell 5/5 (CFG/GND)	1A

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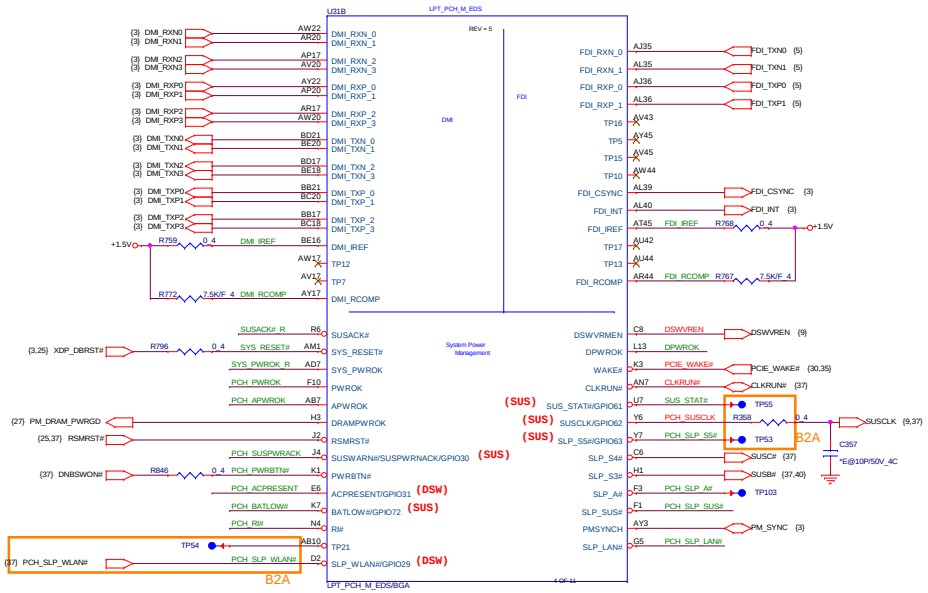
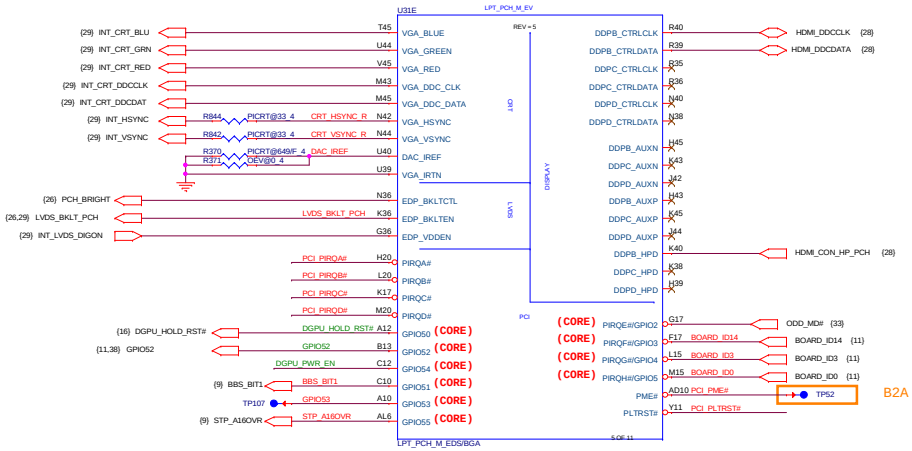
Lynx Point (DMI,FDI,PM)<CLG>

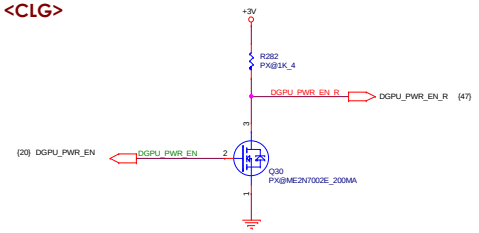


Lynx Point (CRT,PCI,DDI CNTL)<CLG>

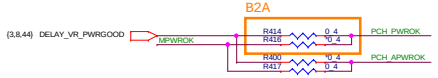


GPIO53 can not PD

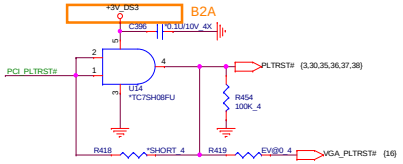
<CLG>



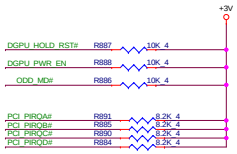
PCH PWROK&APWROK <CLG>



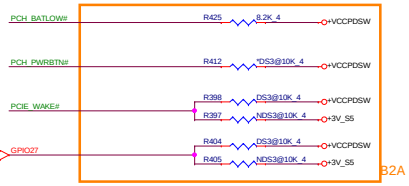
PLTRST# Buffer <CLG>



PCI PU <CLG>

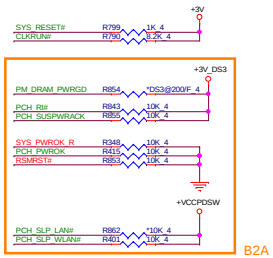


PCH WAKE EVENT <CLG>

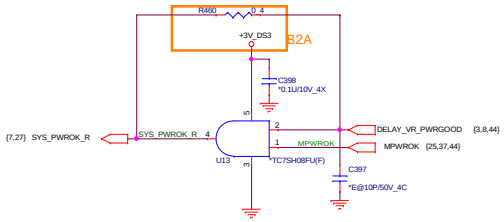


CRT IMPEDANCE MATCHING <CLG>

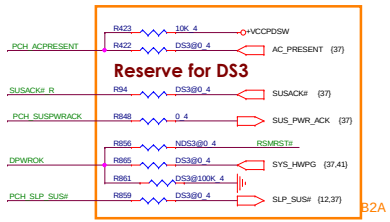
PCH PM PU/PD <CLG>



SYSPWOK <CLG>



DSW Circuit <CLG>



Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	V	NA
SUS_PWR_ACK	V	NA
SUSACK#_R	V	V
DPWROK	V	NA
SLP_SUS	V	NA

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	LPT 1/6 (DMI/FDI/VGA)	1A

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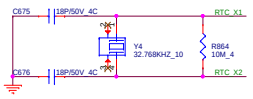
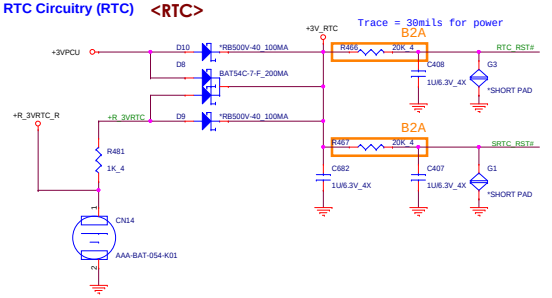
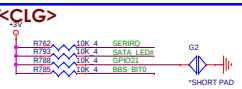
RTC Clock 32.768KHz (RTC) <CLG>



RTC Circuitry (RTC) <RTC>

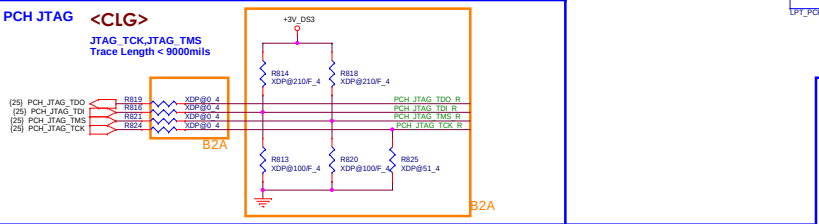


PU & Password Clear <CLG>

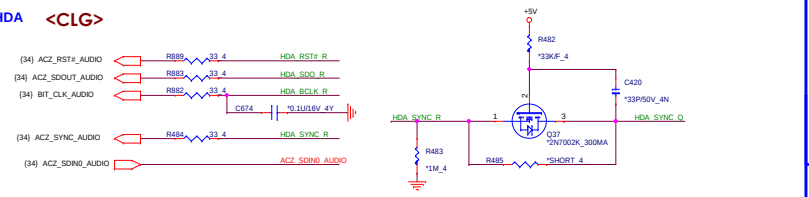


PCH JTAG <CLG>

JTAG_TCK,JTAG_TMS
Trace Length < 9000mils

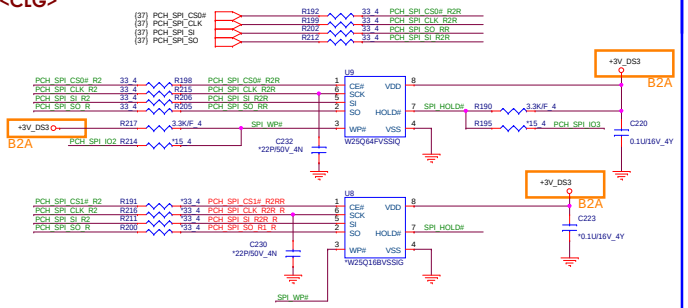


HDA <CLG>



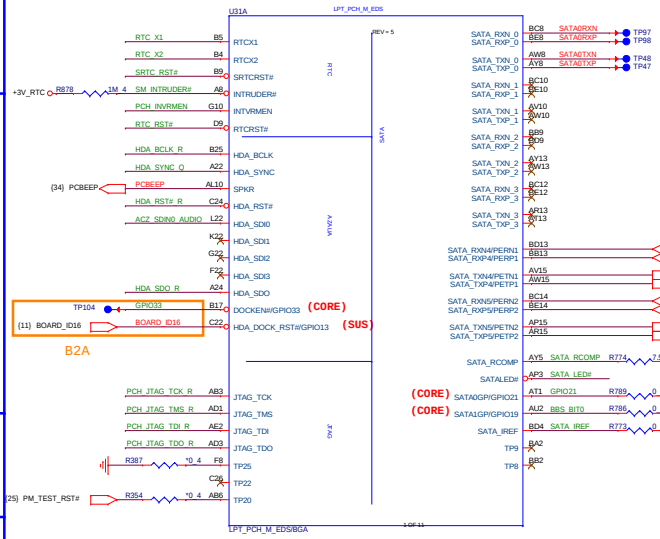
PCH Dual SPI <CLG>

EC+BIOS @4M

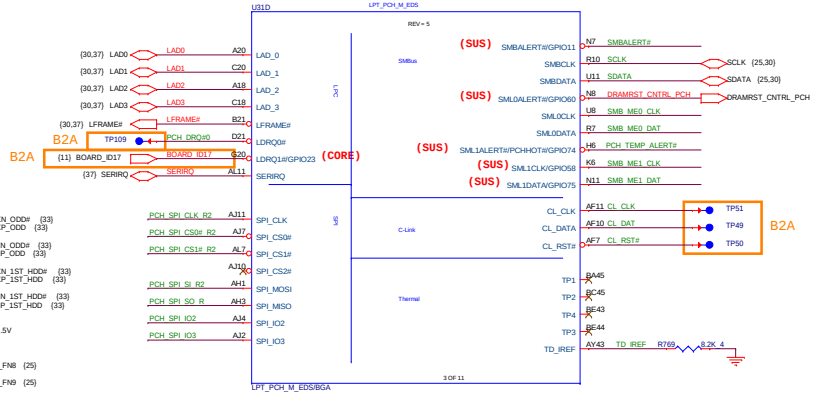


ME@2M

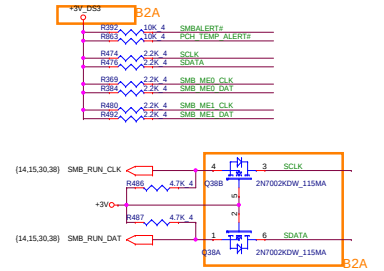
Lynx Point (RTC,IHDA,SATA,JTAG) <CLG>



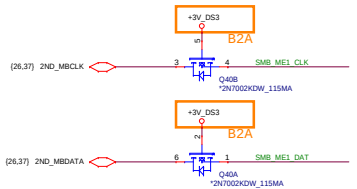
Lynx Point (LPC,SPI,SMBUS,C-LINK,THERMAL) <CLG>



SMBus <CLG>



EC 2nd_SMB read SML1 Bus of PCH temps



PCH STRAPING

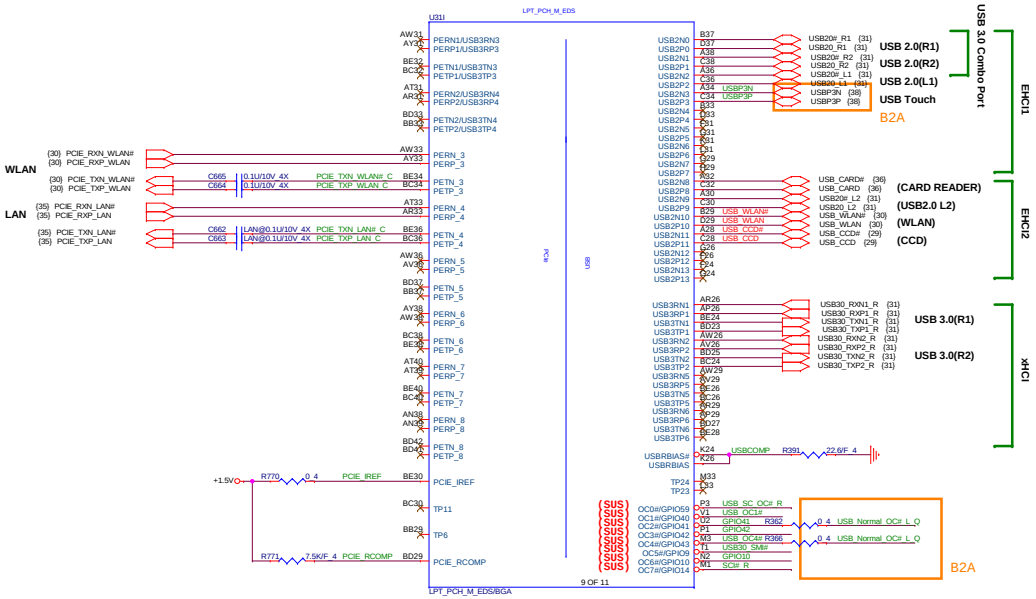
Pin Name	Usage	Sampled	Configuration	Circuitry
SPKR	No Reboot	PWROK	0 = Disable (Int PD) 1 = Enable	PCBEEP R345 *1K_4 +3V
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	(8,37) SUSCLK R357 *1K_4
GPIO55	Top-Block Swap Override	PWROK	0 = Top-Block Swap mode 1 = Default (Int PU)	(8) STP_A16OVR R340 *1K_4
INTVRMEN	Integrated VRM Enable	Always	0 = Disable 1 = Enable	PCH_INVRMEN R403 330K_4 +3V_RTC
GPIO51	Boot BIOS Strap bit 1	PWROK	Bit1 Bit0 1 0 Resvered 1 1 SPI 0 0 LPC	+3V R871 10K_4 (8) BBS_BIT1 R870 *1K_4 BBS_BIT0 R784 *1K_4
SATA1GP/GPIO19	Boot BIOS Strap bit 0	PWROK		
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	(37) ACZ_SDOUT_R HDA_SDO_R R874 *1K_4 +VCC_HDA_IO
GPIO36	RSVD	PWROK	Internal PD	(11) GPIO36 R791 *1K_4 +3V
SATA3GP/GPIO37	TLS Confidentiality	PWROK	0 = TLS no confidentiality (Int PD) 1 = TLS with confidentiality	(11) FDI_OVRVLTG R804 1K_4 +3V
GPIO8	RSVD	RSMRST#	Internal PU	(11) GPIO8 R827 10K_4
GPIO28	PLL on die VR enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	(11) PLL_ODVR_EN R352 *1K_4
DSWVREN	On Die DSW VR Enable	Always	1 = Enable 0 = Disable Must be PU to VCCRTC	(8) DSWVREN R876 330K_4 R877 *330K_4 +3V_RTC

Quanta Computer Inc.
PROJECT : BD6

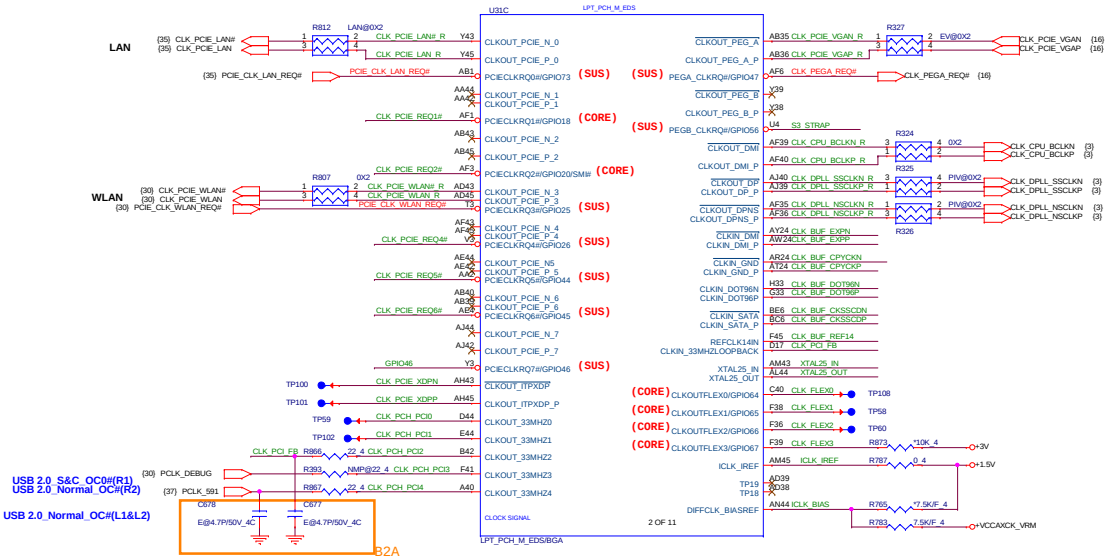
Size	Document Number	Rev
	LPT 2/6 (SATA/HDA/SPI)	1A

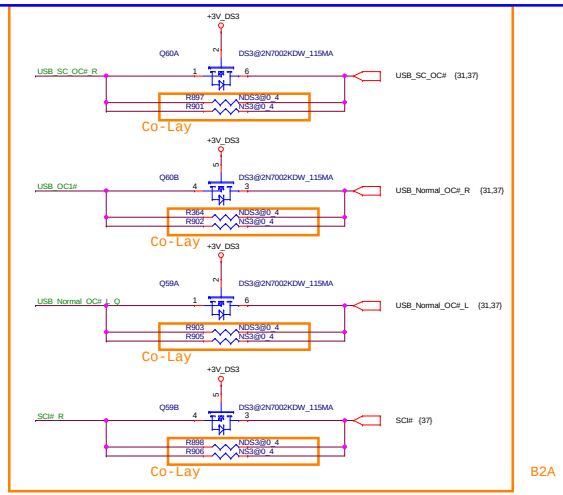
Date: Thursday, December 20, 2012 Sheet 9 of 49

Lynx Point (PCIE,USB3.0,USB2.0) <CLG,U3B,MNW>

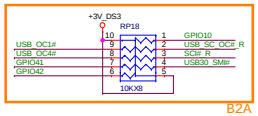


Lynx Point (CLOCK) <CLG>

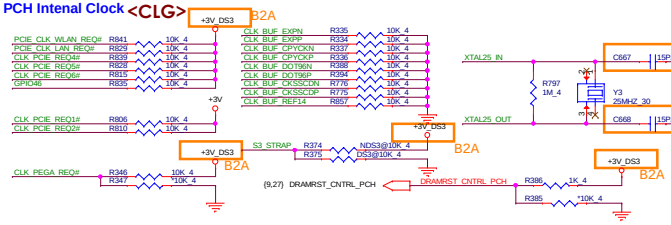




USB Overcurrent <CLG>

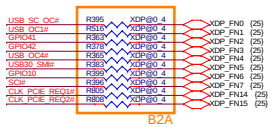


PCH Intenal Clock <CLG>



PCH XDP Signal <CLG>

Routed by 50 ohm



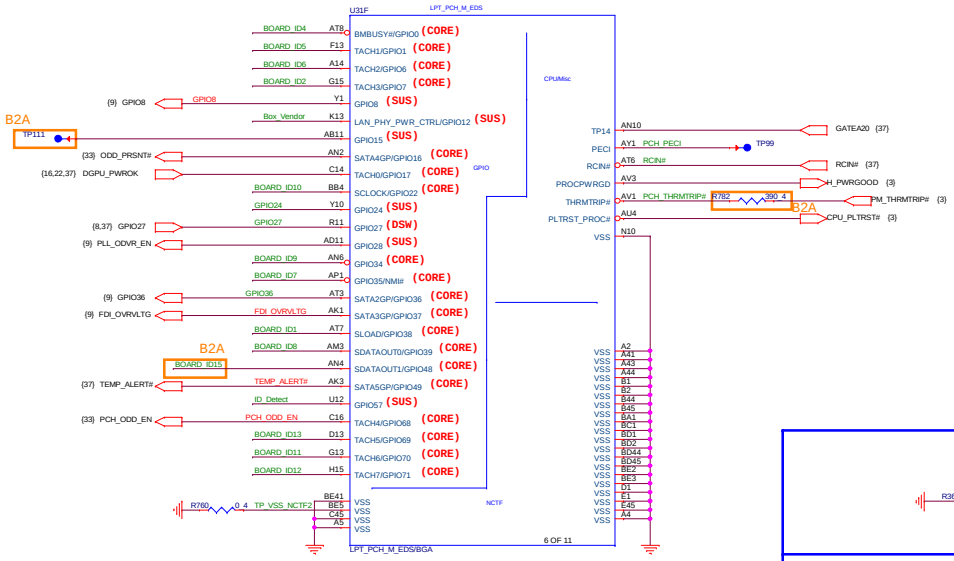
Quanta Computer Inc.

PROJECT : BD6

Size	Document Number	Rev
	LPT 3/6 (PCIE/USB/CLK)	1A

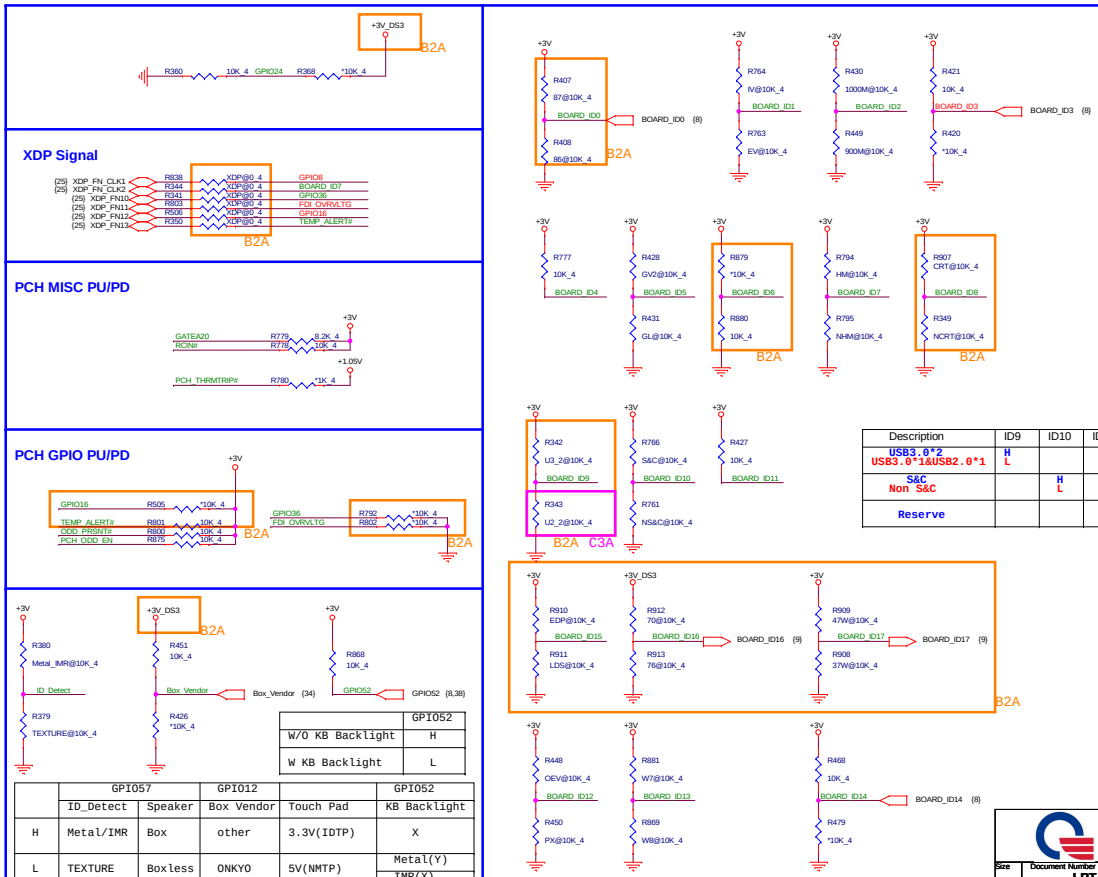
Date: Tuesday, December 25, 2012 Sheet 10 of 49

Lynx Point (GPIO,CPU/MISC,NCTF) <CLG>



BOARD ID SETTING <CLG>

Board ID	ID0	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID12	ID13	ID14	ID15	ID16	ID17
HM87 HM86	H L														
UMA SKU VGA SKU		H L													
VRAM-1000MHz VRAM-900MHz			H L												
Standard ULV				H L											
17" 14"					H L										
GV2 GL						H L									
W/ 4K2K W/O 4K2K							H L								
W/ HDMI W/O HDMI								H L							
W/ CRT W/O CRT									H L						
Only VGA Optimus										H L					
WIN7 WIN8											H L				
Reserve												H L			
EDP LVDS													H L		
Celeron I3/I5/I7														H L	
47W 37W															H L



Description	ID9	ID10	ID11
USB3.0*2 USB3.0*1&USB2.0*1	H L		
S&C Non S&C		H L	
Reserve			H L

	GPIO52
W/O KB Backlight	H
W KB Backlight	L

	GPIO57		GPIO12		GPIO52
	ID_Detect	Speaker	Box Vendor	Touch Pad	KB Backlight
H	Metal/IMR	Box	other	3.3V(IDTP)	X
L	TEXTURE	Boxless	ONKYO	5V(NMTP)	Metal(Y) IMR(X)

Quanta Computer Inc.

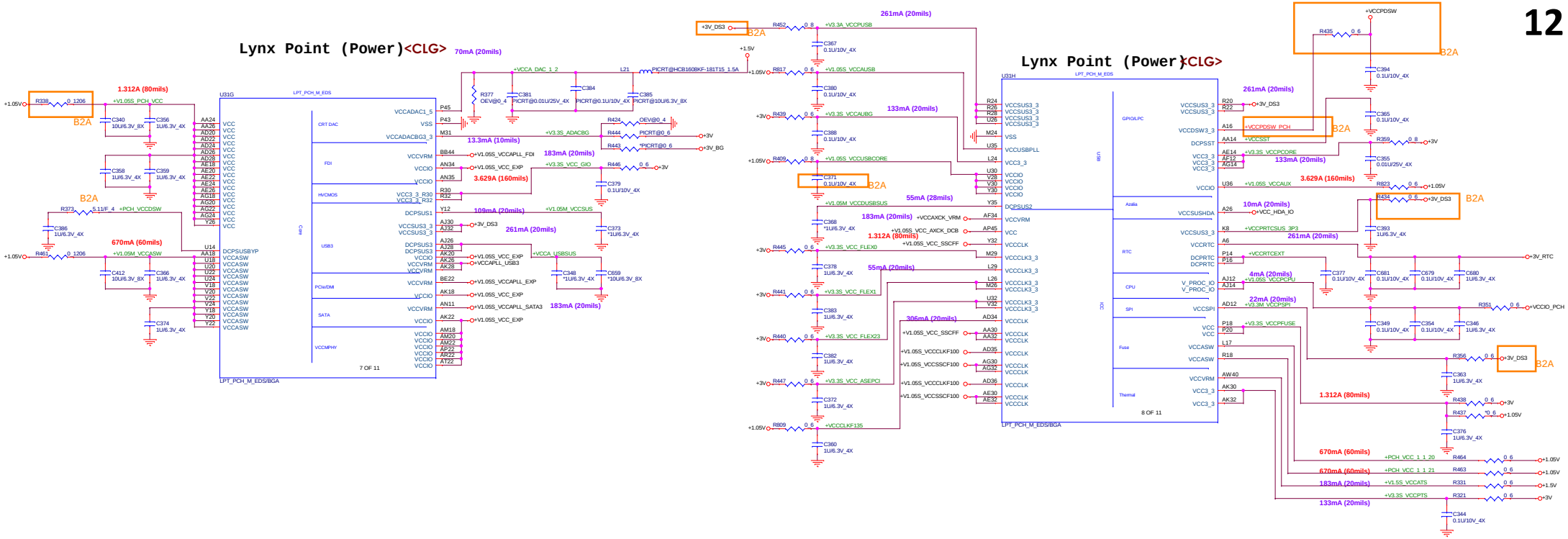
PROJECT : BD6

Size | Document Number | Rev

LPT 4/6 (GPIO/MISC) | 1A

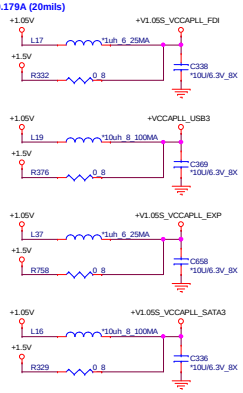
Date: Wednesday, January 09, 2013 | Sheet 11 of 49

Lynx Point (Power)<CLG>

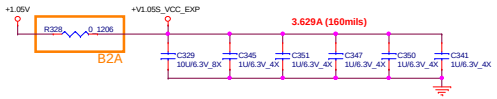


PCH VRM Power

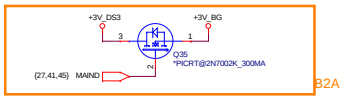
0.179A (20mils)



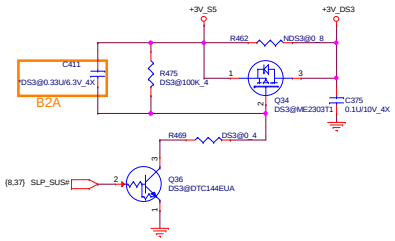
PCH VCCIO Power



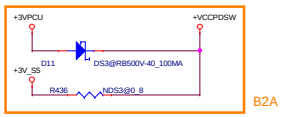
PCH band gap Power

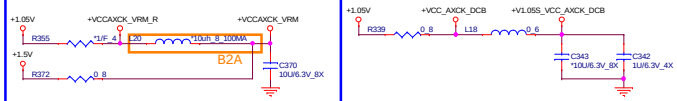


PCH DS3 VCCSUS

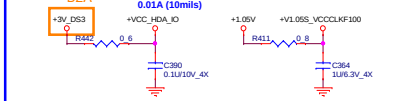


PCH DSW3





PCH HDA Power



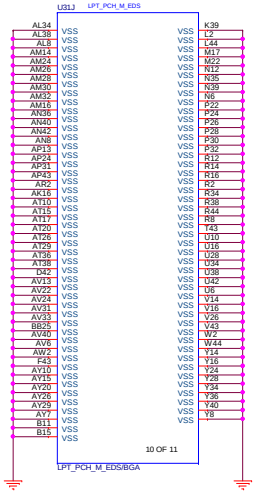
Quanta Computer Inc.

PROJECT : BD6

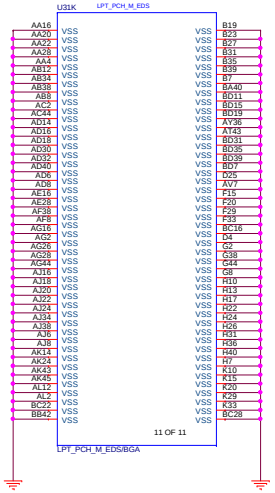
Size	Document Number	Rev
	LPT 5/6 (POWER)	1A

Date: Thursday, December 20, 2012 Sheet 12 of 49

Lynx Point (GND)<CLG>



Lynx Point (GND)<CLG>



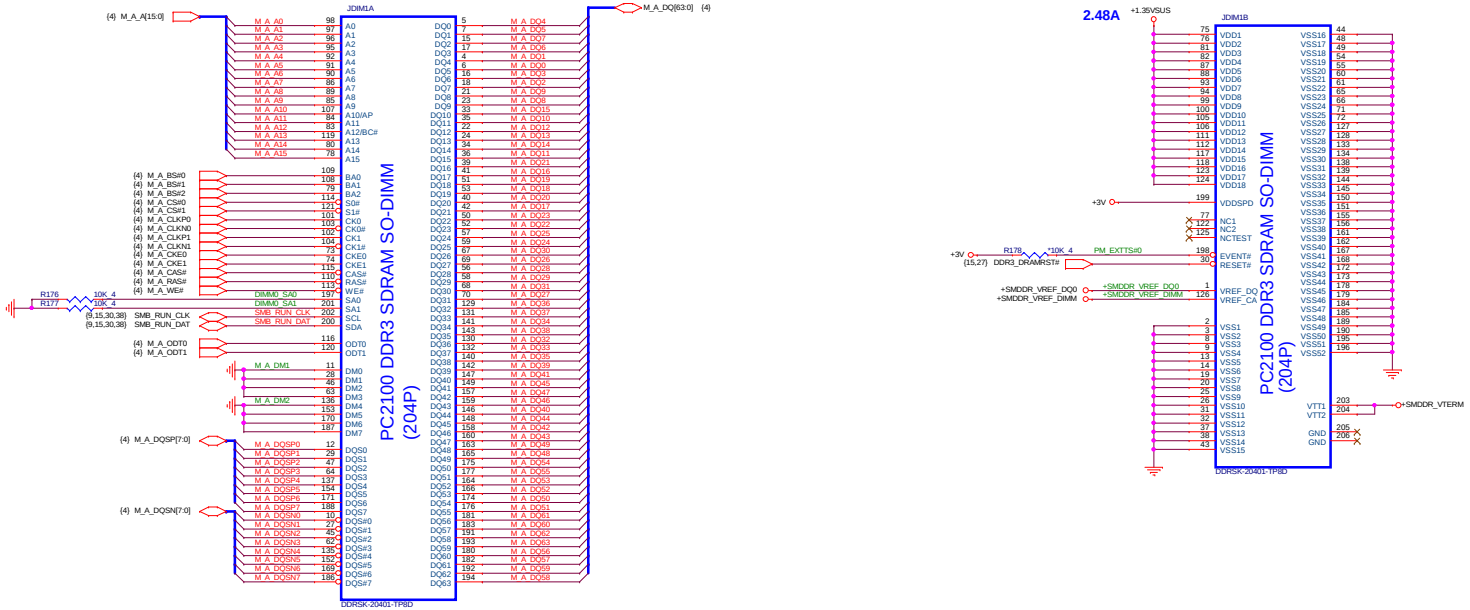
Quanta Computer Inc.

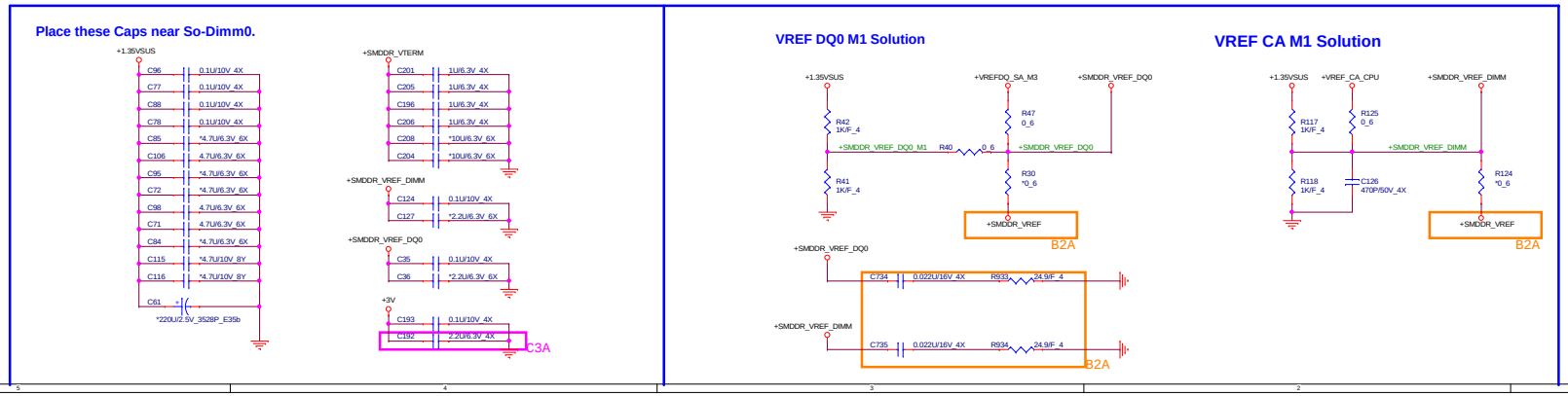
PROJECT : BD6

Size	Document Number	Rev
	LPT 6/6 (GND)	1A

Date: Thursday, December 20, 2012 Sheet 13 of 49

<DDR> H=8 (Rev)





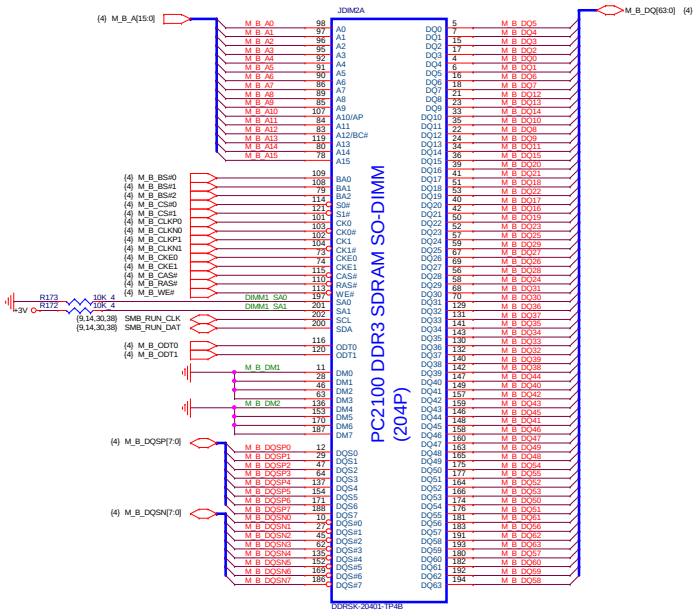
Quanta Computer Inc.

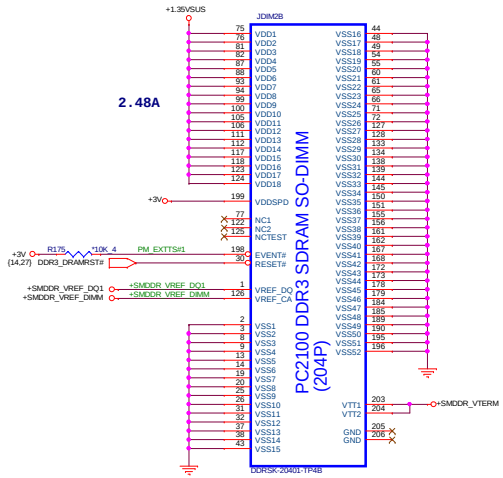
PROJECT : BD6

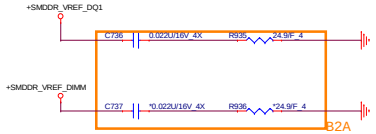
Size	Document Number	Rev
	System Memory 1/2 (5.2H)	1A

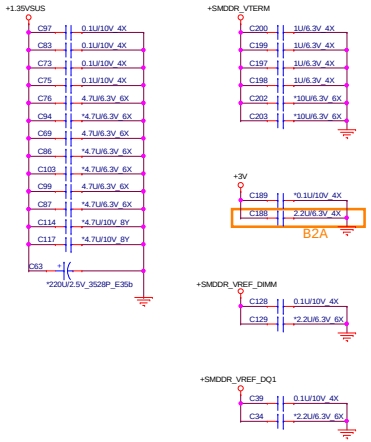
Date: Thursday, December 20, 2012 Sheet 14 of 49

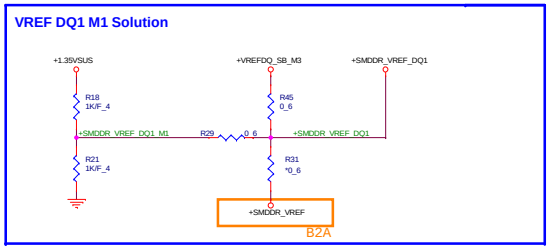
<DDR> H=4 (Rev)



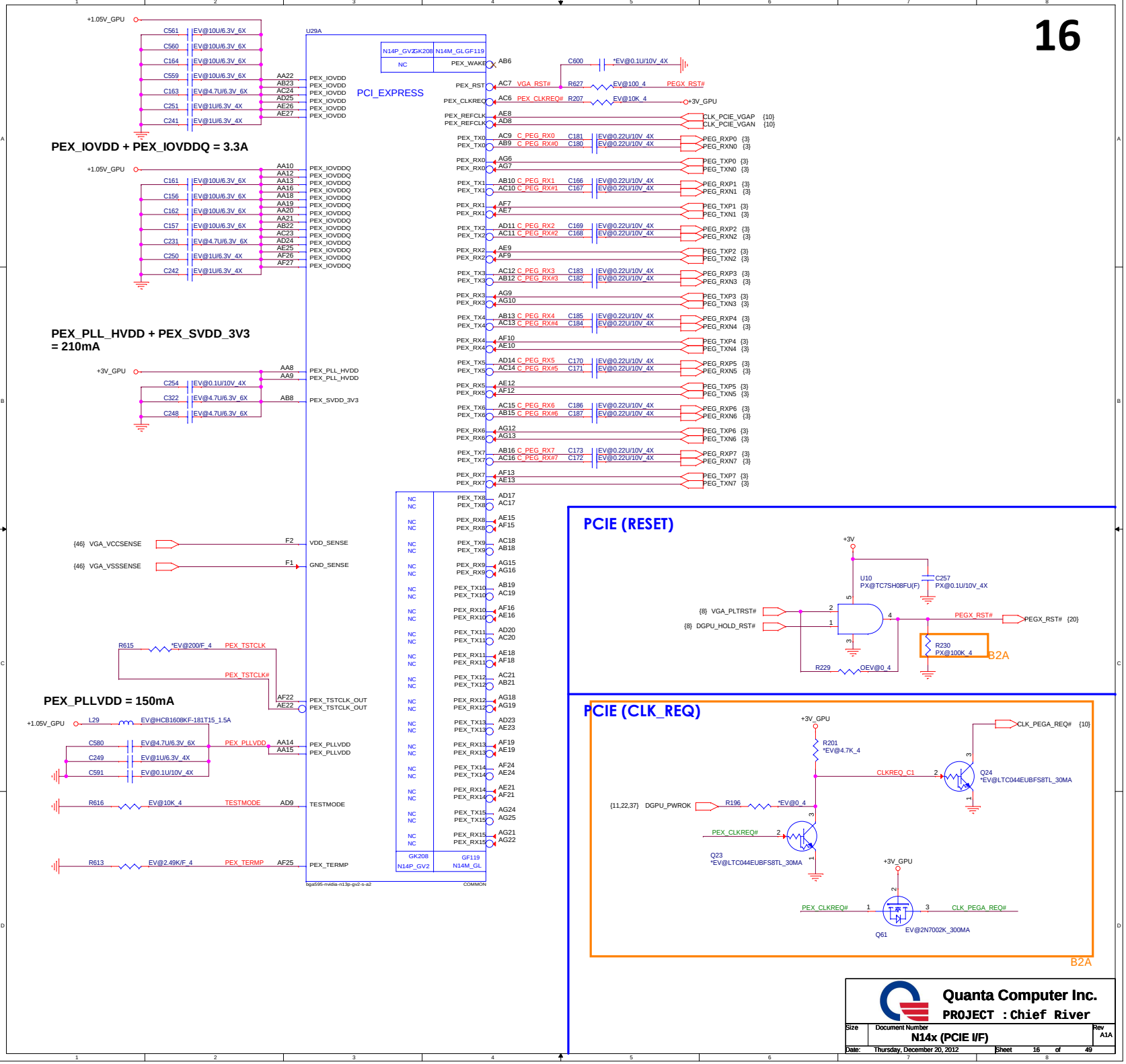


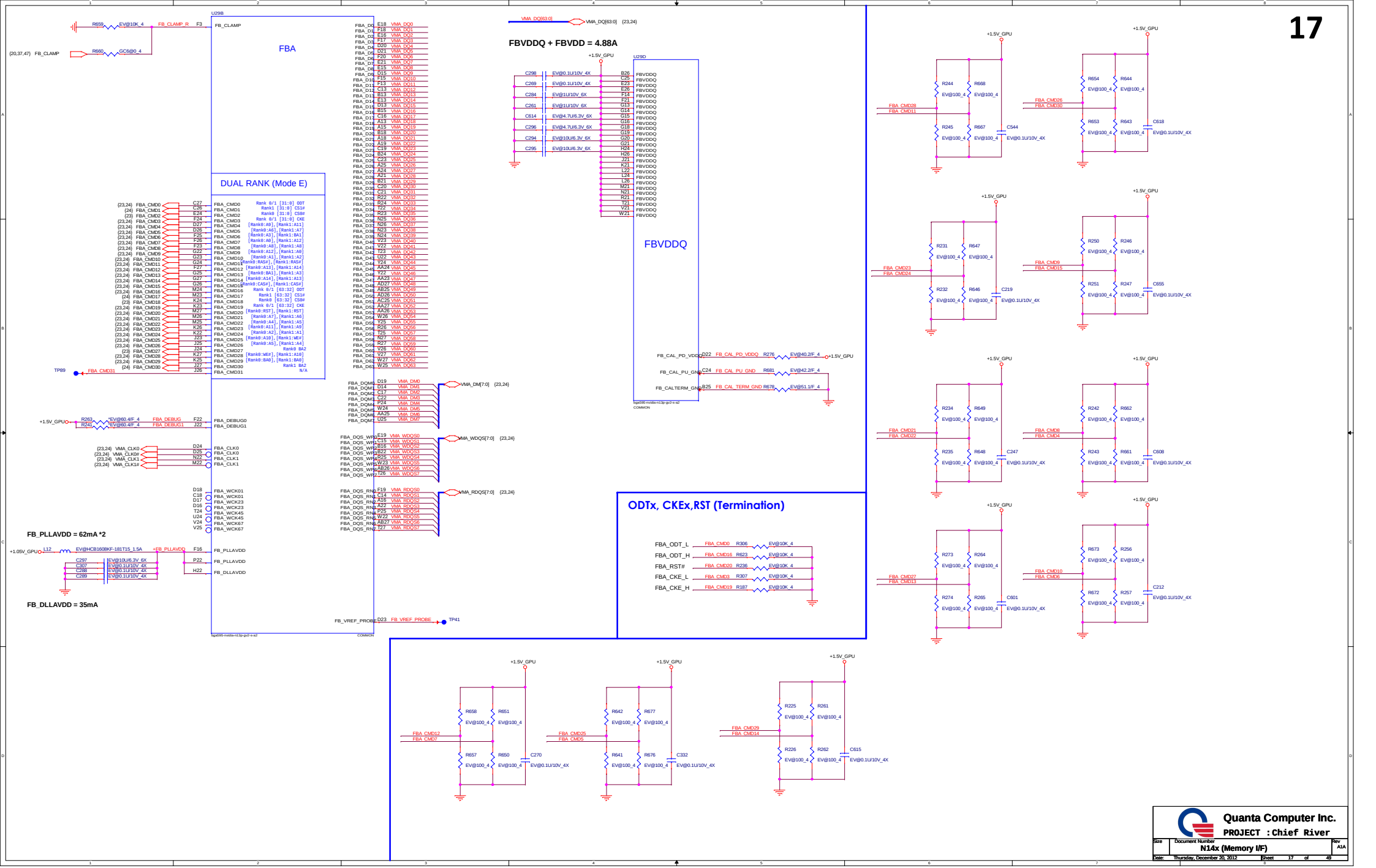






Quanta Computer Inc.		
PROJECT : BD6		
Size	Document Number: System Memory 2/2 (9.2H)	Rev 1A
Date: Thursday, December 20, 2012	Sheet 15 of 49	


PEX_IOVDD + PEX_IOVDDQ = 3.3A
PEX_PLL_HVDD + PEX_SVDD_3V3 = 210mA
PEX_PLLVDD = 150mA
U29A
PCI_EXPRESS
PCIE (RESET)
PCIE (CLK_REQ)
B2A
B2A
Quanta Computer Inc.
PROJECT : Chief River
Size
Document Number
N14x (PCIE I/F)
Rev
A1A
Date: Thursday, December 20, 2012
Sheet 16 of 49

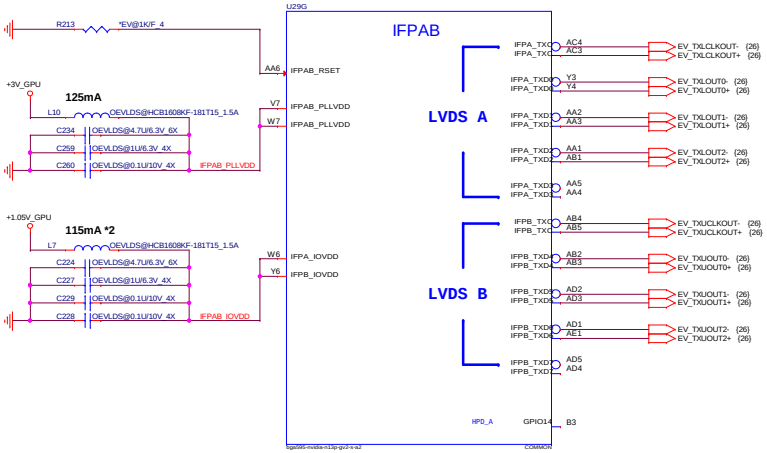


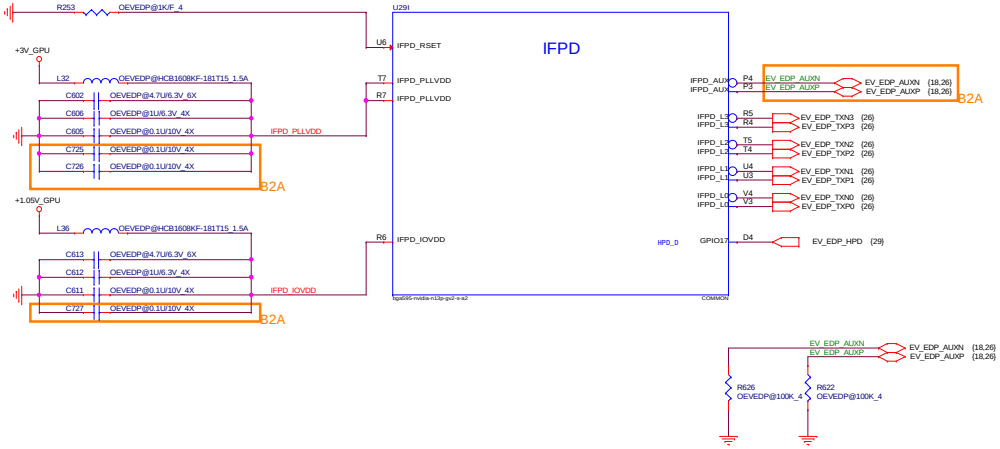
Quanta Computer Inc.

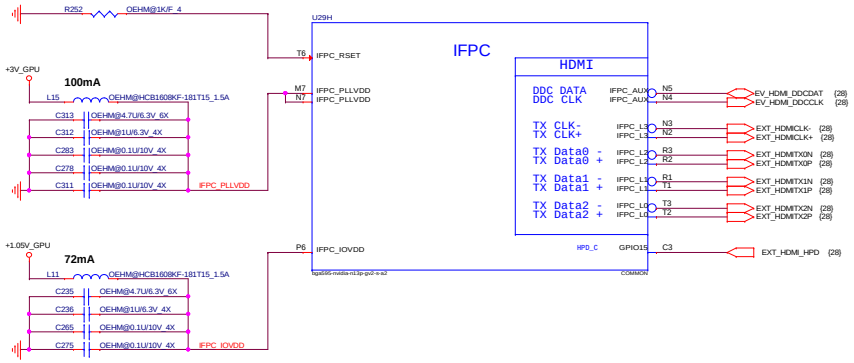
PROJECT : Chief River

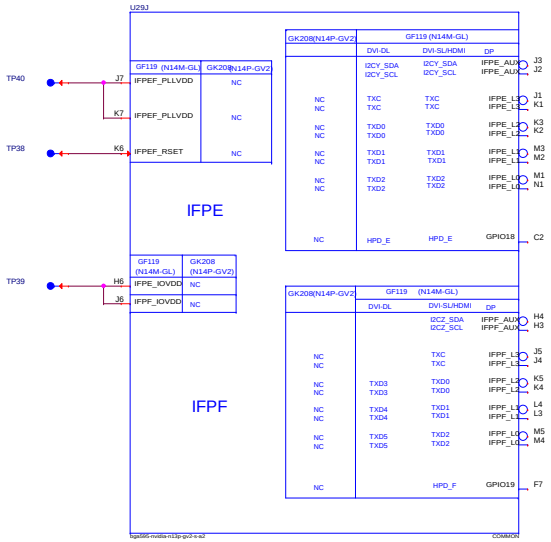
Size	Document Number	Rev
	N14x (Memory I/F)	A1A

Date: Thursday, December 20, 2012 Sheet 17 of 49







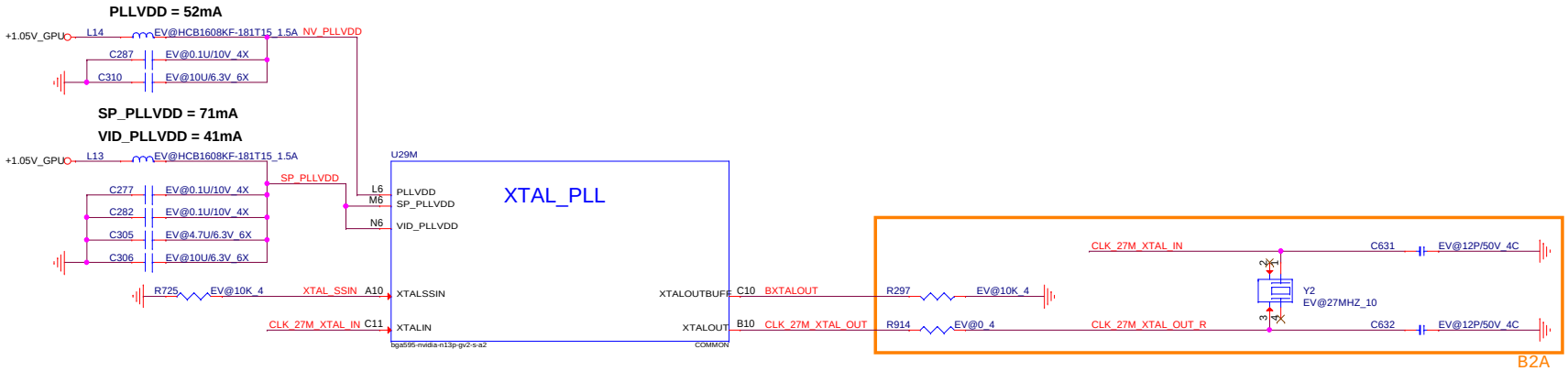


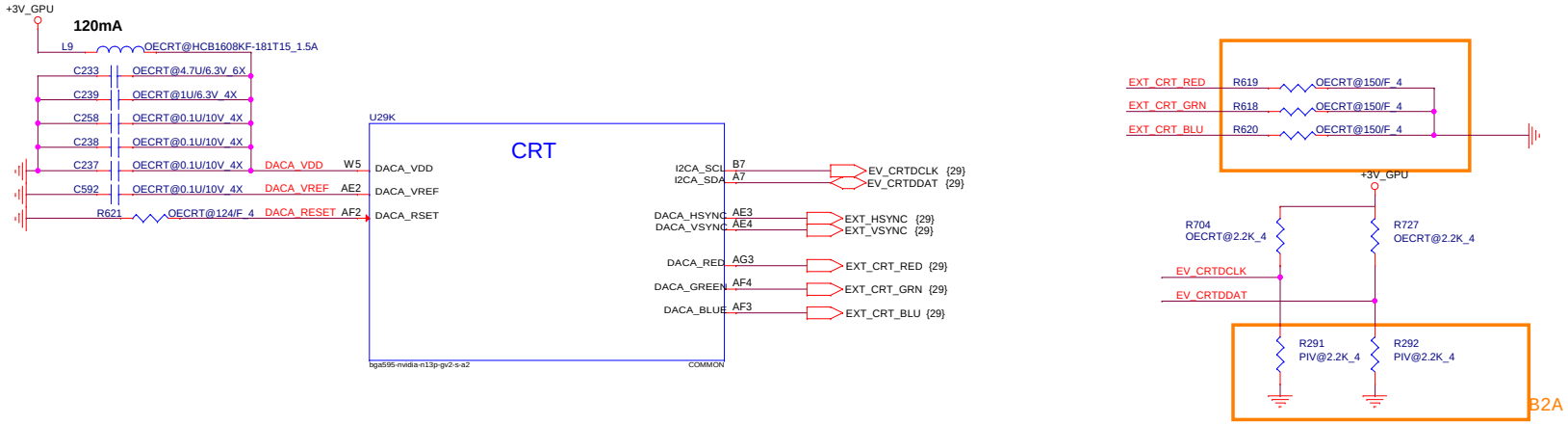
Quanta Computer Inc.

PROJECT : Chief River

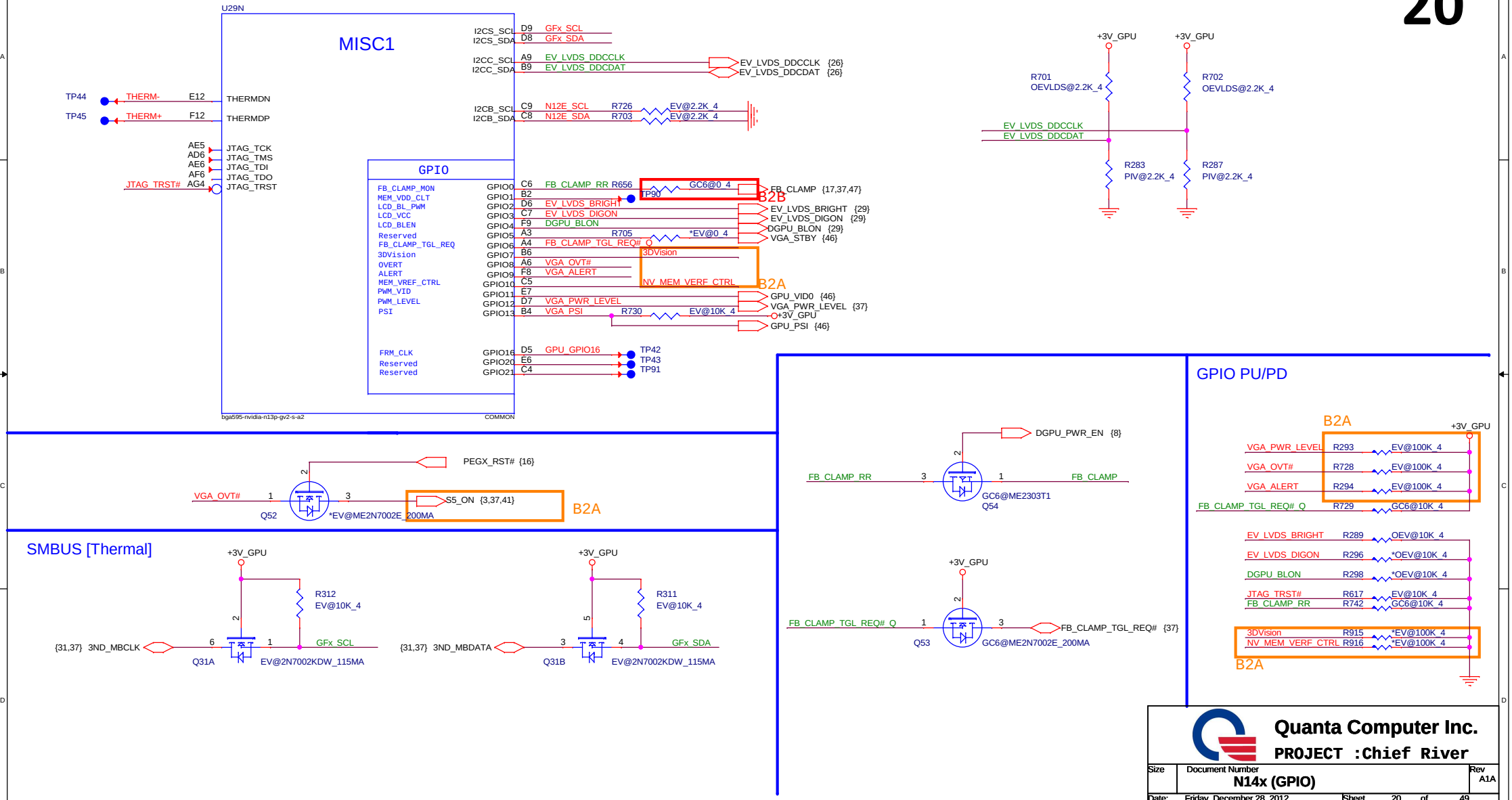
Size	Document Number	Rev
	N14x (Display I/F)	A1A

Date: Thursday, December 20, 2012 Sheet 18 of 49





Quanta Computer Inc.		
PROJECT : Chief River		
Size	Document Number N14x (XTAL/CRT I/F)	Rev A1A
Date: Thursday, December 20, 2012	Sheet 19 of 49	

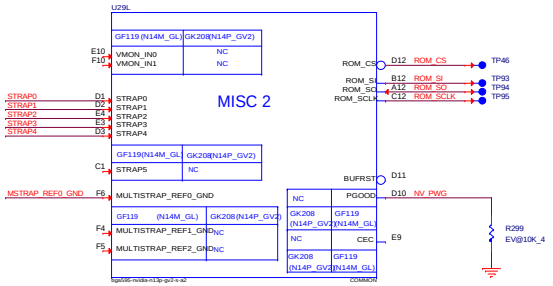


Quanta Computer Inc.

PROJECT :Chief River

Size	Document Number	Rev
	N14x (GPIO)	A1A

Date: Friday, December 28, 2012 Sheet 20 of 49



MULT STRIP [N14P_GV2]

PCI_DEVID STRAP	PCI DEVICE ID	0x1292 -->QS 0x12AD -->ES	DP_PLL_VDD33	1 [Default]	
RAM_CFG	RAM_CFG[3:0] for memory configuration		PEX_PLL_EN_TERM	PCIE PLL termination 0:Disable [Default] ; 1:Enable	
SUB_VENDOR	0:No VBIOS ROM ; 1 BIOS ROM [Default]		3GIO_PADCFG	[0000] --> Gen3 support	
FB[1:0]	[1:0] --> 256MB		PCIE_MAX_SPEED	[1] -->Allow boot to PCIE Gen3	
VGA_DEVICE	0:3D Device ; 1:VGA Device		PCIE_SPEED_CHANG_ GEN3	[1] -->Enable Gen3	
I2CS_Slave Address	0:9E [Default] ; 1:9C		SORx_EXPOSED	SOR0_EXP=0,SOR1_EXP=1 [IFPA/B:LVDS] ; [IFPC:HDMI]	
USER STRAP	Panel EDID Support				

Strap Pin name	Strapping Bits 3	Strapping Bits 2	Strapping Bits 1	Strapping Bits 0	SETTING	NOTE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDER	PCI_DEVID[5]	PEX_PLL_EN_TERM	ROM_SCLK: +3V_GPU R738 GV2@4.99K/F_4 R717 *15K/F_4	
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]	ROM_SI: +3V_GPU R735 *15K/F_4 R714 Strap_GV2@15K/F_4	
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	ROM_SO: +3V_GPU R917 P/V_GV2@4.99K/F_4; +3V_GPU R736 OEV_GV2@10K/F_4; R715 *15K/F_4	
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	STRAP0: +3V_GPU R693 GV2@45.3K/F_4 R692 *15K/F_4	
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	STRAP1: +3V_GPU R698 *15K/F_4 R697 GV2@45.3K/F_4	
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	STRAP2: +3V_GPU R666 *15K/F_4 R670 GV2@15K/F_4	
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	STRAP3: +3V_GPU R675 *15K/F_4 R674 OEV_GV2@15K/F_4; STRAP3: +3V_GPU R685 *15K/F_4 R684 P/V_GV2@4.99K/F_4	
STRAP4	RESERVED	PCIE_SPEED_CHAN CE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	STRAP4: +3V_GPU R720 *15K/F_4 R723 GV2@45.3K/F_4	

4.99K	1000	0000	24.9K	1100	0100
10K	1001	0001	30.1K	1101	0101
15K	1010	0010	34.8K	1110	0110
20K	1011	0011	45.3K	1111	0111
Resistor Value	VDD33	GND	Resistor Value	VDD33	GND

MSTRAP_REF0_GND R260 GV2@40.2K/F_4

Binary Strap [N14M_GL]

Strap Pin name	Strap Mapping	Polarity	SETTING
ROM_SCLK	SMB_ALT_ADDR	Pull-down to GND	ROM_SCLK: +3V_GPU R739 *10K_4 R718 GL@10K_4
ROM_SI	SUB_VENDER	Pull-UP to 3V3 if VBIOS ROM Exists Pull-down to GND if no VBIO ROM	ROM_SI: +3V_GPU R734 *10K_4 R713 GL@10K_4
ROM_SO	VGA_DEVICE	Pull-down to GND (no dispaly)	ROM_SO: +3V_GPU R737 *10K_4 R716 GL@10K_4
STRAP0	RAMCFG[0]	USER defined	STRAP0: A1 +3V_GPU R690 Strap_GL@10K_4 R689 A0 Strap_GL@10K_4
STRAP1	RAMCFG[1]	USER defined	STRAP1: B1 +3V_GPU R709 Strap_GL@10K_4 R708 B0 Strap_GL@10K_4
STRAP2	RAMCFG[2]	USER defined	STRAP2: C1 +3V_GPU R671 Strap_GL@10K_4 R665 C0 Strap_GL@10K_4
STRAP3	RAMCFG[3]	USER defined	STRAP3: D1 +3V_GPU R680 Strap_GL@10K_4 R679 D0 Strap_GL@10K_4
STRAP4	PCIE_MAX_SPEED	Pull-down to GND	STRAP4 R719 GL@10K_4

128M (2G bit)	Hynix H1	H5TQ2G63DFR-N0C (128M*16) GL/GV2		x4=1GB	GL:0x06 0110	GV2:0x06 0110	1000MHz
				x8=2GB		GV2:0x06 0110	1000MHz
	Hynix H2	H5TQ2G63DFR-11C (128M*16) GL/GV2		x4=1GB	GL:0x06 0110	GV2:0x06 0110	900MHz
				x8=2GB		GV2:0x06 0110	900MHz
	Samsung S1	K4W2G1646E-BC1A (128M*16) GL/GV2		x4=1GB	GL:0x05 0101	GV2:0x07 0111	1000MHz
				x8=2GB		GV2:0x07 0111	1000MHz
	Samsung S2	K4W2G1646E-BC11 (128M*16) GL/GV2		x4=1GB	GL:0x05 0101	GV2:0x07 0111	900MHz
				x8=2GB		GV2:0x07 0111	900MHz
	Micron M1	MT41J128M16JT-107G:K (128M*16) GL/GV2		x4=1GB	GL:0x01 0001	GV2:0x05 0101	900MHz
				x8=2GB		GV2:0x05 0101	900MHz
	Micron M2	MT41J128M16JT-093G:K (128M*16) GL/GV2		x4=1GB	GL:0x01 0001	GV2:0x05 0101	1000MHz
				x8=2GB		GV2:0x05 0101	1000MHz
256M (4Gbit)	Micron M3	MT41K256M16HA-107G:E (256M*16) GL/GV2		x4=2GB	GL:0x0D 1101	GV2:0x01 0001	900MHz
				x8=4GB		GV2:0x01 0001	900MHz
	Samsung S3	K4W4G1646B-HC11 (256M*16) GL/GV2		x4=2GB	GL:0x0B 1011	GV2:0x03 0011	900MHz
				x8=4GB		GV2:0x03 0011	900MHz
	Hynix H3	H5TQ4G63MFR-11C (256M*16) GL		x4=2GB	GL:0x03 0011		900MHz
				N/A			
	Hynix H4	H5TQ4G63AFR-11C (256M*16) GL		x4=2GB	GL:0x04 0100		900MHz
				N/A			

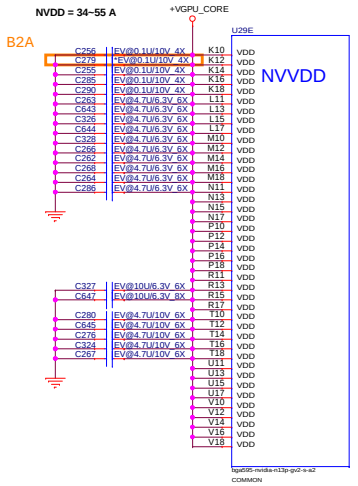
N14P_GV2	H1/H2	S1/S2	M1/M2	S3	M3
ROM_SI	34.8K	45.3K	30.1K	20K	10K
	CS33482FB22	CS34532FB18	CS33012FB18	CS32002FB29	CS31002FB26

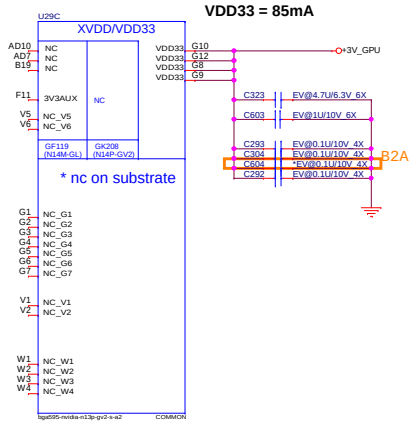
N14M_GL	Strap3	Strap2	Strap1	Strap0
H1	D0	C1	B1	A0
H2	D0	C1	B1	A0
H3	D0	C0	B1	A1
H4	D0	C1	B0	A0
S1	D0	C1	B0	A1
S2	D0	C1	B0	A1
S3	D1	C0	B1	A1
M1	D0	C0	B0	A1
M2	D0	C0	B0	A1
M3	D1	C1	B0	A1

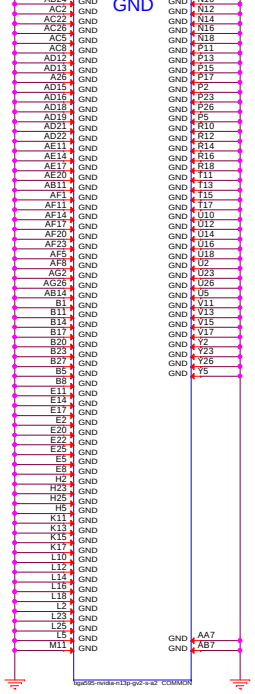
Quanta Computer Inc.
PROJECT : Chief River

Size	Document Number	Rev
	MSIC & STRAP	A1A

Date: Thursday, December 20, 2012 Sheet 21 of 49

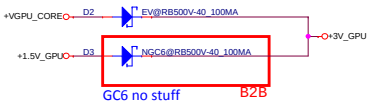


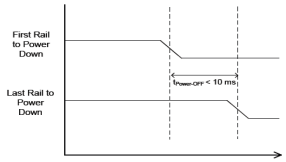


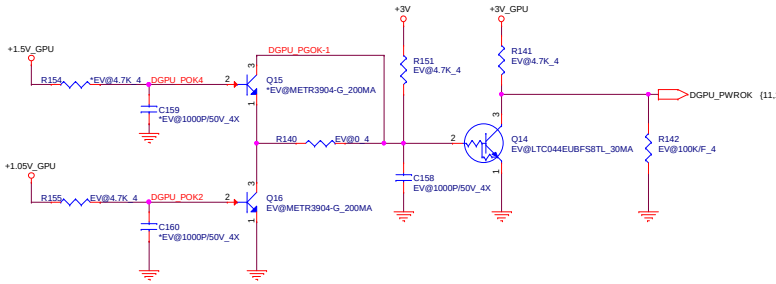


Power down sequence

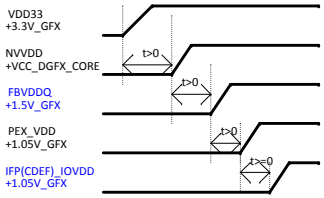
for meet Power down sequence for +3V_GFX







Power up sequence



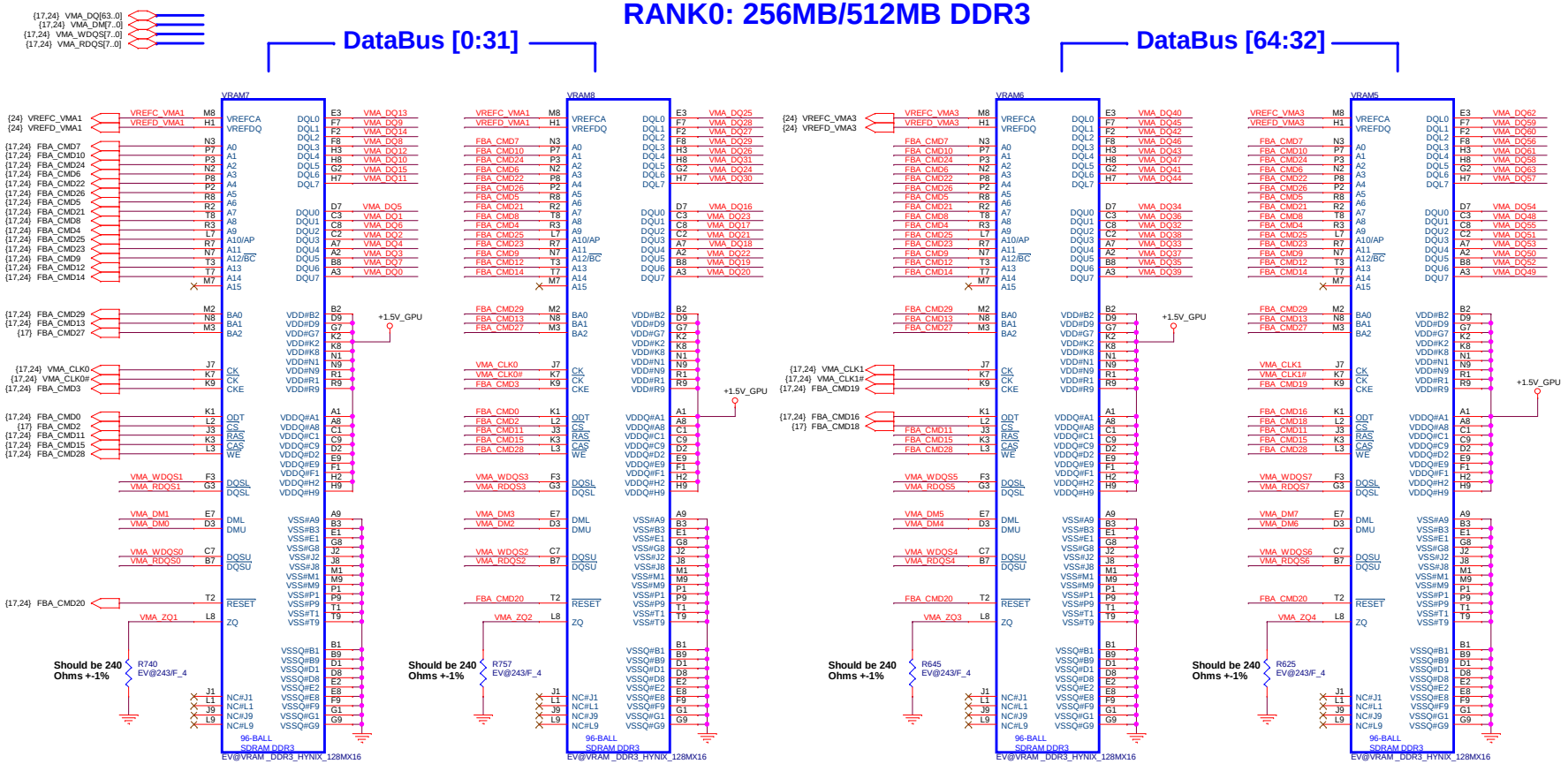
Quanta Computer Inc.

PROJECT : Chief River

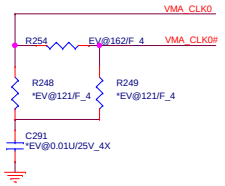
Size	Document Number	Rev
	N14x (Power/GND)	A1A

Date: Thursday, January 03, 2013 Sheet 22 of 49

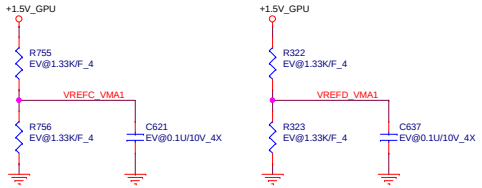
RANK0: 256MB/512MB DDR3



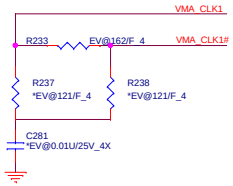
CLK-A0 Termination



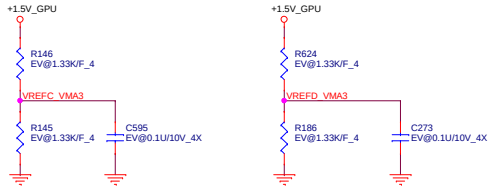
MEM Reference Voltage (Low)



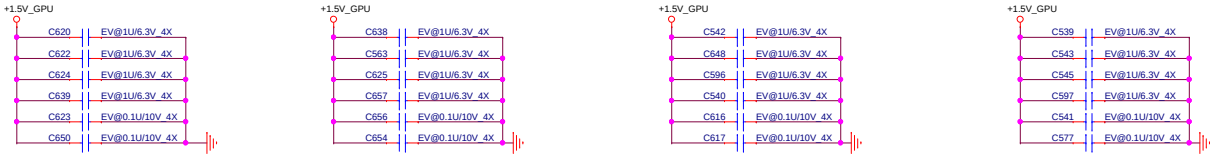
CLK-A1 Termination



MEM Reference Voltage (High Bus)



VRAM De-Coupling



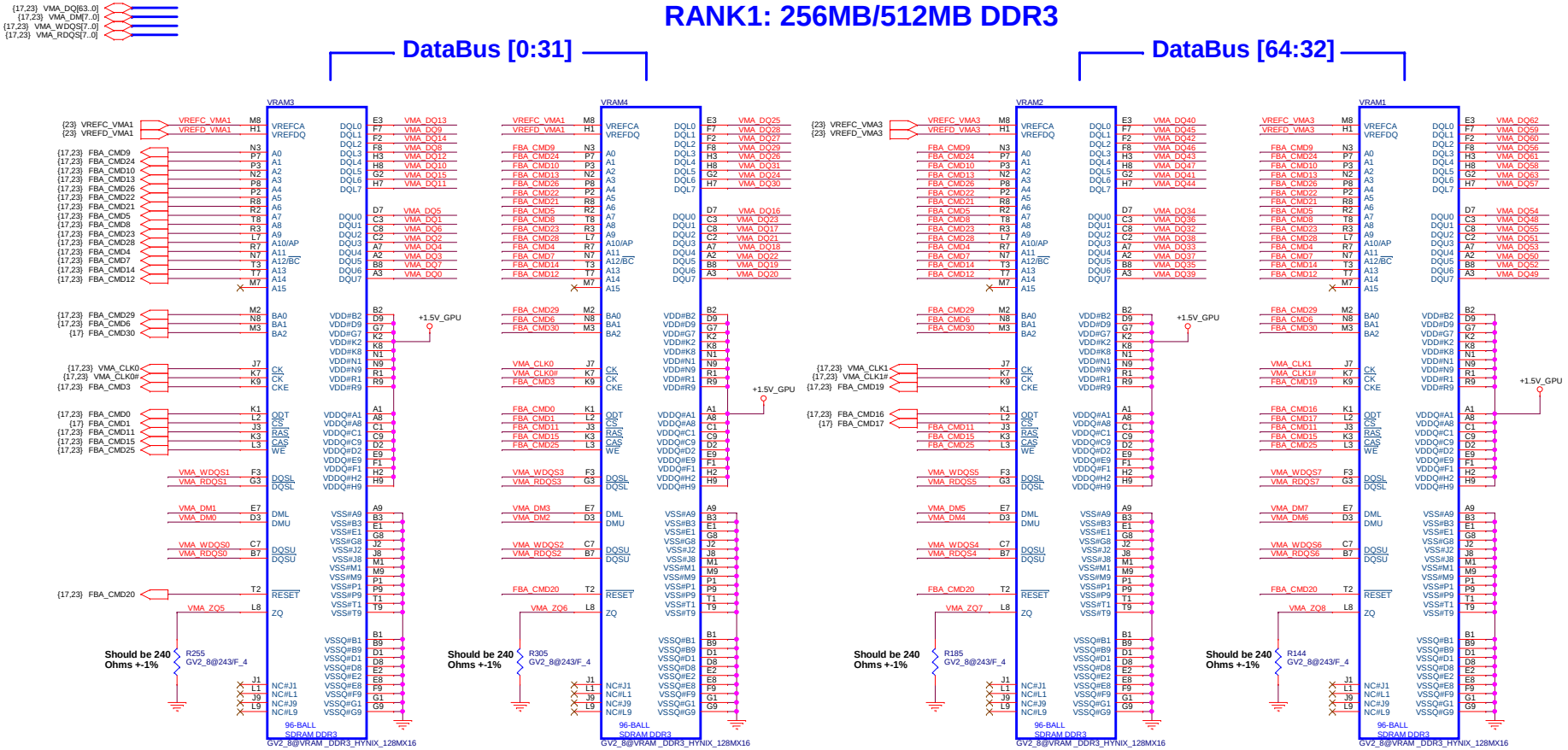
Quanta Computer Inc.

PROJECT : Chief River

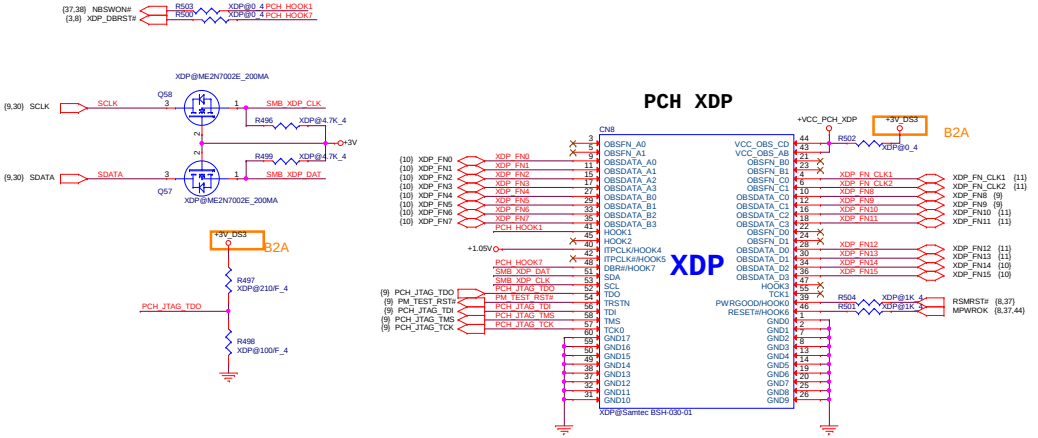
Size	Document Number	Rev
	N14x (DDR/Rank0)	A1A

Date: Thursday, December 20, 2012 Sheet 23 of 49

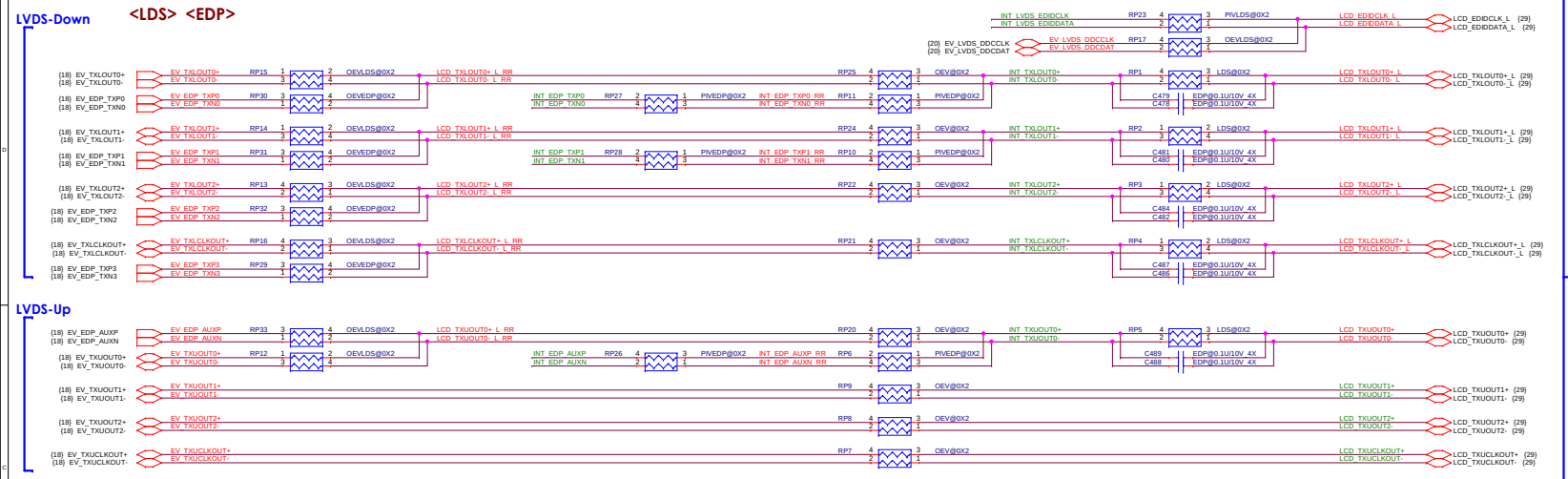
RANK1: 256MB/512MB DDR3



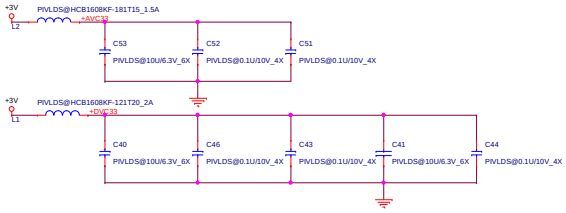
VRAM De-Coupling



Quanta Computer Inc.	
PROJECT : BD6	
Size	Document Number: VRAM_B: DDR3*4PCS — Rev: A1A
Date: Tuesday, December 18, 2012	Sheet 25 of 49



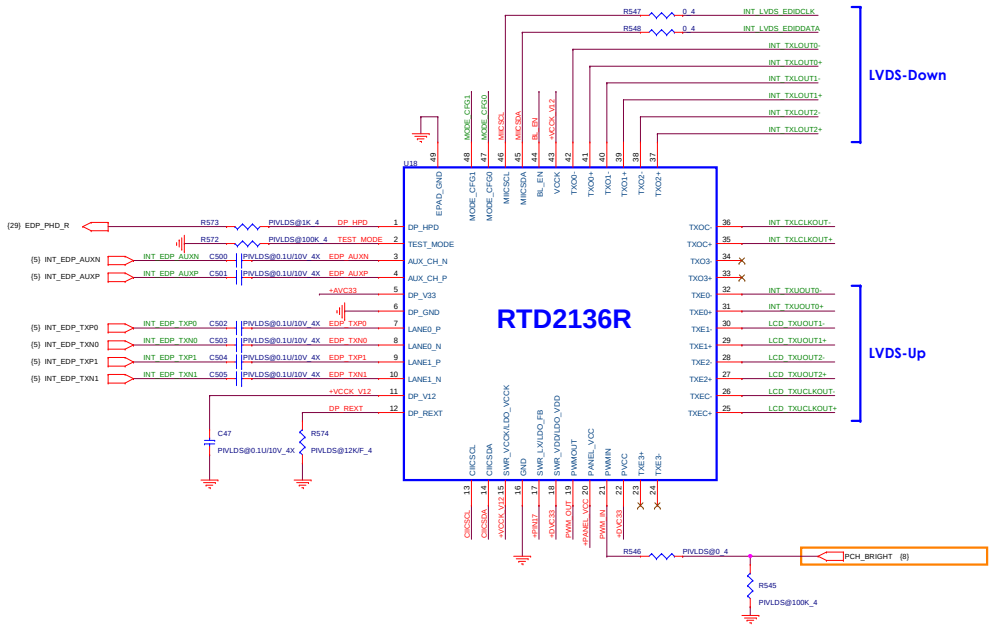
Note:
1. C1,C4,C7,C8,C9,C16 should be closed to chip
2. C9 should be X5R material
3. R8 should be 12K olm with +/- 1%
4 Entire trace of Panel VCC should be wider than 80-mil

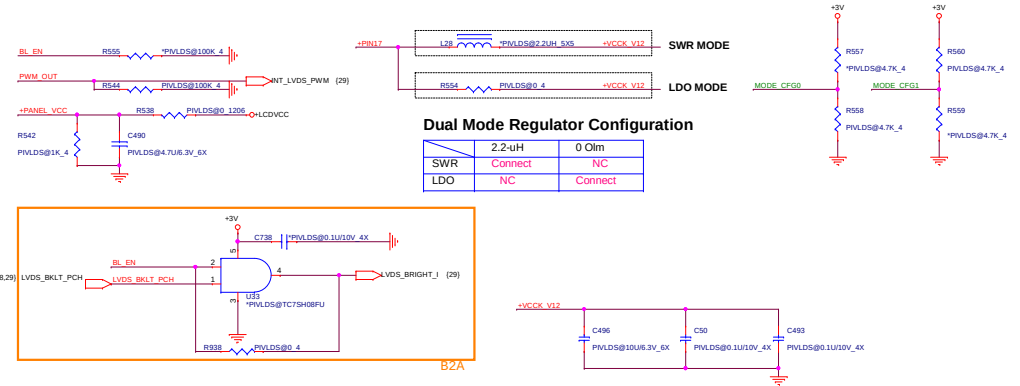


Mode Configure Table(Power On Latch)

		CFG0	
		0	1
CFG1	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

ROM ONLY Mode : CFG0 4.7K pull low, CFG1 4.7K pull high
EP Mode : CFG0 4.7K pull high, CFG1 4.7K pull low
EEPROM Mode : CFG0 4.7K pull high, CFG1 4.7K pull high





Dual Mode Regulator Configuration

	2.2-uH	0 Olm
SWR	Connect	NC
LDO	NC	Connect

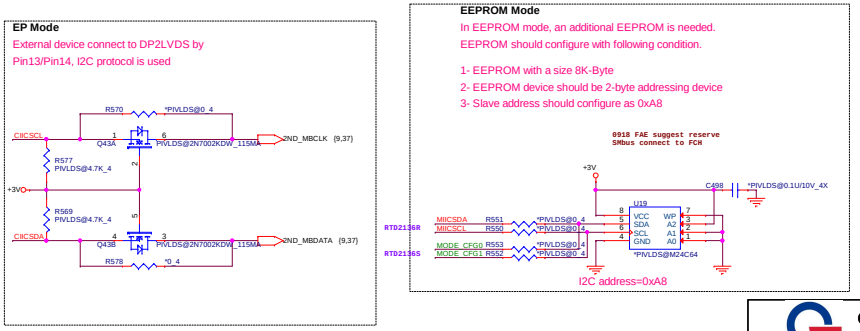
EP Mode

External device connect to DP2LVDS by Pin13/Pin14, I2C protocol is used

EEPROM Mode

In EEPROM mode, an additional EEPROM is needed.
EEPROM should configure with following condition.

1- EEPROM with a size 8K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8

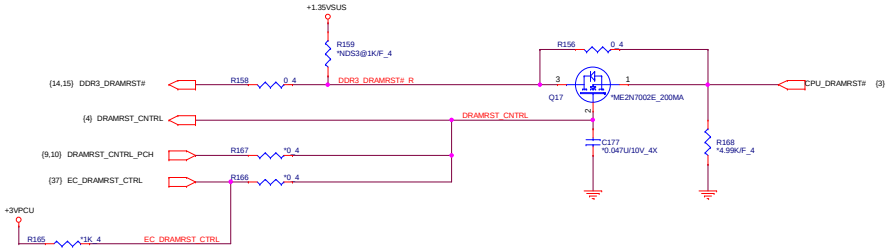


Quanta Computer Inc.
PROJECT : BD6

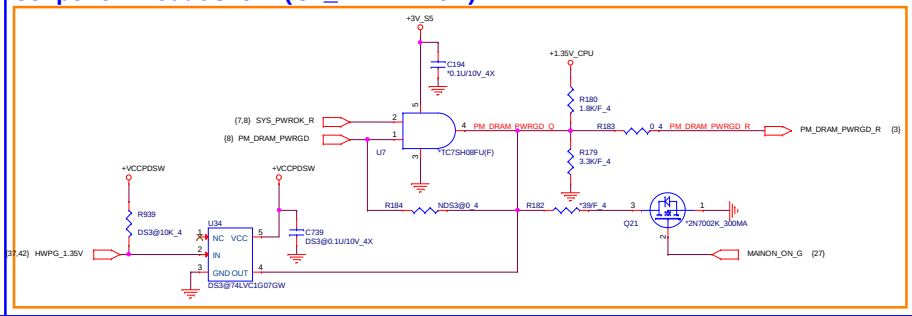
Size	Document Number	Rev
	EDP to LVDS	A1A

Date: Thursday, December 20, 2012 Sheet 26 of 49

S3 power Reduction (SM_DRAMRST#) <S3P>

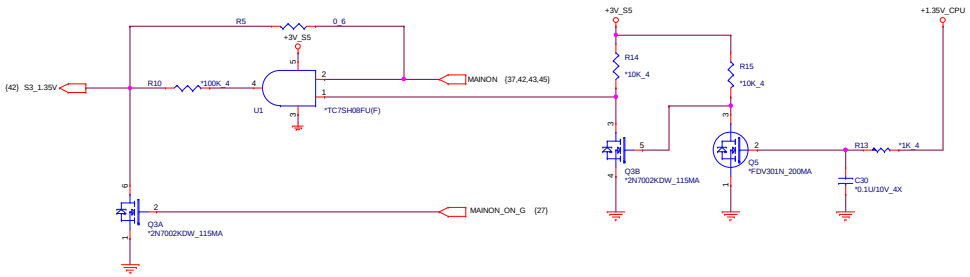


S3 power Reduction (SM_DRAMPWROK) <S3P>

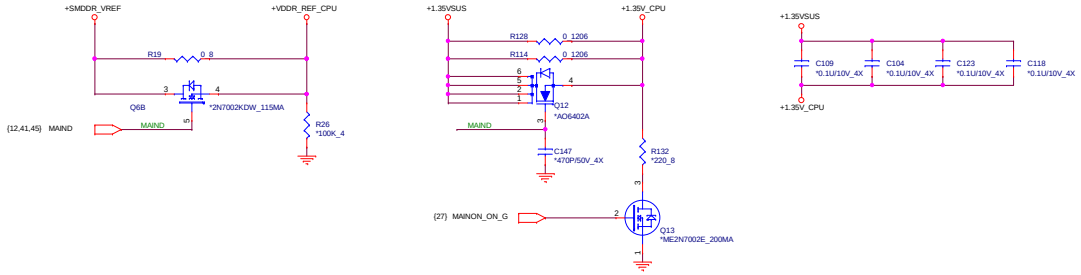


B2A

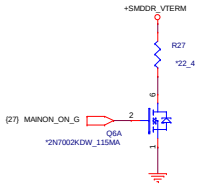
For S3 power Reduction Sequence <S3P>



S3 power Reduction (CPU Power) <S3P>

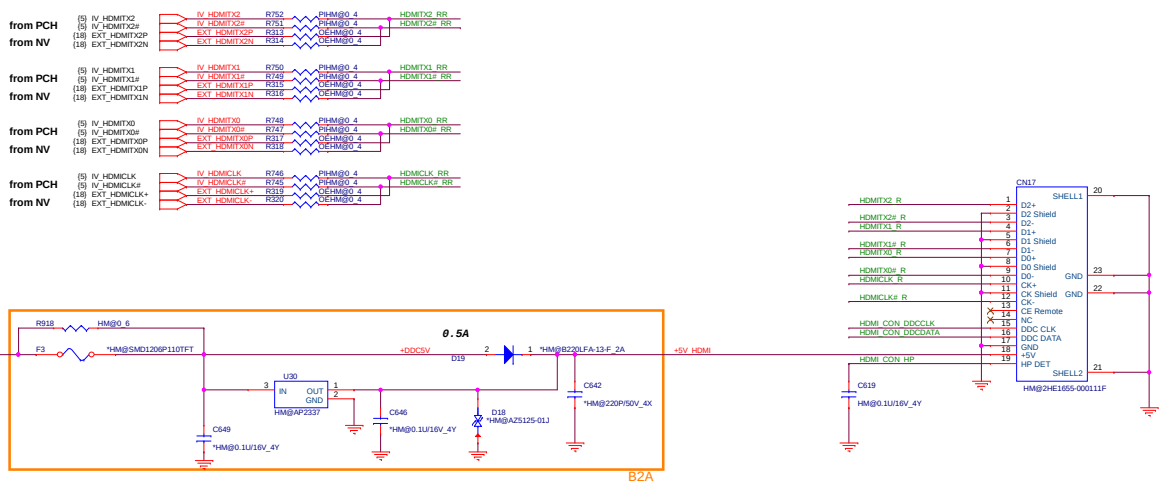


For S3 power Reduction VTT discharge <S3P>

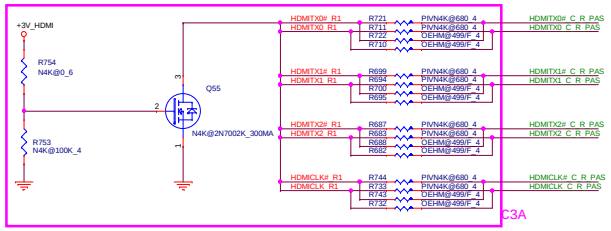


Quanta Computer Inc.		
PROJECT : BD6		
Size	Document Number: S3 power Reduction	Rev: A1A
Date: Thursday, December 20, 2012	Sheet 27 of 49	

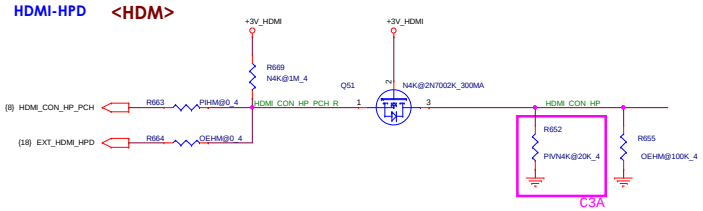
HDMI Conn <HDM>



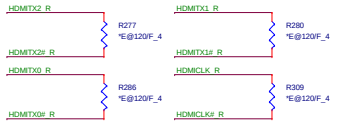
HDMI-passive level shift <HDM>



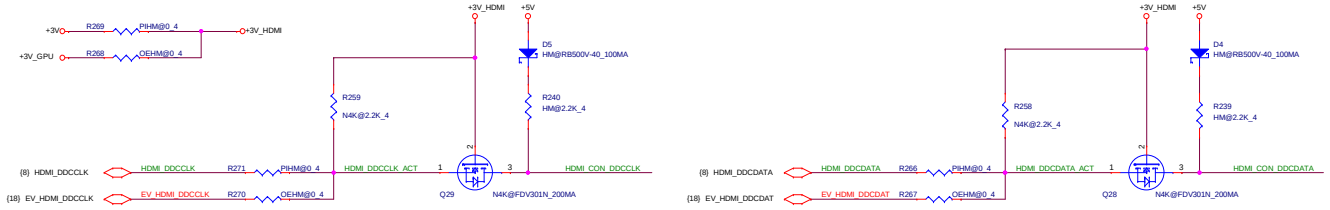
HDMI-HPD <HDM>



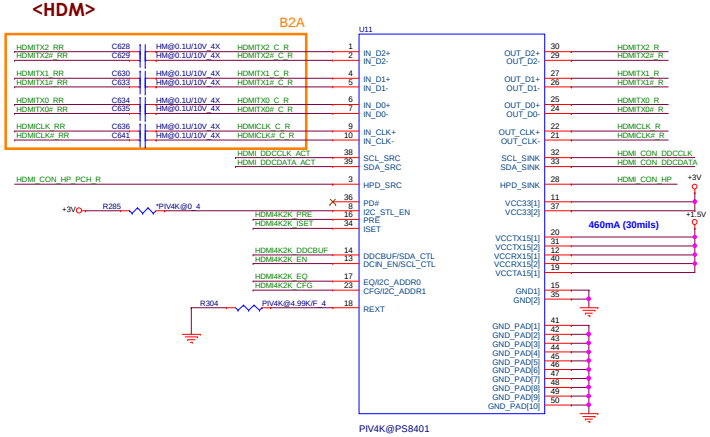
FOR EMI <EMC>

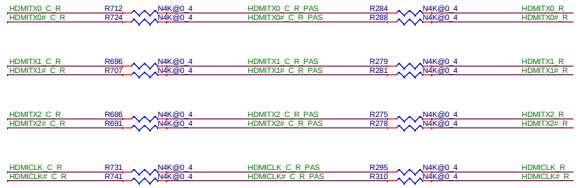


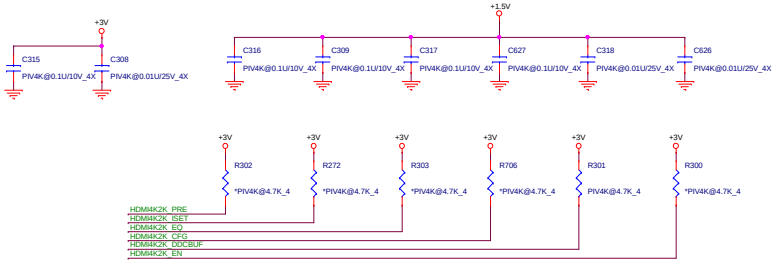
HDMI-SMBus <HDM>



<HDM>







	Pre	ISET	EQ	CFG	DDCBUF	DCIN_EN
NC(Low)	0 dB	default	12.4 dB	HDMI ID disable	default	default,AC coupling input
1(High)	1.6 dB	+13%	4.3 dB	HDMI ID enable	active DDC buffer with default threshold	DC coupling input
M	2.5 dB	-13%	8.6 dB	N/A	active DDC buffer without internal pull up resistor	N/A

Pre	Output pre-emphasis setting
ISET	TMDS output swing adjustment
EQ	Receiver equalization setting
CFG	Configuration pin
DDCBUF	enable active DDC buffer
DCIN_EN	DC coupling enable

Pin	PS8401A	PS8201A
12	VDDRX	NC
15	GND	NC
34	ISET	NC
37	VDD33	NC

Quanta Computer Inc.

PROJECT : BD6

Size	Document Number	Rev
	HDMI CONN	1A

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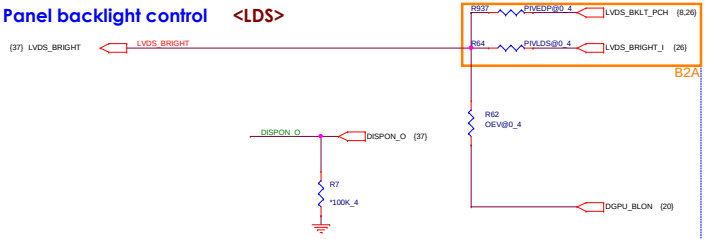
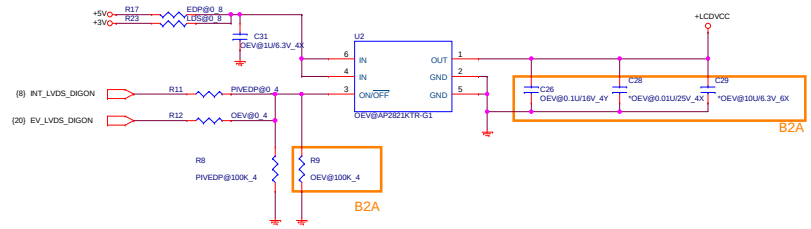
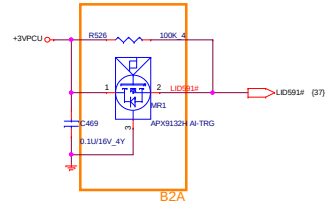
Panel backlight control <LDS>



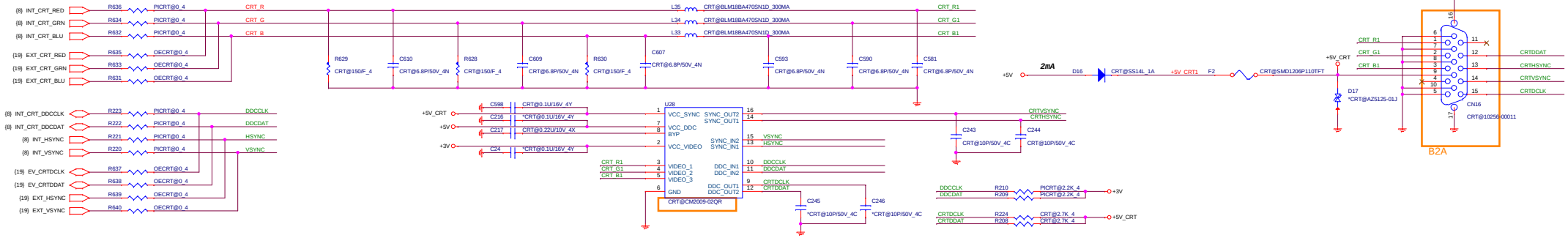
LCD POWER SWITCH <LDS>



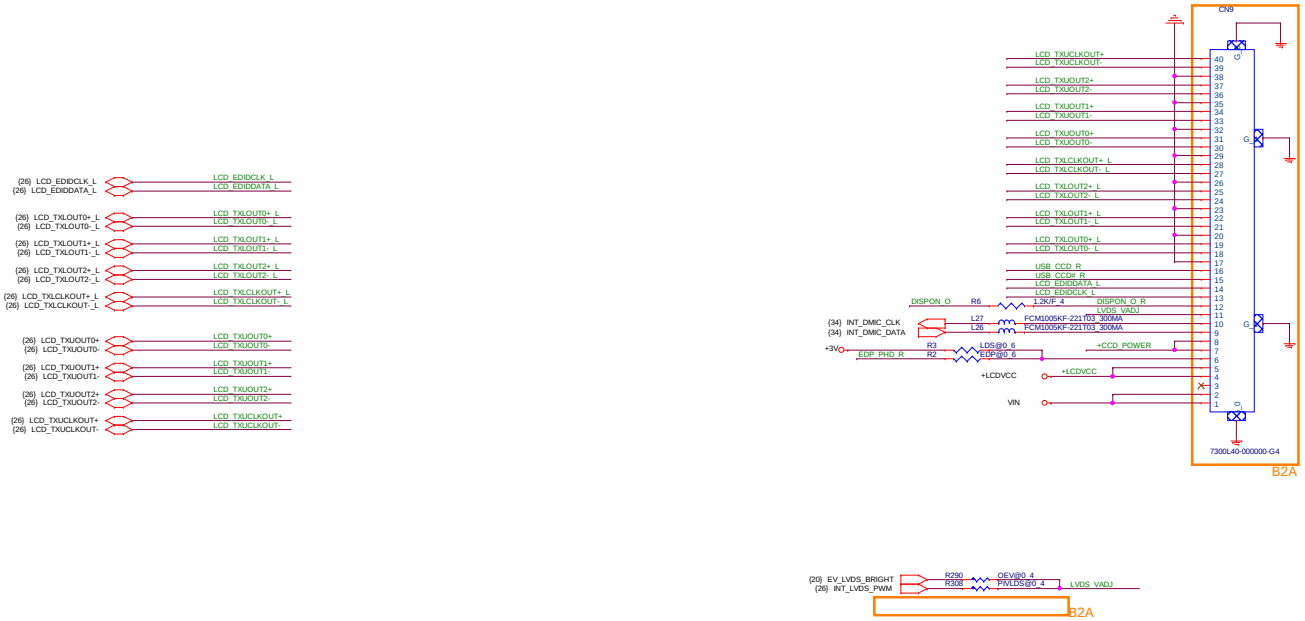
HALL Sensor <HSR>



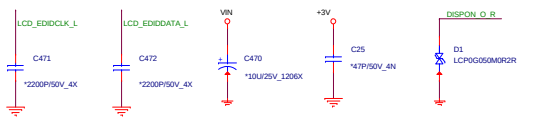
CRT <CRT>



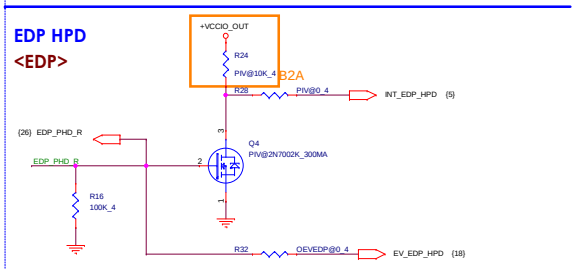
LCD Panel Module <LDS>



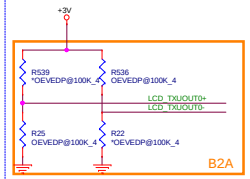
CCD <CCD>



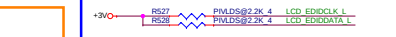
EDP HPD <EDP>



EDP PU/PD <EDP>



SMBus <LDS>



Quanta Computer Inc.

PROJECT : BD6

Size	Document Number	Rev
	LCD/CRT/CCD	1A

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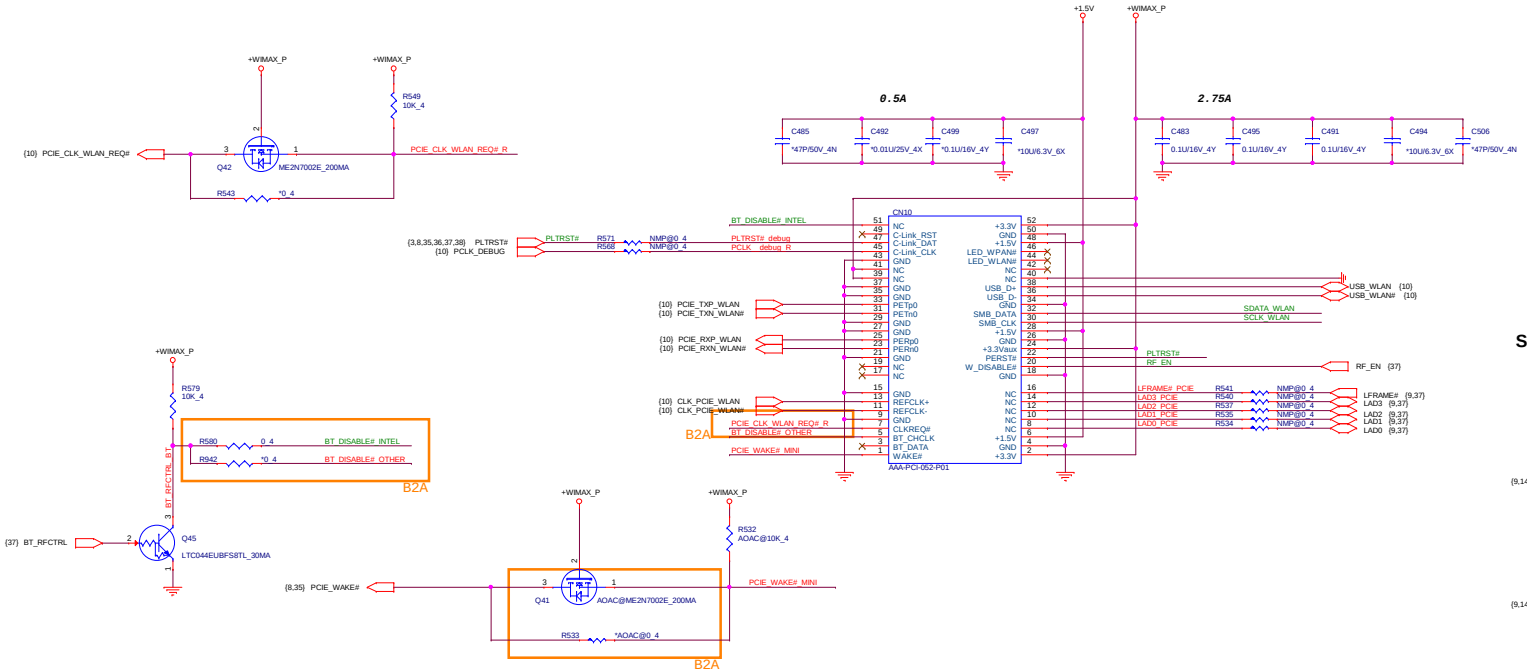
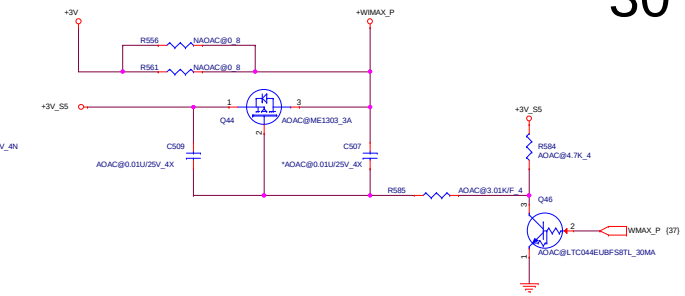
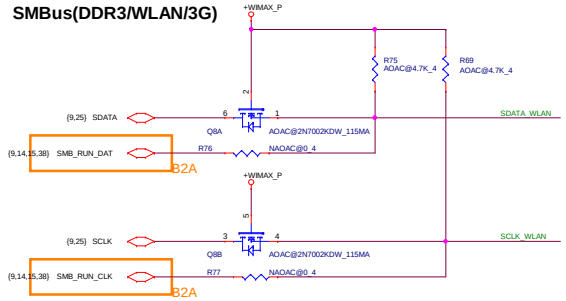
MINI Card Slot#1(WiFi / Wimax / Combo) <MNW>



AOAC <MNW>



SMBus(DDR3/WLAN/3G)



Quanta Computer Inc.

PROJECT : BD5

Size	Document Number	Rev
	MINI CARD(WLAN)	1A

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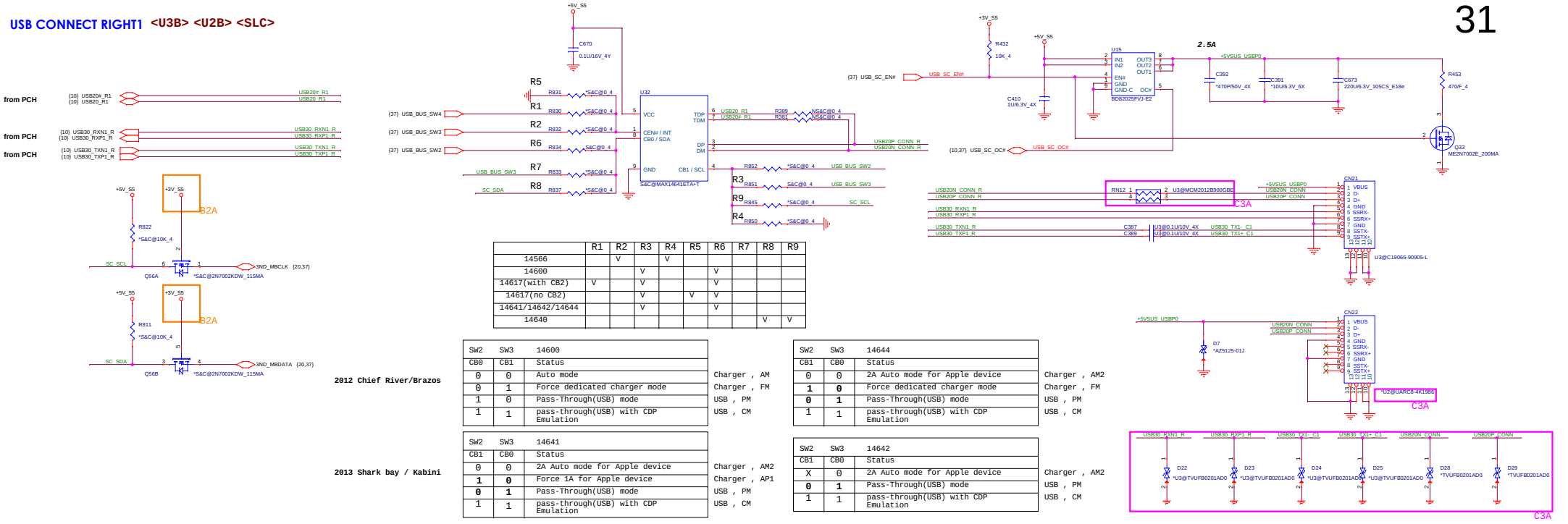
USB CONNECT RIGHT1 <U3B> <U2B> <SLC>



	R1	R2	R3	R4	R5	R6	R7	R8	R9
14566		V		V					
14600			V			V			
14617(with CB2)	V		V			V			
14617(no CB2)			V		V	V			
14641/14642/14644			V			V			
14640								V	V

2012 Chief River/Brazos

SW2	SW3	14600	
CB0	CB1	Status	
0	0	Auto mode	Charger , AM
0	1	Force dedicated charger mode	Charger , FM
1	0	Pass-Through(USB) mode	USB , PM
1	1	pass-through(USB) with CDP Emulation	USB , CM

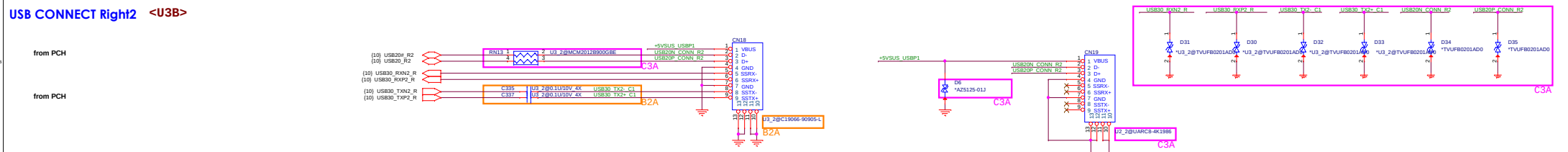
SW2	SW3	14644	
CB1	CB0	Status	
0	0	2A Auto mode for Apple device	Charger , AM2
1	**0**	Force dedicated charger mode	Charger , FM
0	**1**	Pass-Through(USB) mode	USB , PM
1	1	pass-through(USB) with CDP Emulation	USB , CM

2013 Shark bay / Kabini

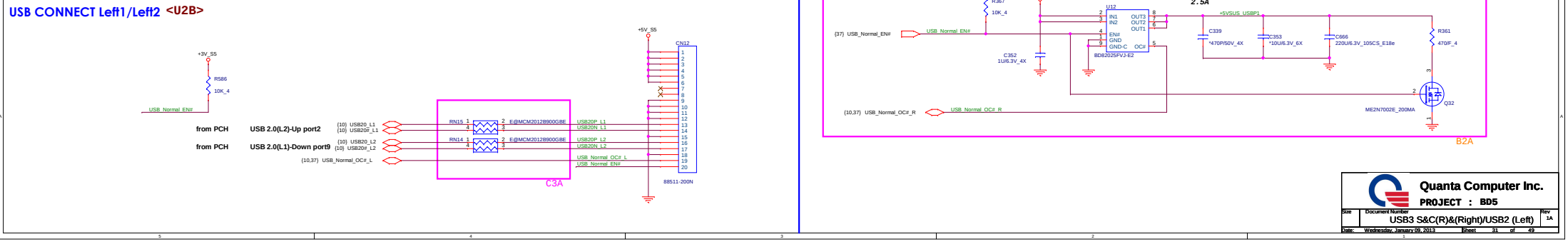
SW2	SW3	14641	
CB1	CB0	Status	
0	0	2A Auto mode for Apple device	Charger , AM2
1	**0**	Force 1A for Apple device	Charger , AP1
0	**1**	Pass-Through(USB) mode	USB , PM
1	1	pass-through(USB) with CDP Emulation	USB , CM

SW2	SW3	14642	
CB1	CB0	Status	
X	0	2A Auto mode for Apple device	Charger , AM2
0	**1**	Pass-Through(USB) mode	USB , PM
1	1	pass-through(USB) with CDP Emulation	USB , CM

USB CONNECT Right2 <U3B>



USB CONNECT Left1/Left2 <U2B>



Quanta Computer Inc.

PROJECT : BD5

Size	Document Number	Rev
	USB3 S&C(R)&(Right)/USB2 (Left)	1A

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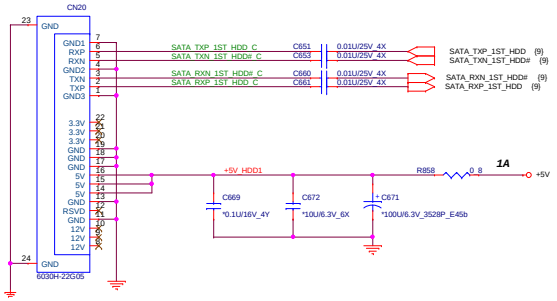
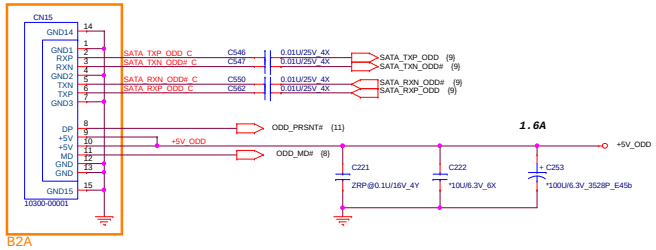
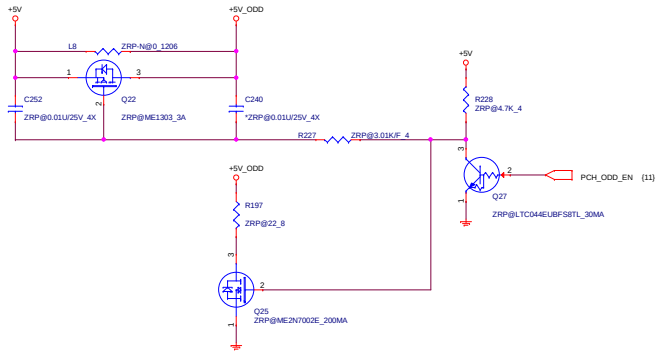
SATA HDD <HDD>



SATA ODD <ODD>

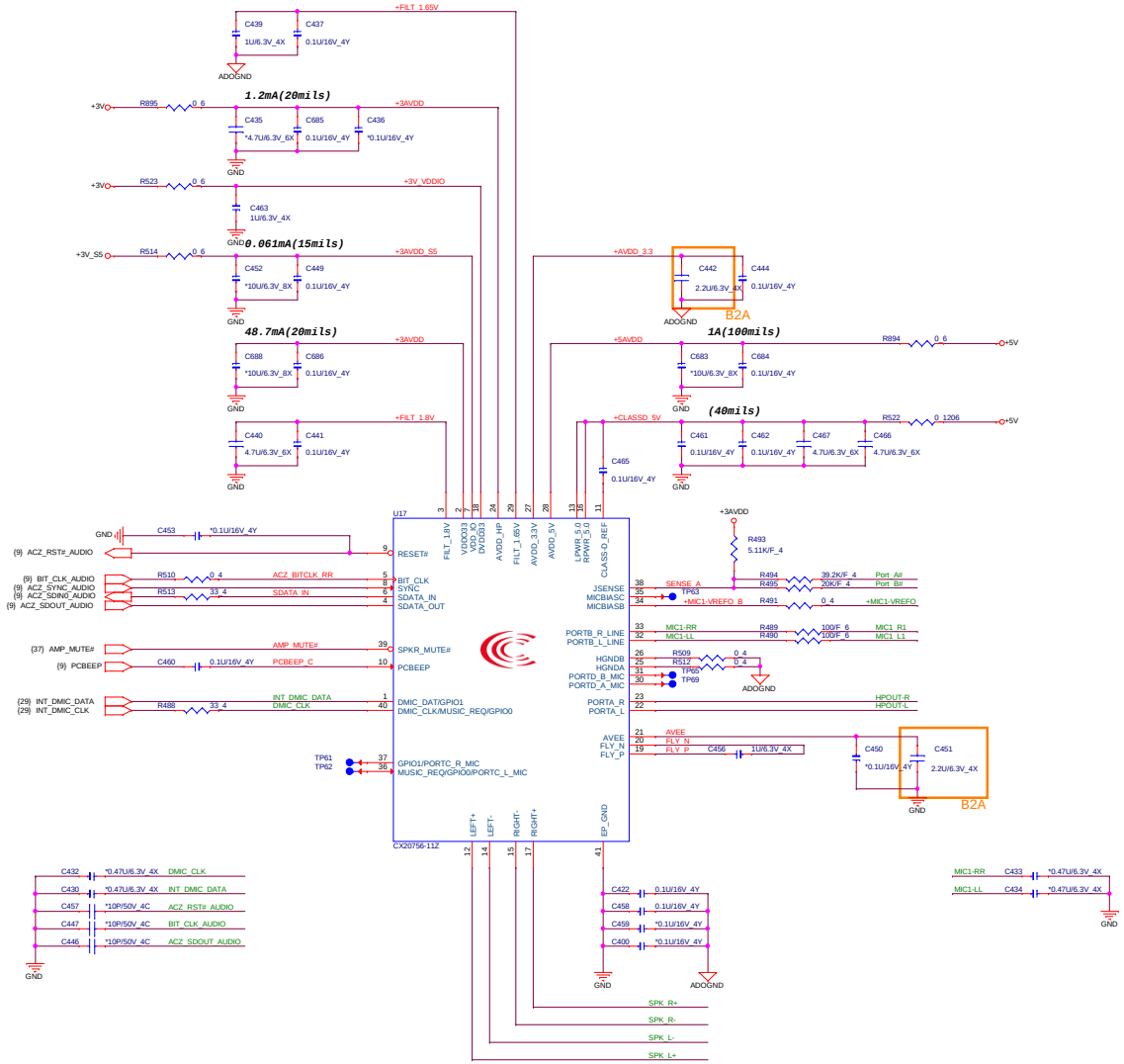


ODD Zero power . (Only for Intel) <OZP>

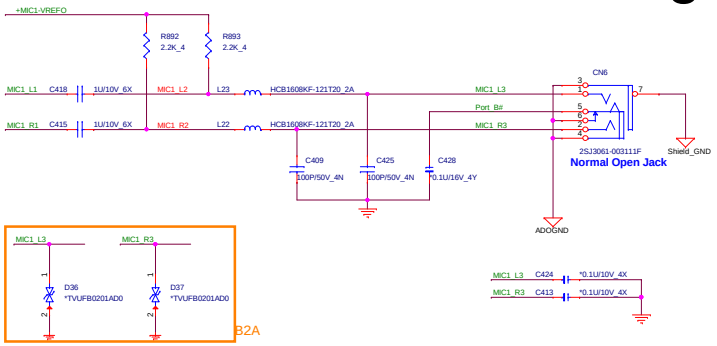


Quanta Computer Inc.		
PROJECT : BD5		
Size	Document Number: HDD/ODD	Rev: 1A
Date: Thursday, December 20, 2012	Sheet 33 of 49	

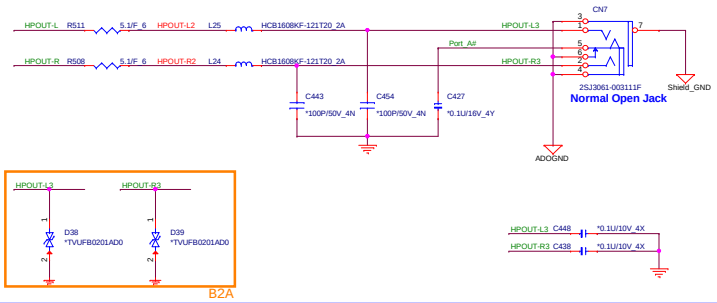
Codec (CX20756-11Z) <ADO>



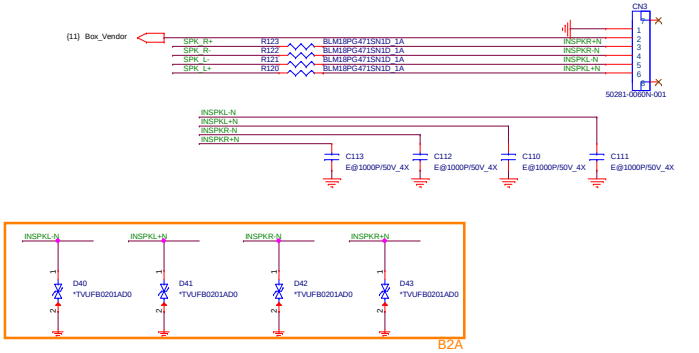
External MIC <ADO>



Headphone <ADO>



Internal Speaker <ADO>



Quanta Computer Inc.

PROJECT : BD5

Size	Document Number	Rev
	Audio Codec (CX20671)	A1A

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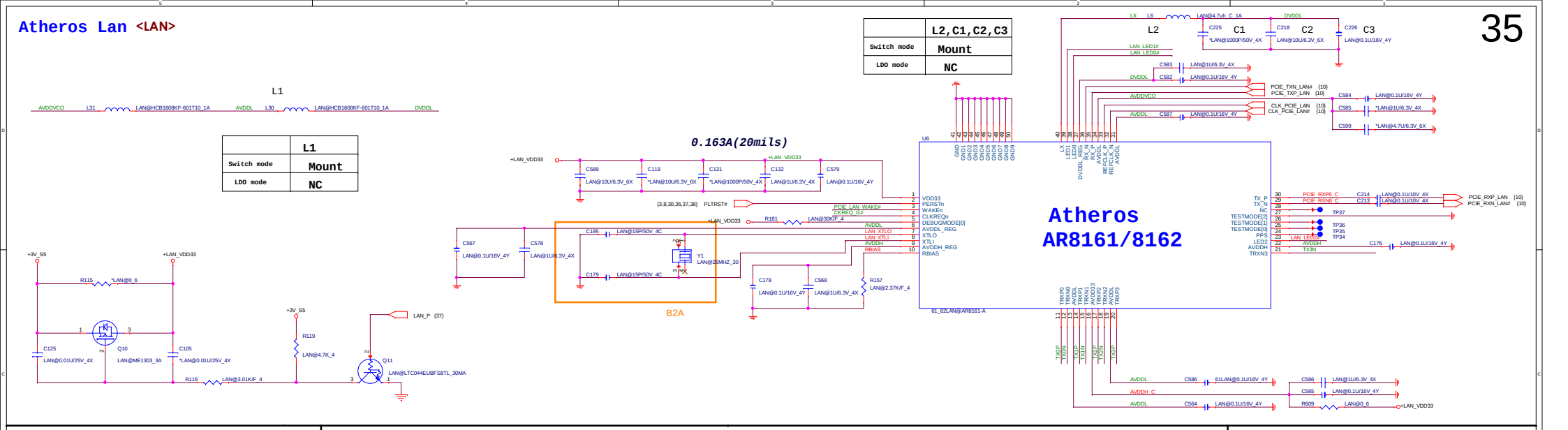
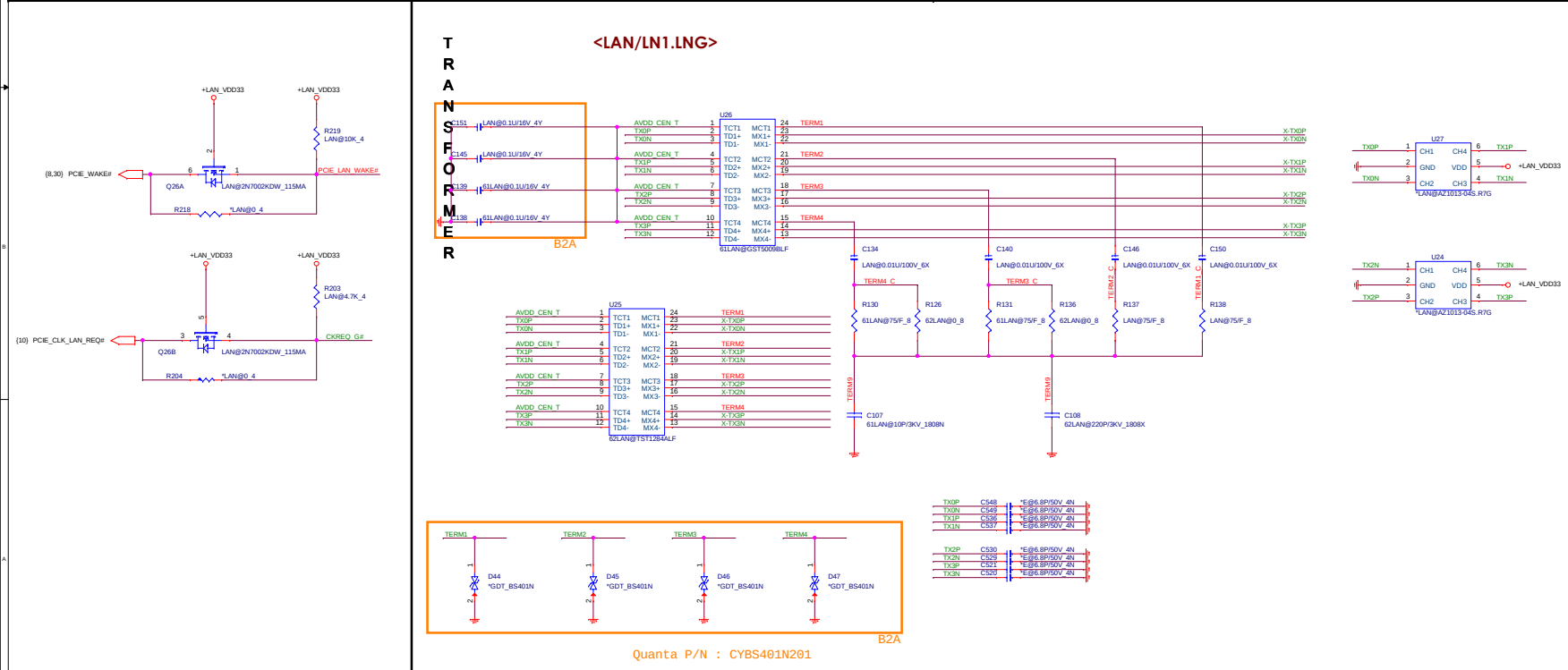
Atheros Lan <LAN>

	L2,C1,C2,C3
Switch mode	Mount
LDO mode	NC

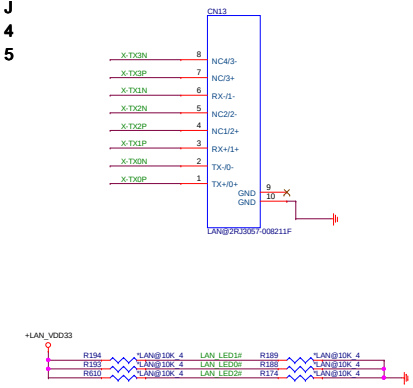
	L1
Switch mode	Mount
LDO mode	NC



TRANSFORMER <LAN/LN1.LNG>



RJ45 <LAN>



LED0 = LAN_ACTLED	1	High core voltage(default=1)
	0	Low core voltage
LED1 = LAN_LINKLED#	1	Switch mode regulator (SWR) select
	0	Linear regulator (LDO) select
LED2	1	25 MHz external clock input
	0	48 MHz external clock input

Quanta Computer Inc.

PROJECT : BD5

Size	Document Number	Rev
	Atheros LAN (AR8161B/62B)	A1A

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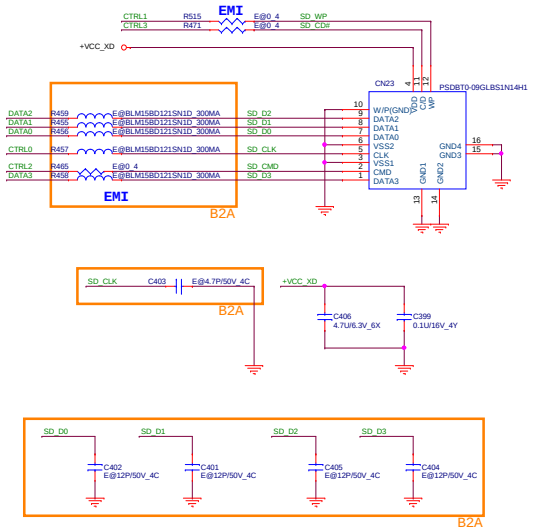
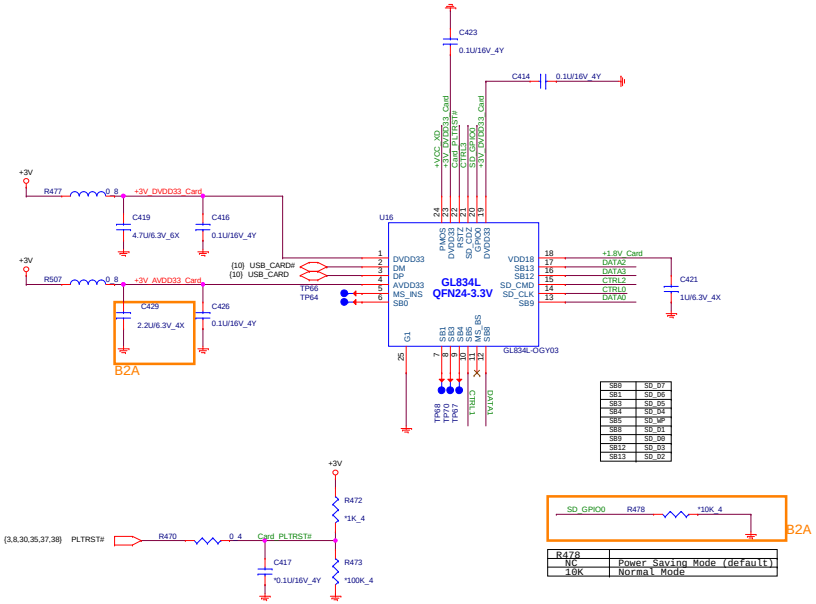
2 IN 1 Card Reader <MMC>



Card Reader (GL834L) <MMC>



SB6	SD_D7
SB1	SD_D6
SB3	SD_D5
SB4	SD_D4
SB5	SD_WP
SB8	SD_D1
SB9	SD_D0
SB12	SD_D3
SB13	SD_D2

R478	
NC	Power Saving Mode (default)
10K	Normal Mode

Quanta Computer Inc.

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Size	Document Number	Rev
	Card Reader(GL834L)	A1A

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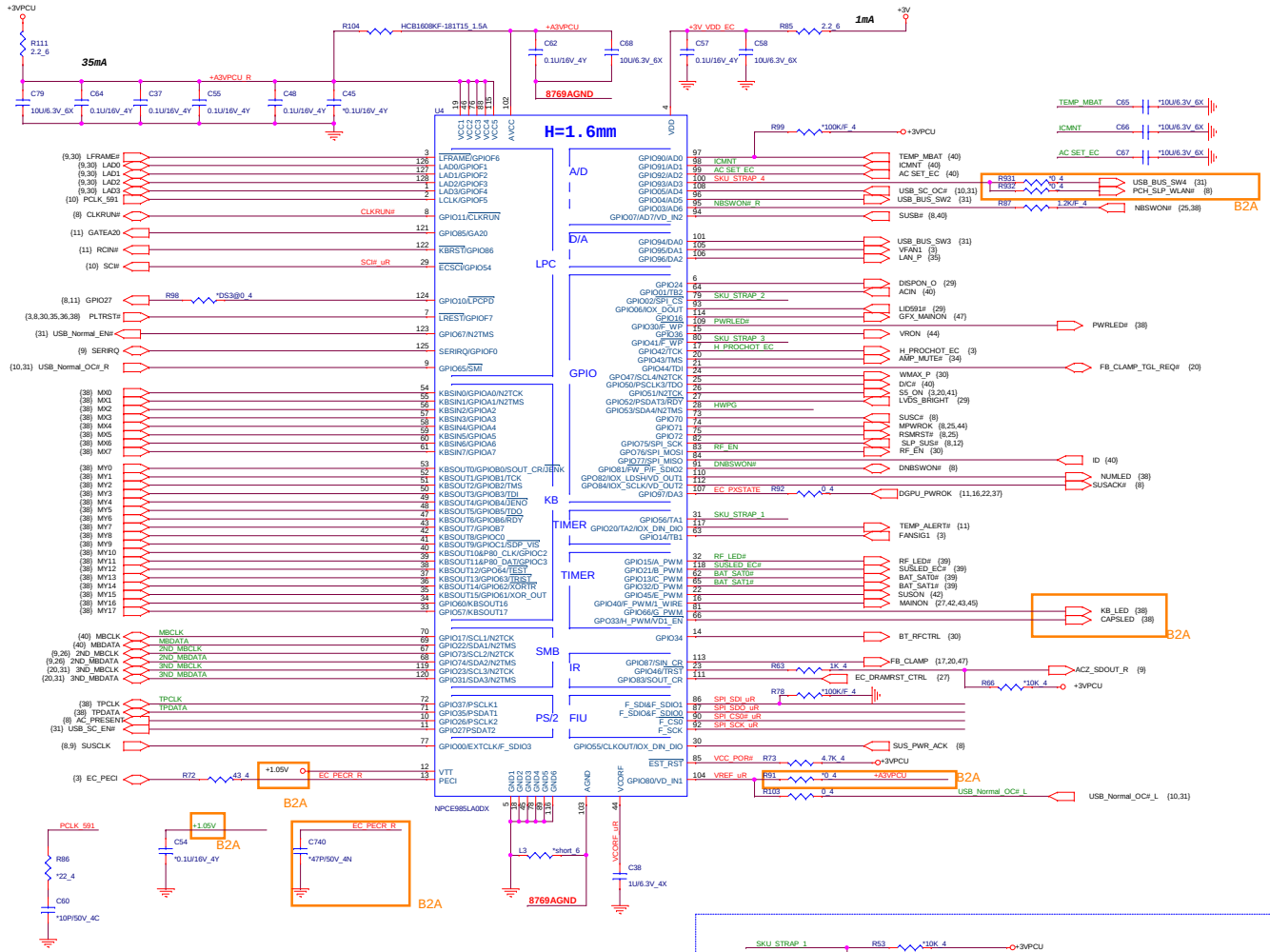
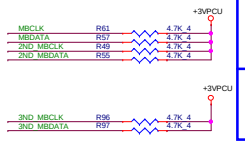
EC <KBC>

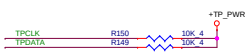


SM BUS PU/Address <KBC>

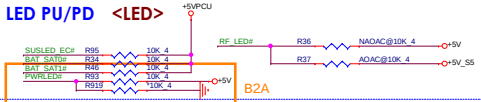


SMBUS	Devices	Address
1	Battery(A)	
2	PCH(S5)	
	G-sensor(S0)	
	IDROM(A)	
3	VGA Thermal(S0)	
	CEC(A)	

TP <KBC>



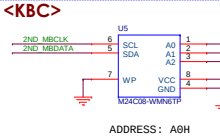
LED PU/PD <LED>



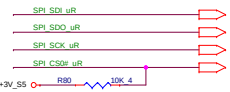
Strap(795) <KBC>

INTERNAL KEYBOARD STRIP SET <KBC>

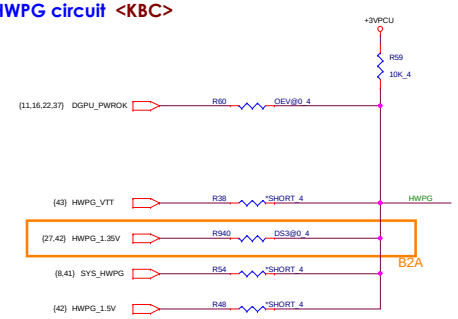
ID EEPROM <KBC>



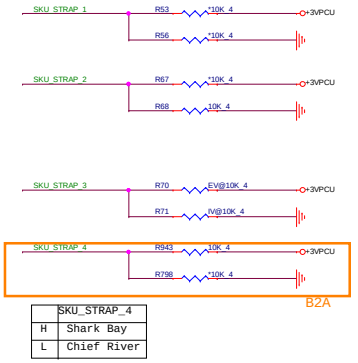
SPI FLASH <KBC>



HWPG circuit <KBC>



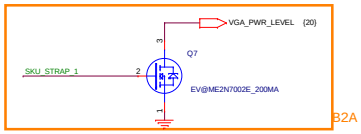
Power Button <KBC>



	SKU_STRAP_4
H	Shark Bay
L	Chief River

Capetown@/Aswan@ EV@ / IV@

MS Strap	SKU_STRAP_2	SKU_STRAP_3
14" Capetown UMA	1	0
14" Capetown DIS	1	1
17" Aswan UMA	0	0
17" Aswan DIS	0	1



Quanta Computer Inc.

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	EC-NPCE795L	1A

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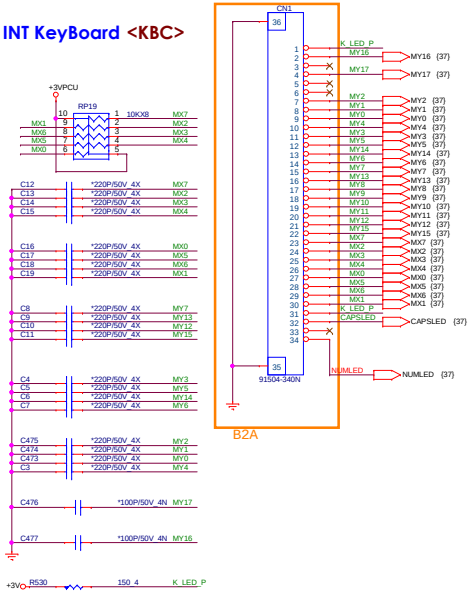
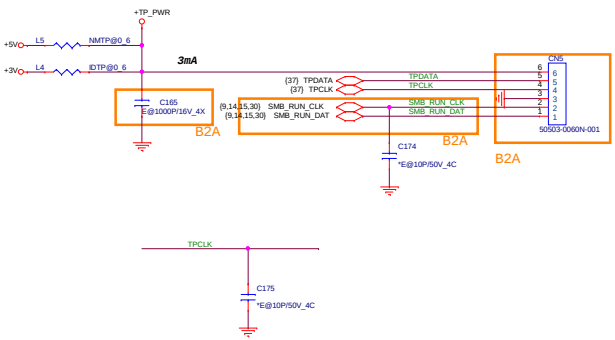
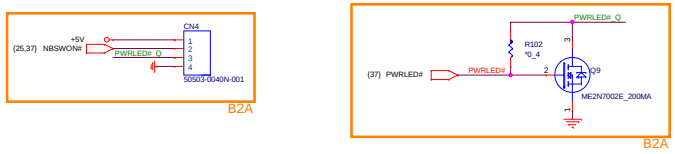
INT KeyBoard <KBC>



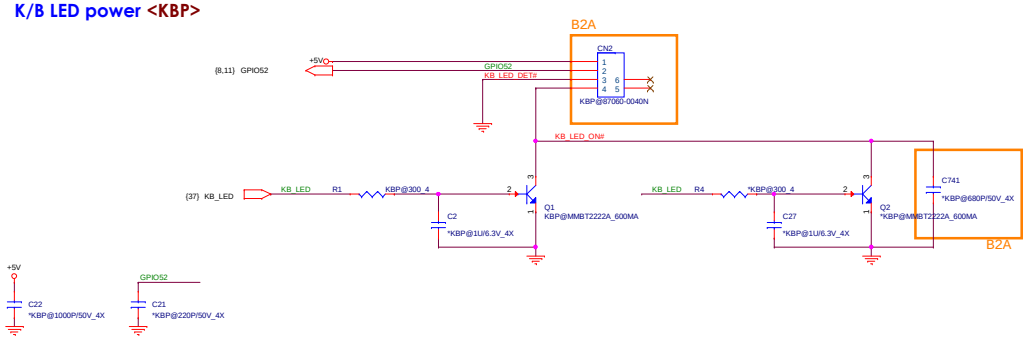
TP board <TPD>



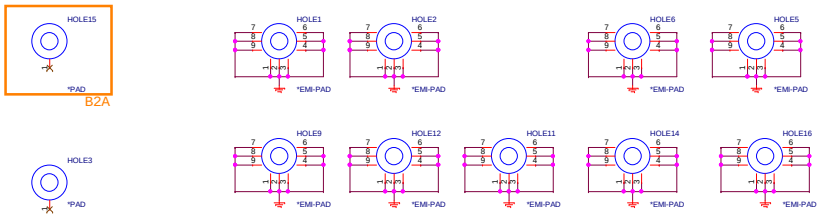
Power board w LED <PSW>



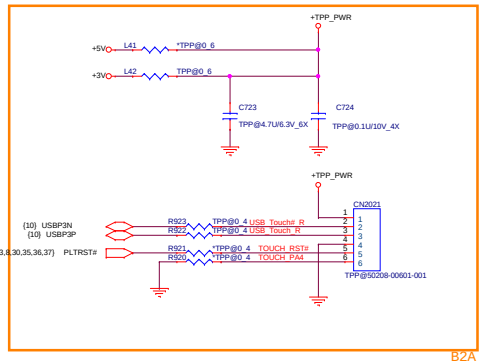
K/B LED power <KBP>



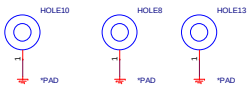
HOLE



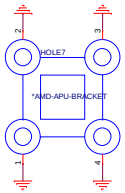
TOUCH PANEL <TPP>



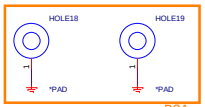
VGA HOLE



CPU HOLE



MINI Card NUT



Quanta Computer Inc.

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	KB/TP/PB/HOLE	1A

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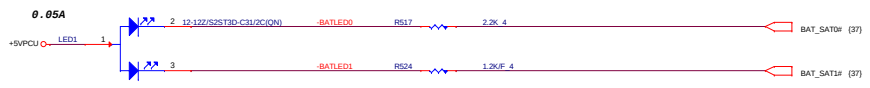
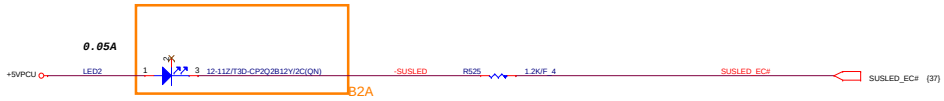
LED-Battery <LED><W+A>

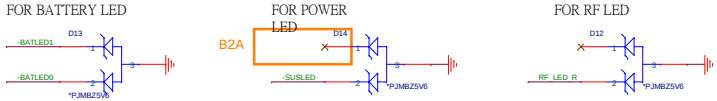


LED-Power <LED><W+A>

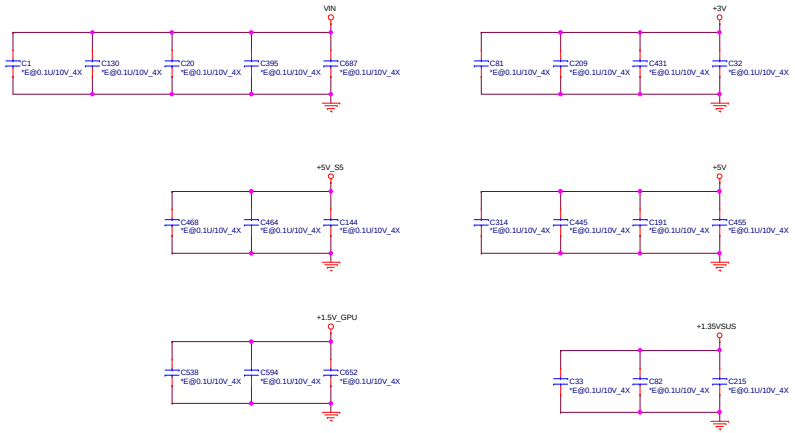


LED-WiFi <LED>

ESD Protect <EMC>



EMI <EMC>



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Size	Document Number: LED/EMI	Rev: 1A
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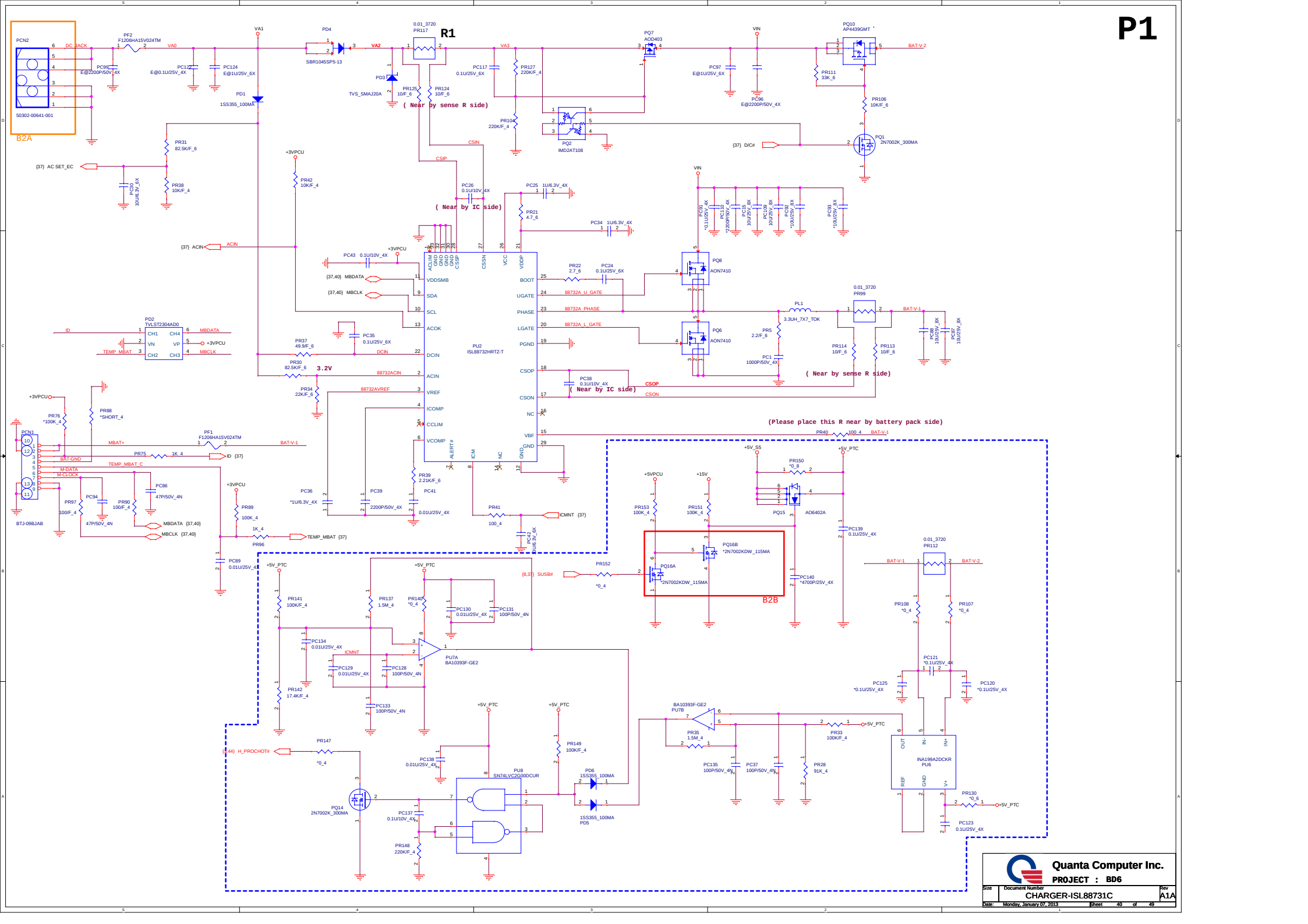

Quanta Computer Inc.

PROJECT : BD6

Size	Document Number	Rev
	CHARGER-ISL88731C	A1A

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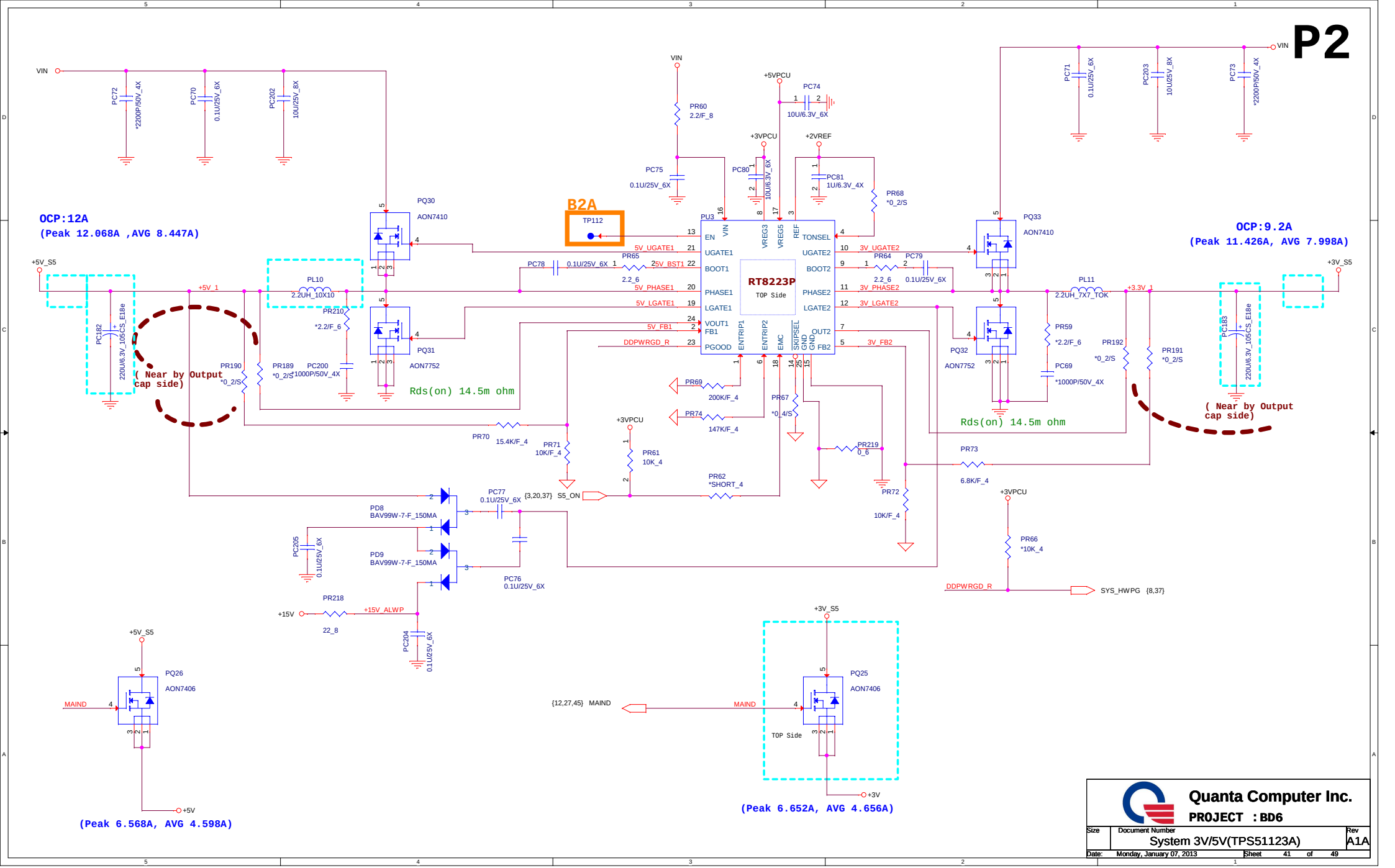
P2
OCP:12A
(Peak 12.068A ,AVG 8.447A)
OCP:9.2A
(Peak 11.426A, AVG 7.998A)
B2A
TP112
RT8223P
TOP Side
PU3
PQ30
AON7410
PQ31
AON7752
PQ33
AON7410
PQ32
AON7752
Rds(on) 14.5m ohm
Rds(on) 14.5m ohm
(Near by Output cap side)
(Near by Output cap side)
PQ26
AON7406
(Peak 6.568A, AVG 4.598A)
PQ25
AON7406
(Peak 6.652A, AVG 4.656A)
PD8
BAV99W-7-F_150MA
PD9
BAV99W-7-F_150MA
{3,20,37} S5_ON
{12,27,45} MAIND
SYS_HWPG {8,37}
DDPWRGD_R
+15V_ALWP
VIN
+5V_S5
+3V_S5
+5V_1
+3.3V_1
+5VPCU
+3VPCU
+2VREF
+15V
+5V
+3V
Quanta Computer Inc.
PROJECT : BD6
Size
Document Number
System 3V/5V(TPS51123A)
Rev
A1A
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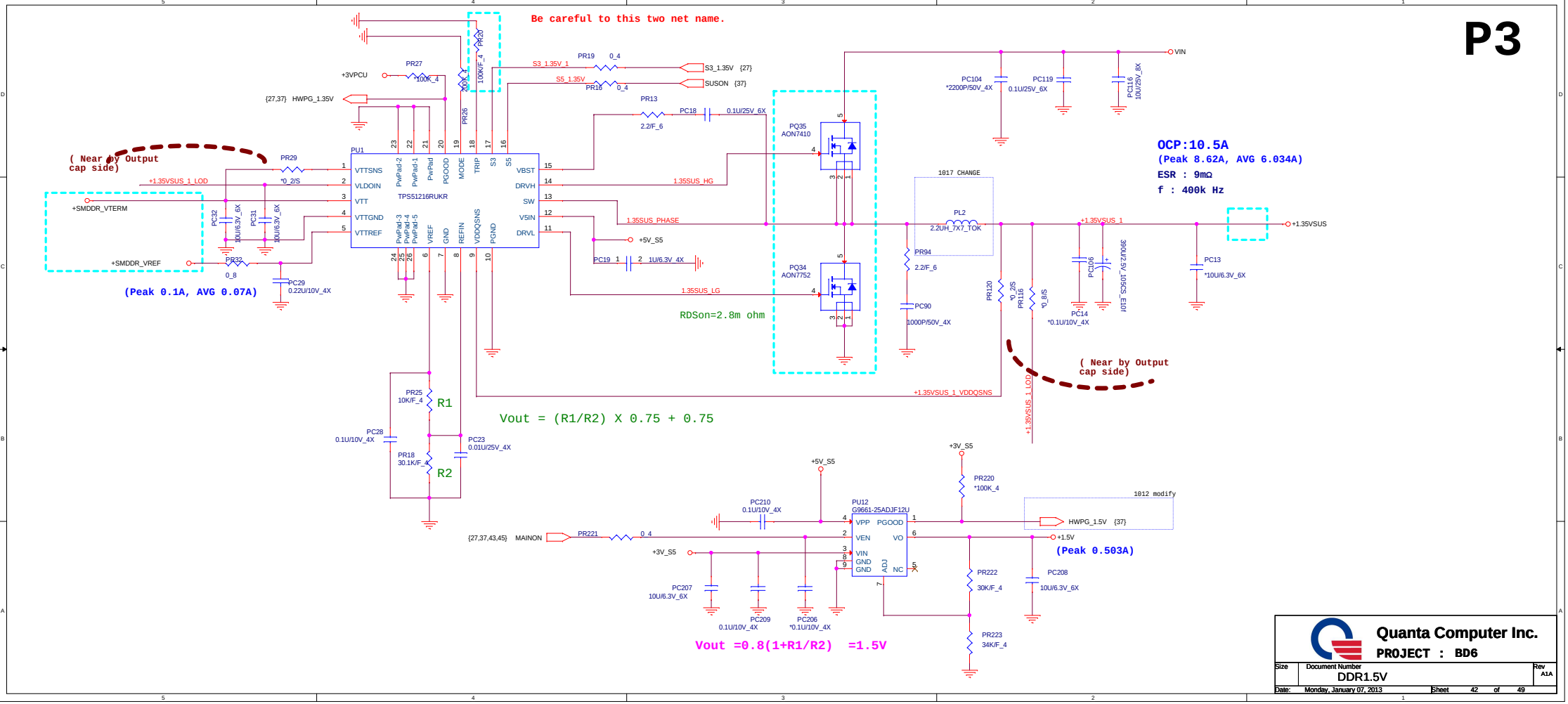
P3
Be careful to this two net name.
PU1
TPS51216RUKR
VTTSNS
VLDOIN
VTT
VTTGND
VTTREF
PwPad-2
PwPad-1
PwPad
PGOOD
MODE
TRIP
S3
S5
VBST
DRVH
SW
V5IN
DRVL
PwPad-3
PwPad-4
PwPad-5
VREF
GND
REFIN
VDDQSNS
PGND
PR27
*100K_4
+3VPCU
{27,37} HWPG_1.35V
PR20
100K/F_4
PR26
200K_1
S3_1.35V_1
S5_1.35V
PR19
0_4
PR18
0_4
S3_1.35V {27}
SUSON {37}
PR13
2.2/F_6
PC18
0.1U/25V_6X
PQ35
AON7410
PQ34
AON7752
1.35SUS_HG
1.35SUS_PHASE
1.35SUS_LG
+5V_S5
PC19
1U/6.3V_4X
RDSon=2.8m ohm
VIN
PC104
*2200P/50V_4X
PC119
0.1U/25V_6X
PC116
10U/25V_8X
OCP:10.5A
(Peak 8.62A, AVG 6.034A)
ESR : 9mΩ
f : 400k Hz
1017 CHANGE
PL2
2.2UH_7X7_TOK
+1.35VSUS_1
+1.35VSUS
PR94
2.2/F_6
PC90
1000P/50V_4X
PR120
*0_2/S
PR116
*0_8/S
PC106
390U/2.5V_10SCS_10E3
PC14
*0.1U/10V_4X
PC13
*10U/6.3V_6X
(Near by Output cap side)
+1.35VSUS_1_VDDQSNS
+1.35VSUS_1_LOD
(Near by Output cap side)
PR29
*0_2/S
+1.35VSUS_1_LOD
+SMDDR_VTERM
PC32
10U/6.3V_6X
PC31
10U/6.3V_6X
+SMDDR_VREF
PR32
0_8
PC29
0.22U/10V_4X
(Peak 0.1A, AVG 0.07A)
PR25
10K/F_4
R1
PC28
0.1U/10V_4X
PR18
30.1K/F_4
R2
PC23
0.01U/25V_4X
Vout = (R1/R2) X 0.75 + 0.75
+3V_S5
PR220
*100K_4
1012 modify
HWPG_1.5V {37}
PC210
0.1U/10V_4X
PU12
G9661-25ADJF12U
VPP
PGOOD
VEN
VO
VIN
GND
GND
ADJ
NC
{27,37,43,45} MAINON
PR221
0_4
+1.5V
(Peak 0.503A)
PR222
30K/F_4
PC208
10U/6.3V_6X
PC207
10U/6.3V_6X
PC209
0.1U/10V_4X
PC206
*0.1U/10V_4X
PR223
34K/F_4
Vout =0.8(1+R1/R2) =1.5V
Quanta Computer Inc.
PROJECT : BD6
Size
Document Number
DDR1.5V
Rev
A1A
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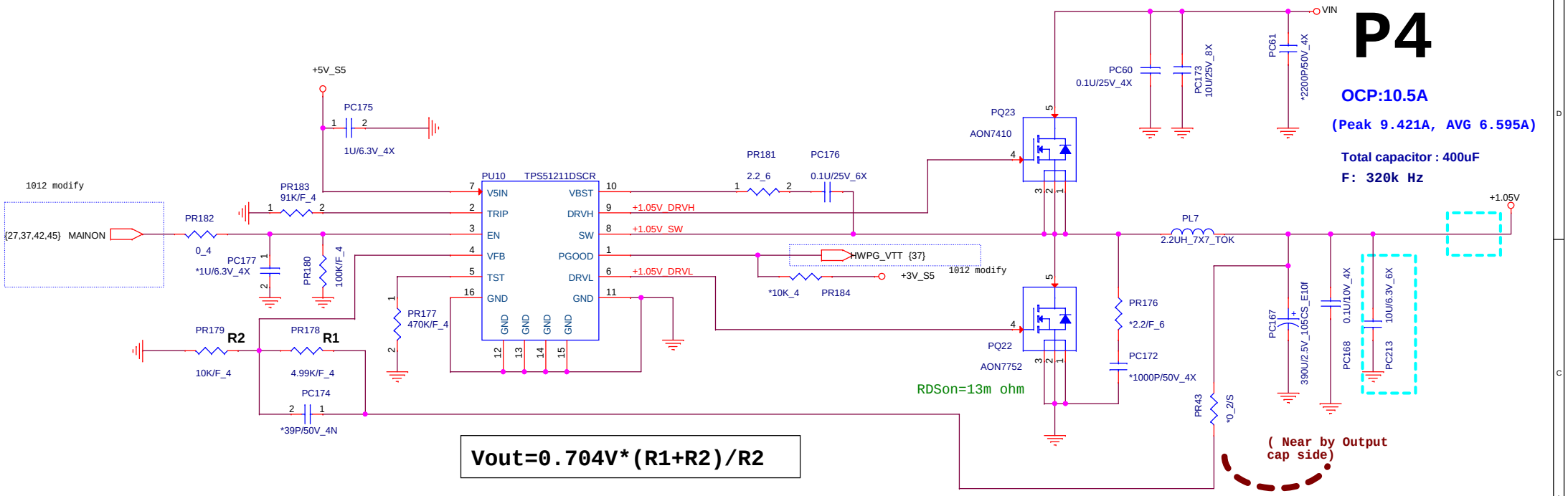

Quanta Computer Inc.

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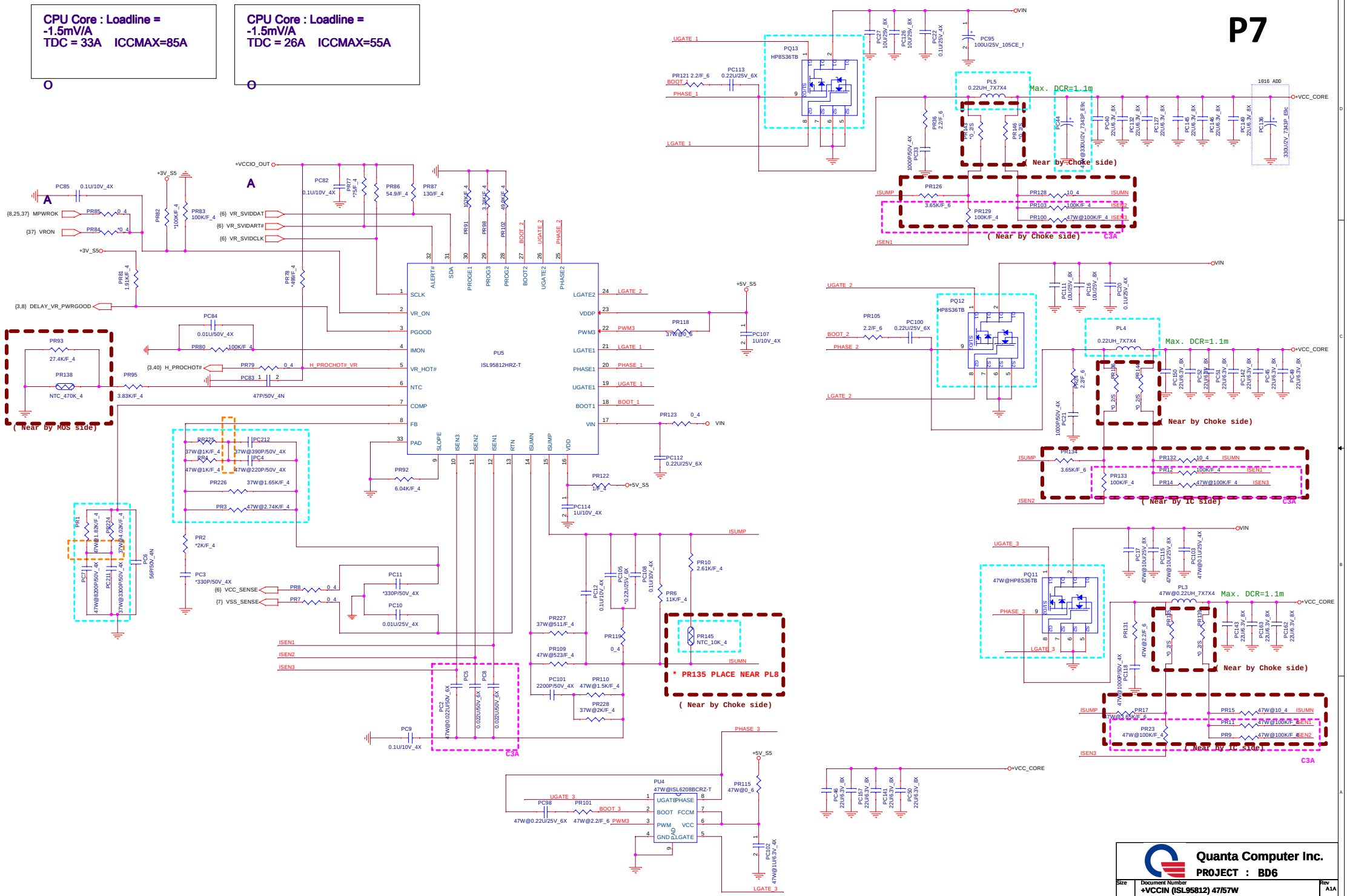
Size	Document Number	Rev
	+1.05V_A(TPS51211DSCR)	A1A

Date: Monday, January 07, 2013 Sheet 43 of 49

CPU Core : Loadline = -1.5mV/A
TDC = 33A ICCMAX=85A

CPU Core : Loadline = -1.5mV/A
TDC = 26A ICCMAX=55A

P7



Quanta Computer Inc.
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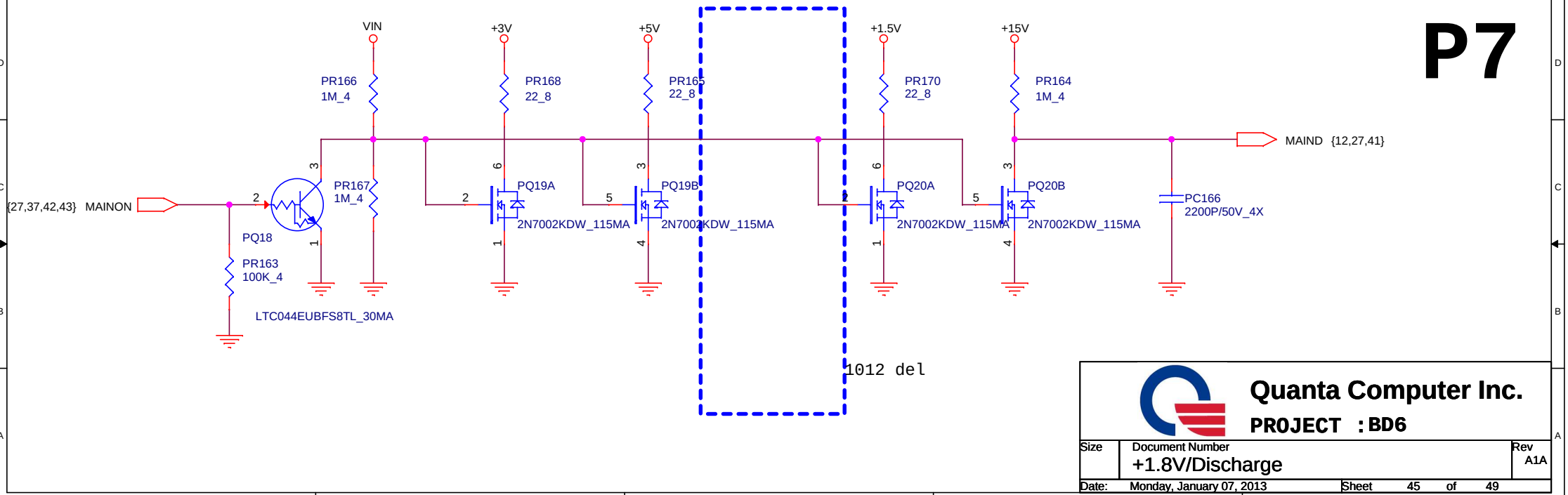
Size	Document Number	Rev
	+VCCIN (ISL95812) 47/57W	A1A

Date: Monday, January 07, 2013 Sheet 44 of 49

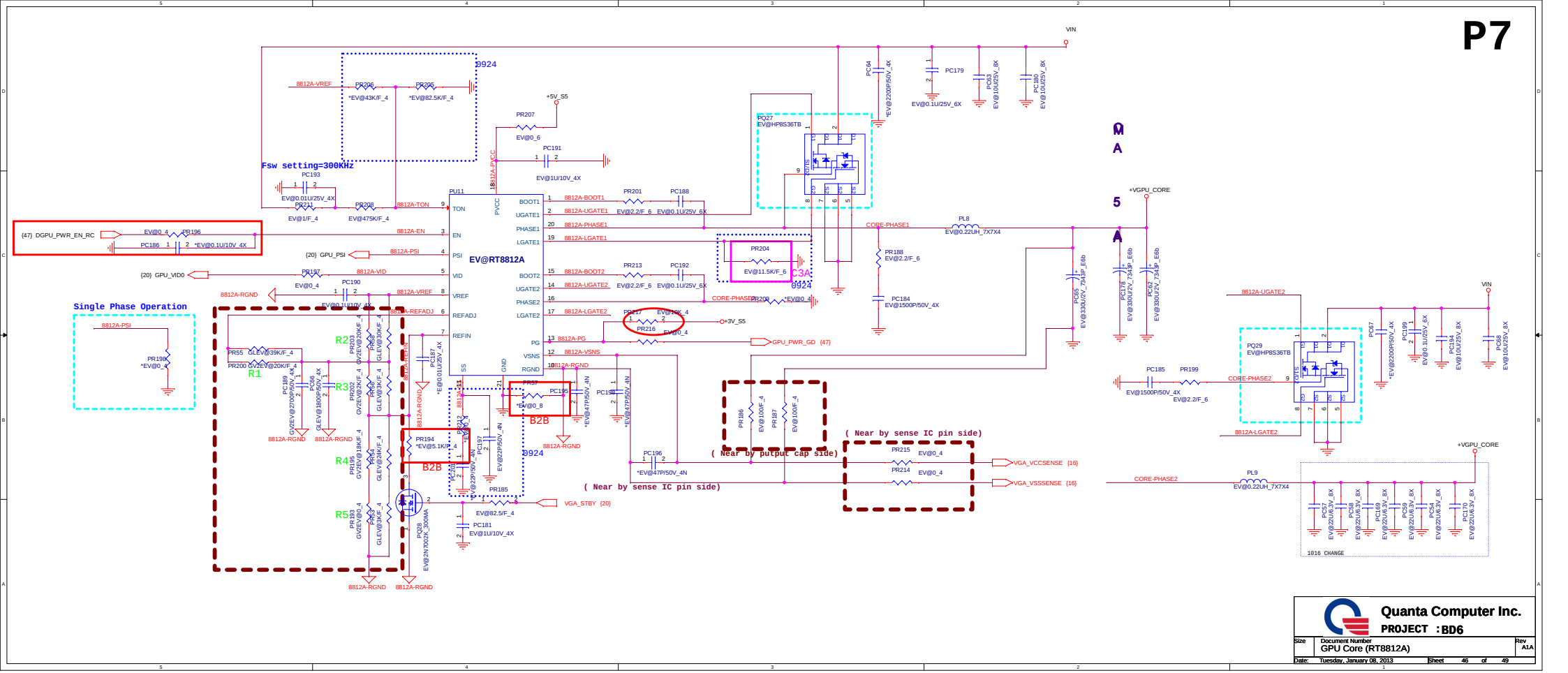


Quanta Computer Inc.

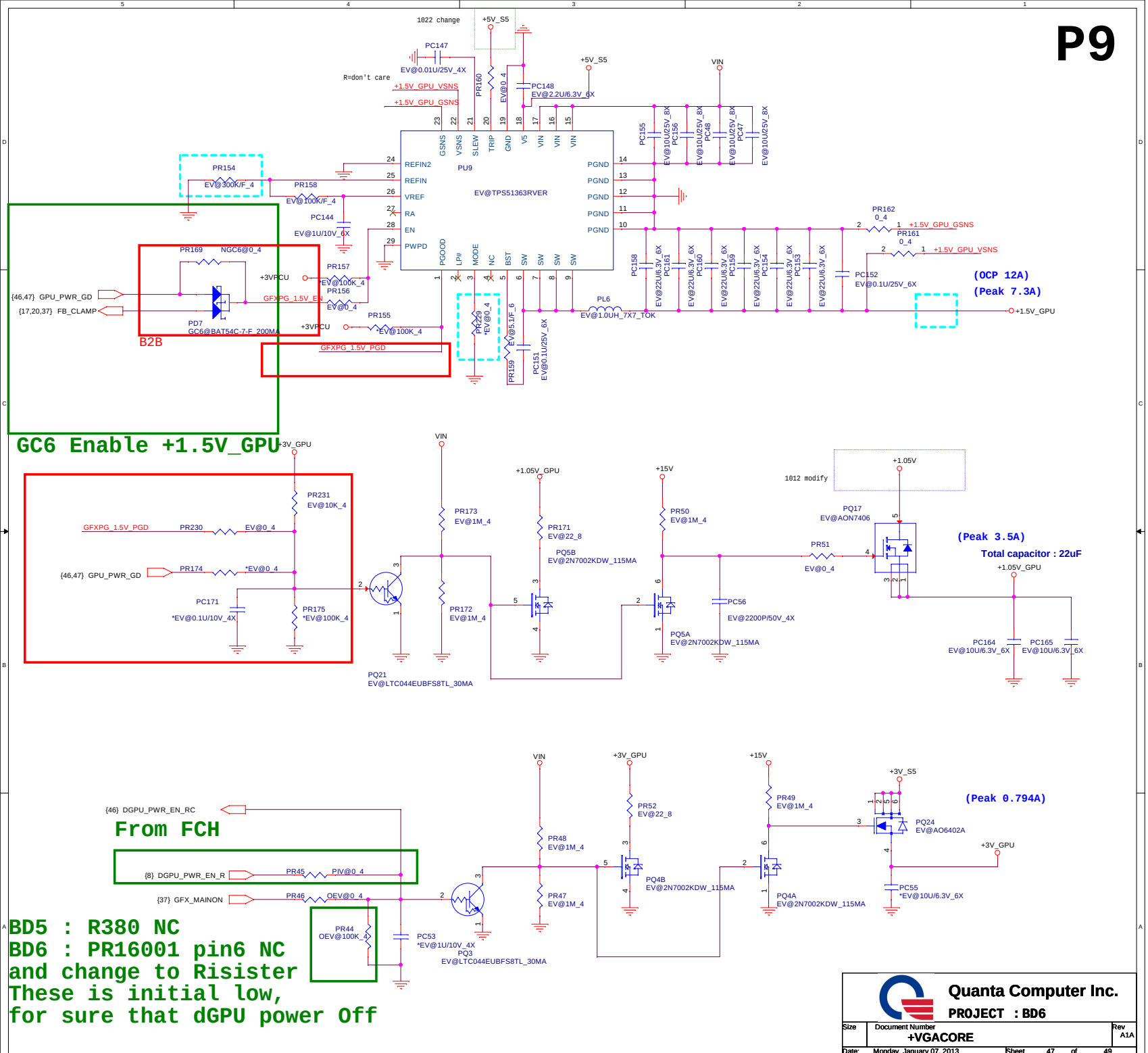
PROJECT : BD6

Size	Document Number	Rev
	+1.8V/Discharge	A1A

Date: Monday, January 07, 2013 Sheet 45 of 49



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.


P9
1022 change
+5V_S5
PC147
EV@0.01U/25V_4X
R=don't care
+1.5V_GPU_VSNS
+1.5V_GPU_GSNS
PR160
EV@0_4
PC148
EV@2.2U/6.3V_6X
VIN
PU9
EV@TPS51363RVER
GSNS
VSNS
SLEW
TRIP
GND
V5
VIN
PGND
REFIN2
REFIN
VREF
RA
EN
PWPD
PGOOD
LP#
MODE
NC
BST
SW
PR154
EV@300K/F_4
PR158
EV@100K/F_4
PC144
EV@1U/10V_6X
PR169
NGC6@0_4
PR157
*EV@100K_4
PR156
EV@0_4
PR155
*EV@100K_4
+3VPCU
{46,47} GPU_PWR_GD
{17,20,37} FB_CLAMP
GFXPG_1.5V_EN
PD7
GC6@BAT54C-7-F_200MA
B2B
GFXPG_1.5V_PGD
PR229
*EV@0_4
PR159
EV@5.1/F_6
PC151
EV@0.1U/25V_6X
PL6
EV@1.0UH_7X7_TOK
PC155
EV@10U/25V_8X
PC156
PC48
PC47
PC158
EV@22U/6.3V_6X
PC161
PC160
PC159
PC154
PC153
PR162
0_4
PR161
0_4
PC152
EV@0.1U/25V_6X
+1.5V_GPU
(OCP 12A)
(Peak 7.3A)
GC6 Enable +1.5V_GPU
+3V_GPU
PR231
EV@10K_4
PR230
EV@0_4
PR174
*EV@0_4
PC171
*EV@0.1U/10V_4X
PR175
*EV@100K_4
PR173
EV@1M_4
PR172
EV@1M_4
PQ21
EV@LTC044EUBFS8TL_30MA
+1.05V_GPU
PR171
EV@22_8
PQ5B
EV@2N7002KDW_115MA
+15V
PR50
EV@1M_4
PQ5A
EV@2N7002KDW_115MA
PC56
EV@2200P/50V_4X
1012 modify
+1.05V
PQ17
EV@AON7406
PR51
EV@0_4
(Peak 3.5A)
Total capacitor : 22uF
PC164
EV@10U/6.3V_6X
PC165
EV@10U/6.3V_6X
{46} DGPU_PWR_EN_RC
From FCH
{8} DGPU_PWR_EN_R
PR45
PIV@0_4
{37} GFX_MAINON
PR46
OEV@0_4
PR44
OEV@100K_4
PC53
*EV@1U/10V_4X
PQ3
EV@LTC044EUBFS8TL_30MA
PR48
EV@1M_4
PR47
EV@1M_4
PR52
EV@22_8
PQ4B
EV@2N7002KDW_115MA
PR49
EV@1M_4
PQ4A
EV@2N7002KDW_115MA
+3V_S5
PQ24
EV@AO6402A
PC55
*EV@10U/6.3V_6X
(Peak 0.794A)
BD5 : R380 NC
BD6 : PR16001 pin6 NC
and change to Risister
These is initial low,
for sure that dGPU power Off
Quanta Computer Inc.
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Size
Document Number
+VGACORE
Rev
A1A
Date: Monday, January 07, 2013
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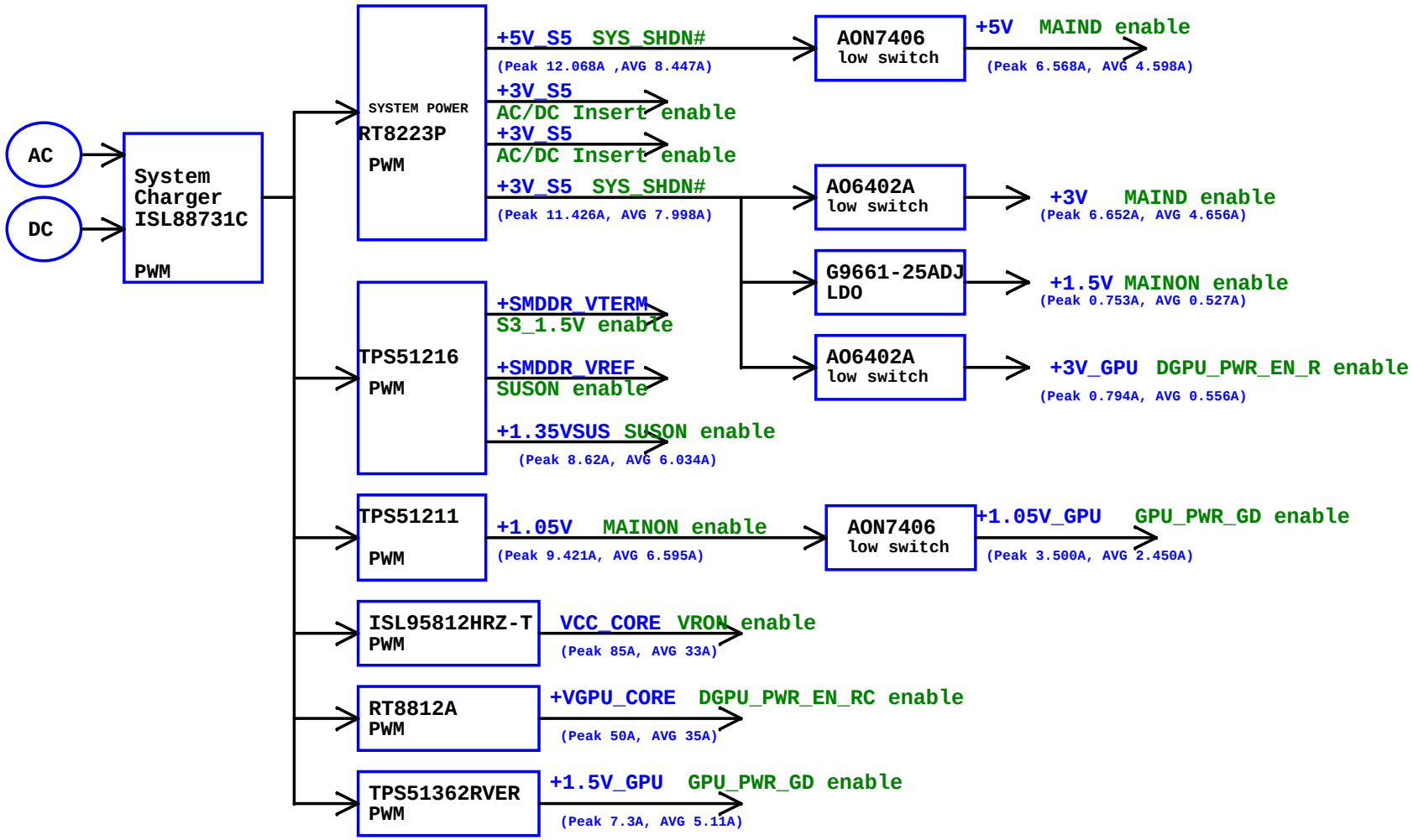

Quanta Computer Inc.

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Size	Document Number	Rev
	POWER TREE TABLE	1A

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Model	REV	CHANGE LIST
BD6 MB	A1A	First Release
	B2A	PAGE 3: Change C510,C508 size and stuff R926,add R148,R152
		PAGE 6: add C728,C729
		PAGE 7: add R929,R930,demount R927,R928,R82,R566,R81
		PAGE 8: modify R425,R412,R398,R397,R404,R405,R414,R146,R854,R862 value to DS3
		PAGE 9: change GPIO13 to BOARD_ID16,GPIO23 to BOARD_ID17,change R819,R816,R821,R824,R814,R818,R813,R823 value dor XDP
		PAGE 10: add USB port3 for Touch Panel function,add R897,R901,R364,R902,R903,R905,R898,R906,Q60,Q59 for DS3,change C667,C668 to 12PF
		PAGE 11: change R407,R408,R879,R880,R907,R349,R342,R343,R910,R911,R912,R913,R908,R909 for BOARD_ID select
		PAGE 12: change R338,R328 size,change C411,D11,R436,Q35 value and add R434,R435 for DS3
		PAGE 15: Change C188 size to 0402.
		PAGE 16: Change R201,R196,Q23,Q61,Q24 value
		PAGE 18: change C725,C726,C727 value
		PAGE 19: add R914 for XTAL,and change R291,R292 value
		PAGE 20: change R293,R728,R294,R915,R916 value
		PAGE 21: add R917 for co-lay
		PAGE 22: change C279,C604 value
		PAGE 26: add U33,R938,C738
		PAGE 27: add R939,C739,U34 for DS3
		PAGE 28: change R918,F3,U30,D19,C628,C629,C630,C633,C634,C635,C636,C641 value for HDMI
		PAGE 29: change R937,R64,R9,C26,C28,C29,MR1,F1,R24,R539,R25,R536,R22 value
		PAGE 30: change R58,R942,Q41,R533 value for AOAC
		PAGE 31: add D6,D22,D23,D24,D25,D28,D29,D31,D30,D32,D33,D34,D35 for ESD,change C339,C353,R361,R367,U12,C666,C335,C337,Q32 value
		PAGE 33: change CN15 value
		PAGE 34: add D36,D37,D38,D39,D40,D41,D42,D43 for ESD
		PAGE 35: change C195,C179,C151,C145,C139,C138 value,add D44,D45,D46,D47 for ESD
		PAGE 36: change R459,R455,R456,R457,R465,R458,R478,C403,C402,C401,C405,C404 value
		PAGE 37: change R91,Q7 value,add R943,R798 for STRAP select
		PAGE 38: change CN1,CN2,CN5,CN4,R102,Q9 value and change C165 value for EMI,and add L41,L42,C723,C724,CN2021,R920,R921,R922,R923 for Touch PAD Panel function
		PAGE 39: change LED2 symbol
	B2B	PAGE 20: change R656 value
		PAGE 22: change D4 value
	C3A	PAGE 14: change C192 size to 0402,chaneg C734,C735,R933,R934 value for DS3
		PAGE 28: change Q55,R754,R753,R721,R711,R694,R699,R678,R683,R744,R733,R652 value for HDMI 4K2K
		PAGE 31: change RN12,RN13,RN14,RN15 pin define
		PAGE 34: change C490,C501 size to 0402
		PAGE 36: change C476 size to 0402

MODEL BD6

PAGE	FROM	To
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DOC NO. 204	PROJECT MODEL :	BD6	APPROVED BY:	Kent Su	DATE:	2012/12/14
	PART NUMBER:		DRAWING BY:	Kent Su	REVISON:	

Quanta Computer Inc.

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