ZY5/ZY5D SYSTEM BLOCK DIAGRAM

CPU CORE ISL6265A PAGE 26

NB CORE +1.1V PAGE 27

NB RUN +1.1V PAGE 28

DDR II SMDDR_VTERM 1.8VSUS(TPS51116REGR) PAGE 29

SYSTEM POWER ISL6237 PAGE 25

SYSTEM CHARGER (ISL6251A) PAGE 24

DISCHARGER / +1.1V_S5, +1.2V,+2.5V PAGE 30

INT or EV selector Resistor

DDRII-SODIMM1 PAGE 6

DDRII-SODIMM2 PAGE 6

DDRII 667/800 MHZ

AMD Griffin Lion Sabie

S1G2 Processor

638P (uPGA)/35W PAGE 2,3,4,5

CPU THERMAL SENSOR PAGE 4

CPU Fan PAGE 17

HT3 LINK

ZY5D NO USED

MXM Connector PAGE 14

PCI-Express 16X

NORTH BRIDGE & SOUTH BRIDGE

MCP77M

27mm X 27mm, 836pin BGA

PAGE 7,8,9,10,11,12,13

14.318MHz

LVDS

CRT

ZY5D NO USED HDMI

LVDS PAGE 15

SN74CBTLV3257PWR Switch PAGE 15

TS3DV520RHUR Switch PAGE 15

CRT PAGE 15

CABLE DOCK PAGE 22

HDMI CONN. PAGE 15

CRT

DVI-D

HDMI

SATA - HDD PAGE 17

SATA - HDD PAGE 17

ODD(PATA) PAGE 17

SATA0

SATA1

SATA2

PCI-E

X1 Mini PCI-E Card (Wireless LAN) PAGE 16

X1 Mini PCI-E Card (TV TUNER) USB2.0 x1 PAGE 16

X1 Express Card (NEW CARD) USB2.0 Ports x2 PAGE 16

X1 Card reader JMicron JMB385-LGEZ0A PAGE 20

X1 LAN BroadCom PCIE-LAN BCM5787/5764 (10/100/GigaLAN) PAGE 18

RJ45/RJ11 PAGE 15

CABLE DOCK LAN/VGA/DVI/USB/AUDIO PAGE 22

USB2.0

USB2.0 Ports x2 PAGE 16

Bluetooth x1 PAGE 16

CCD x1 PAGE 15

Fingrprinter x1 PAGE 16

CABLE DOCK USB x1 PAGE 22

PCI

Card Bus PCMCIA O2 Micro OZ601TN PAGE 23

HDA

Azalia AudioController RealTek ALC268/888 PAGE 19

MDC 1.5 PAGE 19

B TEST MODIFY

Audio Amplifier

Int MIC

Speaker

SPIDF/Phone Jack

Line in

MIC Jack

LPC

Keyboard PAGE 21

CIR PAGE 16

KBC (WPCE775CA0DG) PAGE 21

Touch Pad PAGE 17

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CABLE DOCK AUDIO PAGE 22

PCB STACK UP

LAYER 1 : TOP

LAYER 2 : SGND1

LAYER 3 : IN1

LAYER 4 : IN2

LAYER 5 : VCC

LAYER 6 : GND

Quanta Computer Inc.

PROJECT : ZY5D

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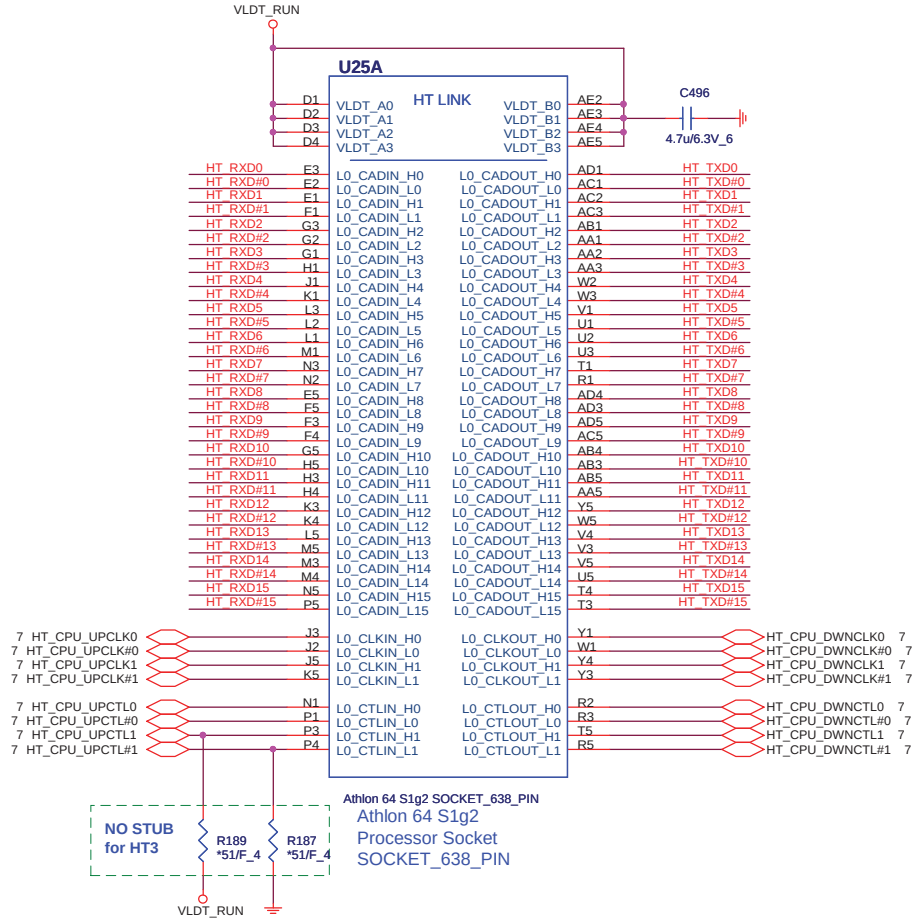
7 HT_RXD#[15..0] — HT_RXD#[15..0]
7 HT_RXD[15..0] — HT_RXD[15..0]
7 HT_TXD[15..0] — HT_TXD[15..0]
7 HT_TXD#[15..0] — HT_TXD#[15..0]

PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

REV:B Modify



HOLE10 *CPU_HOLE
HOLE9 *CPU_HOLE
HOLE19 *CPU_HOLE
HOLE20 *CPU_HOLE

HOLE36 *MINI_HOLE
HOLE37 *MINI_HOLE
HOLE27 *MINI_HOLE
HOLE28 *MINI_HOLE

HOLE8 *MXM_HOLE
HOLE17 *MXM_HOLE
HOLE7 *MXM_HOLE
HOLE16 *MXM_HOLE

HOLE11 *MDC_HOLE
HOLE13 *MDC_HOLE
HOLE6 *MXM1_HOLE
HOLE21 *MXM1_HOLE

PAD2 *EMIPAD
PAD3 *EMIPAD

HOLE3 *H-C295D118P2
HOLE4 *H-C295D118P2
HOLE1 *H-C295D118P2
HOLE23 *H-C295D118P2

HOLE2 *H-C295D118P2
HOLE5 *H-C295D118P2
HOLE25 *H-C295D118P2
HOLE32 *H-C295D118P2

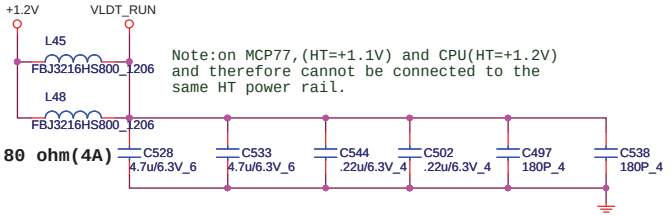
ADOGND

HOLE34 *H-C295D118P2
HOLE35 *H-C295D118P2
HOLE33 *H-C295D118P2
HOLE14 *H-C295D118P2

HOLE38 *FAN_HOLE
HOLE15 *NONP_HOLE1
HOLE24 *H-C295D118P2

HOLE18 *ODD1_HOLE
HOLE22 *ODD1_HOLE
HOLE26 *HDD1_HOLE
HOLE30 *HDD1_HOLE
HOLE29 *HDD2_HOLE
HOLE31 *HDD2_HOLE

MODIFY 10/17,ALEX



LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

Quanta Computer Inc.
PROJECT : ZY5D

Size	Document Number	Rev
	AMD Griffin HT I/F	3B
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Processor DDR2 Memory Interface

VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

PLACE THEM CLOSE TO CPU WITHIN 1"

U25B

MEM:CMD/CTRL/CLK

+SMDDR_VTERM

+1.8VSUS

R378 39.2/F_4

R379 39.2/F_4

R113 1K/F_4

R114 1K/F_4

C178 .1u/10V_4

C101 1000p_4

Athlon 64 S1g2 SOCKET_638_PIN

Athlon 64 S1g2
Processor Socket
SOCKET_638_PIN

U25C

MEM:DATA

To reverse SODIMM socket

To normal SODIMM socket

PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

C327 1.5p_NPO_4

C102 1.5p_NPO_4

C315 1.5p_NPO_4

C115 1.5p_NPO_4

C105 4.7u/6.3V_6

C322 4.7u/6.3V_6

C167 4.7u/6.3V_6

C106 4.7u/6.3V_6

C319 .22u/6.3V_4

C324 .22u/6.3V_4

C108 .22u/6.3V_4

C110 .22u/6.3V_4

C107 1000P_4

C109 1000P_4

C318 1000P_4

C323 1000P_4

C321 180P_4

C320 180P_4

C111 180P_4

C112 180P_4

Quanta Computer Inc.			
PROJECT : ZY5D			
Size	Document Number		Rev
	AMD Griffin DDRII MEMORY I/F		3B
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ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

CPU_VDDA_RUN

+2.5V — L51 BLM18PG330SN1D_6 — CPU_VDDA_RUN

C595 100u/6.3V_3528 | C588 4.7u/6.3V_6 | C275 .22u/6.3V_4 | C286 3300p/50V_4

If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 390- (±5%) pulldown to VSS.

+1.8VSUS

R367 390_4 — CPU_SID — CPU_SID 12

R370 390_4 — CPU_SIC — CPU_SIC 12

R388 *390_4

R387 *1K/F_4 — CPU_ALERT

390 Ohm

+1.8VSUS

R100 300_4 — R104 300_4

7 CPU_THERMTRIP# — CPU_THERMTRIP# — R99 0_4 — Q18 MMBT3904 — SYS_SHDN# 25,30

U25D

CPU_VDDA_RUN — F8 VDDA1, F9 VDDA2

CPU_CLKP — C326 3900P_4 — CPU_CLKIN_SC_P — A9 CLKIN_H

CPU_CLKN — C325 3900P_4 — CPU_CLKIN_SC_N — A8 CLKIN_L

Keep trace from resisor to CPU within 0.6"

keep trace from caps to CPU within 1.2"

7 CPU_CLKP — R218 169/F_6 — 7 CPU_CLKN

place them to CPU within 1.5"

CPU_HT_RESET# — B7 RESET_L

CPU_HT_PWRGD — A7 PWROK

CPU_HT_LDTSTOP# — F10 LDTSTOP_L

CPU_LDT_REQ# CPU — C6 LDTREQ_L

CPU_SIC — AF4 SIC

CPU_SID — AF5 SID

CPU_ALERT — AE6 ALERT_L

VLDT_RUN — R186 44.2/F_4 — R182 44.2/F_4 — CPU_HTREF0 — R6 HT_REF0 — CPU_HTREF1 — P6 HT_REF1

26 CPU_VDD0_FB_H — F6 VDD0_FB_H

26 CPU_VDD0_FB_L — E6 VDD0_FB_L

26 CPU_VDD1_FB_H — Y6 VDD1_FB_H

26 CPU_VDD1_FB_L — AB6 VDD1_FB_L

CPU_DBRDY — G10 DBRDY

CPU_TMS — AA9 TMS

CPU_TCK — AC9 TCK

CPU_TRST# — AD9 TRST_L

CPU_TDI — AF9 TDI

T78 — CPU_TEST23_TSTUPD — AD7 TEST23

T57 — CPU_TEST18_PLLTEST1 — H10 TEST18

T52 — CPU_TEST19_PLLTEST0 — G9 TEST19

CPU_TEST25_H_BYPASSCLK_H — F9 TEST25_H

CPU_TEST25_L_BYPASSCLK_L — E8 TEST25_L

T2 — CPU_TEST21_SCANEN — AB8 TEST21

T73 — CPU_TEST20_SCANCLK2 — AF7 TEST20

T80 — CPU_TEST24_SCANCLK1 — AE7 TEST24

T77 — CPU_TEST22_SCANSHIFTEN — AE8 TEST22

T1 — CPU_TEST12_SCANSHIFTENB — AC8 TEST12

T76 — CPU_TEST27_SINGLECHAIN — AF8 TEST27

R215 0_4 — CPU_TEST9_ANALOGIN — C2 TEST9

T26 — CPU_TEST6_DIECRACKMON — AA6 TEST6

A3 RSVD1, A5 RSVD2, B3 RSVD3, B5 RSVD4, C1 RSVD5

M11 KEY1, W18 KEY2

A6 CPU_SVC_R — SVC

A4 CPU_SVD_R — SVD

AF6 THERMTRIP_L — CPU_THERMTRIP#

AC7 PROCHOT_L — CPU_PROCHOT#

AA8 MEMHOT_L — CPU_MEMHOT#

W7 THERMDC — CPU_THERMDC

W8 THERMDA — CPU_THERMDA

W9 VDDIO_FB_H — CPU_VDDIO_FB_H 29

Y9 VDDIO_FB_L — CPU_VDDIO_FB_L 29

H6 VDDNB_FB_H — VDD_NB_FB_H 26

G6 VDDNB_FB_L — VDD_NB_FB_L 26

E10 CPU_DBREQ#

AE9 CPU_TDO

J7 CPU_TEST28_H_PLLCHRZ_P — T51

H8 CPU_TEST28_L_PLLCHRZ_N — T48

D7 CPU_TEST17_BP3 — T58

E7 CPU_TEST16_BP2 — T56

F7 CPU_TEST15_BP1 — T93

C7 CPU_TEST14_BP0 — T91

C3 CPU_TEST7_ANALOG_T — T89

K8 CPU_TEST10_ANALOGOUT — T46

C4 CPU_TEST8_DIG_T — T88

C9 CPU_TEST29_H_FBCLKOUT_P — T59

C8 CPU_TEST29_L_FBCLKOUT_N — T90

H18 RSVD10, H19 RSVD9, AA7 RSVD8, D5 RSVD7, C5 RSVD6

Athlon 64 S1g2 SOCKET_638_PIN

Athlon 64 S1g2 Processor Socket SOCKET_638_PIN

connect to CPU VDDIO power FB

connect to CPU CORE power FB

connect to CPU VDDNB power FB

route as differential as short as possible testpoint under package

+1.8VSUS

R97 300_4 — R98 330_4 — Q16 MMBT3904

CPU_PROCHOT# — EC_PROCHOT# 21

R96 *0_4 — MCP77_PROCHOT# 7

CHECK MCP thermal

+1.8VSUS

R168 *300_4 — R112 *330_4 — Q17 *MMBT3904

CPU_MEMHOT# — CPUMEMHOT# 21

connect to CPU CORE power controlier

+1.8VSUS

R456 300_4

7 HTCPU_PWRGD — R455 0_4 — CPU_HT_PWRGD

C650 .1u/10V_4

REV:B Modify

+1.8VSUS

R465 300_4

7 HTCPU_STOP# — R464 0_4 — CPU_HT_LDTSTOP#

+1.8VSUS

R457 300_4

7 HTCPU_RST# — R458 0_4 — CPU_HT_RESET#

REV:E Modify by AMD

+1.8VSUS — R206 300_4 — R469 300_4

Add pull up

+1.8VSUS

R466 300_4

CPU_LDT_REQ# CPU — R467 0_4 — HTCPU_REQ# — HTCPU_REQ# 7

VID Override Circuit

+1.8VSUS

R454 1K_4 — R453 1K_4

CPU_SVC_R — R452 0_4 — Serial VID Clock — SVC 26

CPU_SVD_R — R451 0_4 — Serial VID Data — SVD 26

HTCPU_PWRGD — R459 0_4 — PGD_IN 26

R462 *220_4 — R461 *220_4

VFIX MODE

SVC	SVD	Voltage Output(CPU Power)
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V

+1.8VSUS

CPU_TEST27_SINGLECHAIN — R382 *300_4

CPU_TEST18_PLLTEST1 — R204 *300_4

CPU_TEST19_PLLTEST0 — R203 *300_4

CPU_TEST15_BP1 — R470 *300_4

CPU_TEST14_BP0 — R471 *300_4

CPU_TEST23_TSTUPD — R555 300_4

CPU_TEST21_SCANEN — R396 300_4

CPU_TEST20_SCANCLK2 — R385 300_4

CPU_TEST24_SCANCLK1 — R386 300_4

CPU_TEST22_SCANSHIFTEN — R384 *300_4

CPU_TEST12_SCANSHIFTENB — R391 *300_4

Rev:E Add R555 by AMD Design guide 41650 V1_03 on 5/8.

Need Check with nVidia

HDT CONNECTOR

+1.8VSUS

R381 *220_4 — R380 *220_4 — R477 *220_4 — R383 *220_4 — R478 300_4

CPU_DBREQ# — T92

CPU_DBRDY — T55

CPU_TCK — T81

CPU_TMS — T31

CPU_TDI — T75

CPU_TRST# — T79

CPU_TDO — T4

HDTGND

CN21 *ASP-68200-07-25P-LDV

GND1, RSVD1, RSVD0, DBREQ_L, DBRDY, TCK, TMS, TDI, TRST_L, TDO, VCC_PROC_IO_21, VCC_PROC_IO_23, KEY

GND2, GND4, GND6, GND8, GND10, GND12, GND14, GND16, GND18, GND20, GND22, RESET_L, GND26

H_HTCPU_RST#

+1.8VSUS — +3V

R475 *10K_4 — R473 *1K/F_4 — H_HTCPU_RST#

CPU_HT_RESET# — Q45 *MMBT3904

CPU H/W MONITOR

2/20/08' Reserve 0 ohm for CPU thermal issue on C-test

+3V — R151 47/F_6 — 3V_THM — 15 MIL

R515 *0_4 — C120 .1u/10V_4

CPU_THERMDC — C117 2200P_4 — CPU_THERMDA

10 mil trace / 10 mil space

Address 98H

U7 G786: VCC, DXN, DXP, -OVT, -ALT, SMDATA, SMCLK, GND

KBSMDAT, KBSMCLK

+3V — R136 10K_4 — Q33 2N7002E — To SB GPIO — THERM_ALERT# 12

+3V — R140 4.7K_4 — Q37 2N7002E — 2ND_MBDATA 21

+3V — R143 4.7K_4 — Q36 2N7002E — 2ND_MBCLK 21

+3V — R128 10K_4 — To FAN — CPUFAN#_ON 17

Quanta Computer Inc.

PROJECT : ZY5D

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	AMD Griffin CTRL & DEBUG	3B

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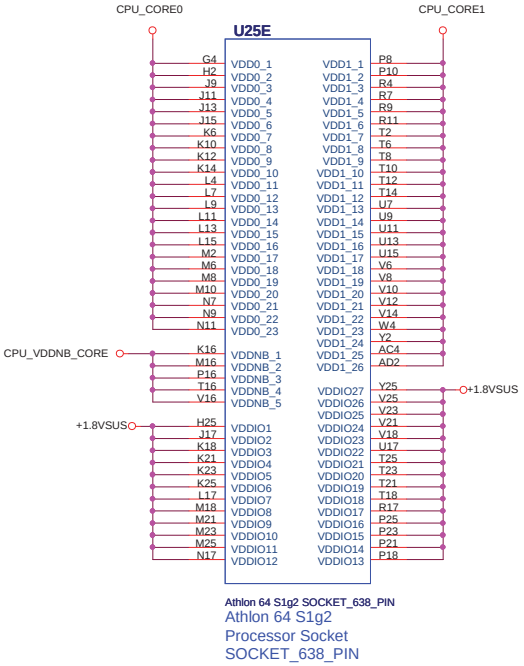
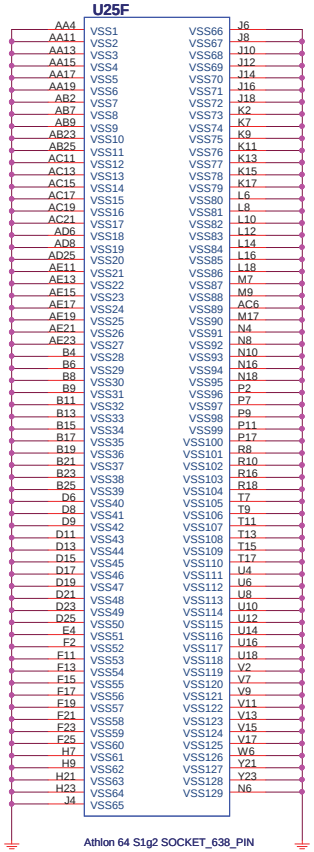
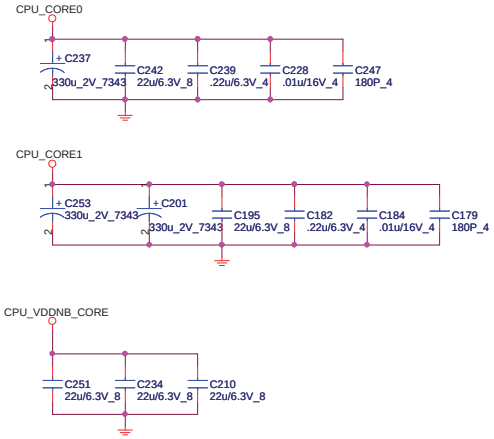
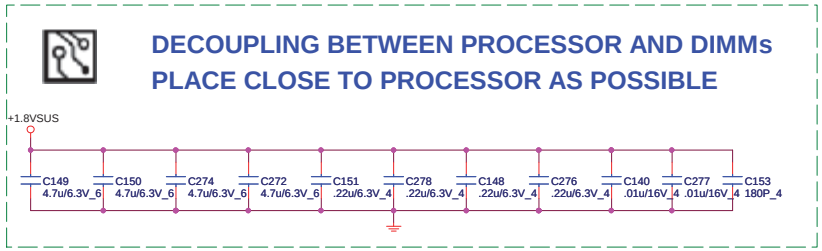
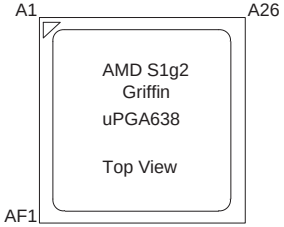
PROCESSOR POWER AND GROUND











Quanta Computer Inc.

PROJECT : ZY5D

Size	Document Number	Rev
	AMD Griffin PWR & GND	3B

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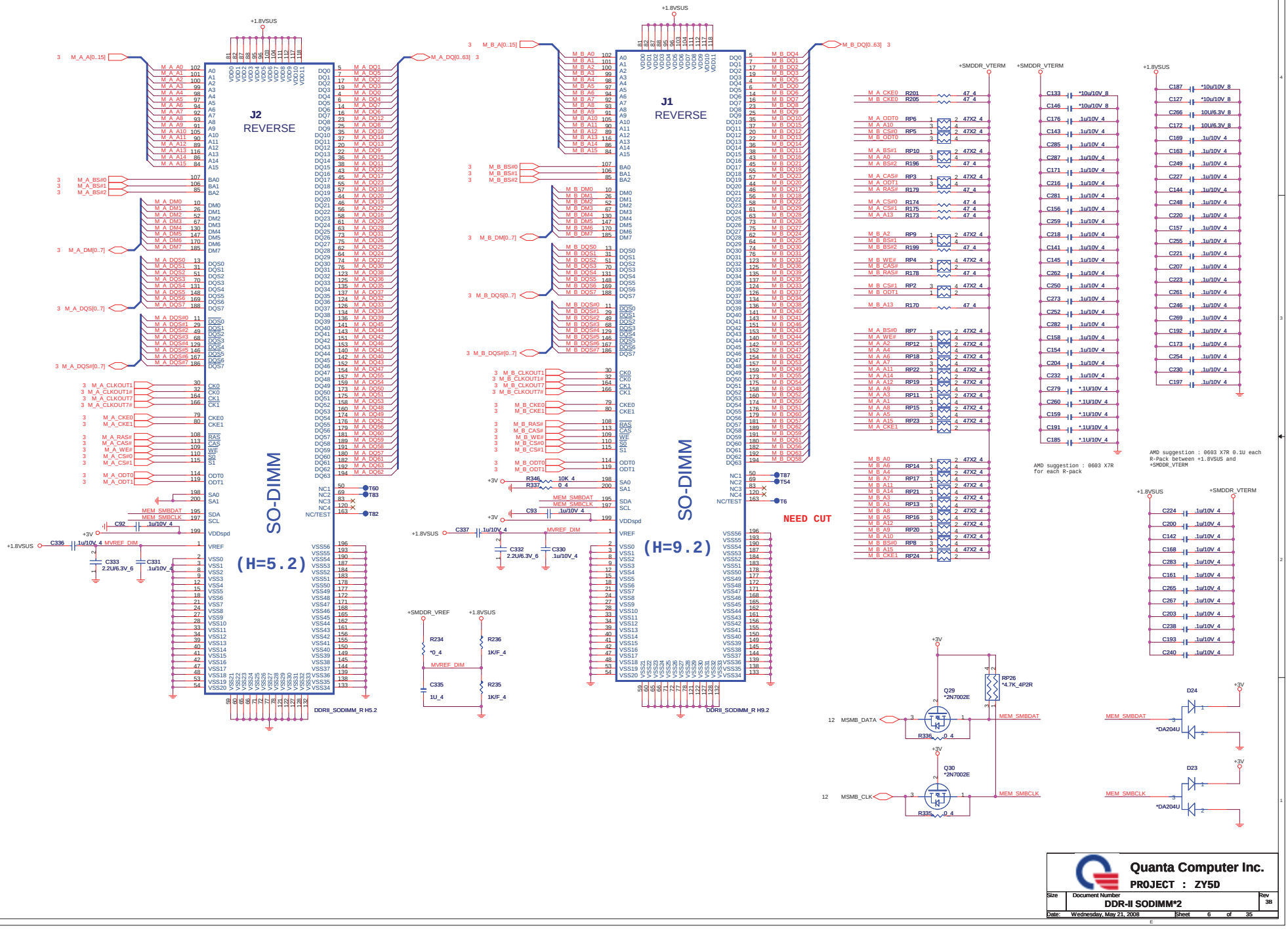
J2
REVERSE
SO-DIMM
(H=5.2)
DDRII_SODIMM_R H5.2
J1
REVERSE
SO-DIMM
(H=9.2)
DDRII_SODIMM_R H9.2
NEED CUT
AMD suggestion : 0603 X7R 0.1U each R-Pack between +1.8VSUS and +SMDDR_VTERM
AMD suggestion : 0603 X7R for each R-pack
Quanta Computer Inc.
PROJECT : ZY5D
Size
Document Number
DDR-II SODIMM*2
Rev 3B
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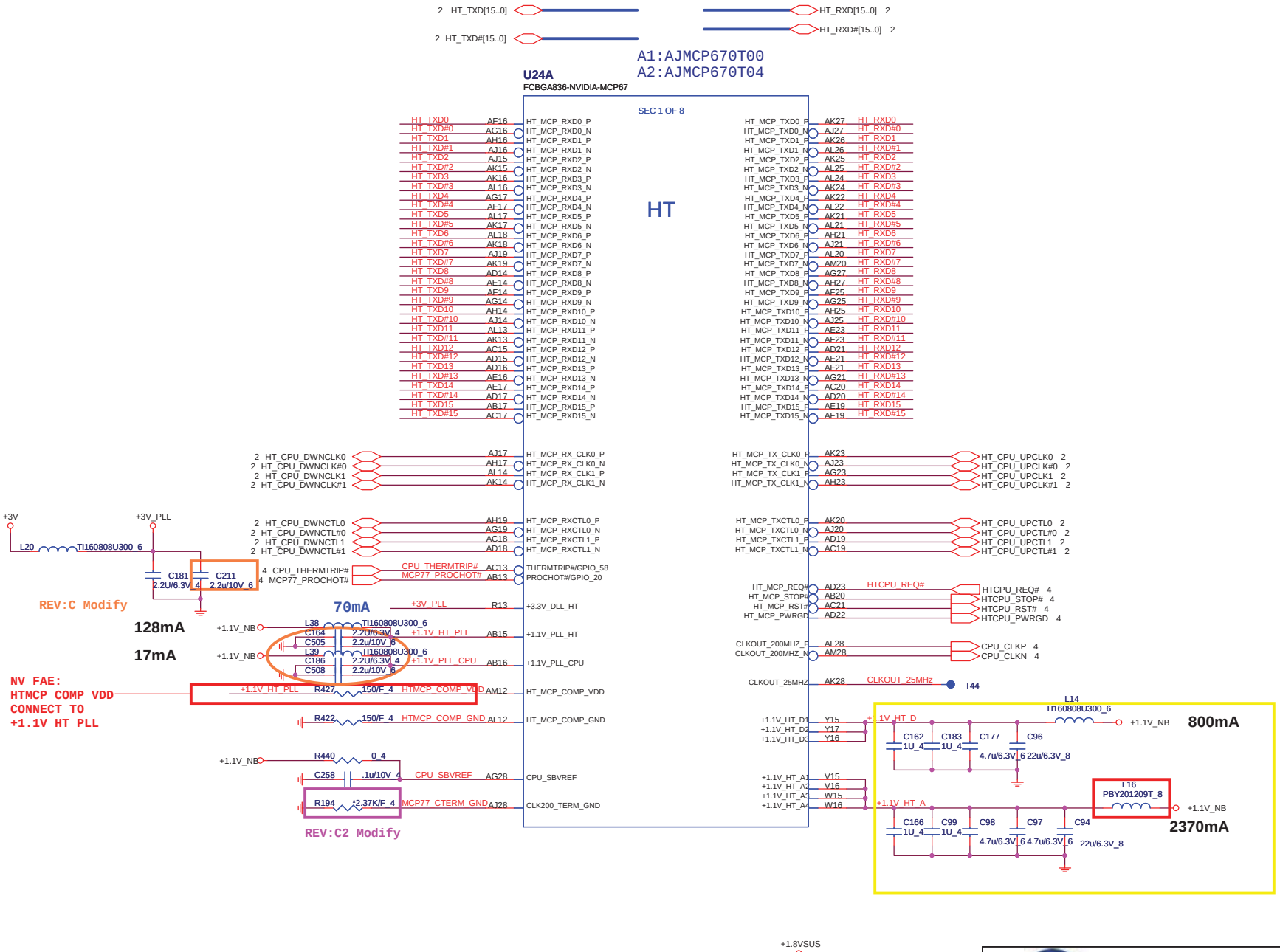

2 HT_TXD[15..0]
2 HT_TXD#[15..0]
HT_RXD[15..0] 2
HT_RXD#[15..0] 2
A1:AJMCP670T00
A2:AJMCP670T04
U24A
FCBGA836-NVIDIA-MCP67
SEC 1 OF 8
HT
HT_TXD0 AE16 HT_MCP_RXD0_P
HT_TXD#0 AG16 HT_MCP_RXD0_N
HT_TXD1 AH16 HT_MCP_RXD1_P
HT_TXD#1 AJ16 HT_MCP_RXD1_N
HT_TXD2 AJ15 HT_MCP_RXD2_P
HT_TXD#2 AK15 HT_MCP_RXD2_N
HT_TXD3 AK16 HT_MCP_RXD3_P
HT_TXD#3 AL16 HT_MCP_RXD3_N
HT_TXD4 AG17 HT_MCP_RXD4_P
HT_TXD#4 AF17 HT_MCP_RXD4_N
HT_TXD5 AL17 HT_MCP_RXD5_P
HT_TXD#5 AK17 HT_MCP_RXD5_N
HT_TXD6 AL18 HT_MCP_RXD6_P
HT_TXD#6 AK18 HT_MCP_RXD6_N
HT_TXD7 AJ19 HT_MCP_RXD7_P
HT_TXD#7 AK19 HT_MCP_RXD7_N
HT_TXD8 AD14 HT_MCP_RXD8_P
HT_TXD#8 AE14 HT_MCP_RXD8_N
HT_TXD9 AE14 HT_MCP_RXD9_P
HT_TXD#9 AG14 HT_MCP_RXD9_N
HT_TXD10 AH14 HT_MCP_RXD10_P
HT_TXD#10 AJ14 HT_MCP_RXD10_N
HT_TXD11 AL13 HT_MCP_RXD11_P
HT_TXD#11 AK13 HT_MCP_RXD11_N
HT_TXD12 AC15 HT_MCP_RXD12_P
HT_TXD#12 AD15 HT_MCP_RXD12_N
HT_TXD13 AD16 HT_MCP_RXD13_P
HT_TXD#13 AE16 HT_MCP_RXD13_N
HT_TXD14 AE17 HT_MCP_RXD14_P
HT_TXD#14 AD17 HT_MCP_RXD14_N
HT_TXD15 AB17 HT_MCP_RXD15_P
HT_TXD#15 AC17 HT_MCP_RXD15_N
HT_MCP_TXD0_P AK27 HT_RXD0
HT_MCP_TXD0_N AJ27 HT_RXD#0
HT_MCP_TXD1_P AK26 HT_RXD1
HT_MCP_TXD1_N AL26 HT_RXD#1
HT_MCP_TXD2_P AK25 HT_RXD2
HT_MCP_TXD2_N AL25 HT_RXD#2
HT_MCP_TXD3_P AL24 HT_RXD3
HT_MCP_TXD3_N AK24 HT_RXD#3
HT_MCP_TXD4_P AK22 HT_RXD4
HT_MCP_TXD4_N AL22 HT_RXD#4
HT_MCP_TXD5_P AK21 HT_RXD5
HT_MCP_TXD5_N AL21 HT_RXD#5
HT_MCP_TXD6_P AH21 HT_RXD6
HT_MCP_TXD6_N AJ21 HT_RXD#6
HT_MCP_TXD7_P AL20 HT_RXD7
HT_MCP_TXD7_N AM20 HT_RXD#7
HT_MCP_TXD8_P AG27 HT_RXD8
HT_MCP_TXD8_N AH27 HT_RXD#8
HT_MCP_TXD9_P AF25 HT_RXD9
HT_MCP_TXD9_N AG25 HT_RXD#9
HT_MCP_TXD10_P AH25 HT_RXD10
HT_MCP_TXD10_N AJ25 HT_RXD#10
HT_MCP_TXD11_P AF23 HT_RXD11
HT_MCP_TXD11_N AF23 HT_RXD#11
HT_MCP_TXD12_P AD21 HT_RXD12
HT_MCP_TXD12_N AE21 HT_RXD#12
HT_MCP_TXD13_P AF21 HT_RXD13
HT_MCP_TXD13_N AG21 HT_RXD#13
HT_MCP_TXD14_P AC20 HT_RXD14
HT_MCP_TXD14_N AD20 HT_RXD#14
HT_MCP_TXD15_P AE19 HT_RXD15
HT_MCP_TXD15_N AF19 HT_RXD#15
2 HT_CPU_DWNCLK0 AJ17 HT_MCP_RX_CLK0_P
2 HT_CPU_DWNCLK#0 AH17 HT_MCP_RX_CLK0_N
2 HT_CPU_DWNCLK1 AL14 HT_MCP_RX_CLK1_P
2 HT_CPU_DWNCLK#1 AK14 HT_MCP_RX_CLK1_N
HT_MCP_TX_CLK0_P AK23 HT_CPU_UPCLK0 2
HT_MCP_TX_CLK0_N AJ23 HT_CPU_UPCLK#0 2
HT_MCP_TX_CLK1_P AG23 HT_CPU_UPCLK1 2
HT_MCP_TX_CLK1_N AH23 HT_CPU_UPCLK#1 2
2 HT_CPU_DWNCTL0 AH19 HT_MCP_RXCTL0_P
2 HT_CPU_DWNCTL#0 AG19 HT_MCP_RXCTL0_N
2 HT_CPU_DWNCTL1 AC18 HT_MCP_RXCTL1_P
2 HT_CPU_DWNCTL#1 AD18 HT_MCP_RXCTL1_N
HT_MCP_TXCTL0_P AK20 HT_CPU_UPCTL0 2
HT_MCP_TXCTL0_N AJ20 HT_CPU_UPCTL#0 2
HT_MCP_TXCTL1_P AD19 HT_CPU_UPCTL1 2
HT_MCP_TXCTL1_N AC19 HT_CPU_UPCTL#1 2
+3V
+3V_PLL
L20 TI160808U300_6
C181 2.2U/6.3V_4
C211 2.2u/10V_6
REV:C Modify
128mA
17mA
4 CPU_THERMTRIP#
4 MCP77_PROCHOT#
CPU_THERMTRIP# AC13 THERMTRIP#/GPIO_58
MCP77_PROCHOT# AB13 PROCHOT#/GPIO_20
70mA
+3V_PLL
R13 +3.3V_DLL_HT
+1.1V_NB
L38 TI160808U300_6
C164 2.2U/6.3V_4
C505 2.2u/10V_6
+1.1V_HT_PLL AB15 +1.1V_PLL_HT
L39 TI160808U300_6
C186 2.2U/6.3V_4
C508 2.2u/10V_6
+1.1V_PLL_CPU AB16 +1.1V_PLL_CPU
NV FAE:
HTMCP_COMP_VDD
CONNECT TO
+1.1V_HT_PLL
R427 150/F_4 HTMCP_COMP_VDD AM12 HT_MCP_COMP_VDD
R422 150/F_4 HTMCP_COMP_GND AL12 HT_MCP_COMP_GND
R440 0_4
C258 .1u/10V_4 CPU_SBVREF AG28 CPU_SBVREF
R194 *2.37K/F_4 MCP77_CTERM_GND AJ28 CLK200_TERM_GND
REV:C2 Modify
HT_MCP_REQ# AD23 HTCPU_REQ#
HT_MCP_STOP# AB20
HT_MCP_RST# AC21
HT_MCP_PWRGD AD22
HTCPU_REQ# 4
HTCPU_STOP# 4
HTCPU_RST# 4
HTCPU_PWRGD 4
CLKOUT_200MHZ_P AL28
CLKOUT_200MHZ_N AM28
CPU_CLKP 4
CPU_CLKN 4
CLKOUT_25MHZ AK28 CLKOUT_25MHz
T44
+1.1V_HT_D1 Y15
+1.1V_HT_D2 Y17
+1.1V_HT_D3 Y16
+1.1V_HT_D
L14 TI160808U300_6
+1.1V_NB
800mA
C162 1U_4
C183 1U_4
C177 4.7u/6.3V_6
C96 22u/6.3V_8
+1.1V_HT_A1 V15
+1.1V_HT_A2 V16
+1.1V_HT_A3 W15
+1.1V_HT_A4 W16
+1.1V_HT_A
L16 PBY201209T_8
+1.1V_NB
2370mA
C166 1U_4
C99 1U_4
C98 4.7u/6.3V_6
C97 4.7u/6.3V_6
C94 22u/6.3V_8
+1.8VSUS
MCP77_PROCHOT# R421 300_4
Quanta Computer Inc.
PROJECT : ZY5D
Size
Document Number
MCP77 HyperTransport Bus
Rev 3B
Date: Wednesday, May 21, 2008
Sheet 7 of 35

14 PEG_RXP[15:0]
14 PEG_RXN[15:0]
PEG_TXP[15:0] 14
PEG_TXN[15:0] 14

U24B
FCBGA836-NVIDIA-MCP67

SEC 2 OF 8

PCIE

+3V_S5 R424 *10K_4 PCIE_WAKE#

PEG_RXP0 F23 PE0_RX0_P
PEG_RXN0 G23 PE0_RX0_N
PEG_RXP1 F24 PE0_RX1_P
PEG_RXN1 F25 PE0_RX1_N
PEG_RXP2 D25 PE0_RX2_P
PEG_RXN2 D26 PE0_RX2_N
PEG_RXP3 C28 PE0_RX3_P
PEG_RXN3 D28 PE0_RX3_N
PEG_RXP4 C29 PE0_RX4_P
PEG_RXN4 C30 PE0_RX4_N
PEG_RXP5 D29 PE0_RX5_P
PEG_RXN5 D30 PE0_RX5_N
PEG_RXP6 F26 PE0_RX6_P
PEG_RXN6 F27 PE0_RX6_N
PEG_RXP7 F28 PE0_RX7_P
PEG_RXN7 F29 PE0_RX7_N
PEG_RXP8 H23 PE0_RX8_P
PEG_RXN8 H24 PE0_RX8_N
PEG_RXP9 H25 PE0_RX9_P
PEG_RXN9 H26 PE0_RX9_N
PEG_RXP10 H27 PE0_RX10_P
PEG_RXN10 H28 PE0_RX10_N
PEG_RXP11 K24 PE0_RX11_P
PEG_RXN11 K25 PE0_RX11_N
PEG_RXP12 K27 PE0_RX12_P
PEG_RXN12 K26 PE0_RX12_N
PEG_RXP13 K28 PE0_RX13_P
PEG_RXN13 K29 PE0_RX13_N
PEG_RXP14 J31 PE0_RX14_P
PEG_RXN14 J30 PE0_RX14_N
PEG_RXP15 K31 PE0_RX15_P
PEG_RXN15 K30 PE0_RX15_N

PE0_TX0_P D24 C_PEG_TXP0 C504 *_EV^.1u/10V^4G_TXP0
PE0_TX0_N C24 C_PEG_TXN0 C506 *_EV^.1u/10V^4G_TXN0
PE0_TX1_P A24 C_PEG_TXP1 C507 *_EV^.1u/10V^4G_TXP1
PE0_TX1_N B24 C_PEG_TXN1 C509 *_EV^.1u/10V^4G_TXN1
PE0_TX2_P B25 C_PEG_TXP2 C510 *_EV^.1u/10V^4G_TXP2
PE0_TX2_N C25 C_PEG_TXN2 C513 *_EV^.1u/10V^4G_TXN2
PE0_TX3_P B26 C_PEG_TXP3 C514 *_EV^.1u/10V^4G_TXP3
PE0_TX3_N C26 C_PEG_TXN3 C517 *_EV^.1u/10V^4G_TXN3
PE0_TX4_P C27 C_PEG_TXP4 C518 *_EV^.1u/10V^4G_TXP4
PE0_TX4_N D27 C_PEG_TXN4 C519 *_EV^.1u/10V^4G_TXN4
PE0_TX5_P A28 C_PEG_TXP5 C520 *_EV^.1u/10V^4G_TXP5
PE0_TX5_N B28 C_PEG_TXN5 C521 *_EV^.1u/10V^4G_TXN5
PE0_TX6_P A29 C_PEG_TXP6 C522 *_EV^.1u/10V^4G_TXP6
PE0_TX6_N B29 C_PEG_TXN6 C524 *_EV^.1u/10V^4G_TXN6
PE0_TX7_P A30 C_PEG_TXP7 C525 *_EV^.1u/10V^4G_TXP7
PE0_TX7_N B30 C_PEG_TXN7 C529 *_EV^.1u/10V^4G_TXN7
PE0_TX8_P B31 C_PEG_TXP8 C531 *_EV^.1u/10V^4G_TXP8
PE0_TX8_N B32 C_PEG_TXN8 C536 *_EV^.1u/10V^4G_TXN8
PE0_TX9_P C31 C_PEG_TXP9 C537 *_EV^.1u/10V^4G_TXP9
PE0_TX9_N C32 C_PEG_TXN9 C541 *_EV^.1u/10V^4G_TXN9
PE0_TX10_P D31 C_PEG_TXP10 C545 *_EV^.1u/10V^4G_TXP10
PE0_TX10_N D32 C_PEG_TXN10 C547 *_EV^.1u/10V^4G_TXN10
PE0_TX11_P E31 C_PEG_TXP11 C550 *_EV^.1u/10V^4G_TXP11
PE0_TX11_N E30 C_PEG_TXN11 C551 *_EV^.1u/10V^4G_TXN11
PE0_TX12_P F31 C_PEG_TXP12 C552 *_EV^.1u/10V^4G_TXP12
PE0_TX12_N F30 C_PEG_TXN12 C554 *_EV^.1u/10V^4G_TXN12
PE0_TX13_P G29 C_PEG_TXP13 C560 *_EV^.1u/10V^4G_TXP13
PE0_TX13_N G30 C_PEG_TXN13 C561 *_EV^.1u/10V^4G_TXN13
PE0_TX14_P H29 C_PEG_TXP14 C566 *_EV^.1u/10V^4G_TXP14
PE0_TX14_N H30 C_PEG_TXN14 C567 *_EV^.1u/10V^4G_TXN14
PE0_TX15_P H32 C_PEG_TXP15 C572 *_EV^.1u/10V^4G_TXP15
PE0_TX15_N H31 C_PEG_TXN15 C574 *_EV^.1u/10V^4G_TXN15

PEA_REFCLK_P R29 PE0_REFCLK_P R216 *_EV^22_4 CLK_PCIE_MXM 14
PEA_REFCLK_N R30 PE0_REFCLK_N R217 *_EV^22_4 CLK_PCIE_MXM# 14

Notice

Page 08 : MXM circuit ZY5D no use it

16,18,21 PCIE_WAKE# PCIE_WAKE# H17 PE_WAKE#/GPIO_21
T85 PE0_PRSNTX1 U31 PE0_PRSNT_1#
T86 PE0_PRSNTX4 U30 PE0_PRSNT_4#
T84 PE0_PRSNTX8 U29 PE0_PRSNT_8#
PE0_PRSNTX16# U28 PE0_PRSNT_16#
14 PE0_PRSNTX16#
9 MXM_ON#
R410 *_EV^0_4

[MINI CARD]
16 PCIE_RXP1 L29 PE1_RX_P
16 PCIE_RXN1 L30 PE1_RX_N
16 MINI_CLKREQ# MINI_CLKREQ# W27 PEB_CLKREQ#
W28 PEB_PRSNT#

[TV]
16 PCIE_RXP2 M26 PE2_RX_P
16 PCIE_RXN2 M27 PE2_RX_N
16 TV_CLKREQ# TV_CLKREQ# U26 PEC_CLKREQ#
R198 0_4 U27 PEC_PRSNT#

[Giga LAN]
18 PCIE_RXP3 N23 PE3_RX_P
18 PCIE_RXN3 N22 PE3_RX_N
18 LAN_CLKREQ# LAN_CLKREQ# U25 PED_CLKREQ#
R193 0_4 U24 PED_PRSNT#

[NEW CARD]
16 PCIE_RXP5 P31 PE5_RX_P
16 PCIE_RXN5 P30 PE5_RX_N
16 NEW_CLKREQ# NEW_CLKREQ# T22 PEF_CLKREQ#/GPIO_17
16 CPPE# D30 BAS16 CPPE#_C V31 PEF_PRSNT#

N30 PE4_RX_P
N31 PE4_RX_N
R22 PEE_CLKREQ#/GPIO_16
U23 PEE_PRSNT#

P26 PE6_RX_P
P27 PE6_RX_N
U22 PEG_CLKREQ#/GPIO_18
V30 PEG_PRSNT#

PE1_TX_P M28 PCIE_TXP1_C C294 *_MINI^.1u/10V_4 PCIE_TXP1 16
PE1_TX_N M29 PCIE_TXN1_C C298 *_MINI^.1u/10V_4 PCIE_TXN1 16
PEB_REFCLK_P T32 CLK_PCIE_MINI1_R R214 *_MINI^22_4 CLK_PCIE_MINI 16
PEB_REFCLK_N T31 CLK_PCIE_MINI1#_R R213 *_MINI^22_4 CLK_PCIE_MINI# 16

PE2_TX_P M24 PCIE_TXP2_C C270 .1u/10V_4 PCIE_TXP2 16
PE2_TX_N M25 PCIE_TXN2_C C263 .1u/10V_4 PCIE_TXN2 16
PEC_REFCLK_P T29 CLK_PCIE_TV_R R207 22_4 CLK_PCIE_TV 16
PEC_REFCLK_N T30 CLK_PCIE_TV#_R R208 22_4 CLK_PCIE_TV# 16

PE3_TX_P M22 PCIE_TXP3_C C233 .1u/10V_4 PCIE_TXP3 18
PE3_TX_N M23 PCIE_TXN3_C C226 .1u/10V_4 PCIE_TXN3 18
PED_REFCLK_P T27 CLK_PCIE_LAN_R R191 22_4 CLK_PCIE_LAN 18
PED_REFCLK_N T28 CLK_PCIE_LAN#_R R195 22_4 CLK_PCIE_LAN# 18

PE4_TX_P M30
PE4_TX_N M31
PEE_REFCLK_P T25
PEE_REFCLK_N T26

PE5_TX_P P29 PCIE_TXP5_C C300 *_NEW^.1u/10V_4 PCIE_TXP5 16
PE5_TX_N P28 PCIE_TXN5_C C299 *_NEW^.1u/10V_4 PCIE_TXN5 16
PEF_REFCLK_P T23 CLK_PCIE_NEW_C_R R210 *_NEW^22_4 CLK_PCIE_NEW_C 16
PEF_REFCLK_N T24 CLK_PCIE_NEW_C#_R R209 *_NEW^22_4 CLK_PCIE_NEW_C# 16

PE6_TX6_P P24
PE6_TX6_N P25
PEG_REFCLK_P P23
PEG_REFCLK_N R23

Notice

[MXM]

Page 08 : MXM circuit ZY5D no use it

Notice

[MINI CARD ZY5 only]

[TV ZY5 only , MINI CARD ZY7 only]

[Giga LAN]

ZY5D B modify use single stack _wireless Card

[Card Reader] By Jack Weng

[NEW CARD]

Page 08 : NEW CARD circuit ZY5D no use it

Notice

+1.1V_NB +1.1V_PLLPE_SS

L40 MLG1608B10NJ_6

REV:B Modify

10mA

C194 4.7u/6.3V_6
C199 2.2U/6.3V_4
+1.1V_PLLPE_SS U19 +1.1V_PLL_PE_SS1

80mA

L41 MLG1608B10NJ_6
C215 2.2U/6.3V_4
C515 2.2u/10V_6
+1.1V_PLLPE R20 +1.1V_PLL_PE1
R19 NC2/+1.2V_PLL_PE2

POWER connect to DLL_HT

+3V_PLL +3V_PLL P20 NC1/+3.3V_PLL_PE_SS2

REV:C Modify

C217 .1u/10V_4 PE_CLK_COMP V24 PE_CLK_COMP

R192 *2.37K/F_4 <500mil

Remove R116 for Nvidia suggest.

700mA

+1.1V_PED A1 W26 +1.1V_PED
+1.1V_PED B1 W24
+1.1V_PED B2 V23
+1.1V_PED B3 V22
+1.1V_PED B4 W25

C225 .1u/10V_4 C241 1U_4 C549 1U_4 C548 22u/6.3V_8
L44 0_6 +1.1V_NB

2063mA

+1.1V_PEA A1 Y29
+1.1V_PEA A2 Y27
+1.1V_PEA B1 Y25
+1.1V_PEA B2 Y24
+1.1V_PEA B3 W23
+1.1V_PEA B4 Y23
+1.1V_PEA B5 W22
+1.1V_PEA B6 Y22

+1.1V_PEA

C236 .1u/10V_4 C244 .1u/10V_4 C214 .1u/10V_4 C229 1U_4 C558 4.7u/6.3V_6 C571 22u/6.3V_8 C564 22u/6.3V_8 C575 22u/6.3V_8
L50 PBY201209T_8 +1.1V_NB

PE_RST0# W30
PE_RST1# W29

PCIE_RST0# 14,18 (For MXM, LAN ,Card Reader)

Add 0R resistor, The resistor should only be stuffed for MCP67D

R448 *0_4

PCIE_RST1# 16 (For New card, WL,TV)

For EMI

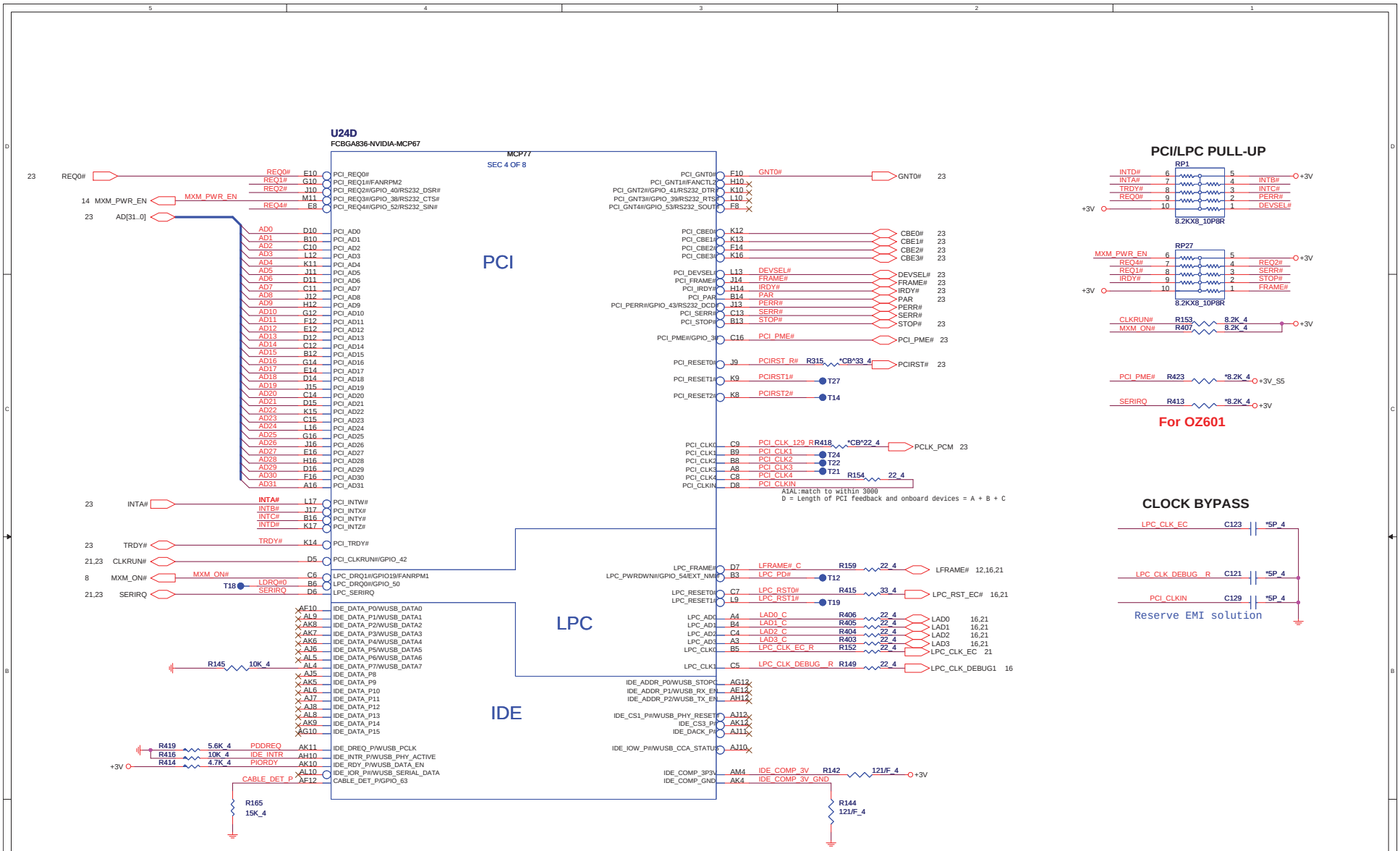
CLK_PCIE_MXM C316 *10P_4
CLK_PCIE_MXM# C317 *10P_4
CLK_PCIE_MINI C310 *10P_4
CLK_PCIE_MINI# C309 *10P_4
CLK_PCIE_NEW_C C297 *10P_4
CLK_PCIE_NEW_C# C296 *10P_4
CLK_PCIE_LAN C235 *10P_4
CLK_PCIE_LAN# C245 *10P_4
CLK_PCIE_TV C284 *10P_4
CLK_PCIE_TV# C292 *10P_4

Internal 15K to 3.3V

R220 *22K_4 MINI_CLKREQ#
R188 *22K_4 NEW_CLKREQ#
R449 *22K_4 CPPE#_C
R219 *22K_4 TV_CLKREQ#
R197 *22K_4 LAN_CLKREQ#

Quanta Computer Inc.
PROJECT : ZY5D

Size	Document Number	Rev
	MCP77 PCI-Express Bus	3B
Date: Friday, July 25, 2008	Sheet 8 of 35	

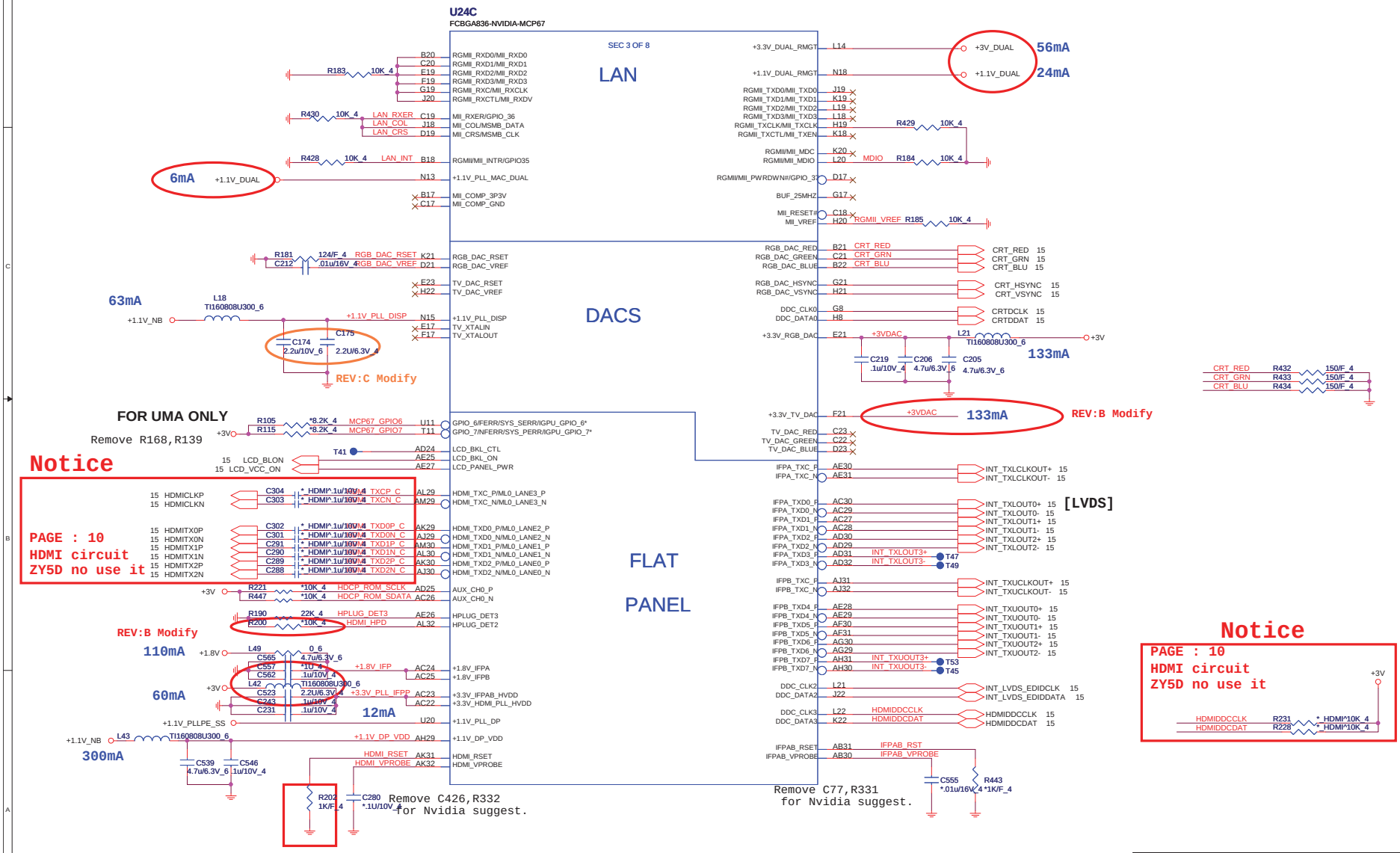


Quanta Computer Inc.

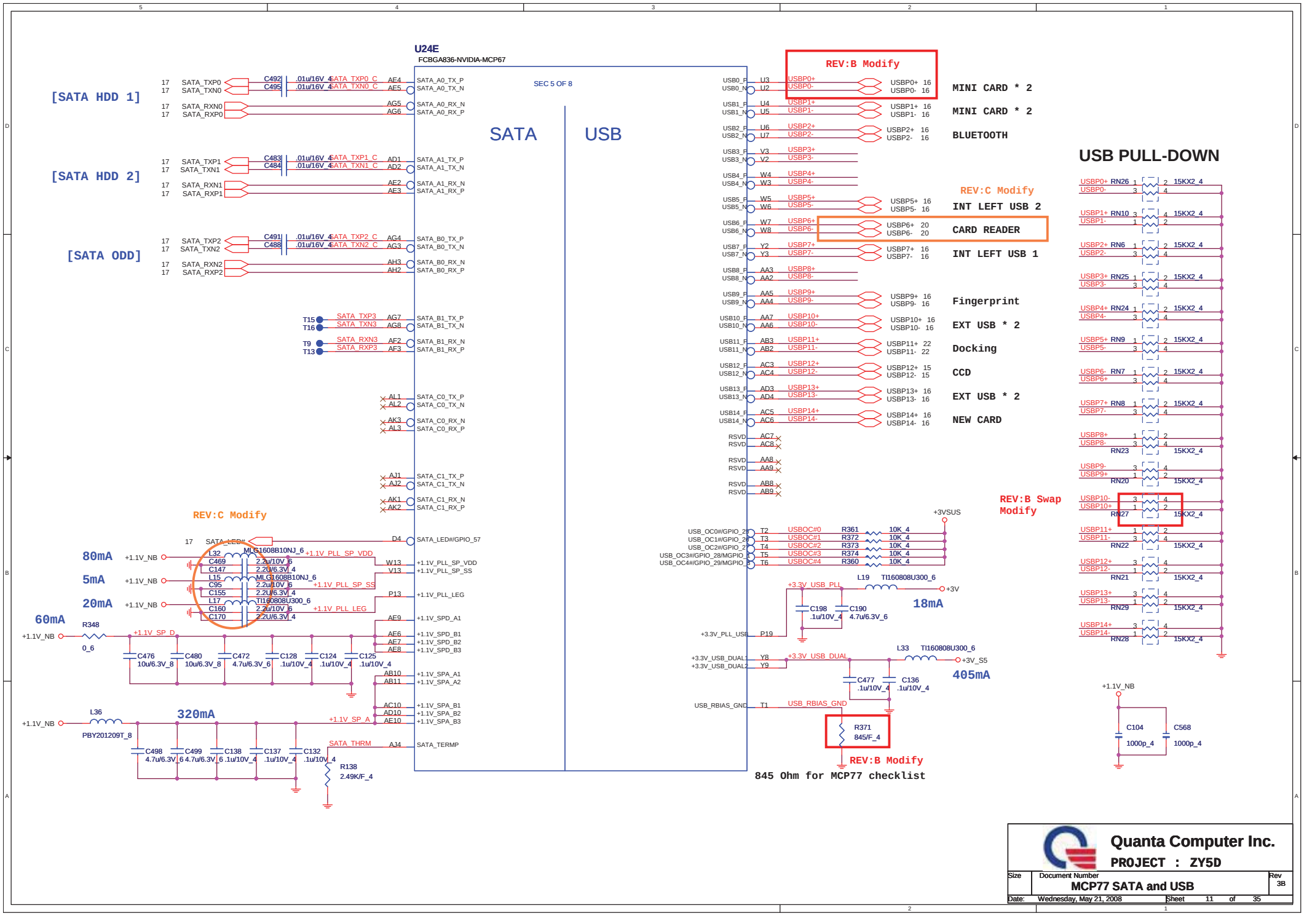
PROJECT : ZY5D

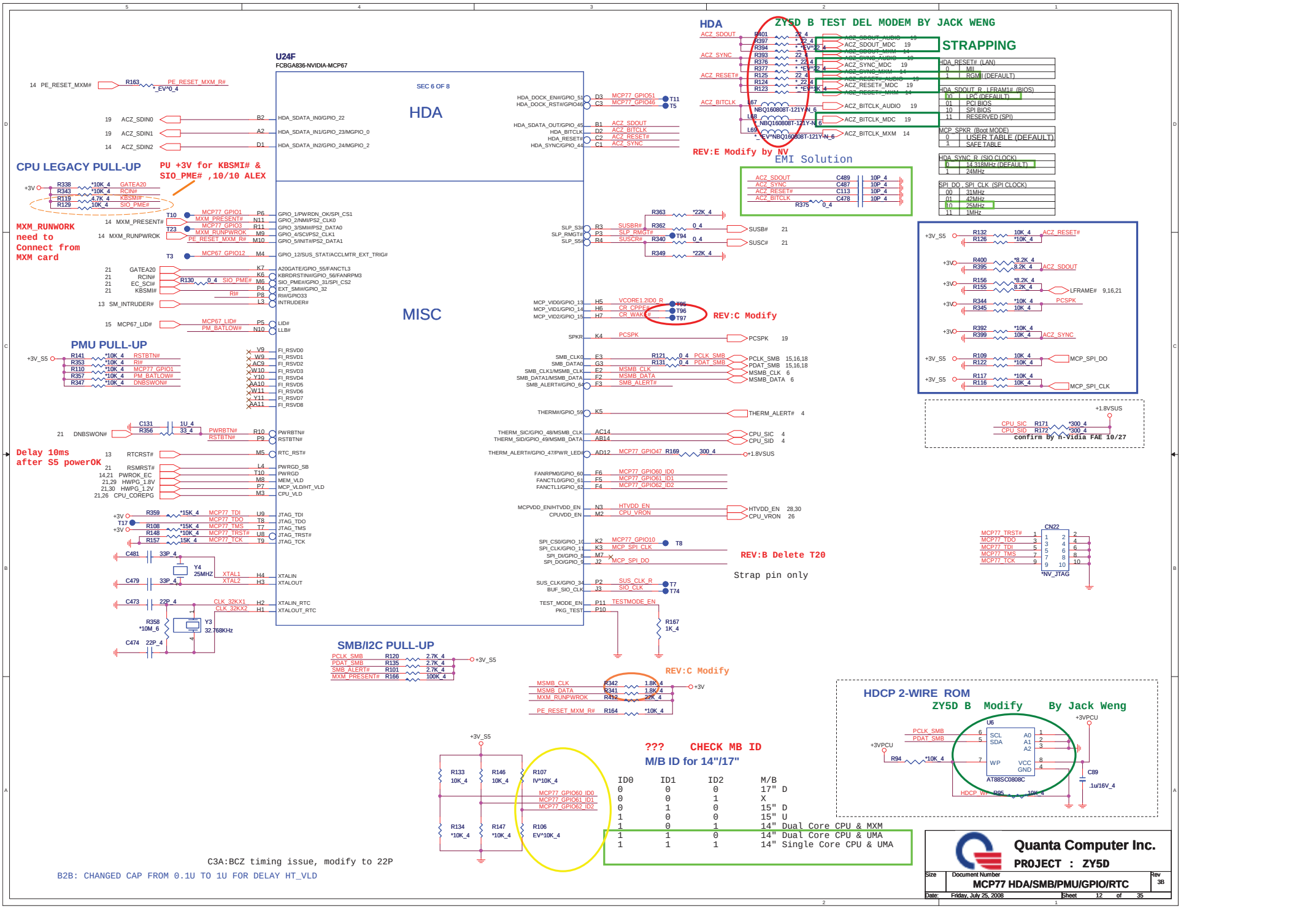
Size	Document Number	Rev
	MCP77 PCI/LPC/IDE	3B

Date: Wednesday, May 21, 2008 Sheet 9 of 35



Quanta Computer Inc.			
PROJECT : ZY5D			
Size	Document Number		Rev
	MCP77 LAN and Graphics		3B
Date: Wednesday, May 21, 2008		Sheet 10 of 35	


U24E
FCBGA836-NVIDIA-MCP67
SEC 5 OF 8
SATA
USB
[SATA HDD 1]
[SATA HDD 2]
[SATA ODD]
REV:B Modify
MINI CARD * 2
MINI CARD * 2
BLUETOOTH
REV:C Modify
INT LEFT USB 2
CARD READER
INT LEFT USB 1
Fingerprint
EXT USB * 2
Docking
CCD
EXT USB * 2
NEW CARD
USB PULL-DOWN
REV:B Swap Modify
REV:C Modify
80mA
5mA
20mA
60mA
320mA
18mA
405mA
REV:B Modify
845 Ohm for MCP77 checklist
Quanta Computer Inc.
PROJECT : ZY5D
MCP77 SATA and USB
Wednesday, May 21, 2008


HDA
ZY5D B TEST DEL MODEM BY JACK WENG
STRAPPING
U24F
FCBGA836-NVIDIA-MCP67
SEC 6 OF 8
HDA
MISC
CPU LEGACY PULL-UP
PU +3V for KBSMI# & SIO_PME# ,10/10 ALEX
MXM_RUNWORK need to Connect from MXM card
PMU PULL-UP
Delay 10ms after S5 powerOK
REV:E Modify by NV
EMI Solution
REV:C Modify
REV:B Delete T20
Strap pin only
SMB/I2C PULL-UP
HDCP 2-WIRE ROM
ZY5D B Modify By Jack Weng
??? CHECK MB ID
M/B ID for 14"/17"
ID0 ID1 ID2 M/B
0 0 0 17" D
0 0 1 X
0 1 0 15" D
1 0 0 15" U
1 0 1 14" Dual Core CPU & MXM
1 1 0 14" Dual Core CPU & UMA
1 1 1 14" Single Core CPU & UMA
confirm by n-Vidia FAE 10/27
C3A:BCZ timing issue, modify to 22P
B2B: CHANGED CAP FROM 0.1U TO 1U FOR DELAY HT_VLD
Quanta Computer Inc.
PROJECT : ZY5D
MCP77 HDA/SMB/PMU/GPIO/RTC
Size
Document Number
Rev 3B
Date: Friday, July 25, 2008
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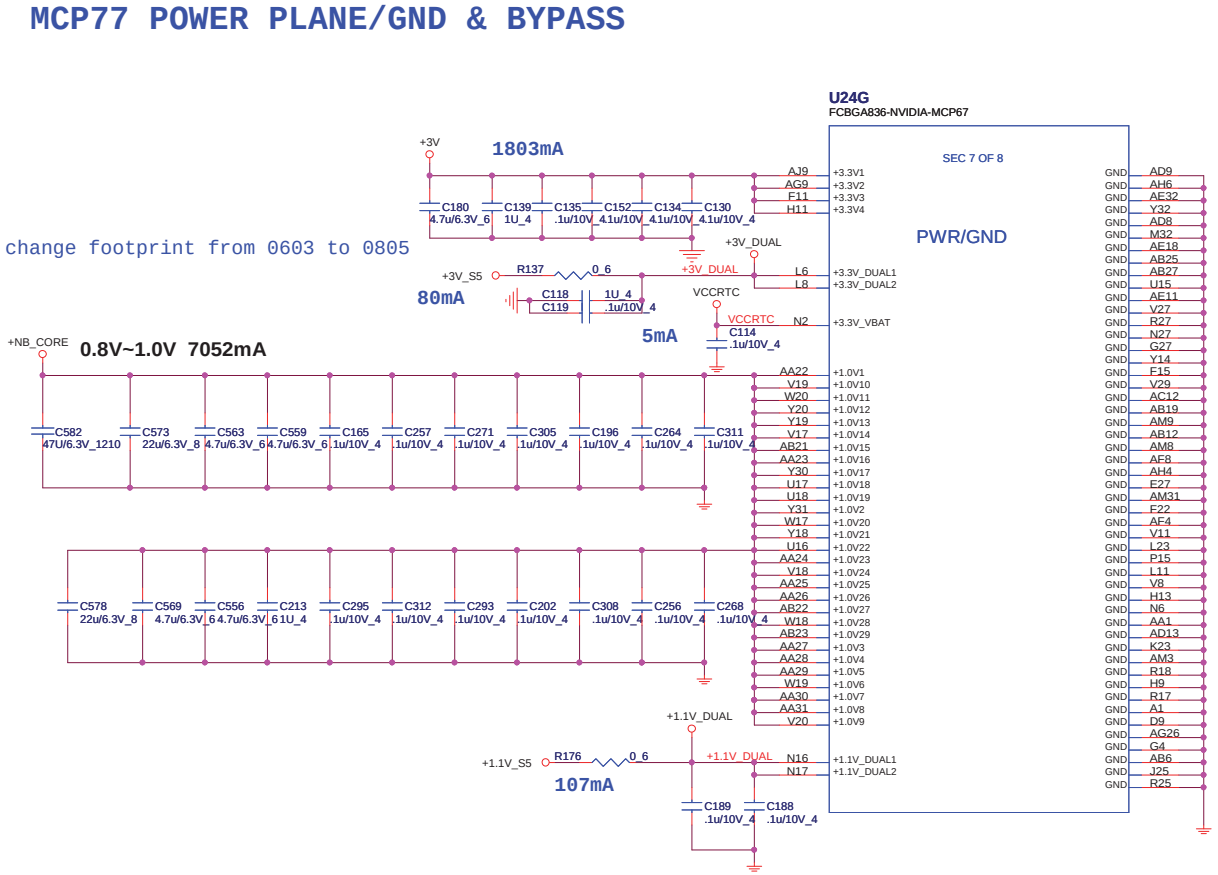
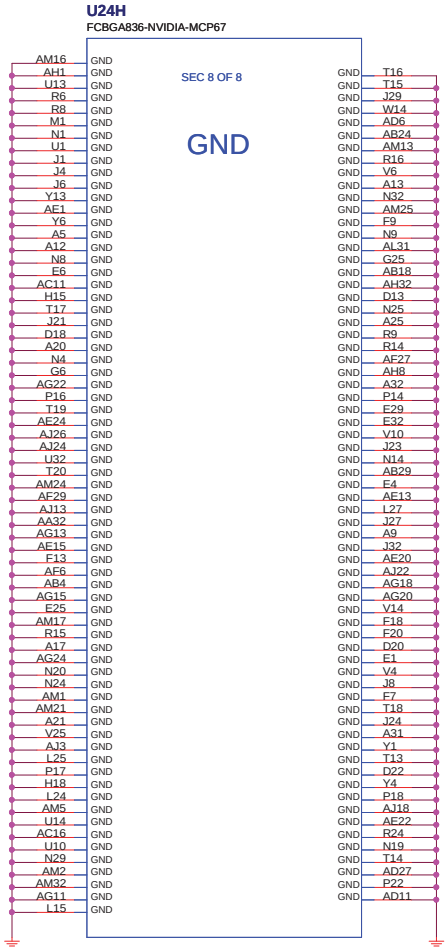
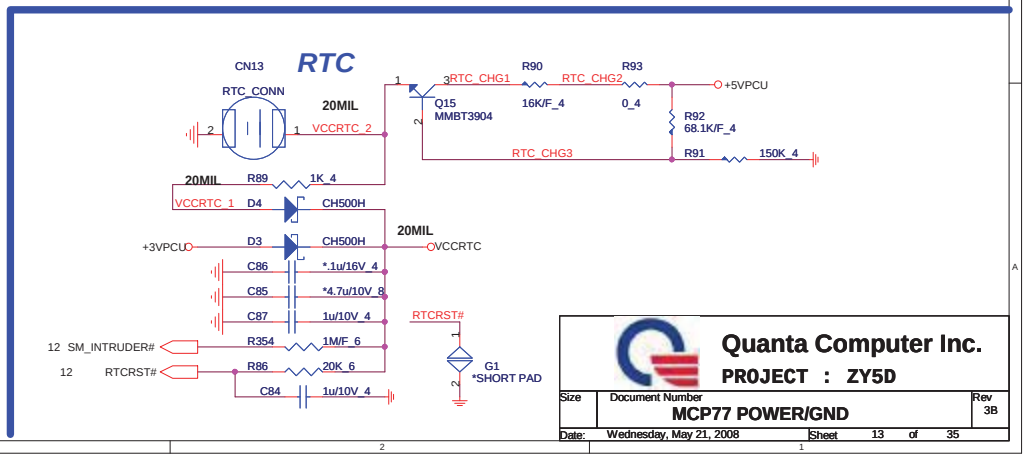
MCP77 POWER PLANE/GND & BYPASS





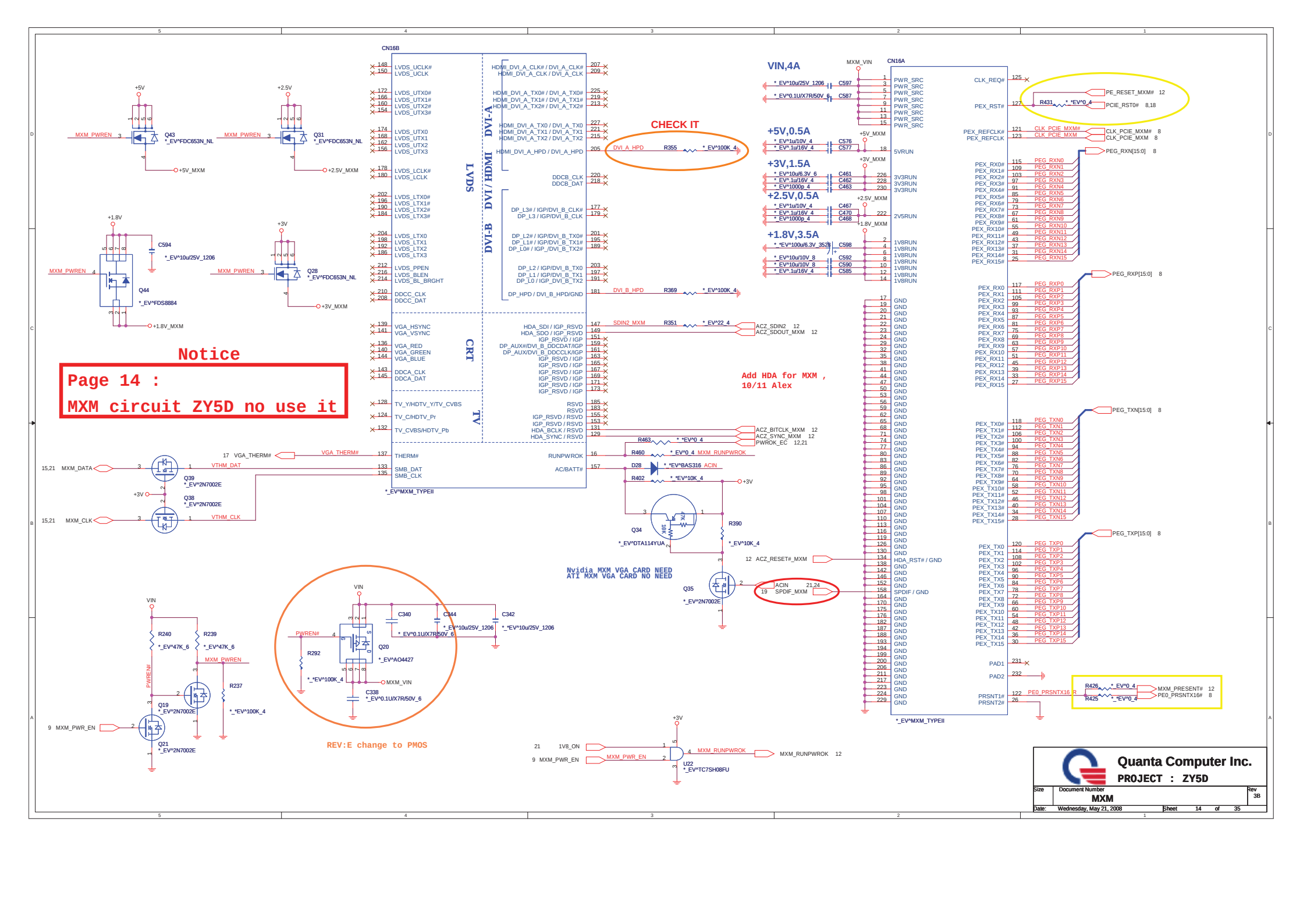


Quanta Computer Inc.

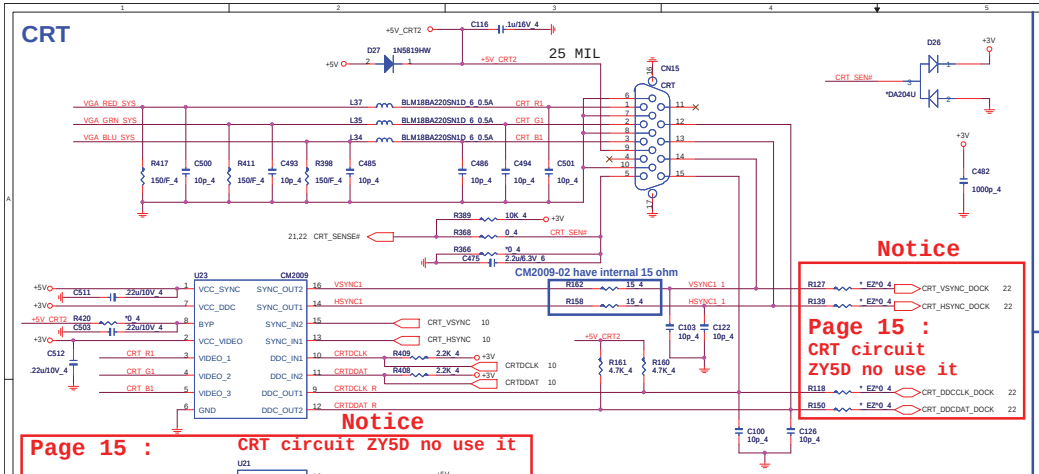
PROJECT : ZY5D

Size	Document Number	Rev
	MCP77 POWER/GND	3B

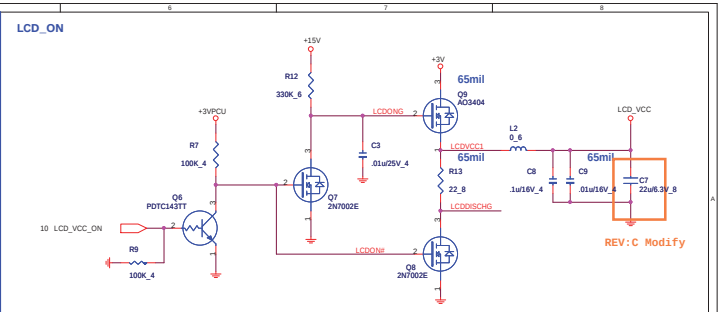
Date: Wednesday, May 21, 2008 Sheet 13 of 35


CN16B
LVDS
DVI-A
DVI / HDMI
DVI-B
CRT
TV
LVDS_UCLK#
LVDS_UCLK
LVDS_UTX0#
LVDS_UTX1#
LVDS_UTX2#
LVDS_UTX3#
LVDS_UTX0
LVDS_UTX1
LVDS_UTX2
LVDS_UTX3
LVDS_LCLK#
LVDS_LCLK
LVDS_LTX0#
LVDS_LTX1#
LVDS_LTX2#
LVDS_LTX3#
LVDS_LTX0
LVDS_LTX1
LVDS_LTX2
LVDS_LTX3
LVDS_PPEN
LVDS_BLEN
LVDS_BL_BRGHT
DDCC_CLK
DDCC_DAT
VGA_HSYNC
VGA_VSYNC
VGA_RED
VGA_GREEN
VGA_BLUE
DDCA_CLK
DDCA_DAT
TV_Y/HDTV_Y/TV_CVBS
TV_C/HDTV_Pr
TV_CVBS/HDTV_Pb
THERM#
SMB_DAT
SMB_CLK
HDMI_DVI_A_CLK# / DVI_A_CLK#
HDMI_DVI_A_CLK / DVI_A_CLK
HDMI_DVI_A_TX0# / DVI_A_TX0#
HDMI_DVI_A_TX1# / DVI_A_TX1#
HDMI_DVI_A_TX2# / DVI_A_TX2#
HDMI_DVI_A_TX0 / DVI_A_TX0
HDMI_DVI_A_TX1 / DVI_A_TX1
HDMI_DVI_A_TX2 / DVI_A_TX2
HDMI_DVI_A_HPD / DVI_A_HPD
DDCB_CLK
DDCB_DAT
DP_L3# / IGP/DVI_B_CLK#
DP_L3 / IGP/DVI_B_CLK
DP_L2# / IGP/DVI_B_TX0#
DP_L1# / IGP/DVI_B_TX1#
DP_L0# / IGP_/DVI_B_TX2#
DP_L2 / IGP/DVI_B_TX0
DP_L1 / IGP/DVI_B_TX1
DP_L0 / IGP_DVI_B_TX2
DP_HPD / DVI_B_HPD/GND
HDA_SDI / IGP_RSVD
HDA_SDO / IGP_RSVD
IGP_RSVD / IGP
DP_AUX#/DVI_B_DDCDAT/IGP
DP_AUX/DVI_B_DDCCLK/IGP
RSVD
RSVD / RSVD
IGP_RSVD / RSVD
HDA_BCLK / RSVD
HDA_SYNC / RSVD
RUNPWROK
AC/BATT#
*_EV^MXM_TYPEII
CHECK IT
DVI_A_HPD
R355
*_EV^100K_4
DVI_B_HPD
R369
SDIN2_MXM
R351
*_EV^22_4
ACZ_SDIN2
ACZ_SDOUT_MXM
ACZ_BITCLK_MXM
ACZ_SYNC_MXM
PWROK_EC
R463
*_EV^0_4
R460
MXM_RUNPWROK
D28
*_EV^BAS316
ACIN
R402
*_EV^10K_4
+3V
Q34
*_EV^DTA114YUA
R390
Q35
*_EV^2N7002E
ACZ_RESET#_MXM
HDA_RST# / GND
SPDIF_MXM
SPDIF / GND
Add HDA for MXM , 10/11 Alex
Nvidia MXM VGA CARD NEED
ATI MXM VGA CARD NO NEED
VIN,4A
MXM_VIN
*_EV^10u/25V_1206
C597
*_EV^0.1U/X7R/50V_6
C587
+5V,0.5A
+5V_MXM
*_EV^1u/10V_4
C576
*_EV^1u/16V_4
C577
5VRUN
+3V,1.5A
+3V_MXM
*_EV^10u/6.3V_6
C461
*_EV^1u/16V_4
C462
*_EV^1000p_4
C463
3V3RUN
+2.5V,0.5A
+2.5V_MXM
*_EV^1u/10V_4
C467
*_EV^1u/16V_4
C470
*_EV^1000p_4
C468
2V5RUN
+1.8V,3.5A
+1.8V_MXM
*_EV^100u/6.3V_3528
C598
*_EV^10u/10V_8
C592
*_EV^1u/16V_4
C590
C585
1V8RUN
CN16A
PWR_SRC
GND
CLK_REQ#
PEX_RST#
PE_RESET_MXM#
R431
*_EV^0_4
PCIE_RST0#
PEX_REFCLK#
PEX_REFCLK
CLK_PCIE_MXM#
CLK_PCIE_MXM
PEG_RXN[15:0]
PEG_RXP[15:0]
PEG_TXN[15:0]
PEG_TXP[15:0]
PAD1
PAD2
PRSNT1#
PRSNT2#
PE0_PRSNTX16_R
R426
R425
MXM_PRESENT#
PE0_PRSNTX16#
*_EV^MXM_TYPEII
+5V
+2.5V
+1.8V
+3V
MXM_PWREN
Q43
*_EV^FDC653N_NL
Q31
*_EV^FDC653N_NL
+5V_MXM
+2.5V_MXM
C594
*_EV^10u/25V_1206
Q44
*_EV^FDS8884
Q28
*_EV^FDC653N_NL
+3V_MXM
+1.8V_MXM
Notice
Page 14 :
MXM circuit ZY5D no use it
15,21 MXM_DATA
15,21 MXM_CLK
VGA_THERM#
VTHM_DAT
VTHM_CLK
Q39
*_EV^2N7002E
Q38
*_EV^2N7002E
VIN
R240
R239
*_EV^47K_6
MXM_PWREN
R237
*_EV^100K_4
PWREN#
Q19
*_EV^2N7002E
Q21
*_EV^2N7002E
9 MXM_PWR_EN
C340
C344
C342
*_EV^0.1U/X7R/50V_6
*_EV^10u/25V_1206
PWREN#
R292
Q20
*_EV^AO4427
*_EV^100K_4
MXM_VIN
C338
*_EV^0.1U/X7R/50V_6
REV:E change to PMOS
21 1V8_ON
9 MXM_PWR_EN
MXM_RUNPWROK
U22
*_EV^TC7SH08FU
Quanta Computer Inc.
PROJECT : ZY5D
Size
Document Number
MXM
Rev
3B
Date: Wednesday, May 21, 2008
Sheet 14 of 35

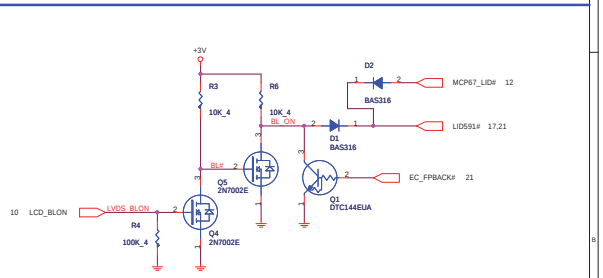
CRT



LCD_ON

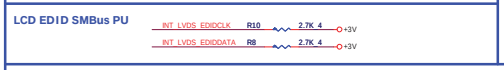


Backlight Control

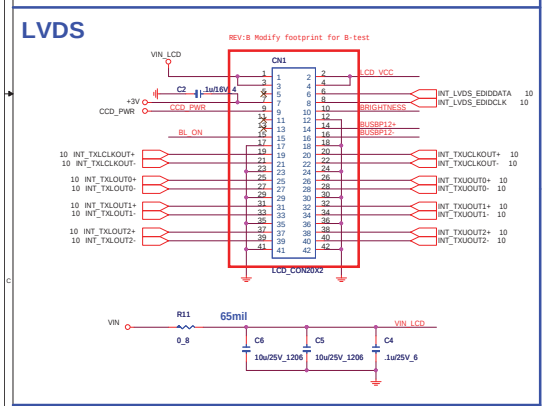


BRIGHTNESS

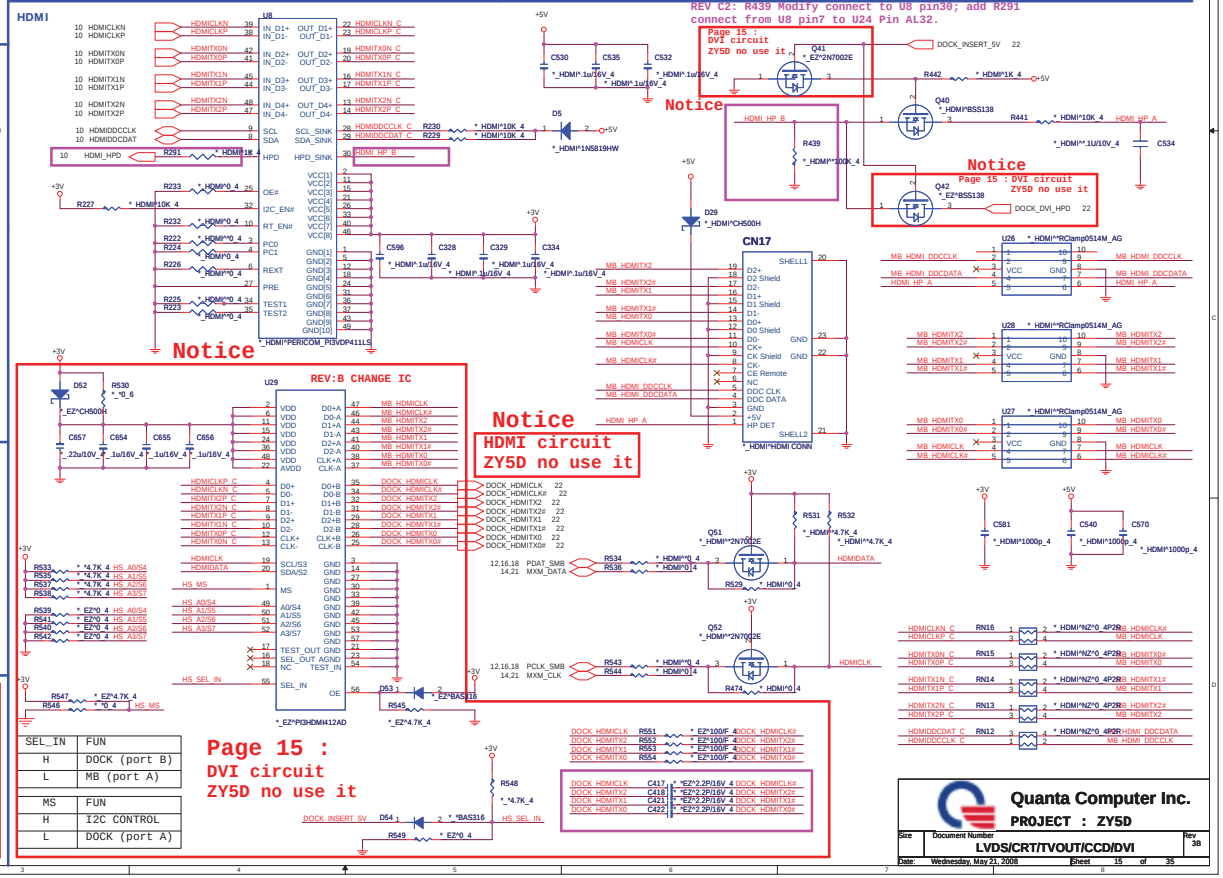
LCD EDID SMBus PU



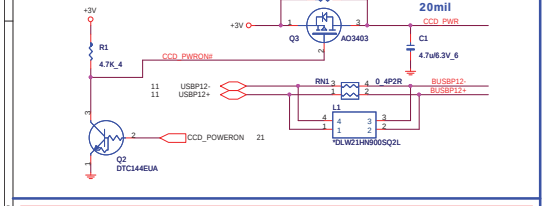
LVDS



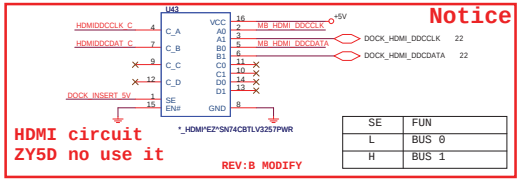
HDMI



Camera



HDMI circuit ZY5D no use it



SE	FUN
L	BUS 0
H	BUS 1

SEL_IN	FUN
H	DOCK (port B)
L	MB (port A)

MS	FUN
H	I2C CONTROL
L	DOCK (port A)

Quanta Computer Inc.
PROJECT : ZY5D
Size | Document Number: LVDS/CRT/TVOUT/CCD/DVI | Rev 3B
Date: Wednesday, May 21, 2008 | Sheet 15 of 35

To NEW-CARD & EXT. USB

650mA 2A 1.3A 275mA

+1.5V +5VPCU +3V +3V_S5

CN8

NEW^NEW CARD_CON20X2

PDAT_SMB PCLK_SMB USBON# USBP14- USBP14+ USBP13- USBP13+ USBP10- USBP10+

PCIE_RST1# CPPE# NEW_CLKREQ# CLK_PCIE_NEW_C# CLK_PCIE_NEW_C PCIE_RXN5 PCIE_RXP5 PCIE_TXN5 PCIE_TXP5

REV:B Modify footprint for B-test

21 CPPE#_EC R261 CPPE# *_NEW^0_4

REV:B Modify

+3V C383 *_NEW^4.7u/6.3V_6 C381 *_NEW^1u/10V_4 C382 *_NEW^.1u/16V_4

Fingerprint

REV:C2 Modify

+3VSUS +3V R17 * FP^0_6 R25 * FP^0_6 CN7

RN11 * FP^0_4P2R L22 *_FP^DLW21HN900SQ2L

USBP9- USBP9+ BUSBP9- BUSBP9+ *_FP^Finger_H1.95

Notice

Page 16 :
NEW CARD circuit ZY5D no use it
Finger print circuit ZY5D no use it

Bluetooth

Notice

Page 16 :
B/T circuit ZY5D no use it

+3VSUS Q25 *_BT^AO3403 BT_POWER 20mil C441 *_BT^4.7u/6.3V_6 CN10

21 BT_POWERON#

RN19 * BT^0_4P2R L31 *_BT^USB_BT_5P

USBP2+ USBP2- BUSBP2+ BUSBP2-

17 BT_LED * BT^^DLW21HN900SQ2L

CIR

Notice

Page 16 :
CIR circuit ZY5D no use it

+3VPCU +5VPCU R513 *_CIR^47_6 R512 *_CIR^47_6 U34 CIR_VCC C649 *_CIR^.1u/25V_6 *_CIR^CIR

Q50 OE# VCC A GND *_CIR^^NC7SZ125P5X CIRRX2_1 CIRRX2 21 R514 *_CIR^0_4

INT. USB

USBPWRP1 60mil L24 TI201209G121_8_3A

RN17 *0_4P2R L23 DLW21HN900SQ2L USBP7- USBP7+ BUSBP7- BUSBP7+

REV:C Modify

C586 470p_4 C579 330u/6.3V_6X5.7 SYUIN_USB

C341 10u/10V_8 C339 1u/10V_4 U9 RT9711BPF IN1 IN2 OUT1 OUT2 OUT3 EN# GND GND-C OC# USBON# R238 *6.34K/F_4 60mil USBPWR1

RN18 *0_4P2R L25 DLW21HN900SQ2L USBP5- USBP5+ BUSBP5- BUSBP5+

CN20 USBPWRP1 C343 470p_4 SYUIN_USB

BUSBP7+ D47 BUSBP7- D48 BUSBP5+ D49 BUSBP5- D50 MLVG06031R

REV:C Modify

MINI-CARD

Notice

CN33

+3V_MINI R522 * MINI^0_8 +3V_MINI_A +3V_MINI_B R523 0_8 +3V_MINI

RF_LED# R524 *_MINI^0_4 RF_LED#_A RF_LED#_B R306 0_4 RF_LED# 17

USBP1+ USBP1- R325 R321 USBP1+_C USBP1-_C USBP0+_C USBP0-_C R516 R517 USBP0+ 11 USBP0- 11

MINI_SMDATA MINI_SMCLK PCIE_TXP2 PCIE_TXN2 PCIE_RXP2 PCIE_RXN2 PCIE_RST1# CLK_PCIE_TV TV_CLKREQ# PCIE_TXP1 PCIE_TXN1 PCIE_RXP1 PCIE_RXN1 PCIE_RST1# CLK_PCIE_MINI CLK_PCIE_MINI# MINI_CLKREQ#

PCIE_WAKE_WL_R_# R525 0_4 WAKE_WL_A# WAKE_WL_B# R526 *_MINI^0_4 PCIE_WAKE_WL_R_#

ZY5D A modify Jack W

+1.5V

LFRAME# LAD3 LAD2 LAD1 LAD0 R299 R294 R300 R295 R301 * MINI^0_4

Debug

LPC_RST_EC# LPC_CLK_DEBUG1 R507 R506 *0_4

TV use +3V

+3V_MINI R508 * MINI^0_6 +3V_MINI_R_A +3V_MINI_R_B R578 +3V_MINI C645 *_MINI^.1u/16V_4 C659 *_MINI^.1u/16V_4

TV use +5V

RF_EN R579 * MINI^0_4 A_RF_EN +5V_TV-CARD R510 * MINI^0_6 +5V_TV-CARD_R_A +5V_TV-CARD_R_B R581 *_MINI^0_6 +5V_TV-CARD

A_W_DISABLE# B_W_DISABLE# B_RF_EN R580 0_4 RF_EN 21

A_BT_CHCLK A_BT_DATA B_BT_CHCLK B_BT_DATA

GND

SP@QUASAR-CA0404-092N21_92P

Page 16 :
DUAL MINI CARD circuit ZY5D no use it

REV:C Modify

+3V for WWAN card is 2.75A

+3V R298 0_8 +3V_MINI C431 C433 C428 C429 4.7u/6.3V_6

+3V_MINI_B C437 C426 C434 .1u/16V_4

+3V_MINI_A C652 C651 C653 .1u/16V_4

REV:B Modify

Notice

+1.5V +5V C435 C436 C425 .1u/16V_4 4.7u/6.3V_6 R509 * MINI^0_6 +5V_TV-CARD C646 C647 *_MINI^4.7u/6.3V_6 *_MINI^.1u/16V_4

500mA, 25mil

Page 16 :
DUAL MINI CARD circuit
ZY5D no use it

+3VSUS Q26 *DTC144EUA R314 4.7K_4 8,18,21 PCIE_WAKE#

12,15,18 PDAT_SMB Q23 2N7002E R302 10K_4 R296 *0_4 MINI_SMDATA

12,15,18 PCLK_SMB Q24 2N7002E R303 10K_4 R297 *0_4 MINI_SMCLK

ZY5D B test has modified to single stack
no TV card, only Wireless card

CAPACITOR on Module

MODULE 'A' TV card

MODULE 'B' Wireless card

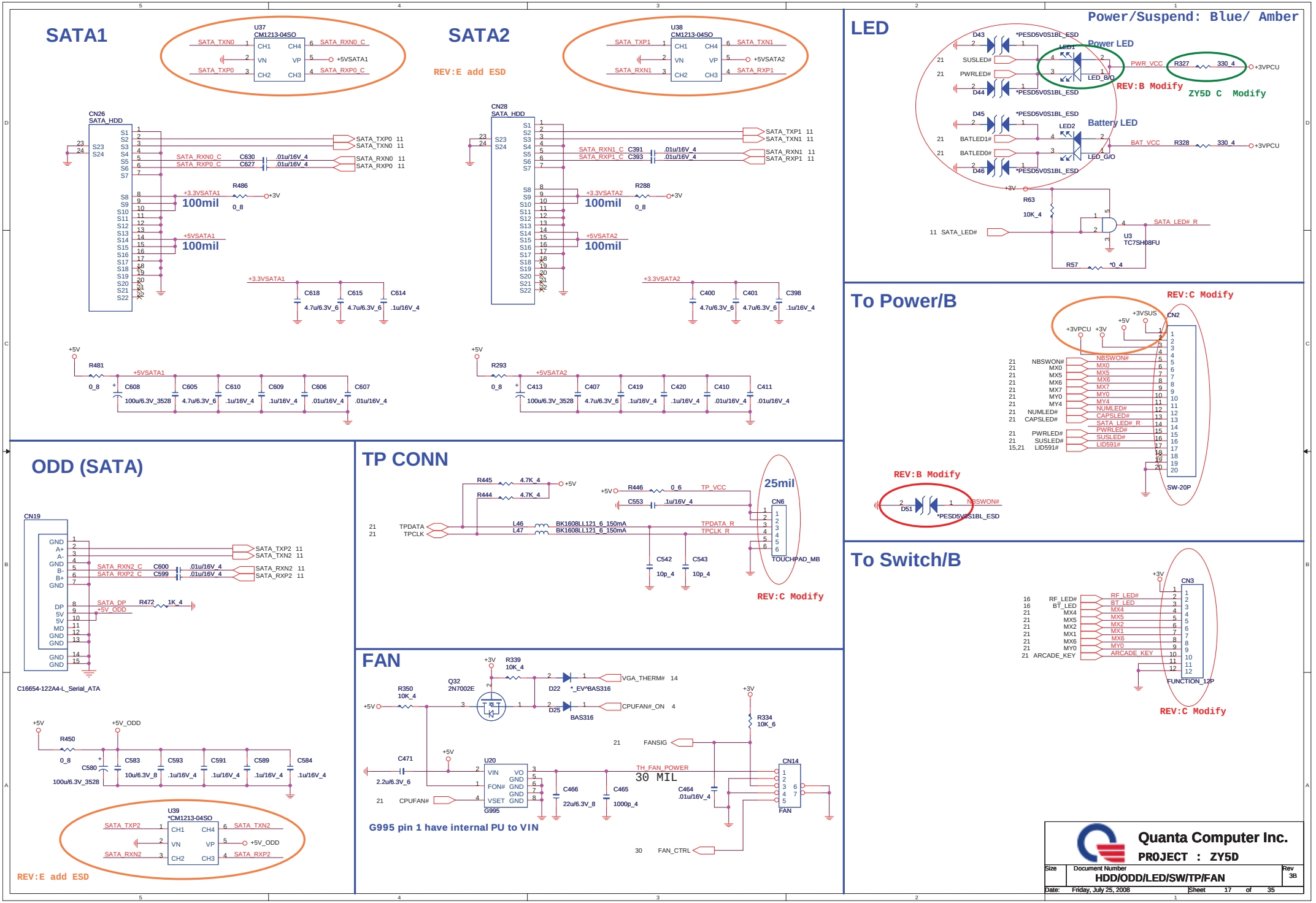
Double Stack MINI CARD

C648 *10P_4 R511 *22_4 LPC_CLK_DEBUG1 For EMI

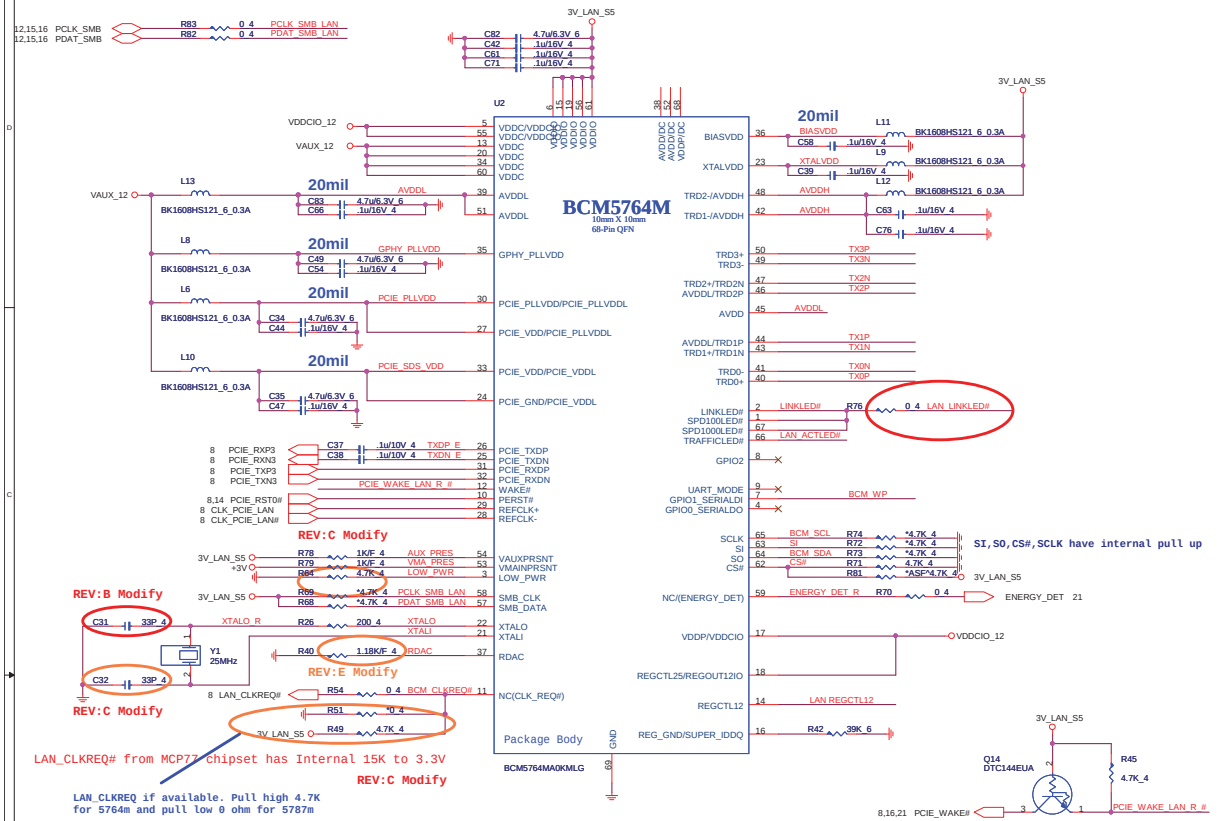
Quanta Computer Inc.

PROJECT : ZY5D

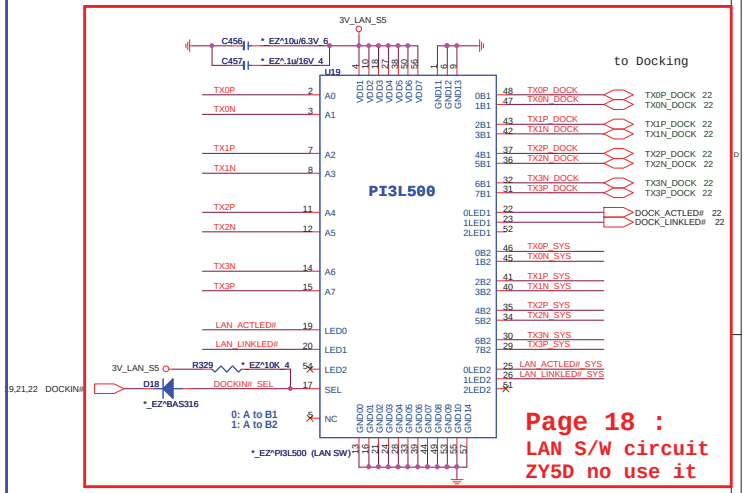
Size	Document Number	Rev
	NEW&MINI&TV CARD/USB/BT/CIR	3B
Date: Thursday, July 24, 2008	Sheet 16 of 35	


SATA1
U37
CM1213-04SO
SATA_TXN0
SATA_TXP0
SATA_RXN0_C
SATA_RXP0_C
+5VSATA1
CN26
SATA_HDD
SATA_RXN0_C
SATA_RXP0_C
C630
C627
.01u/16V_4
SATA_TXP0 11
SATA_TXN0 11
SATA_RXN0 11
SATA_RXP0 11
+3.3VSATA1
100mil
R486
0_8
+3V
+5VSATA1
100mil
C618
C615
C614
4.7u/6.3V_6
.1u/16V_4
+5V
R481
C608
100u/6.3V_3528
C605
C610
C609
C606
C607
SATA2
REV:E add ESD
U38
CM1213-04SO
SATA_TXP1
SATA_RXN1
SATA_TXN1
SATA_RXP1
+5VSATA2
CN28
SATA_HDD
SATA_RXN1_C
SATA_RXP1_C
C391
C393
SATA_TXP1 11
SATA_TXN1 11
SATA_RXN1 11
SATA_RXP1 11
+3.3VSATA2
100mil
R288
+5VSATA2
100mil
C400
C401
C398
R293
C413
C407
C419
C420
C410
C411
LED
Power/Suspend: Blue/ Amber
D43
D44
D45
D46
*PESD5V0S1BL_ESD
Power LED
LED1
SUSLED#
PWRLED#
PWR_VCC
R327
330_4
+3VPCU
LED_B/O
REV:B Modify
ZY5D C Modify
Battery LED
LED2
BATLED1#
BATLED0#
BAT_VCC
R328
LED_G/O
R63
10K_4
SATA_LED#
SATA_LED# R
U3
TC7SH08FU
R57
*0_4
To Power/B
REV:C Modify
CN2
+3VPCU
+3V
+5V
+3VSUS
NBSWON#
MX0
MX5
MX6
MX7
MY0
MY4
NUMLED#
CAPSLED#
SATA_LED# R
PWRLED#
SUSLED#
LID591#
SW-20P
REV:B Modify
D51
*PESD5V0S1BL_ESD
To Switch/B
CN3
RF_LED#
BT_LED
MX4
MX5
MX2
MX1
MX6
MY0
ARCADE_KEY
FUNCTION_12P
REV:C Modify
ODD (SATA)
CN19
C16654-122A4-L_Serial_ATA
SATA_TXP2 11
SATA_TXN2 11
SATA_RXN2 11
SATA_RXP2 11
SATA_DP
+5V_ODD
R472
1K_4
R450
C580
C583
C593
C591
C589
C584
10u/6.3V_8
U39
*CM1213-04SO
SATA_TXP2
SATA_RXN2
SATA_TXN2
SATA_RXP2
REV:E add ESD
TP CONN
R445
R444
4.7K_4
R446
0_6
TP_VCC
C553
.1u/16V_4
25mil
CN6
TOUCHPAD_MB
TPDATA
TPCLK
L46
L47
BK1608LL121_6_150mA
TPDATA_R
TPCLK_R
C542
C543
10p_4
REV:C Modify
FAN
R339
10K_4
Q32
2N7002E
R350
10K_4
D22
*_EV^BAS316
D25
BAS316
VGA_THERM# 14
CPUFAN#_ON 4
R334
10K_6
FANSIG
C471
2.2u/6.3V_6
U20
G995
VIN
VO
FON#
VSET
GND
CPUFAN#
C466
22u/6.3V_8
C465
1000p_4
TH_FAN_POWER
30 MIL
C464
.01u/16V_4
CN14
FAN
FAN_CTRL
G995 pin 1 have internal PU to VIN
Quanta Computer Inc.
PROJECT : ZY5D
Size
Document Number
HDD/ODD/LED/SW/TP/FAN
Rev
3B
Date: Friday, July 25, 2008
Sheet 17 of 35

Giga LAN BCM5787M/5764M



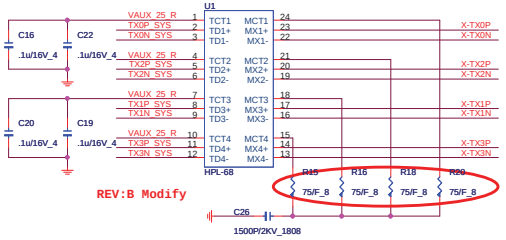
LAN SWITCH



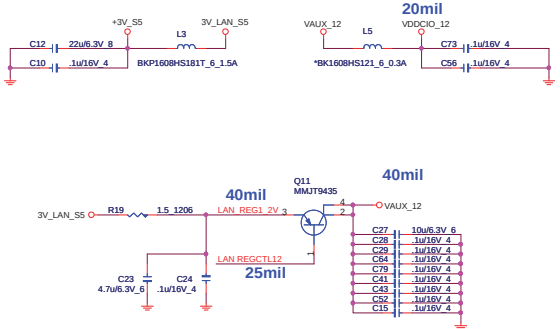
Transfomer

Source 1: DELTA LFE9249 DB0ZR1LAN11

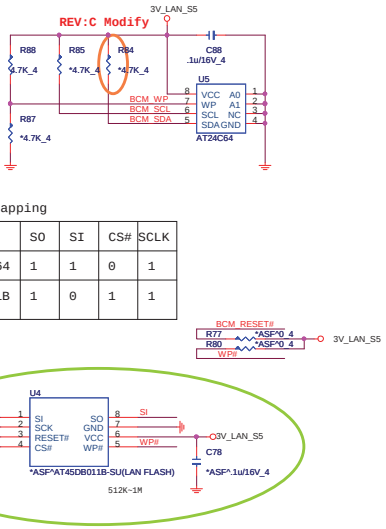
Source 2: Bothand GST5009 DBKN1NLAN03



LAN POWER



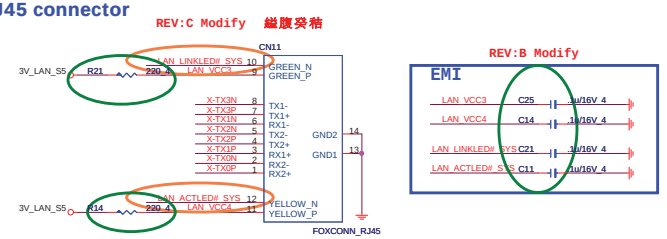
EEPROM



EEPROM Strapping

	SO	SI	CS#	SCLK
24c64	1	1	0	1
AT45DB011B	1	0	1	1

RJ45 connector

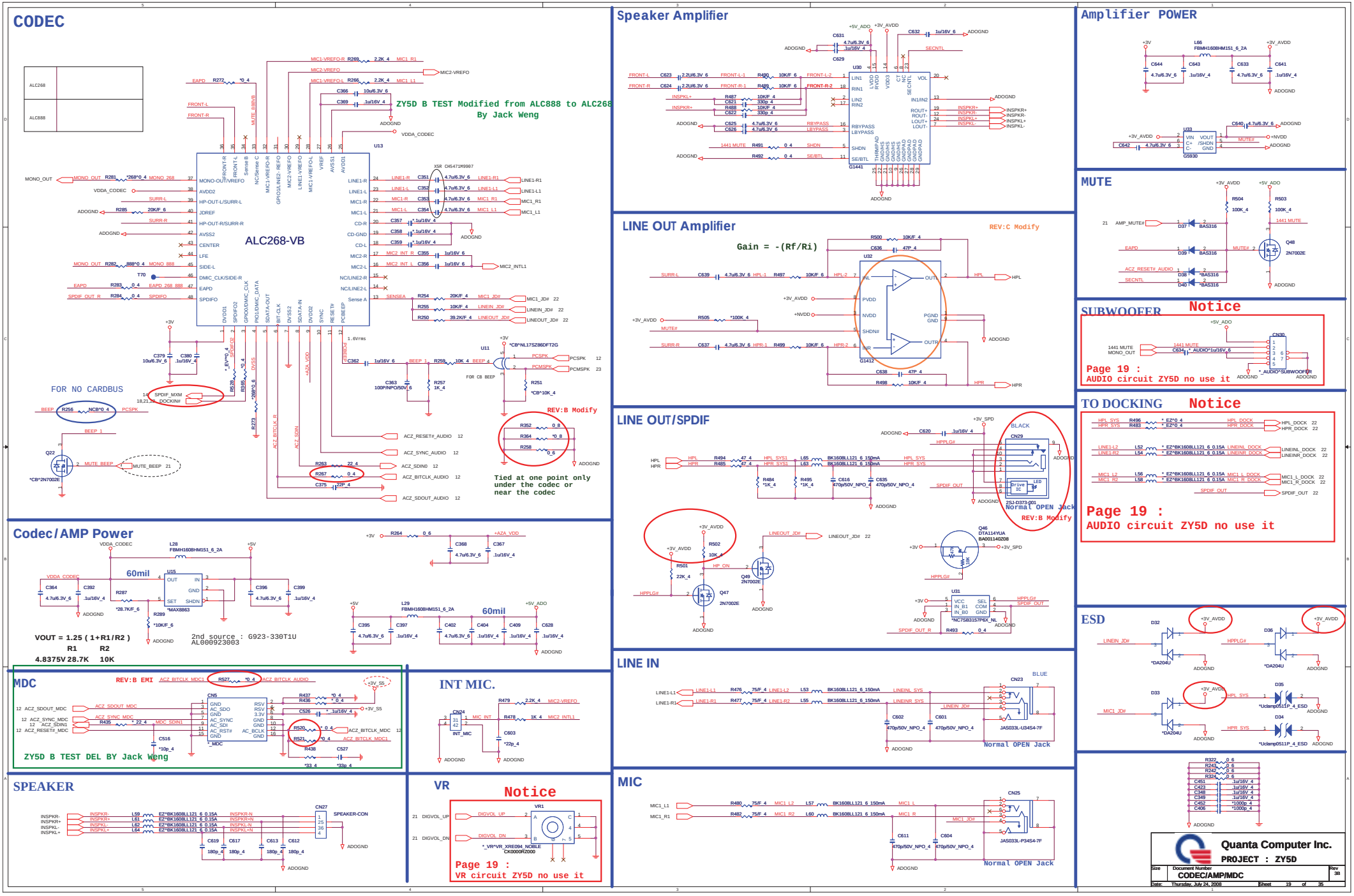


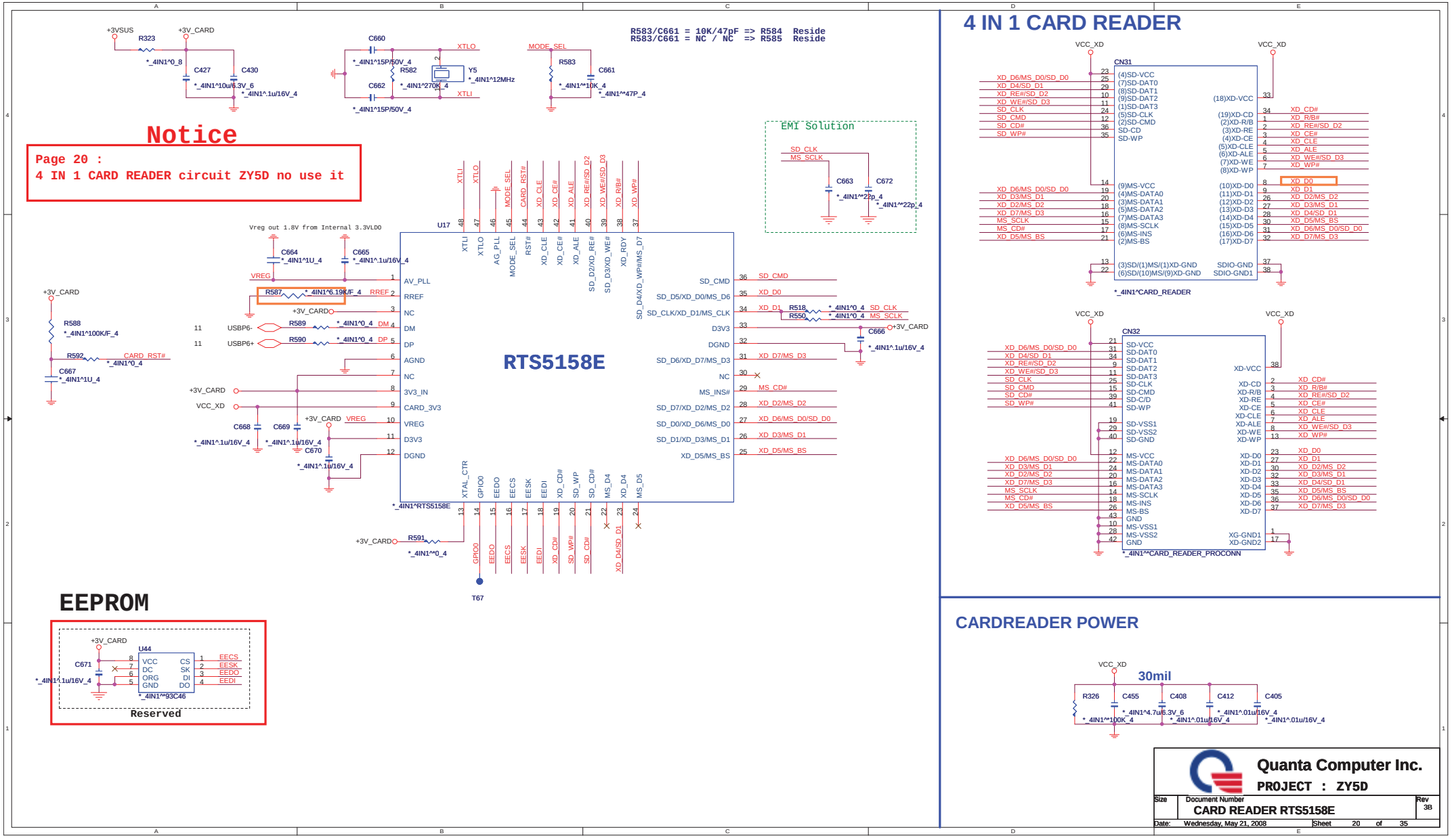
ZY5D C TEST Modified footprint from 0402 to 0805
to solve Lan burnt issue on Acer project
By Jack Weng

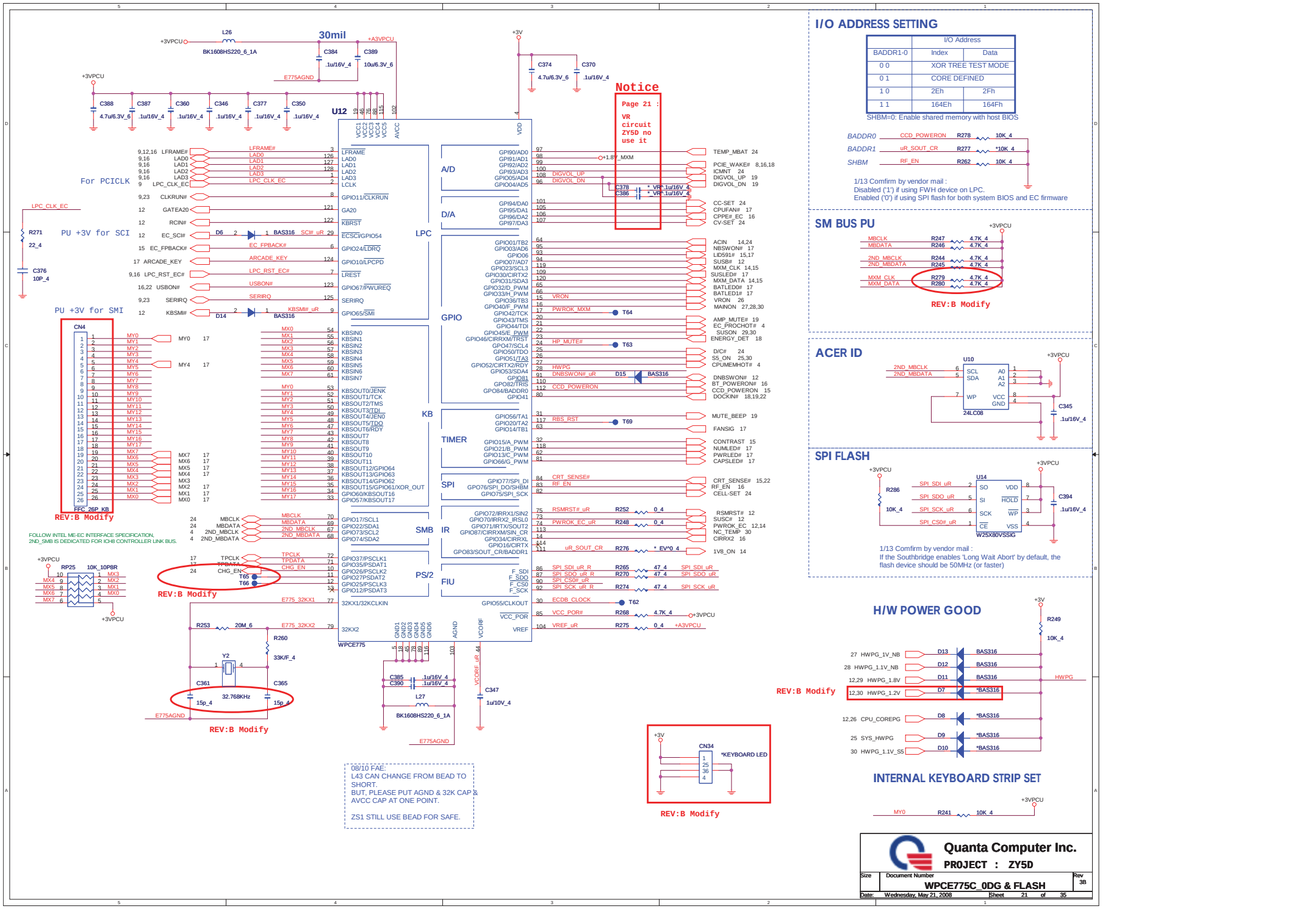
Quanta Computer Inc.
PROJECT : ZY5D

Size	Document Number	Rev
	GigaLAN BCM5787M/5764M & RJ45	3B

Date: Thursday, July 24, 2008 Sheet 18 of 35


CODEC
ALC268-VB
ZY5D B TEST Modified from ALC888 to ALC268
By Jack Weng
FOR NO CARDBUS
REV:B Modify
Tied at one point only
under the codec or
near the codec
Codec/AMP Power
VOUT = 1.25 (1+R1/R2)
R1 R2
4.8375V 28.7K 10K
2nd source : G923-330T1U
AL000923003
MDC
REV:B EMI
ZY5D B TEST DEL BY Jack Weng
SPEAKER
INT MIC.
VR
Notice
Page 19 :
VR circuit ZY5D no use it
Speaker Amplifier
LINE OUT Amplifier
Gain = -(Rf/Ri)
REV:C Modify
LINE OUT/SPDIF
Normal OPEN Jack
REV:B Modify
LINE IN
MIC
Amplifier POWER
MUTE
SUBWOOFER
Notice
Page 19 :
AUDIO circuit ZY5D no use it
TO DOCKING
Notice
Page 19 :
AUDIO circuit ZY5D no use it
ESD
Quanta Computer Inc.
PROJECT : ZY5D
CODEC/AMP/MDC
Thursday, July 24, 2008
Sheet 19 of 35


R583/C661 = 10K/47pF => R584 Reside
R583/C661 = NC / NC => R585 Reside
Notice
Page 20 :
4 IN 1 CARD READER circuit ZY5D no use it
EMI Solution
RTS5158E
EEPROM
Reserved
4 IN 1 CARD READER
CARDREADER POWER
30mil
Quanta Computer Inc.
PROJECT : ZY5D
CARD READER RTS5158E
Wednesday, May 21, 2008
Sheet 20 of 35


30mil
U12
WPCE775
Notice
Page 21 :
VR circuit ZY5D no use it
For PCICLK
PU +3V for SCI
PU +3V for SMI
REV:B Modify
FOLLOW INTEL ME-EC INTERFACE SPECIFICATION, 2ND_SMB IS DEDICATED FOR ICH8 CONTROLLER LINK BUS.
08/10 FAE:
L43 CAN CHANGE FROM BEAD TO SHORT.
BUT, PLEASE PUT AGND & 32K CAP & AVCC CAP AT ONE POINT.
ZS1 STILL USE BEAD FOR SAFE.
I/O ADDRESS SETTING
I/O Address
BADDR1-0
Index
Data
0 0
XOR TREE TEST MODE
0 1
CORE DEFINED
1 0
2Eh
2Fh
1 1
164Eh
164Fh
SHBM=0: Enable shared memory with host BIOS
1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware
SM BUS PU
ACER ID
SPI FLASH
1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)
H/W POWER GOOD
INTERNAL KEYBOARD STRIP SET
Quanta Computer Inc.
PROJECT : ZY5D
WPCE775C_0DG & FLASH
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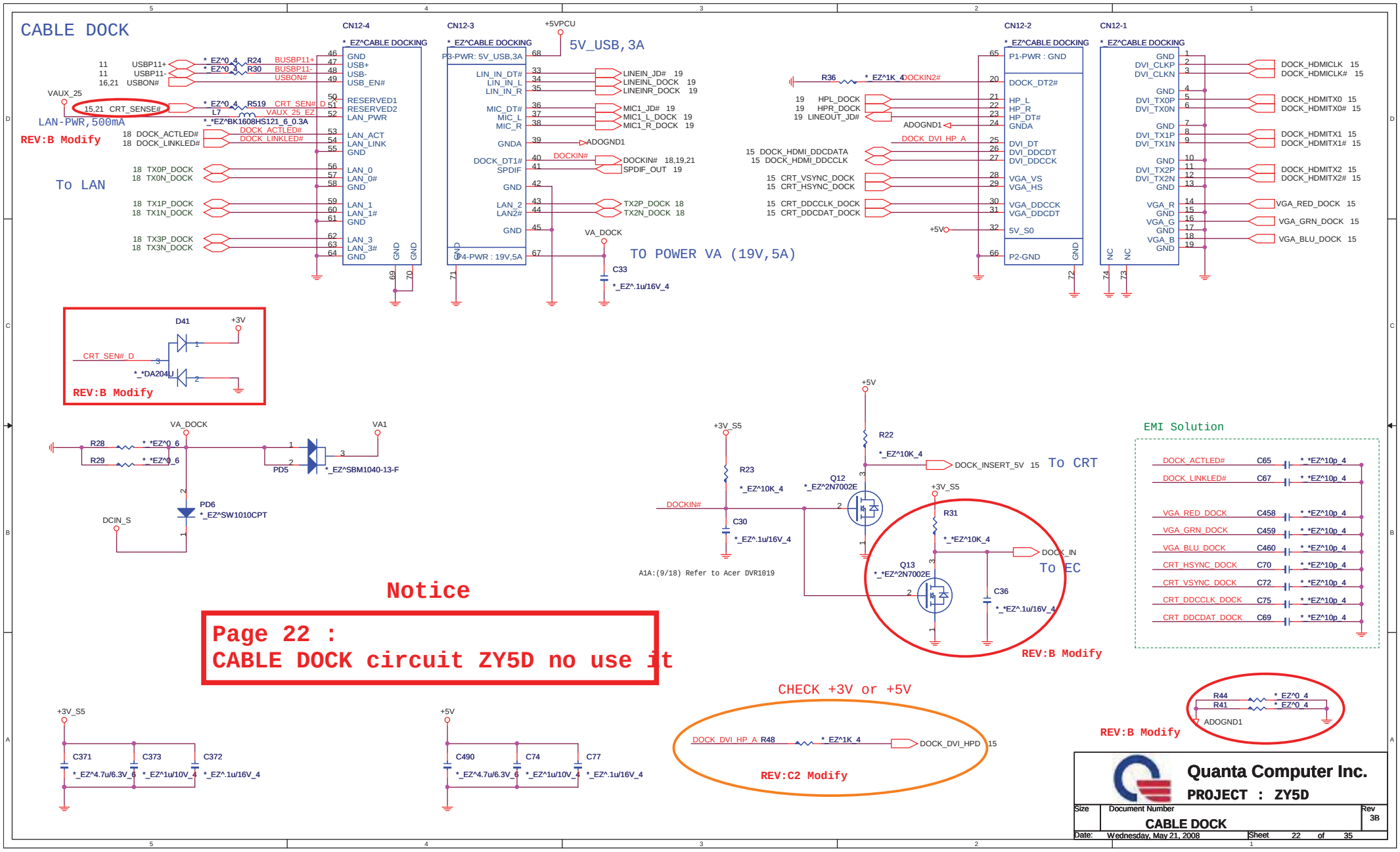
CABLE DOCK
CN12-4
CN12-3
CN12-2
CN12-1
* EZ^CABLE DOCKING
5V_USB, 3A
+5VPCU
VAUX_25
LAN-PWR,500mA
REV:B Modify
To LAN
TO POWER VA (19V,5A)
D41
+3V
CRT_SEN# D
*_*DA204U
REV:B Modify
VA_DOCK
VA1
PD5
*_EZ^SBM1040-13-F
PD6
*_EZ^SW1010CPT
DCIN_S
+3V_S5
+5V
DOCKIN#
Q12
Q13
*_EZ^2N7002E
DOCK_INSERT_5V
To CRT
DOCK_IN
To EC
A1A:(9/18) Refer to Acer DVR1019
REV:B Modify
EMI Solution
Notice
Page 22 :
CABLE DOCK circuit ZY5D no use it
CHECK +3V or +5V
DOCK_DVI_HP_A R48
DOCK_DVI_HPD
REV:C2 Modify
REV:B Modify
ADOGND1
Quanta Computer Inc.
PROJECT : ZY5D
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NOTE: IDSEL SELECTION!

THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME.
IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE
PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE
REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO
SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS.
THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS
FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY
CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST
BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

VCC5# (124)	VPP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	PIN 127

AD20 R309 *CB^100/F_4 PCM_IDSEL

ID Select : AD20
Interrupt Pin : INTA#
Request Indicate : REQ0#
Grant Indicate : GNT0#

For EMI

PCLK_PCM — R290 *CB^22_4 — C414 *CB^22p_4

IDSEL SELECT POWER-ON-STRAPPING (SEE NOTE & TABLE FOR OPTIONS)

+3V — C415 *CB^4.7u/6.3V_6, C416 *CB^.1u/16V_4, C403 *CB^.1u/16V_4, C439 *CB^.1u/16_4

R313 *CB^33K/F_6 — VPPD0
R312 *CB^33K/F_6 — VCCD0, VCCD1

U16 *CB^OZ601T

64	CORE_VCC	VCC5#/VCCD0#/SDATA	124
77	CORE_VCC	VCC3#/VCCD1#/SCLK	125
97	CORE_VCC	VPP_PGM/VPPD0/SLATCH	123
115	CORE_VCC		
1	PCI_VCC		
20	PCI_VCC		
33	PCI_VCC		

9 AD[31..0]

AD31	4	AD31	CAD31	103	A_CAD31
AD30	5	AD30	CAD30	102	A_CAD30
AD29	6	AD29	CAD29	101	A_CAD29
AD28	7	AD28	CAD28	100	A_CAD28
AD27	8	AD27	CAD27	99	A_CAD27
AD26	9	AD26	CAD26	110	A_CAD26
AD25	10	AD25	CAD25	109	A_CAD25
AD24	13	AD24	CAD24	108	A_CAD24
AD23	14	AD23	CAD23	106	A_CAD23
AD22	15	AD22	CAD22	105	A_CAD22
AD21	16	AD21	CAD21	104	A_CAD21
AD20	17	AD20	CAD20	118	A_CAD20
AD19	18	AD19	CAD19	95	A_CAD19
AD18	19	AD18	CAD18	94	A_CAD18
AD17	21	AD17	CAD17	93	A_CAD17
AD16	22	AD16	CAD16	75	A_CAD16
AD15	28	AD15	CAD15	73	A_CAD15
AD14	29	AD14	CAD14	74	A_CAD14
AD13	30	AD13	CAD13	71	A_CAD13
AD12	31	AD12	CAD12	72	A_CAD12
AD11	34	AD11	CAD11	70	A_CAD11
AD10	35	AD10	CAD10	69	A_CAD10
AD9	36	AD9	CAD9	68	A_CAD9
AD8	37	AD8	CAD8	85	A_CAD8
AD7	38	AD7	CAD7	84	A_CAD7
AD6	39	AD6	CAD6	82	A_CAD6
AD5	40	AD5	CAD5	83	A_CAD5
AD4	41	AD4	CAD4	80	A_CAD4
AD3	42	AD3	CAD3	81	A_CAD3
AD2	43	AD2	CAD2	78	A_CAD2
AD1	44	AD1	CAD1	79	A_CAD1
AD0	46	AD0	CAD0	76	A_CAD0
PCM_IDSEL	127	IDSEL			

9	CBE3#	CBE3#	11	C/BE3#	
9	CBE2#	CBE2#	12	C/BE2#	
9	CBE1#	CBE1#	49	C/BE1#	
9	CBE0#	CBE0#	50	C/BE0#	
9	PCLK_PCM		26	PCI_CLK	CCLK	107	R_A_CCLK
9	DEVSEL#	DEVSEL#	27	DEVSEL#	CFRAME#	114	A_CFRAME#
9	FRAME#	FRAME#	23	FRAME#	CIRDY#	117	A_CIRDY#
9	IRDY#	IRDY#	24	IRDY#	CTRDY#	116	A_CTRDY#
9	TRDY#	TRDY#	25	TRDY#	CDEVSEL#	113	A_CDEVSEL#
9	STOP#	STOP#	47	STOP#	CSTOP#	61	A_CSTOP#
9	PAR	PAR	48	PAR	CPAR	58	A_CPAR
					CPERR#	60	A_CPERR#
				PERR#/SPKR_OUT	CSERR#	91	A_CSERR#
19	PCMSPK	PCMSPK	51		CREQ#	89	A_CREQ#
					CGNT#	62	A_CGNT#
9	REQ0#	REQ0#	2	REQ#	CINT#	88	A_CINT#
9	GNT0#	GNT0#	3	GNT#	CBLOCK#	59	A_CBLOCK#
					CCLKRUN#	87	A_CCLKRUN#
9	PCIRST#	R308 *CB^0_4 PCIRST#_R	126	RST#	CRST#	119	A_CRST#
9	PCI_PME#	R310 *CB^0_4 PCM_PME#	120	PME#/RI_OUT#	R_D2	98	A_CRSVD/D2
					R2_D14	86	A_CRSVD/D14
9,21	CLKRUN#		55	MF6 (CLKRUN#)	R2_A18	63	A_CRSVD/A18
				MF4 (RI_OUT#)	CVS1	57	A_CVS1#
9,21	SERIRQ	SERIRQ	53	MF3 (SERIRQ#)	CVS2	121	A_CVS2#
9	INTA#		52	MF0 (INTA#)	CCD1#	56	A_CCD1#
					CCD2#	122	A_CCD2#
					CAUDIO	92	A_CAUDIO
					CSTSCHG	90	A_CSTSCHG
					CC/BE3#	111	A_CC/BE3#
					CC/BE2#	112	A_CC/BE2#
					CC/BE1#	66	A_CC/BE1#
					CC/BE0#	67	A_CC/BE0#

GND GND GND GND GND — 32 45 65 96 128

SKT_VCC — R311 *CB^47K — A_CRST#

SKT_VCC — C443 *CB^4.7u/6.3V_6, C449 *CB^.1u/16V_4; +3V — C453 *CB^4.7u/6.3V_6, C450 *CB^.1u/16V_4; +5V — C442 *CB^4.7u/6.3V_6, C444 *CB^.1u/16V_4

U18 *CB^OZ2210G

6	VCC1	+3.3	1
5	VCC2	+3.3	2
7	VCC5#	+5V	3
8	VCC3#	GND	4

VCCD0, VCCD1

Check Footprint & P/N

22K TO 47K PULL-UPS MUST BE PLACED
ON INTA#, PME#, SERIRQ# & CLKRUN#.

R_A_CCLK R307 *CB^33_4 A_CCLK

PCMCIA SOCKET

CN9 — Check it

A_CAD0	2	GND1	SKTA/VCC1	17	SKT_VCC
A_CAD1	3	SKTAAD0/D3	SKTA/VCC2	51	
A_CAD3	4	SKTAAD1/D4			
A_CAD5	5	SKTAD3/D5	SKTA/VPP1	18	
A_CAD7	6	SKTAD5/D6	SKTA/VPP2	52	
A_CC/BE0#	7	SKTAAD7/D7			
A_CAD9	8	-SKTACBE0/CE1#			
A_CAD11	9	SKTAAD9/A10			
A_CAD12	10	SKTABAD11/OE#	GND5	69	
A_CAD14	11	SKTAAD12/A11	GND6	70	
A_CC/BE1#	12	SKTAAD14/A9	GND7	71	
A_CPAR	13	-SKTACBE1/A8	GND8	72	
A_CPERR#	14	SKTAPAR/A13	GND9	73	
A_CGNT#	15	-SKTAPERR/A14	GND10	74	
A_CINT#	16	-SKTAGNT/WE#	GND11	75	
		-SKTAINT/RDY	GND12	76	
		UPPER PIN	GND13	77	
A_CCLK	19	SKTAPCLK/A16	GND14	78	
A_CIRDY#	20	-SKTAIRDY/A15	GND15	79	
A_CC/BE2#	21	-SKTACBE2/A12	GND16	80	
A_CAD18	22	SKTAAD18/A7	GND17	81	
A_CAD20	23	SKTAAD20/A6	GND18	82	
A_CAD21	24	SKTAAD21/A5	GND19	83	
A_CAD22	25	SKTAAD22/A4	GND20	84	
A_CAD23	26	SKTAAD23/A3			
A_CAD24	27	SKTAAD24/A2			
A_CAD25	28	SKTAAD25/A1			
A_CAD26	29	SKTAAD26/A0	NC	85	
A_CAD27	30	SKTAAD27/D0	NC	86	
A_CAD29	31	SKTAAD29/D1	NC	87	
A_CRSVD/D2	32	SKTARSVD/D2	NC	88	
A_CCLKRUN#	33	-SKTACLKRUN/WP			
	34	GND2			
	35	GND3			
A_CCD1#	36	-SKTACD1/CD1#			
A_CAD2	37	SKTAAD2/D11			
A_CAD4	38	SKTAD4/D12			
A_CAD6	39	SKTAAD6/D13			
A_CRSVD/D14	40	SKTARSVD/D14			
A_CAD8	41	SKTAAD8/D15			
A_CAD10	42	-SKTAD10/CE2#			
A_CVS1#	43	-SKTAVS1/VS1#			
A_CAD13	44	SKTAAD13/IORD#			
A_CAD15	45	SKTAAD15/IOWR#			
A_CAD16	46	SKTAAD16/A17			
A_CRSVD/A18	47	-SKTRSVD/A18			
A_CBLOCK#	48	-SKTALOCK/A19			
A_CSTOP#	49	-SKTASTOP/A20			
A_CDEVSEL#	50	-SKTADEVSEL/A21			
		LOWER PIN			
A_CTRDY#	53	-SKTATRDY/A22			
A_CFRAME#	54	-SKTAFRAME/A23			
A_CAD17	55	SKTAAD17/A24			
A_CAD19	56	SKTAAD19/A25			
A_CVS2#	57	-SKTAVS2VS2#			
A_CRST#	58	-SKTARST/RESET			
A_CSERR#	59	0SKTASERR/WAIT#			
A_CREQ#	60	-SKTAREQ/INPACK#			
A_CC/BE3#	61	-SKTACBE3/REG#			
A_CAUDIO	62	SKTAAUDIO/BVD2			
A_CSTSCHG	63	-SKTASTSCHG/BVD1			
A_CAD28	64	SKTAAD28/D8			
A_CAD30	65	SKTAAD30/D9			
A_CAD31	66	SKTAAD31/D10			
A_CCD2#	67	-SKTACD2/CD2#			
	68	GND4			

*CB^PCMCIA_SOCKET

Quanta Computer Inc.
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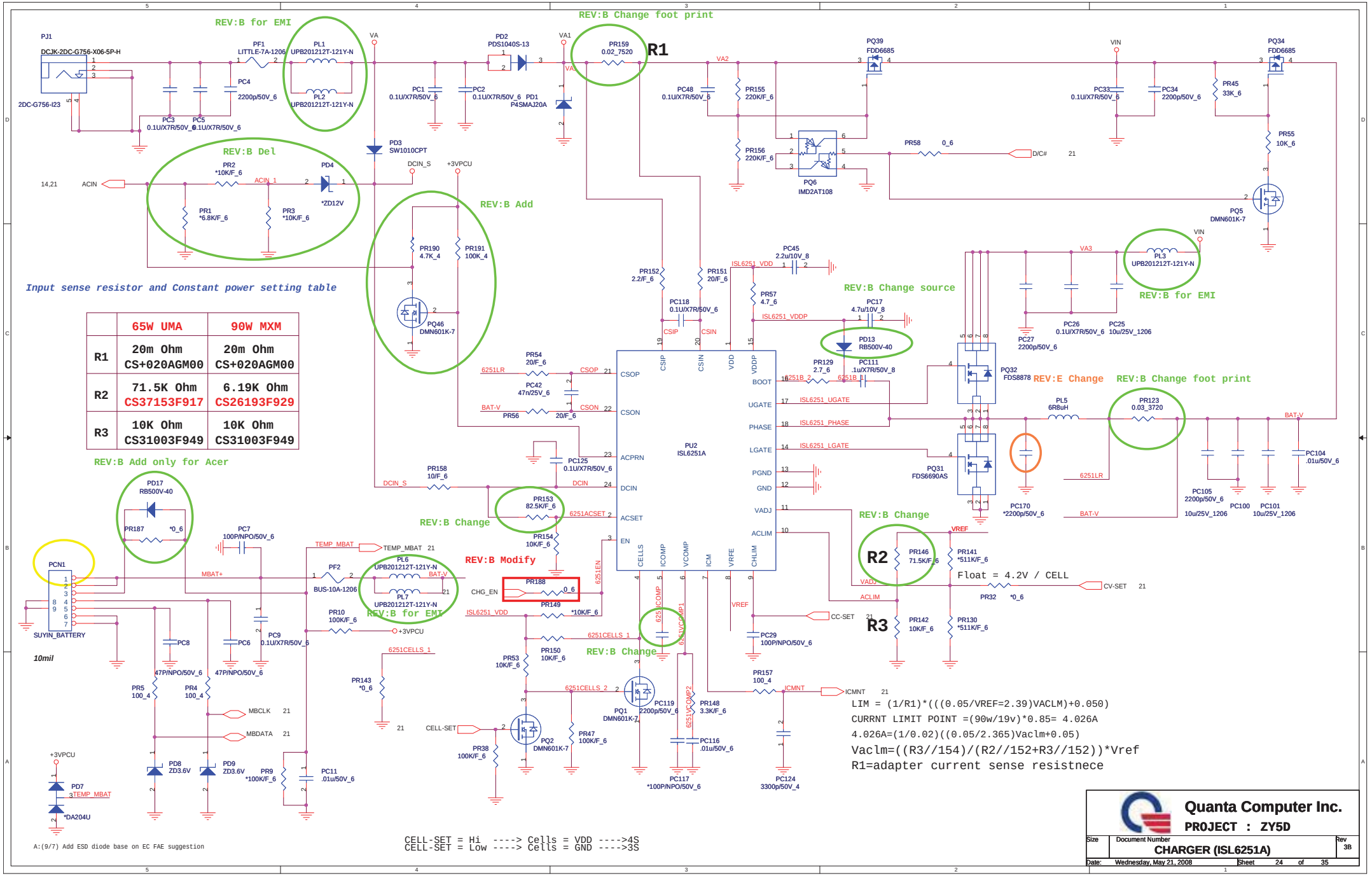
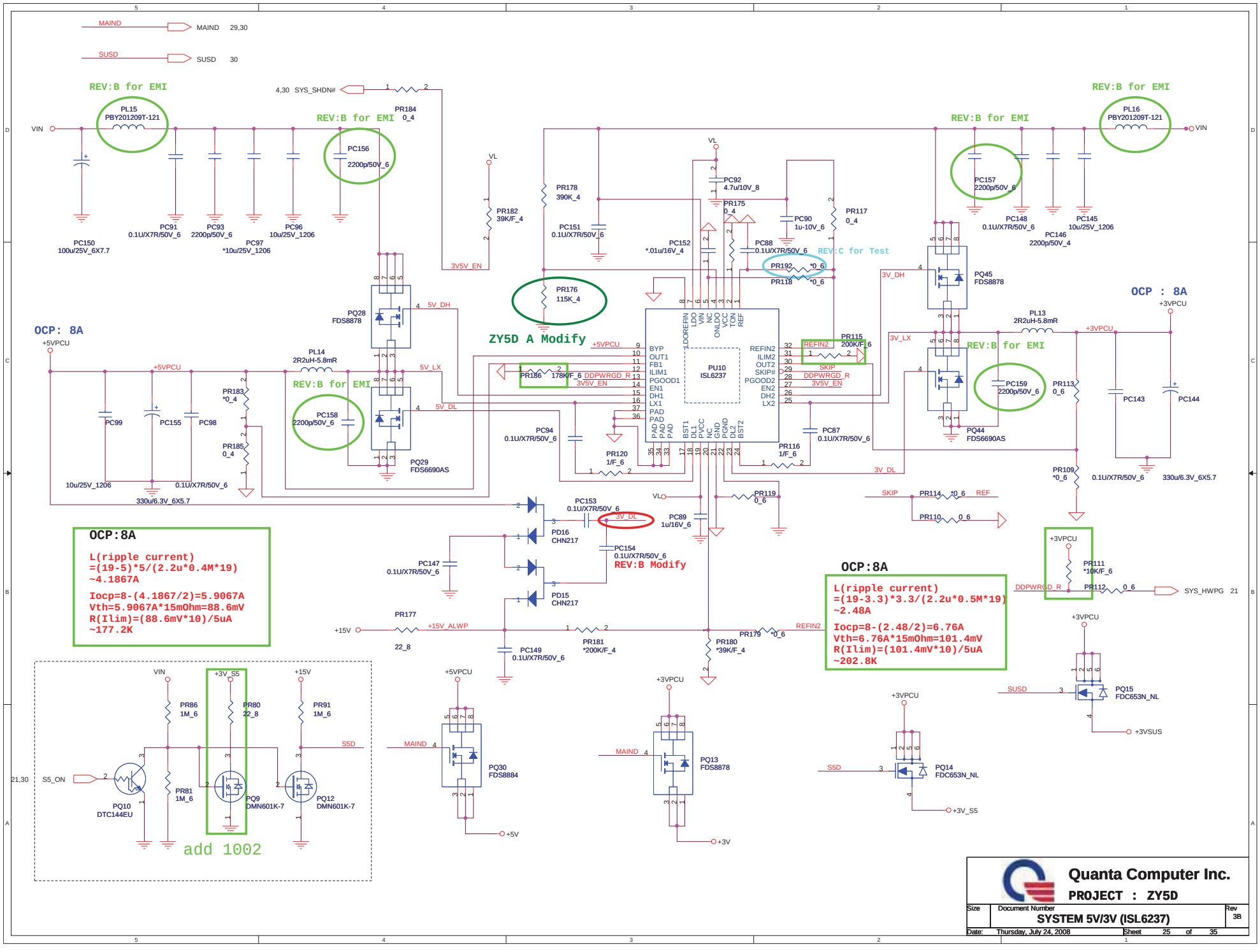


Input sense resistor and Constant power setting table

	65W UMA	90W MXM
R1	20m Ohm CS+020AGM00	20m Ohm CS+020AGM00
R2	71.5K Ohm CS37153F917	6.19K Ohm CS26193F929
R3	10K Ohm CS31003F949	10K Ohm CS31003F949


MAIND
MAIND 29,30
SUSD
SUSD 30
REV:B for EMI
4,30 SYS_SHDN#
PR184 0_4
VIN
PL15 PBY201209T-121
PC150 100u/25V_6X7.7
PC91 0.1U/X7R/50V_6
PC93 2200p/50V_6
PC97 *10u/25V_1206
PC96 10u/25V_1206
PC156 2200p/50V_6
VL
PR182 39K/F_4
3V5V_EN
PR178 390K_4
PC151 0.1U/X7R/50V_6
PR176 115K_4
ZY5D A Modify
PC92 4.7u/10V_8
PR175 0_4
PC90 1u-10V_6
PR117 0_4
PC88 0.1U/X7R/50V_6
REV:C for Test
PR192 *0_6
PR118 *0_6
PR152 *.01u/16V_4
PU10 ISL6237
LDOREFIN LDO VIN NC ONLDO VCC TON REF
BYP OUT1 FB1 ILIM1 PGOOD1 EN1 DH1 LX1 PAD PAD PAD
REFIN2 ILIM2 OUT2 SKIP# PGOOD2 EN2 DH2 LX2
BST1 DL1 PVCC NC GND PGND DL2 BST2
+5VPCU
PR186 178K/F_6
DDPWRGD_R
PR115 200K/F_6
SKIP
PR116 1/F_6
PR120 1/F_6
PC94 0.1U/X7R/50V_6
PC87 0.1U/X7R/50V_6
OCP: 8A
PL14 2R2uH-5.8mR
PR183 *0_4
PR185 0_4
PC99
PC155
PC98
10u/25V_1206
0.1U/X7R/50V_6
330u/6.3V_6X5.7
PC158 2200p/50V_6
PQ28 FDS8878
PQ29 FDS6690AS
5V_LX
5V_DH
5V_DL
PR119 0_6
PC89 1u/16V_6
PC153 0.1U/X7R/50V_6
PC154 0.1U/X7R/50V_6
REV:B Modify
PD16 CHN217
PD15 CHN217
PC147 0.1U/X7R/50V_6
PC149 0.1U/X7R/50V_6
PR177 22_8
+15V
+15V_ALWP
PR181 *200K/F_4
PR180 *39K/F_4
PR179 *0_6
REFIN2
3V_DL
OCP:8A
L(ripple current) =(19-5)*5/(2.2u*0.4M*19) ~4.1867A
Iocp=8-(4.1867/2)=5.9067A
Vth=5.9067A*15mOhm=88.6mV
R(Ilim)=(88.6mV*10)/5uA ~177.2K
REV:B for EMI
PL16 PBY201209T-121
PC157 2200p/50V_6
PC148 0.1U/X7R/50V_6
PC146 2200p/50V_4
PC145 10u/25V_1206
PQ45 FDS8878
PQ44 FDS6690AS
3V_DH
3V_LX
OCP : 8A
PL13 2R2uH-5.8mR
PC159 2200p/50V_6
PR113 0_6
PC143
PC144
PR109 *0_6
0.1U/X7R/50V_6
330u/6.3V_6X5.7
SKIP
PR114 *0_6
REF
PR110 0_6
PR111 *10K/F_6
DDPWRGD_R
PR112 0_6
SYS_HWPG 21
OCP:8A
L(ripple current) =(19-3.3)*3.3/(2.2u*0.5M*19) ~2.48A
Iocp=8-(2.48/2)=6.76A
Vth=6.76A*15mOhm=101.4mV
R(Ilim)=(101.4mV*10)/5uA ~202.8K
PQ15 FDC653N_NL
SUSD
+3VSUS
PQ14 FDC653N_NL
S5D
+3V_S5
PQ30 FDS8884
MAIND
+5V
PQ13 FDS8878
+3V
21,30 S5_ON
PQ10 DTC144EU
PR86 1M_6
PR80 22_8
PR91 1M_6
PR81 1M_6
PQ9 DMN601K-7
PQ12 DMN601K-7
+3V_S5
S5D
add 1002
Quanta Computer Inc.
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OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	0	0	X
+3.3V	X	X	0
+5V	X	0	X

Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

add 1002

add 1002

add 1002

add 1002

add 1002

REV:B for EMI

REV:B for EMI

REV:B for EMI

REV:B for EMI

REV:B Remove JP5

REV:B Remove JP5

REV:C Change source

REV:C Change source

REV:C Change source

REV:C Change source

REV:C2 for EMI

REV:B Add

REV:B Modify

ZY5D A Modify

ZY5D A Modify

ZY5D A Modify

Pin 49 is GND Pin

Close to CPU socket

Close to CPU socket

Parallel

PU11 ISL6265

PQ33 FDS6900AS

PQ35 TPCA8023-H

PQ37 TPCA8019-H

PQ38 TPCA8023-H

PQ36 TPCA8019-H

PQ42 DTC144EU

Quanta Computer Inc.

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AMD Gfiffin (ISL6265)

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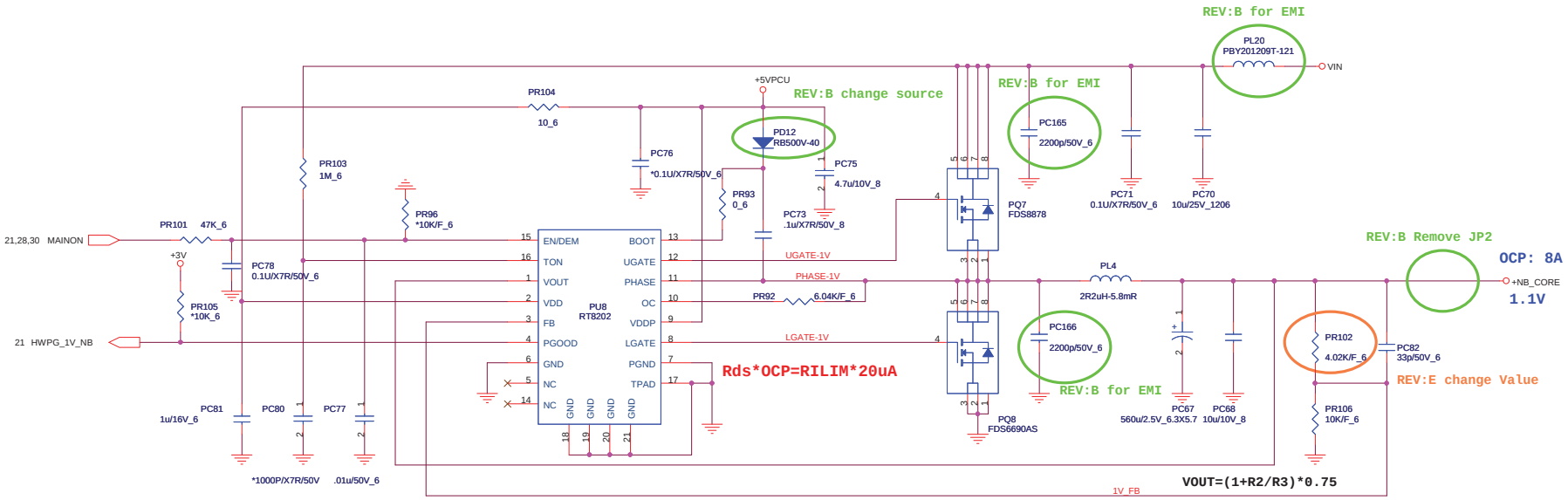

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

8A OCP --- OC=6.04K
FDS6690AS Rds=15mOhm

Quanta Computer Inc.		
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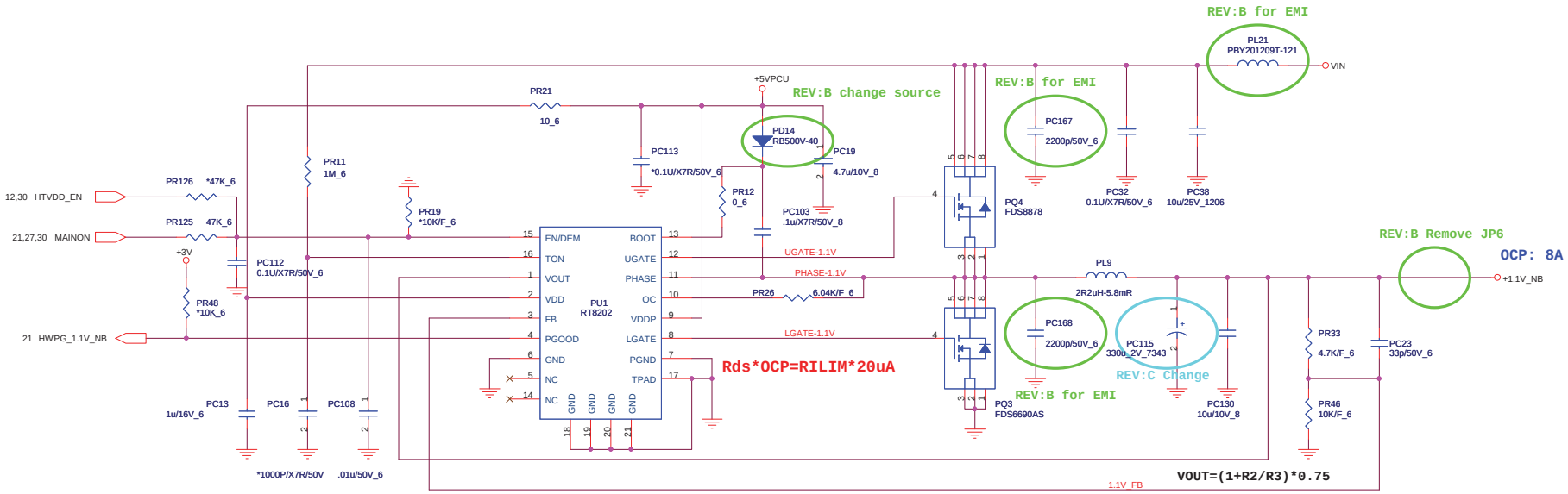

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

8A OCP --- OC=6.04K
FDS6690AS Rds=15mOhm

Quanta Computer Inc.		
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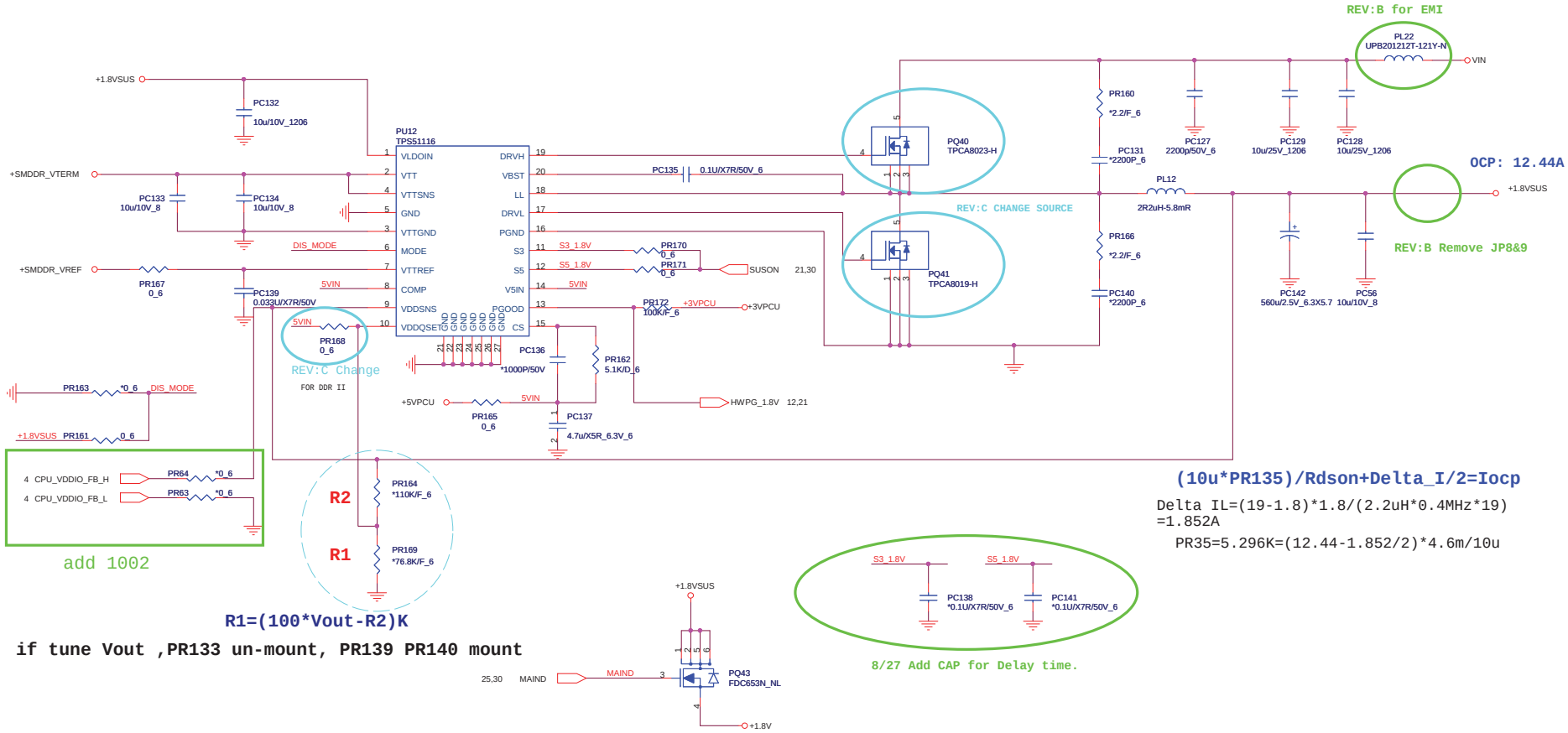

Quanta Computer Inc.		
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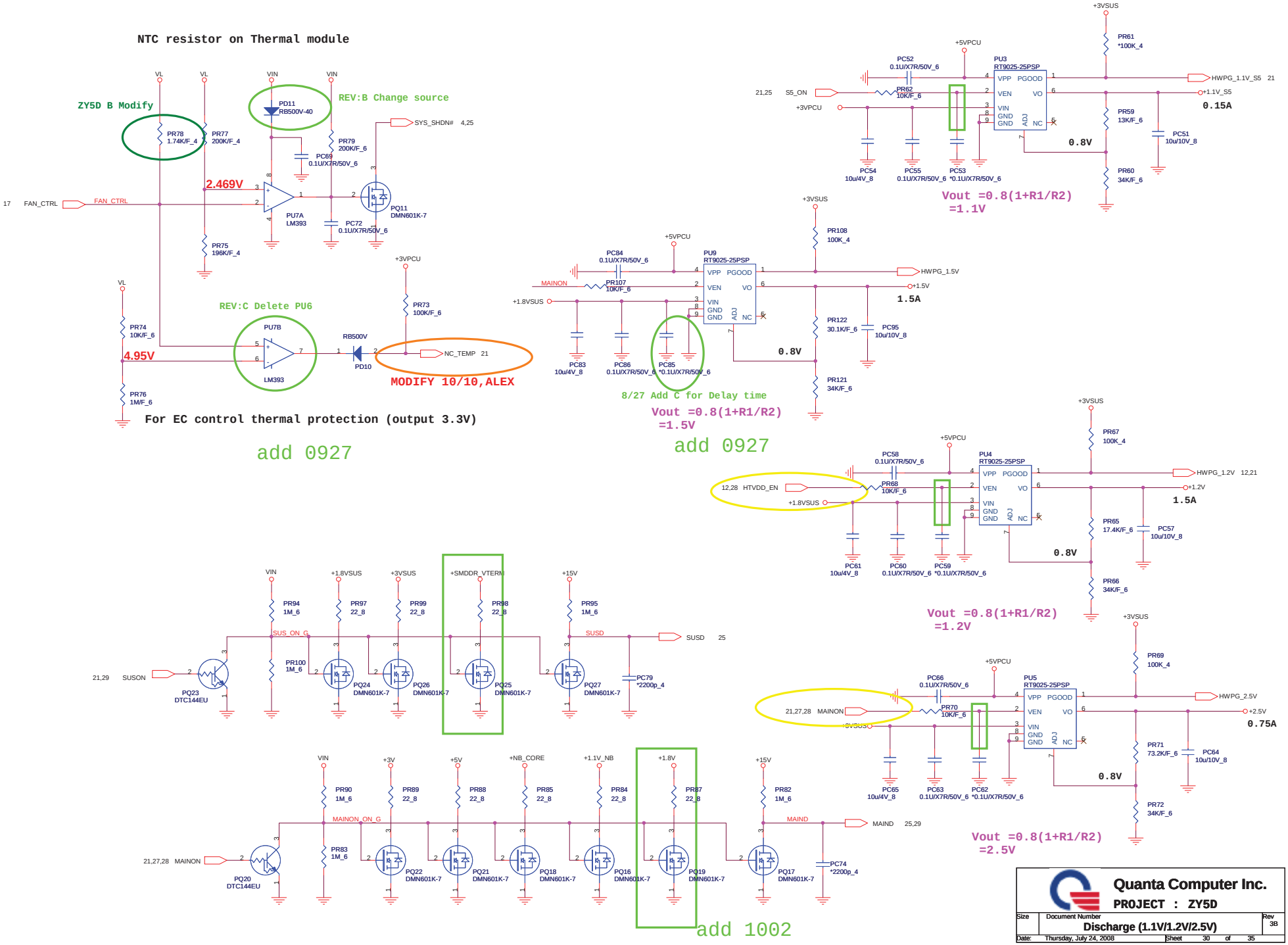
NTC resistor on Thermal module
ZY5D B Modify
REV:B Change source
PD11
RB500V-40
PR78
1.74K/F_4
PR77
200K/F_4
PR79
200K/F_6
PC69
0.1U/X7R/50V_6
SYS_SHDN# 4,25
2.469V
17 FAN_CTRL
FAN_CTRL
PU7A
LM393
PQ11
DMN601K-7
PC72
0.1U/X7R/50V_6
PR75
196K/F_4
REV:C Delete PU6
PU7B
PR74
10K/F_6
4.95V
LM393
RB500V
PD10
PR73
100K/F_6
NC_TEMP 21
MODIFY 10/10,ALEX
PR76
1M/F_6
For EC control thermal protection (output 3.3V)
add 0927
+3VSUS
PR61
*100K_4
PC52
0.1U/X7R/50V_6
+5VPCU
PU3
RT9025-25PSP
21,25 S5_ON
PR62
10K/F_6
+3VPCU
HWPG_1.1V_S5 21
+1.1V_S5
0.15A
PR59
13K/F_6
PC51
10u/10V_8
0.8V
PC54
10u/4V_8
PC55
0.1U/X7R/50V_6
PC53
*0.1U/X7R/50V_6
PR60
34K/F_6
Vout =0.8(1+R1/R2)
=1.1V
+3VSUS
PR108
100K_4
PC84
0.1U/X7R/50V_6
+5VPCU
PU9
RT9025-25PSP
MAINON
PR107
10K/F_6
+1.8VSUS
HWPG_1.5V
+1.5V
1.5A
PR122
30.1K/F_6
PC95
10u/10V_8
0.8V
PC83
10u/4V_8
PC86
0.1U/X7R/50V_6
PC85
*0.1U/X7R/50V_6
PR121
34K/F_6
8/27 Add C for Delay time
Vout =0.8(1+R1/R2)
=1.5V
add 0927
+3VSUS
PR67
100K_4
PC58
0.1U/X7R/50V_6
+5VPCU
PU4
RT9025-25PSP
12,28 HTVDD_EN
PR68
10K/F_6
+1.8VSUS
HWPG_1.2V 12,21
+1.2V
1.5A
PR65
17.4K/F_6
PC57
10u/10V_8
0.8V
PC61
10u/4V_8
PC60
0.1U/X7R/50V_6
PC59
*0.1U/X7R/50V_6
PR66
34K/F_6
Vout =0.8(1+R1/R2)
=1.2V
VIN
+1.8VSUS
+3VSUS
+SMDDR_VTERM
+15V
PR94
1M_6
PR97
22_8
PR99
22_8
PR98
22_8
PR95
1M_6
SUS_ON_G
SUSD
SUSD 25
21,29 SUSON
PR100
1M_6
PQ23
DTC144EU
PQ24
DMN601K-7
PQ26
DMN601K-7
PQ25
DMN601K-7
PQ27
DMN601K-7
PC79
*2200p_4
+3VSUS
PR69
100K_4
PC66
0.1U/X7R/50V_6
+5VPCU
PU5
RT9025-25PSP
21,27,28 MAINON
PR70
10K/F_6
+3VSUS
HWPG_2.5V
+2.5V
0.75A
PR71
73.2K/F_6
PC64
10u/10V_8
0.8V
PC65
10u/4V_8
PC63
0.1U/X7R/50V_6
PC62
*0.1U/X7R/50V_6
PR72
34K/F_6
Vout =0.8(1+R1/R2)
=2.5V
VIN
+3V
+5V
+NB_CORE
+1.1V_NB
+1.8V
+15V
PR90
1M_6
PR89
22_8
PR88
22_8
PR85
22_8
PR84
22_8
PR87
22_8
PR82
1M_6
MAINON_ON_G
MAIND
MAIND 25,29
21,27,28 MAINON
PR83
1M_6
PQ20
DTC144EU
PQ22
DMN601K-7
PQ21
DMN601K-7
PQ18
DMN601K-7
PQ16
DMN601K-7
PQ19
DMN601K-7
PQ17
DMN601K-7
PC74
*2200p_4
add 1002
Quanta Computer Inc.
PROJECT : ZY5D
Size
Document Number
Discharge (1.1V/1.2V/2.5V)
Rev
3B
Date: Thursday, July 24, 2008
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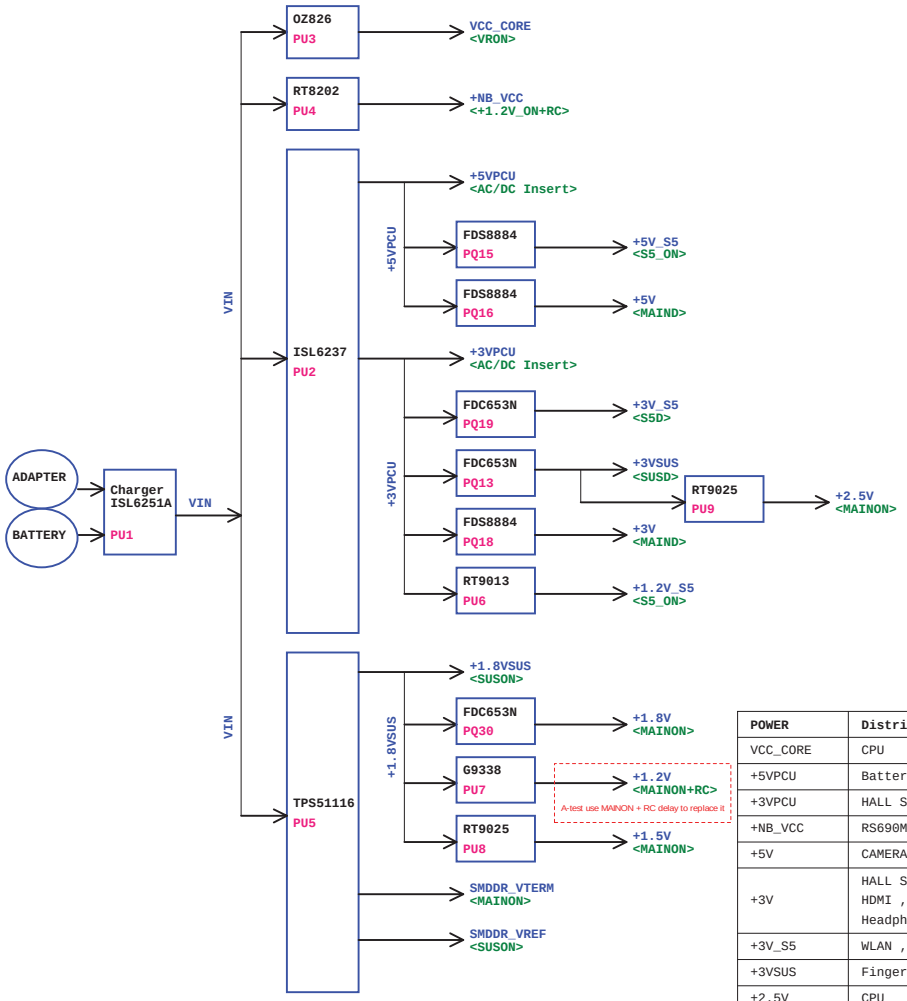

POWER	Distribution
VCC_CORE	CPU
+5VPCU	Battery LED , Power LED , USB , CIR , RTC
+3VPCU	HALL SENSOR , Battery LED , RF LED , kill SW , Jumper LED , KB , Power Board , EC , ID , SPI Flash , CIR
+NB_VCC	RS690M
+5V	CAMERA , Card Reader LED , ODD/HDD LED , Felica , T/P , T/sensor , CRT , HDMI , SB600 , CPU FAN , MXM , Headphone , EC , INT SPK AMP
+3V	HALL SENSOR , LCD PANEL , LVDS , WLAN , HD Decoder , NEW CARD , KB , KB LED , XD LED , Blue tooth , Touch sensor , Card Reader (OZ129) , ODD/HDD , HDMI , CRT , TVOUT , REQUIRED STRAPS , DEBUG STRAPS , SB600 , RS690M , DDR , CPU Thermal monitor , CPU FAN , CLK , MXM , VR , FM Tuner MDC , Headphone , EC , LAN , Codec(CX 20561)
+3V_S5	WLAN , NEW CARD , SB600 , MXM , LAN
+3VSUS	Finger print , SB600
+2.5V	CPU
+1.2V_S5	SB600
+1.8VSUS	SB600 , DDR , CPU , HDT
+1.8V	SB600 , LCD , LVDS , RS690M
+1.2V	SB600 , RS690M , CPU , WLAN , HD Decoder , NEW CARD
+SMDDR_VTERM	DDR , CPU
+SMDDR_VREF	DDR
+5V_S5	

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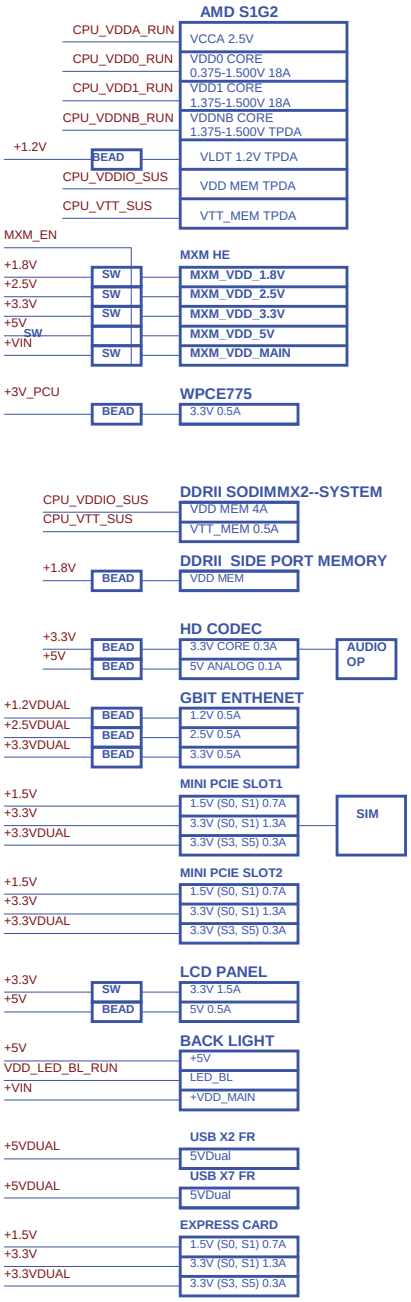
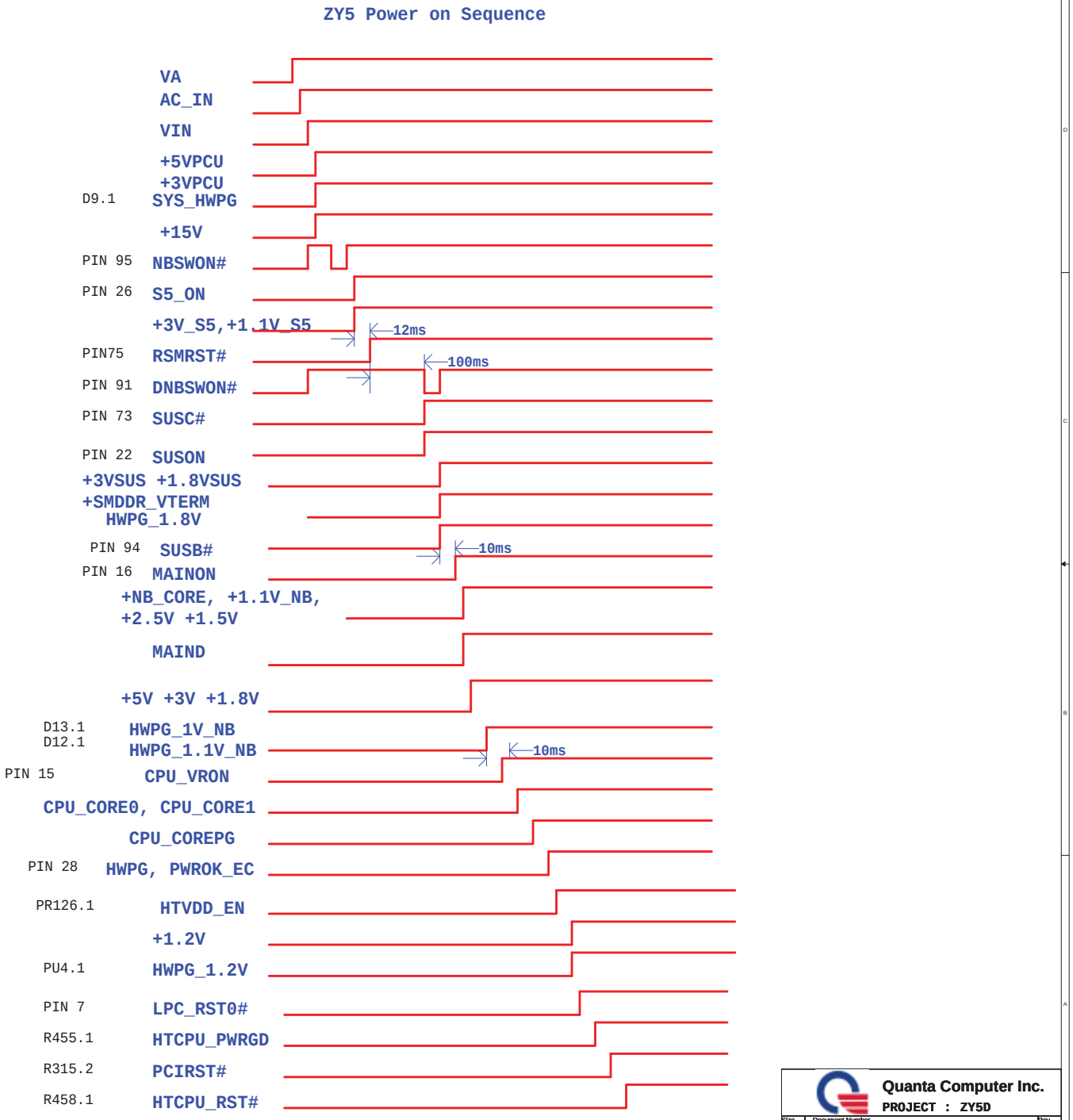
PROJECT : ZY5D
Power Tree





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