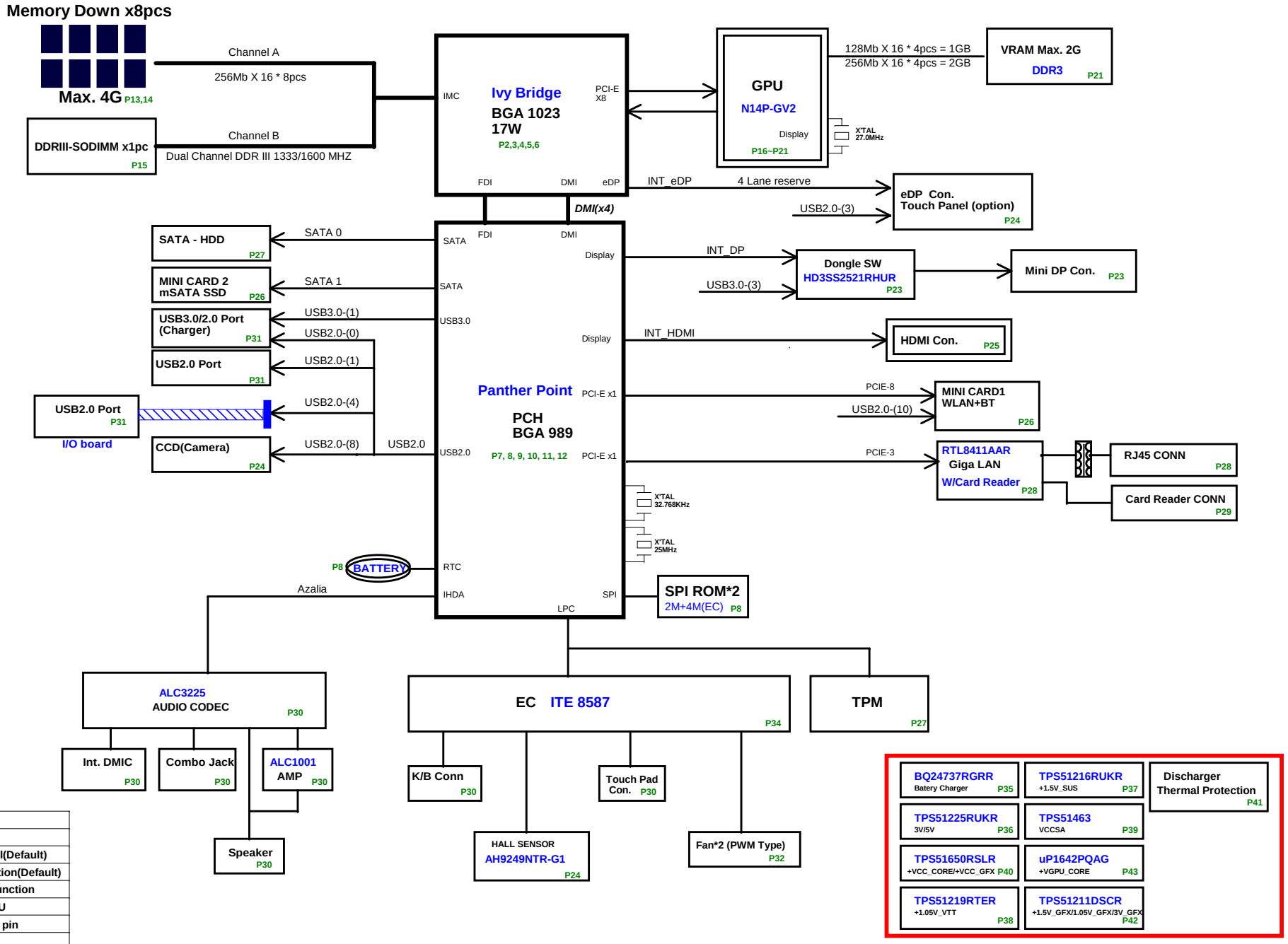
ZQK ULV SYSTEM BLOCK DIAGRAM



TPL@	Touch panel
TPM@	TPM module
NP@	Normal panel(Default)
CH@	Charge function(Default)
NCH@	No Charge function
EV@	Optimize SKU
RAMID@	RAMID strap pin
SUG@	LAN Surge
NSW@	w/o Dongle switch
SW@	w Dongle switch
KBL@	KB Backlight LED
RD@	mSATA Re-driver

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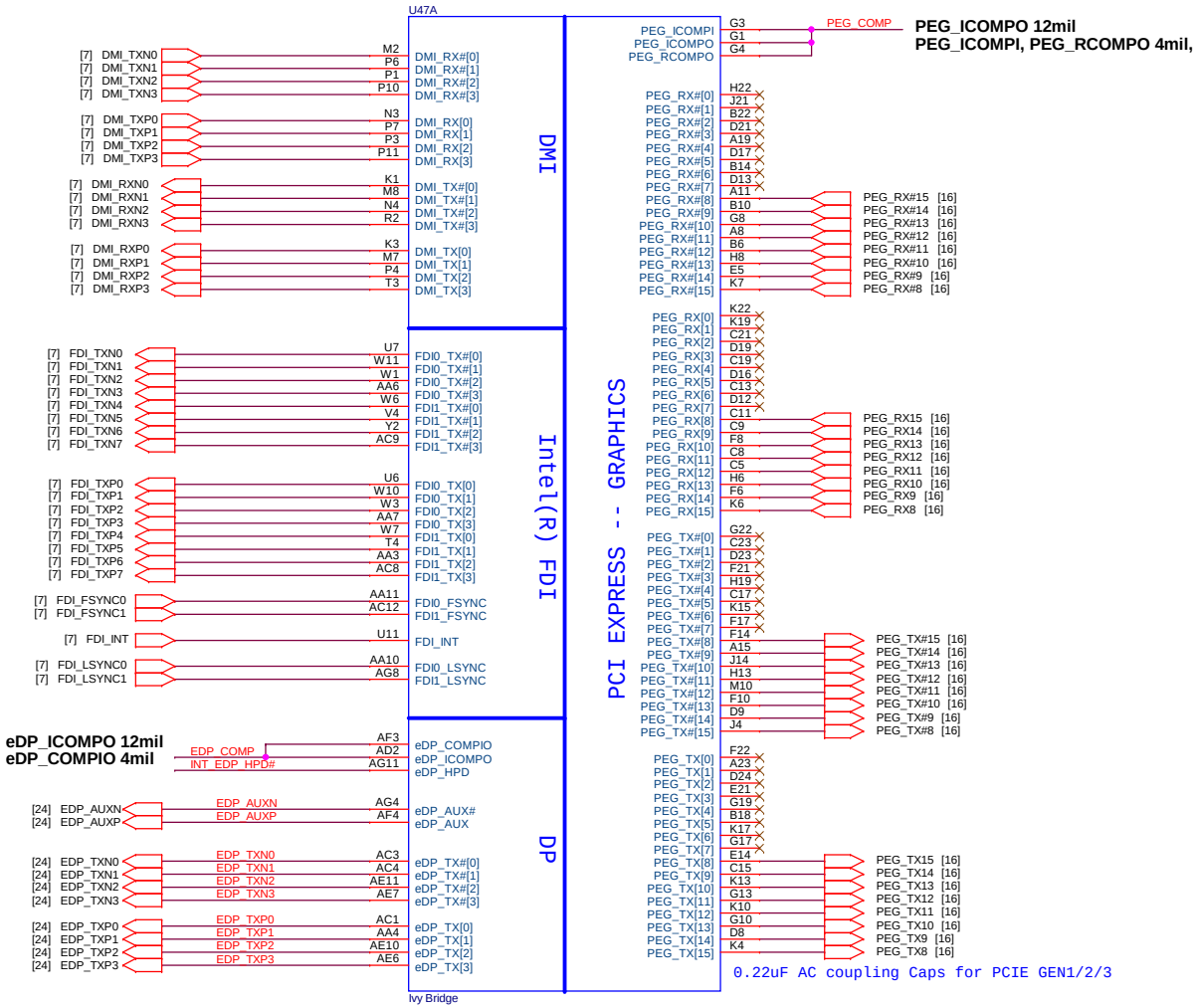
Size	Document Number	Rev
	Block Diagram	1A

Date: Monday, January 07, 2013 Sheet 1 of 46

Ivy Bridge Processor (DMI,PEG,FDI) (CPU)

PEG_ICOMPI and RCOMPO signals
should be shorted and routed with
- max length = 500 mils
- typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with
- max length = 500 mils
- typical impedance = 14.5 mohms

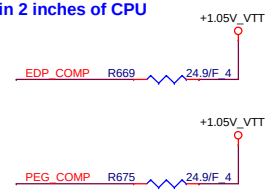


DP_COMPIO and ICOMPO signals
should be shorted near balls and routed with
- typical impedance < 25 mohms

DG 1.0 :
The recommended AC cap value is changed to 220nF for compatibility with
PCIe Gen3 on future platforms.
For Gen2 only designs, it is acceptable to continue to use the 100nF capacitor.

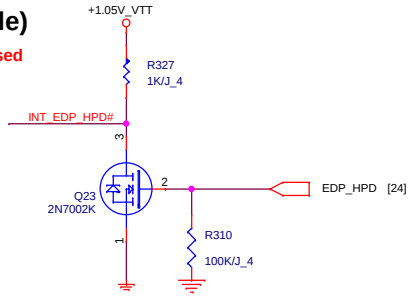
DP & PEG Compensation

CAD Note: Place PU resistor
within 2 inches of CPU



eDP Hot-plug (Disable)

HPD PU/PD resistor values based
on CRB and different to DG



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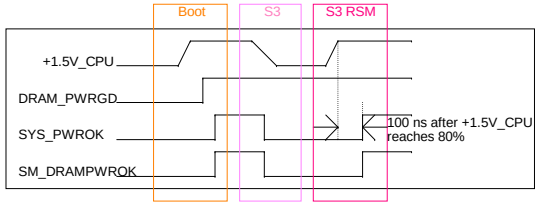
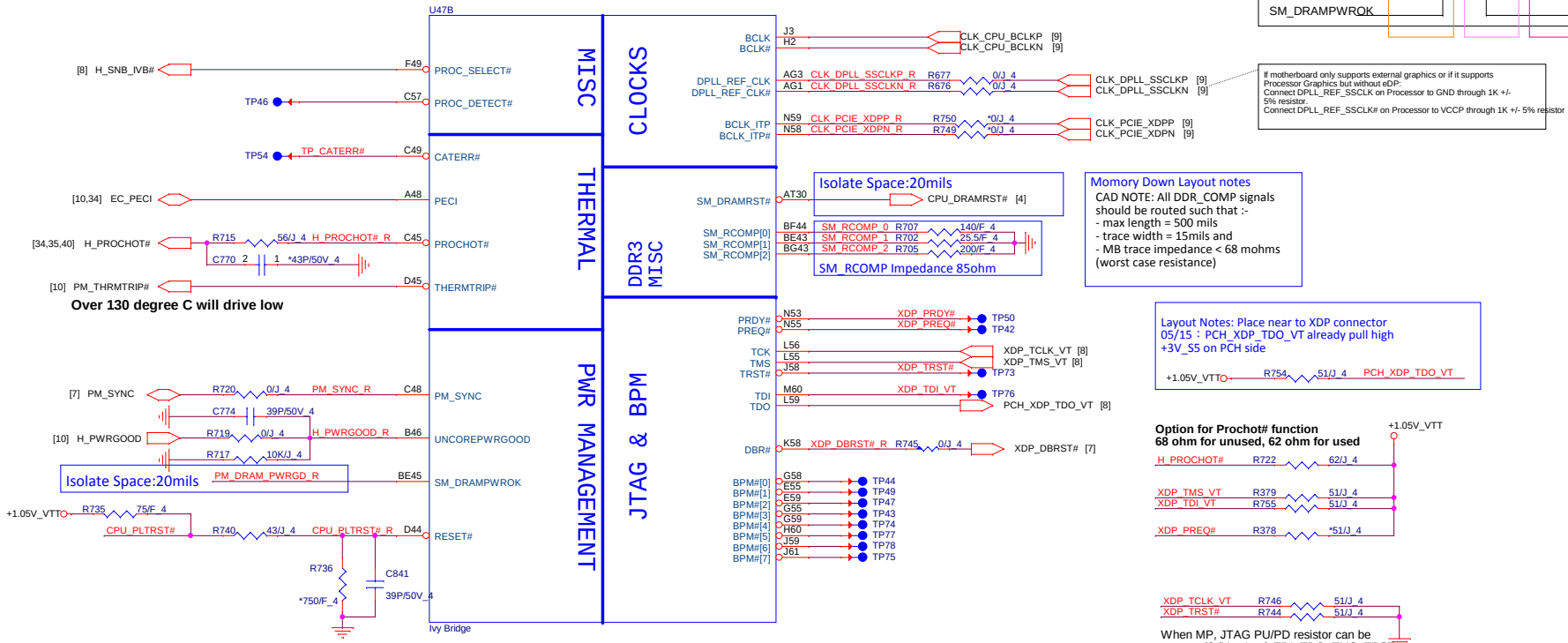
Size	Document Number	Rev
	Ivy Bridge 1/5 (HOST & PCIE)	1A
Date: Monday, January 07, 2013	Sheet 2 of 46	

Ivy Bridge Processor (CLK,MISC,JTAG) (CPU)





Isolate Space:20mils

Memory Down Layout notes
CAD NOTE: All DDR_COMP signals should be routed such that :-
- max length = 500 mils
- trace width = 15mils and
- MB trace impedance < 68 mohms (worst case resistance)

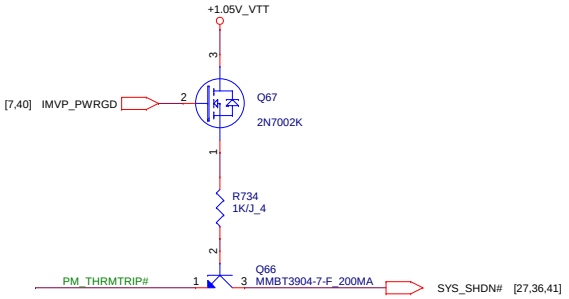
If motherboard only supports external graphics or if it supports Processor Graphics but without eDP:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistor

Layout Notes: Place near to XDP connector
05/15：PCH_XDP_TDO_VT already pull high
+3V_S5 on PCH side
+1.05V_VTT R754 51/J_4 PCH_XDP_TDO_VT

Option for Prochot# function
68 ohm for unused, 62 ohm for used

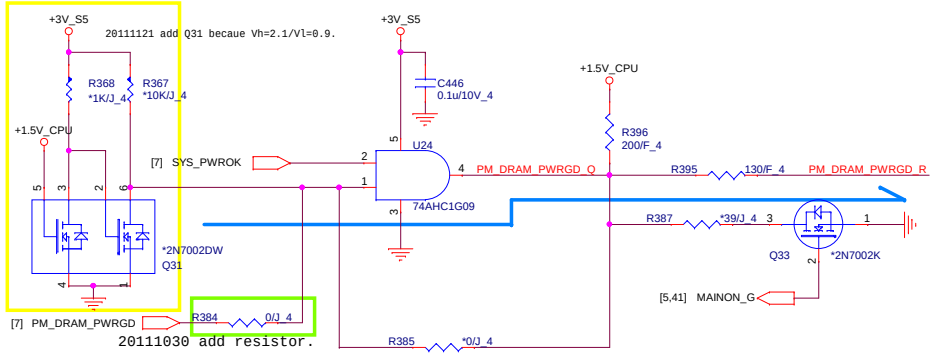
When MP, JTAG PU/PD resistor can be removed? (Yes Intel, TDI, TDO, TMS, TRST#, TCK,PREQ#, PRDY#)

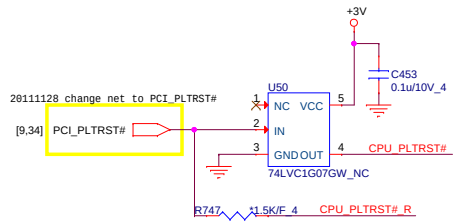
Thermal Trip (CPU)



S3 leakage circuit (CPU)

If PM_DRAM_PWEGD connector,the R5180 must stuff.





IN	OUT
L	L
H	High-Z

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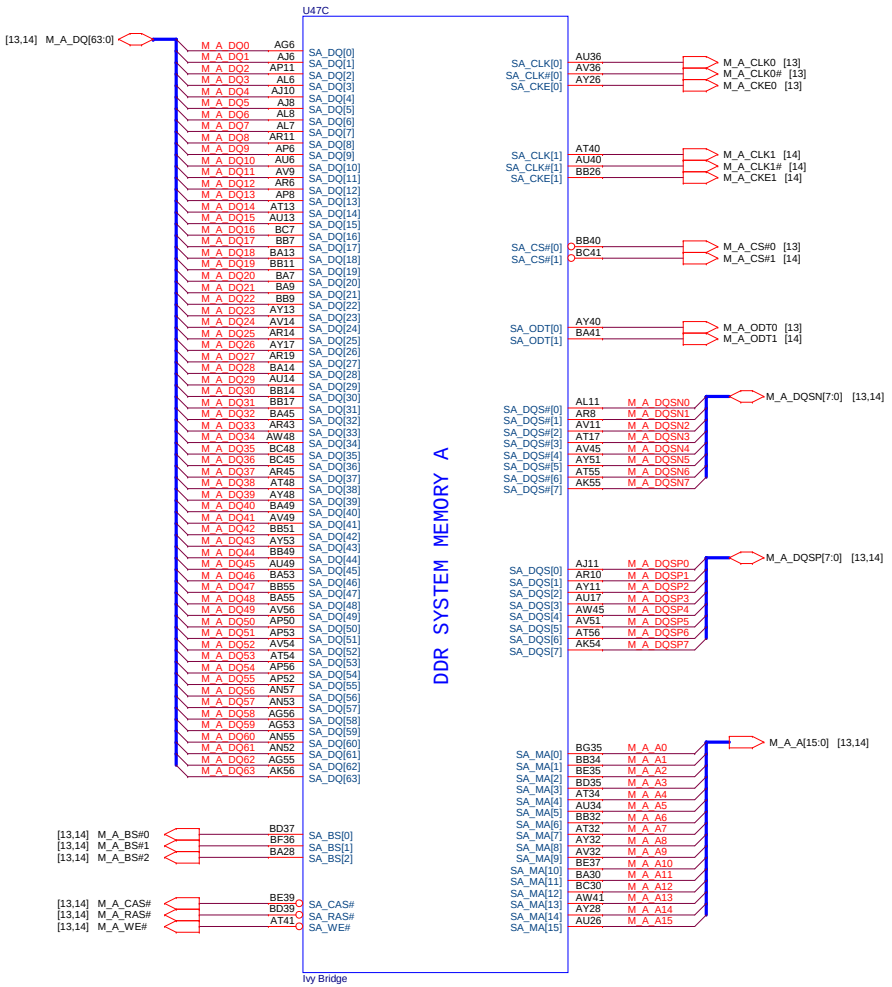
PROJECT : ZQK

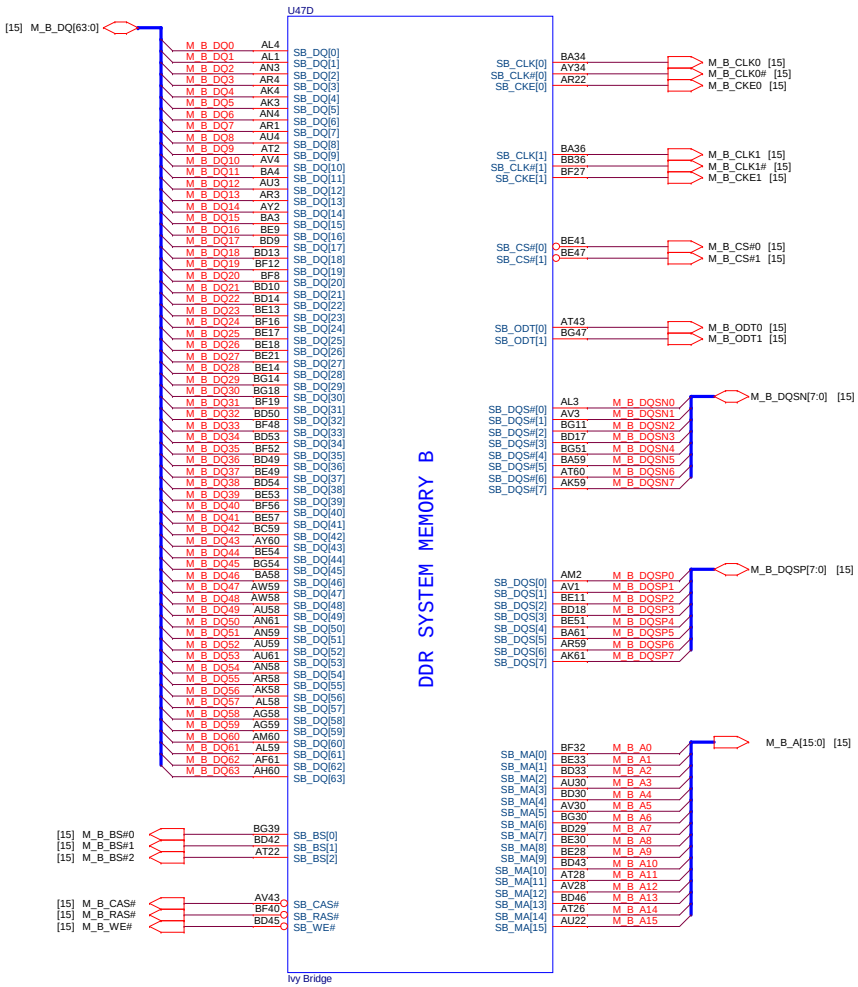
Size	Document Number	Rev
	Ivy Bridge 2/5 (CLK & JTAG)	1A
Date: Monday, January 07, 2013	Sheet 3 of 46	

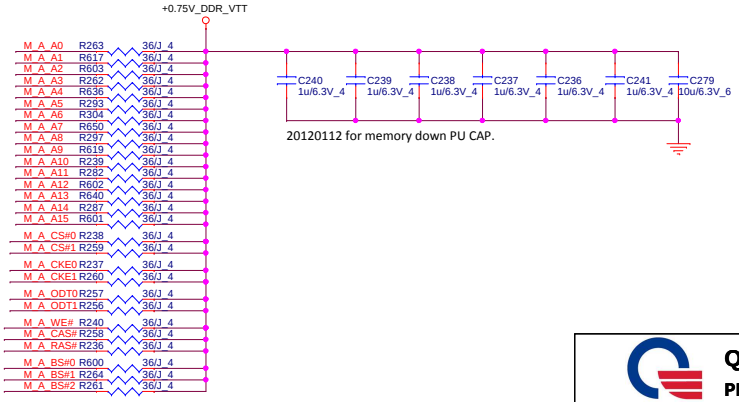
Ivy Bridge Processor (CPU)

Channel A: On board RAM 2Rx16 8pcs



Channel B: SO-DIMM

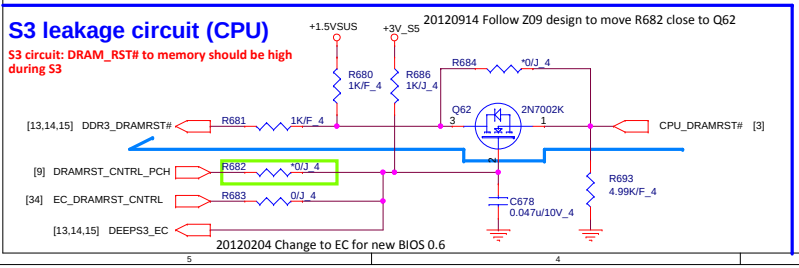




20120112 for memory down PU CAP.

S3 leakage circuit (CPU)

S3 circuit: DRAM_RST# to memory should be high during S3



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Size	Document Number	Rev
	Ivy Bridge 3/5 (DDR3 I/F)	1A

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IVY Bridge Processor (POWER) (CPU)

IVY Bridge Processor (GRAPHIC POWER) (CPU)

CPU VCCIO
IVY 17W:8.5A

SNB : Spec	Cose down
330uF/6mohm x 2	330uF/6mohm x 1
10uF x 10	10uF x 10
1uF x 26	1uF x 26

CPU VCCAXG
IVY 17W:TDC 18A

Spec	Cose down
3.9mΩ/LoadlineDesign	3.9mΩ/LoadlineDesign
total : 1uF x 11	total : 1uF x 11
total : 10uF x 6	total : 10uF x 12
total : 22uF x 6	tatal : 470u x 1(power side*2)
tatal : 470u x 1(power side*2)	

CPU VDDQ
IVY 45W: 5A

Spec
330uF/6mohm x 1
10uF x 8
1uF x 10

CPU Core Power
IVY 17W:TDC 33A

IVY SPEC
1.9mΩ/LoadlineDesign
total : 2.2uF x 35
total : 22uF x 12
tatal : 470u x3(Power side*1)

Cose down
IVY SPEC
1.9mΩ/LoadlineDesign
total : 2.2uF x 35
total : 10uF x 12
tatal : 470u x1(Power side*1)

IVY SPEC
22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

Voltage selection for VCCIO: this pin must be pulled high on the motherboard

On CRB
H_SNB_IVB#_PWRCTRL = low, 1.0V
H_SNB_IVB#_PWRCTRL = high/NC, 1.05V

CPU VCCPL
IVY 17W:1.5A

Spec	Real
330uF/7mohm x 1	10uF x 1
1uF x 2	1uF x 2

IVY SPEC
330uF x1, 10uF_8 x1, 1uF_4 x2
Socket BOT edge.

IVY SPEC
330uF x1, 10uF_8 x1 Socket BOT edge, 10uF_8 x2 Socket BOT cavity.

CPU VCCSA
IVY 17W: 6A

Spec

330uF/7mohm x 1	Real
10uF x 5	10uF x 3
1uF x 5	

VCCAXG_SENSE/VSSAXG_SENSE R=100, Trace impedance 15.5~34.5, <25mils.

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

20121203 : Add 39pF for ESD

S3	STUFF	NO_STUFF
enable	-	R5347/R6362
disable	R5347/R6362	-

S3 circuit: 1.5V input to IVB is gated & IVB Read Vref 0.75V is gated

4.5A

20111024 from +1.5VSUS change to +1.5V_CPU

For IV Bridge

VID[0]	VID[1]	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

For SN Bridge

VID[1]	+VCCSA
0	0.9V
1	0.8V

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK

Place PU resistor close to CPU

SVID DATA

Place PU resistor close to CPU

SVID ALERT

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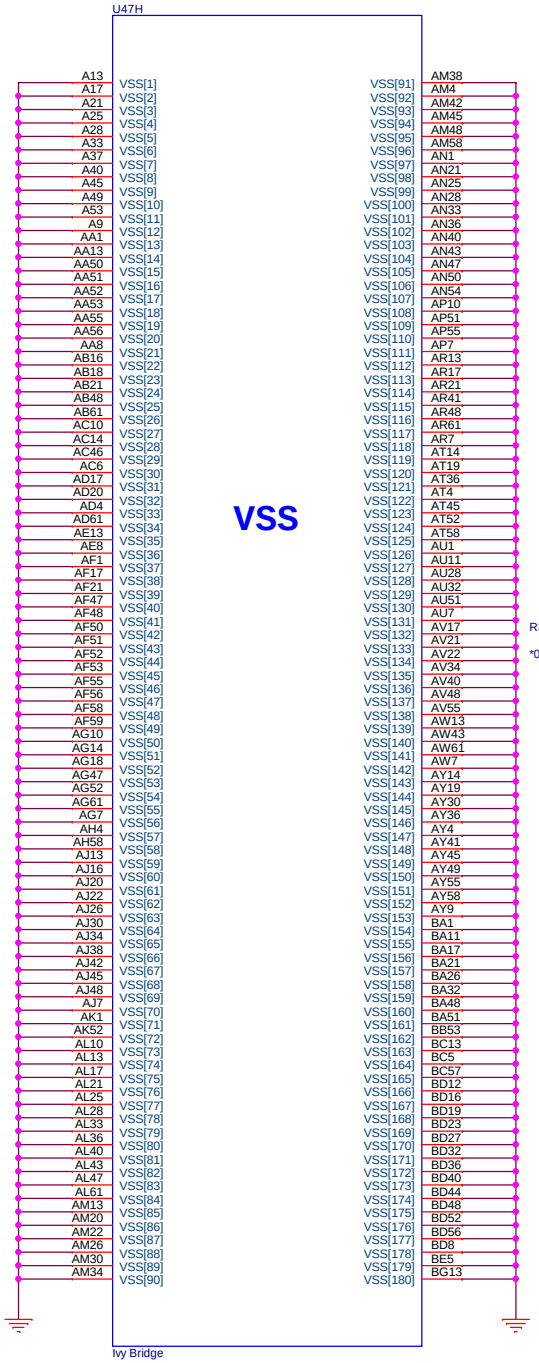
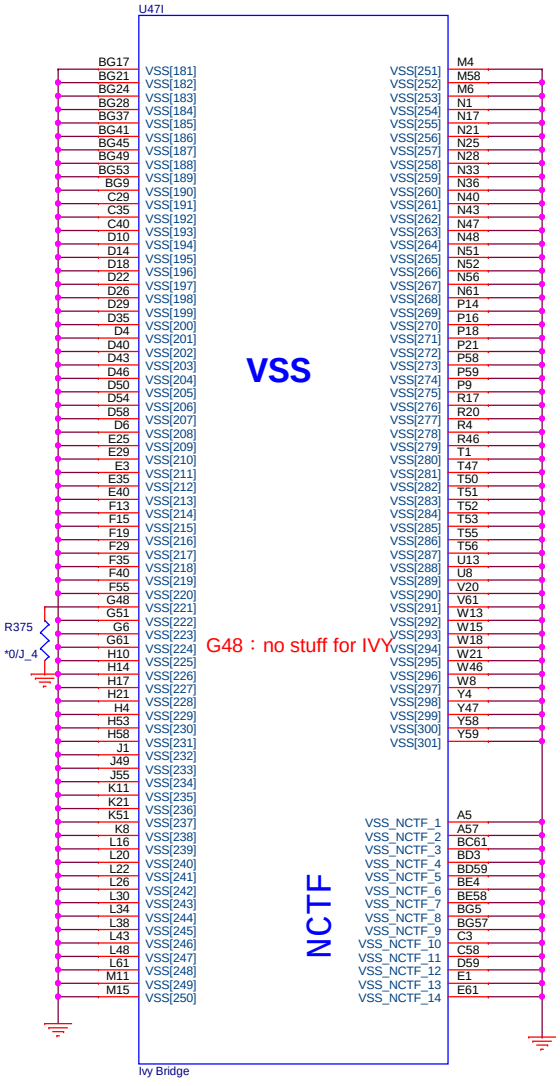
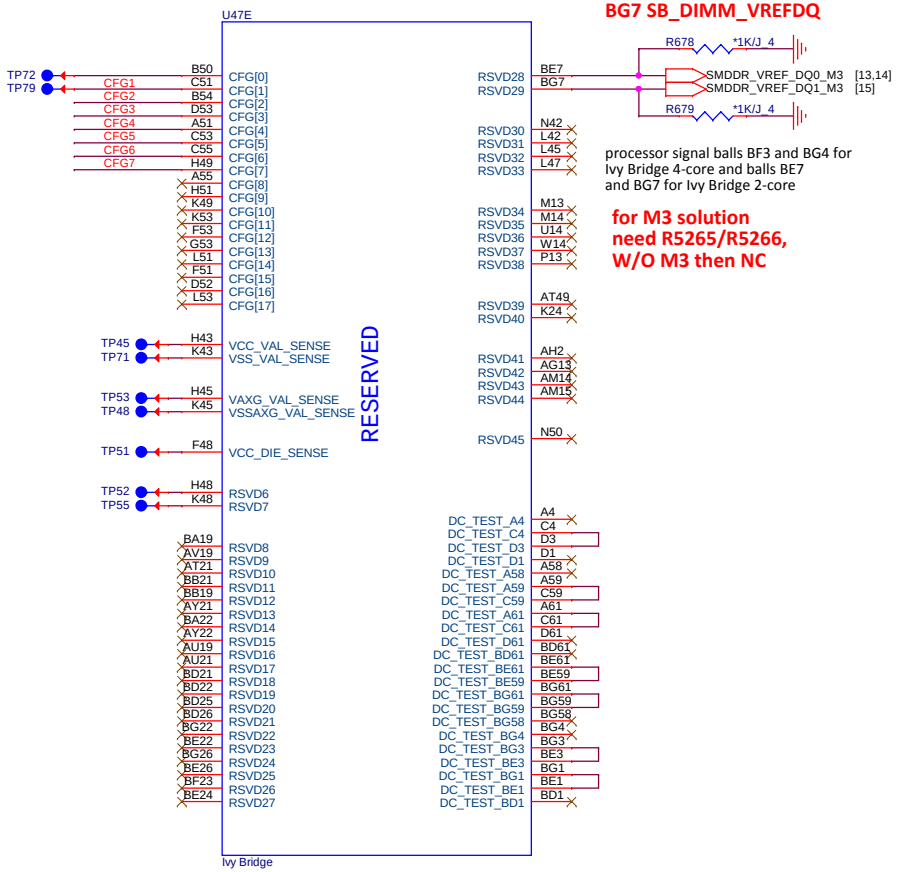
Size	Document Number	Rev
	Ivy Bridge 4/5 (POWER)	1A
Date: Monday, January 07, 2013	Sheet 5 of 46	

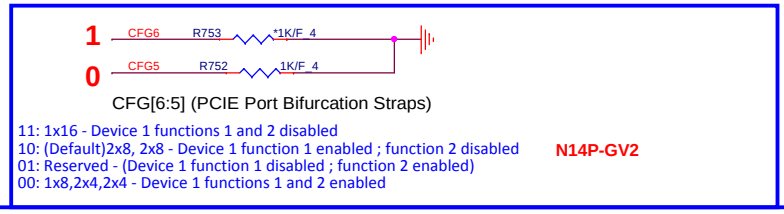
IVY Bridge Processor (GND) (CPU)





IVY Bridge Processor (RESERVED, CFG) (CPU)

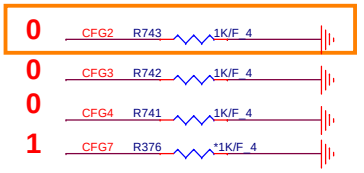




Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	**Lane Reversed**
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	**Lane Reversed**
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	**Enable; An ext DP device is connected to eDP**
CFG7 (PEG Defer Training)	**PEG train immediately following xxRESETB de assertion**	PEG wait for BIOS training



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Size	Document Number	Rev
	Ivy Bridge 5/5 (GND)	1A

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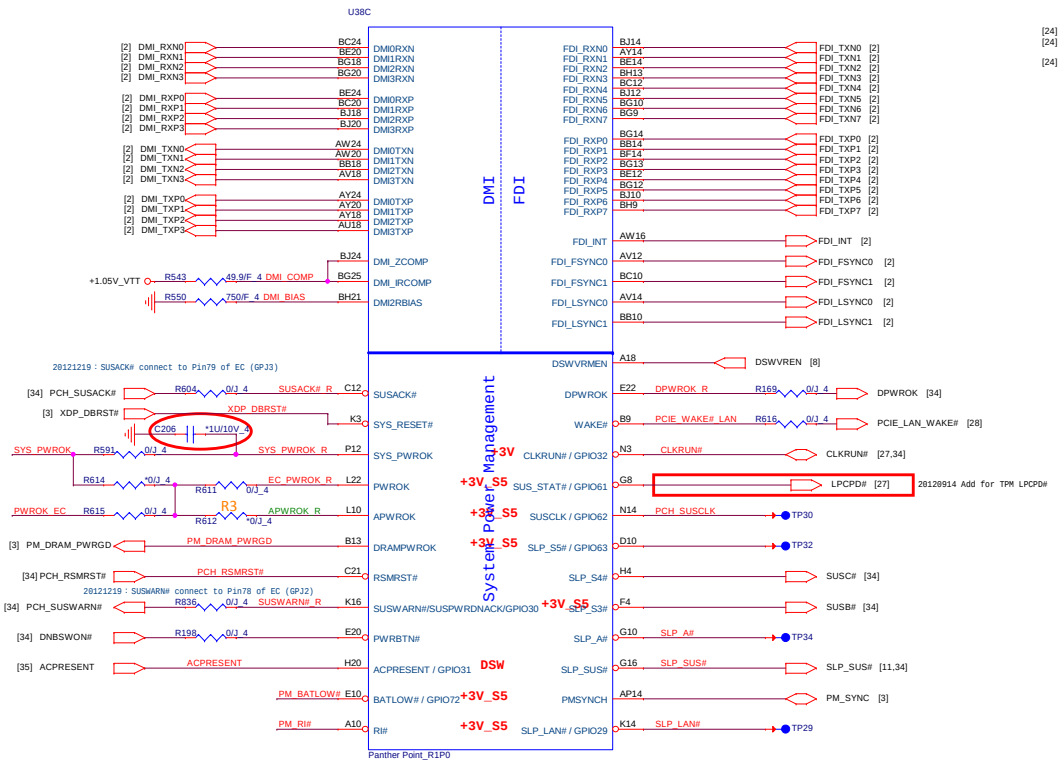
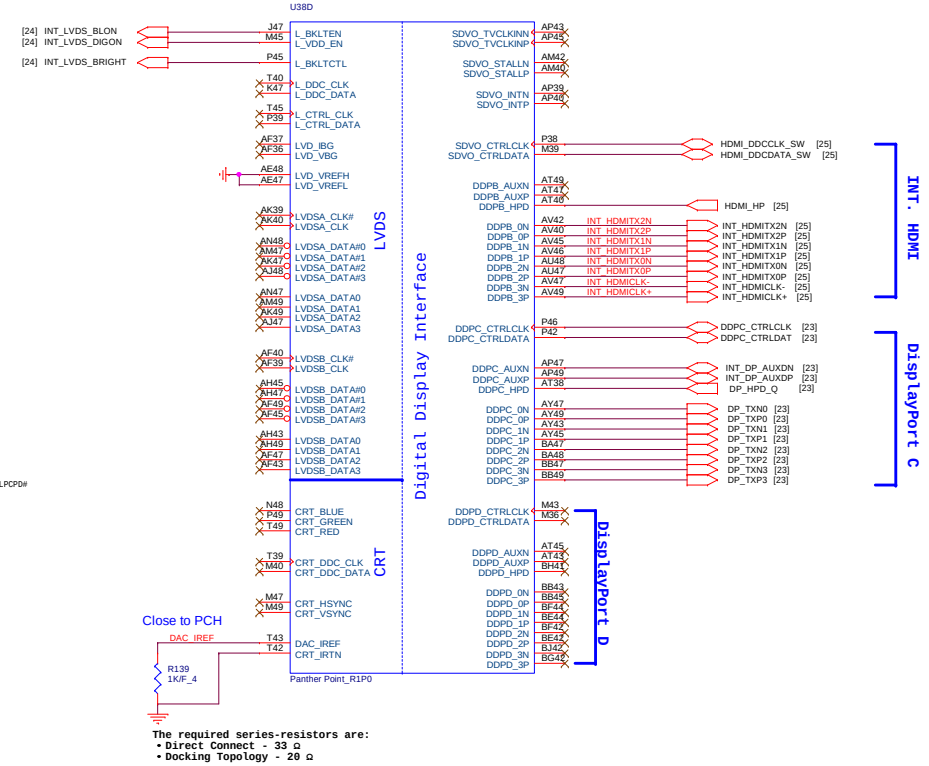
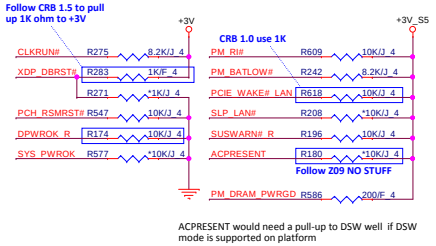
CPT/PPT (DMI,FDI,PM) (CLG)



CPT/PPT (LVDS,DDI)



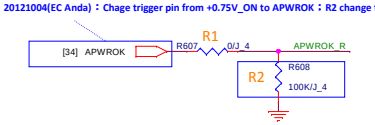
PCH Pull-high/low (CLG)



ACPRESENT would need a pull-up to DSW well if DSW mode is supported on platform

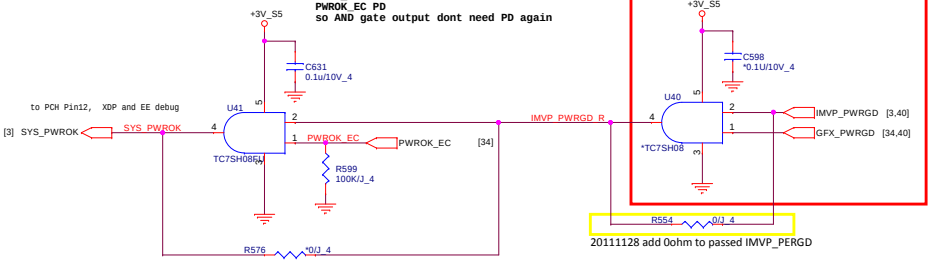
20120706:Speed up 250ms to boot up
R1,R2,R3 for EC power on 250 ms

20121004(EC Anda)：Chage trigger pin from +0.75V_ON to APWROK：R2 change to 100K



System PWR_OK (CLG)

IMVP_PWRGD PU +3V
PWROK_EC PD
so AND gate output dont need PD again



20111128 add 0ohm to passed IMVP_PERGD

include GFX_PWRGD to SYS_PWROK for PCH check

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PROJECT : ZQK

Size	Document Number	Rev
	PCH 1/6 (DMI/FDI/VIDEO)	1A

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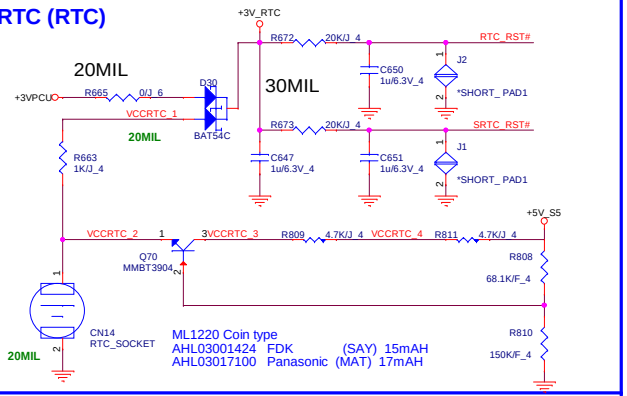
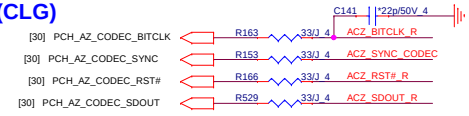
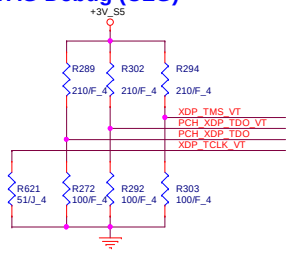
RTC (RTC)



HDA Bus (CLG)

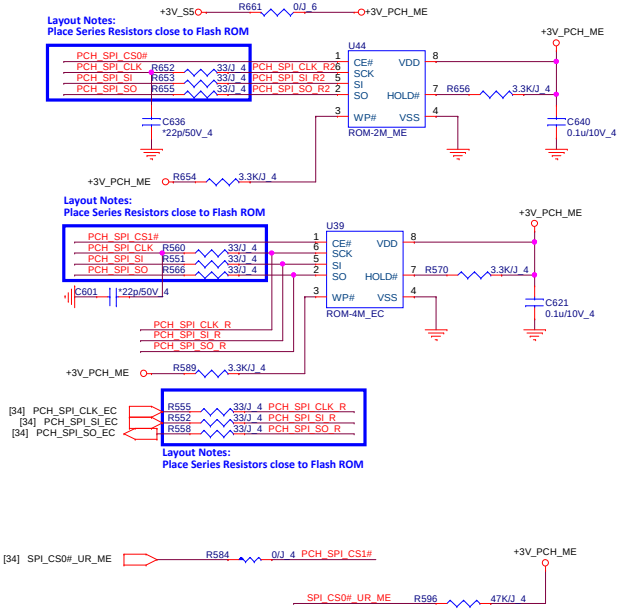


PCH JTAG Debug (CLG)



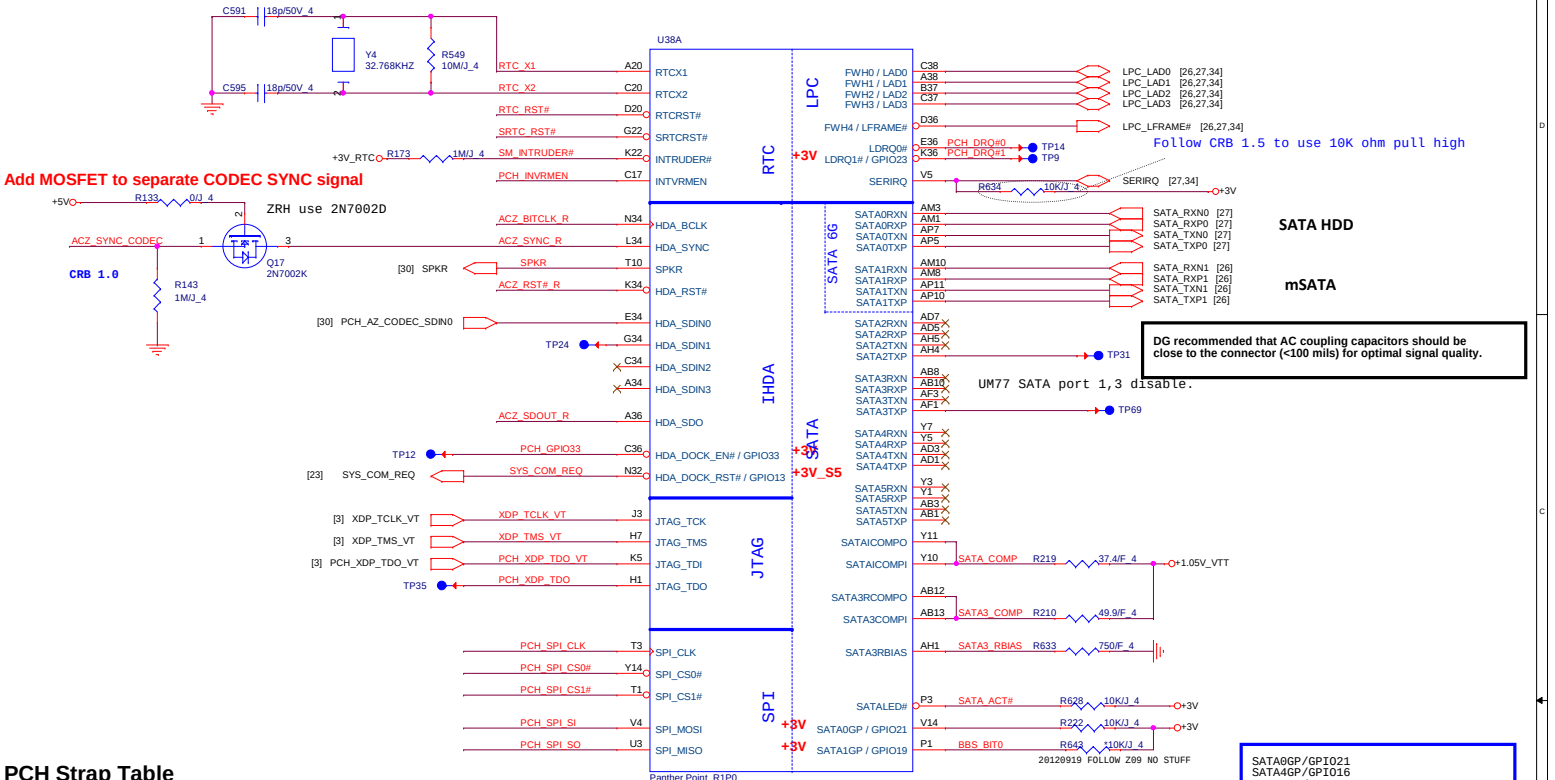
PCH Dual SPI (CLG) (Default for WIN8)

W25Q32BVSSIG / AKE391P0N00------>4MB
W25Q16BVSSIG / AKE38FP0N01----->2MB



PCH2 (CLG)

CPT/PPT (HDA,JTAG,SATA) (CLG)

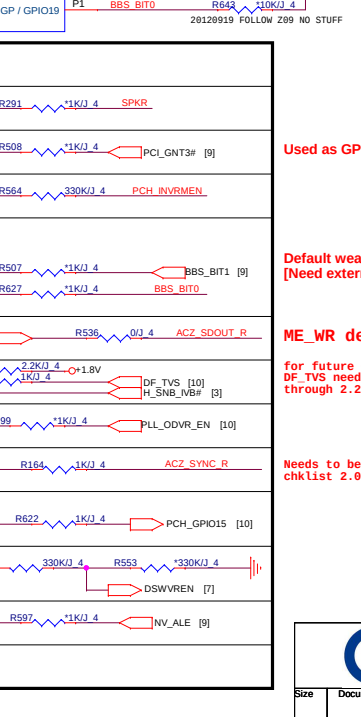


PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	

GNT1#	GPIO19	Boot Location
1	1	SPI *
0	0	LPC

HDA_SDO	Flash Descriptor Security	RSMRST	0 = effect (default)(weak pull-down 20K) 1 = overridden
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss (weak pull-down 20K) 1 = Set to Vcc
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 10K)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite internal PD	RSMRST	0 = Disable (Default) 1 = Enable
DSWVREN	DEEP S4/S5 well On Die DSW VR Enable	DSW	High = Enable (Default) Low = Disable
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)



Used as GPIO only. at chklist 1.2

Default weak pull-up on GNT0/1#
[Need external pull-down for LPC BIOS]

ME_WR# default EC setting folating

for future CPU, Sandy Bridge NC
DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kOhm ±5% - R8361 change to 0 or not??

Needs to be pulled High for Chief River platform chklist 2.0

Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	PCH 2/6 (SATA/RTC/HDA/LPC)	1A

Date: Monday, January 07, 2013 Sheet 8 of 46

CPT/PPT (PCI,USB,NVRAM) (CLG)

CPT/PPT (PCI-E,SMBUS,CLK)

20111122 add for Touch pad interrupt pin from GPIO13 to GPIO11.

Layout Notes:
USB3 TX AC cap place at connector side, AC cap to connector < 400mils

USB30 Port1: EXT USB3.0 Port
USB30 Port3: Mini DP port

MB USB WITH 3.0 PORT
MB USB 2.0 Port
Mini DP WITH 3.0 PORT
Touch Panel
DB USB 2.0 Port

EHCI1

USB Port1 can be used on debug mode
XHCI for USBP0-3

USB port6/7 may not be available on all PCH sku (HM55 support 12port only)

Camera
BT+WL

USB Port9 can be used on debug mode
1001：(BIOS) Use port1 is enough
EHCI2

UM77 USB port 6,7,12,13 disable.

PCIE port 1 for commeral model S3 can't weak up.

Wireless
LAN

UM77/HM70 will disable 5~8 PCIE ports

20110908 WLAN support S3 wake up function.

Wireless
LAN

For LAN
For EC

PLTRST#(CLG)

20120522：follow CRB to modify power plan to +3V
check list 2.0：When connected to the processor the PLTRST# signal should be level shifted to 1.05V.

PCI/USBOC# Pull-up(CLG)

MPC Switch Control	
MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

CLK_REQ/Strap Pin(CLG)

SMBus(EC) (CLG)

SMBus(PCH) (CLG)

20120712：Add 0ohm reserved for two sides of SMBUS since they are the same power plane (CRB no level shift)

DDRIII Memory down strap (CLG)

Vender	RAM_IDn	Q PN	Mfr. PN	Freq.
Hynix	0000			
Elpida	0001	AKD5JGST400	EDJ4216EBBG-DJ-F	1333MHz
	0010	AKD5JGST407	EDJ4216EFBG-GNL-F	1600MHz

EV@: For Optimize SKU
IV@: For UMA SKU

	dGPU_PW_CTRL# (GPIO68) CTL : dGPU_VRON	SKU_ID1 (GPIO64)	SKU_ID0 (GPIO16)	VGA H/W Signal	Setup Menu	
UMA Only	1	0	0	UMA	Hidden	UMA boot
dGPU Only	0 or 1	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	0	1	0	UMA+GPU	dGPU/SG	UMA boot
Optimize (Muxless)	0	1	1	UMA	UMA/SG	UMA boot

dGPU_PW_CTRL#
1 = GPU power is control by H/W (pure Discrete SKU)
0 = GPU power is control by PCH GPIO (Discrete, SG or Optimize)

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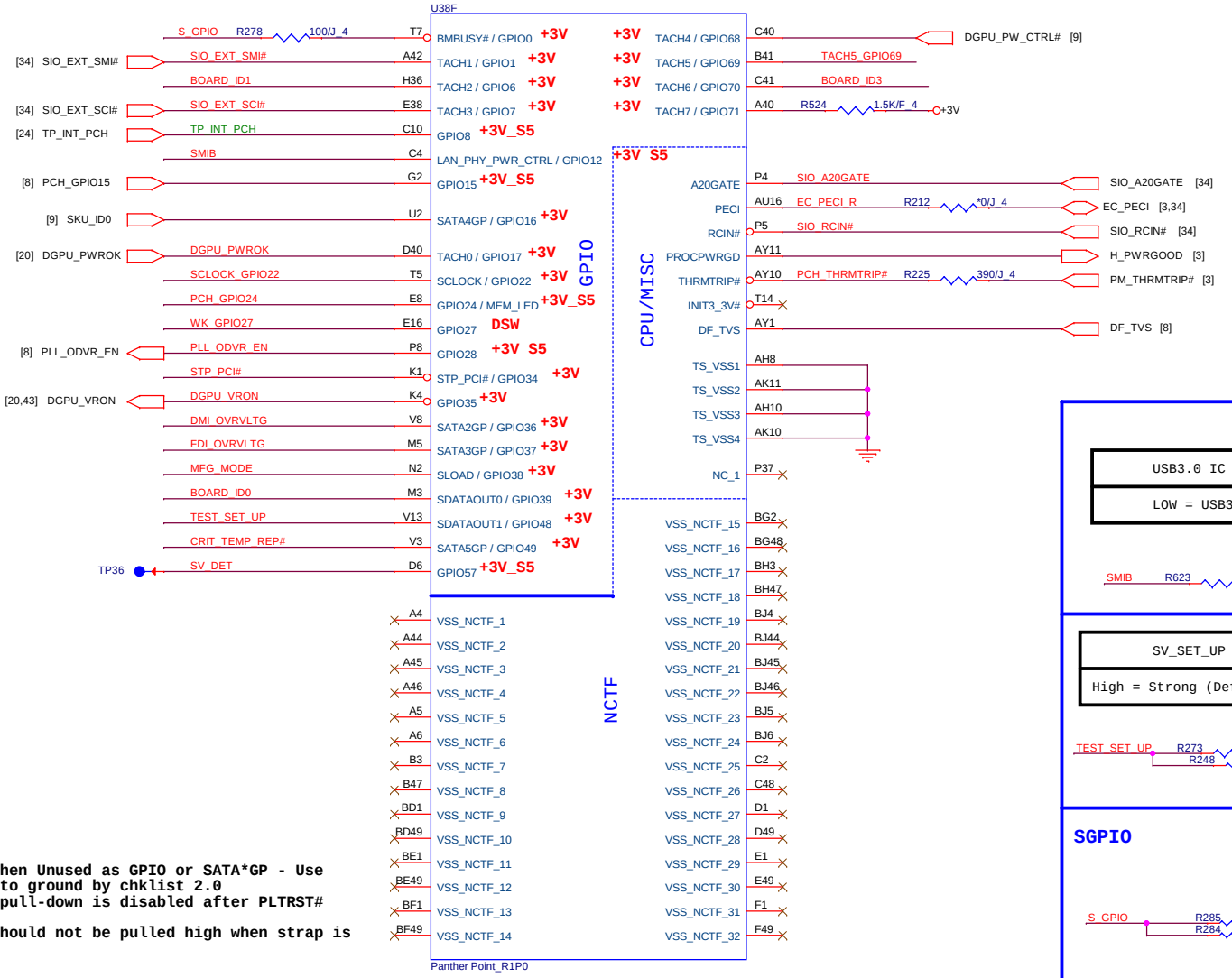
PROJECT : ZQK
Size: Document Number: PCH 3/6 (PCIE/USB/CLK/SMB) Rev: 1A
Date: Monday, January 07, 2013 Sheet 9 of 46

CPT/PPT (GPIO,VSS_NCTF,RSVD) (CLG)

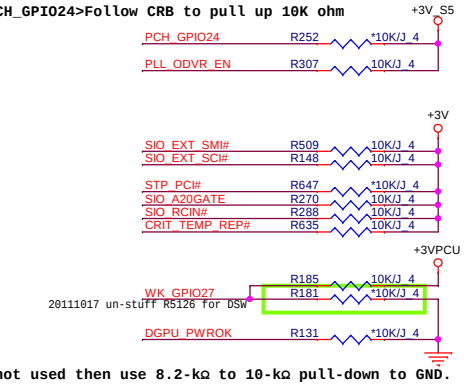


SATA2GP/SATA3GP : When Unused as GPIO or SATA*GP - Use 8.2K-10K pull-down to ground by chklist 2.0
NOTE: The internal pull-down is disabled after PLTRST# deasserts.
NOTE: This signal should not be pulled high when strap is sampled.

GPIO Pull-up/Pull-down (CLG)

10

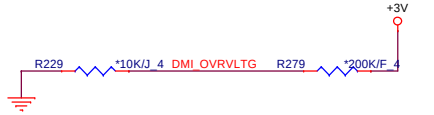
20120625 : <PCH_GPIO24>Follow CRB to pull up 10K ohm



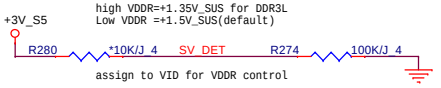
GPIO27 : If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

USB3.0 IC CTL
LOW = USB3.0 IC

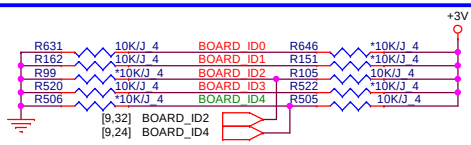
DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)



SV_SET_UP
High = Strong (Default)



SGPIO

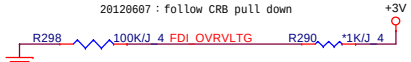


	High	Low
BOARD_ID0	GDDR5	DDR3
BOARD_ID1	Disable on board memory	Enable on board memory
BOARD_ID2	Pin8 of SYNAPTICS and ELAN are NC pin Default is pull high BIOS maybe will use EEPROM detection	
BOARD_ID3		
BOARD_ID4	No touch panel	Touch panel

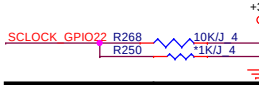
2011/09/01 add select resistor

LVDS = Pull HIGH eDP = Pull LOW

20120607 : follow CRB pull down



FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage



G_SENSOR_ID	High = Disable (Default) Low = Enable

MFG-TEST

Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	PCH 4/6 (GPIO/MISC)	1A
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CPT/PPT (POWER) (CLG)

VccCORE =1.3 A(60mils)

VccIO =2.925 A(140mils)

VccADAC =1mA(8mils)

When Dis sku and eDP , LVDS power can short to GND

VCCDMI = 42mA(10mils)

+1.1V VCC_DMI widthh >= 20mils.

VCCCLKDMI = 20mA(8mils)

VCCPNAND = 190 mA(15mils)

VCCSPI = 20mA(8mils)

+1.1V VCC_DMI widthh >= 20mils.

VccDMI needs to be powered by the same 1.05 V voltage source as the CPU VCCIO, and the trace needs to be at least 20 mils width with full VSS/VCC reference plane.

VCCVRM: 1.0V (Destop) 0.720 del for Pre-ES1
1.5V (Mobile)

20120105 change power plant to +3V for power saving.

Reserve +3V_S5 to VCCSPI for EC 795 co-layout

CPT/PPT (POWER) (CLG)

VCCDSW3_3= 3mA

20120104 change power plant from +3V_S5 to +3VPCU.

VCCME(+1.05V) = ??A(??mils)

VccASW =1.01 A(60mils)

20120216 remove R168 for power plant chnge to +1.05V_VTT.

+1.1V VCC_DMI witdth >= 20mils.

65mA(10mils)
8mA(8mils)

VCCDIFFCLKN= 55mA(18mils)

VCCSSC= 95mA(10mils)

1mA(8mils)

20120216 remove R172 for power plant chnge to +1.05V_VTT.

VCCRTC<1mA(8mils)

VCCSUS3_3 = 119mA(15mils)

VCC5REFSUS=1mA

VSREF= 1mA

VCCSUS3_3 = 119mA(15mils)

VCCPCORE = 28mA(10mils)

??mA(??mils)

VCCVRM= 114mA(15mils)

VCCME = 1.01A(60mils)

VCCSUSHDA= 10mA(8mils)

20111018 ADD DSW Cricuit
20111030 modify cuirucit.

Quanta Computer Inc.
PROJECT :ZQK

Size	Document Number	Rev
	PCH 5/6 (POWER)	1A
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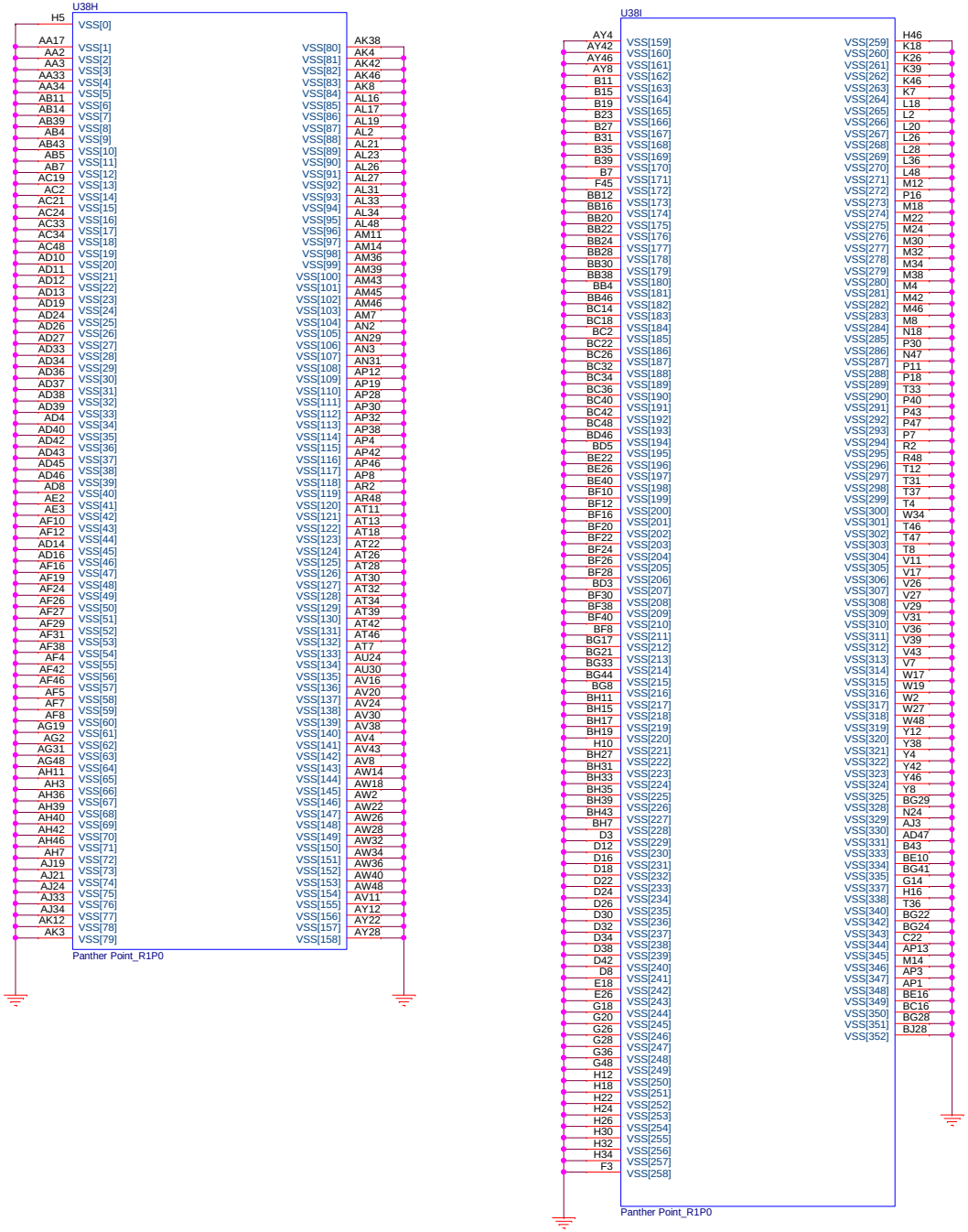
IBEX PEAK-M (GND) (CLG)



Quanta Computer Inc.		
PROJECT : ZQK		
Size	Document Number: PCH 6/6 (GND)	Rev: 1A
Date: Monday, January 07, 2013	Sheet 12 of 46	

DDR ON BOARD RAM (DDR)

Checklist 2.0:
M3 has to be no stuff on Chief River

BYTE0_0-7
BYTE1_8-15
BYTE2_16-23
BYTE3_24-31
BYTE4_32-39
BYTE5_40-47
BYTE6_48-55
BYTE7_56-63

SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34

Should be 240 Ohms +-1%

Place these Caps near Memory Down

SPD address= A0 hex (for MD devices)

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

WP =1 : WRITE DISABLE

CRB Add

Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	DDR3 MEMORY DOWN X 16	1A

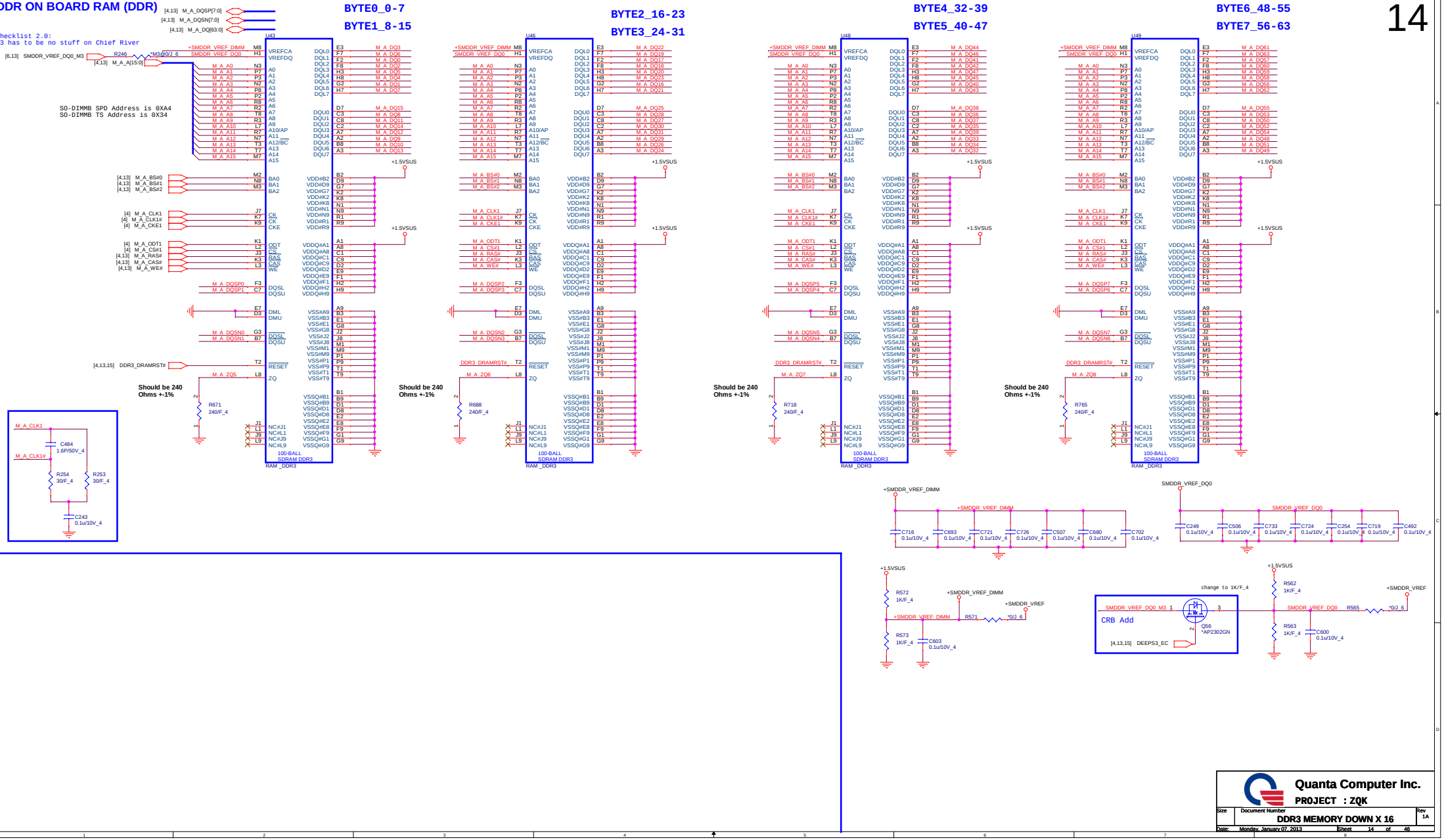
Date: Monday, January 07, 2013 Sheet 13 of 46

DDR ON BOARD RAM (DDR)

Checklist 2.0:
M3 has to be no stuff on Chief River

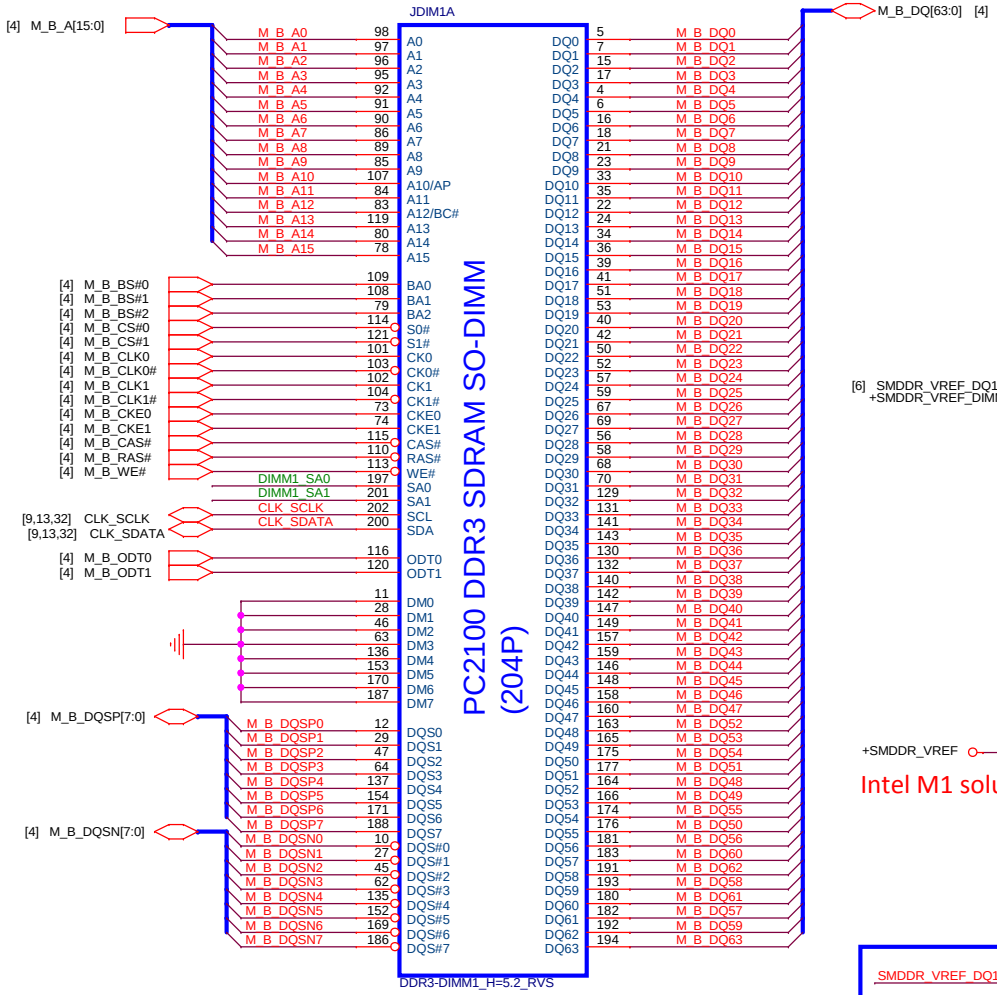
SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34

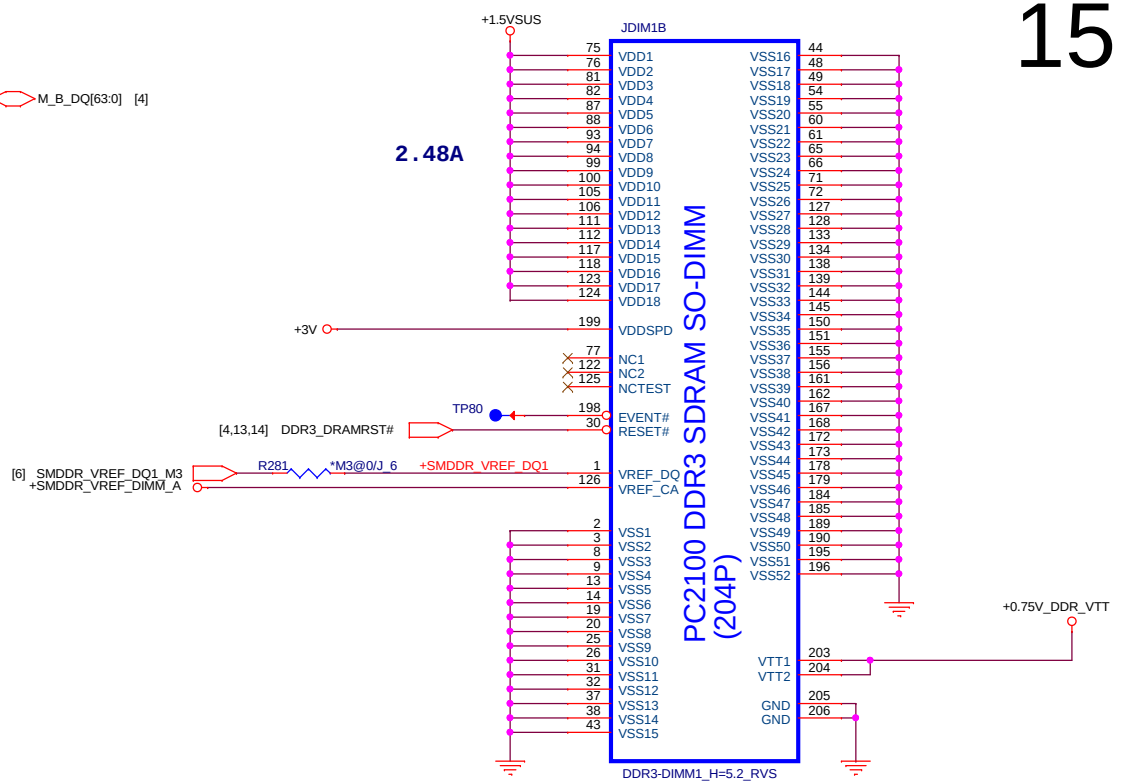
BYTE0_0-7
BYTE1_8-15
BYTE2_16-23
BYTE3_24-31
BYTE4_32-39
BYTE5_40-47
BYTE6_48-55
BYTE7_56-63

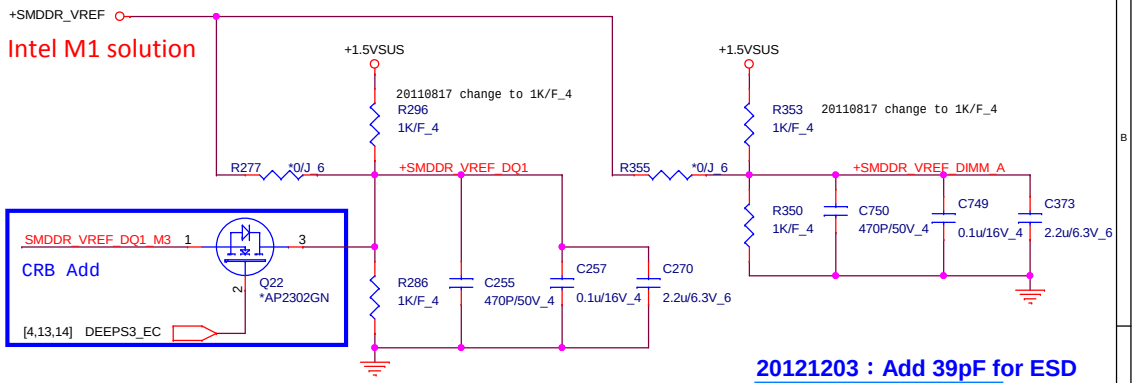


Quanta Computer Inc.	
PROJECT : ZQK	
Size	Document Number: DDR3 MEMORY DOWN X 16 — Rev: 1A
Date: Monday, January 07, 2013	Sheet 14 of 46

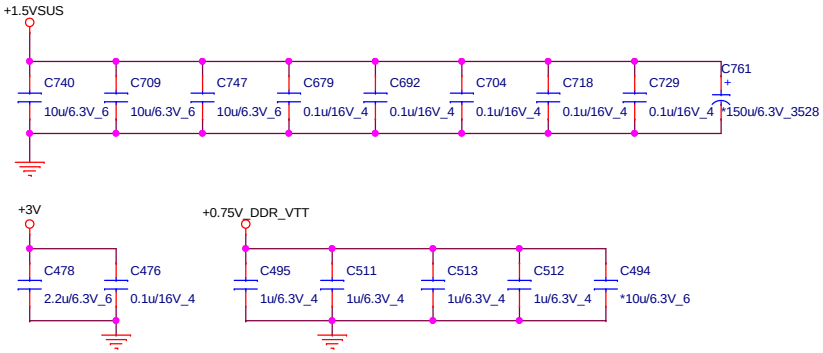
DDR3 DIMM-A (DDR)

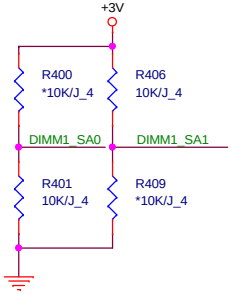






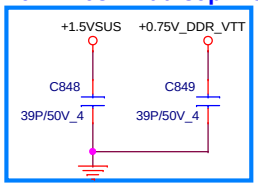
Place these Caps near SO_DIMM-A





	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

20121203 : Add 39pF for ESD



Quanta Computer Inc.

PROJECT : ZQK

Size	Document Number	Rev
	DDR3 DIMMA-RSV H=5.2	1A
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Layout Notes:
+1.05_GFX trace width = 250mils

1000mA

+1.05V_GFX

To be placed no further from the GPU than bewteen BGA and Power supply
C207 EV@22u/6.3V_8
C208 EV@22u/6.3V_8
C171 EV@10u/6.3V_6
C183 EV@10u/6.3V_6
place near balls
C158 EV@4.7u/6.3V_6
C147 EV@1u/6.3V_4
place under BGA
C154 EV@1u/6.3V_4

+1.05V_GFX
C226 EV@22u/6.3V_8
To be placed no further from the GPU than bewteen BGA and Power supply
C225 EV@22u/6.3V_8
C246 EV@10u/6.3V_6
C247 EV@10u/6.3V_6
place near balls
C178 EV@4.7u/6.3V_6
C149 EV@1u/6.3V_4
place under BGA
C148 EV@1u/6.3V_4

2500mA

U35A

AG19 PEX_IOVDD_1
AG21 PEX_IOVDD_2
AG22 PEX_IOVDD_3
AG24 PEX_IOVDD_4
AH21 PEX_IOVDD_5
AH25 PEX_IOVDD_6

AG13 PEX_IOVDDQ_1
AG15 PEX_IOVDDQ_2
AG16 PEX_IOVDDQ_3
AG18 PEX_IOVDDQ_4
AG25 PEX_IOVDDQ_5
AH15 PEX_IOVDDQ_6
AH18 PEX_IOVDDQ_7
AH26 PEX_IOVDDQ_8
AH27 PEX_IOVDDQ_9
AJ27 PEX_IOVDDQ_10
AK27 PEX_IOVDDQ_11
AL27 PEX_IOVDDQ_12
AM28 PEX_IOVDDQ_13
AN28 PEX_IOVDDQ_14

[PEG Interface]

PEX_RX0	AN12	PEG_TX8_C	C629	EV@0.22u/10V_4
PEX_RX0_N	AM12	PEG_TX#8_C	C628	EV@0.22u/10V_4
PEX_RX1	AN14	PEG_TX9_C	C611	EV@0.22u/10V_4
PEX_RX1_N	AM14	PEG_TX#9_C	C612	EV@0.22u/10V_4
PEX_RX2	AP14	PEG_TX10_C	C627	EV@0.22u/10V_4
PEX_RX2_N	AP15	PEG_TX#10_C	C626	EV@0.22u/10V_4
PEX_RX3	AN15	PEG_TX11_C	C610	EV@0.22u/10V_4
PEX_RX3_N	AM15	PEG_TX#11_C	C609	EV@0.22u/10V_4
PEX_RX4	AN17	PEG_TX12_C	C624	EV@0.22u/10V_4
PEX_RX4_N	AM17	PEG_TX#12_C	C625	EV@0.22u/10V_4
PEX_RX5	AP17	PEG_TX13_C	C608	EV@0.22u/10V_4
PEX_RX5_N	AP18	PEG_TX#13_C	C607	EV@0.22u/10V_4
PEX_RX6	AN18	PEG_TX14_C	C623	EV@0.22u/10V_4
PEX_RX6_N	AM18	PEG_TX#14_C	C622	EV@0.22u/10V_4
PEX_RX7	AN20	PEG_TX15_C	C605	EV@0.22u/10V_4
PEX_RX7_N	AM20	PEG_TX#15_C	C606	EV@0.22u/10V_4
PEX_RX8	AP20			
PEX_RX8_N	AP21			
PEX_RX9	AN21			
PEX_RX9_N	AM21			
PEX_RX10	AN23			
PEX_RX10_N	AM23			
PEX_RX11	AP23			
PEX_RX11_N	AP24			
PEX_RX12	AN24			
PEX_RX12_N	AM24			
PEX_RX13	AN26			
PEX_RX13_N	AM26			
PEX_RX14	AP26			
PEX_RX14_N	AP27			
PEX_RX15	AN27			
PEX_RX15_N	AM27			

PEG_TX8 [2]
PEG_TX#8 [2]
PEG_TX9 [2]
PEG_TX#9 [2]
PEG_TX10 [2]
PEG_TX#10 [2]
PEG_TX11 [2]
PEG_TX#11 [2]
PEG_TX12 [2]
PEG_TX#12 [2]
PEG_TX13 [2]
PEG_TX#13 [2]
PEG_TX14 [2]
PEG_TX#14 [2]
PEG_TX15 [2]
PEG_TX#15 [2]

LAYOUT NOTES:
UNDAER: WITHIN 150MILS
NEAR: WITHIN 1378MILS

PEX_TX0	AK14	PEG_RX8_C	C197	EV@0.22u/10V_4
PEX_TX0_N	AJ14	PEG_RX#8_C	C198	EV@0.22u/10V_4
PEX_TX1	AH14	PEG_RX9_C	C216	EV@0.22u/10V_4
PEX_TX1_N	AG14	PEG_RX#9_C	C217	EV@0.22u/10V_4
PEX_TX2	AK15	PEG_RX10_C	C214	EV@0.22u/10V_4
PEX_TX2_N	AJ15	PEG_RX#10_C	C215	EV@0.22u/10V_4
PEX_TX3	AL16	PEG_RX11_C	C195	EV@0.22u/10V_4
PEX_TX3_N	AK16	PEG_RX#11_C	C196	EV@0.22u/10V_4
PEX_TX4	AK17	PEG_RX12_C	C213	EV@0.22u/10V_4
PEX_TX4_N	AJ17	PEG_RX#12_C	C212	EV@0.22u/10V_4
PEX_TX5	AH17	PEG_RX13_C	C194	EV@0.22u/10V_4
PEX_TX5_N	AG17	PEG_RX#13_C	C193	EV@0.22u/10V_4
PEX_TX6	AK18	PEG_RX14_C	C192	EV@0.22u/10V_4
PEX_TX6_N	AJ18	PEG_RX#14_C	C191	EV@0.22u/10V_4
PEX_TX7	AL19	PEG_RX15_C	C211	EV@0.22u/10V_4
PEX_TX7_N	AK19	PEG_RX#15_C	C210	EV@0.22u/10V_4
PEX_TX8	AK20			
PEX_TX8_N	AJ20			
PEX_TX9	AH20			
PEX_TX9_N	AG20			
PEX_TX10	AK21			
PEX_TX10_N	AJ21			
PEX_TX11	AL22			
PEX_TX11_N	AK22			
PEX_TX12	AK23			
PEX_TX12_N	AJ23			
PEX_TX13	AH23			
PEX_TX13_N	AG23			
PEX_TX14	AK24			
PEX_TX14_N	AJ24			
PEX_TX15	AL25			
PEX_TX15_N	AK25			

PEG_RX8 [2]
PEG_RX#8 [2]
PEG_RX9 [2]
PEG_RX#9 [2]
PEG_RX10 [2]
PEG_RX#10 [2]
PEG_RX11 [2]
PEG_RX#11 [2]
PEG_RX12 [2]
PEG_RX#12 [2]
PEG_RX13 [2]
PEG_RX#13 [2]
PEG_RX14 [2]
PEG_RX#14 [2]
PEG_RX15 [2]
PEG_RX#15 [2]

1001：Remove 3V3MISC by FAE Nelson suggestion
FAE：Please use +3V_GFX to instead 3V3MISC power rail

1001：Remove 3V3MISC's Cap by FAE Nelson suggestion

PLACE NEAR TO GPU BALLS

PLACE UNDER GPU BALLS

AC6 NC_1
AJ28 NC_2
AJ4 NC_3
AJ5 NC_4
AL11 NC_5
C15 NC_6
D19 NC_7
D20 NC_8
D23 NC_9
D26 NC_10
H31 NC_11
T8 NC_12
V32 NC_13

1001：Remove 3V3MISC by FAE Nelson suggestion
FAE：Please use +3V_GFX to instead 3V3MISC power rail

+3V_GFX
L8/M8/K8/J8 0.4MM = 16mils

J8 VDD33_1
K8 VDD33_2
L8 VDD33_3
M8 VDD33_4

PLACE NEAR TO GPU L8/M8
+3V_GFX
C144 EV@4.7u/6.3V_6
C152 *EV@1u/6.3V_4
C153 EV@0.1u/10V_4
C59 EV@0.1u/10V_4
C65 *EV@0.1u/10V_4
PLACE UNDAER GPU BALLS L8/M8

EV@N14P_GV2

PEX_REFCLK	AL13	CLK_PCIE_VGAP [9]		
PEX_REFCLK_N	AK13	CLK_PCIE_VGAN [9]		
PEX_TSTCLK_OUT	AJ26	PEX_TSTCLK	R186	*EV@200/F_4
PEX_TSTCLK_OUT_N	AK26	PEX_TSTCLK#		
PEX_WAKE	AJ11	PEGX_WAKE	TP26	
PEX_RST_N	AJ12	PEGX_RST#		
PEX_CLKREQ_N	AK12	PEX_CLKREQ#		
PEX_TERMP	AP29	PEX_TERMP	R590	EV@2.49K/F_4
TESTMODE	AK11	TESTMODE	R195	EV@10K/F_4
PEX_PLLVDD	AG26	PEX_PLLVDD	R207	EV@0_6
PEX_PLL_HVDD	AH12			
PEX_SVDD_3V3	AG12			
3.3V_AUX_NC	P8			
VDD_SENSE	L4			
GND_SENSE	L5			

0815 change R53 to 1% tolerance

0817 RSVD R46 and C49 for GV2 co-layout sDDR3

PEX_PLLVDD : 0.3MM = 12mils (150mA)

+1.05V_GFX

C185 EV@4.7u/6.3V_6
C145 EV@1u/6.3V_4
C163 EV@0.1u/10V_4
Place near BGA
PLACE UNDAER BALLS
C199 *EV@1u/6.3V_4

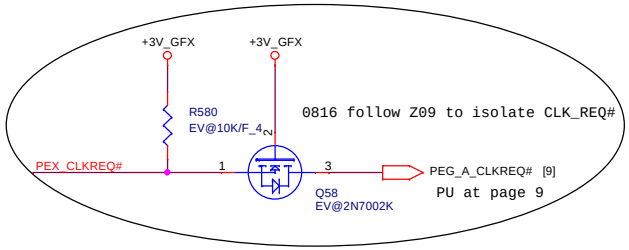
C72 EV@0.1u/10V_4
C89 EV@4.7u/6.3V_6
C99 EV@4.7u/6.3V_6
+3V_GFX
PLACE NEAR BALLS

AH12/AG12 need 210mA of +3V_GFX

GPU_VCCP_SENSE [43]
GPU_VSSP_SENSE [43]

8mils width (0.2MM)

Layout Notes:
Place decoupling CAPs close to GPU



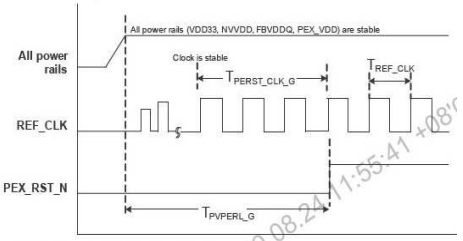
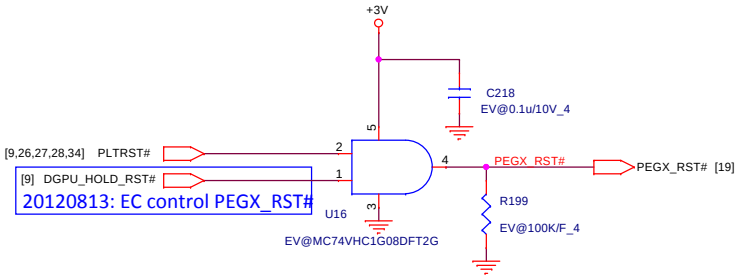


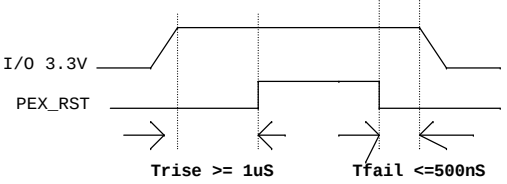
Figure 3-18. PEX_RST_N Timing for GPU

Table 3-8. N11x Reset Requirements for PCI Express 2.0

Constraint Parameter	Requirement	Notes
T_{PVPERL_G}	$T_{PVPERL\_G} \geq 1us$	
$T_{PERST\_CLK\_G}$	$T_{PERST\_CLK\_G} \geq 1T_{REF\_CLK}$	



PEX_RST timing



Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	DGPU 1/5 (PEG)	1A
Date: Monday, January 07, 2013	Sheet 16 of 46	

DBI

EDC

U35B [MEMORY I/F A]

U35C MEMORY I/F C

0816 follow DG to place caps

LAYOUT NOTES:
UNDAER: WITHIN 150MILS
NEAR: WITHIN 1378MILS

PLACE UNDER GPU BALLS

0.1u x 6 stuff x4

1u x 6 stuff x4

4.7u x 6 stuff x4

10u x 4 stuff x2

22u x 4 stuff x2

PLACE NEAR TO GPU BALLS

15mils width

0815 no stuff follow CRB

GC6 connect to EC

C6218 close ball K27 35mA

PLACE NEAR TO GPU BALLS
PLACE UNDER GPU BALLS

+FB_PLLAVDD = 0.3mm 12mils
U27+H17 62mA

1012(FAE)：Reserve +FB_PLLAVDD evan without CH-B

C107 close to ball H17

0815 confirm with ZQS (sDDR3)

0813
sDDR3
R1=42.2/F
R2=51.1/F

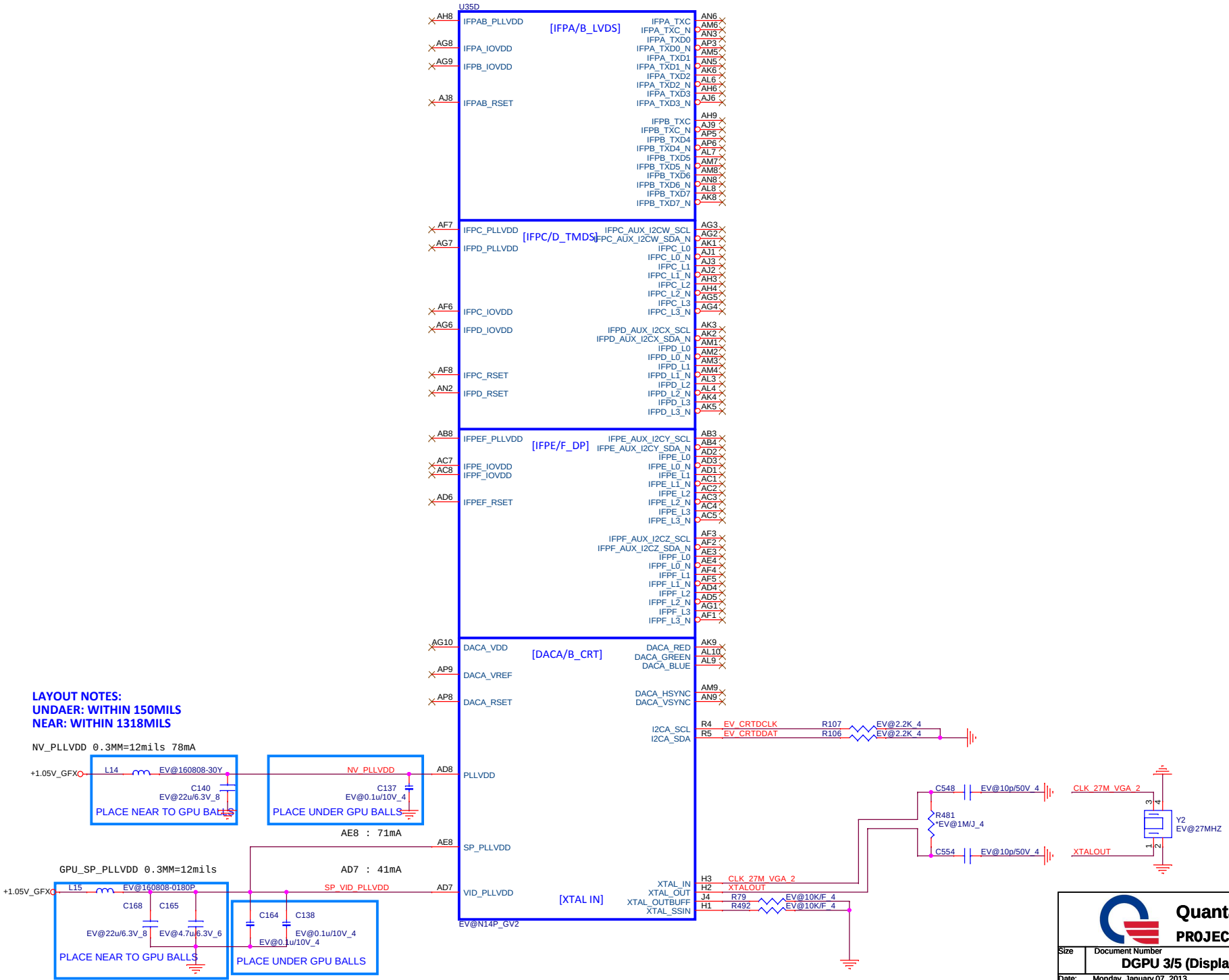
Layout Notes: PLACE CLOSE TO GPU BALLS

RSVD 330u, ZQS have one

EV@N14P_GV2

EV@N14P_GV2

Quanta Computer Inc.			
PROJECT : ZQK			
Size	Document Number		Rev
	DGPU 2/5 (Memory)		1A
Date: Monday, January 07, 2013		Sheet 17 of 46	


U35D
[IFPA/B_LVDS]
IFPAB_PLLVDD
IFPA_IOVDD
IFPB_IOVDD
IFPAB_RSET
IFPA_TXC
IFPA_TXC_N
IFPA_TXD0
IFPA_TXD0_N
IFPA_TXD1
IFPA_TXD1_N
IFPA_TXD2
IFPA_TXD2_N
IFPA_TXD3
IFPA_TXD3_N
IFPB_TXC
IFPB_TXC_N
IFPB_TXD4
IFPB_TXD4_N
IFPB_TXD5
IFPB_TXD5_N
IFPB_TXD6
IFPB_TXD6_N
IFPB_TXD7
IFPB_TXD7_N
[IFPC/D_TMDS]
IFPC_PLLVDD
IFPD_PLLVDD
IFPC_IOVDD
IFPD_IOVDD
IFPC_RSET
IFPD_RSET
IFPC_AUX_I2CW_SCL
IFPC_AUX_I2CW_SDA_N
IFPC_L0
IFPC_L0_N
IFPC_L1
IFPC_L1_N
IFPC_L2
IFPC_L2_N
IFPC_L3
IFPC_L3_N
IFPD_AUX_I2CX_SCL
IFPD_AUX_I2CX_SDA_N
IFPD_L0
IFPD_L0_N
IFPD_L1
IFPD_L1_N
IFPD_L2
IFPD_L2_N
IFPD_L3
IFPD_L3_N
[IFPE/F_DP]
IFPEF_PLLVDD
IFPE_IOVDD
IFPF_IOVDD
IFPEF_RSET
IFPE_AUX_I2CY_SCL
IFPE_AUX_I2CY_SDA_N
IFPE_L0
IFPE_L0_N
IFPE_L1
IFPE_L1_N
IFPE_L2
IFPE_L2_N
IFPE_L3
IFPE_L3_N
IFPF_AUX_I2CZ_SCL
IFPF_AUX_I2CZ_SDA_N
IFPF_L0
IFPF_L0_N
IFPF_L1
IFPF_L1_N
IFPF_L2
IFPF_L2_N
IFPF_L3
IFPF_L3_N
[DACA/B_CRT]
DACA_VDD
DACA_VREF
DACA_RSET
DACA_RED
DACA_GREEN
DACA_BLUE
DACA_HSYNC
DACA_VSYNC
I2CA_SCL
I2CA_SDA
R4 EV_CRTDCLK R107 EV@2.2K_4
R5 EV_CRTDDAT R106 EV@2.2K_4
[XTAL IN]
PLLVDD
SP_PLLVDD
VID_PLLVDD
XTAL_IN
XTAL_OUT
XTAL_OUTBUFF
XTAL_SSIN
H3 CLK_27M_VGA_2
H2 XTALOUT
J4 R79 EV@10K/F_4
H1 R492 EV@10K/F_4
EV@N14P_GV2
LAYOUT NOTES:
UNDAER: WITHIN 150MILS
NEAR: WITHIN 1318MILS
NV_PLLVDD 0.3MM=12mils 78mA
+1.05V_GFX
L14 EV@160808-30Y
C140 EV@22u/6.3V_8
PLACE NEAR TO GPU BALLS
NV_PLLVDD
C137 EV@0.1u/10V_4
PLACE UNDER GPU BALLS
AE8 : 71mA
AD7 : 41mA
GPU_SP_PLLVDD 0.3MM=12mils
+1.05V_GFX
L15 EV@160808-0180P
C168 C165
EV@22u/6.3V_8 EV@4.7u/6.3V_6
PLACE NEAR TO GPU BALLS
SP_VID_PLLVDD
C164 C138
EV@0.1u/10V_4 EV@0.1u/10V_4
PLACE UNDER GPU BALLS
C548 EV@10p/50V_4
R481 *EV@1M/J_4
C554 EV@10p/50V_4
CLK_27M_VGA_2
XTALOUT
Y2 EV@27MHZ
Quanta Computer Inc.
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Document Number
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Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	FB_1	FB_0	SMB_ALT_ADDR	VGA_DEVICE	1000
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM	1292
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0010
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	PCIE SPEED CHANGE GEN3	PCIE_MAX SPEED	DP_PLL_VDD33	0111

STRAP3
Optimus ---> 4.99k PD
Discrete only ---> 15K PD

Resistor P/N
4.99K---> CS24992FB26
10K ---> CS31002FB26
15K ---> CS31502FB24
20K ---> CS32002FB29
24.9K---> CS32492FB16
30.1K---> CS33012FB18
34.8K---> CS33482FB22
45.3K---> CS34532FB18

Table 123 Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SUB_VENDOR	10k Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See Note below
STRAP1	RAM_CFG[1]	10k Ω	See Note below
STRAP2	RAM_CFG[2]	10k Ω	See Note below
STRAP3	RAM_CFG[3]	10k Ω	See Note below
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND

N14M-GE device ID is 0x1140
N14M-GE is use binary strap setting
A.ROM_SI - 10K pull down
B.ROM_SO - 10K pull down
F.STRAP 3 - 10k pull down

Micron : MT41K256M16HA-107G:E (QPN = AKD5PGSTL05)
strap= 0xD =(0x1101)
STRAP 3&2&0 =10K Pull high
STRAP 1= 10K Pull down

1001 : Remove 3V3MISC by FAE Nelson suggestion
FAE : Please use +3V_GFX to instead 3V3MISC power rail

A.ROM_SI - Memeory strap
B.ROM_SO - 5K pull high
D.STRAP 0 - 45k pull high
E.STRAP 1 : GV2- 45K pull down
GT - 5K pull down
F.STRAP 3 - 5k pull down
C2.For N14P-GV2+SDDR3 sku
N14P-GV2 QS device ID=0x1292 'This is QS device ID
1.ROM_SCLK =5K pull high
2.STRAP2= 15k pull down
3.STRAP4=45 pull down 'For N14P-GV2 QS

N14P-GT device ID=0x0FE4
1.ROM_SCLK =15K pull down
2.STRAP2= 25k pull down
3.STRAP4=45K pull down

0817 : FB_CLAMP have PD, EC programing to avoid leakage
0928 FAE Nelson : Add a MOS to avoid power leakage issue pin 2 connect to +3V_GFX power rail

0928 FAE Nelson : Please add 10k pull up to +3V on FB_CLAMP_REQ# signal also

0816 EC programing GPI

PSI stuff 10k at GPU side ready, remove power page of pu 10k
GPIO20/21 available on N14P-GV2

R3	
N14x others	40.2K
N14M-GE/GL	NC

GPIO8 VGA thrmtrip# => inform EC over temperature protect

0816 dGPU_OTP# = EC control

GPIO9 for ADPS circuit to infrom EC NV dGPU VPS Alert

0816 dGPU_ALT# = EC control

0817 CEC is NC for GK107

0816 dGPU_OPP# = EC control

GPIO12 AC detect
AC high
DC low

0815 RSVD VGPU_TALERT# to throttle GPU power

GPIO12 HW throttle over power protect

SMBus (VGA)

1001 : Remove 3V3MISC by FAE Nelson suggestion
FAE : Please use +3V_GFX to instead 3V3MISC power rail

EC/SS

VGA/+3V_GFX

Table 3. N14M-GS/LP and N14P-GV2 DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
128Mx16 DDR3	Samsung	0x7	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production Candidate
				K4W2G1646E-BC11	900	1204	Production Candidate
	Micron	0x5	1.5 V/ 1.5 V	MT41J128M16JT-093G:K	1000	1150	Production Candidate
				MT41J128M16JT-107G:K	900	1150	Production Candidate
256Mx16 DDR3	Samsung	0x3	1.5 V/ 1.5 V	K4W4G1646B-HC11	900	H/A	Production Candidate
	Micron	0x1	1.5 V/ 1.5 V	MT41K256M16HA-107G:E	900	H/A	Production Candidate

Table 8. N14P-GS/LP/GE/GT DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
128M~16 DDR3	Samsung	0x7	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production ready
				K4W2G1646E-BC11	900	1204	Production ready
	Micron	0x5	1.5 V/ 1.5 V	MT41J128M16JT-093G:K	1000	1234	Production ready
				MT41J128M16JT-107G:K	900	1150	Production ready
	Hynix	0x6	1.5V/ 1.5V	H5TQ2G63DFR-H0C	1000	H/A	Production Candidate
				H5TQ2G63DFR-11C	900	H/A	Production Candidate

Table 2. N14M-GE/GL DDR3 Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
256M~16 DDR3	Samsung	0x8	1.5 V/ 1.5 V	K4W4G1646B-HC11	900	H/A	Production ready
	Micron	0xD	1.5 V/ 1.5 V	MT41K256M16HA-107G:E	900	H/A	Production ready
	Hynix	0x3	1.5V/ 1.5V	H5TQ4G63MFR-11C	900	H/A	Production ready
		0x4		H5TQ4G63AFR-11C		H/A	Post Production Candidate

Table 1. N14M-GE/GL DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
128M~16 DDR3	Micron	0x1	1.5 V/ 1.5 V	MT41J128M16JT-093G:K	1000	1234	Production ready
				MT41J128M16JT-107G:K	900	1150	Production ready
	Samsung	0x5	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production ready
				K4W2G1646E-BC11	900	1204	Production ready
	Hynix	0x6	1.5V/ 1.5V	H5TQ2G63DFR-H0C	1000	H/A	Production ready
				H5TQ2G63DFR-11C	900	H/A	Production ready

Vender	Strap	Q PN	Mfr. PN	Freq.	GPU
Micron	0001	AKD5PGSTL05	MT41K256M16HA-107G:E	900MHz	N14P-GT1 & GV2
Hynix	0110	AKD5MGWTW17	H5TQ2G63DFR-11C	900MHz	N14P-GT

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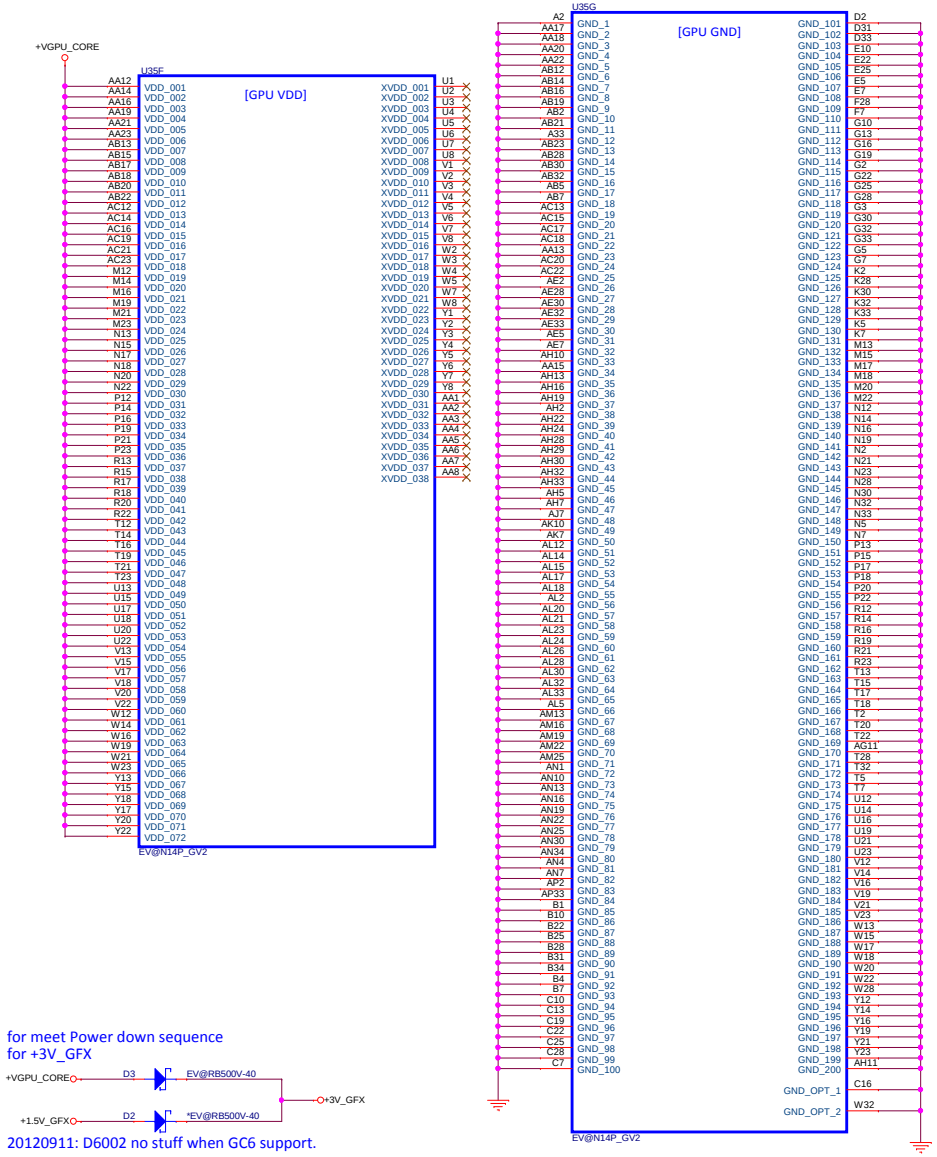
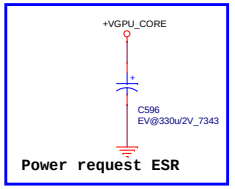
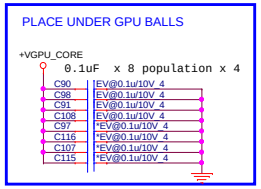
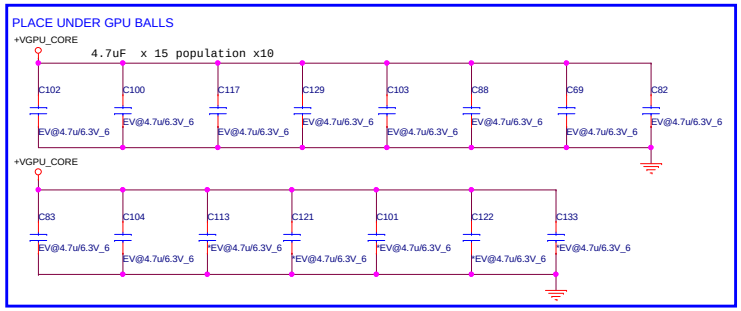
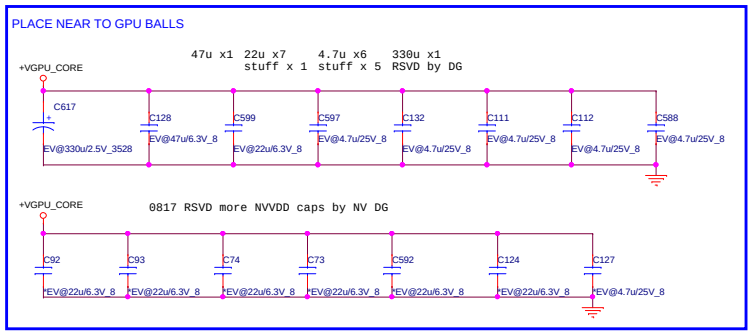


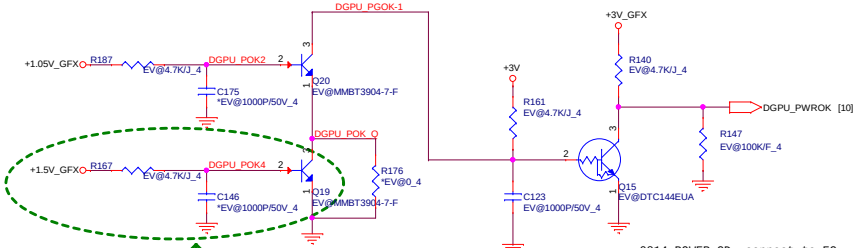




LAYOUT NOTES:
UNDAER: WITHIN 150MILS
NEAR: WITHIN 1378MILS

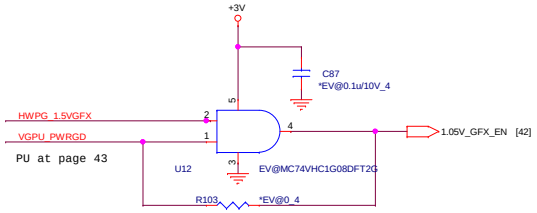




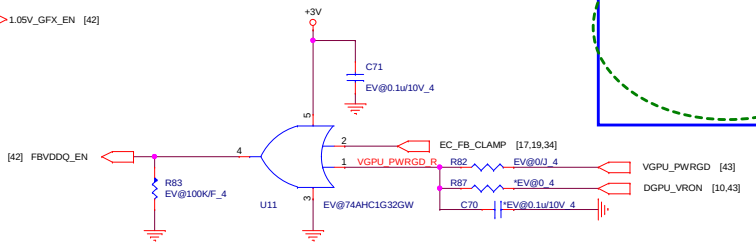


for meet Power down sequence
for +3V_GFX

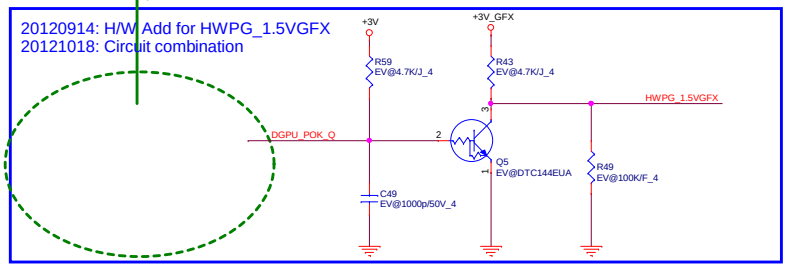
20120911: D6002 no stuff when GC6 support.



0816 GC6 need system 3V to control FBVDDQ



20120914: H/W Add for HWPG_1.5VGFX
20121018: Circuit combination



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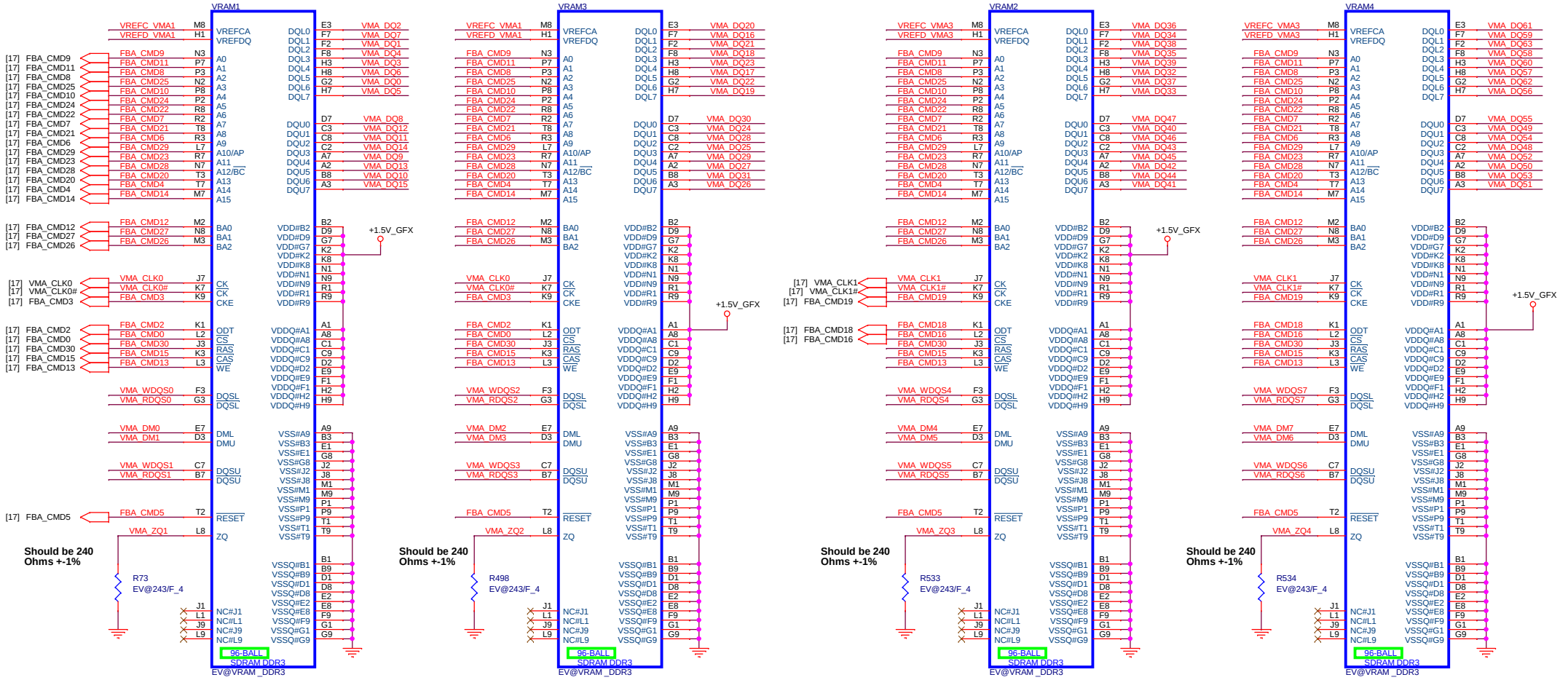
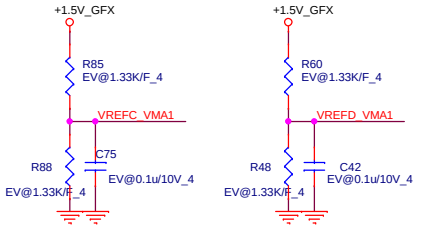
CHANNEL A: 1024MB DDR3

[17] VMA_DQ[63..0]
[17] VMA_DM[7..0]
[17] VMA_WDQS[7..0]
[17] VMA_RDQS[7..0]



Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

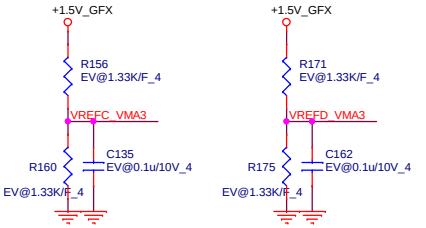
VMA_CLK0 — R489 EV@162/F_4 — VMA_CLK0#

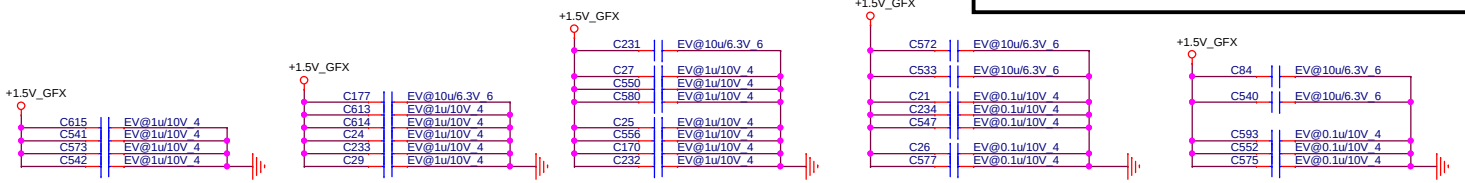


[17] FBA_CMD17 — FBA_CMD17 — TP11
[17] FBA_CMD1 — FBA_CMD1 — TP6
10/14 modify

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

VMA_CLK1 — R542 EV@162/F_4 — VMA_CLK1#





Quanta Computer Inc.
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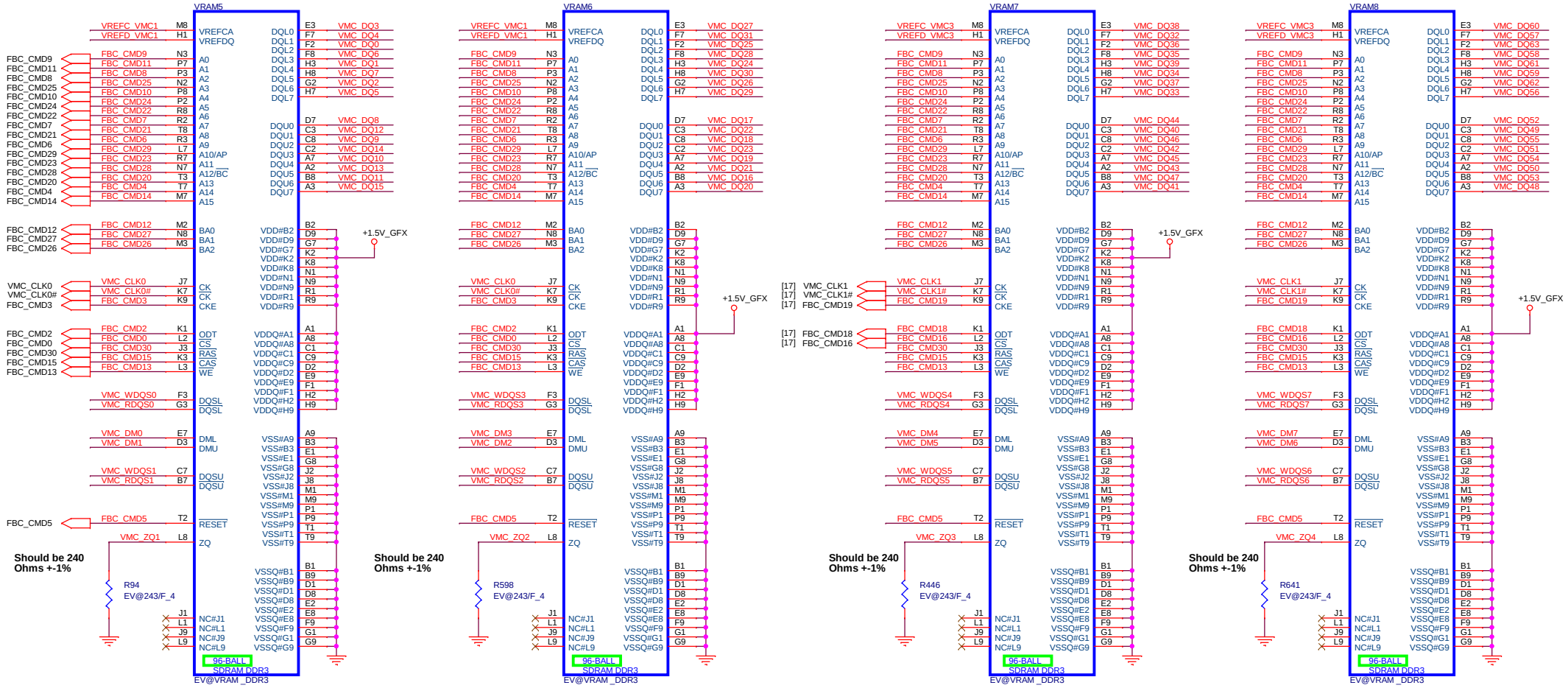
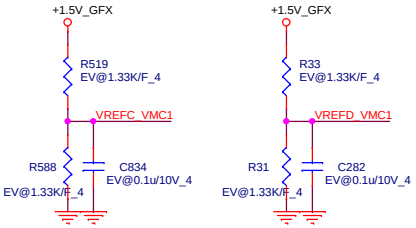
HYNIX 900MHz 1G AKD5LZWTW02
HYNIX 900MHz 2G AKD5MGWTW16

[17] VMC_DQ[63..0]
[17] VMC_DM[7..0]
[17] VMC_WDQS[7..0]
[17] VMC_RDQS[7..0]

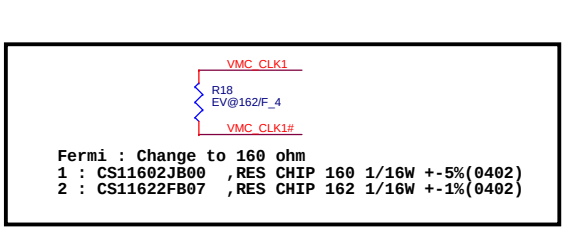
CHANNEL B: 1024MB DDR3

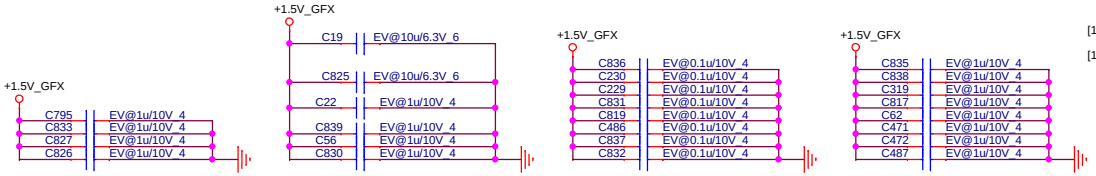


Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

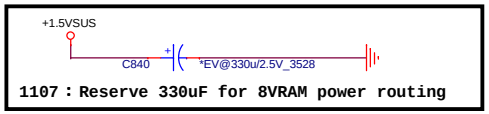


Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)





[17] FBC_CMD17 — FBC_CMD17 — TP113
[17] FBC_CMD1 — FBC_CMD1 — TP110



1107 : Reserve 330uF for 8VRAM power routing

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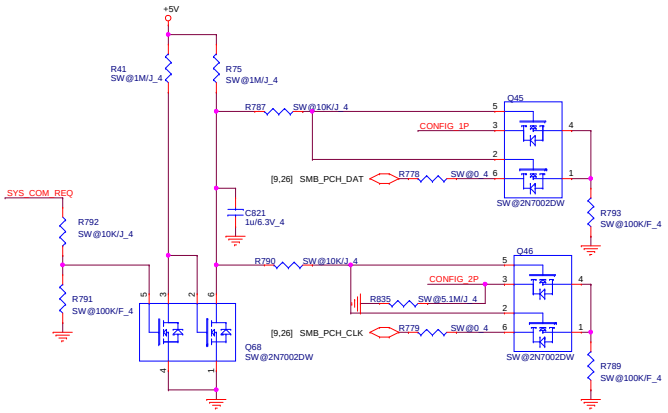
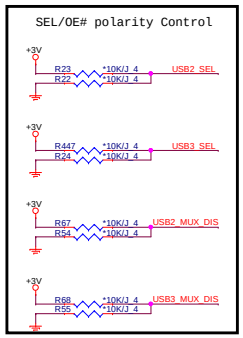
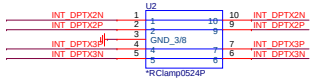
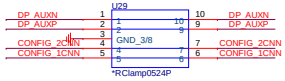
mini DP ML (DPP)

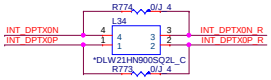


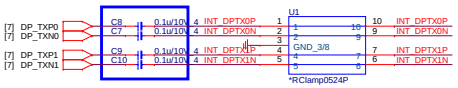


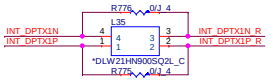
ESD Protect (EMC)







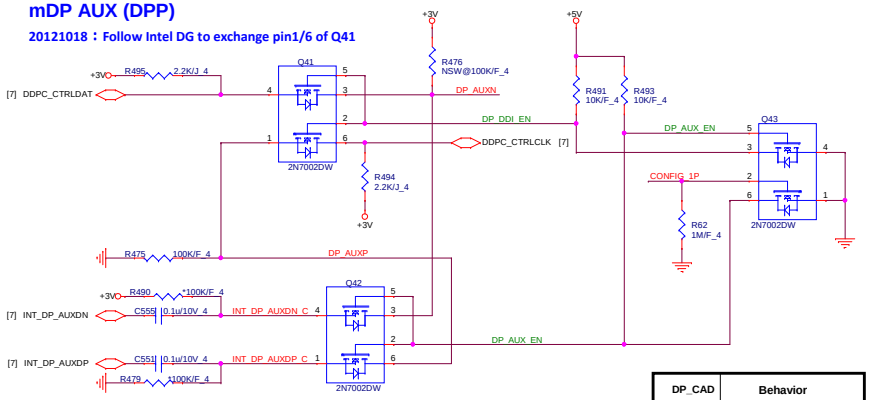




Layout Notes:
Place decoupling CAPs close to Connector **Close to DP connector**

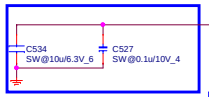
mDP AUX (DPP)

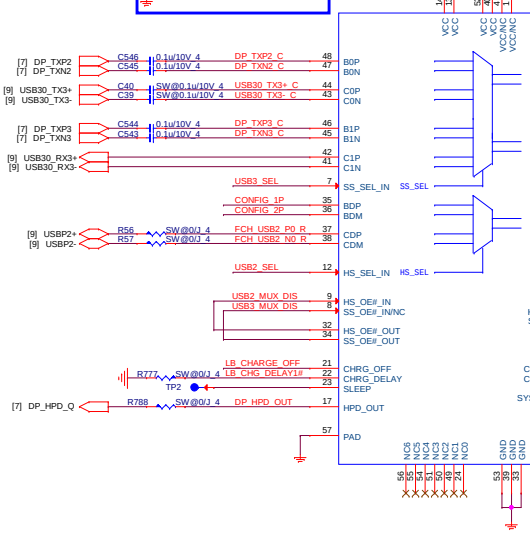
20121018：Follow Intel DG to exchange pin1/6 of Q41



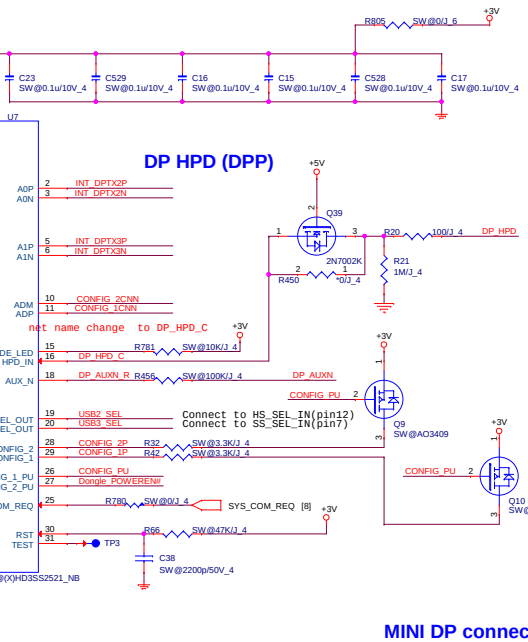
DP_CAD	Behavior
Low	DP signal (AC couple)
High	TMDS signal (DC couple)

Layout Notes:
Place near Pin13 and Pin14

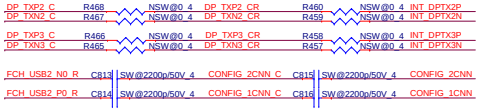


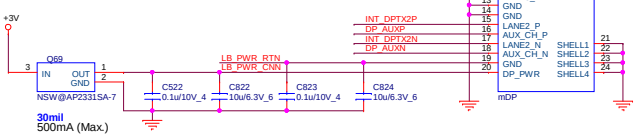


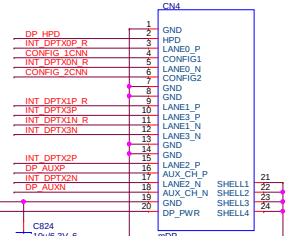
DP HPD (DPP)

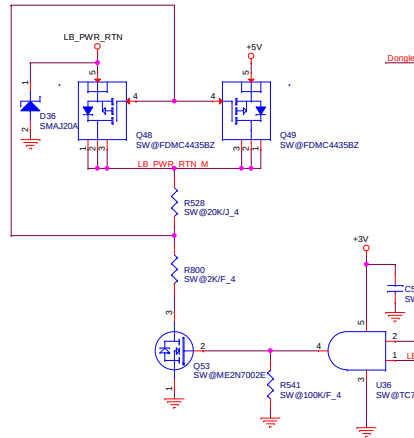


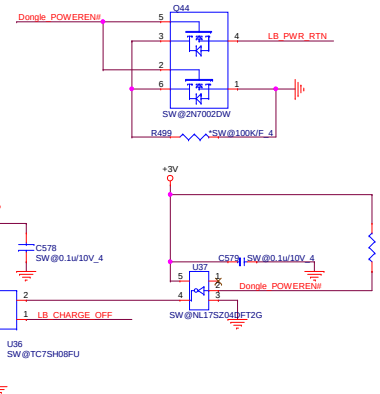
MINI DP connector (DPP)

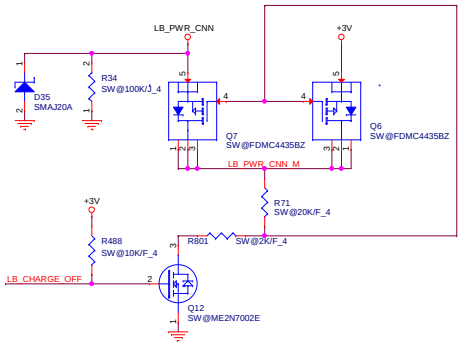












Quanta Computer Inc.			
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Size	Document Number: Mini DP		Rev: 1A
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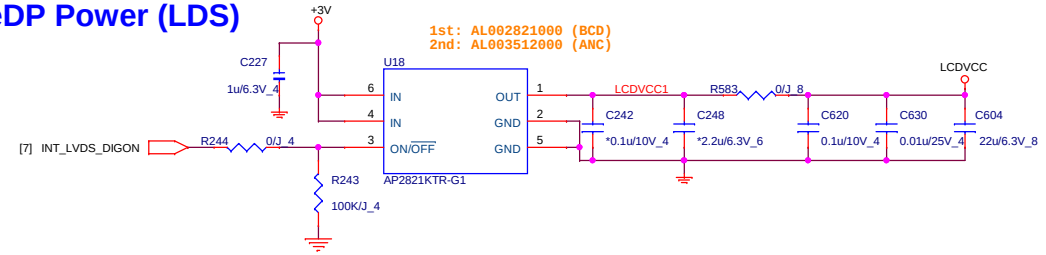
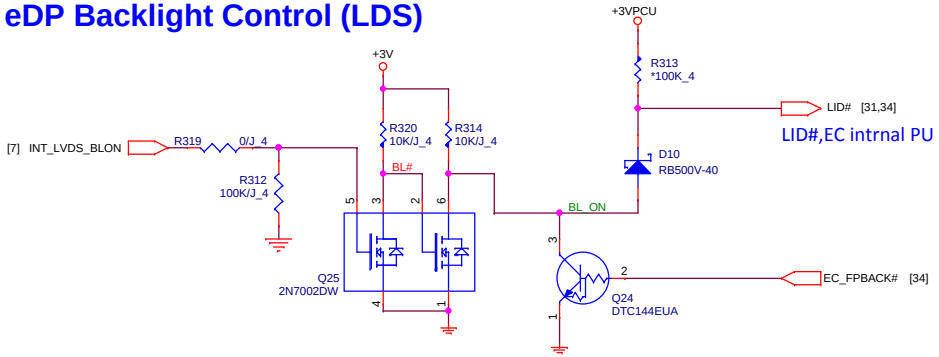
eDP Power (LDS)

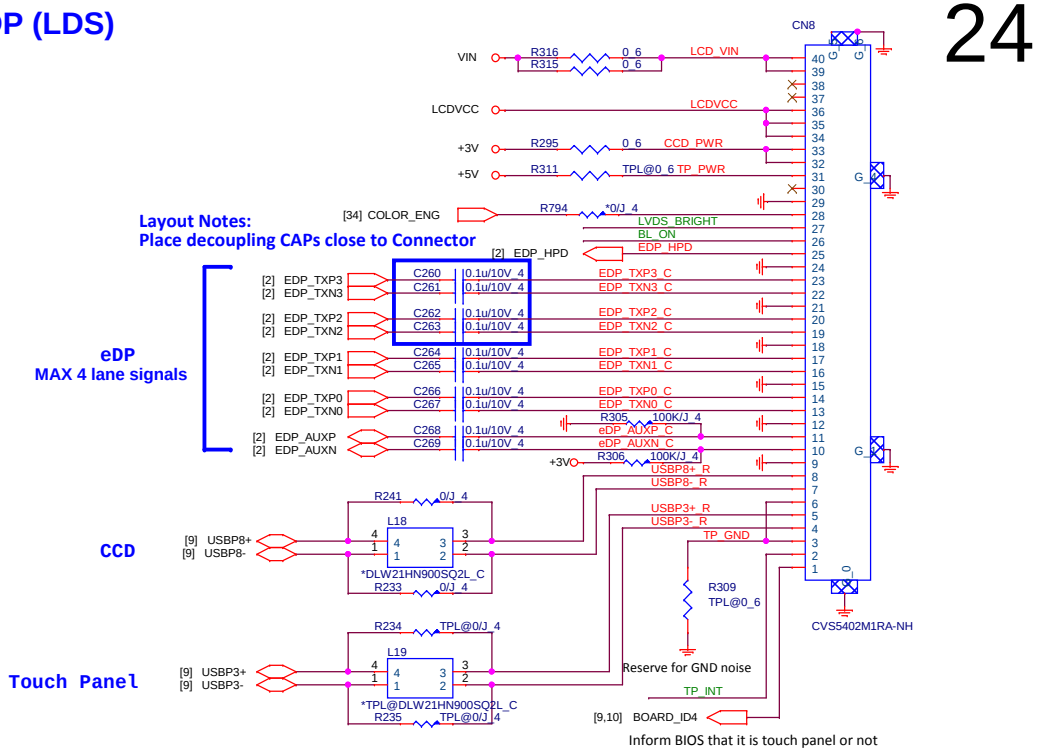


eDP Backlight Control (LDS)

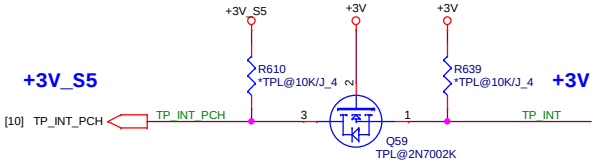


eDP Brightness Control (LDS)

eDP (LDS)



Touch Panel interrupt signal：
1016：Exchange Q59 pin 1 & 3 direction to prevent leakage



Quanta Computer Inc.
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Size	Document Number	Rev
	eDP/CAMERA/LID	1A
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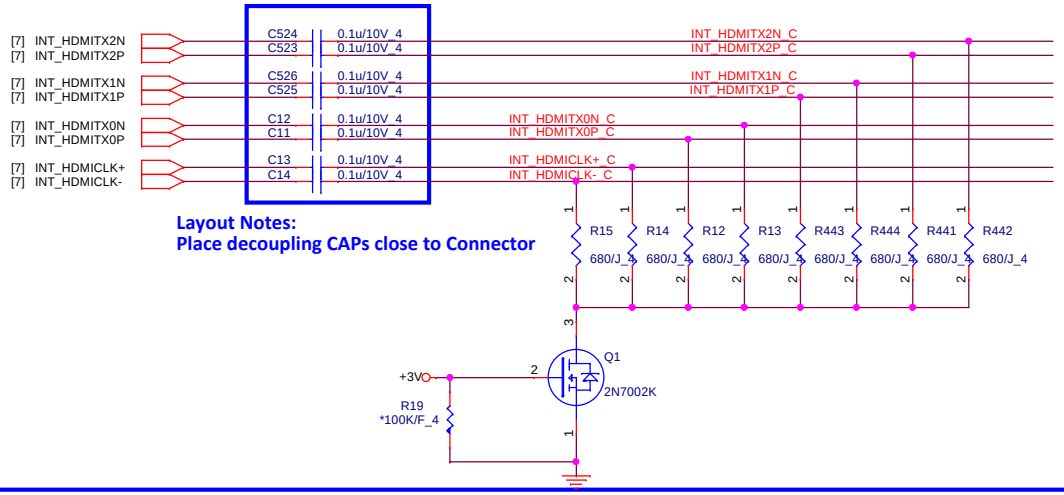
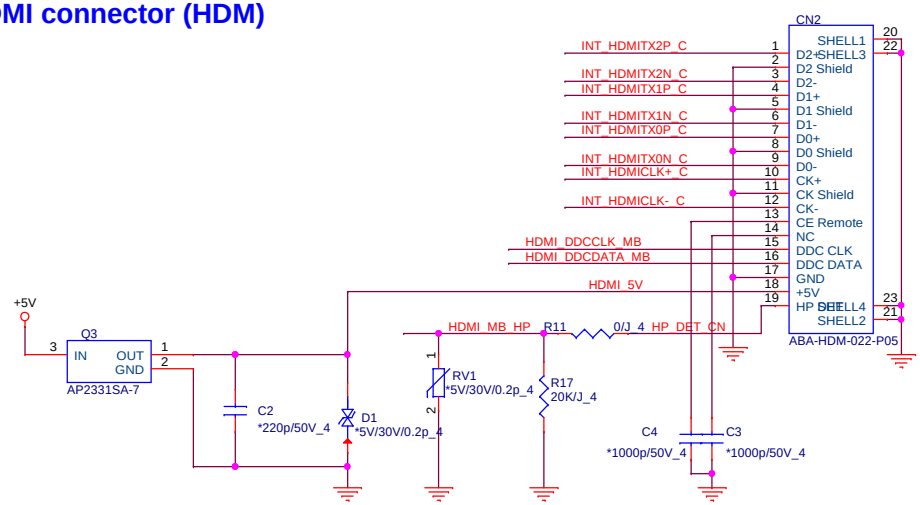
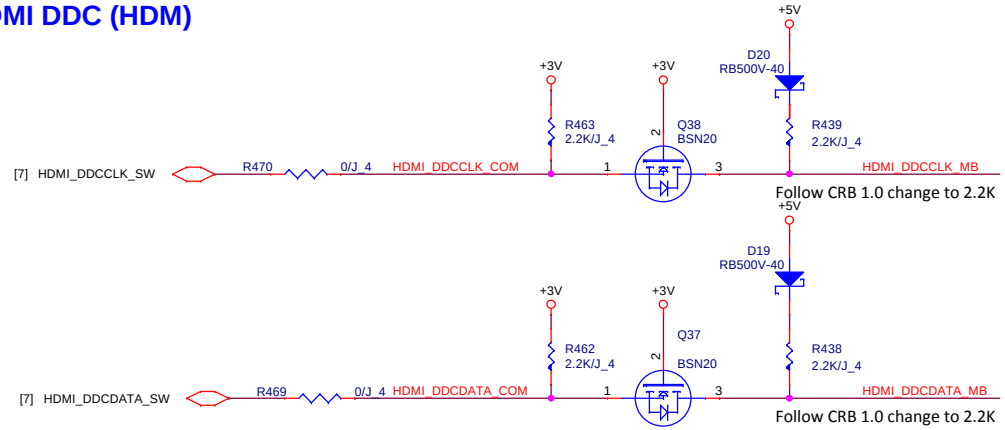
HDMI Cost Reduced level shift (HDM)



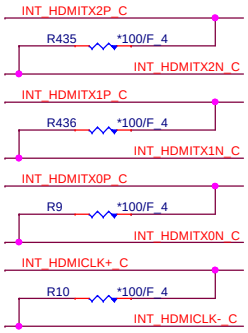
HDMI connector (HDM)



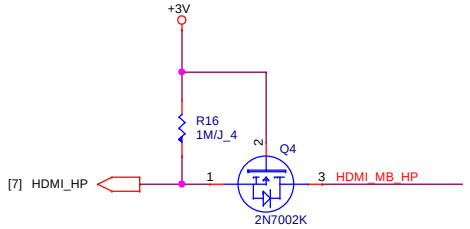
HDMI DDC (HDM)



EMI (EMC)



HDMI-detect (HDM)



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	HDMI	1A
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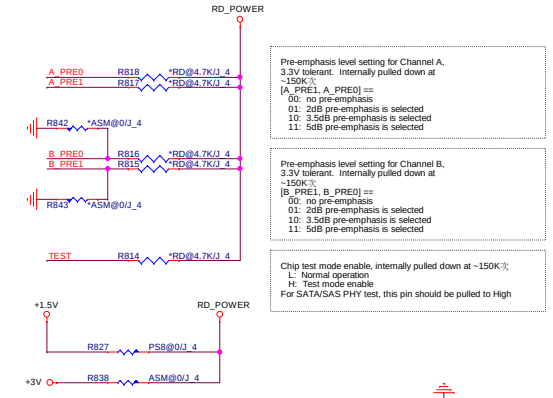
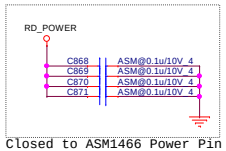
mSATA Redriver (HDD)



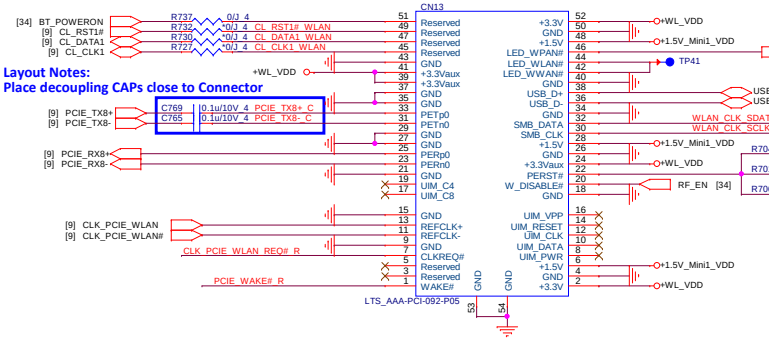


Closed to ASM1466 Power Pin

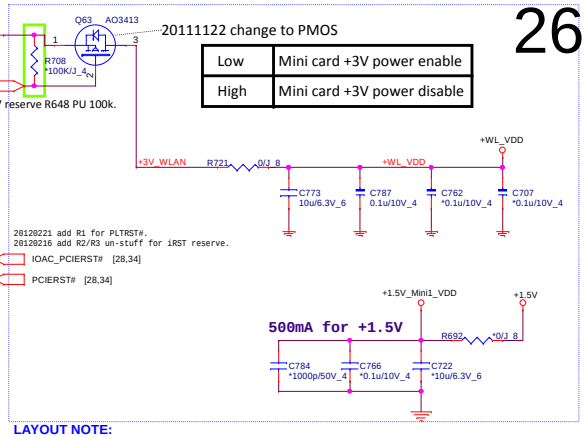
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Check LED signal. (active high or low)
H=5.2mm



Layout Notes:
Place decoupling CAPs close to Connector



LAYOUT NOTE:
CLOSE TO CONNECTOR

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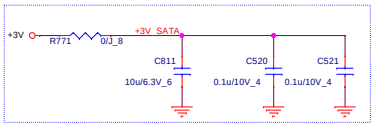
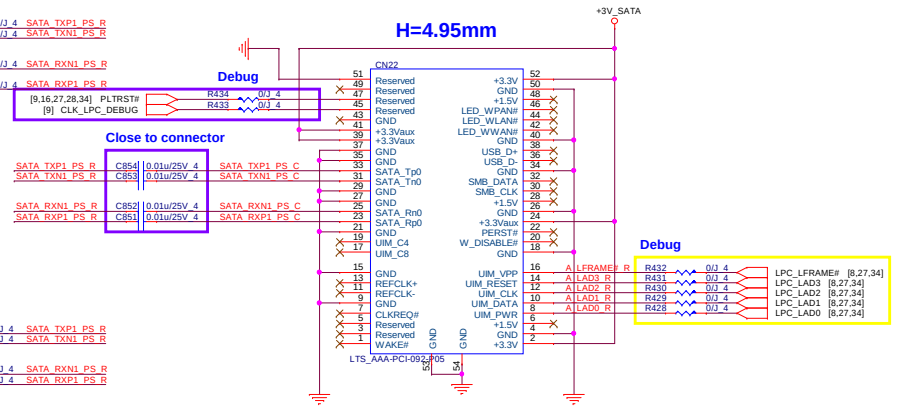
mSATA (HDD)



LAYOUT NOTE:
CLOSE TO CONNECTOR

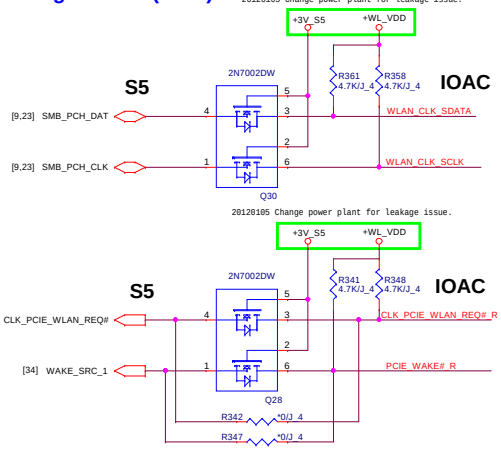
rating = 1000mA @ 128G

H=4.95mm



Leakage circuit (MPC)

20120105 Change power plant for leakage issue.



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	Mini Card/mSATA	1A
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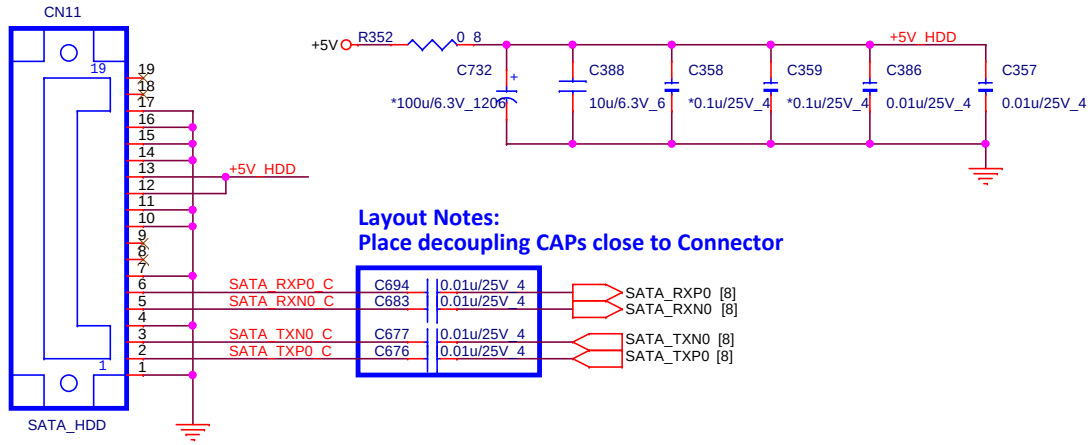
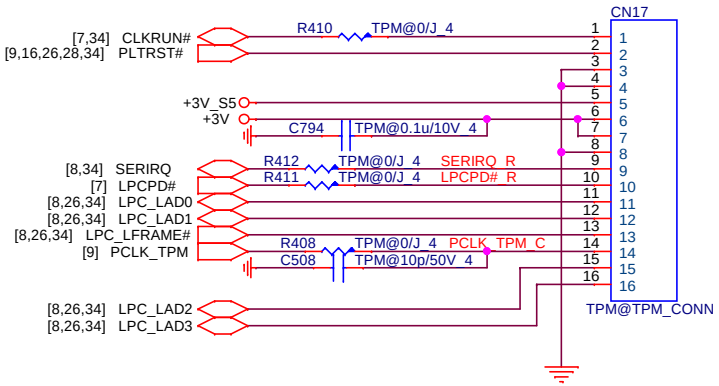
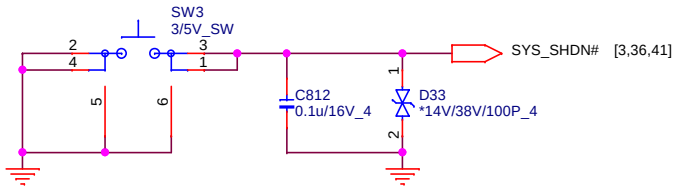
MAIN SATA HDD (HDD)



TPM (TPM)



3/5VPCU reset switch (CLG)



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Size	Document Number	Rev
	SATA-HDD/ TPM	1A
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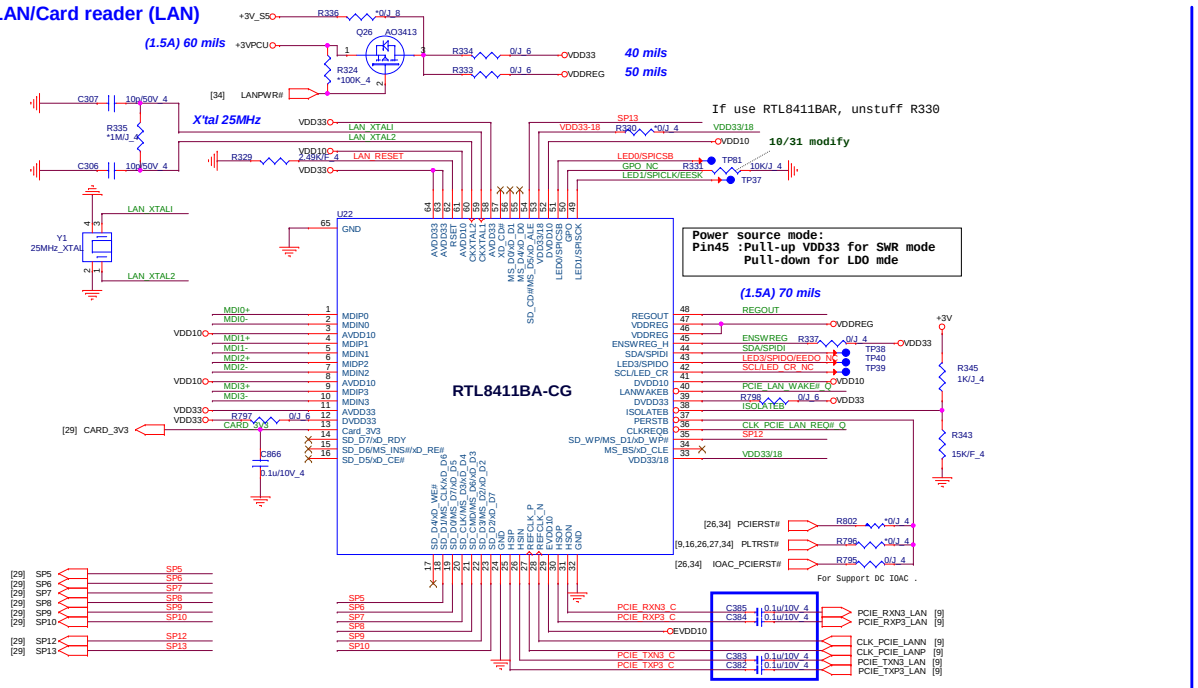
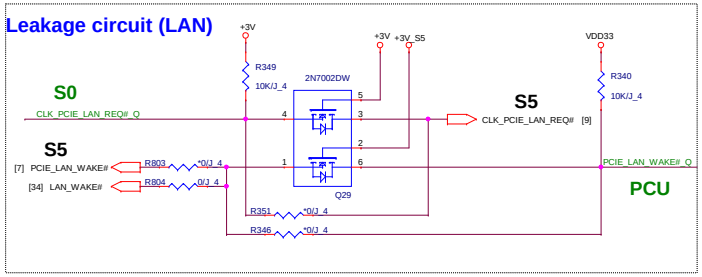
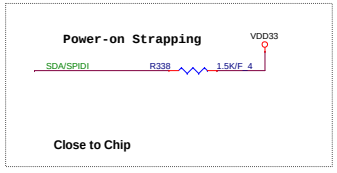
LAN/Card reader (LAN)

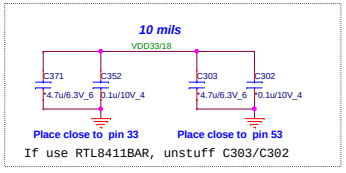


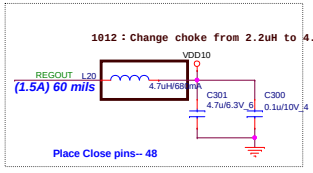
Leakage circuit (LAN)

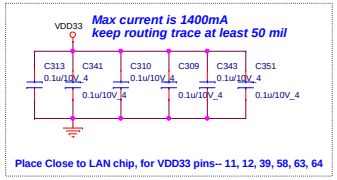


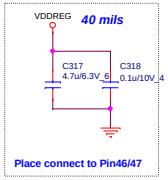
1012 : LAN request pin power domain need to sync with ISOLATEB pin
1016 : Exchange Q29 pin 3 & 4 to prevent leakage issue

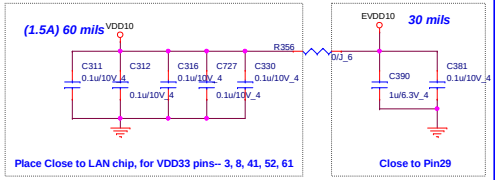




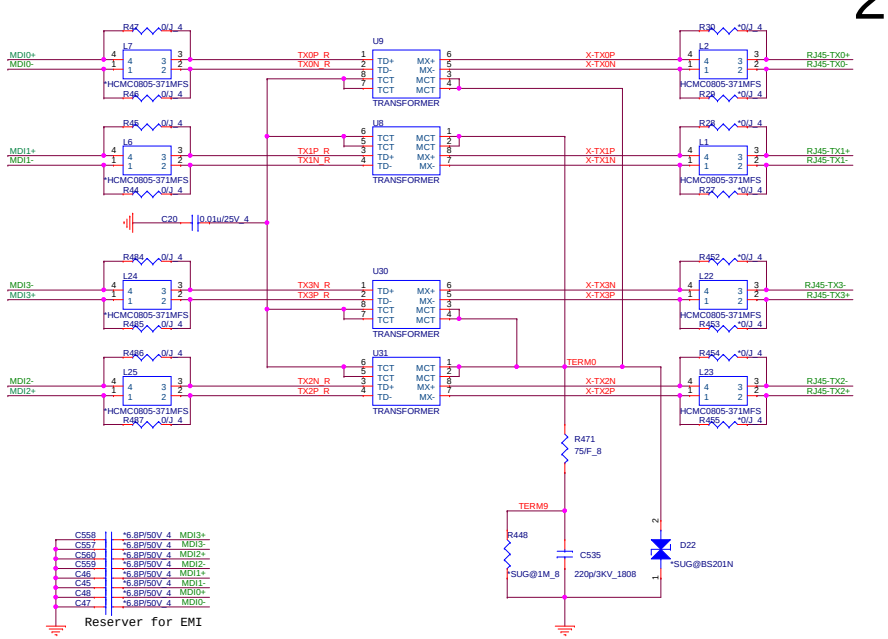




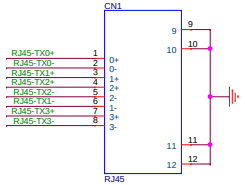




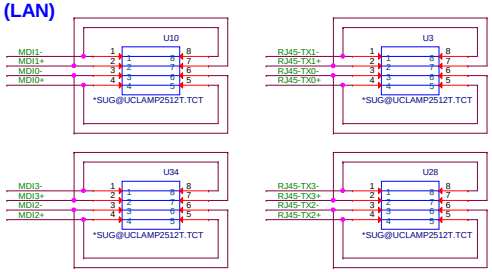
Transformer (LAN)



RJ45 CONNECTOR (LAN)



SURGE (LAN)



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	LAN-RTL8411/CARD READER	1A
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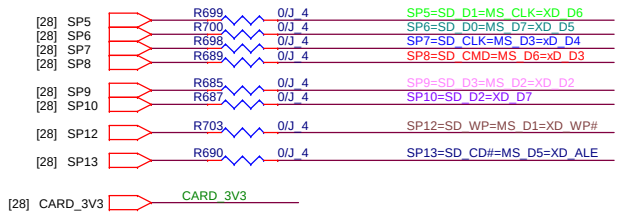
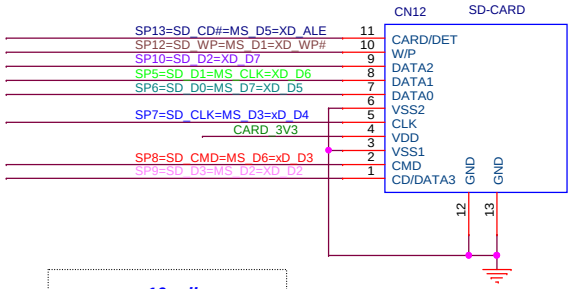
CARD READER CONNECTOR (MMC)

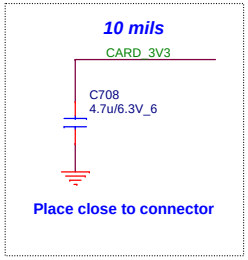
SD/MMC CARD READER (MMC)

Share Pin

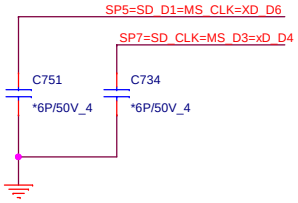
SP1	SD_D7		xD_RDY
SP2	SD_D6	MS_INS#	xD_RE#
SP3	SD_D5		xD_CE#
SP4	SD_D4		xD_WE#
SP5	SD_D1	MS_CLK	xD_D6
SP6	SD_D0	MS_D7	xD_D5
SP7	SD_CLK	MS_D3	xD_D4
SP8	SD_CMD	MS_D6	xD_D3
SP9	SD_D3	MS_D2	xD_D2
SP10	SD_D2		xD_D7
SP11		MS_BS	xD_CLE
SP12	SD_WP	MS_D1	xD_WP#
SP13	SD_CD#	MS_D5	xD_ALE
SP14		MS_D4	xD_D0
SP15		MS_D0	xD_D1
SP16			xD_CD#







EMI



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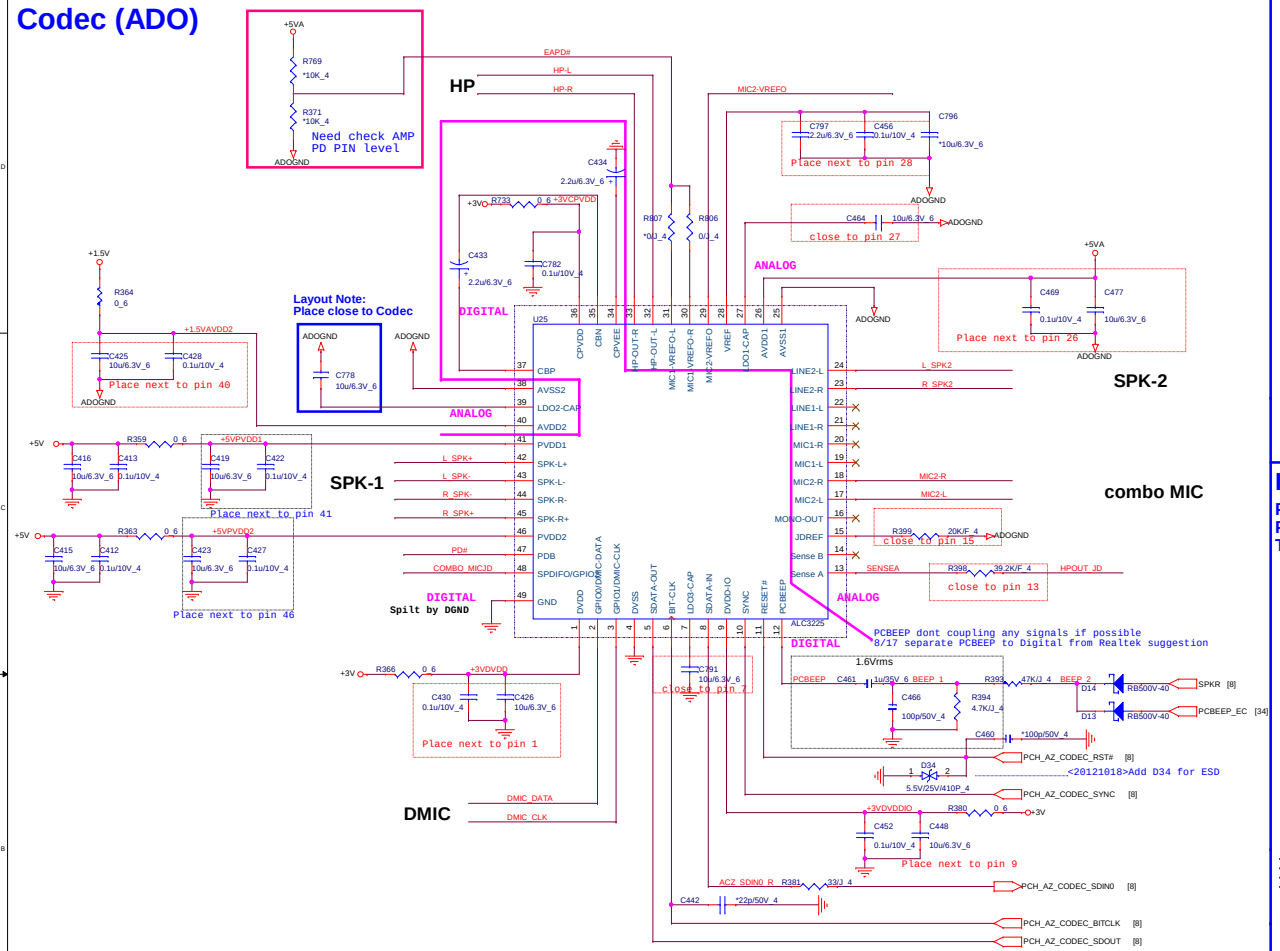
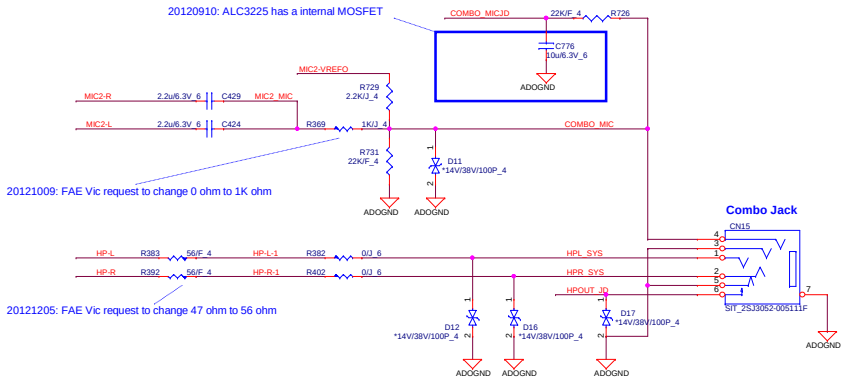
Codec (ADO)



HEADPHONE/Mic combo (AMP)

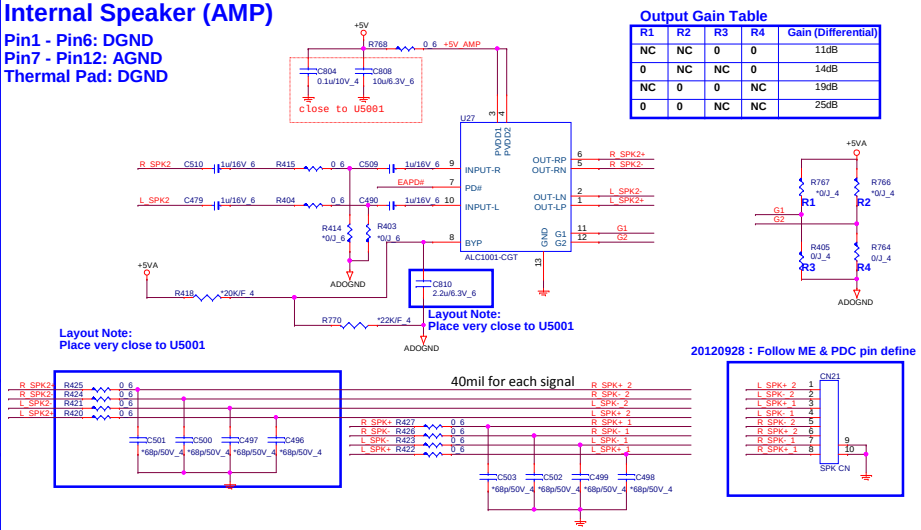


Internal Speaker (AMP)

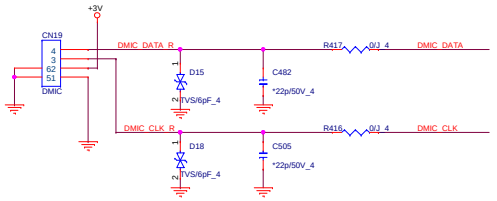
Pin1 - Pin6: DGND
Pin7 - Pin12: AGND
Thermal Pad: DGND

Output Gain Table

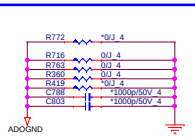
R1	R2	R3	R4	Gain (Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB



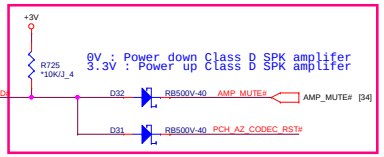
INT DMIC (AMP)



Power(ADO)



Mute(ADO)



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	REALTEK ALC3225	1A

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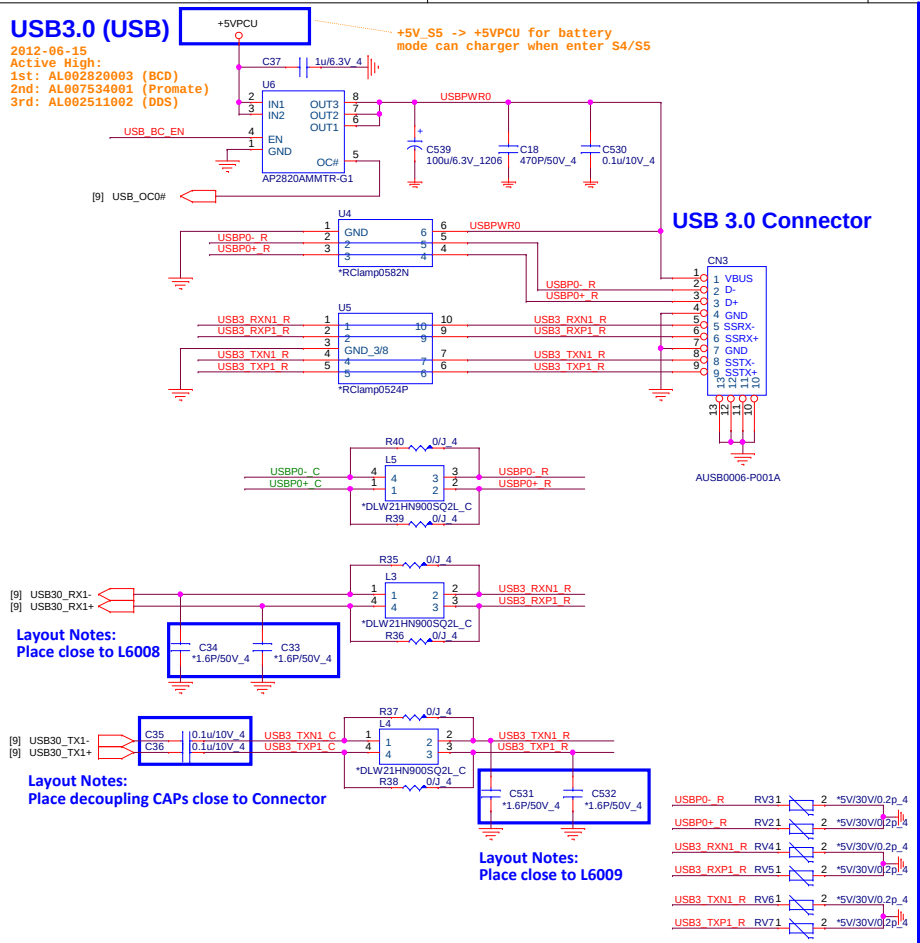
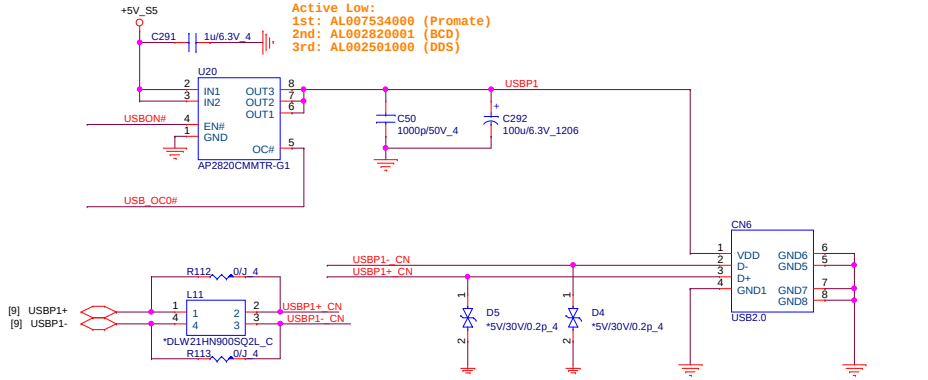
USB3.0 (USB)

2012-06-15
Active High:
1st: AL002820003 (BCD)
2nd: AL007534001 (Promate)
3rd: AL002511002 (DDS)



USB2.0 (USB)

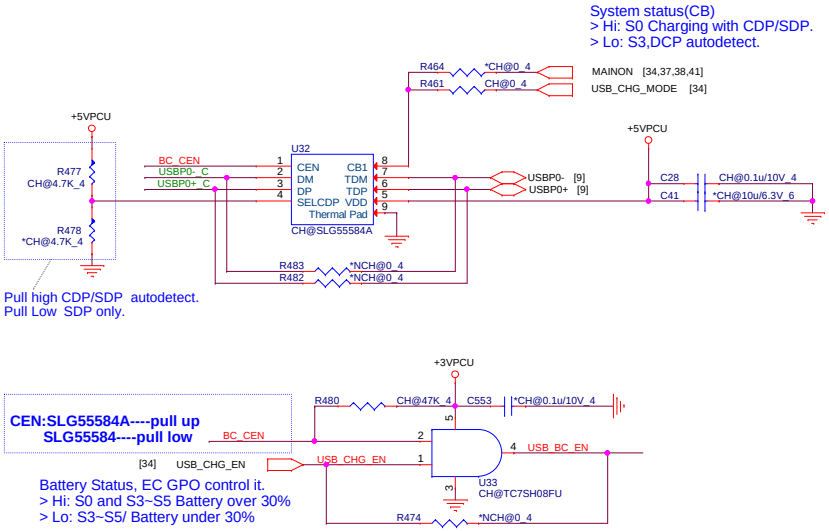


USB Charger to 3.0 (USB)

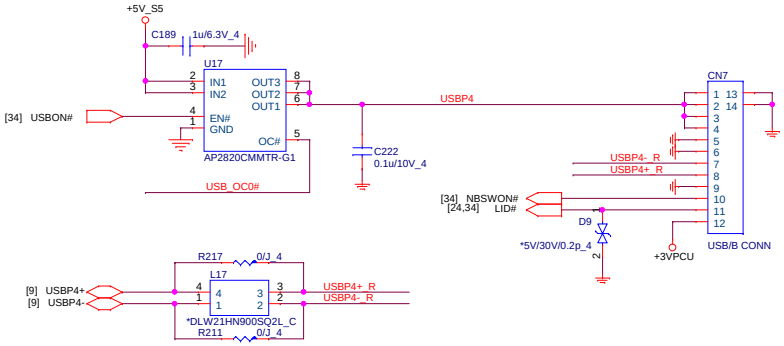
Name	USB data	State	Max Current	Apple Device
SDP	YES	S0~S3	500mA	500mA
CDP	YES	S0~S3	1500mA	500mA
DCP,Auto	NO	S4~S5	1800mA	1800mA

CB	SELCDP	FuncionFuncion
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)

CH@: Default stuff



I/O board (USB)

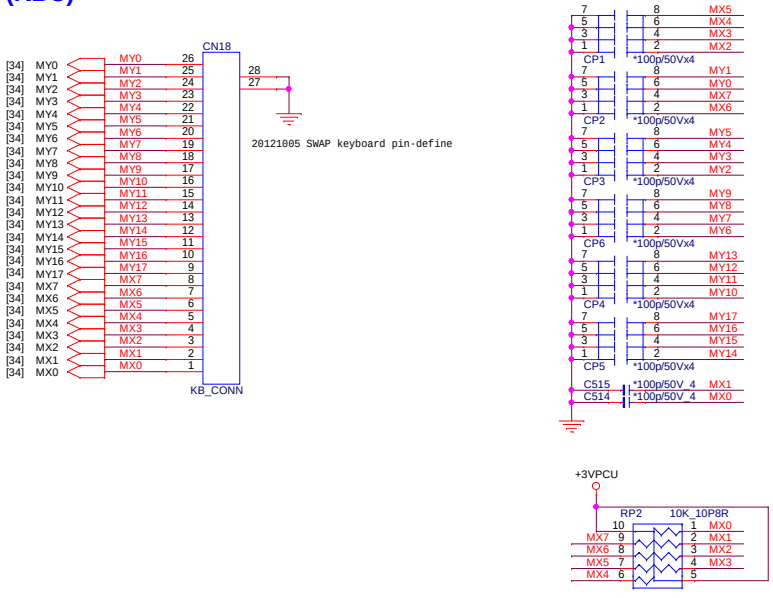


Quanta Computer Inc.
PROJECT : ZQK

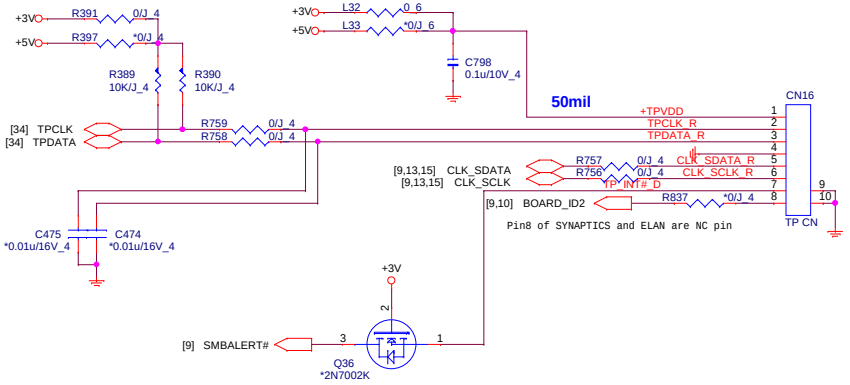
Size	Document Number	Rev
	INT&EXT USB	1A

Date: Monday, January 07, 2013 Sheet 31 of 46

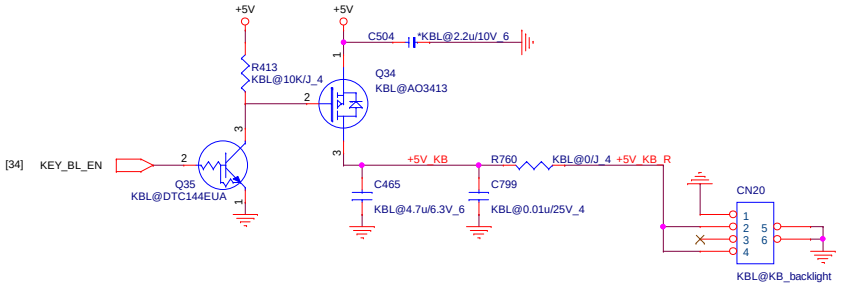
K/B (KBC)



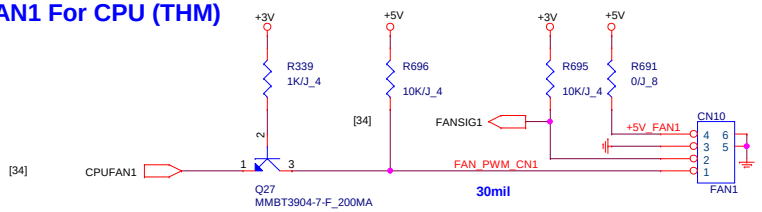
TOUCHPAD BOARD CONN (TPD)



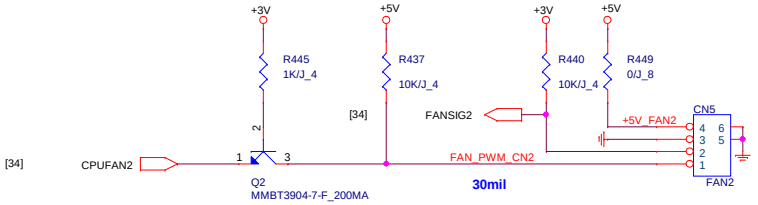
KB_BL LED (KBC)



FAN1 For CPU (THM)



FAN2 For GPU (THM)



Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	KB/TP/FAN	1A

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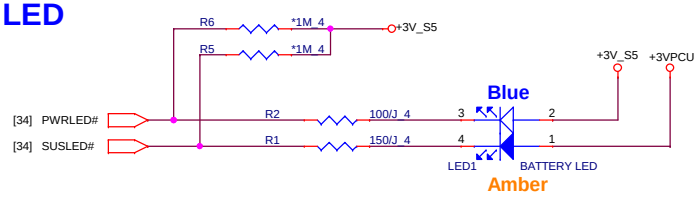
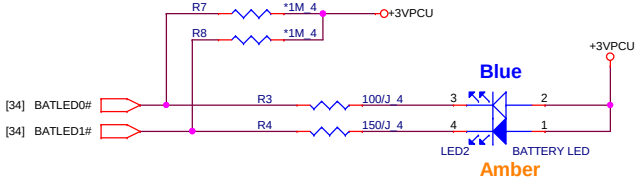
LED(UIF)

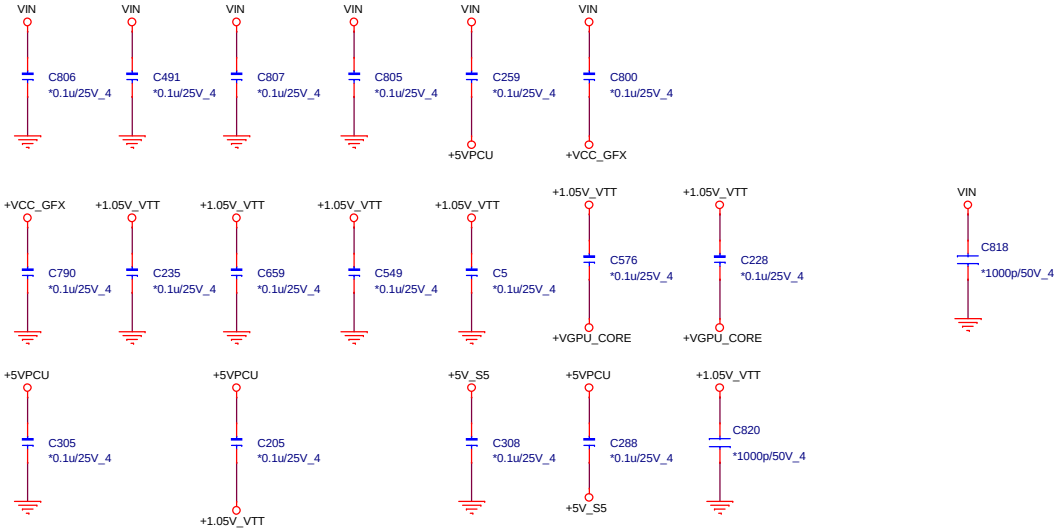
Power LED



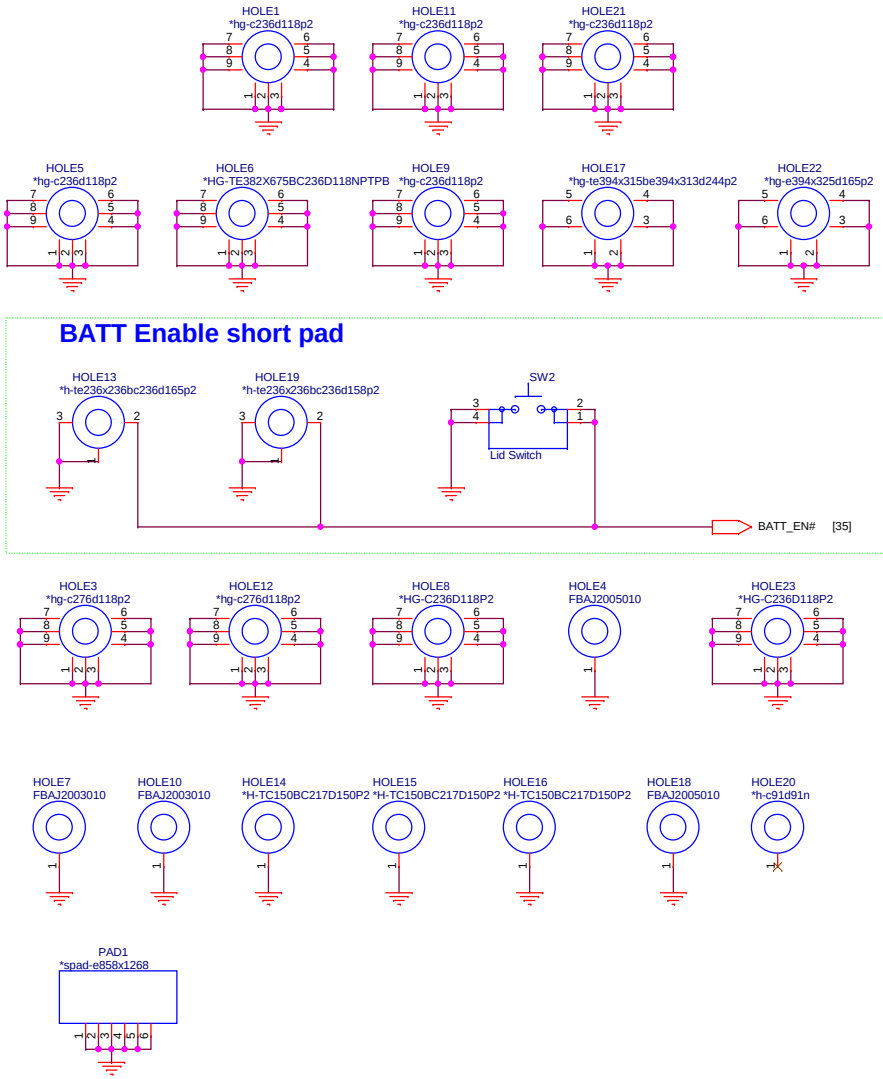
Battery



Stitching cap (EMC)



HOLE(OTH)



Quanta Computer Inc.		
PROJECT : ZQK		
Size	Document Number	Rev
	LED/ Hole	1A
Date: Monday, January 07, 2013	Sheet 33 of 46	

EC(KBC)

+3VPCU_EC and +3V_RTC minimum trace width 12mils.

1008 : Change Power rail from +3VPCU to +3VPCU_EC (For PLL Power)

12 mils

12 mils

Please do not place any pull-up resistor on GPG0, GPG2, and GPG6 (Reserved hardware strapping).

Layout Notes: Place Series Resistors close to ITE8587

IT8587

IT8587E/EX

LPC

GPIO

SM BUS

PS/2

CIR

PWM

UART port

WAKE UP

EXTERNAL SERIAL FLASH

Input only

A/D D/A

SPI ENABLE

KBMX

CLOCK

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH/VGA

SM BUS PU(KBC)

HWPG(KBC)

For test only

SW1 — Power Switch

iRST

20120217 reserve iRST function.

U13 *TC7SH08FU

Quanta Computer Inc.	
PROJECT : ZQK	
Size	Document Number: KBC IT8587 — Rev: 1A
Date: Monday, January 07, 2013	Sheet 34 of 46

recommend 200mA at least.
PU9 BQ24737RGRR
ACDET
VCC
ACOK#
SDA
SCL
BM#
CMPOUT
ILIM
CMPIN
IOUT
REGN
BTST
HIDRV
PHASE
LCDRV
PGND
SRP
SRN
ACP
ACN
24737_REGN
24737_BST
24737_DH
24737_LX
24737_DL
24737_SRP
24737_SRN
24737_ACDET
24737_VCC
24737_BM#
24737_CMPOUT
24737_ILIM
24737_CMPIN
MBDATA
MBCLK
For battery reverse
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit
Pin10 ILIM=0.793V
Rsr = 0.01ohm
Limit set on 60W/3.16A
Add ESD diode base on EC FAE suggestion
Quanta Computer Inc.
PROJECT : ZQK
Charger(BQ24737RGRR)
Monday, January 07, 2013
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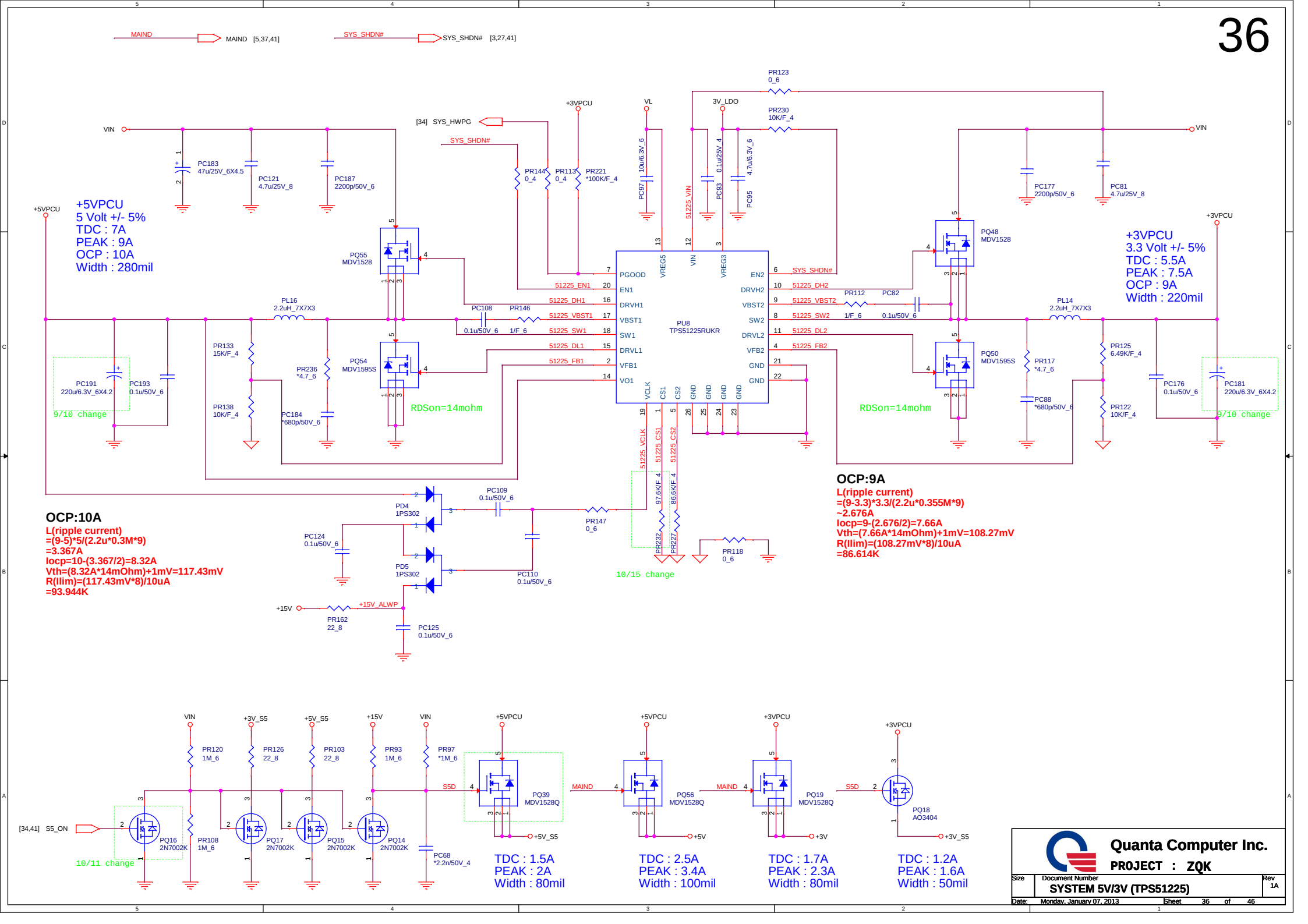
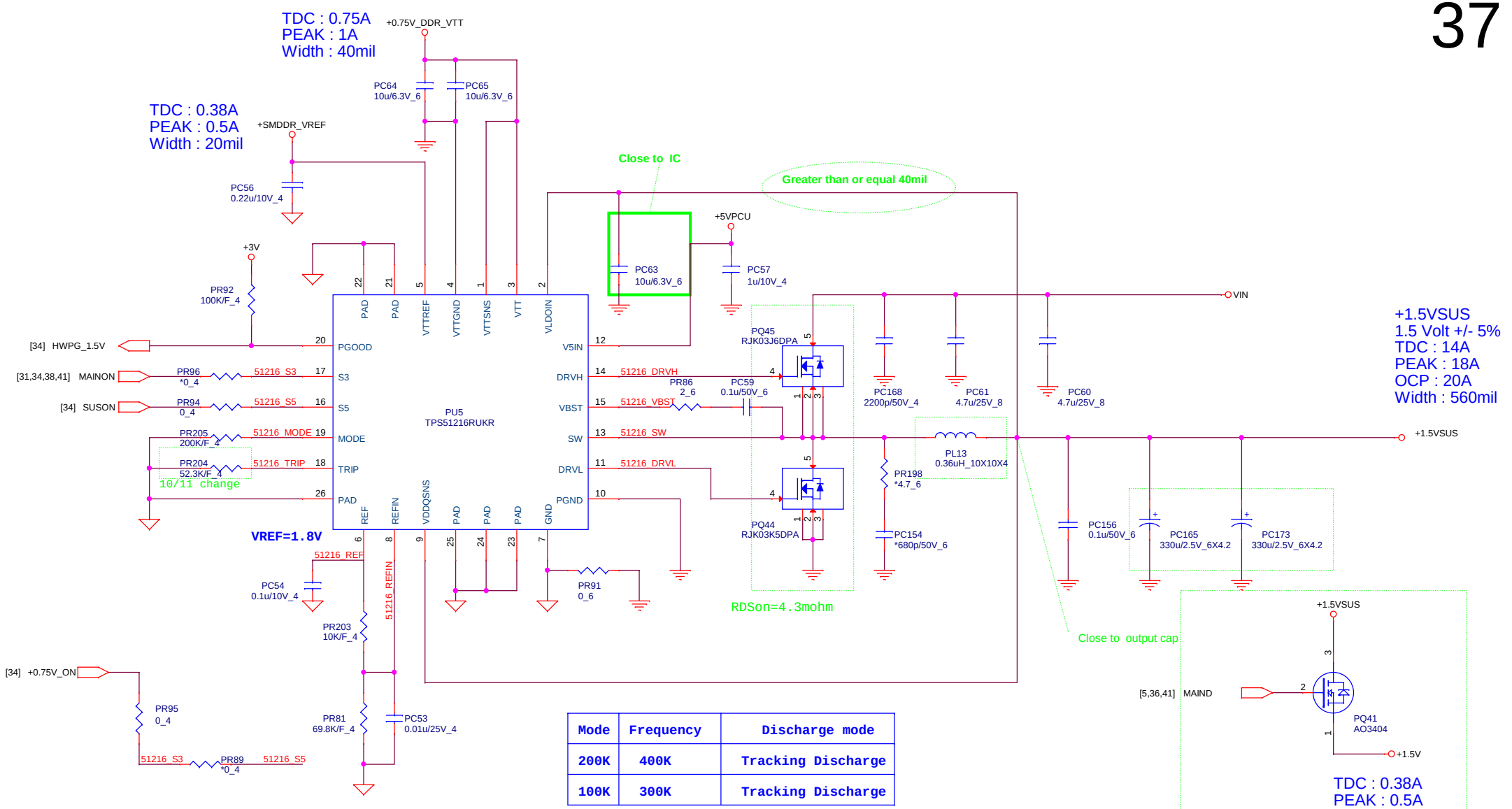


Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	SYSTEM 5V/3V (TPS51225)	1A
Date: Monday, January 07, 2013	Sheet 36 of 46	



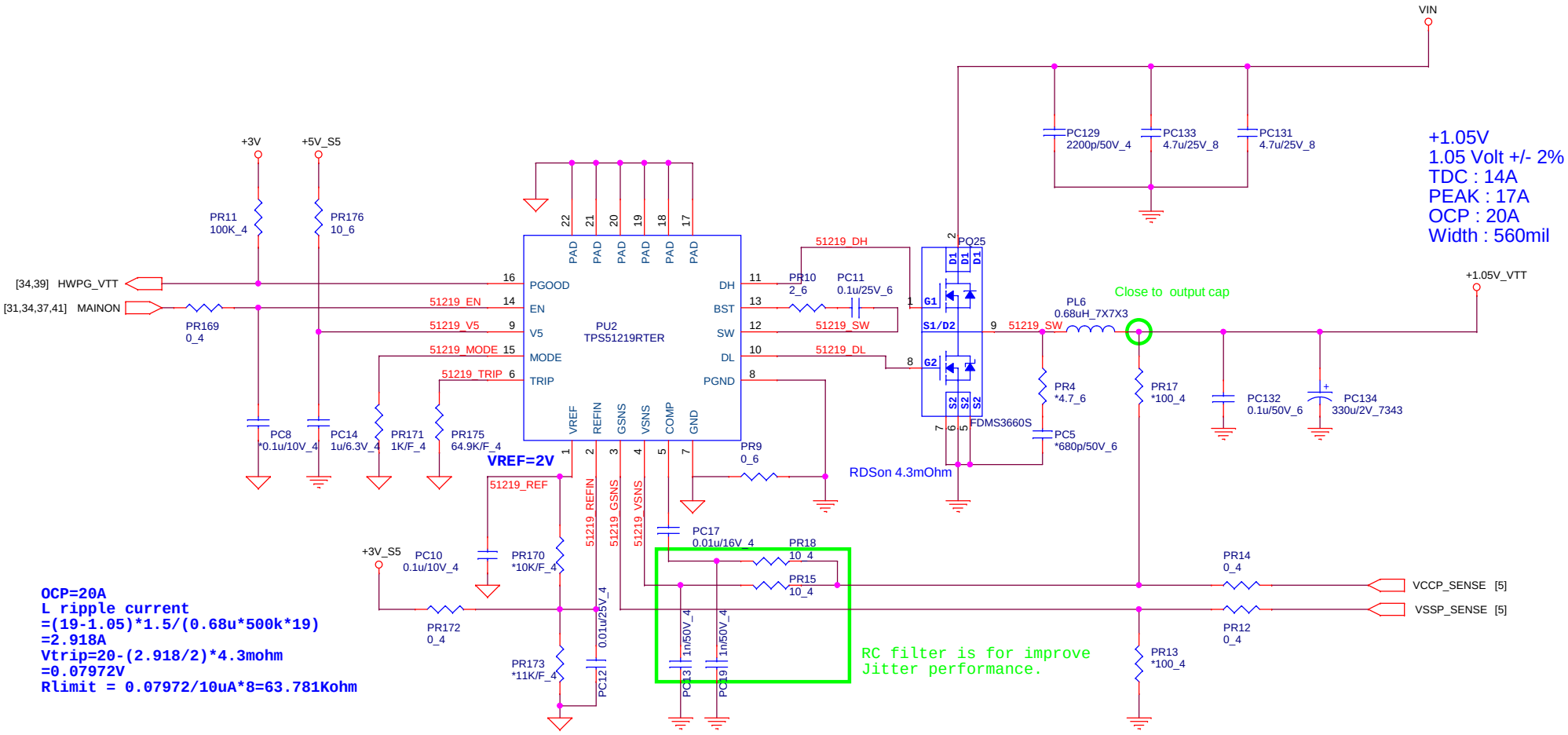
Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

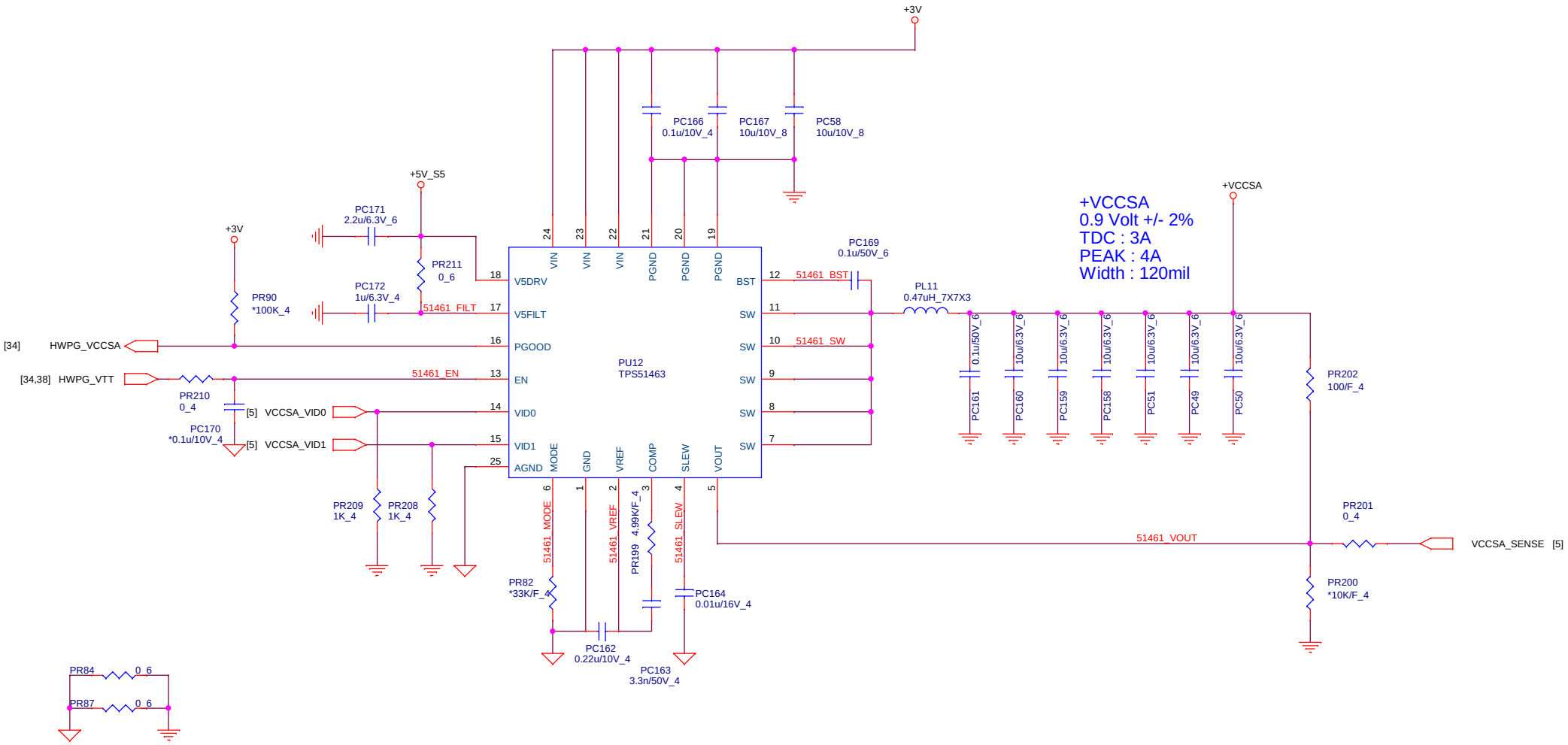
OCP=20A
L ripple current
=(19-1.5)*1.5/(0.36u*400k*19)
=9.594A
Vtrip=20-(9.594/2)*4.3mohm
=0.065372V
Rlimit=0.065372/10uA*8=52.297Kohm

Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	DDR 1.5V(TPS51216)	1A
Date: Monday, January 07, 2013	Sheet 37 of 46	



Quanta Computer Inc.		
PROJECT : ZQK		
Size	Document Number: +1.05V (TPS51219)	Rev: 1A
Date: Monday, January 07, 2013	Sheet 38 of 46	



VID0	VID1	+VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

default 0.9V

Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	VCCSA(TPS51463)	1A

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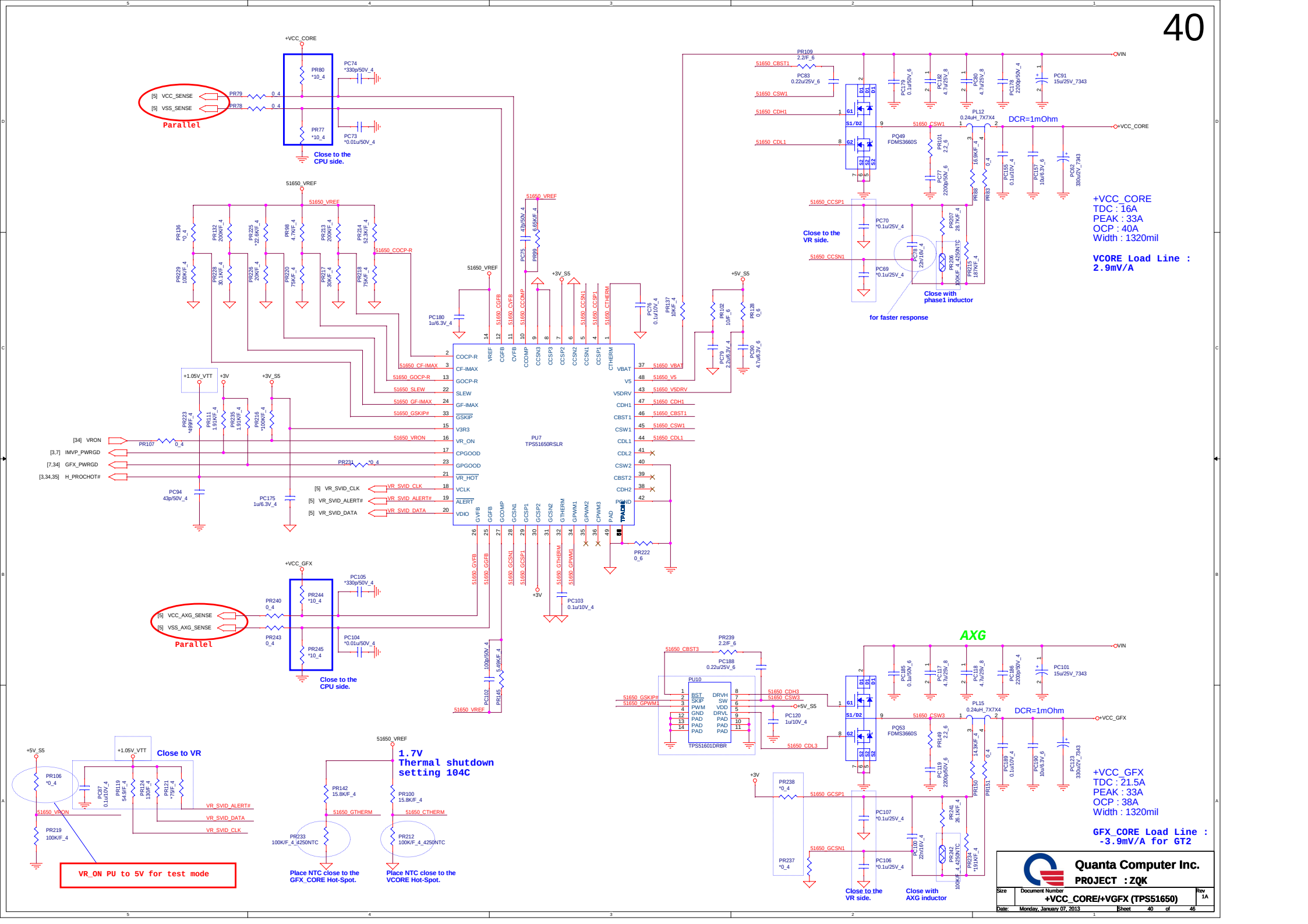
+VCC_CORE
[5] VCC_SENSE
[5] VSS_SENSE
Parallel
Close to the CPU side.
51650_VREF
PU7 TPS51650RSLR
+1.05V_VTT
+3V
+3V_S5
+5V_S5
[34] VRON
[3,7] IMVP_PWRGD
[7,34] GFX_PWRGD
[3,34,35] H_PROCHOT#
[5] VR_SVID_CLK
[5] VR_SVID_ALERT#
[5] VR_SVID_DATA
51650_COCP-R
51650_CF-IMAX
51650_GOCP-R
51650_SLEW
51650_GF-IMAX
51650_GSKIP#
51650_VRON
51650_VBAT
51650_V5
51650_V5DRV
51650_CDH1
51650_CBST1
51650_CSW1
51650_CDL1
51650_CSCOMP
51650_CSCSN1
51650_CSCSP1
51650_CTHERM
51650_CVFB
51650_CGFB
51650_GVFB
51650_GGFB
51650_GCOMP
51650_GCSN1
51650_GCSP1
51650_GTHERM
51650_GPWM1
51650_GPWM2
51650_GCPWM3
VR_SVID_CLK
VR_SVID_ALERT#
VR_SVID_DATA
+VCC_GFX
[5] VCC_AXG_SENSE
[5] VSS_AXG_SENSE
Close to the CPU side.
51650_CBST3
51650_CDH3
51650_CSW3
51650_CDL3
51650_GSKIP#
51650_GPWM1
PU10 TPS51601DRBR
Close to VR
VR_ON PU to 5V for test mode
1.7V Thermal shutdown setting 104C
Place NTC close to the GFX_CORE Hot-Spot.
Place NTC close to the VCORE Hot-Spot.
VIN
DCR=1mOhm
PQ49 FDMS3660S
PQ53 FDMS3660S
Close to the VR side.
Close with phase1 inductor
for faster response
Close with AXG inductor
AXG
+VCC_CORE
TDC : 16A
PEAK : 33A
OCP : 40A
Width : 1320mil
VCORE Load Line : 2.9mV/A
+VCC_GFX
TDC : 21.5A
PEAK : 33A
OCP : 38A
Width : 1320mil
GFX_CORE Load Line : -3.9mV/A for GT2
Quanta Computer Inc.
PROJECT : ZQK
+VCC_CORE/+VGFX (TPS51650)
Rev 1A
Monday, January 07, 2013
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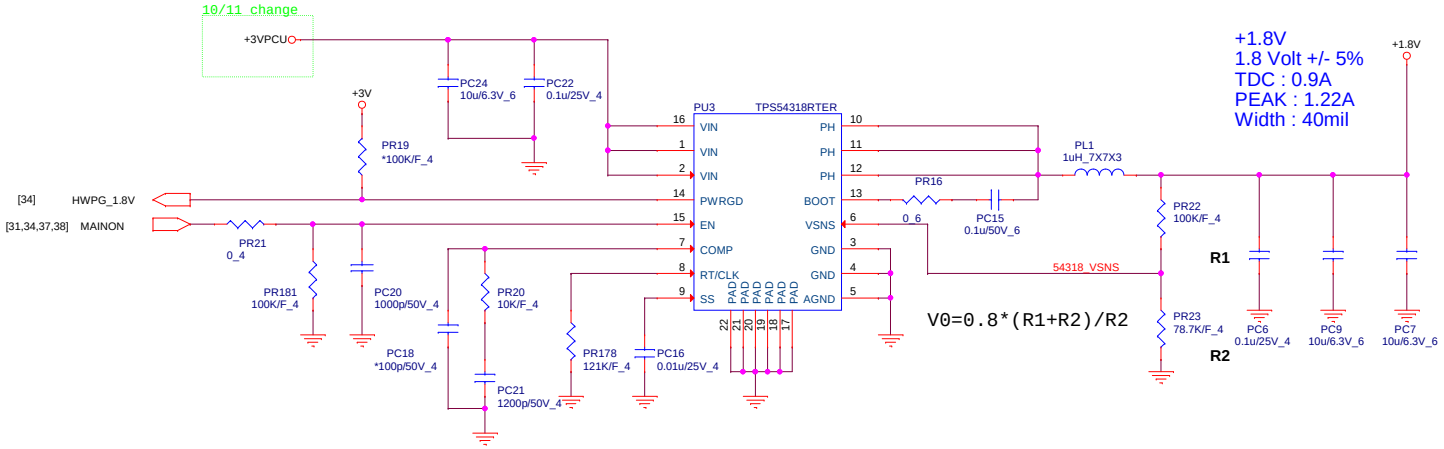
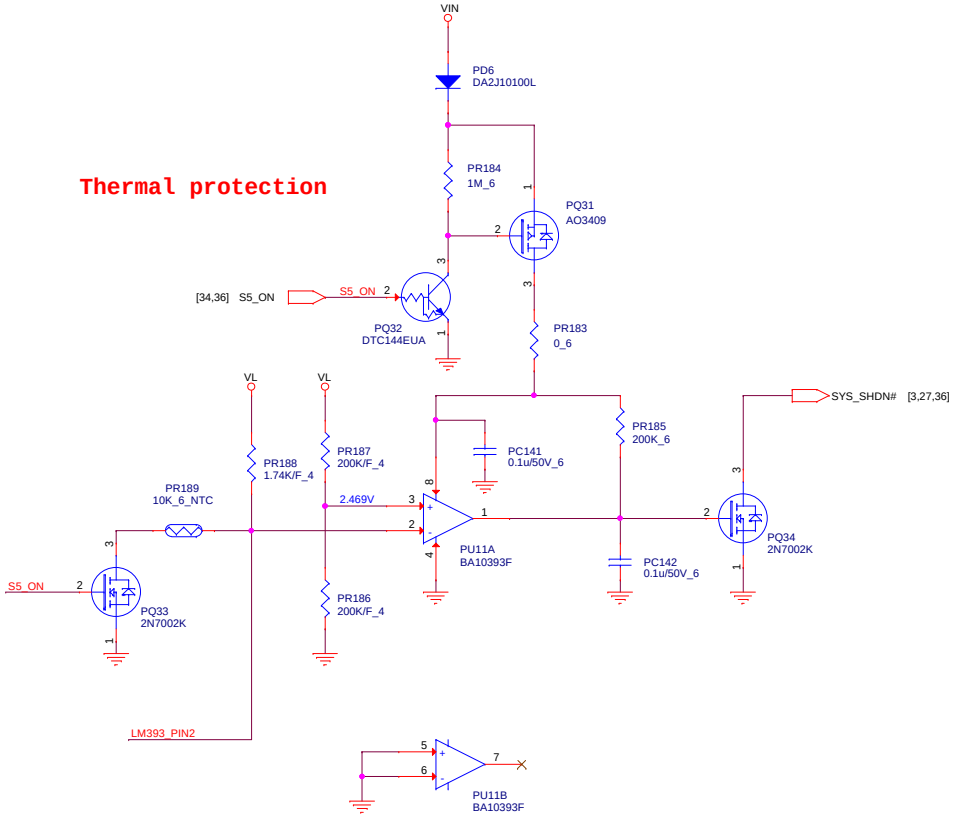
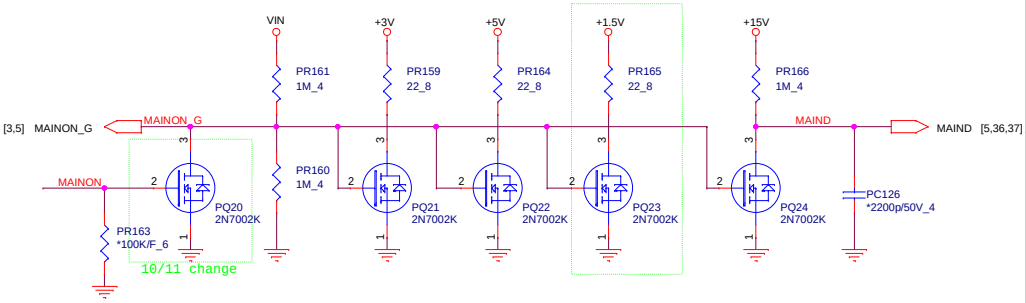


Thermal protection



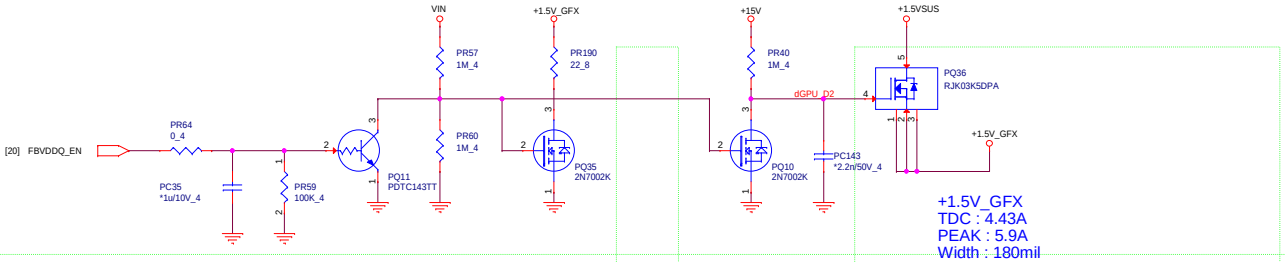


For EC control thermal protection (output 3.3V)

Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	+1.8V/Discharge/Thermal	1A
Date: Monday, January 07, 2013	Sheet 41 of 46	

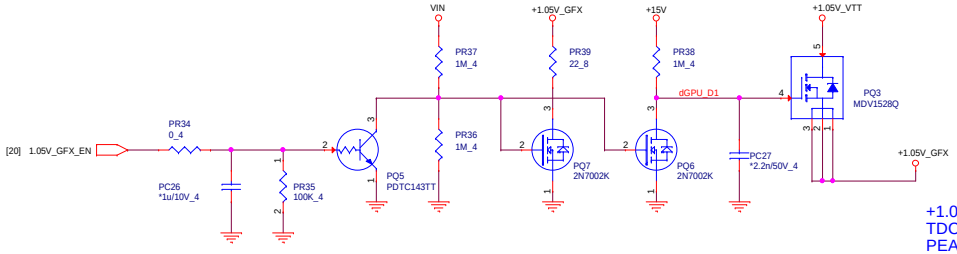
10/1 Change



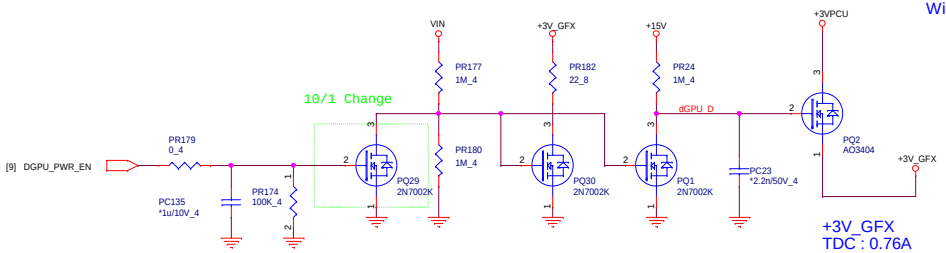
+1.5V_GFX
TDC : 4.43A
PEAK : 5.9A
Width : 180mil

10/5 Reserve switching power for +1.5V_GFX

OCP=7.5A
L ripple current
=(19-1.5)*1.5/(2.2u*290k*19)
=2.165A
Vtrip=7.5-(2.165/2)*14mohm
=0.0898V
Rlimit=0.0898/10uA*8=71.873Kohm



+1.05V_GFX
TDC : 2.3A
PEAK : 3A
Width : 100mil



+3V_GFX
TDC : 0.76A
PEAK : 1A
Width : 40mil

Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	+VGPU_CORE(UP1642PQAG)	1A
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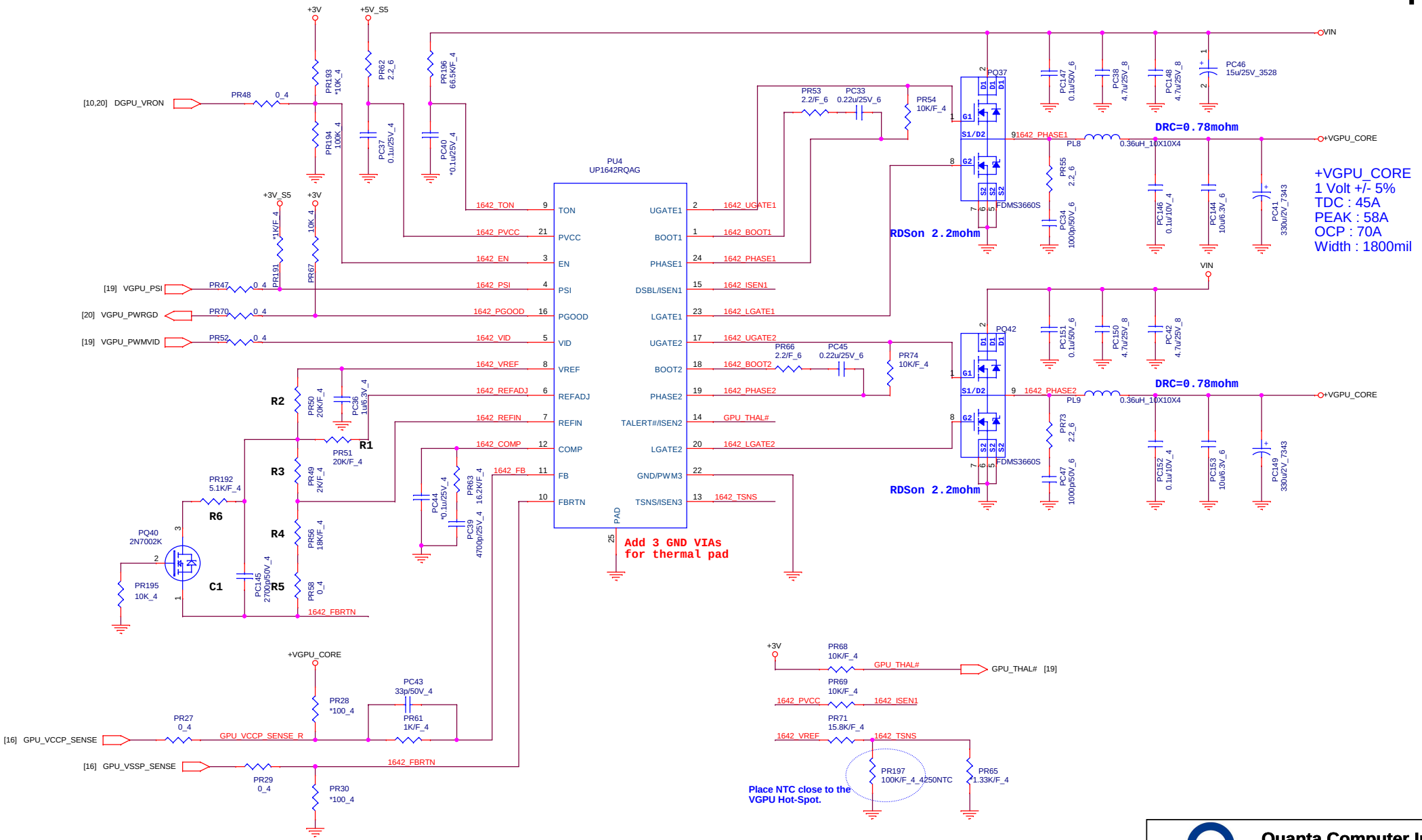
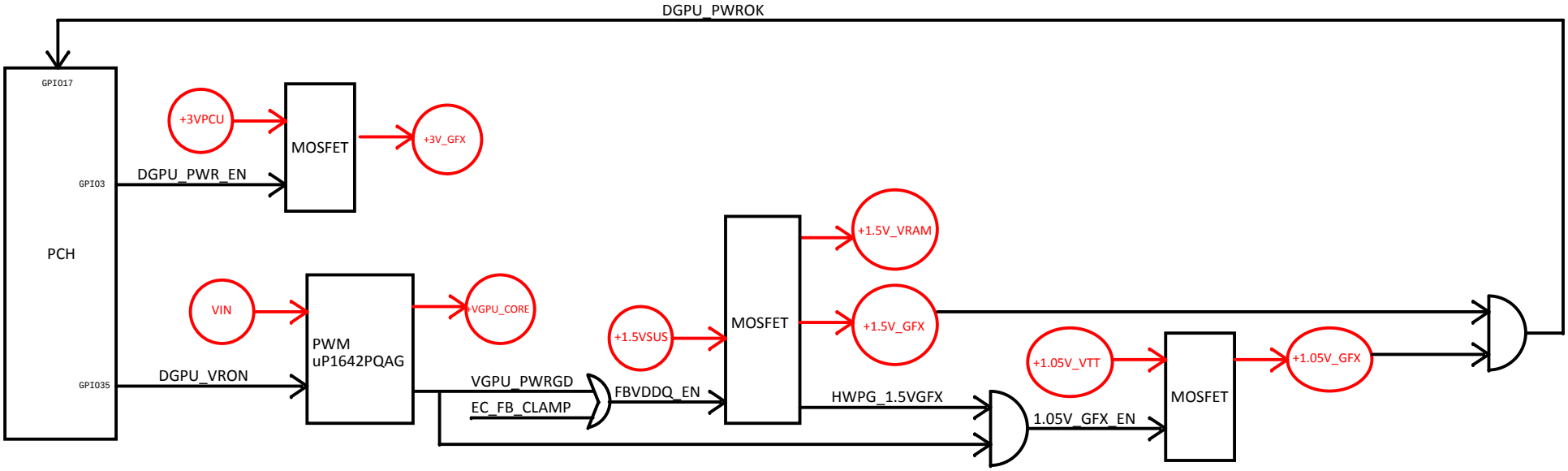
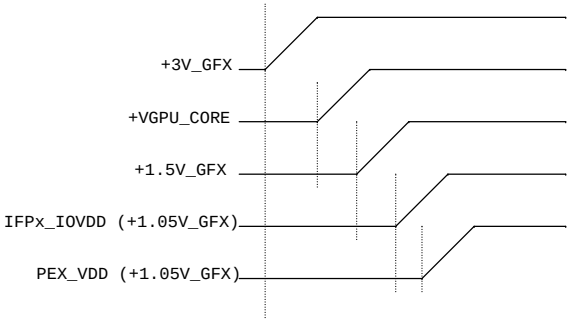


Quanta Computer Inc.	
PROJECT : ZQK	
Size	Document Number: +VGPU_CORE(UP1642PQAG) — Rev: 1A
Date: Monday, January 07, 2013	Sheet 43 of 46



Power Sequence

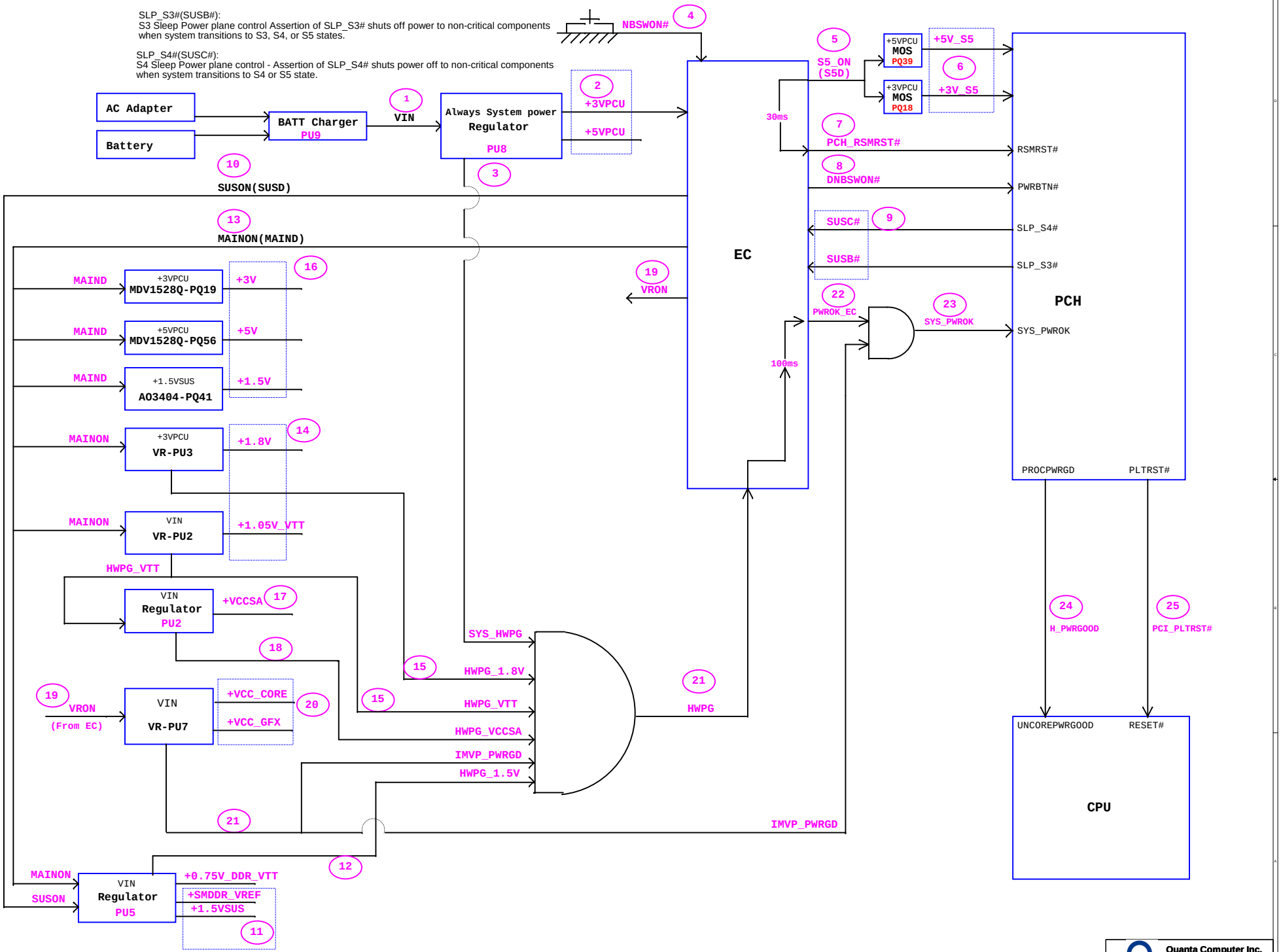


All rails must be powered off within 10 ms from the first rail powering off.

Quanta Computer Inc. PROJECT : ZQK		
Size	Document Number: Power Sequence	Rev 1A
Date: Monday, January 07, 2013	Sheet 44 of 46	

SLP_S3#(SUSB#):
S3 Sleep Power plane control Assertion of SLP_S3# shuts off power to non-critical components when system transitions to S3, S4, or S5 states.

SLP_S4#(SUSC#):
S4 Sleep Power plane control - Assertion of SLP_S4# shuts power off to non-critical components when system transitions to S4 or S5 state.



Quanta Computer Inc.
PROJECT : ZQK
power sequence block diagram
Rev 1A
Monday, January 07, 2013

Model	Date	CHANGE LIST
ZQK	1203	1.Change C774 from 0.1uF to 39pF for ESD 2.Add C841~C850 39pF for ESD 3.Change U19,U21,U23,U26,U43,U46,U48,U49 PN from AKD5JGST404 to AKD5JGST407
	1205	1.Change LED1/LED2 PN：BEB00028ZA0；FP：led19-123-y2st1d-c30-2t-4p 2.Change R383/R392 from 47 ohm to 56 ohm
	1206	1.Change SW2 PN： DHPATE2CK03；FP：sw-ate-2ck-v-tr-4p
	1210	1.Delete PL2/PL3/PL4/PL5 2.Add RTC charge circiut and modify CN14 PN and FP (DFHS02FS032/ml1220-smt) 3.Update CN4 FP to "dp-adis0022-p001a-20p-smt"
	1211	1.Add mSATA re-driver circuit 2.Change CN22 PN & FP as same as CN13
	1212	1.Modify Hole4 FP to H-TC197BC142D142P2 2.Change mSATA redriver power rail to +1.5V
	1213	1.Add R828~R831 for co-layout 2.Add N14M-GE binary strap setting information
	1214	1.Change USB DB power to 4 pins 2.Change CN4 PN to DFTD20FR001
	1217	1.Update Hole6/Hole17/Hole22 FP 2.Add C866 by FAE suggestion 3.Change C706 from 10uF to 4.7uF 4.Add pull down 100K by EC-Anda command (R832/R833/R834) 5.Change TEMP_MBAT fromPJ1 pin 5 to pin 6 (BATT_EN#) , then pin 6 is NC pin 6.Un stuff PR96 7.Add R835 and change R785 to 5.1M ohm 8.Mark R746 to NSW@ due to pin18 of U7 has internal +3V
	1219	1.SUSLED# power from +3V_S5 to +3V_PCU (for Deep S3) 2.Change eDP connector CN8 PN and FP (DFHS40FS095 / gs12401-1011-40p-r-nh-smt)
	1220	1.Add net PCH_SUSWARN# connect to Pin78 of EC (GPJ2) 2.Add net PCH_SUSACK# connect to Pin79 of EC (GPJ3)
	1221	1.Change PR191 PU voltage from +3V to +3V_S5
	1224	1.Unstuff PR28/PR30 2.Reserve R837
	1225	1.Change PU4 PN from AL001642000 to AL001642001
	1226	1.Change U15 PN from AJ085870F03 to AJ085870F04
	1228	1.Co-layout mSATA re-driver IC-U51 (PS8521A & ASM1466)
	0102	1.Unstuff PR191 (Already PU on HW side) 2.Reserve R842/R843
	0103	1.SWAP EC pin：BATLED1# change to pin32 ; ME_WR# change to pin25
	0104	1.Change U38 PN from AJ0QPRG0T03 to AJSLJ8C0T05
	0107	1.Update Hole6/Hole17 FP 2.Update Pad1 PN to FBZRK011010 3.Update Hole4 PN to FBAJ2005010

Quanta Computer Inc. PROJECT : ZQK Size / Document Number: Change list / Rev: 1A Date: Monday, January 07, 2013 Sheet 46 of 46	DOC NO.	PROJECT MODEL :	ZQK	APPROVED BY:		DATE:
		PART NUMBER:		DRAWING BY:		REVISON: