

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT

DB

QP/N

32ZM2PB0000
33ZM1MA0010
34ZM2TB0000
35ZM2LB0000
3BZM2BB0000

USB&PCIE PORT

USB Port#	Destination
0	Right top
1	Right bottom
2	Left side
3	Bluetooth
4	Camera
5	Touch Screen
6	Mini-WLAN
7	Mini-WWAN

PCI-E Port#	Destination
PCI-E-1	Mini-WWAN
PCI-E-2	Mini-WLAN
PCI-E-3	Card reader
PCI-E-4	LAN

Power

+3.3V_ALW/+5V_ALW(MAX17020)
PAGE 36

+1.8VSUS(RT8207)/
+VTT_MEM
PAGE 35

+VCC_CORE (MAX8796)
PAGE 33

CHARGER (MAX8731A)
PAGE 32

+VCC_GFX_CORE(RT8209A)
PAGE 31

+VCCP(RT8209A)/
+VCC1.5(RT9018B)
PAGE 34

ZM2 BLOCK DIAGRAM

CLOCK GEN

SLG8SP513VTR

Page 14

DDRII-SODIMM

Page 12

CHA

667 MHZ

Intel
PineView-M N470
559 Micro-BGA

22mm X 22mm

Page 3, 4, 5, 6

VGA

CRT

Page 16

LVDS

10.1" LCD

Page 15

FAN & THERMAL
EMC1423

Page 26

DMI x2

Note:
Half-size Mini-card for WLAN

WLAN

Page 20

Note:
Full size Mini-card for WWAN

WWAN

Page 21

SIM Card

Page 21

SATA

SATA - HDD

Page 22

PCI-E

SD/SDHC/MMC card reader
(RTS5208)

Page 19

USB 2.0

USB CNN x3

Page 27

CCD

Page 15

Bluetooth

Page 20

PCI-E
USB2.0

PCI-E

LAN
BCM57760

Page 24, 25

RJ-45

Page 25

HD Audio

Audio Codec
ALC269

Page 28

DMic

Page 28

MIC-In Jack

Page 28

HP Jack

Page 28

INT Speaker
1W x2

Page 28

LPC

EC
MEC5035

Page 17

17X8

ECE1077
PG 23

Keyboard
PG 23

PS/2

Touchpad
Connector

PG 23

QUANTA
COMPUTER

Title BLOCK DIAGRAM			
Size	Document Number ZM2	Rev D	
Date	Monday, March 01, 2010	Sheet	1 of 43

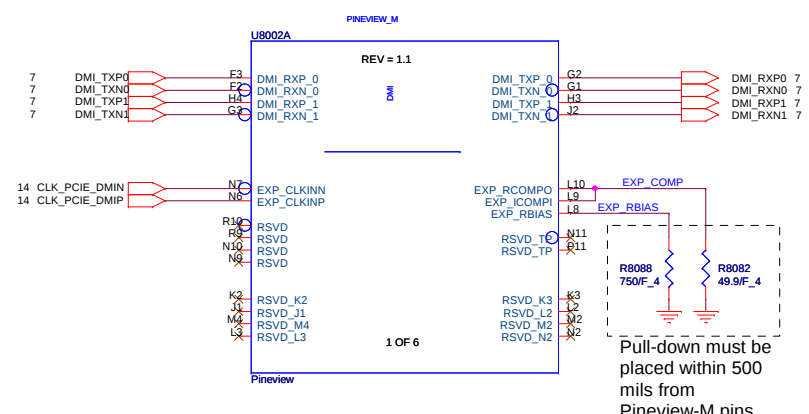
Table of Contents

PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-6	Prineview
7-11	TGP
12	DDRII SO-DIMM(200P)
13	XDP Debug Port
14	Clock Generator
15	LCD Conn. ,CCD,TouchScr
16	CRT Conn
17	SIO(MEC_5035)
18	FLASH/RTC
19	Card Reader-RTS5208
20	Mini Card(WLAN)
21	MINI-WWAN
22	SATA (HDD)
23	KB/TP
24	LAN POWER
25	LAN(BCM57760)
26	FAN & Thermal
27	USB
28	Audio CODEC(ALC269)
29	LED &SWITCH
30	System Reset Circuit
31	VGA Power
32	Charger (MAX8731A)
33	CPU(MAX8796)
34	1.05VCCP & VCC1.5
35	1.8VSUS & 0.9VTT (TPS51116)
36	3.3V/5V_ALWPower
37	RUN Power Switch
38	DCIN&Batt
39	PAD& SCREW
40	EMI CAP
41	SMBUS BLOCK
42	Power Block Dianram
43	Port Mapping

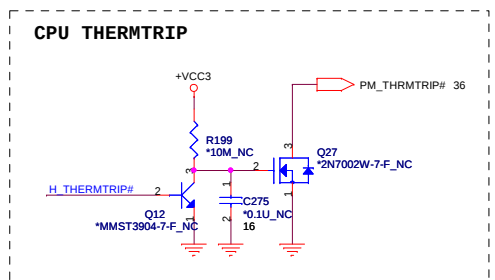
Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	15,18,,32,33,35,36,40	MAIN POWER		S0~S5
+VCCRTC	+3.0V~+3.3V	10,11,17,18	RTC		S0~S5
+3.3V_ALW	+3.3V	17,18,24,25,29,31,32,34,35,36,37,38,40	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	23,24,29,34,35,36,37,38	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	15,24,36,37	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	24,25,40	LAN POWER	LAN_PWR_ON	
+5V_SUS	+5V	24,27,29,33,37,40	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	15,24,29,30,33,34,37	SLP_S5# CTRLD POWER	SUS_ON	
+1.8VSUS	+1.8V	4,5,12,13,34,35,37	SODIMM POWER	SUS_ON	
+VTT_MEM	+0.9V	12,13,35,37	SODIMM POWER	RUN_ON	
+VCC1.8	+1.8V	5,37		RUN_ON	
+VCC5	+5V	11,15,16,22,23,26,28,29,37,40	SLP_S3# CTRLD POWER	RUN_ON	
+VCC3	+3.3V	3,5,6,8,9,10,11,12,13,14,15,16,17,19,20,21,22,24,25,26,28,29,33,37,40	SLP_S3# CTRLD POWER	RUN_ON	
+VCC1.5	+1.5V	5,7,11,20,21,34,37,40	CALISTOGA/ICH8 POWER	RUN_ON	
+VCCP	+1.05V	3,5,8,11,34,40	CPU/CALISTOGA/ICH8 POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	5,33,40	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	15	LCD Power	LCDVCC_TST_EN & ENVDD	
+VCHGR	+10V~+17V	32,38	MAIN BATTERY	CHG_PBATT	

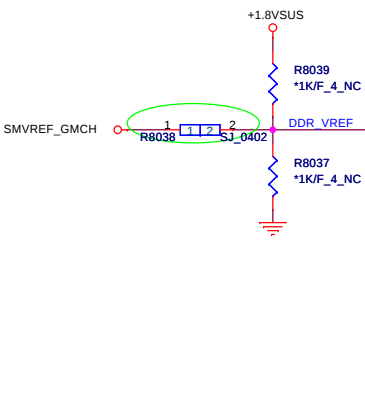
GND PLANE	PAGE	DESCRIPTION
⏏ GNDA_CHG	35	
⏏ GND_1.05V	36	
⏏ AGND_DC/DC	38	
⏏ GND POWER	33	
⏏ AGND_DDR		
⏏ PM6686TR		
⏏ GND	ALL	



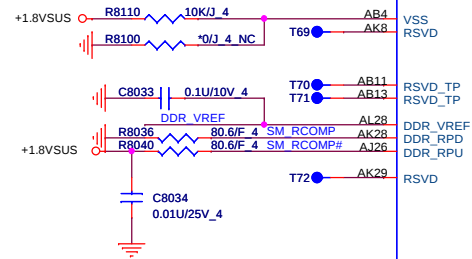
The diagram shows a voltage divider circuit connected to the H_GTLREF pin. The circuit consists of two resistors, R8010 (1K) and R8005 (1K), connected in series between the +VCCP supply and ground. The node between the two resistors is connected to the H_GTLREF pin. A capacitor, C8008 (1uF), is connected from the H_GTLREF pin to ground. Another capacitor, C8007 (220pF), is connected from the H_GTLREF pin to a net labeled *220P/50V_4_NC. The H_GTLREF pin is also connected to ground through a capacitor, C8009 (1uF).



 QUANTA COMPUTER	
Title: PINEVIEW 1/4(DMI,L,VDS)	
Size: Document Number ZM2	Rev D
Date: Wednesday, March 10, 2010	Sheet 3 of 43



1C: reserve for ES1(WW10 MOW)



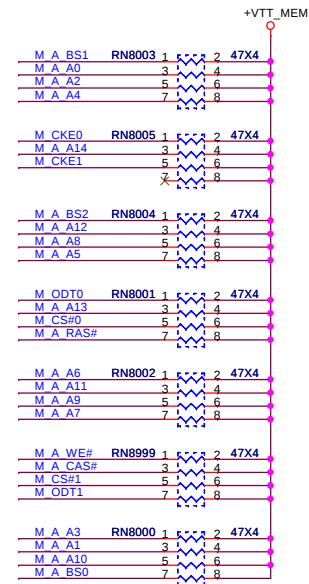
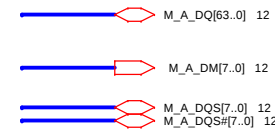
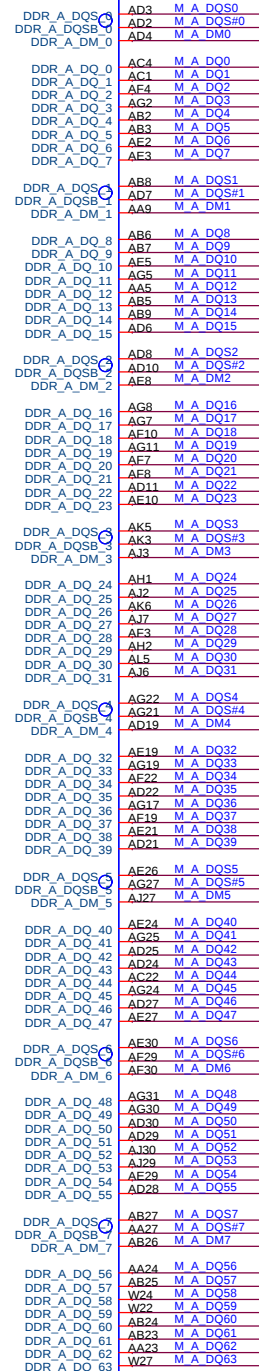
U8002B

PINEVIEW_M

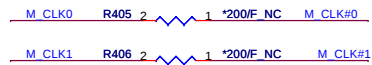
REV = 1.1

2 OF 6

Pineview



10/21 For EMI Reserve



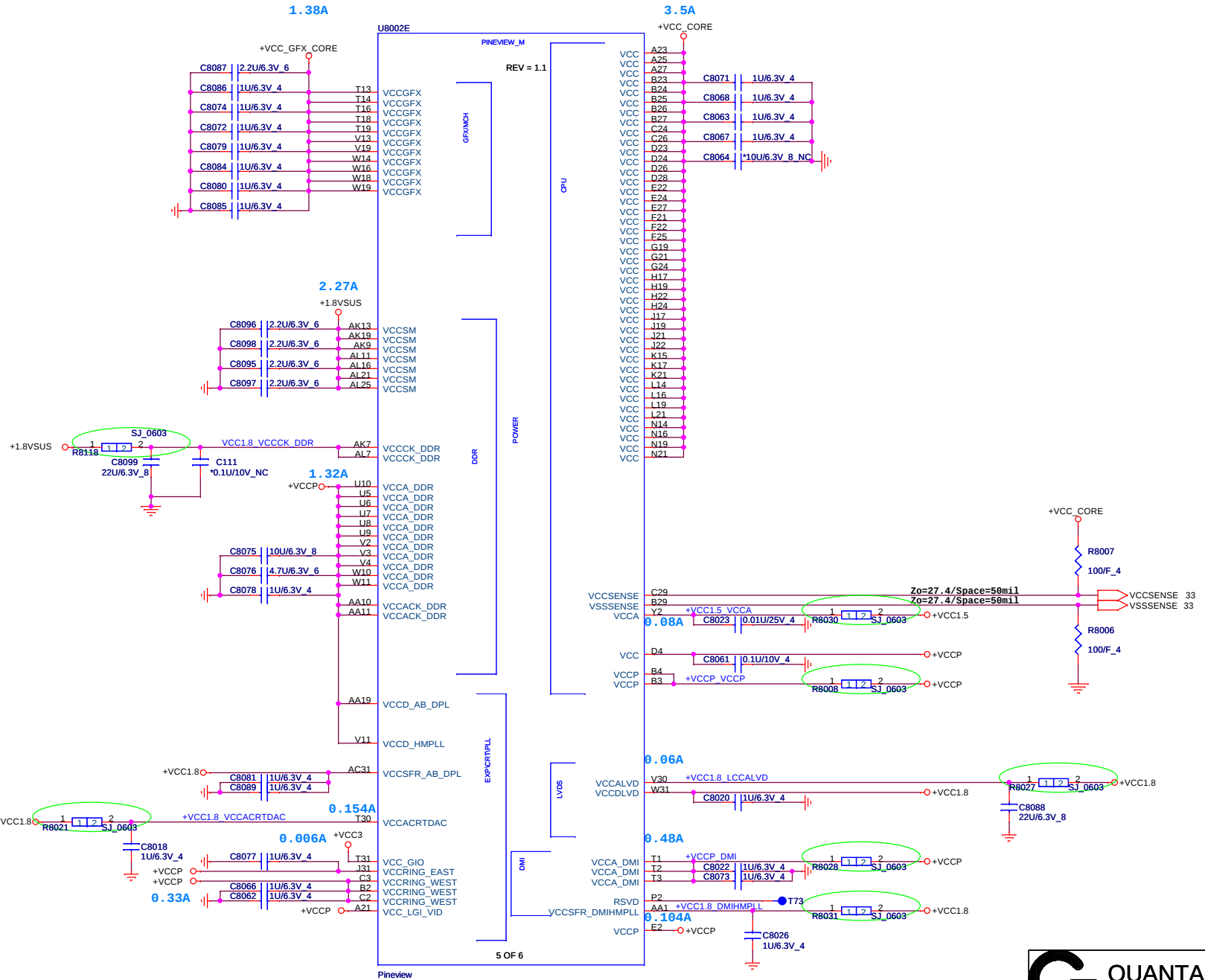
Title
DDR2

Size
Document Number
ZM2

Date: Wednesday, March 10, 2010

Sheet 4 of 43

Rev D



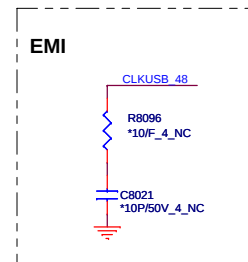
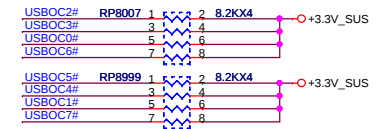
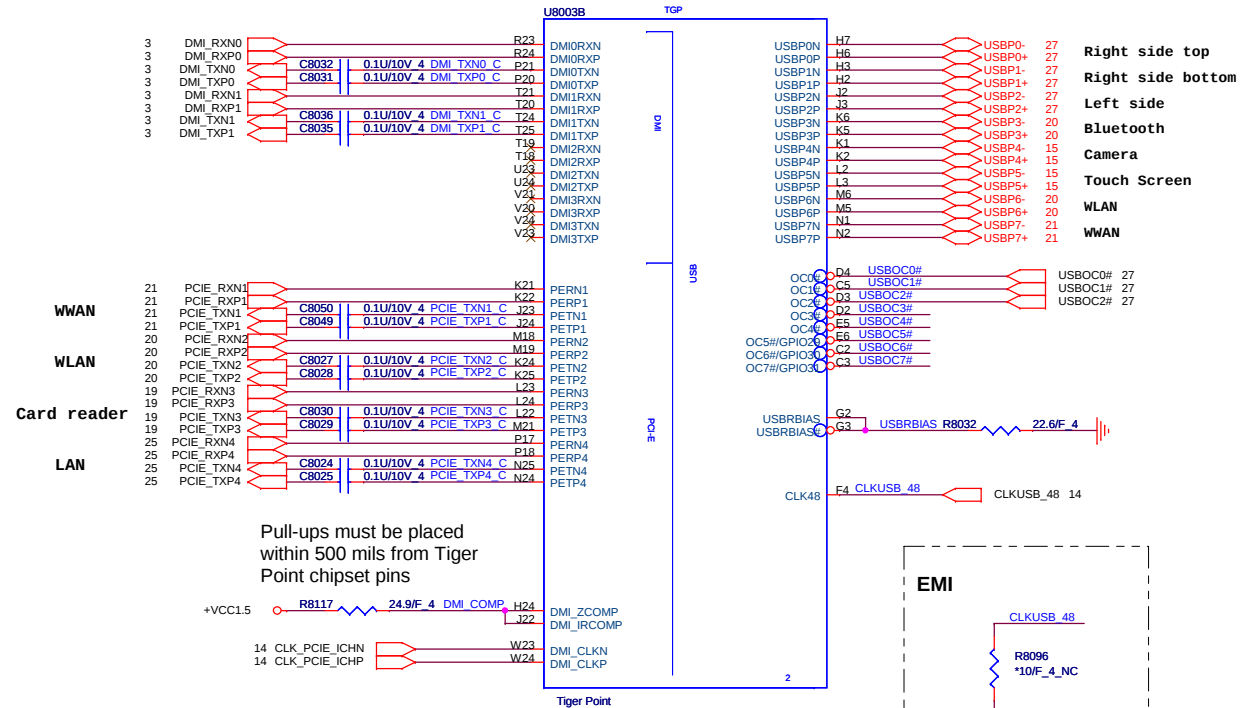
Title
PINEVIEW 3/4(POWER)

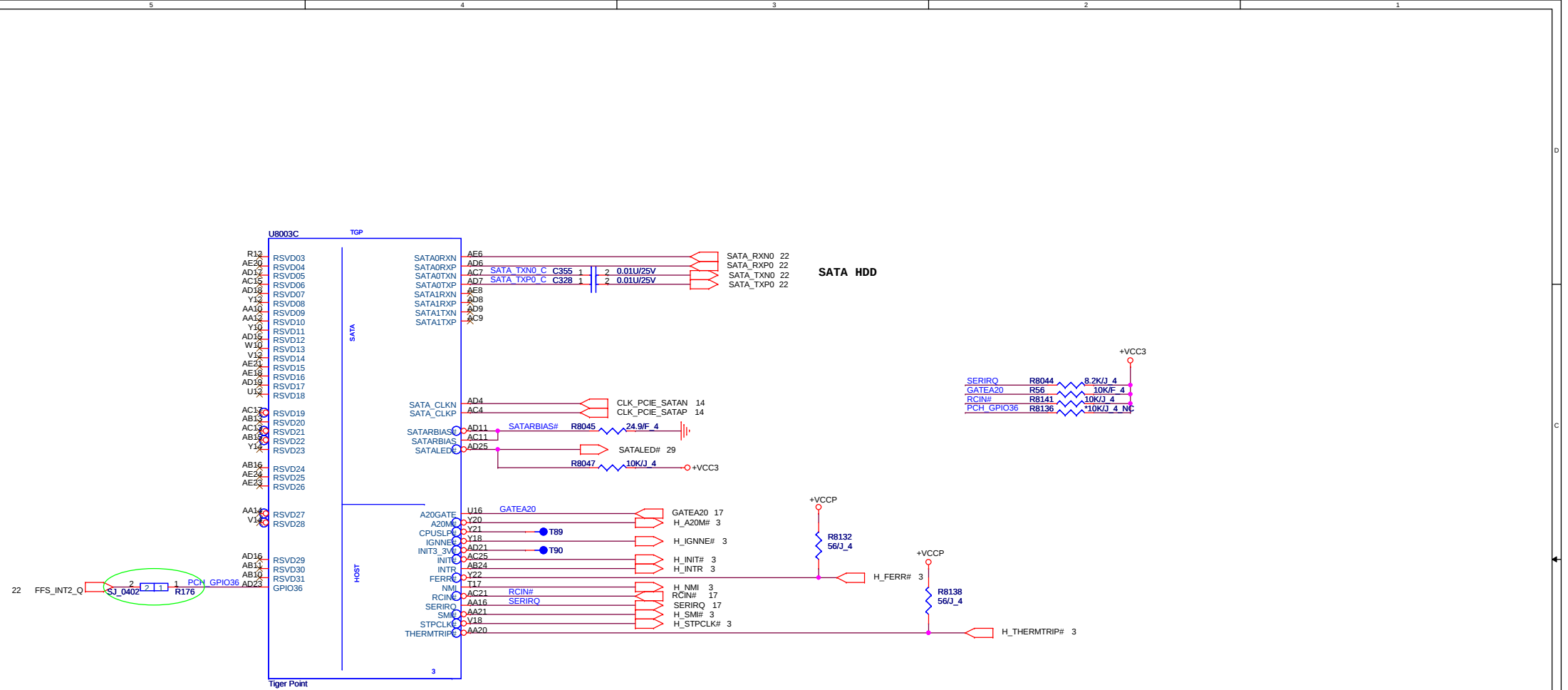
Size
Document Number
ZM2

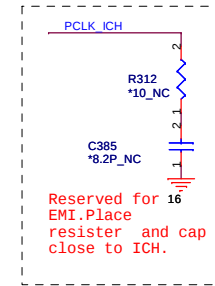
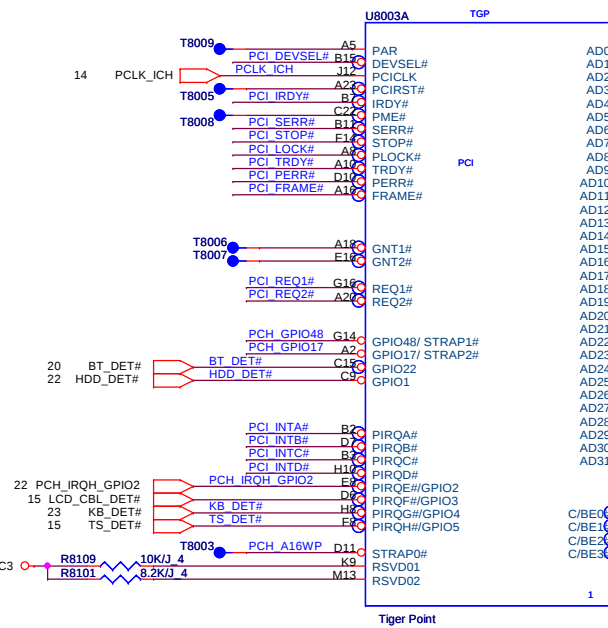
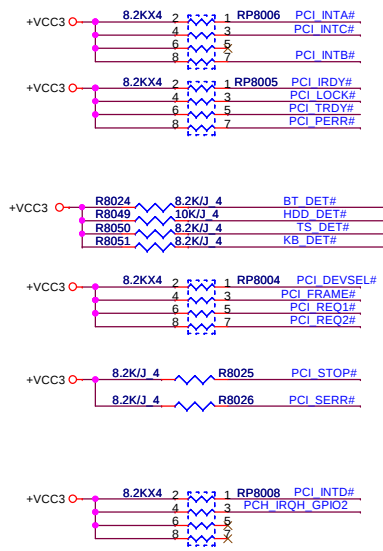
Rev
D

Date: Wednesday, March 10, 2010

Sheet 5 of 43







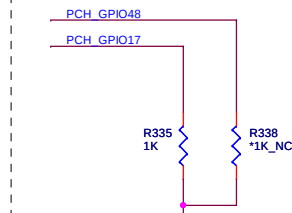
check
ICH Boot BIOS select

PCH_GPIO17 (INT PU)	PCH_GPIO48 (INT PU)	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC (Default)

A16 SWAP Override strap

PCH_A16WP (INT PU)	Low = A16 swap override enabled High = Default
-----------------------	---

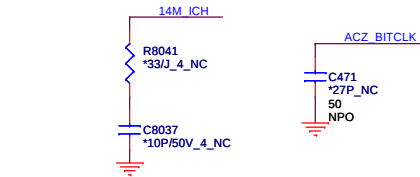
SB Boot BIOS select



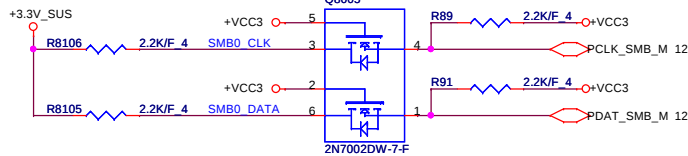
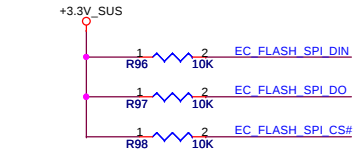
IRQ	Description
PIRQA	USB UHCI Controller #1, #4
PIRQB	AC'97 Codec; option for SMBUS
PIRQC	USB UH Controller #3; SATA/IDE Native Mode
PIRQD	USB UHCI Controller #2
PIRQE	Internal LAN; Option for SCI, TCO, HPET#0,1,2
PIRQF	Option for SCI, TCO, HPET#0,1,2
PIRQG	Option for SCI, TCO, HPET#0,1,2
PIRQH	USB EHCI Controller; Option for SCI, TCO, HPET#0,1,2
PCI_GNT#2	Internal PU Should not be PD



EMI

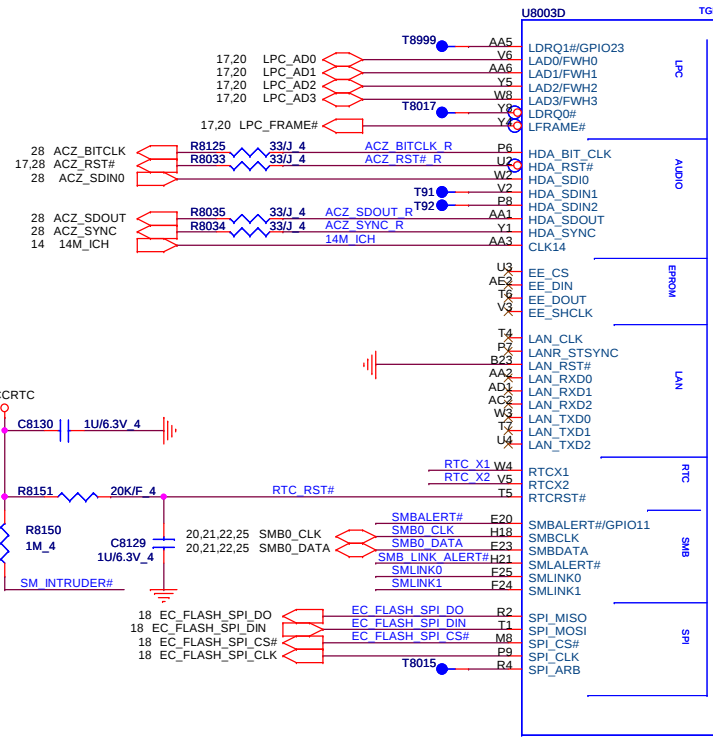


RTC

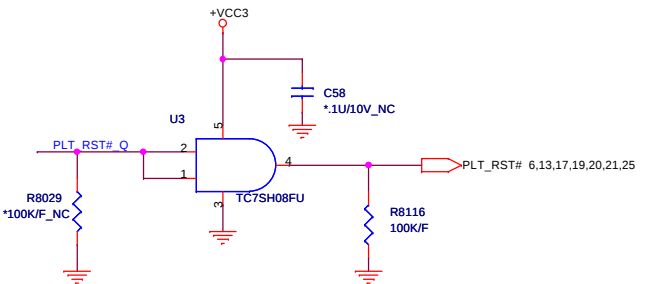
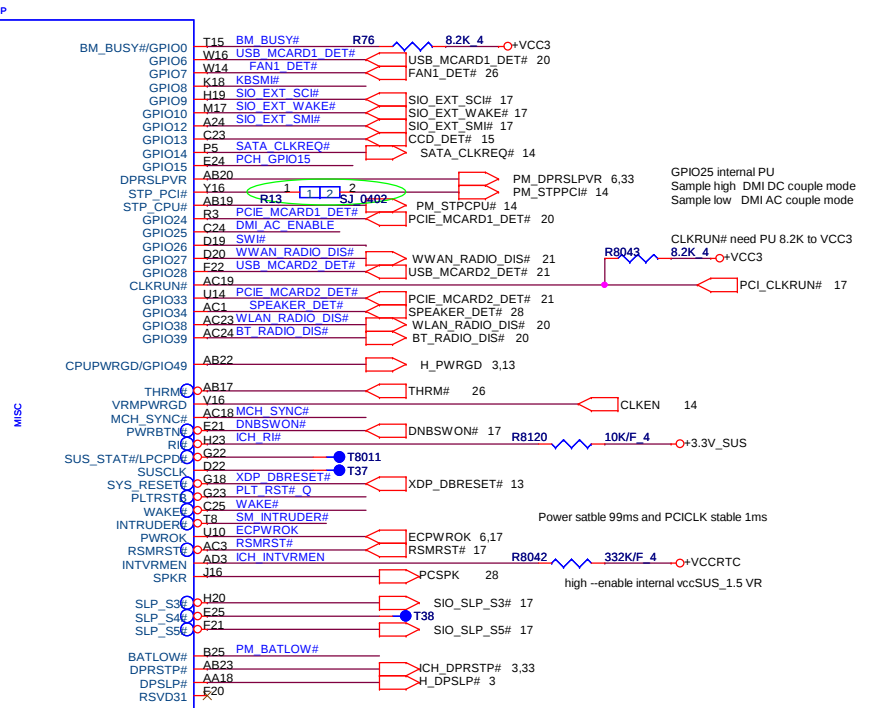
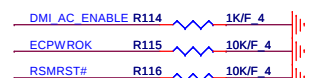
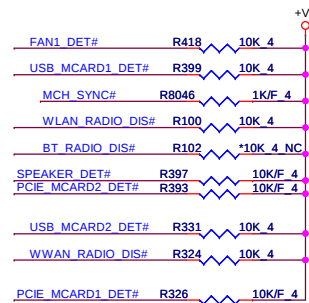
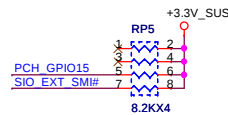
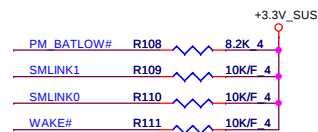
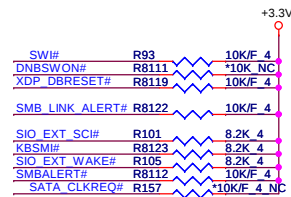


	INTVRMEN
Enable (default)	1
Disable	0

ACZ_SDOUT (INT PD)	ACZ_SYNC (INT PD)	Description
0	0	* 4 x 1s
1	0	Reserved
0	1	Reserved
1	1	1 x 4s(1 port/4 lanes)



Follow ZM1 Support WOL PCIE from S5

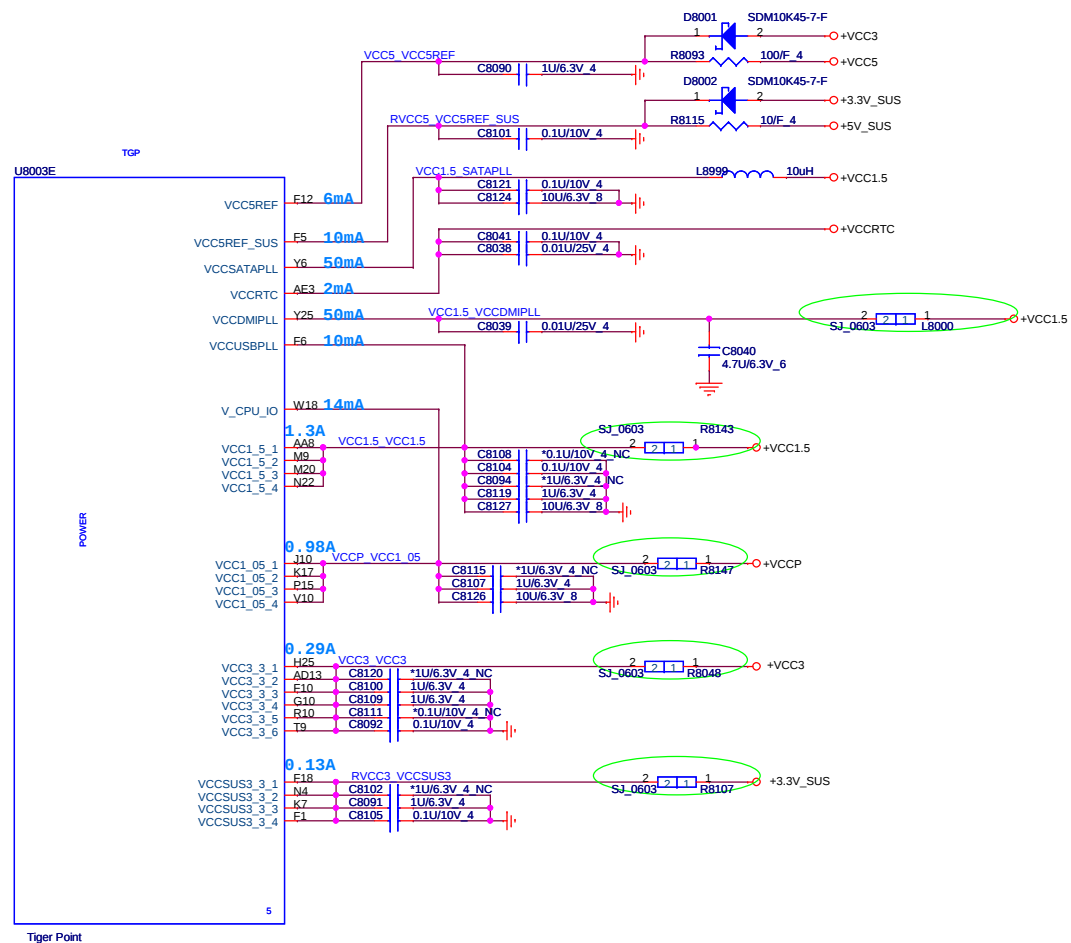
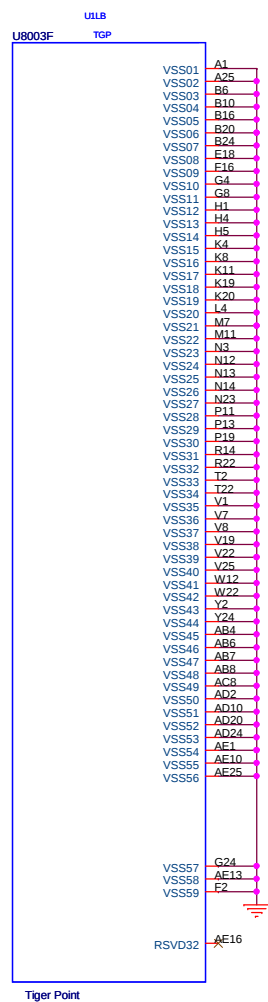


Title TGP 4/5(LPC,HDA,RTC,MISC)

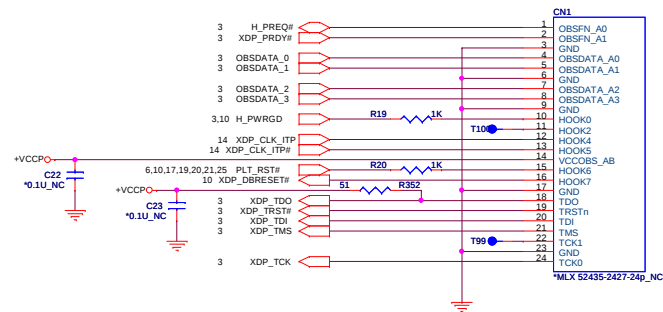
Size Document Number ZM2 Rev D

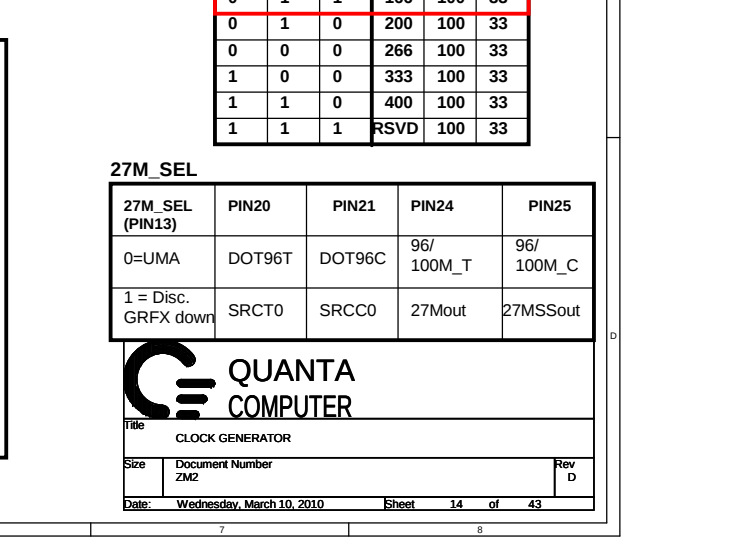
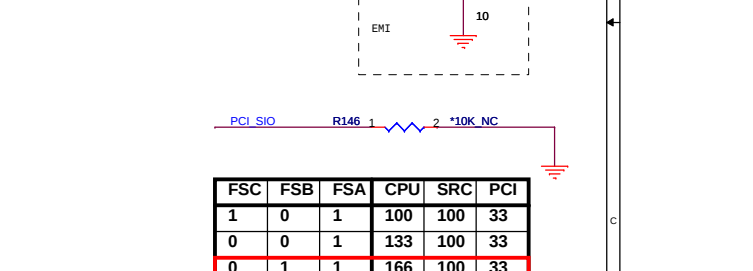
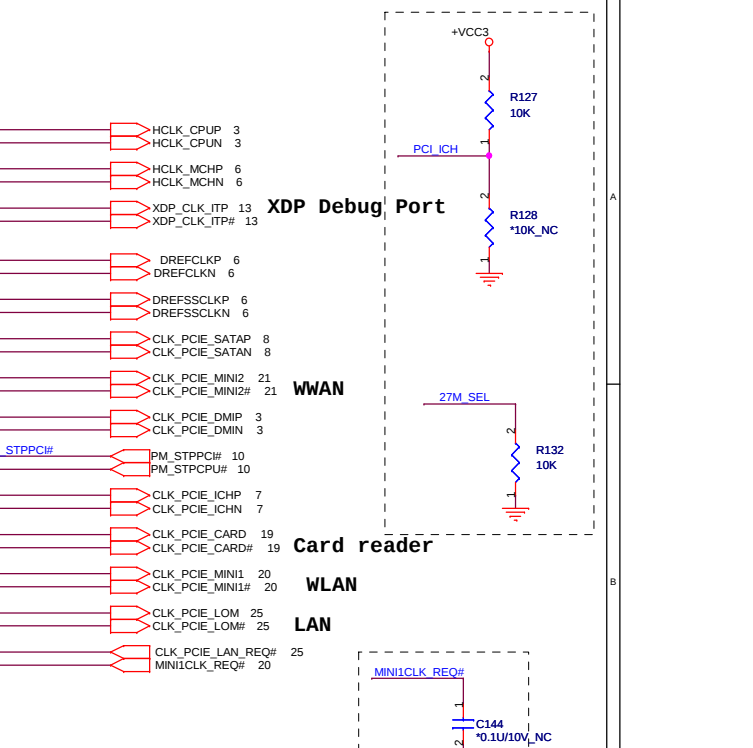
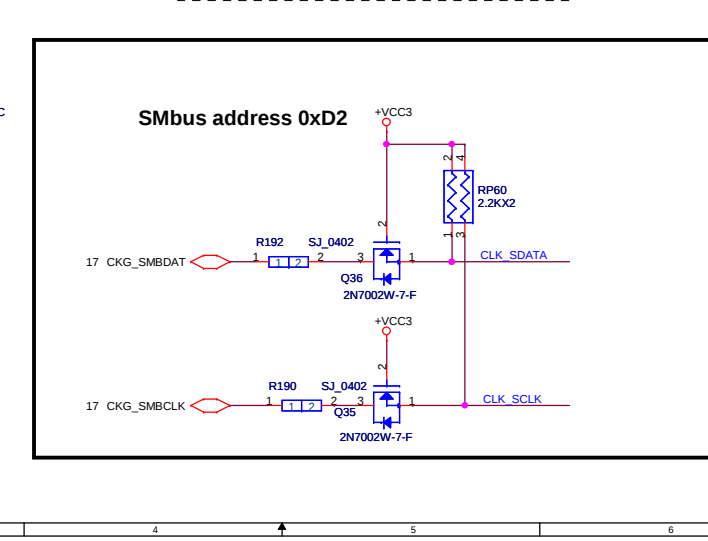
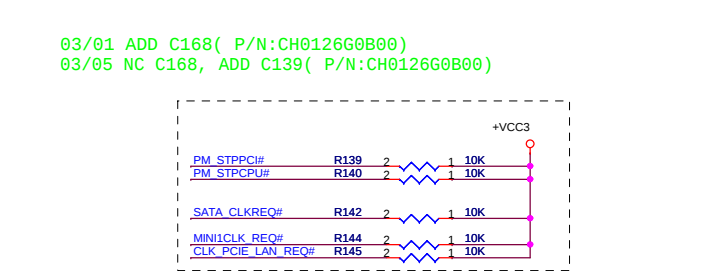
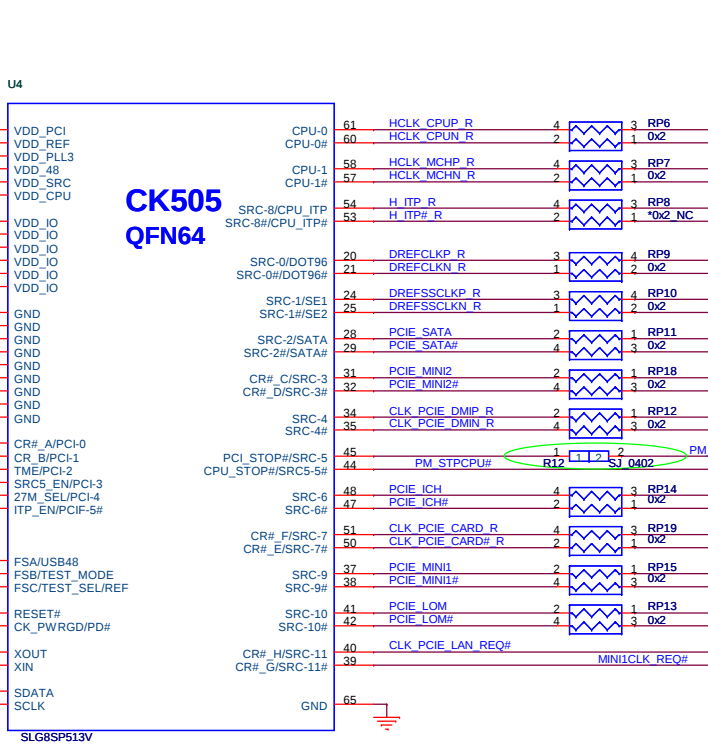
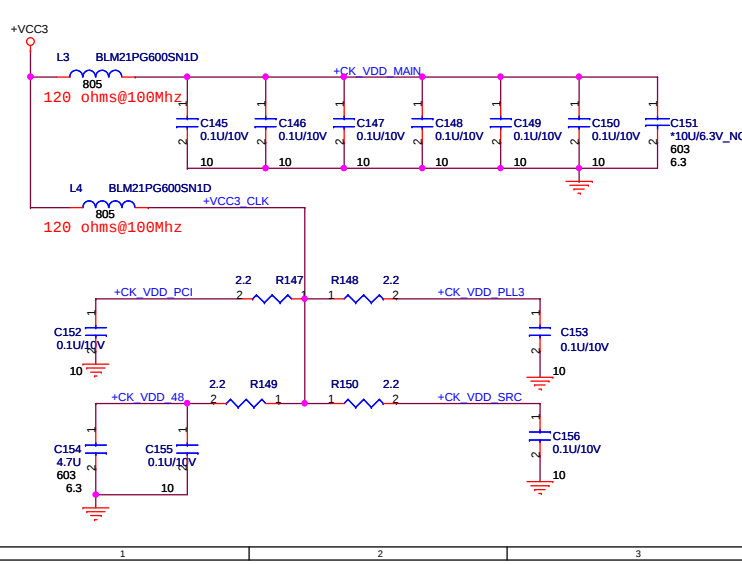
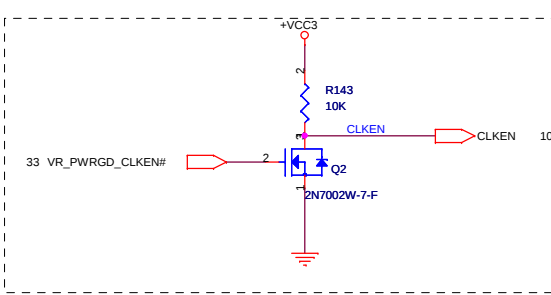
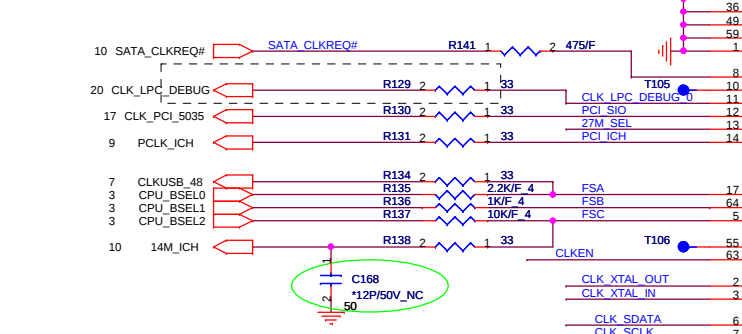
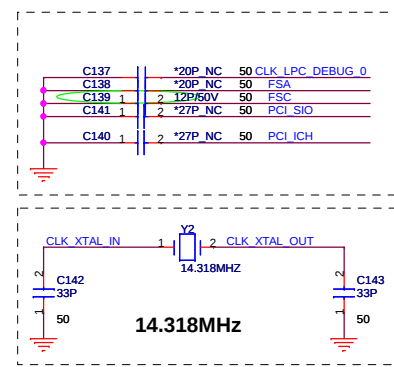
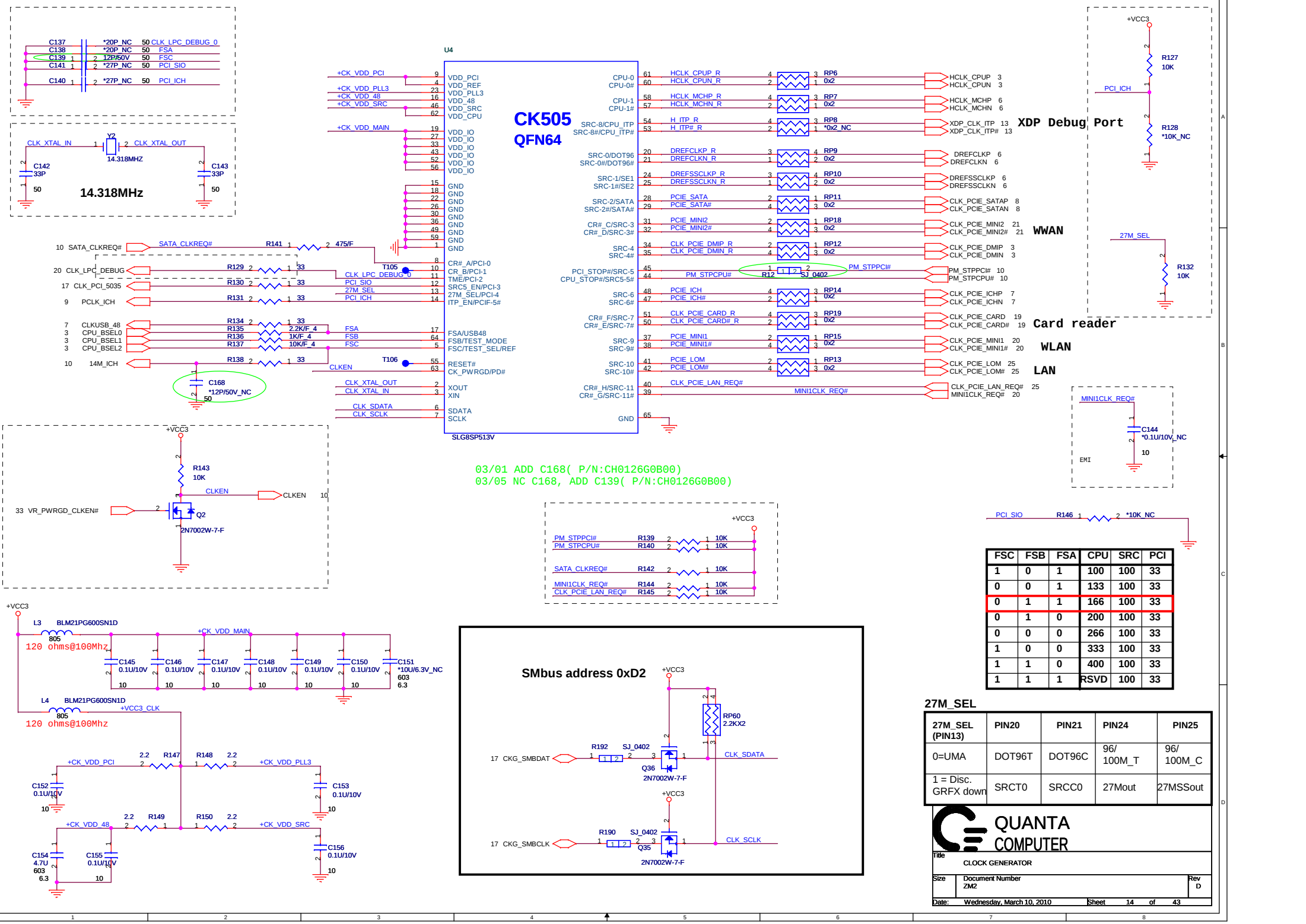
Date: Wednesday, March 10, 2010 Sheet 10 of 43

PWRBTN# internal 18k-42k PU

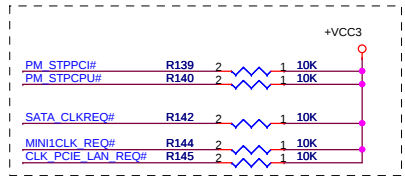








03/01 ADD C168(P/N:CH0126G0B00)
03/05 NC C168, ADD C139(P/N:CH0126G0B00)



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

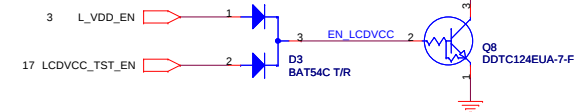
27M_SEL	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout

CLOCK GENERATOR

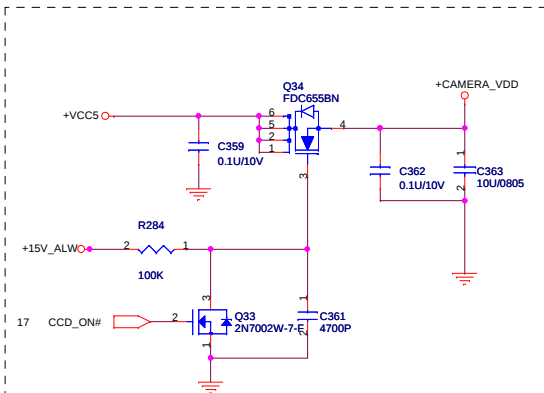
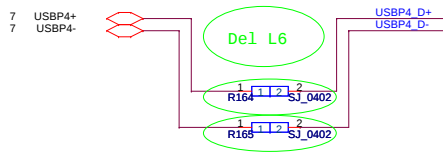
Size: Document Number: Rev D

Date: Wednesday, March 10, 2010 Sheet 14 of 43

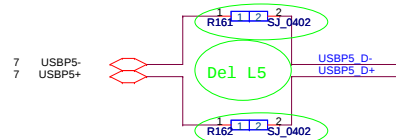
Support the new imbedded diagnostics.



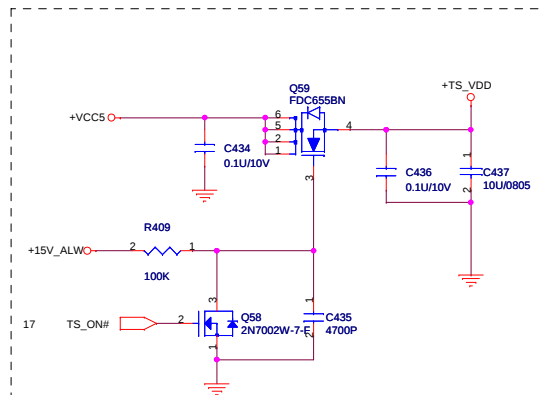
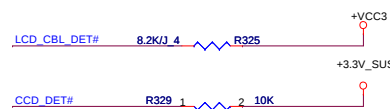
CCD



Touch Screen



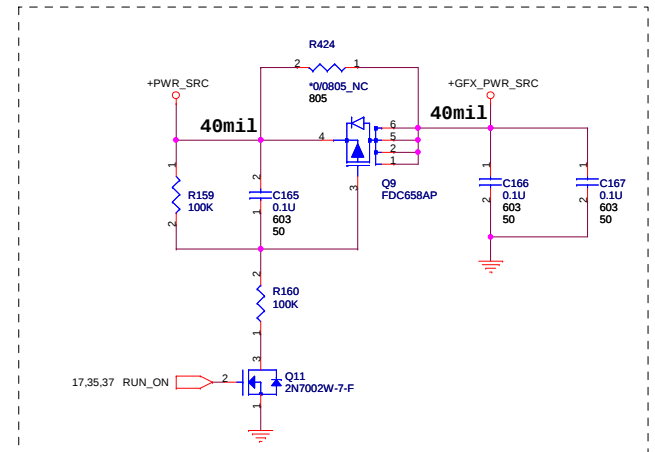
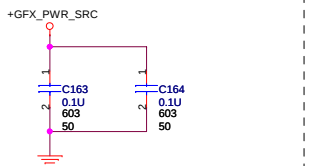
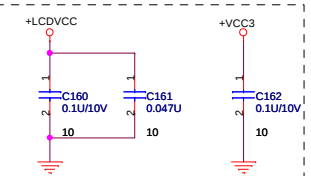
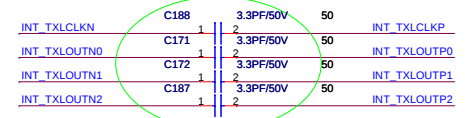
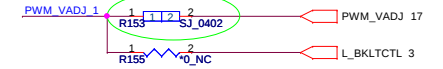
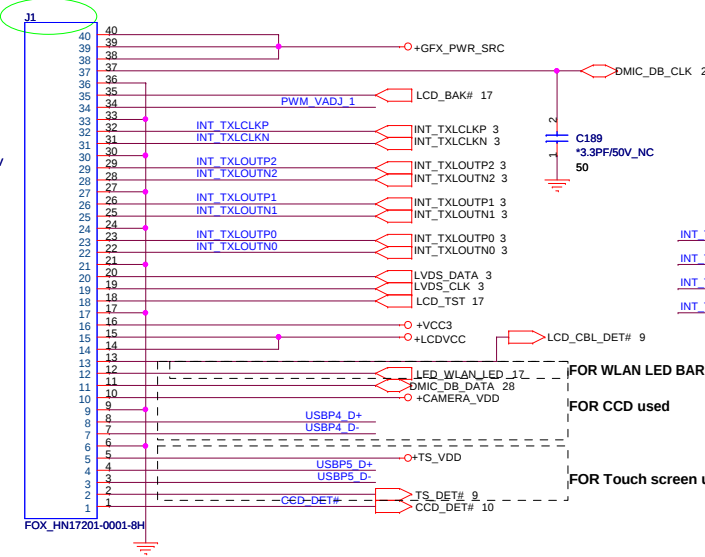
03/01 ADD C171,C172,C187,C188(P/N:CH-33380B00)
03/02 Change J1 P/N from DFHD40MR017 to DFHD40MR029



FOR WLAN LED BAR

FOR CCD used

FOR Touch screen used



QUANTA
COMPUTER

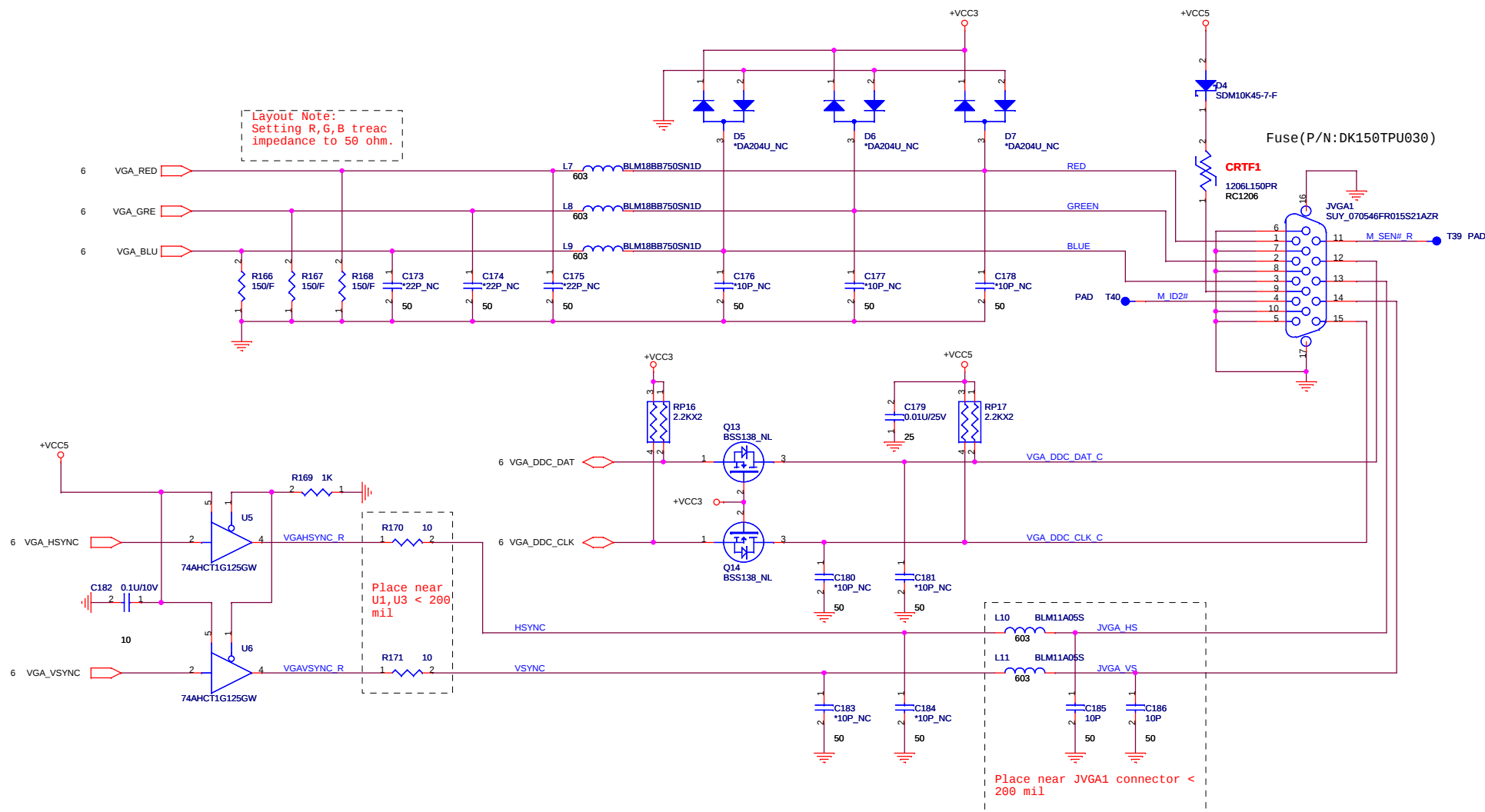
Title
LCD CONN & CCD & TS

Size
ZM2

Date: Wednesday, March 10, 2010

Sheet 15 of 43

Rev
D



Title			CRT&TV CONN
Size	Document Number	Rev	
	ZM2	D	
Date:	Wednesday, March 10, 2010	Sheet	16 of 43

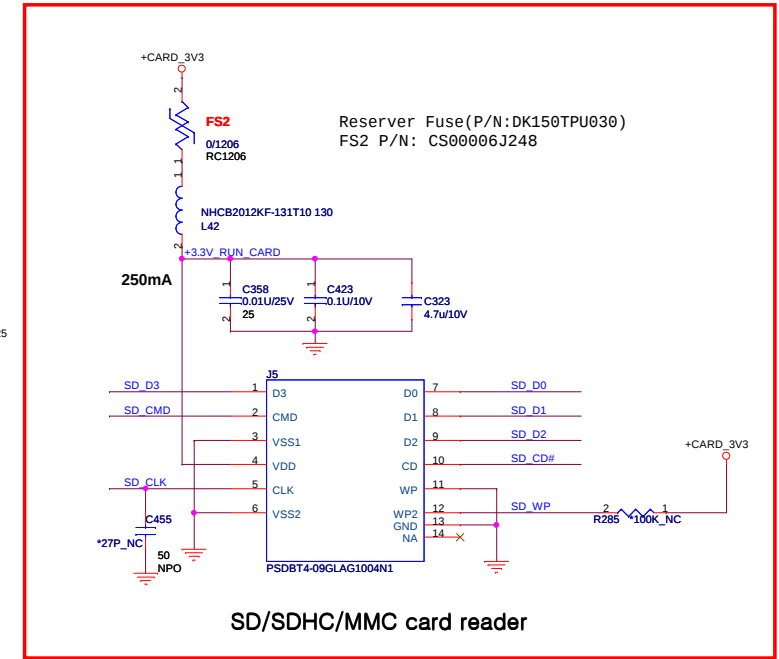
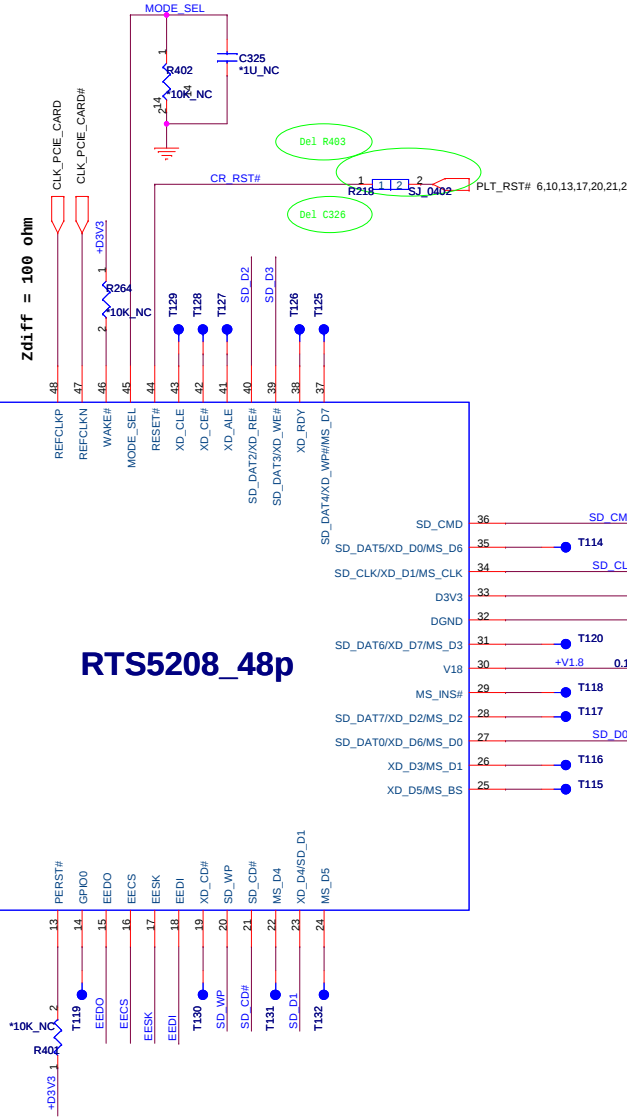
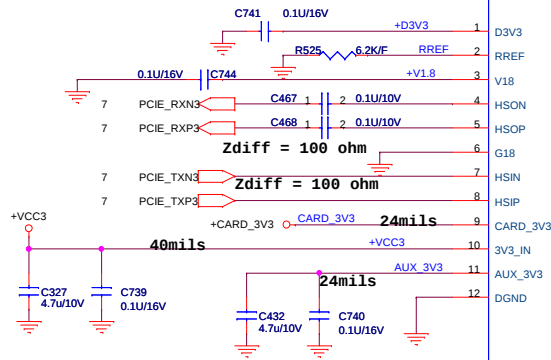
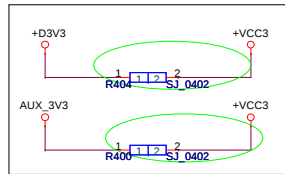
SPI ROM Socket

The schematic diagram illustrates the electrical connections for an SPI ROM socket. On the left, four red arrows represent signals from a microcontroller: EC_FLASH_SPI_CS#, EC_FLASH_SPI_CLK, EC_FLASH_SPI_DIN, and EC_FLASH_SPI_DO. These are connected through resistors R196, R197, and R198 to pins 1, 2, and 15 of the MX25L1605DM2I-12G chip (U8). Pin 15 is also connected to pin 2. A +3.3V_SUS supply is connected through resistor R194 to pin 3 (SPI WP#). The chip's VDD (pin 8) and HOLD# (pin 7) are connected to a common node that goes through resistor R195 to another +3.3V_SUS supply. The WP# (pin 4) is connected to ground through capacitor C201 (0.1uF/10V).

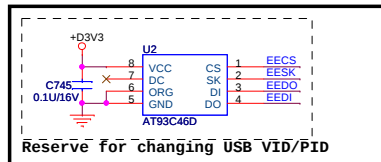
16Mbit (2M Byte), SPI

[illegible]

03/01 Del C326 for ASF issue
03/10 Del C326,R403 Location



Need update EEPROM Footprint

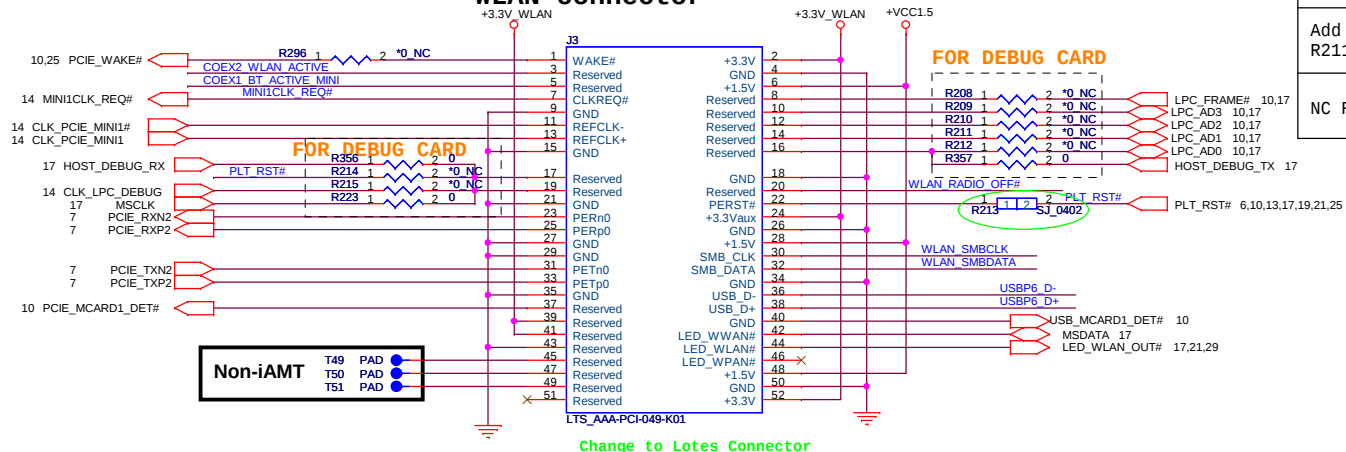


EEPROM

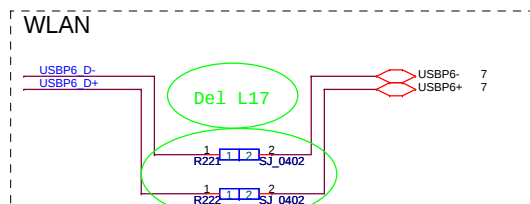
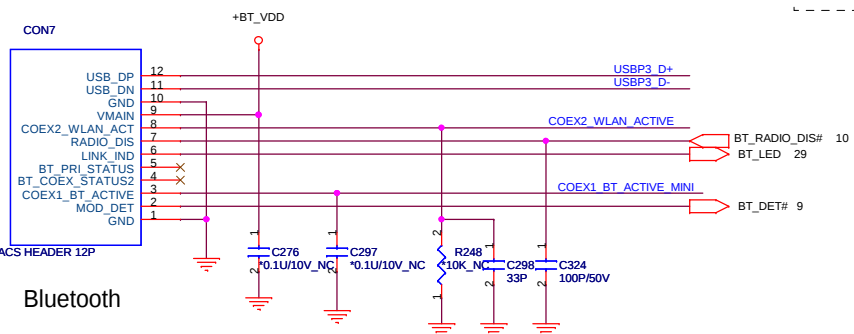
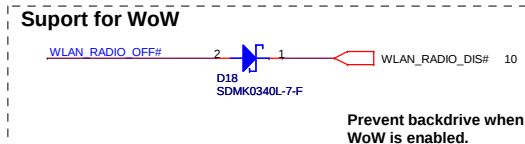
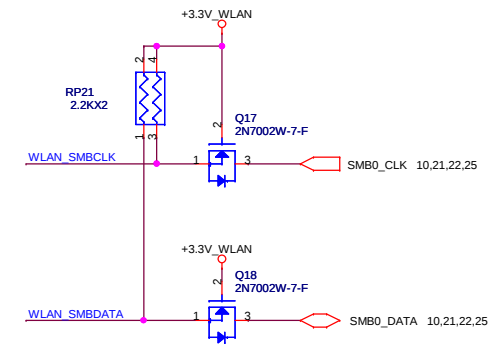
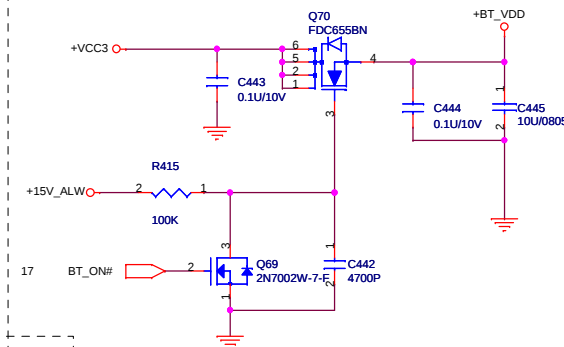
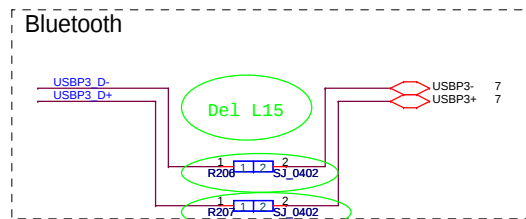
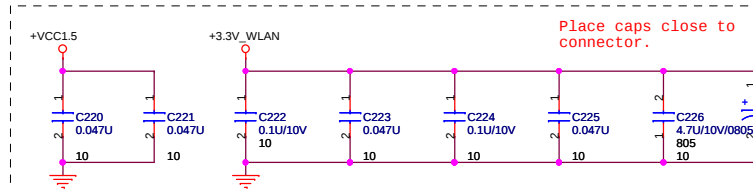


Title			Card Reader
Size	Document Number	Rev	
	ZM2	D	
Date:	Wednesday, March 10, 2010	Sheet	19 of 43

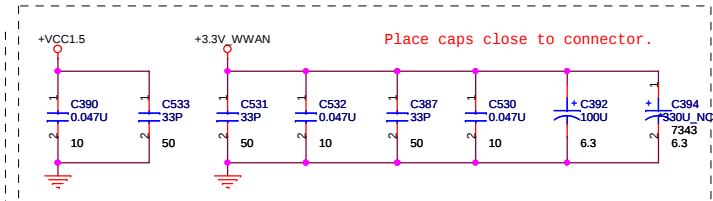
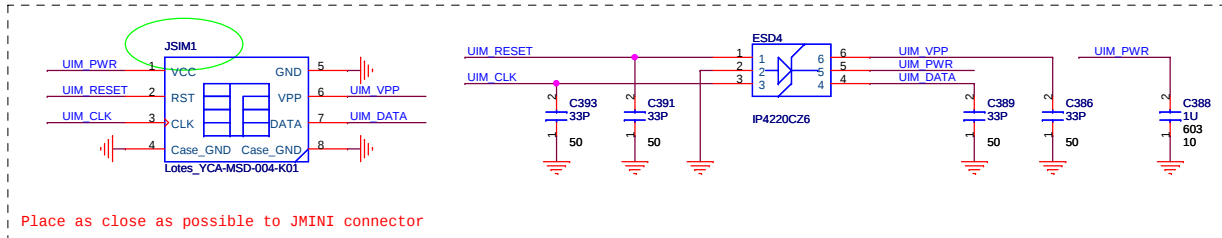
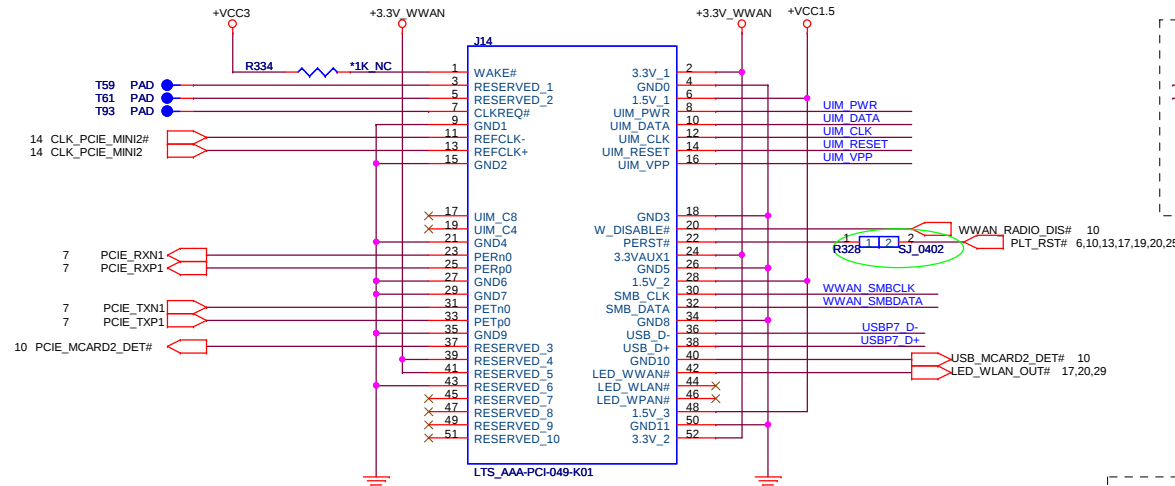
**Half MiniCard
WLAN connector**



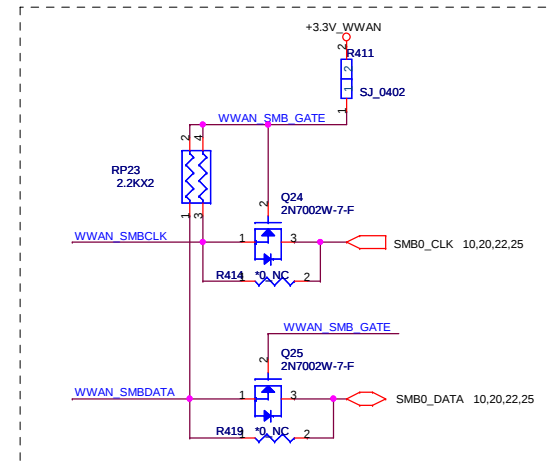
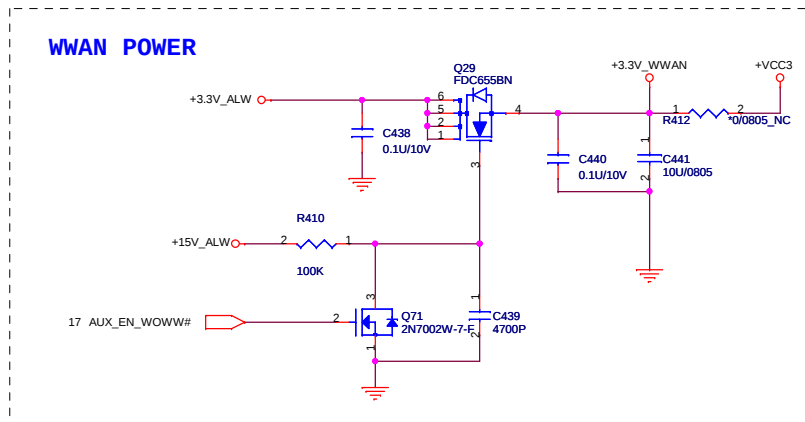
	80 port	EC Debug
	Add R208, R209, R210, R211, R212, R214, R215	Add R356, R223, R357
17	NC R356, R223, R357	NC R208, R209, R210, R211, R212, R214, R215



MiniCard WWAN connector

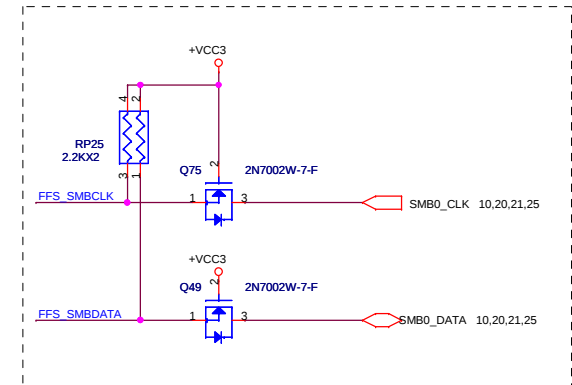
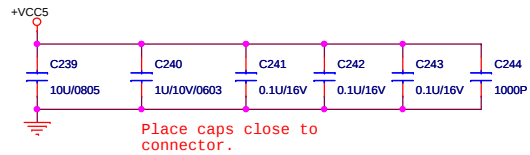
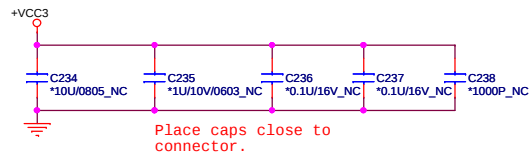
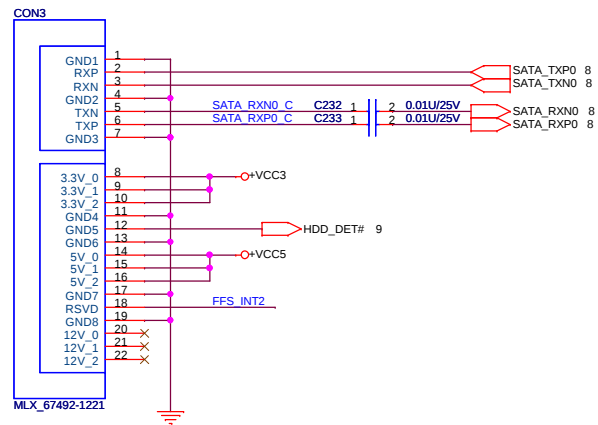


03/02 Change JSIM1 P/N from DG006000020 to DG006000031

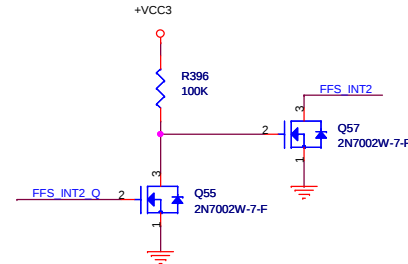
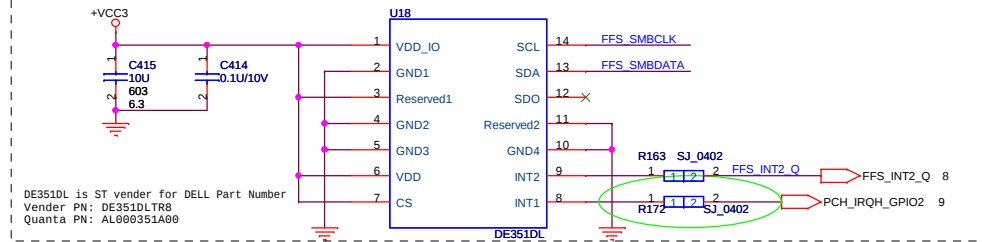


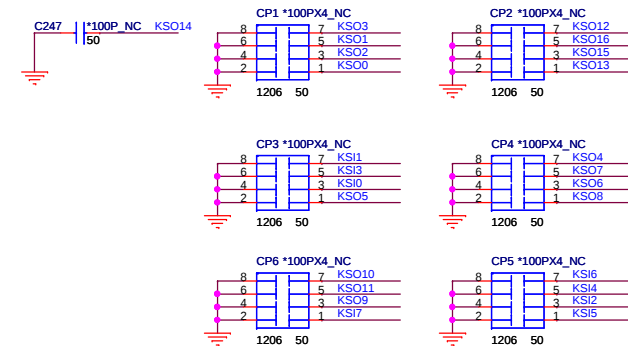
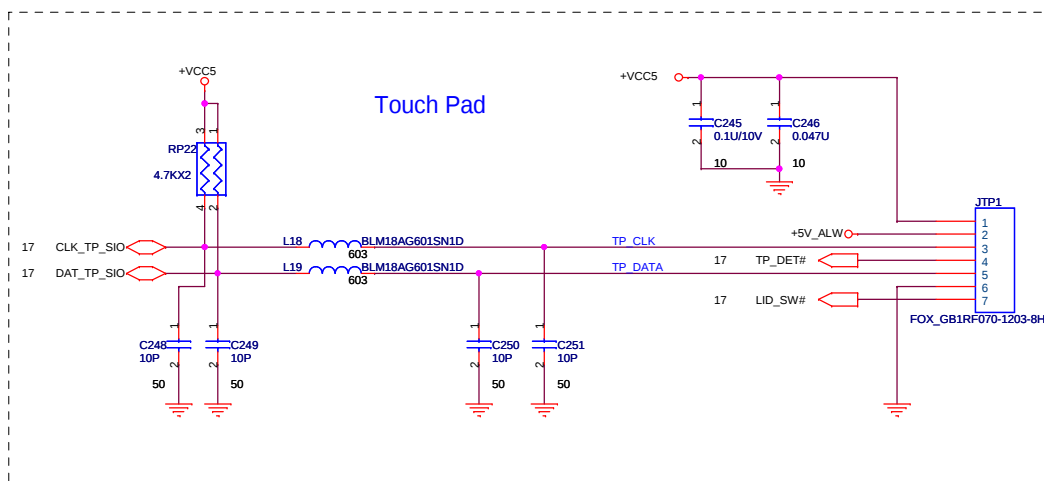
Title		
MINI-WWAN		
Size	Document Number	Rev
ZM2		D
Date:	Wednesday, March 10, 2010	Sheet 21 of 43

SATA HDD Connector.



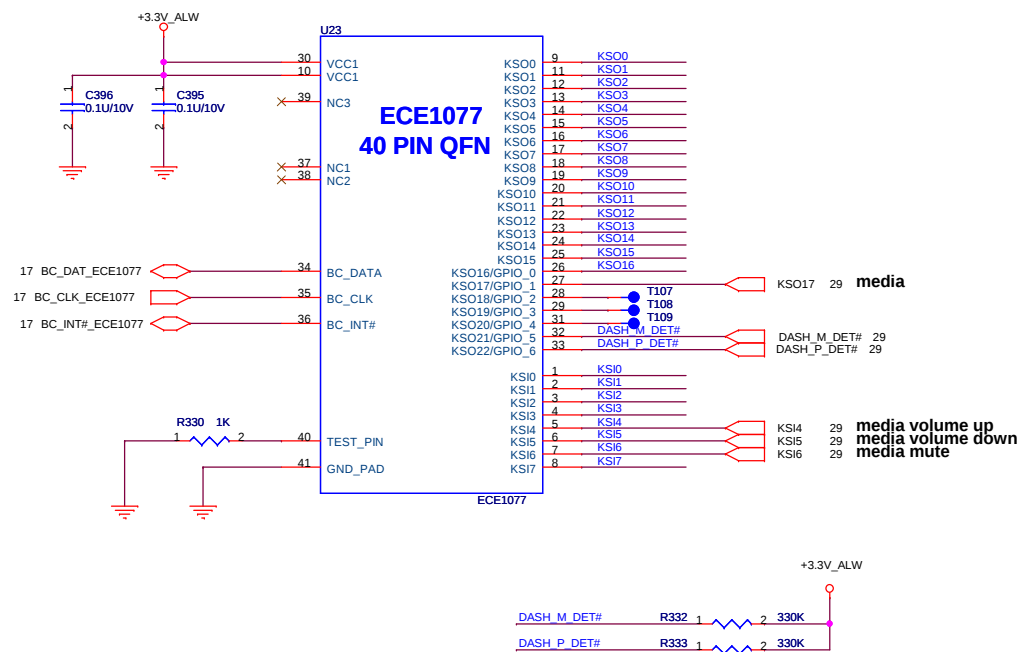
3-axis Fall Sensor (HDD data protector)



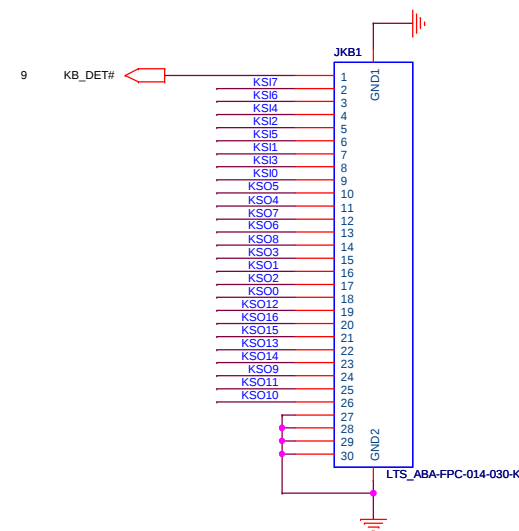


100P CAPS CLOSE TO JKB1

Keyboard Scan Extension



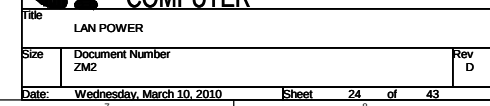
KEYBOARD CONNECTOR

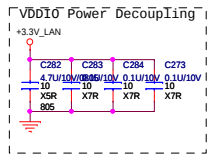
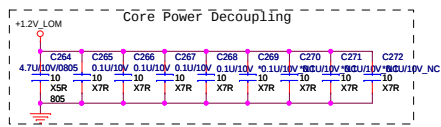


[illegible]

The schematic diagram illustrates the WLAN power supply circuit. It includes the following components and connections:

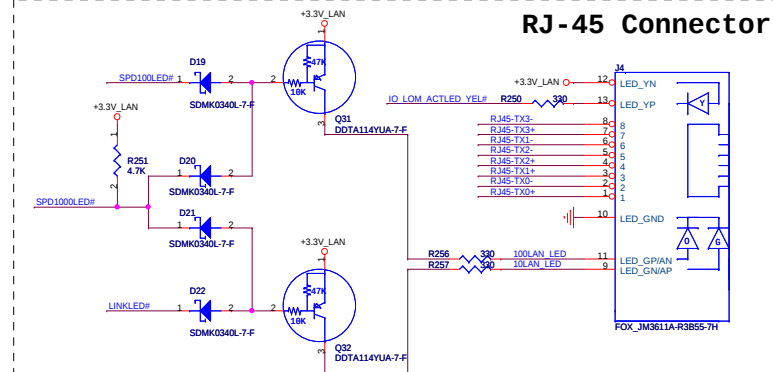
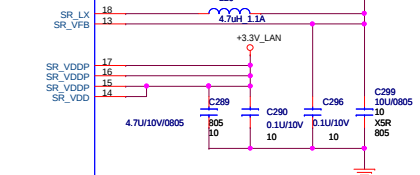
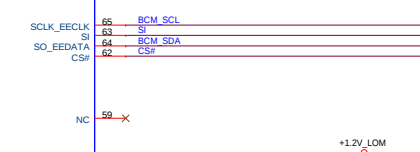
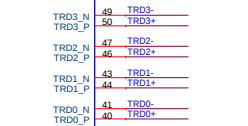
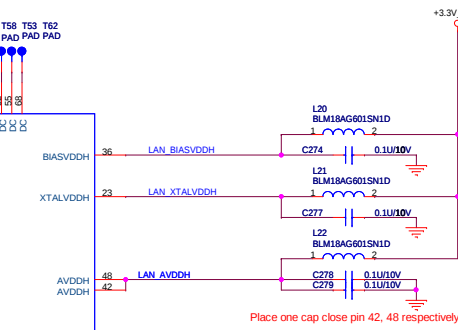
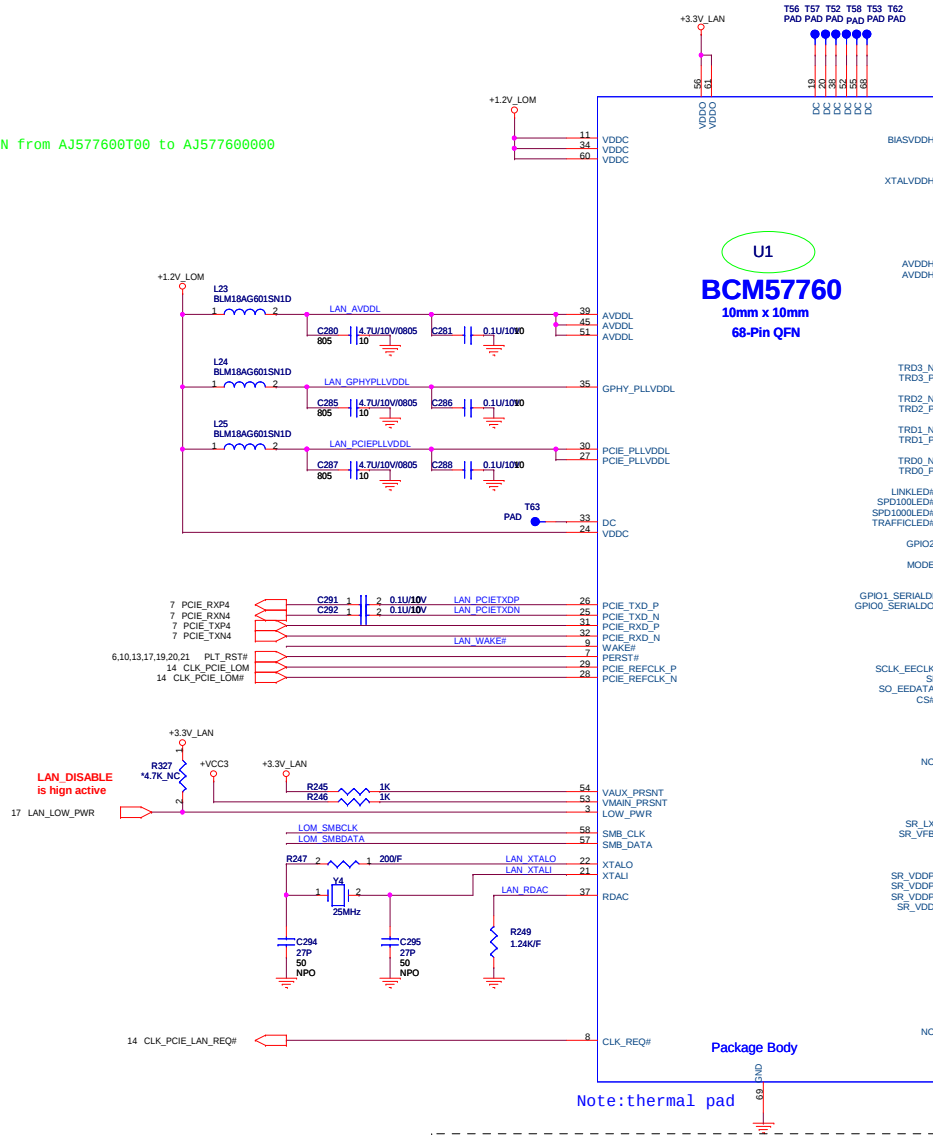
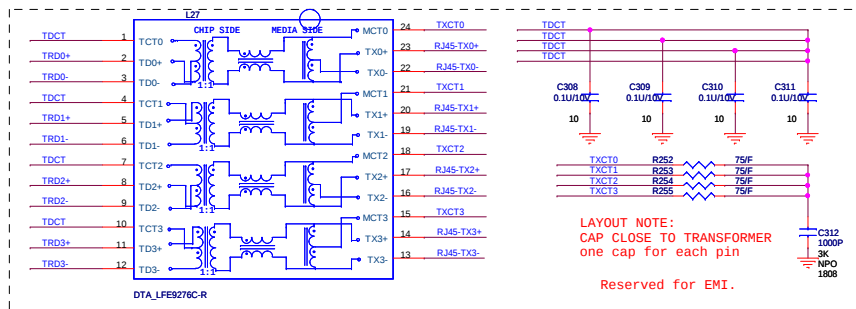
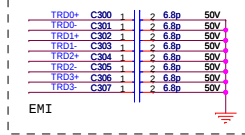
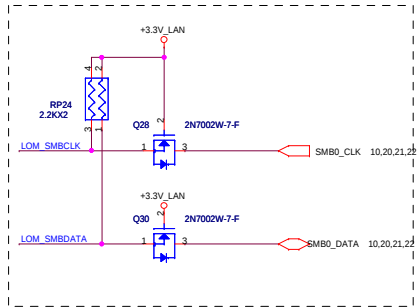
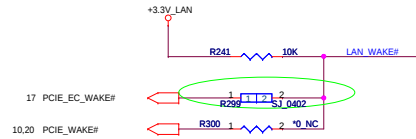
- Inputs:**
 - `+3.3V_ALW`: Input for the 3.3V WLAN supply.
 - `+15V_ALW`: Input for the 15V WLAN supply.
 - `17 AUX_EN_WOWL#`: Input for the WLAN enable signal.
- Transistors:**
 - Q73 (FDC655BN)**: A MOSFET used for the 3.3V WLAN output. Its gate is connected to the `+3.3V_ALW` input through a capacitor **C446** (0.1u/10V). The drain is connected to the `+3.3V WLAN` output, and the source is connected to ground.
 - Q72 (2N7002W-7-E)**: A MOSFET used for the 15V WLAN output. Its gate is connected to the `17 AUX_EN_WOWL#` input through a capacitor **C447** (4700P). The drain is connected to the `+15V_ALW` input through a resistor **R392** (100K). The source is connected to ground.
- Capacitors:**
 - C446** (0.1u/10V): Capacitor connected to the gate of Q73.
 - C447** (4700P): Capacitor connected to the gate of Q72.
 - C448** (0.1u/10V): Capacitor connected to the drain of Q73.
 - C449** (10u/0805): Capacitor connected to the drain of Q73.
- Resistors:**
 - R392** (100K): Resistor connected to the gate of Q72.
 - R236**: Resistor connected to the `+3.3V WLAN` output.
- Outputs:**
 - `+3.3V WLAN`: Output of the 3.3V WLAN supply.
 - `+VCC3`: Output of the 3.3V supply.
 - `*0/0805_NC`: A no-connection point for a 0805 component.



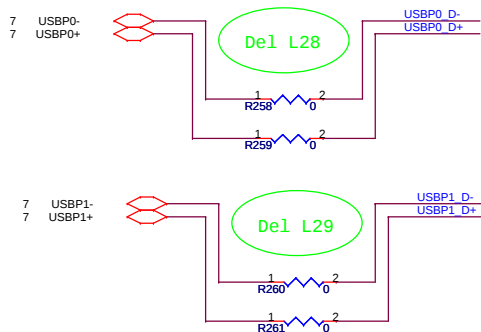


03/01 change U1 P/N from AJ577600T00 to AJ577600000

support WOL from S5.



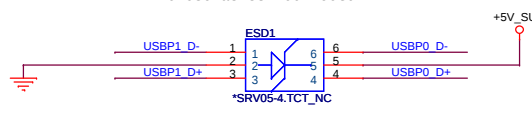
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



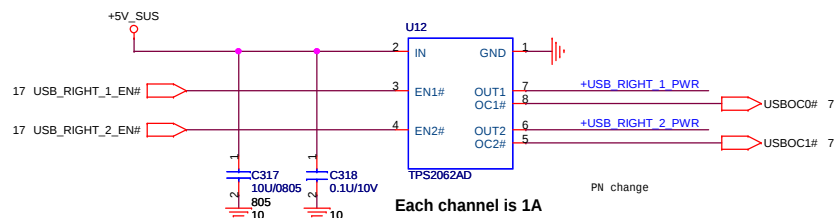
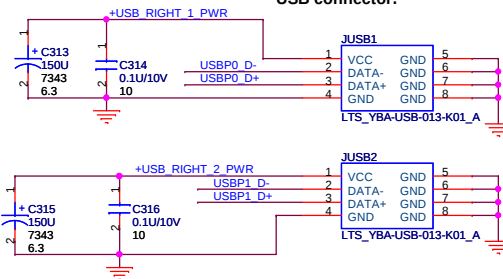
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

USB Right Side x2

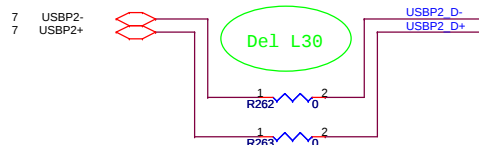
Place ESD diodes as close as USB connector.



Place one 150uF cap by each USB connector.

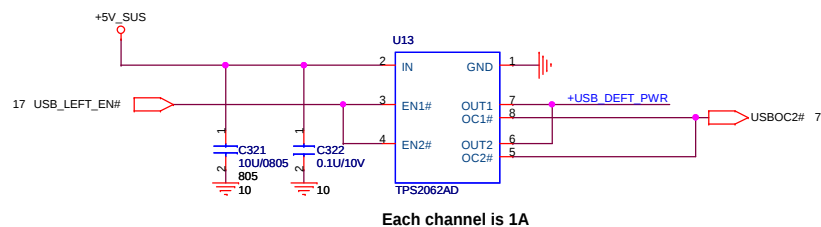
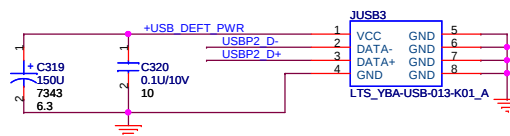
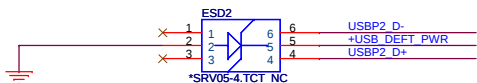


USB Left Side

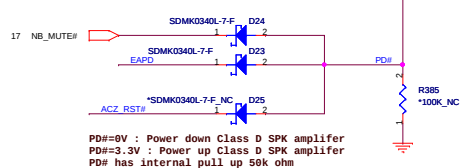
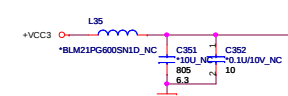
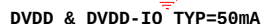
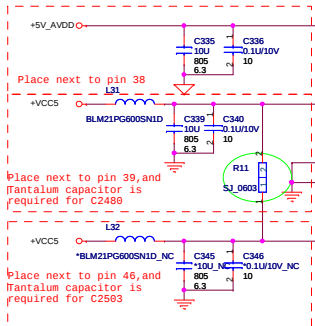


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

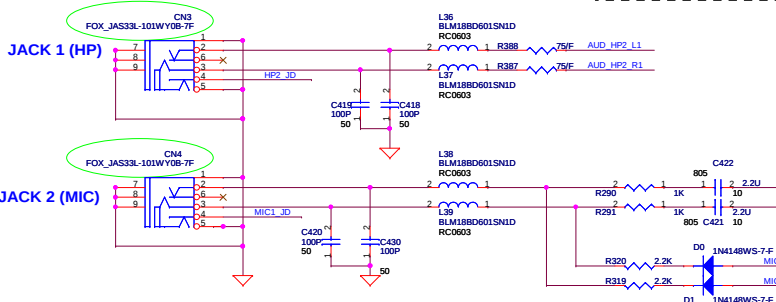
Place ESD diodes as close as USB connector.



```
03/01 Change CN3,CN4 Footprint from audio-jas33l-101wy0x-7f-5p-h
to audio-jas33l-101wy0x-7f-5p-v
03/01 Add C433,C354(P/N:CH0126G0B00),
Addr407, R282(P/N:CS00002JB38)
```



<Attention>
For power_on/off de-pop circuit and system booting warning
signal: Please System BIOS Engineer Note :
1. If you want the system make warning signal after power on
, please let EC_MUTE# High first.
2. When you want to exit your Bios Programming Code, please let
the EC_MUTE# Low. (The programming is different from before.)



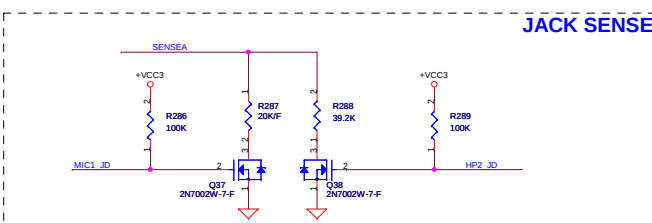
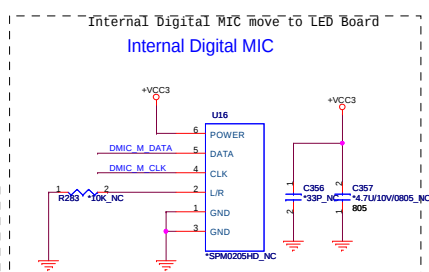
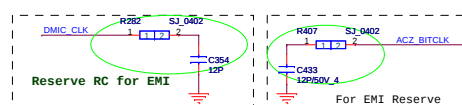
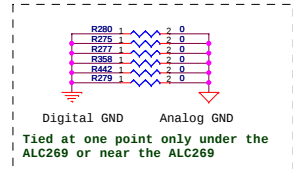
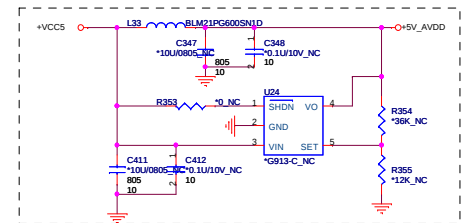
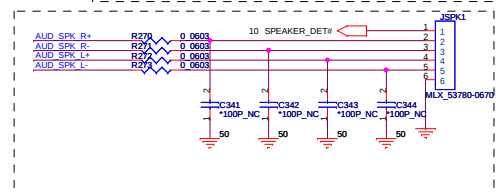
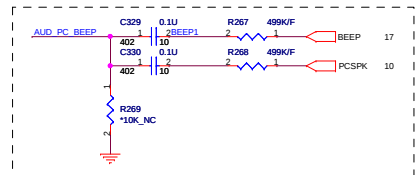
NOTE: ALC269_VB type add the LDO circuit in I

PIN NAME	R425	R375	R369	C417	CODEC IC
28 MIC1_VREF0-L			POP	NC	ALC269
31 CPVREF	POP	NC			VA

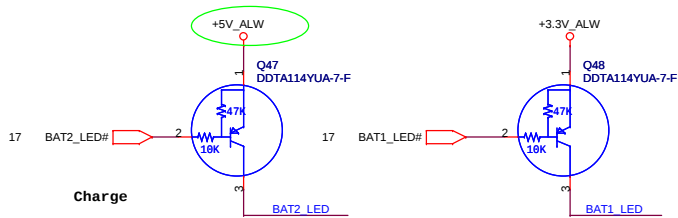
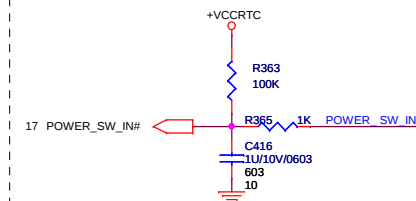
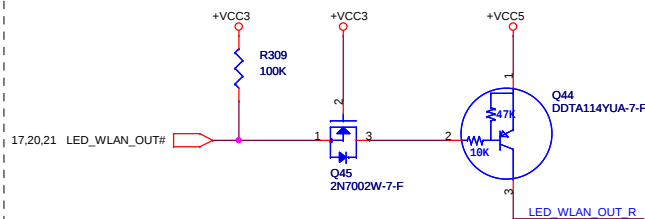
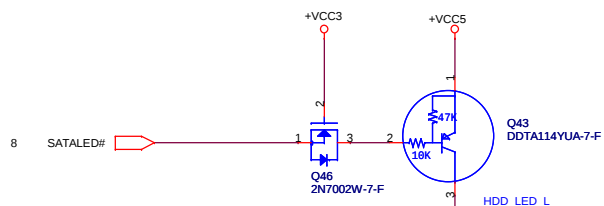
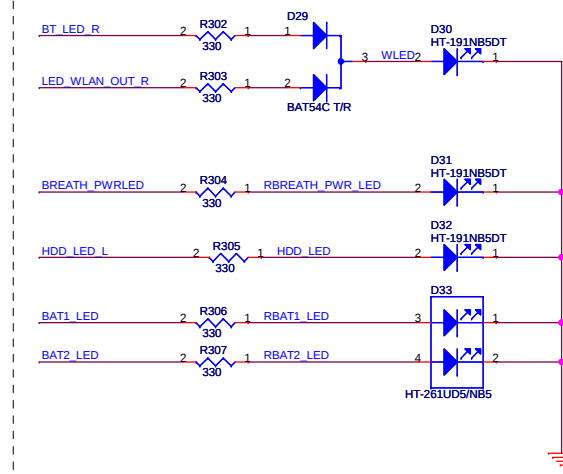
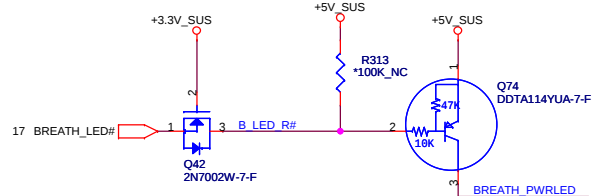
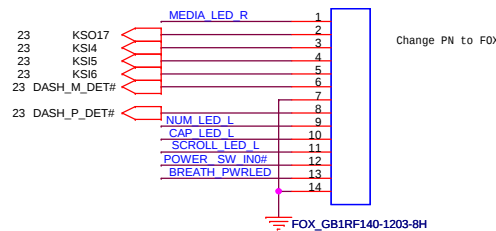
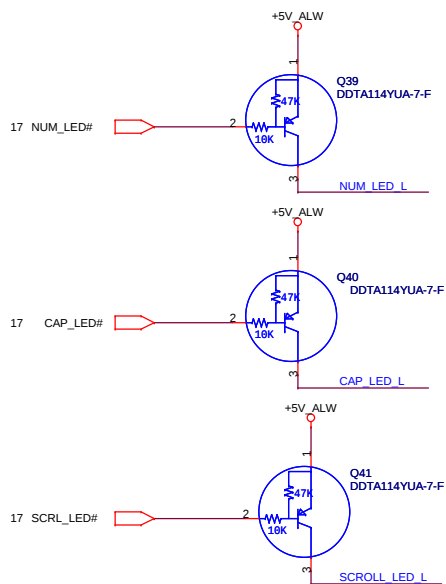
PIN NAME	R425	R375	R369	C417	CODEC IC
28 MIC1_VREF0-L			NC	POP	ALC269
31 CPVREF	NC	POP			VB

VA type: PIN28 as Bias Voltage for MIC1 Jack
PIN31 connect to analog ground

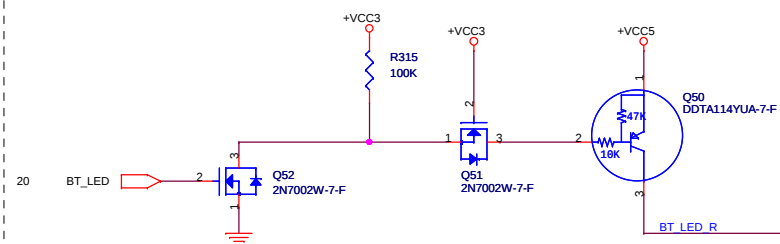
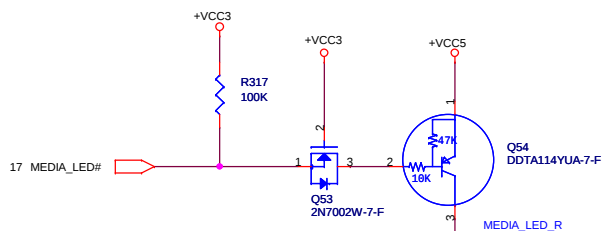
VB type: PIN31 as Bias Voltage for MIC1 Jack
PIN28 connect capacitor to analog ground



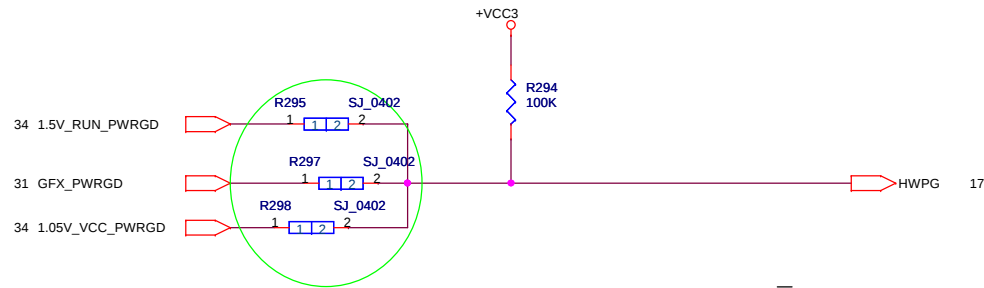
Title		CODEC	
Size	Document Number	Rev	
	ZM2	D	
Date:	Wednesday, March 10, 2010	Sheet	28 of 43



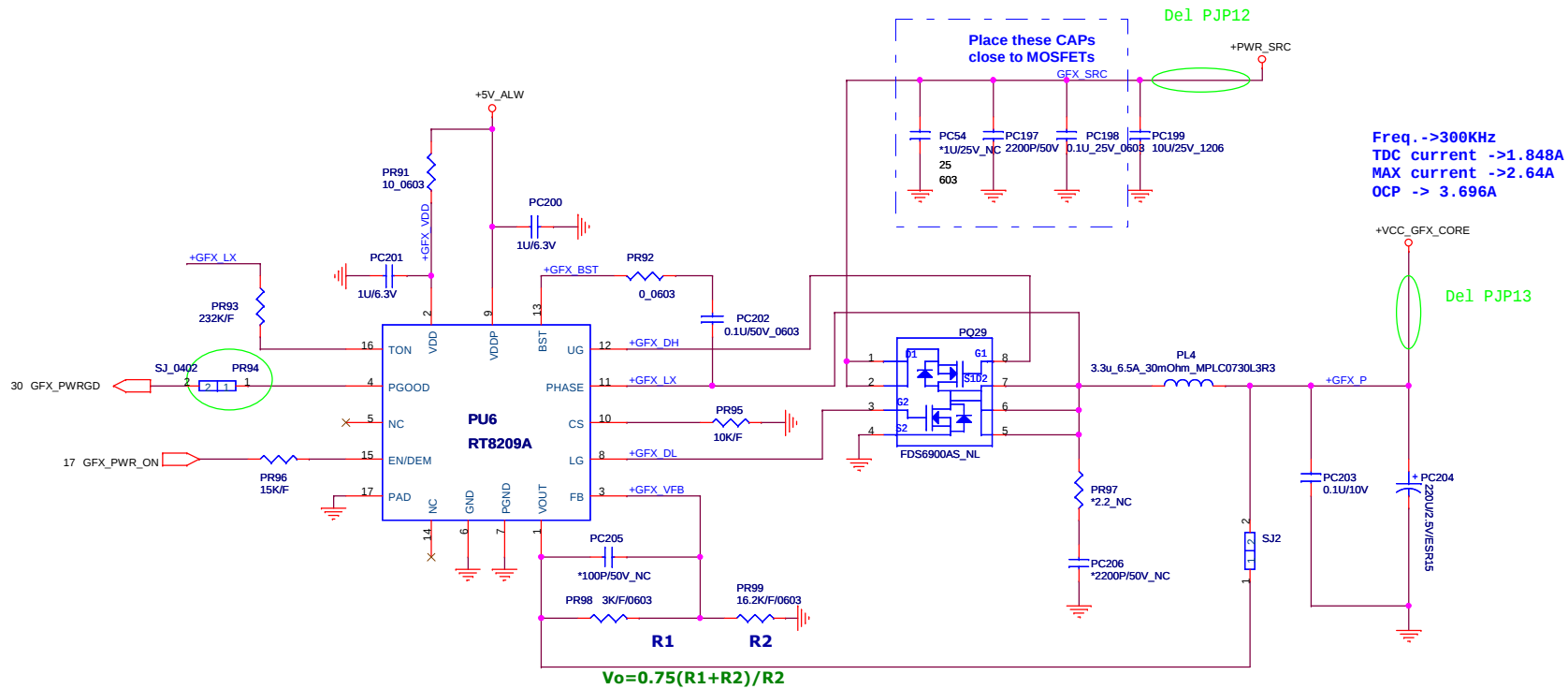
03/01 Change Q47 pin1 Power rail from +3.3V_ALW to +5V_ALW

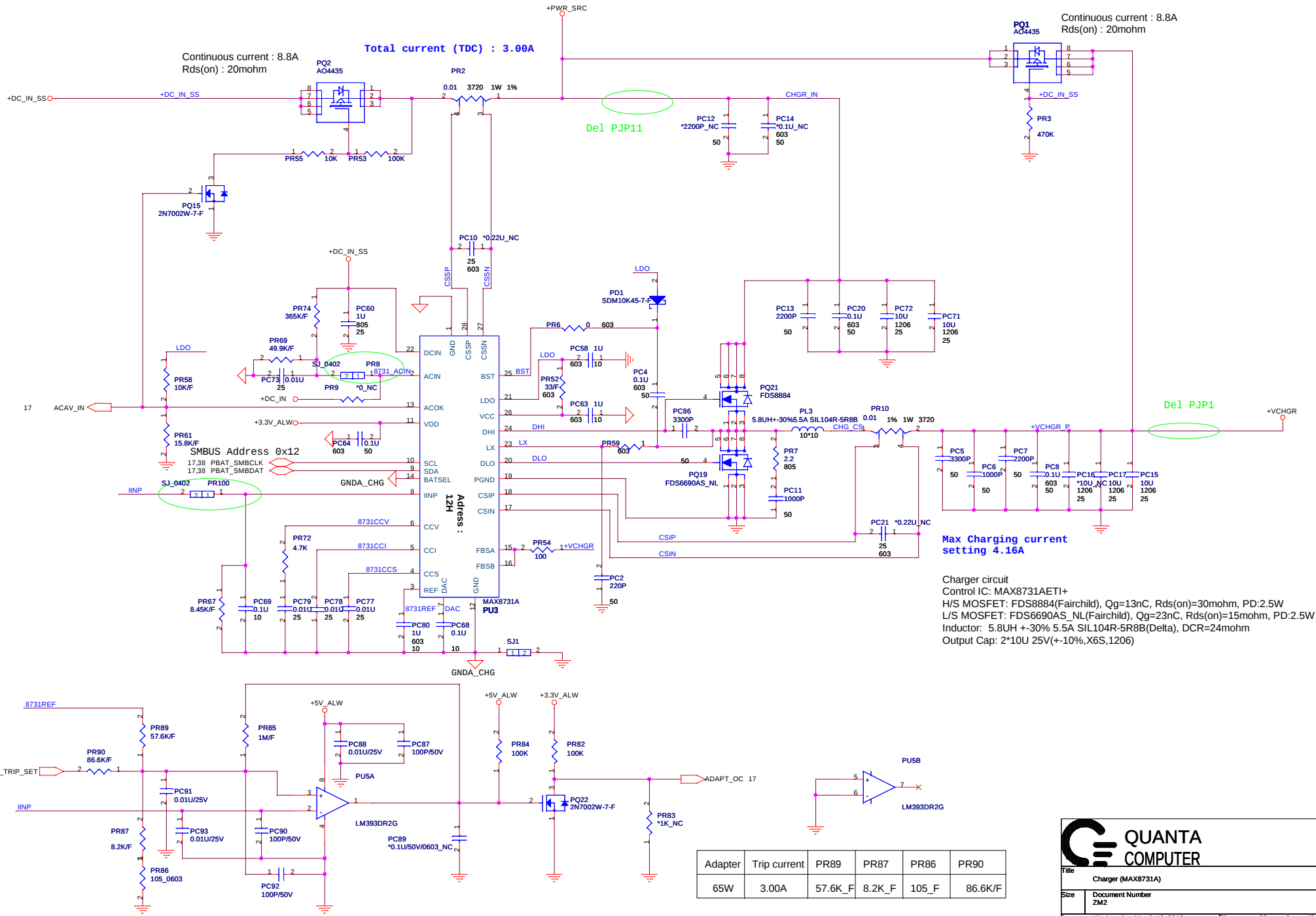


Title		
LED & SWITCH		
Size	Document Number	Rev
ZM2		D
Date:	Wednesday, March 10, 2010	Sheet 29 of 43



 QUANTA COMPUTER			
Title System Reset Circuit			
Size	Document Number		Rev
	ZM2		D
Date:	Wednesday, March 10, 2010	Sheet	30 of 43

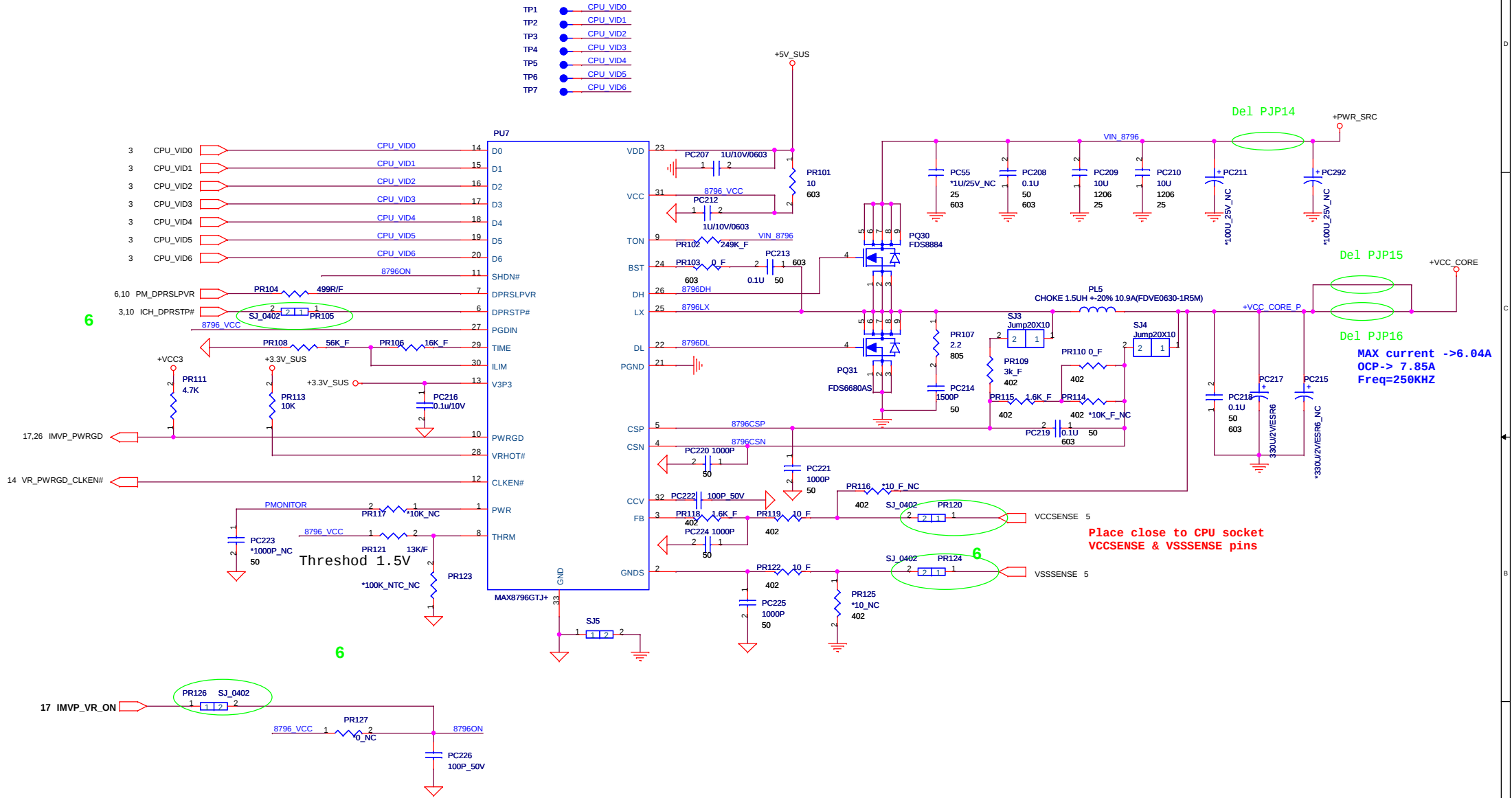




Charger (MAX8731A)

Size	Document Number	Rev
ZM2		D

CPU Vcore power rail:
Control IC: MAX8796GTJ+
H/S MOSFET: AO4496, Qg=6.1nC, Rds(on)=26mohm, PD:3.1W
L/S MOSFET: AO4712, Qg=12nC, Rds(on)=18mohm, PD:3.1W
Inductor: 3.3uH +-20% 13.5A(MPLC0730L3R3)DCR=30mohm
Output Cap: 1*330U 2V(+10/-35%,7343,ESR=6)



1.8V_SUS power rail:
Control IC: RT8207AGQW
H/S MOSFET:AO4476, Qg=8.5nC, Rds(on)=17mohm, PD:3.7W
L/S MOSFET: AO4710, Qg=15nC, Rds(on)=14.2mohm, PD:3.1W
Inductor: 1.5UH +-30%12.5A(SIL1055RC-1R5-R)(Delta), DCR=7.6mohm
Output Cap: 1* 330U2.5V(20%,ESR9,7343,H1.9)

VDDQ and VTT discharge control

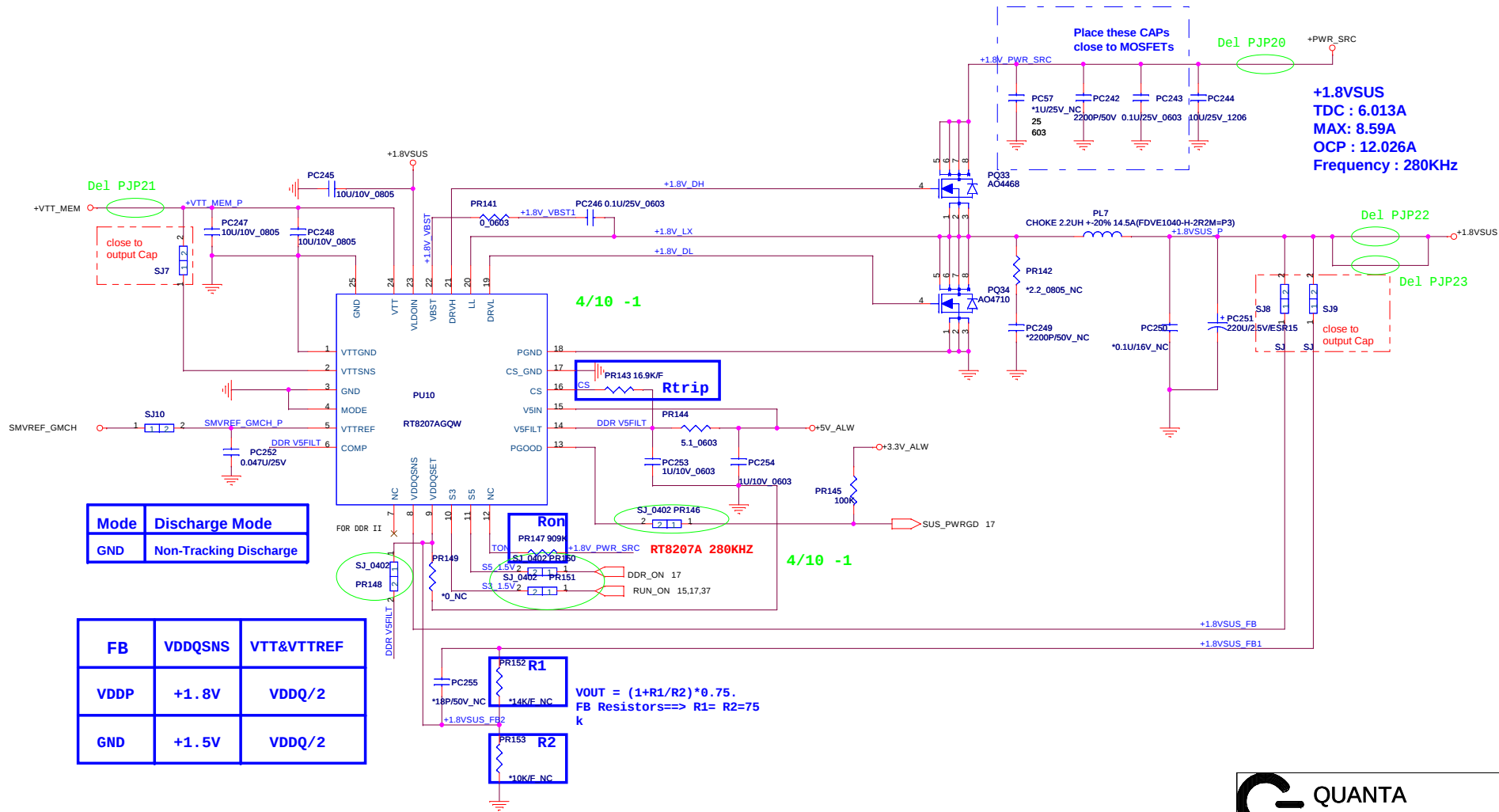
MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

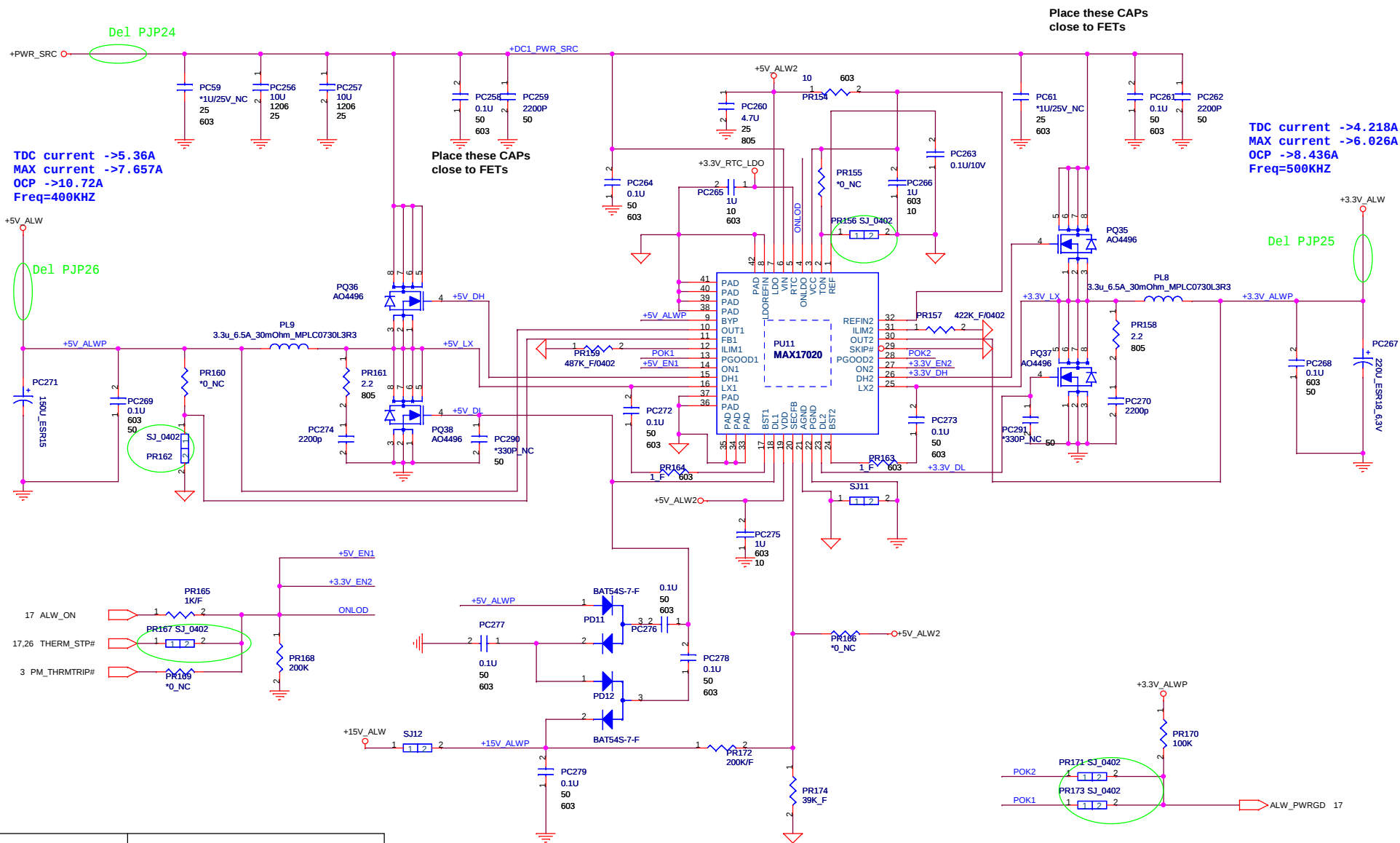
VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	L0	HI	On	On	Off (Hi-Z)
S4/S5	L0	L0	On (discharge)	Off (discharge)	Off (discharge)



3.3V_ALW power rail:
Control IC: RT82064
H/S MOSFET: AO4496, Qg=6.1nC, Rds(on)=26mohm, PD:3.1W
L/S MOSFET: AO4496, Qg=6.1nC, Rds(on)=26mohm, PD:3.1W
Inductor: 3.8UH 30% 6A(SIL104R-3R8B)(Delta), DCR=13mohm
Output Cap: 1* 330U 6.3V(20%ESR)7.63*5.8



Switching regulator	TON setting
SMPS1	200KHZ (TON=VCC)
	400KHZ (TON=REF or GND)
SMPS2	300KHZ (TON=REF or VCC)
	500KHZ (TON=GND)



Title	5V_ALW, 3V_ALW, 15V_ALW
-------	-------------------------

Size

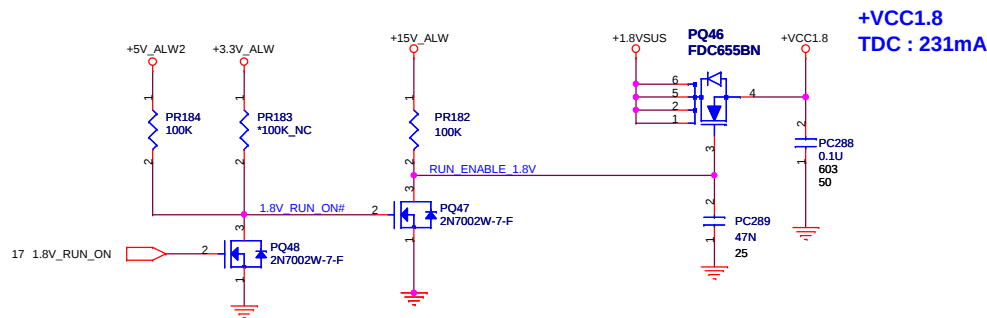
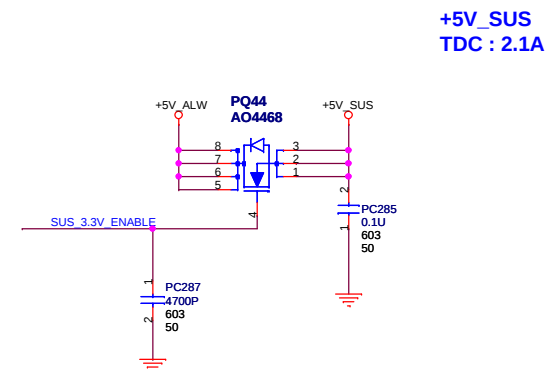
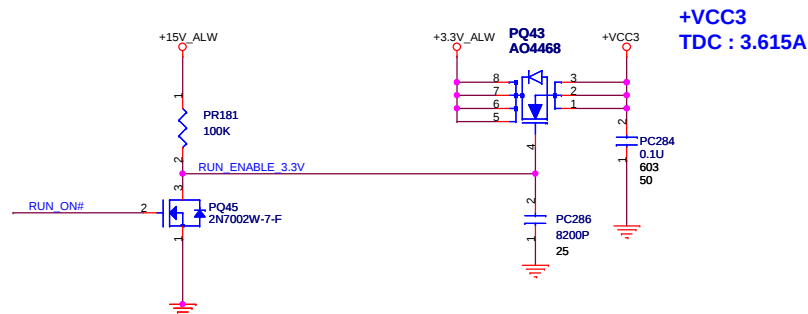
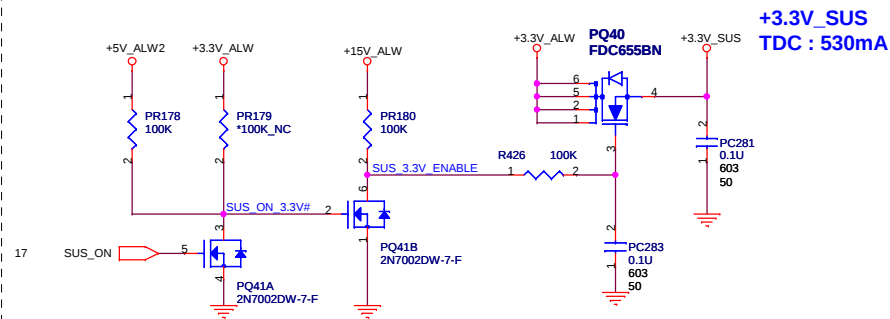
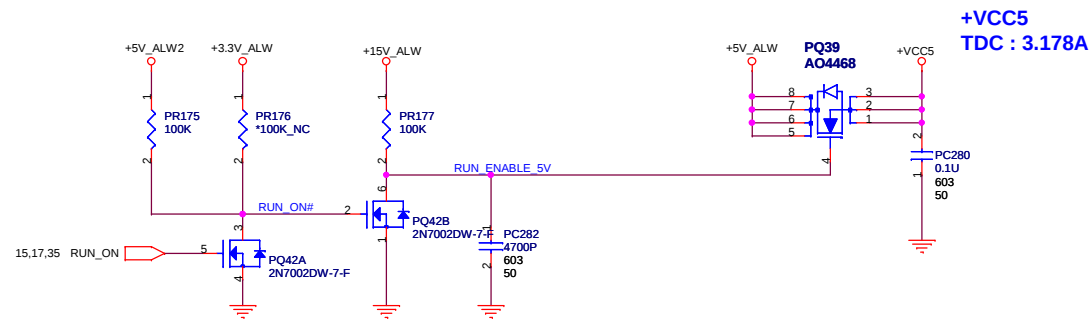
Document Number	
-----------------	--

1

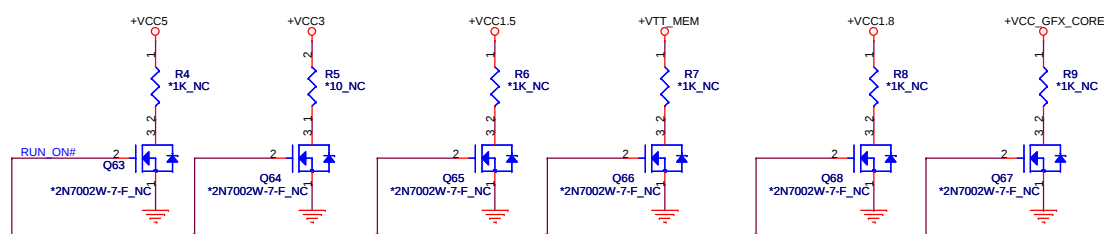
ZM2

Date: Wednesday, March 10, 2010

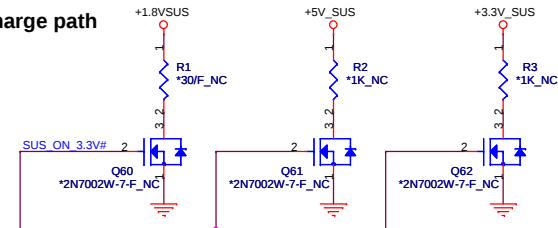
Sheet 36 of 43



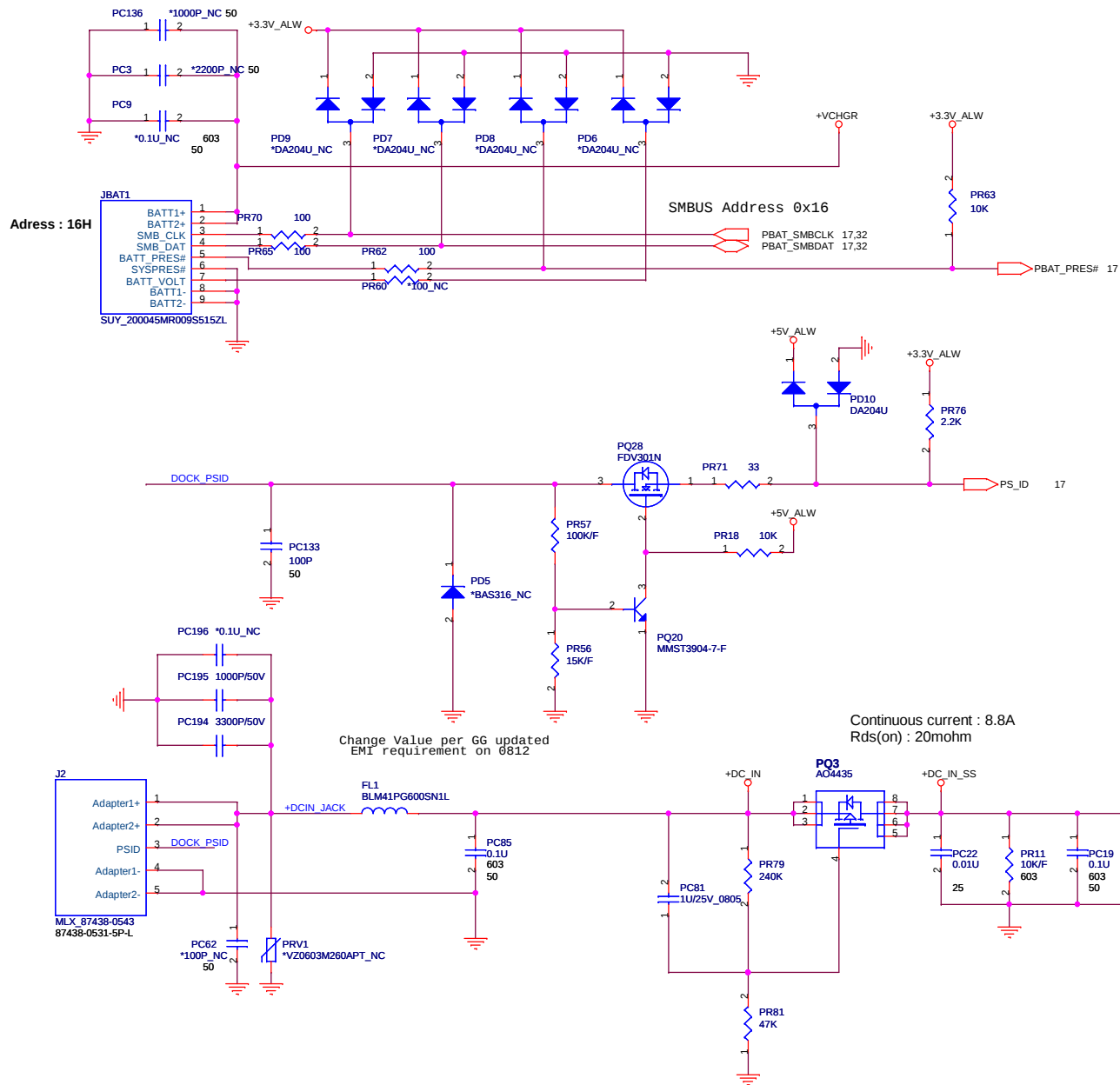
Reserve discharge path



Reserve discharge path



Title			RUN POWER SW
Size	Document Number	Rev	
ZM2		D	
Date:	Wednesday, March 10, 2010	Sheet	37 of 43



Title
DCIN,BATT CONNECTOR

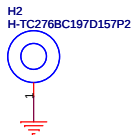
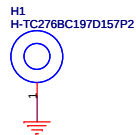
Size
Document Number
ZM2

Rev
D

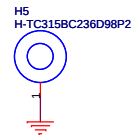
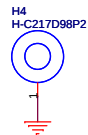
Date: Wednesday, March 10, 2010

Sheet 38 of 43

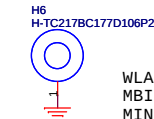
H - TC276BC197D157P2



H - TC315BC236D126P2

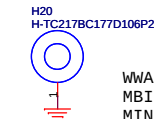


H - TC217BC177D106P2



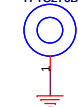
WLAN USE
MBIM3001010
MINI CARD NUT H16 IM3(MBIM3001, REV3A)CU

H - TC217BC177D106P2

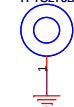


WWAN USE
MBIM3001010
MINI CARD NUT H16 IM3(MBIM3001, REV3A)CU

H7 H-TC276BC197D169P2



H8 H-TC276BC197D157P2



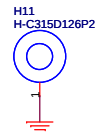
H9 H-TC315BC236D39P2



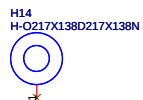
H10 H-TC315BC236D98P2



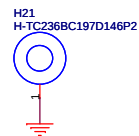
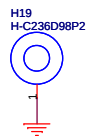
H - C315D126P2



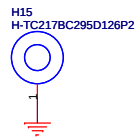
H - C157D157N



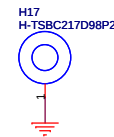
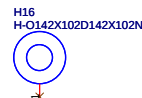
H - C236D98P2



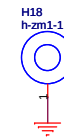
h-tc217bc197d126p2



h-c118d118n

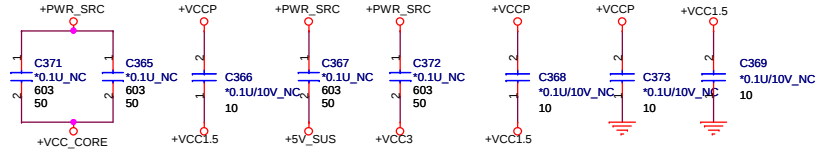
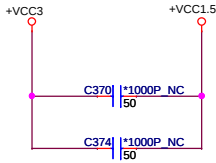


h-zm1-1

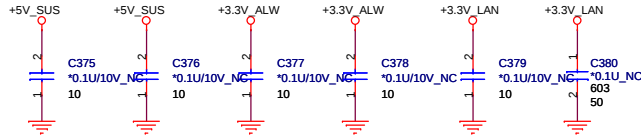
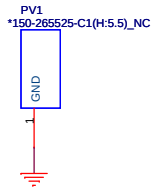
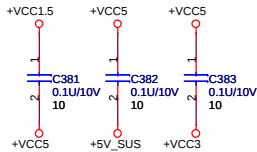


Reserved for EMI.

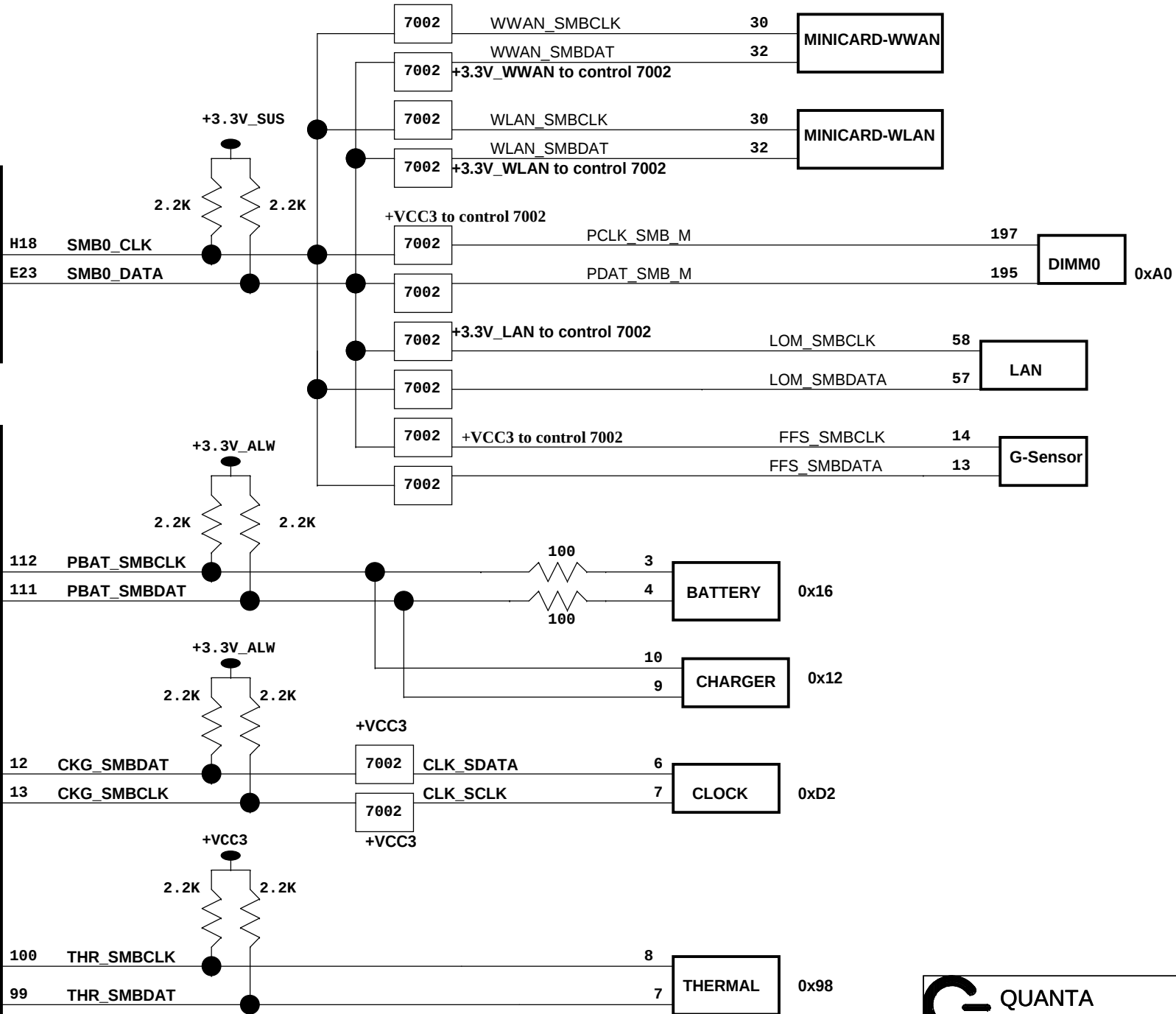
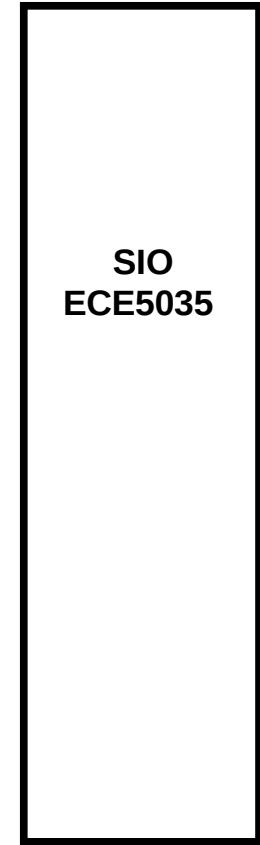
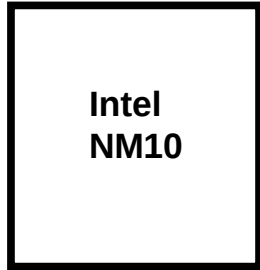
Stitching caps.



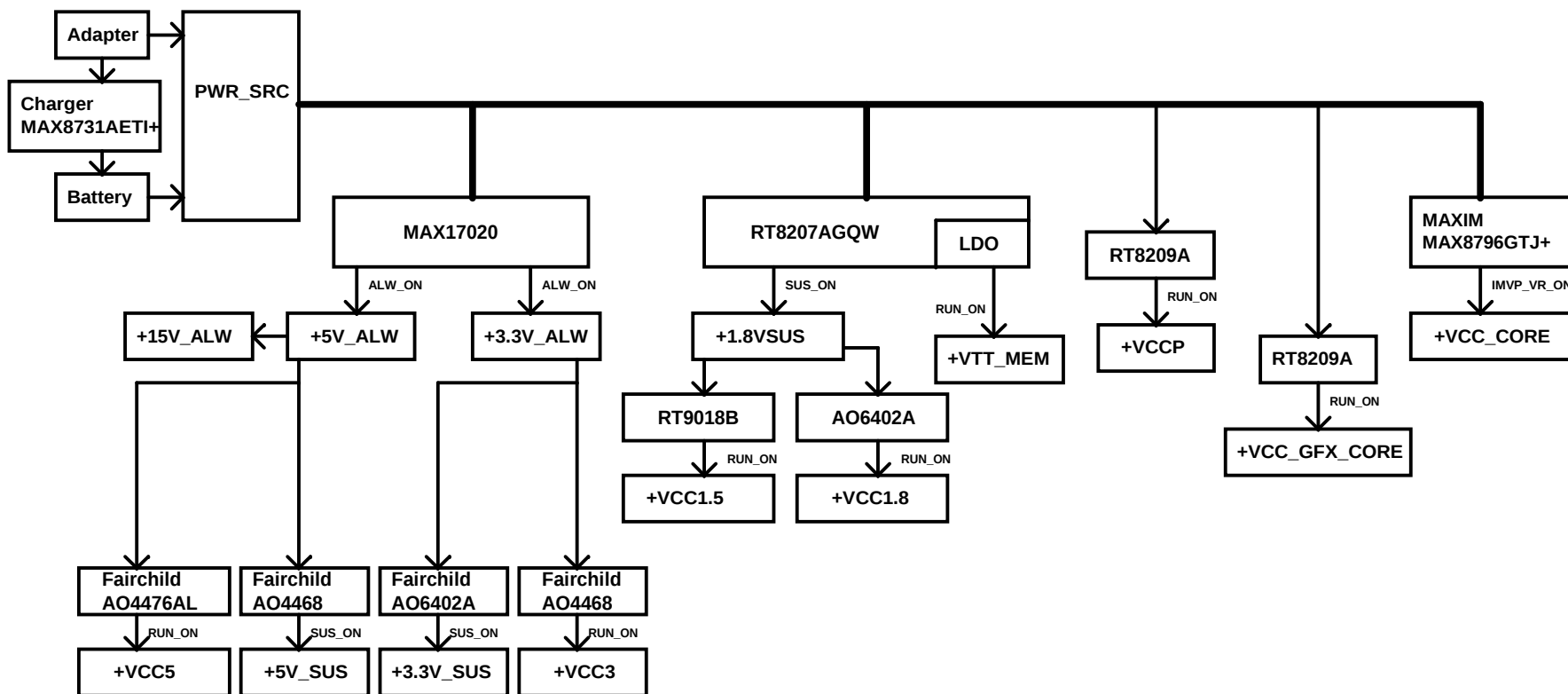
Stitching caps for PCI bus.



Add cap near LAN



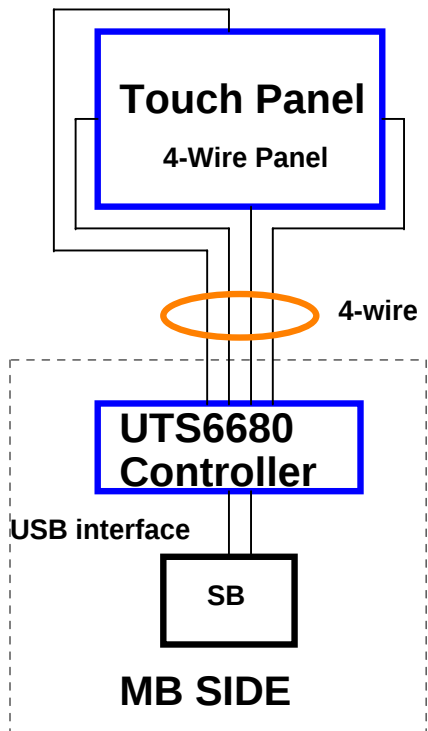
VER : 1A



USB Port#	Destination
USBP0	Right side top
USBP1	Right side bottom
USBP2	Left side
USBP3	Bluetooth
USBP4	Camera
USBP5	Touch Screen
USBP6	Mini WLAN
USBP7	Mini WWAN

PCI-E	Destination
PCIE-1	Mini WWAN
PCIE-2	Mini WLAN
PCIE-3	Card reader
PCIE-4	LAN

SATA	Device
SATA0	SATA/SSD HDD
SATA1	NC



AL006680B00IC OTHER(32P) UTS6680EF(LQFP)



Title Port Mapping			
Size	Document Number ZM2		Rev D
Date:	Monday, March 01, 2010	Sheet	43 of 43

[illegible]

Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
ZM2	1	35	100125					Change PL7 P/N from DC-2282M000 to CV-22E5MZ00 Change PL7 footprint from CHOKE-MPLC0730L3R3 to CHOKE-MP0104-1R5

QUANTA
COMPUTER

File

Change List

Size

Document Number

Date

Monday, March 01, 2010

Sheet

2 of 2

Rev

D