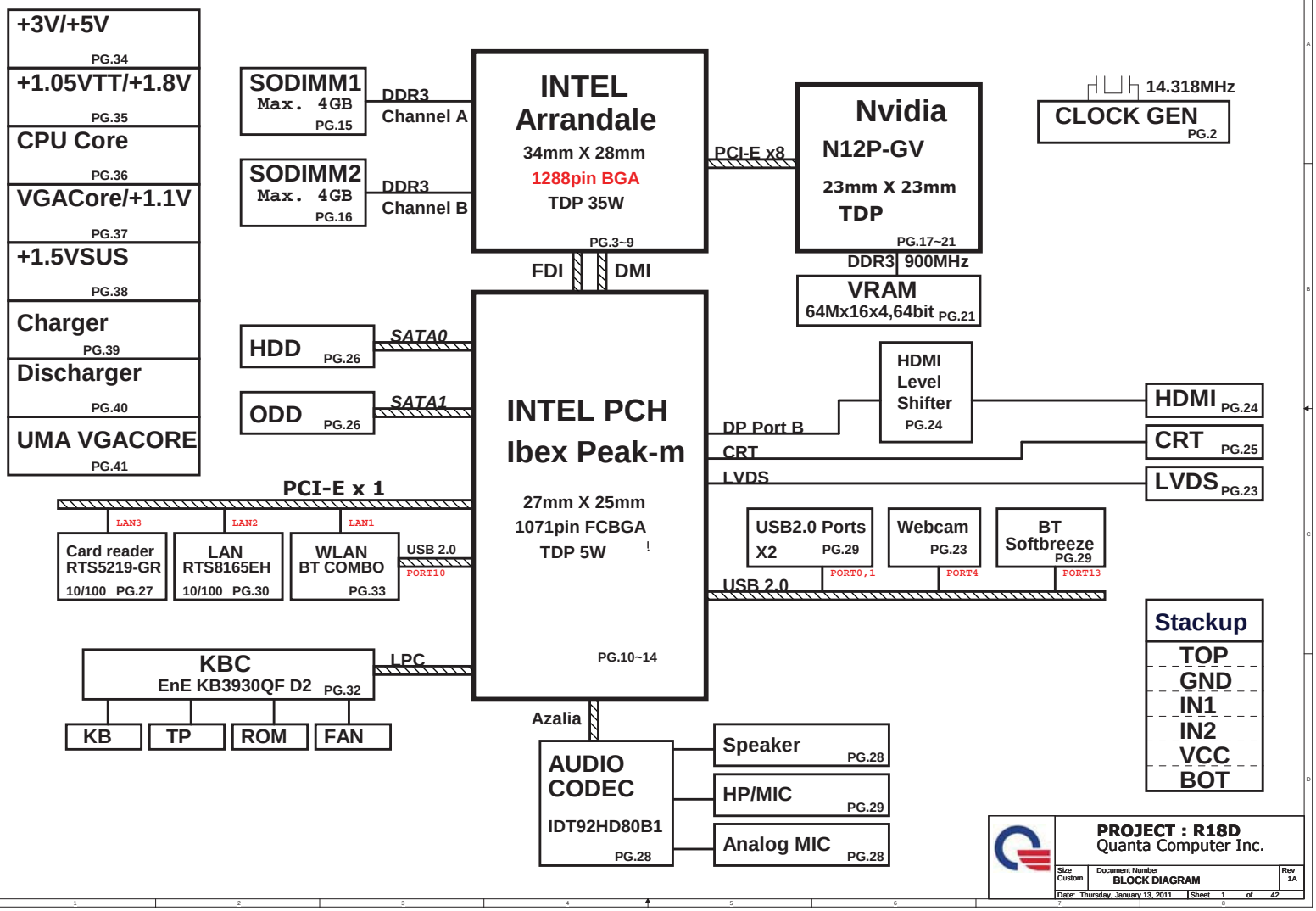
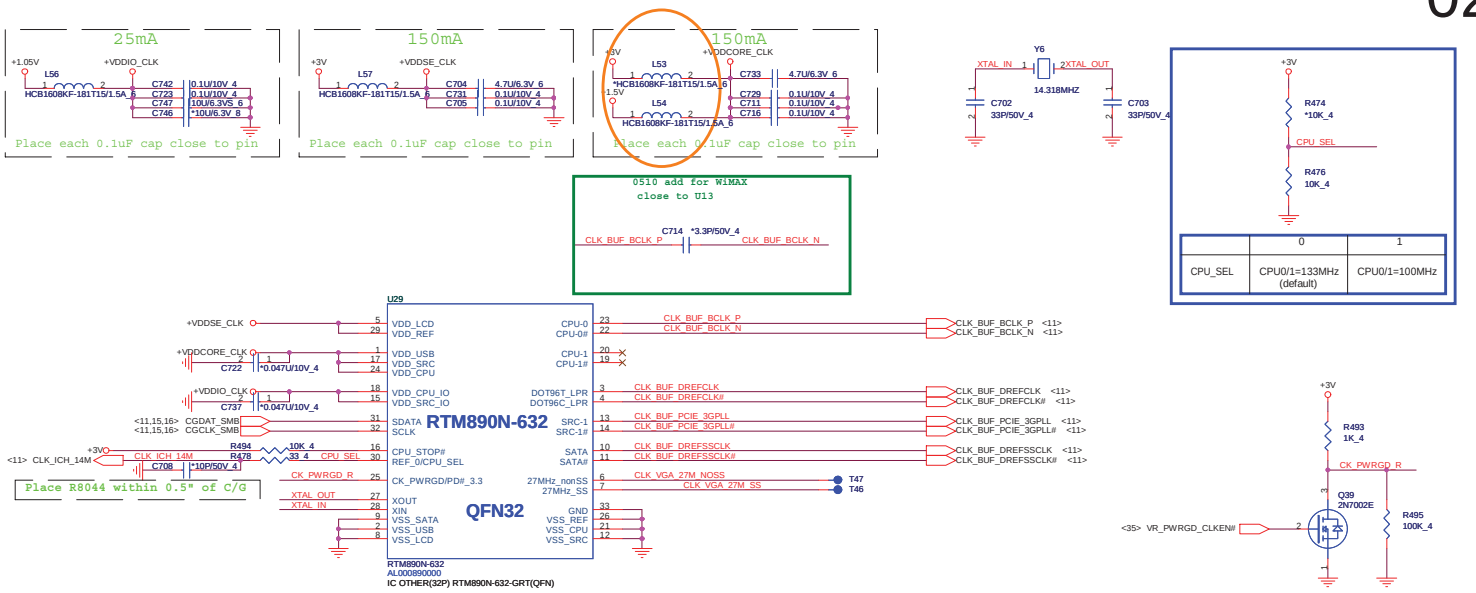
R18D INTEL UMA/DISCRETE SYSTEM DIAGRAM





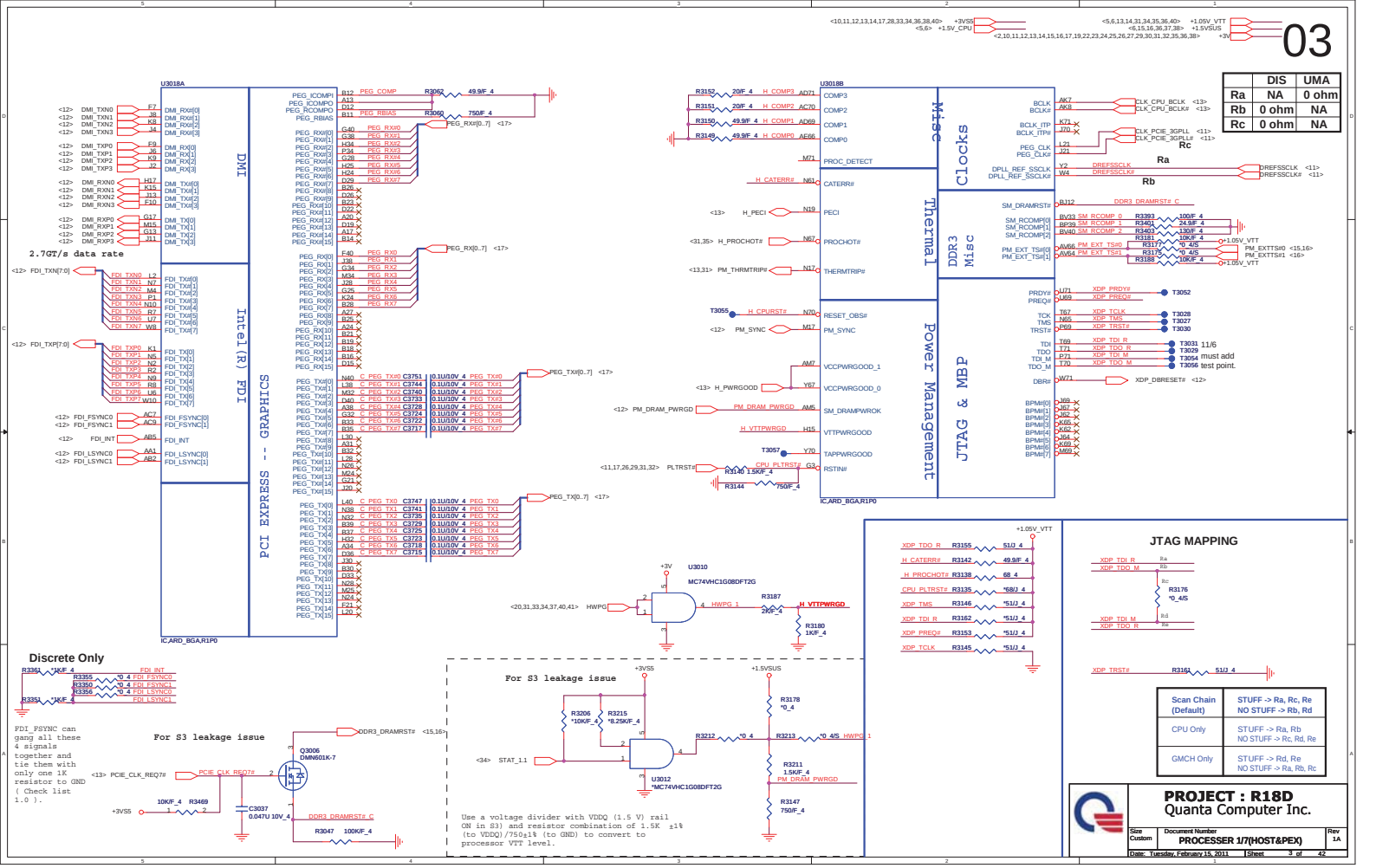
Vender	Part	Part Number	Part Description
ICS	ICS9LVS3197	AL003197001	IC OTHER(32P) ICS9LVS3197AKLFT(MLF)
Realtek	RTM890N-632	AL000890000	IC OTHER(32P) RTM890N-632-GRT(QFN)
Silego	SLG8LV595VTR	AL000595000	IC OTHER(32P)SLG8LV595VTR(QFN)

+1.05V <10,11,12,14,41>
+1.5V <6,32>
+3V <3,10,11,12,13,14,15,16,17,19,22,23,24,25,26,27,29,30,31,32,35,36,38>

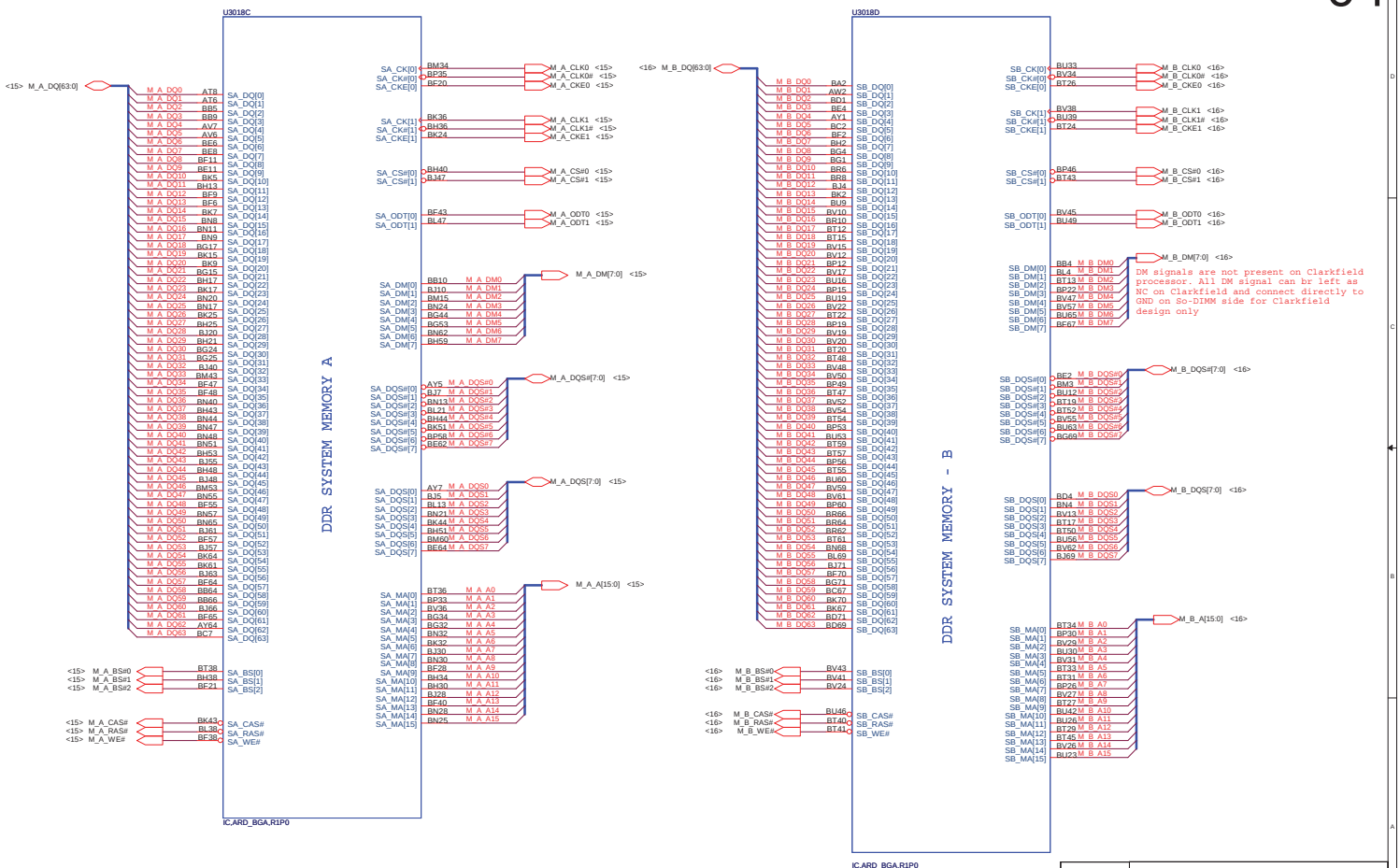
PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Clock Gen(9LRS3197)	1A

Date: Tuesday, February 15, 2011 Sheet 2 of 42



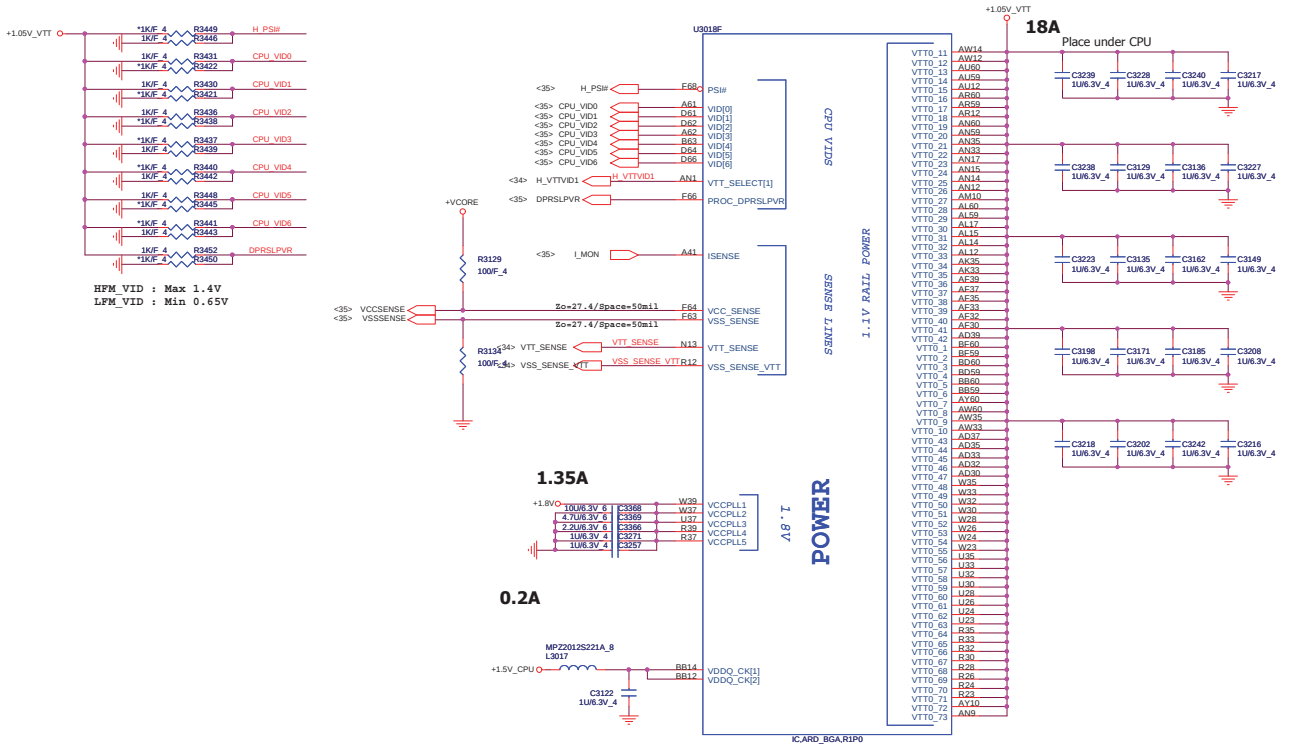
ARRANDALE/CLARKSFIELD PROCESSOR (DDR3)



PROJECT : R18D
Quanta Computer Inc.

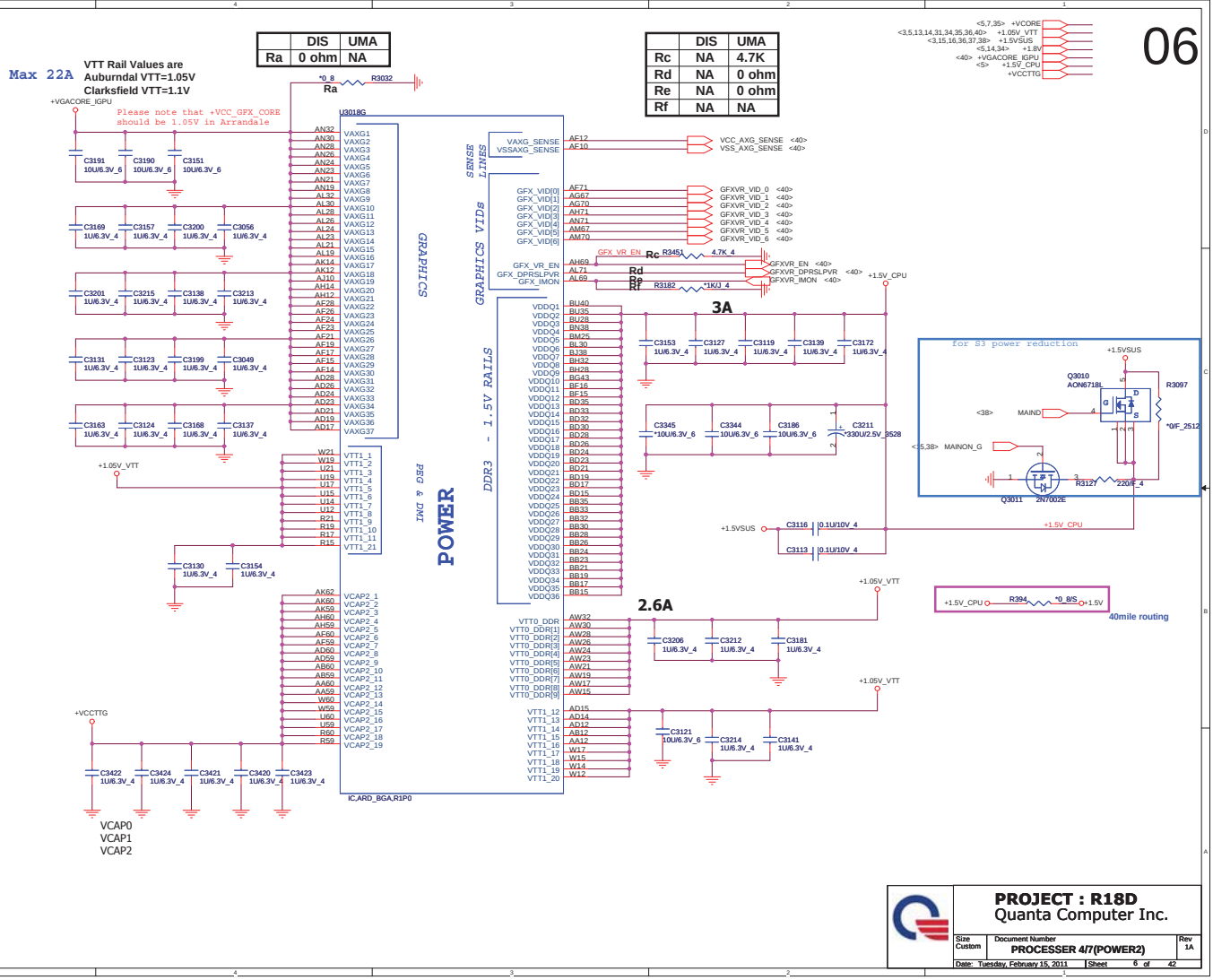
Size	Document Number	Rev
Custom	PROCESSER 2/7(DDR3)	1A

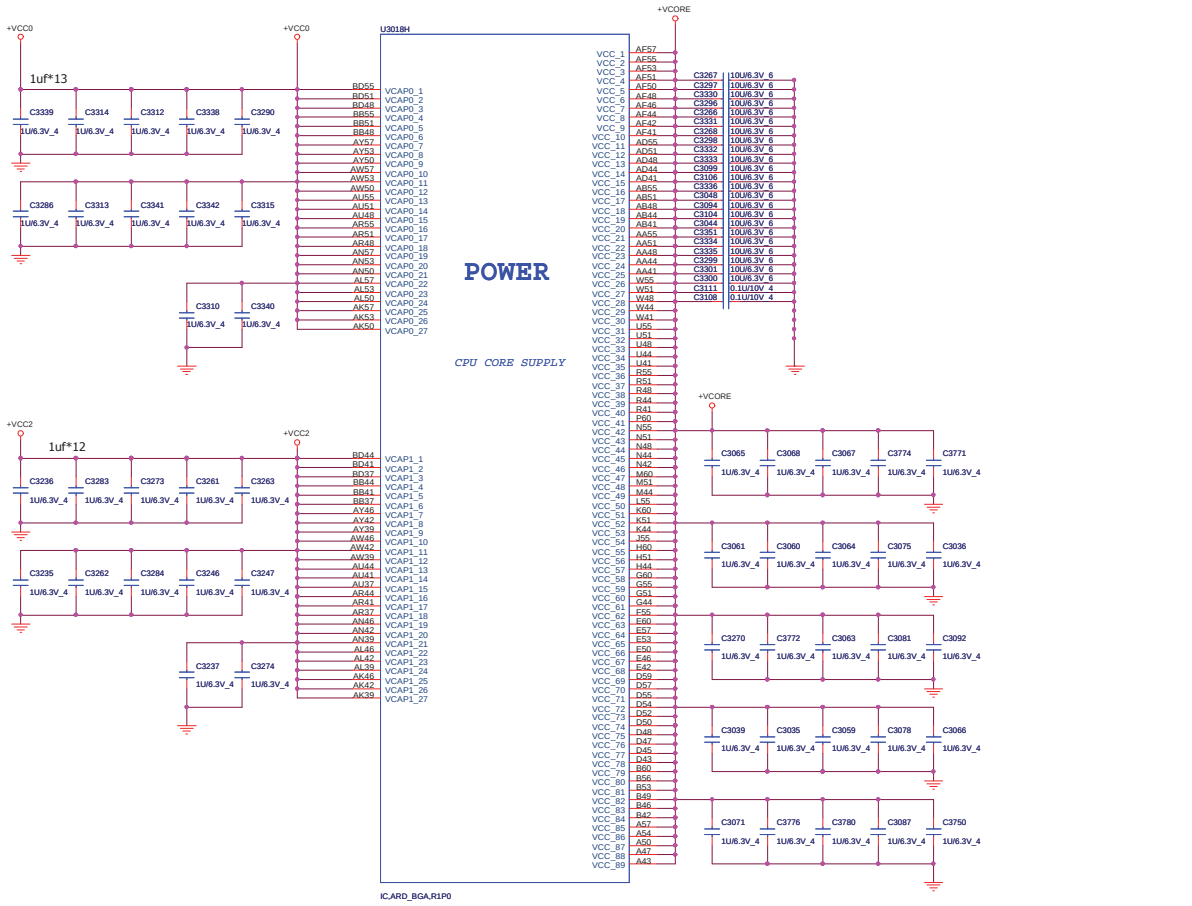
Date: Tuesday, February 15, 2011 | Sheet 4 of 42



Size: Custom	Document Number: PROCESSER 3/7(POWER1)	Rev: 1A
Date: Tuesday, February 15, 2011	Sheet 5 of 42	

PROJECT : R18D
Quanta Computer Inc.

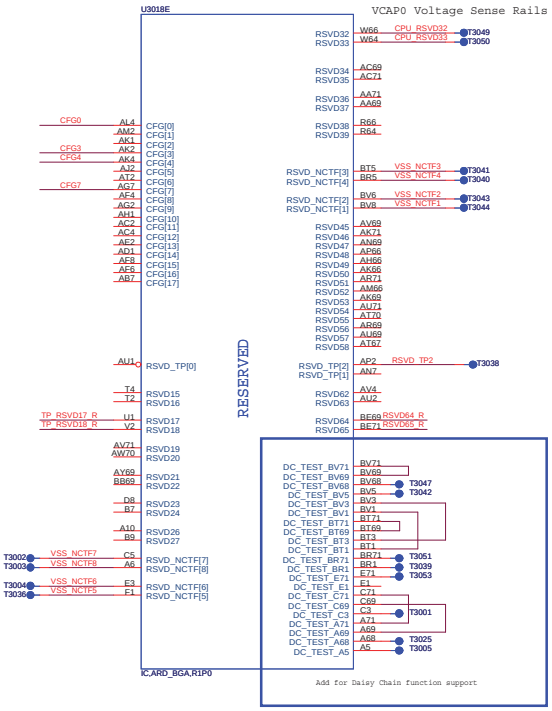


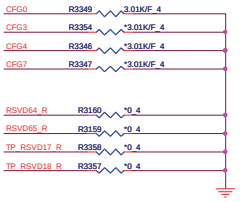


PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 5/7(POWER3)	1A

Date: Tuesday, February 15, 2011 | Sheet 7 of 42





CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

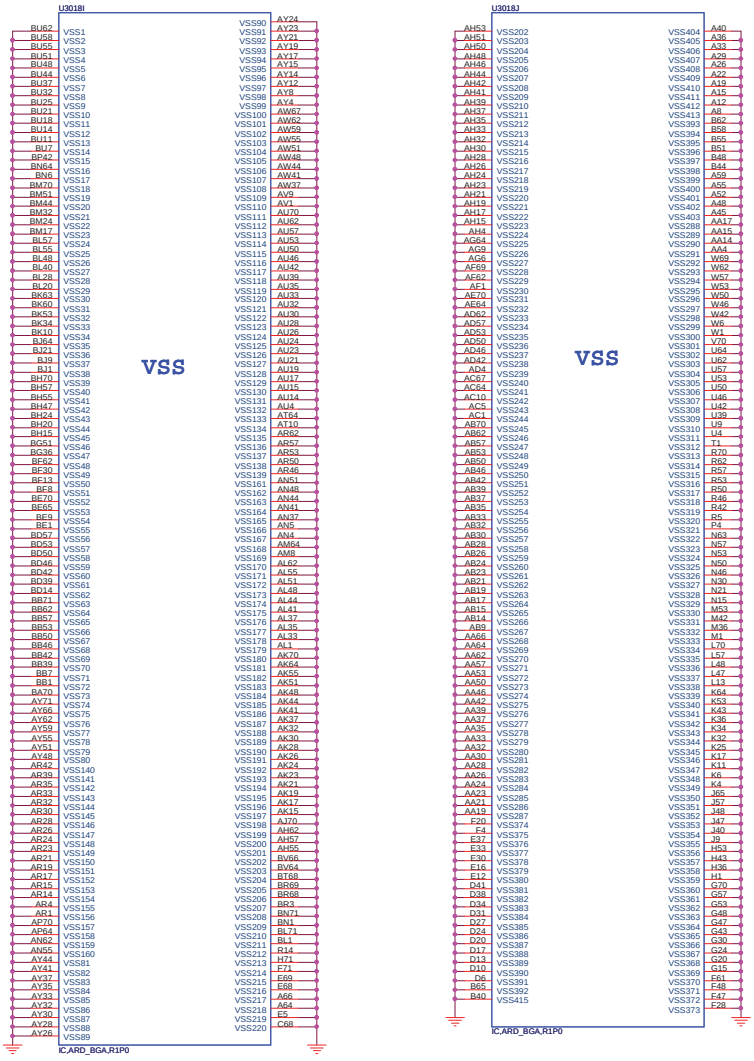
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 6/7(CFG)	1A

Date: Friday, January 14, 2011 | Sheet 8 of 42

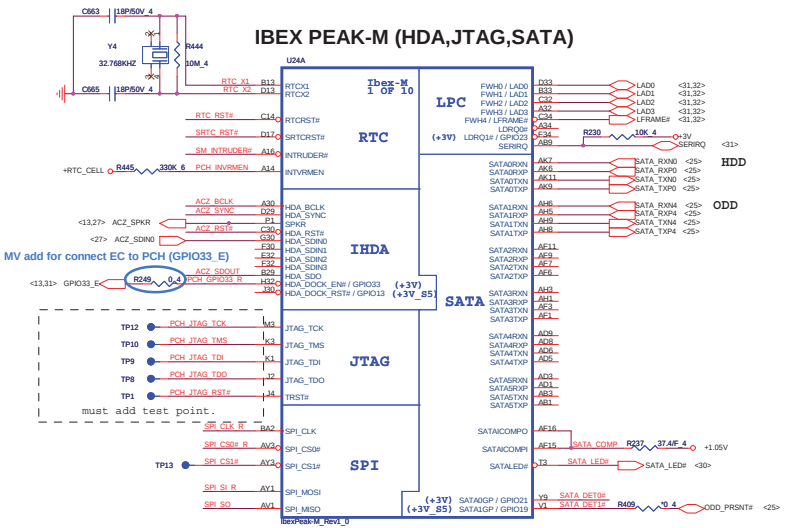
ARRANDALE PROCESSOR (GND)



PROJECT : R18D	
Quanta Computer Inc.	
Size: Custom	Document Number: PROCESSER 7/7(GND)
Rev: 1A	
Date: Thursday, January 13, 2011	Sheet 9 of 42

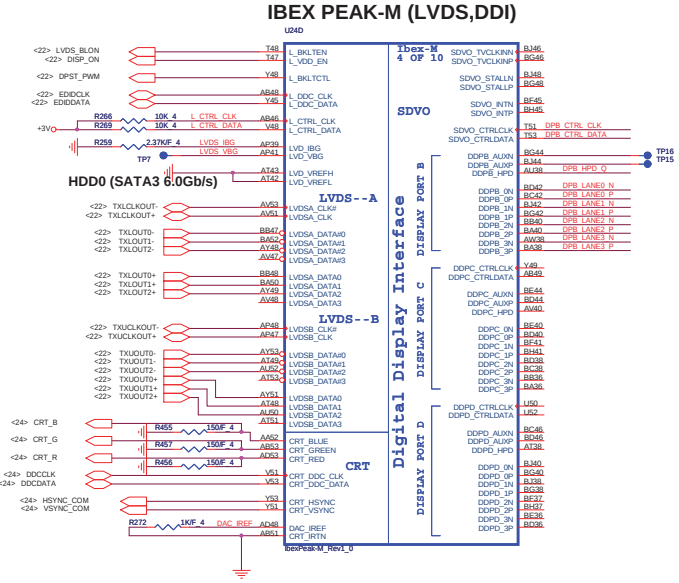
INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)



UMA CRT,LVDS&HDMI signals

IBEX PEAK-M (LVDS,DDI)



1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.

UMA HDMI signals

10/25 PV modify

For ES1 ONLY.NI for ES2.

For ES1 ONLY.NI for ES2.

Part	Part Number	Part Description

For AUDIO

For MDC

RTC

1mA

8/25 SI for M/E.

4M byte SPI ROM

Vender

Socket DG008000031

EON - EN25F32-100HIP

AKE39FN0Q00 IC FLASH(8P) EN25F32-100HIP (SOIC)

WINBOND - W25Q32BVSSIG

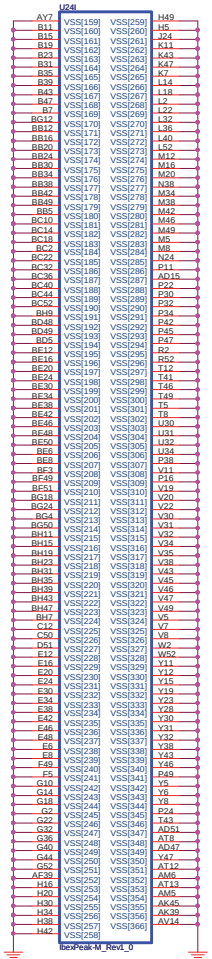
AKE391P0N00 IC FLASH(8P) W25Q32BVSSIG(SOIC)

PROJECT : R18D
Quanta Computer Inc.

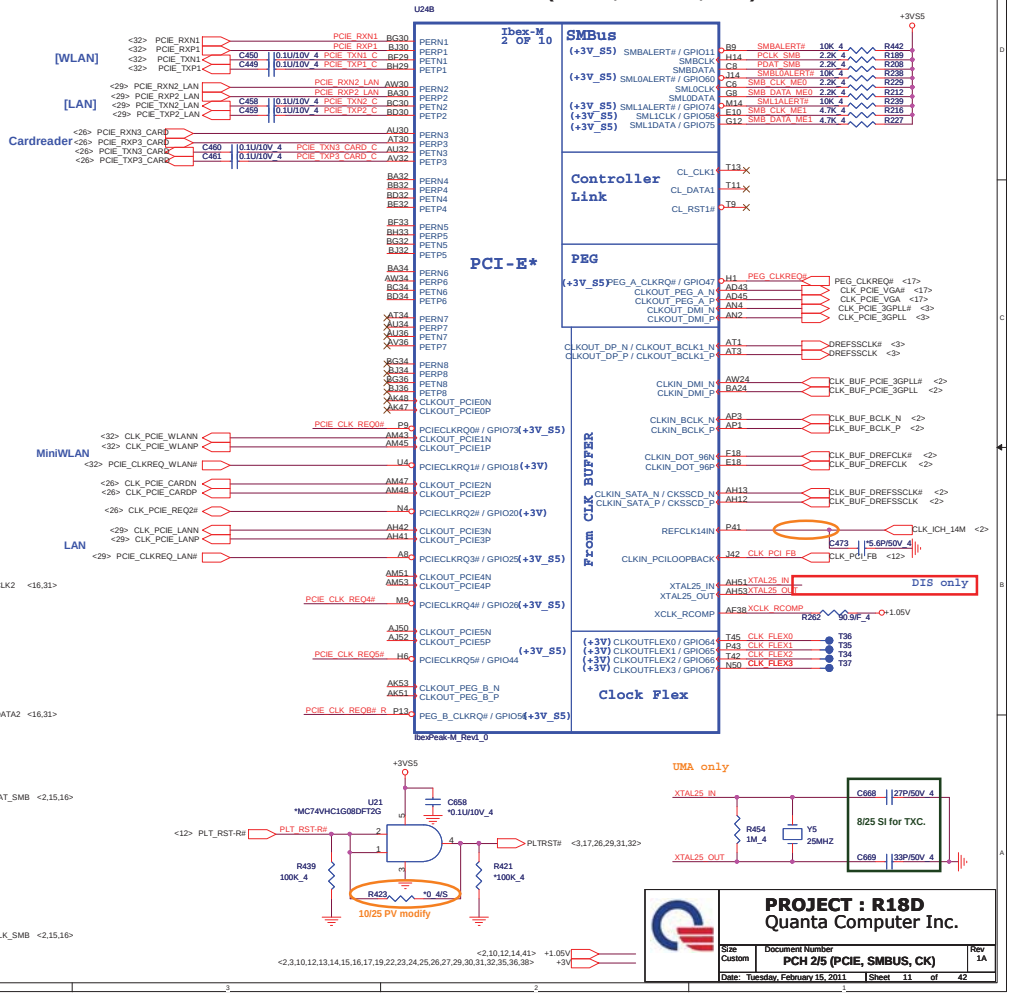
Size	Document Number	Rev
Custom	PCH 1/5 (SATA,HDA,LPC)	1A

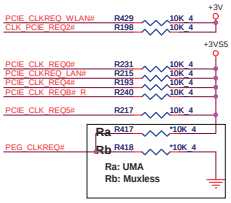
Date: Tuesday, February 15, 2011 Sheet 10 of 42

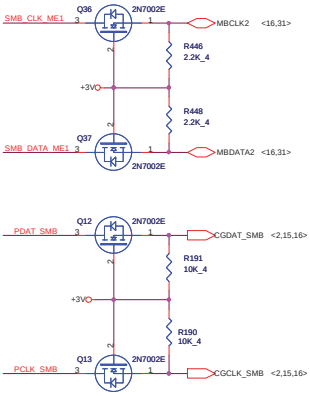
IBEX PEAK-M (GND)



IBEX PEAK-M (PCI-E,SMBUS,CLK)





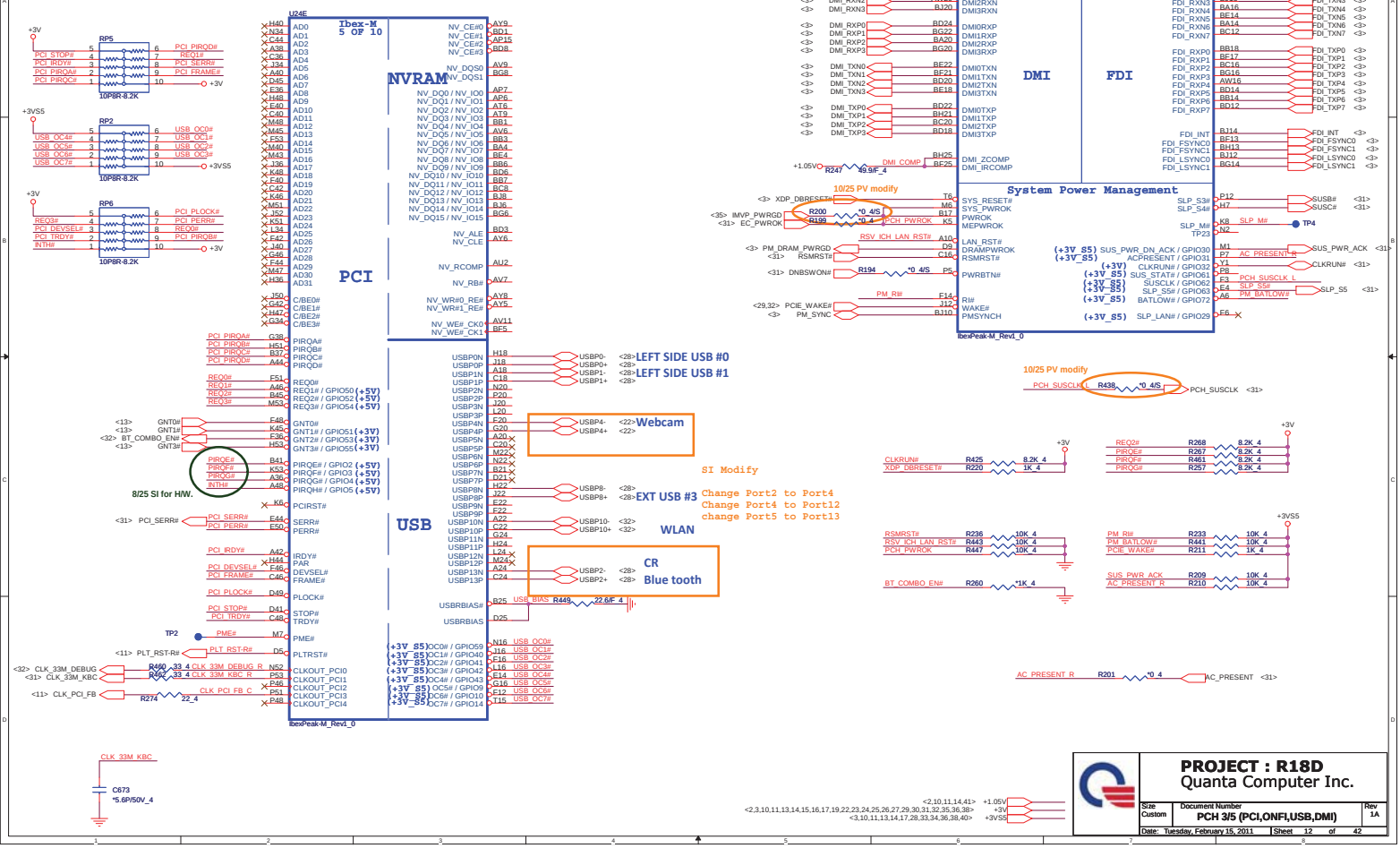


PROJECT : R18D
Quanta Computer Inc.

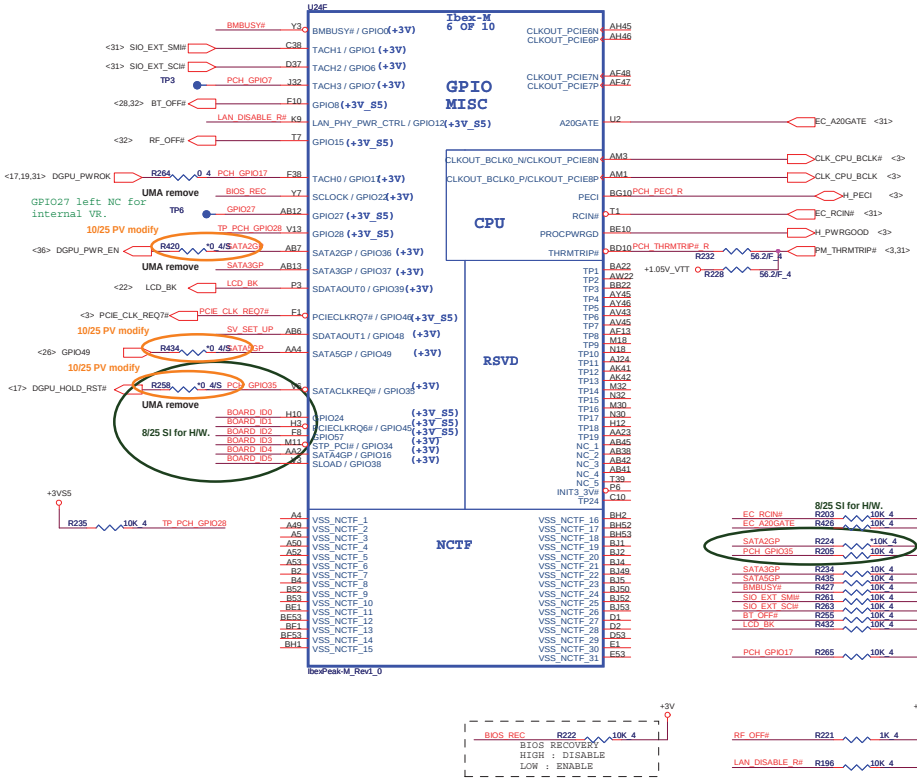
Size	Document Number	Rev
Custom	PCH 2/5 (PCIE, SMBUS, CK)	1A
Date: Tuesday, February 15, 2011	Sheet 11 of 42	

IBEX PEAK-M (DMI,FDI,GPIO)

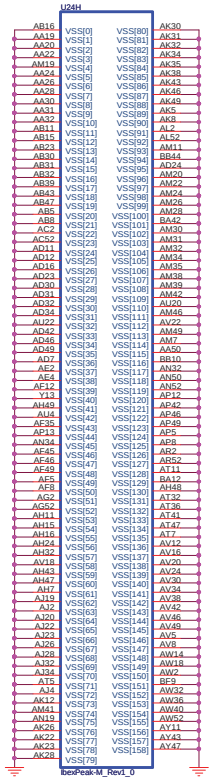
IBEX PEAK-M (PCI,USB,NVRAM)

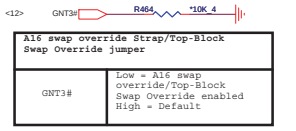


IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)





A16 swap override Strap/Top-Block Swap Override jumper

GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

SV_SET_UP	1-X High = Strong (Default)

Boot BIOS Strap

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Danbury Technology Enabled

NV_ALE	High = Enable Low = Disable

DMI Termination Voltage

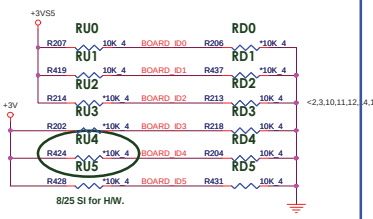
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

No Reboot Strap

R12 MB P/N	ID0	ID1	ID2	ID3	ID4	ID5
UMA						
31R12MB0000 (PIM) 31R12MB0010 (PDT)	0 0	0 0	0 0	0 0	0 0	0 0
Seymour XT Hynix 512						
31R12MB0020 (PIM) 31R12MB0030 (PDT)	1 1	0 0	0 0	0 0	0 0	0 0
Samsung 512						
31R12MB0040 (PIM) 31R12MB0050 (PDT)	1 1	0 0	0 0	0 0	0 0	0 0
Hynix 1G						
31R12MB0060 (PIM) 31R12MB0070 (PDT)	1 1	0 0	0 0	0 0	0 0	0 0
Samsung 1G						
31R12MB0080 (PIM) 31R12MB0090 (PDT)	1 1	0 0	0 0	0 0	0 0	0 0

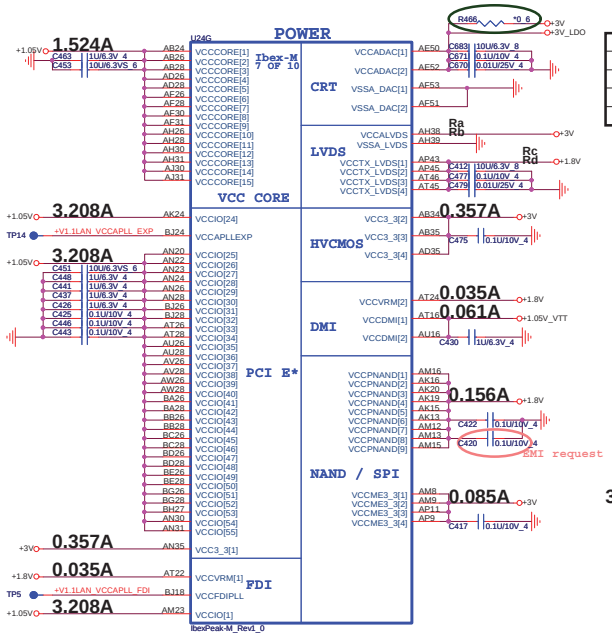
Board ID	ID0 GPIO24	ID1 GPIO45	ID2 GPIO57	ID3 GPIO34	ID4 GPIO35	ID5 GPIO38
UMA/DIS	0=UMA 1=Dis.					
1.1/1.0		1=1.1 0=1.0				
Reserve			0=No 1=Yes			
Reserve				0=No 1=Yes		
Reserve					0=No 1=Yes	
Reserve						0=No 1=Yes

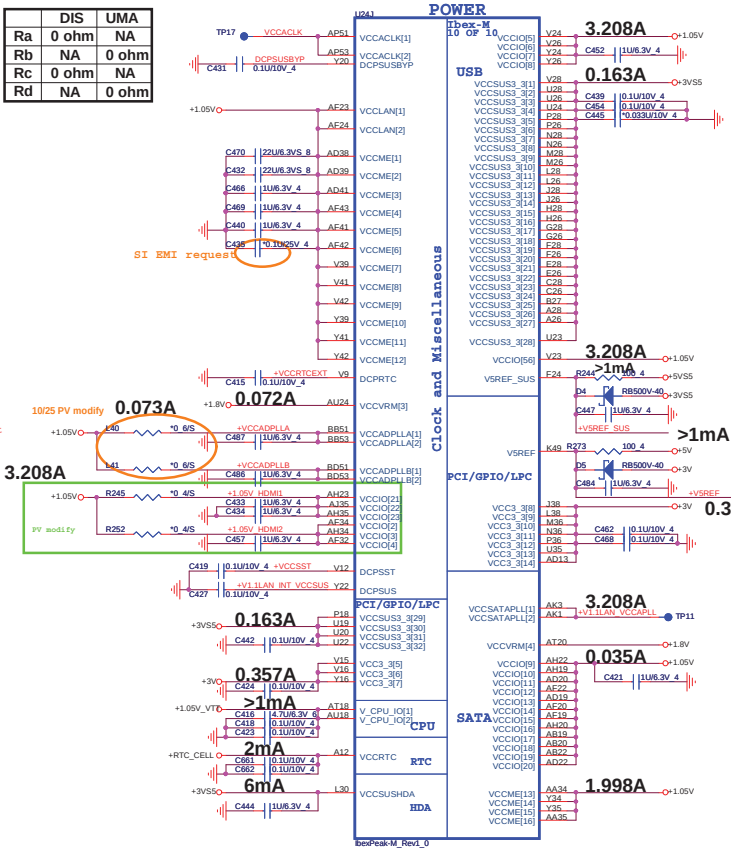
BOARD_ID1設成HIGH代表Rockey 1.1



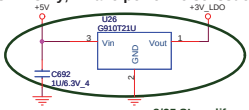
8/25 SI modify
Uninstall on UMA
Install on DIS

	DIS	UMA
Ra	0 ohm	NA
Rb	NA	0 ohm
Rc	0 ohm	NA
Rd	NA	0 ohm

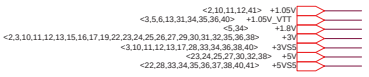




UMA Only, If have power noise issue then stuff it.



8/25 SI modify
Install LDO when UMA



PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 5/5 (POWER)	1A

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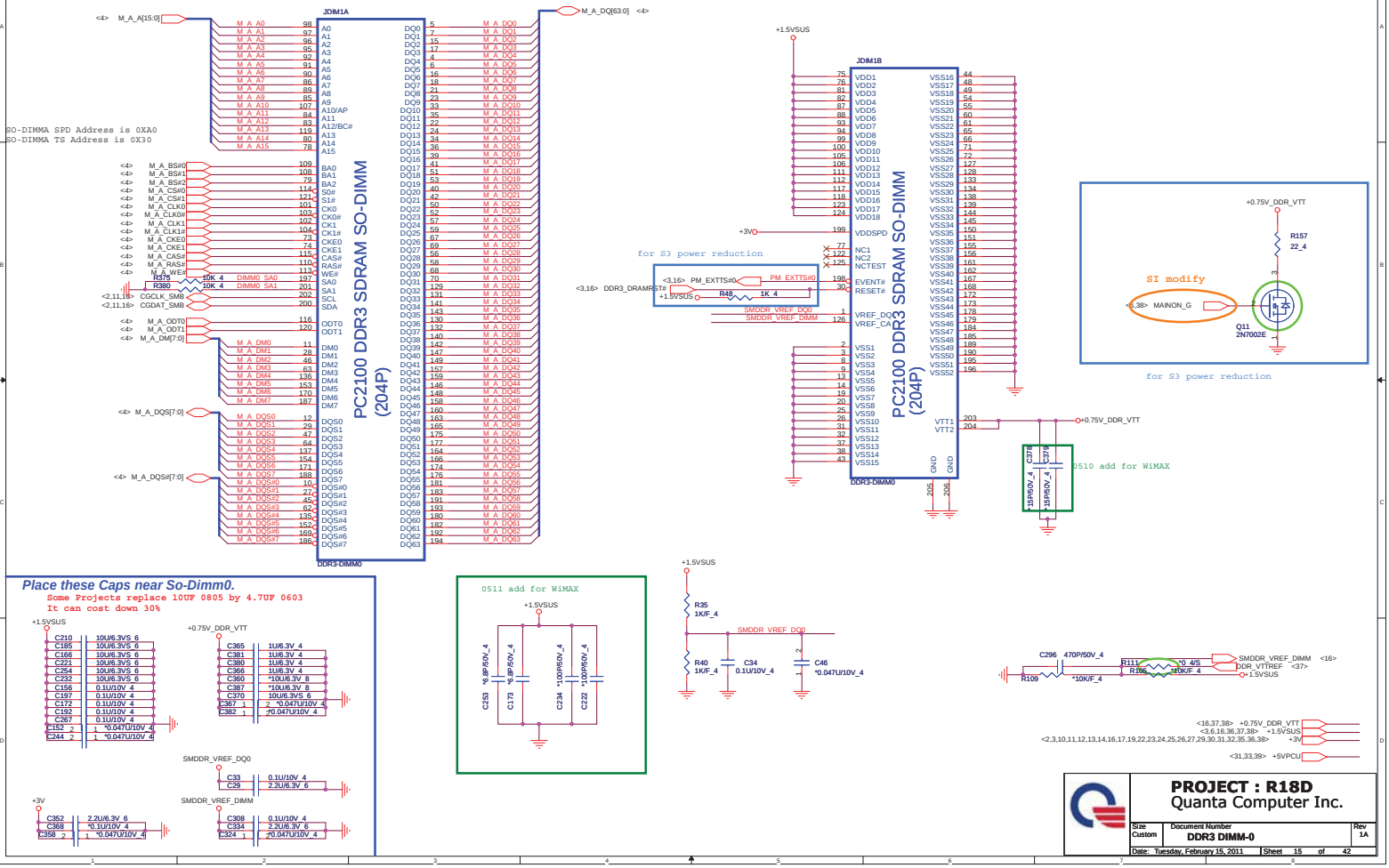
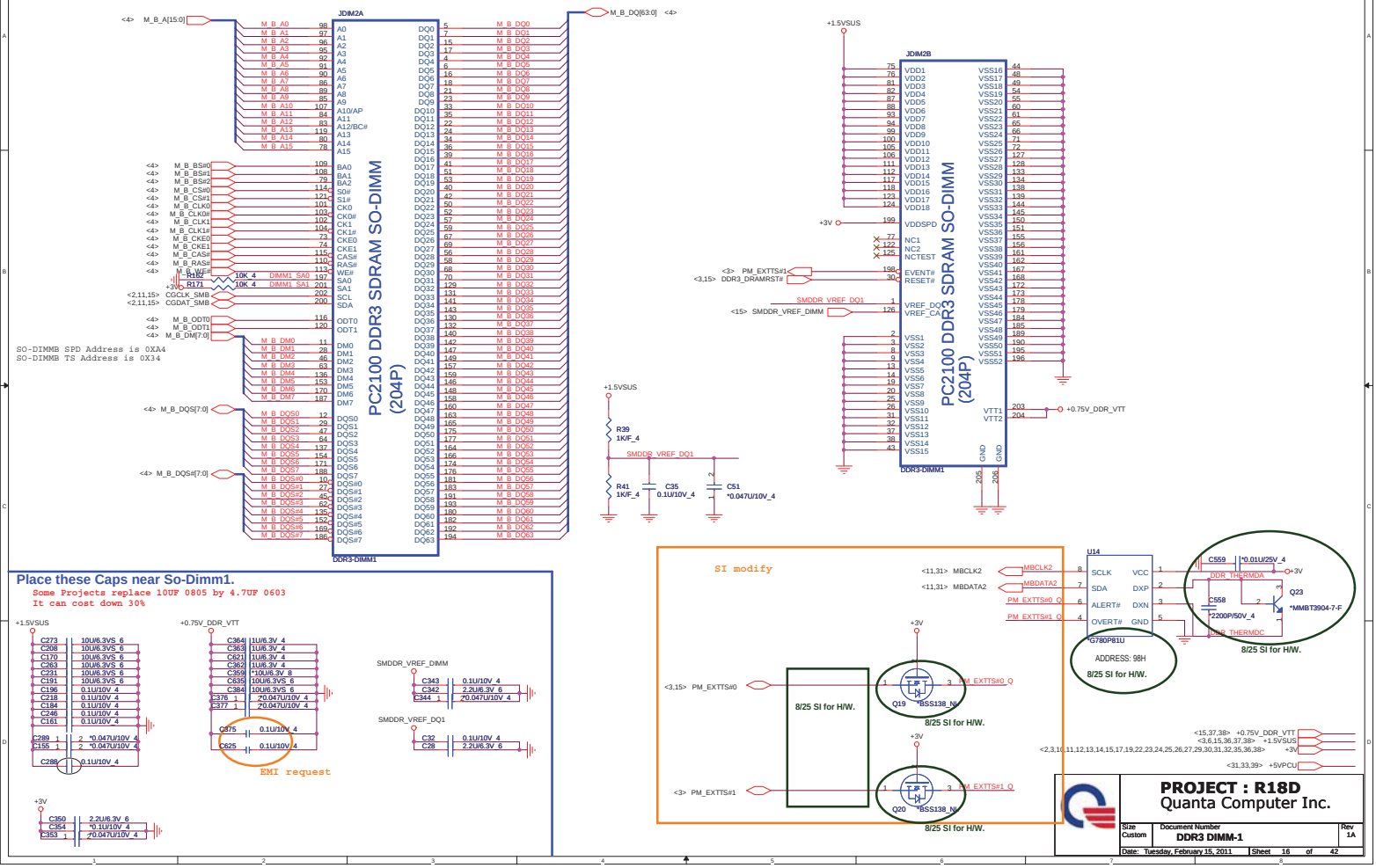
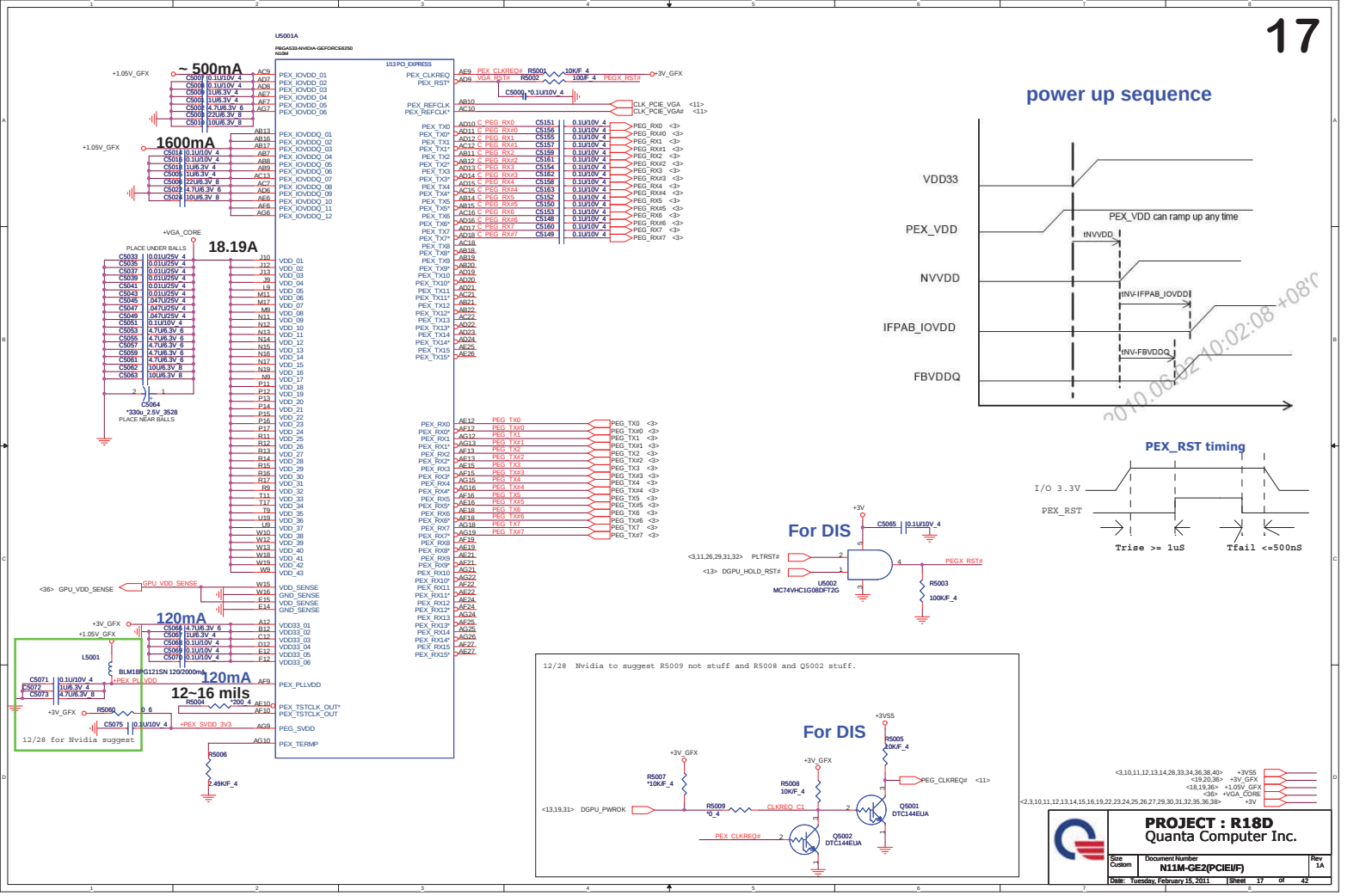
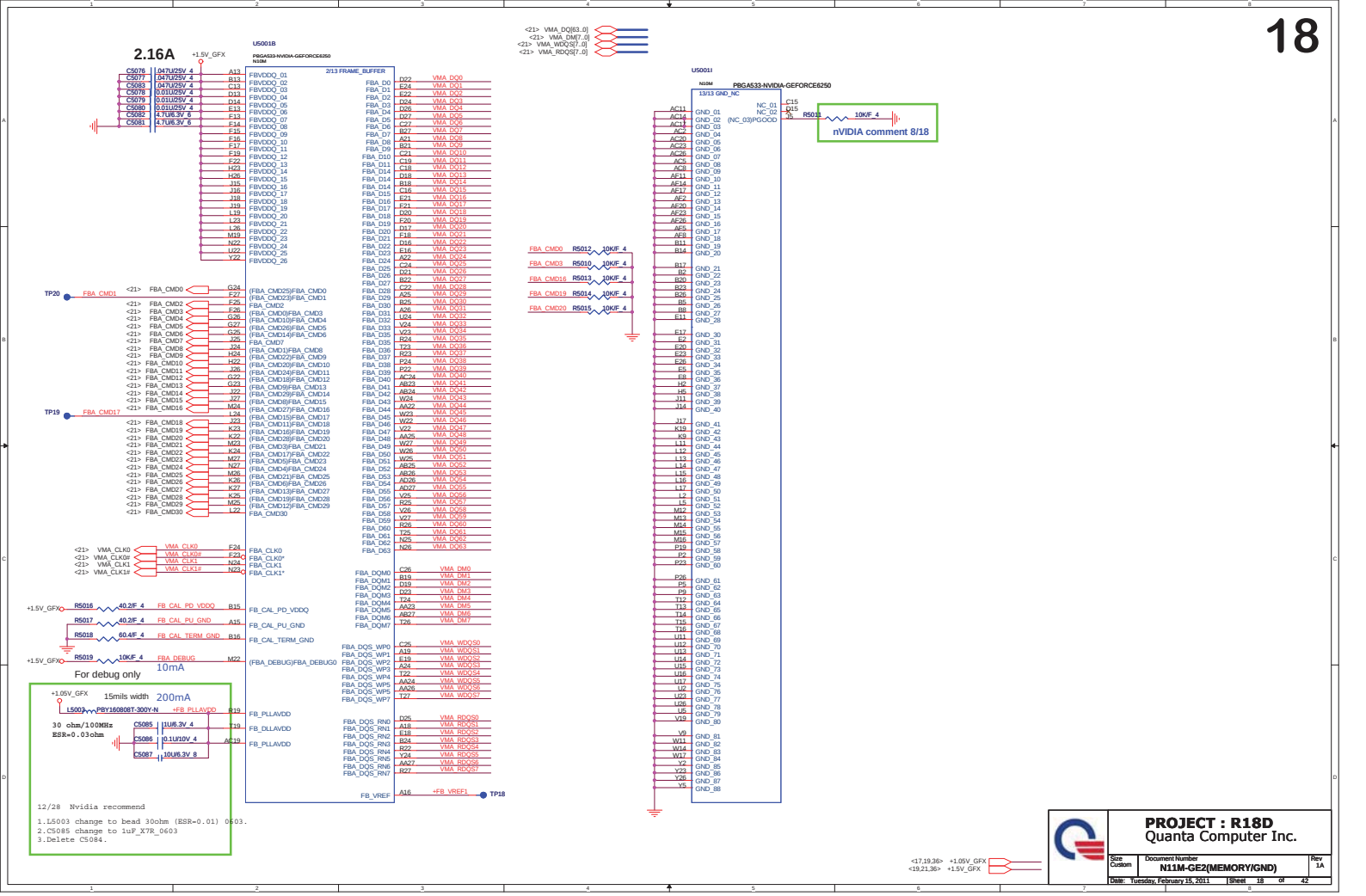
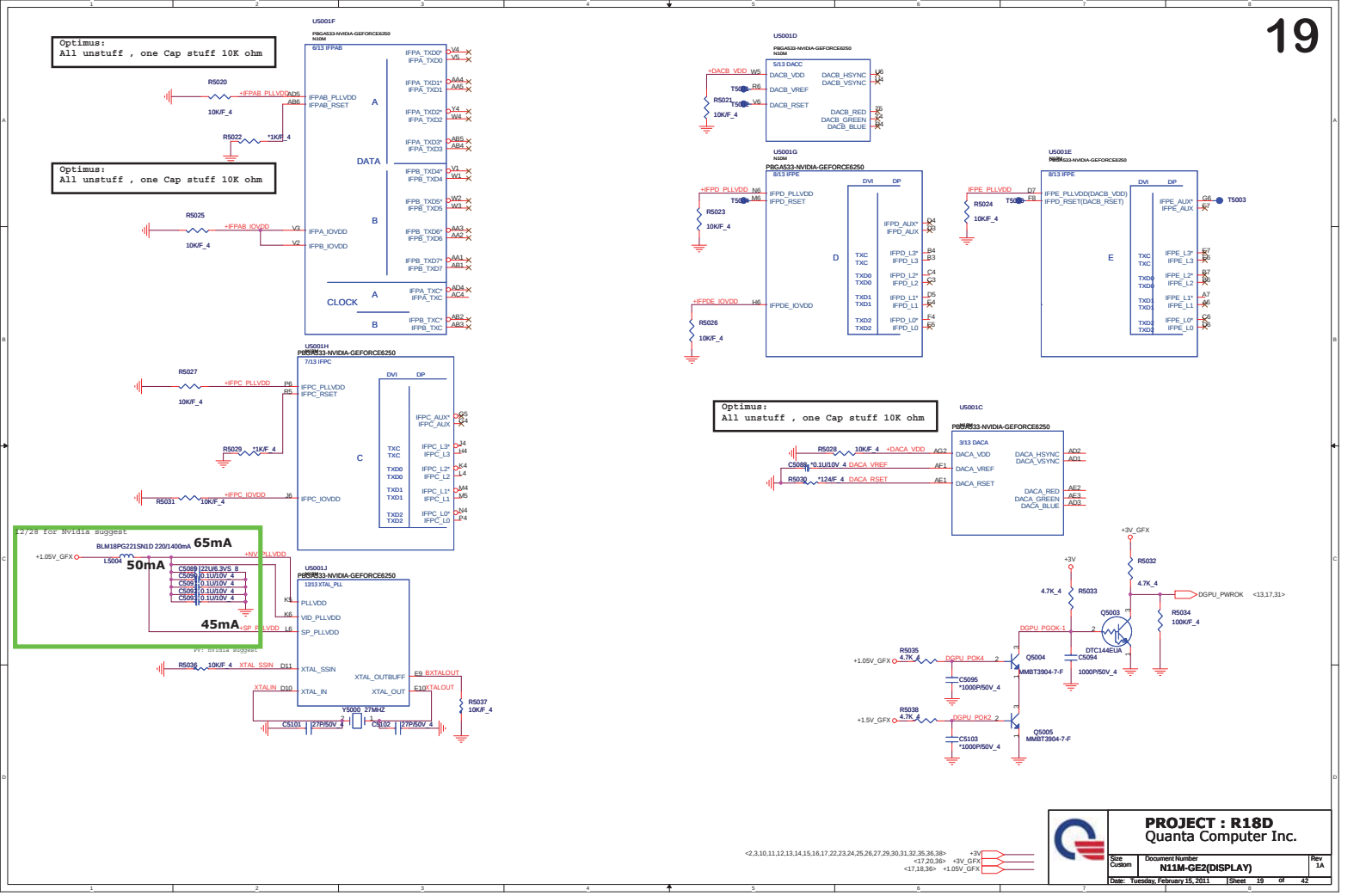










N12P-GV -> 0x17F

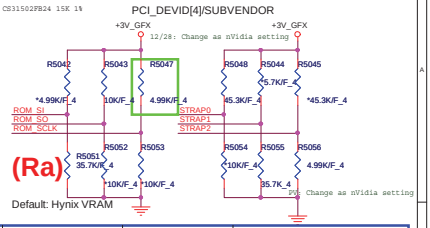
N12M-GE -> 0xA7A 1010 ->PU15K

4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
30.1K/F_4: CS33012FB18 [RES CHIP 30.1K 1/16W +-1%(0402)]
35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

PCI_DEVID[4]/SUBVENDOR



Default: Hynix VRAM

ROM_SI -> based on VRAM.

ROM_SO -> PU 10K

ROM_SCLK -> PU 5K

STRAP0 -> PU 45K

STRAP1 -> PD 35K

STRAP2 -> PD 5K

STRAP3 -> PD 5K

STRAP 4 -> PD 10K.

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33V

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix		PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung		PD 20K
0110	DDR3 128Mx16x4, 128bit, 1GB,800MHz	Hynix		PD 35K
0111	DDR3 128Mx16x4, 128bit, 1GB,800MHz	Samsung		PD 45K
XXXX				
XXXX				

(Ra)

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	Memory VREF SELECT
11	I/O	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	THERM_LOAD_STEP_DOWN
14	OUT	N/A	THERM_LOAD_STEP_UP

12/28 for Nvidia suggest

12/28 for Nvidia suggest

N12P-GV default boot up voltage should be set to 0.85V. Therefore, please add 10K pull down resistors to GFX_CORE_CNTRL0 and GFX_CORE_CNTRL1

12/29 Nvidia suggest for AC/Batt# function

12/29 Nvidia suggest

PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N12P-GV(GPIO/STRAPS)	1A

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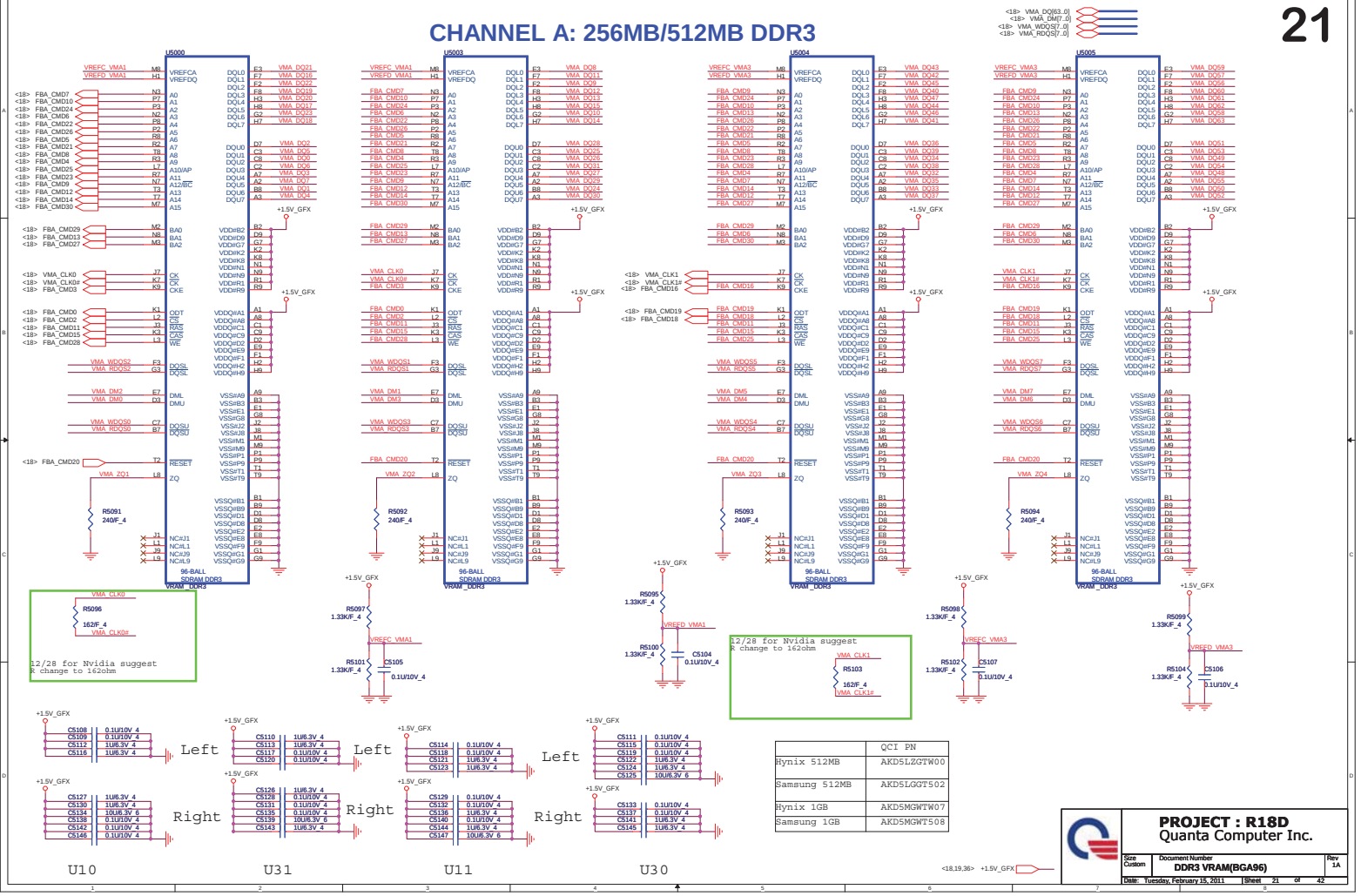
CHANNEL A: 256MB/512MB DDR3

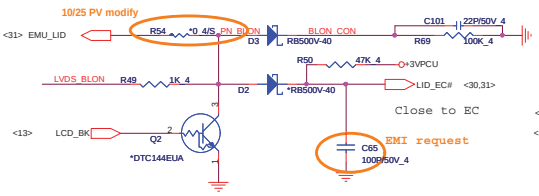


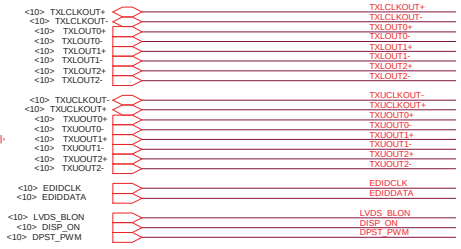
	QCI PN
Hynix 512MB	AKD5LZGTW00
Samsung 512MB	AKD5LGGT502
Hynix 1GB	AKD5MGWTW07
Samsung 1GB	AKD5MGWT508

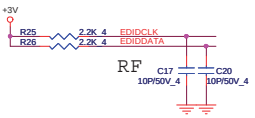
PROJECT : R18D
Quanta Computer Inc.

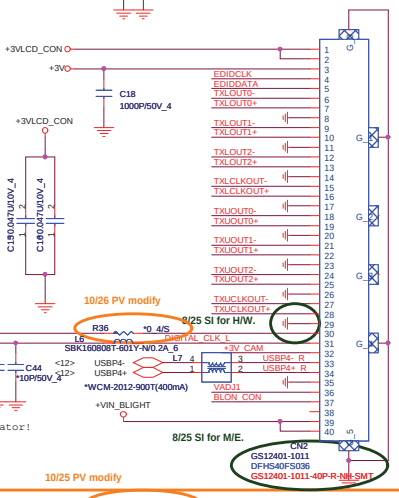
Size	Document Number	Rev
Custom	DDR3 VRAM(BGA96)	1A
Date: Tuesday, February 15, 2011	Sheet 21 of 42	

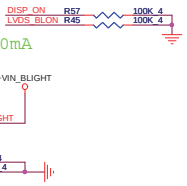
LID Switch

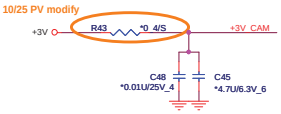






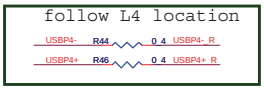


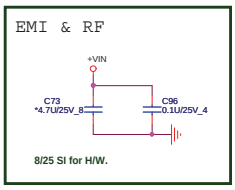


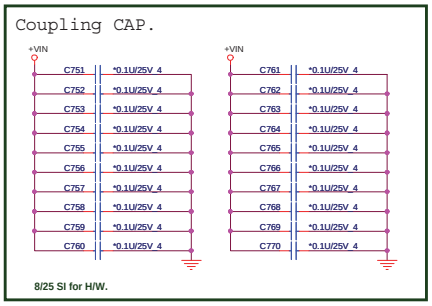


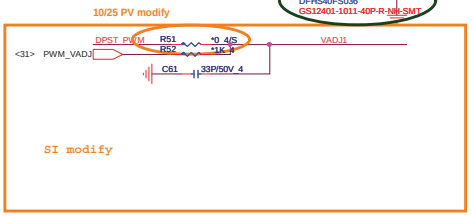
Please note that 2011 camera is +3V a We do not need to use 5V -> 3.95V regulator!

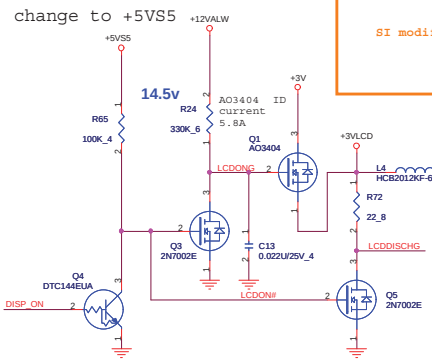
follow L4 location









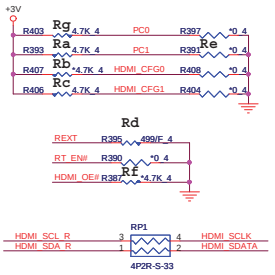


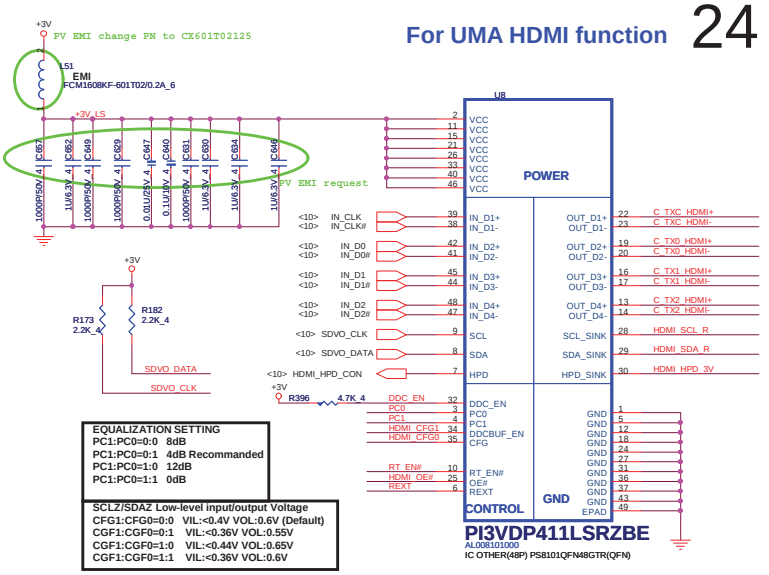
<10,30,31,33,39> +3VPCU
<2,3,10,11,12,13,14,15,16,17,19,23,24,25,26,27,29,30,31,32,35,36,38> +3V
<25,36,38,39> +12VALW
<33,34,35,36,37,38,39,40,41> +VIN

PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A
Date: Tuesday, February 15, 2011	Sheet 22 of 42	

Signals		PDT	PIM	CHR
PC1	Ra	4.7K	4.7K	NC
HDMI_CFG0	Rb	NC	NC	NC
HDMI_CFG1	Rc	4.7K	NC	NC
REXT	Rd	499	4.7K	1.2K
PC1	Re	NC	NC	4.7K
HDMI_OE#	Rf	NC	NC	4.7K
PC0	Rg	4.7K	4.7K	4.7K





Vender	Part	Part Number	Part Description
PDT	PS8101	AL008101000	IC OTHER(48P) PS8101QFN48GTR(QFN)
PIM	PI3VDP411LSRZBE	ALP411LS004	IC OTHER(48P) PI3VDP411LSRZBE(TQFN)
CHR	CH7318C	AL007318002	IC OTHER(48P) CH7318C-BF-TR(QFN)

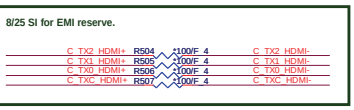
9/16 : PIM: need use ALP411LS000 or ALP411LS004 for capella

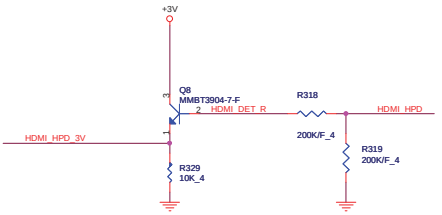
CHR : need Na R1182, add R1027 for capella

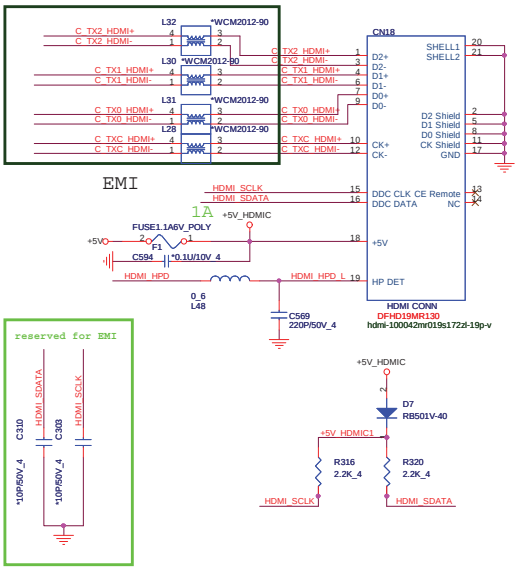
EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

SCLZ/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CFG1:CFG0=0:1 VIL:<0.36V VOL:0.55V
CFG1:CFG0=1:0 VIL:<0.44V VOL:0.65V
CFG1:CFG0=1:1 VIL:<0.36V VOL:0.6V

8/25 SI for EMI reserve.



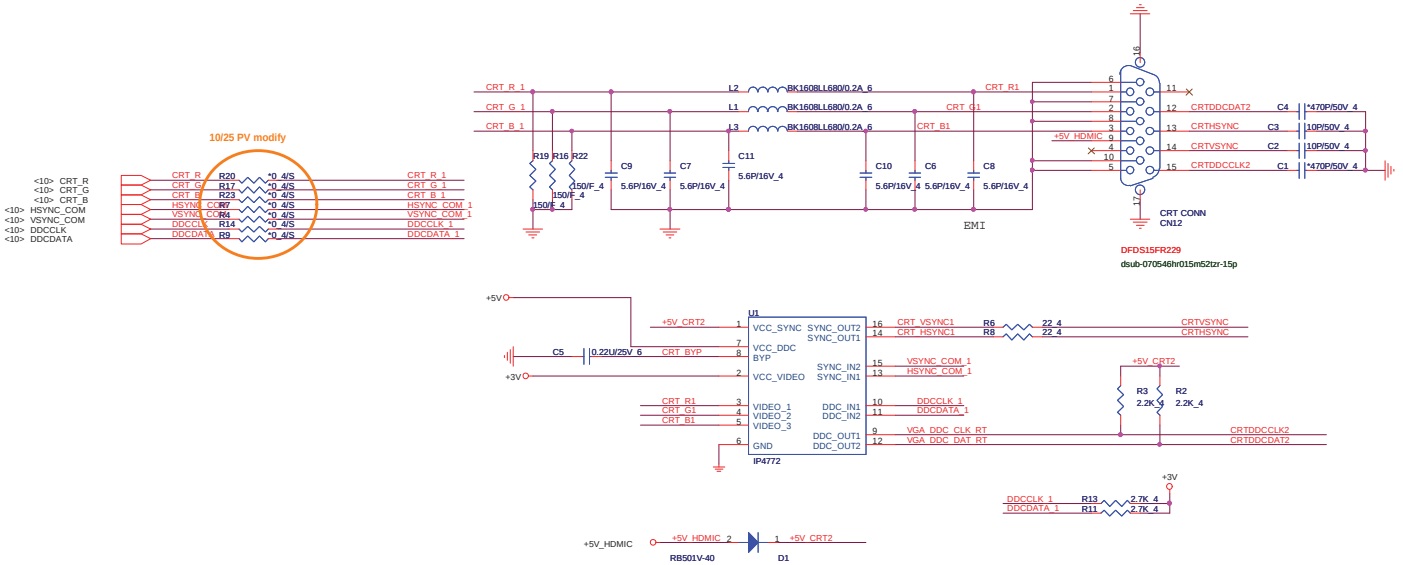




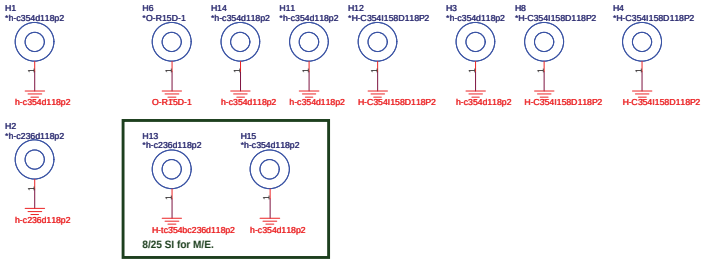
PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI CONN	1A
Date: Tuesday, February 15, 2011	Sheet 23 of 42	

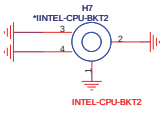
CRT PORT



HOLE



CPU



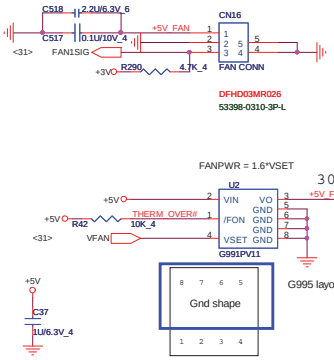
VGA

PROJECT : R18D
Quanta Computer Inc.

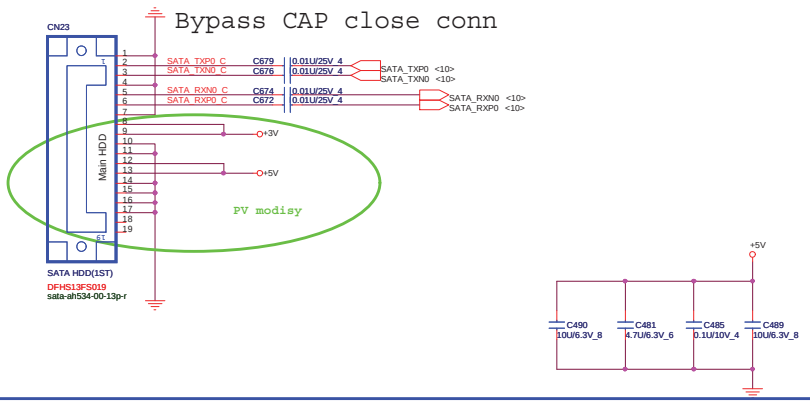
Size	Document Number	Rev
Custom	CRT,Hole	1A

Date: Tuesday, February 15, 2011 Sheet 24 of 42

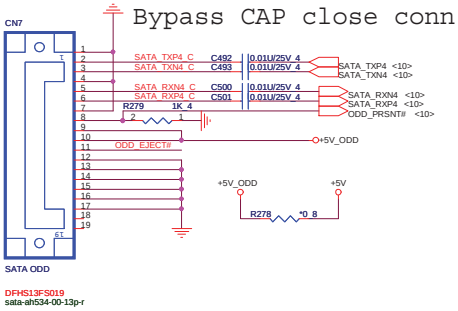
CPU FAN

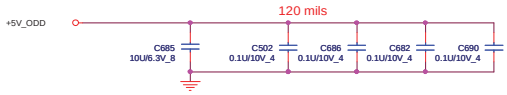


SATA HDD CONNECTOR

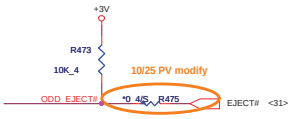


SATA ODD CONNECTOR

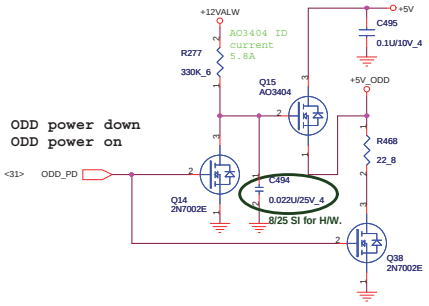




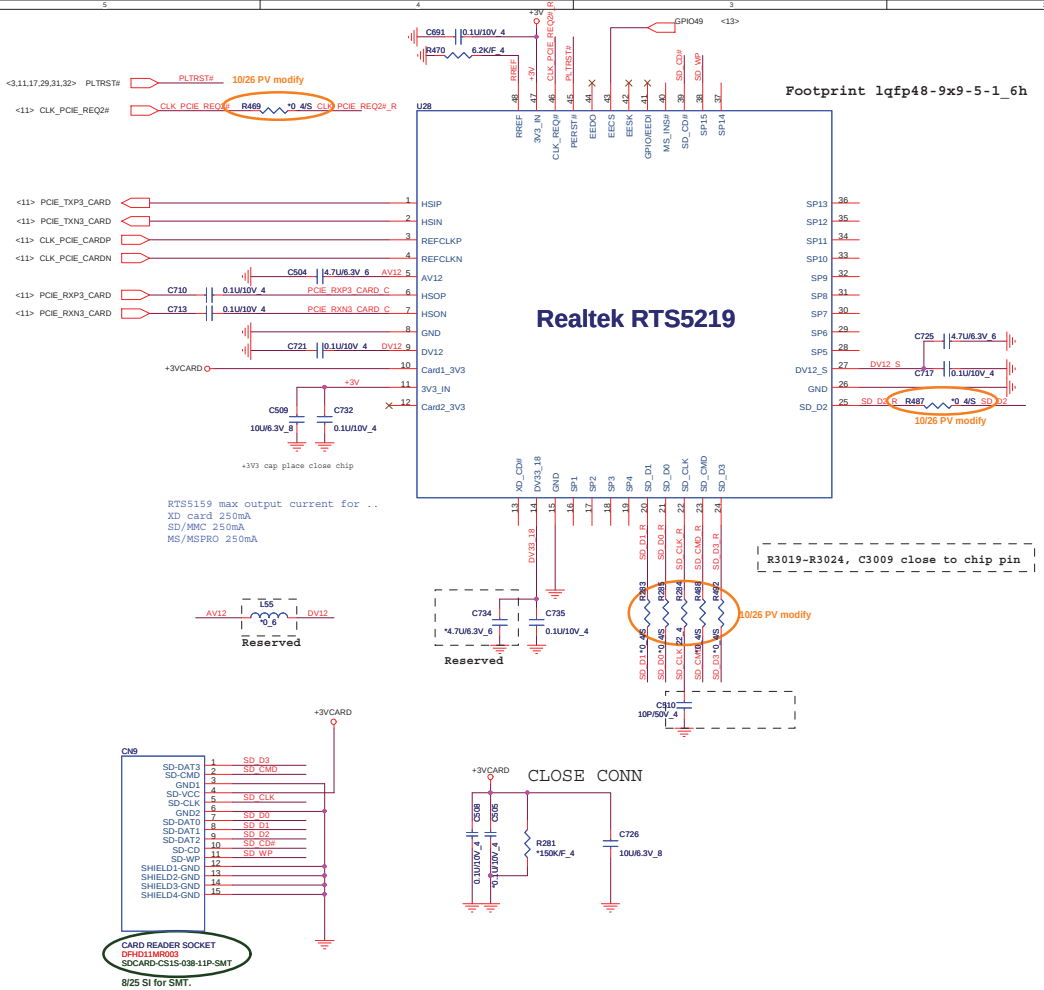
follow INTEL DG change eject PU to +3V.



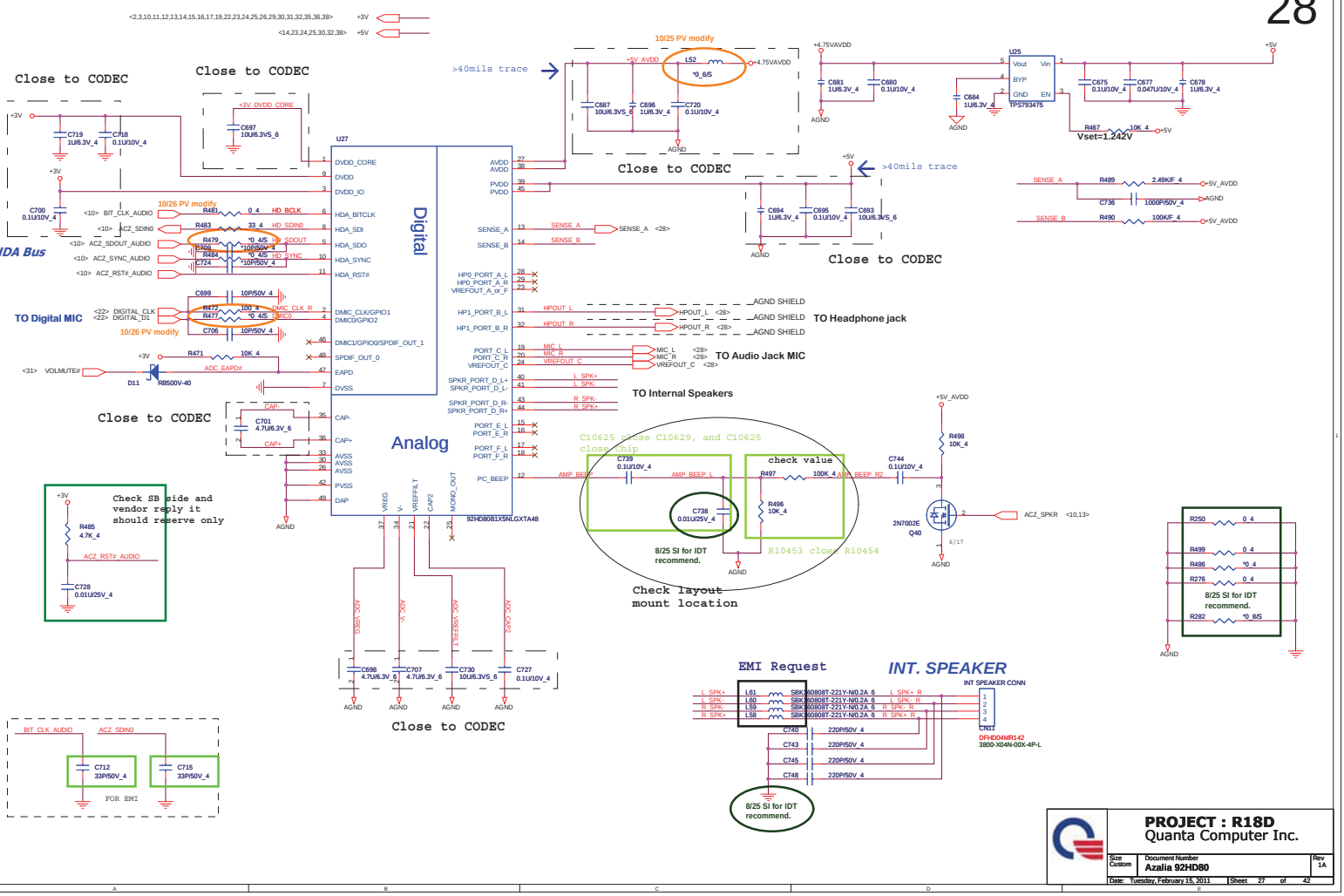
High : ODD power down
Low : ODD power on

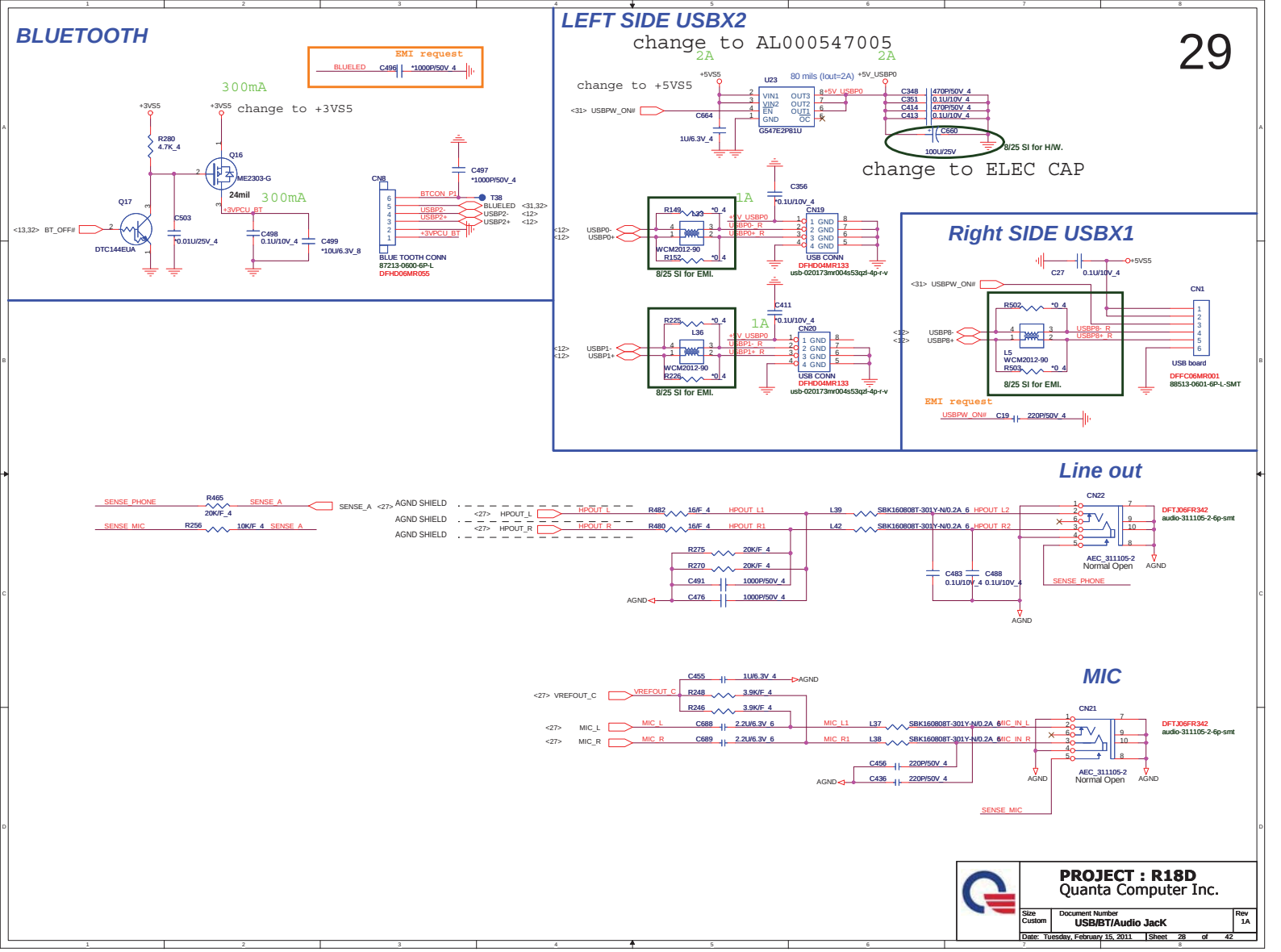


	PROJECT : R18D Quanta Computer Inc.	
Size Custom	Document Number HDD/ODD/FAN	Rev 1A
Date: Tuesday, February 15, 2011	Sheet 25 of 42	



PROJECT : R18D Quanta Computer Inc.		
Size: Custom	Document Number: RTS5219 & CR SOCKET &HOLE	Rev: 1A
Date: Tuesday, February 15, 2011	Sheet 26 of 42	

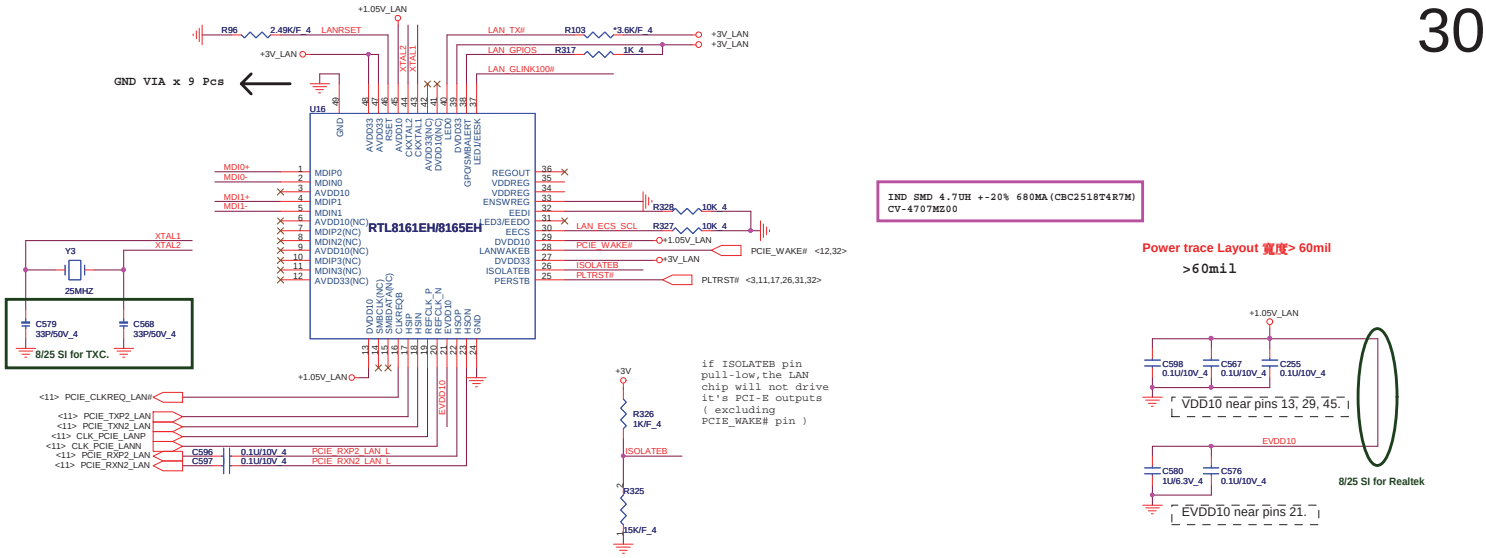


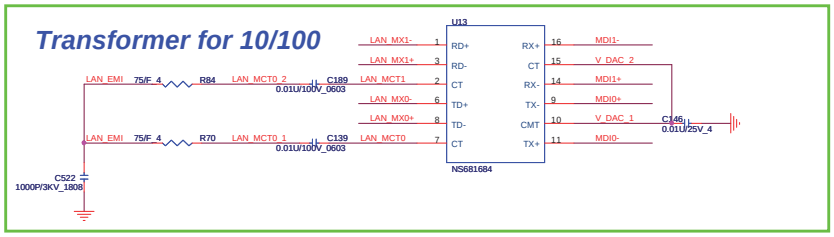


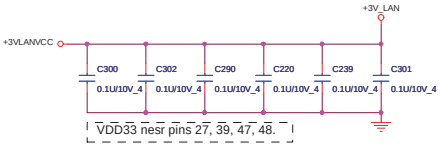
29

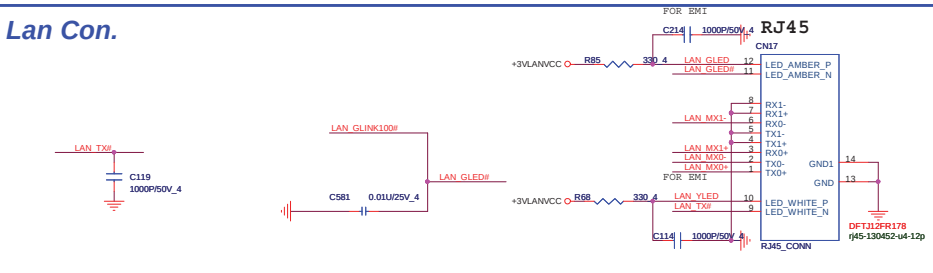
PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB/BT/Audio JacK	1A
Date: Tuesday, February 15, 2011	Sheet 28 of 42	









PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL8165EH	1A

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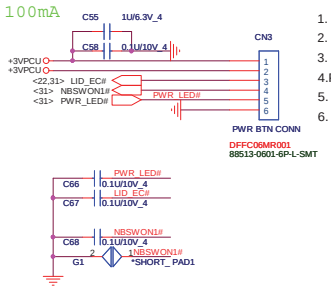
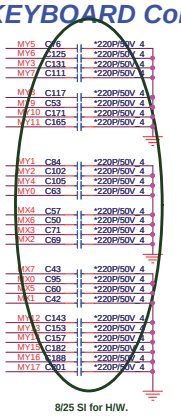
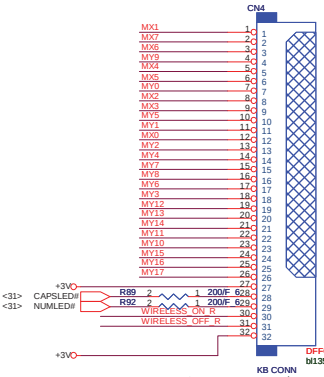
POWER BOTTON CONNECT



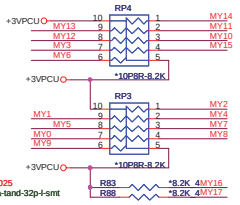
1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4.POWERON#
5. PWRLED#
6. GND

KEYBOARD Con.



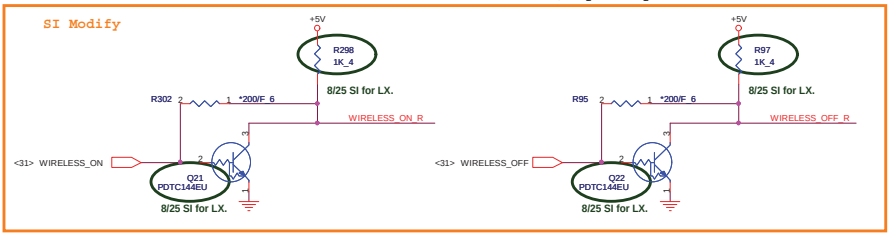


KEYBOARD PULL-UP

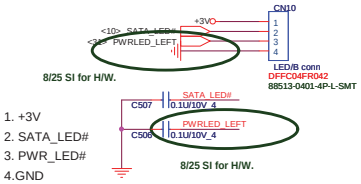


EC KB3930 has included K/B pull-up resistor and function

SI Modify



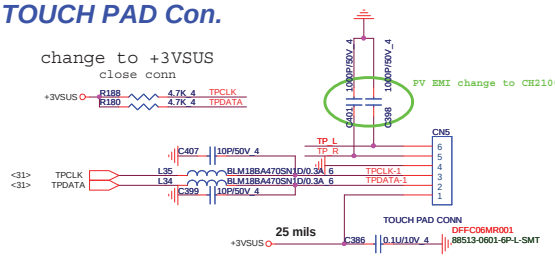
LED Con.



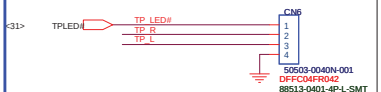
1. +3V
2. SATA_LED#
3. PWR_LED#
4.GND

TOUCH PAD Con.

change to +3VSUS
close conn



To TOUCH PAD SW board



PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/KB/SW/TP	1A

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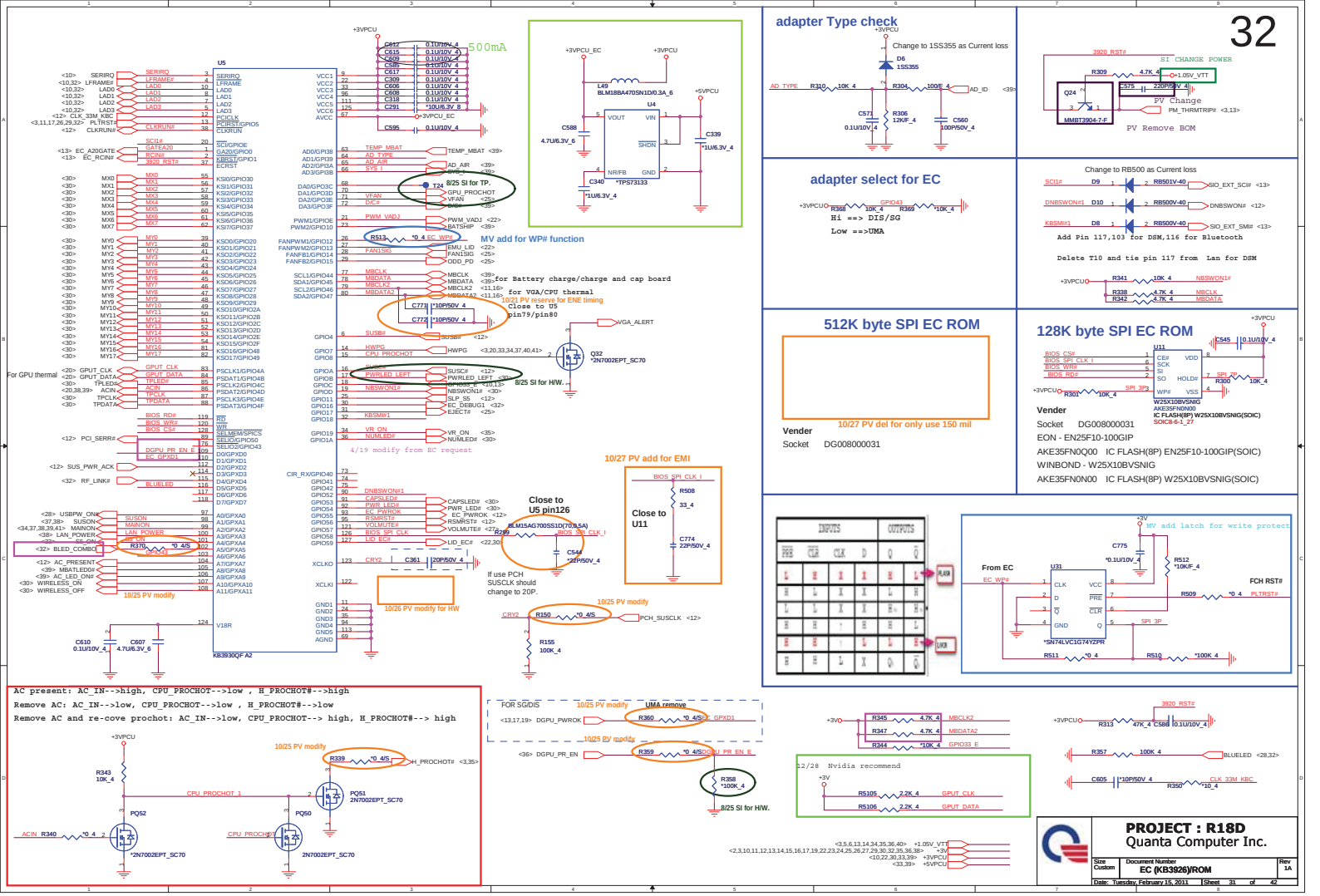
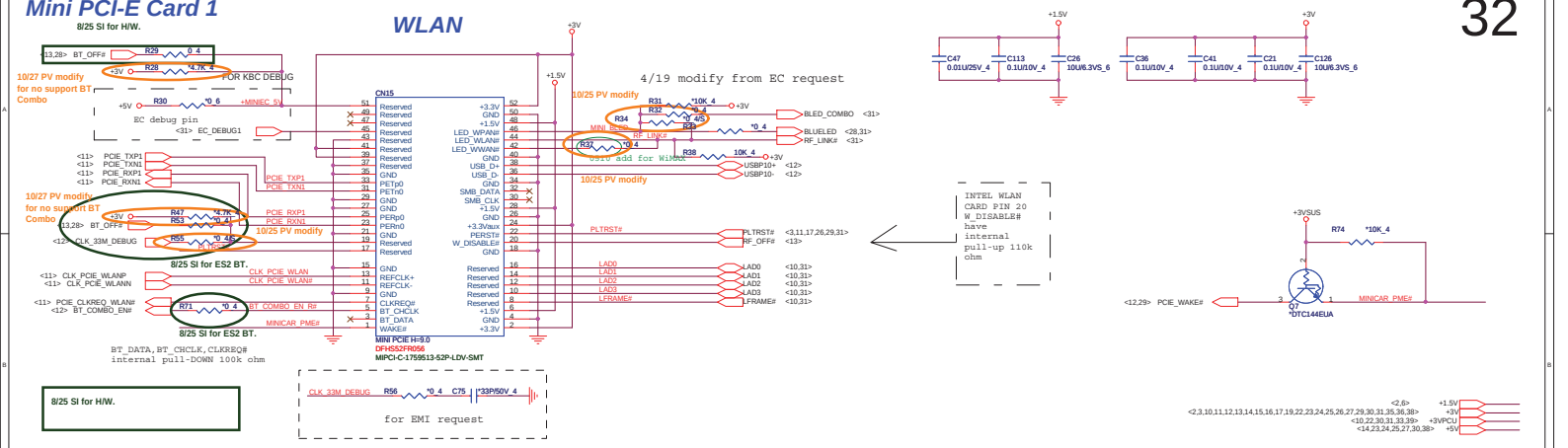
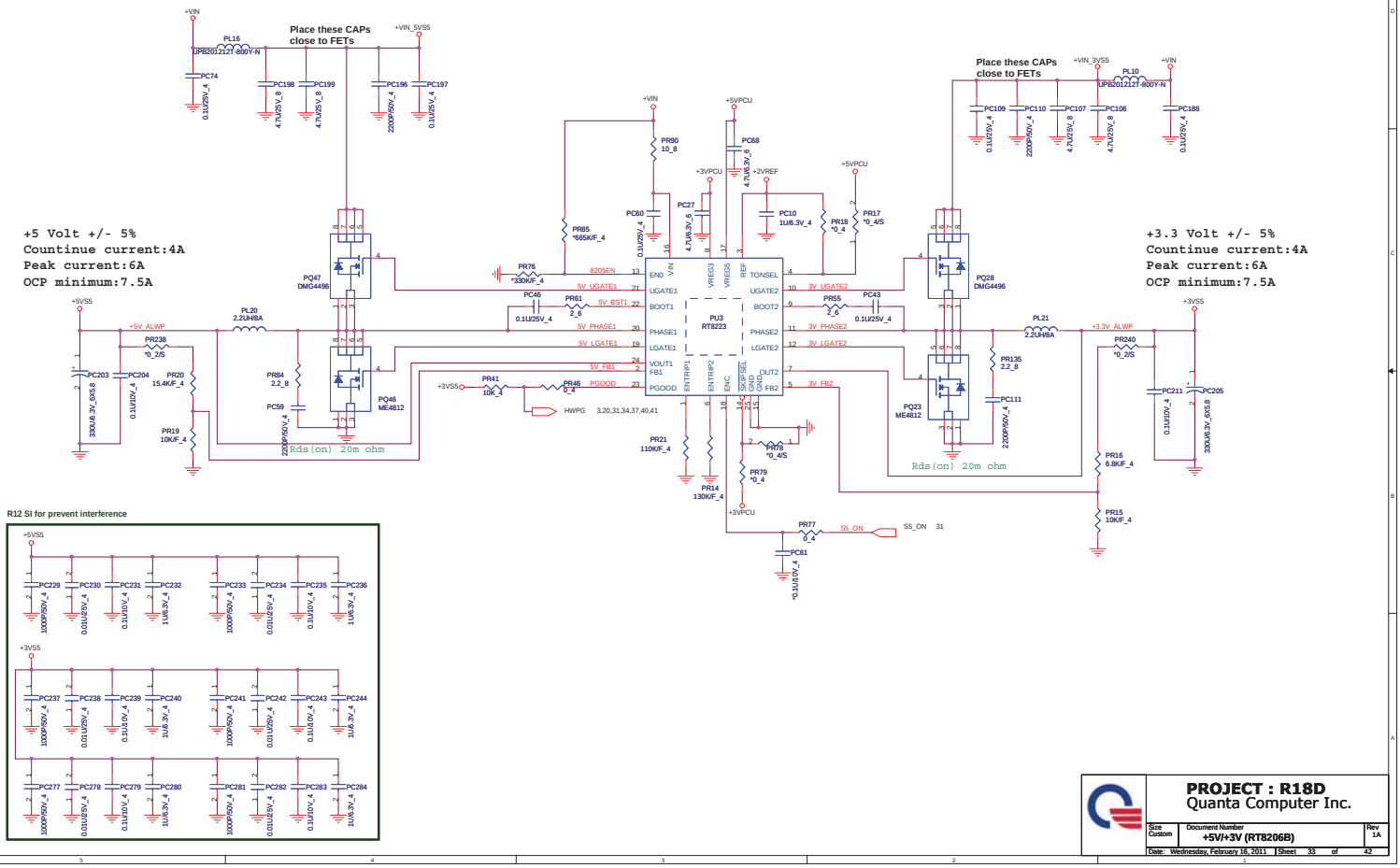


Mini PCI-E Card 1

WLAN



PROJECT :	R18D
Quanta Computer Inc.	
Size: Custom	Document Number: MINI PCIE CONN X1
Rev: 1A	
Date: Tuesday, February 15, 2011	Sheet 32 of 42



PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+5V/+3V (RT8206B)	1A

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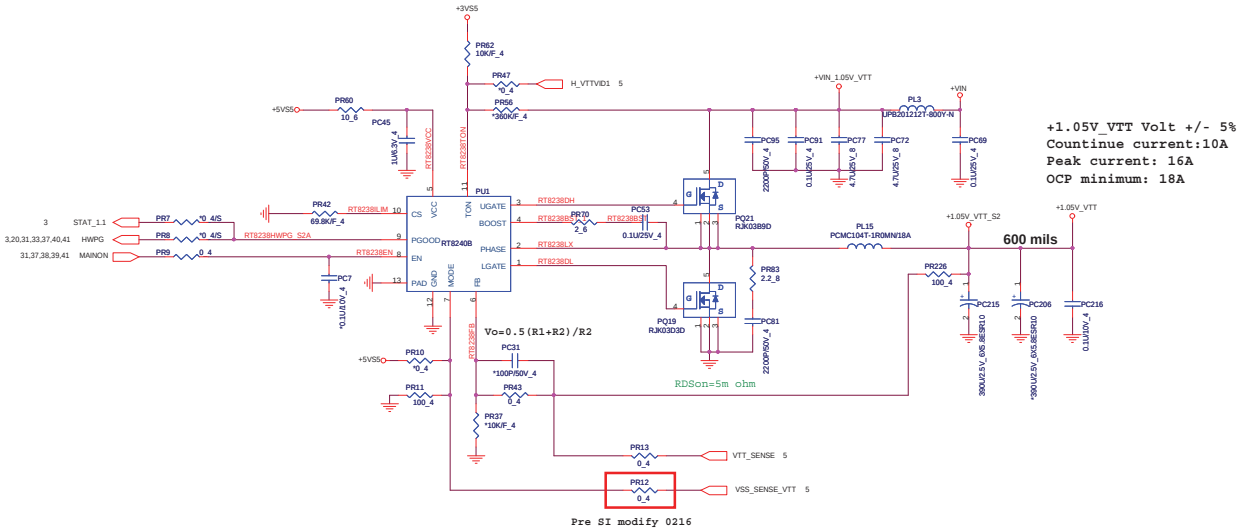

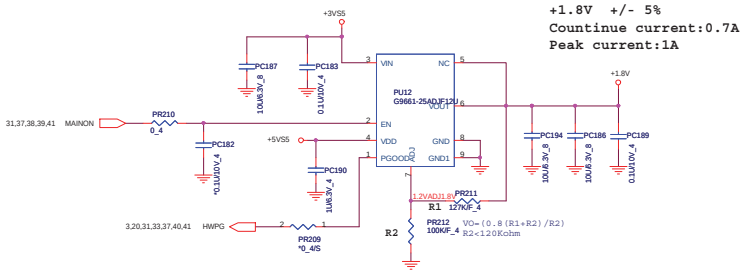

PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.1V VTT / PCH	1A

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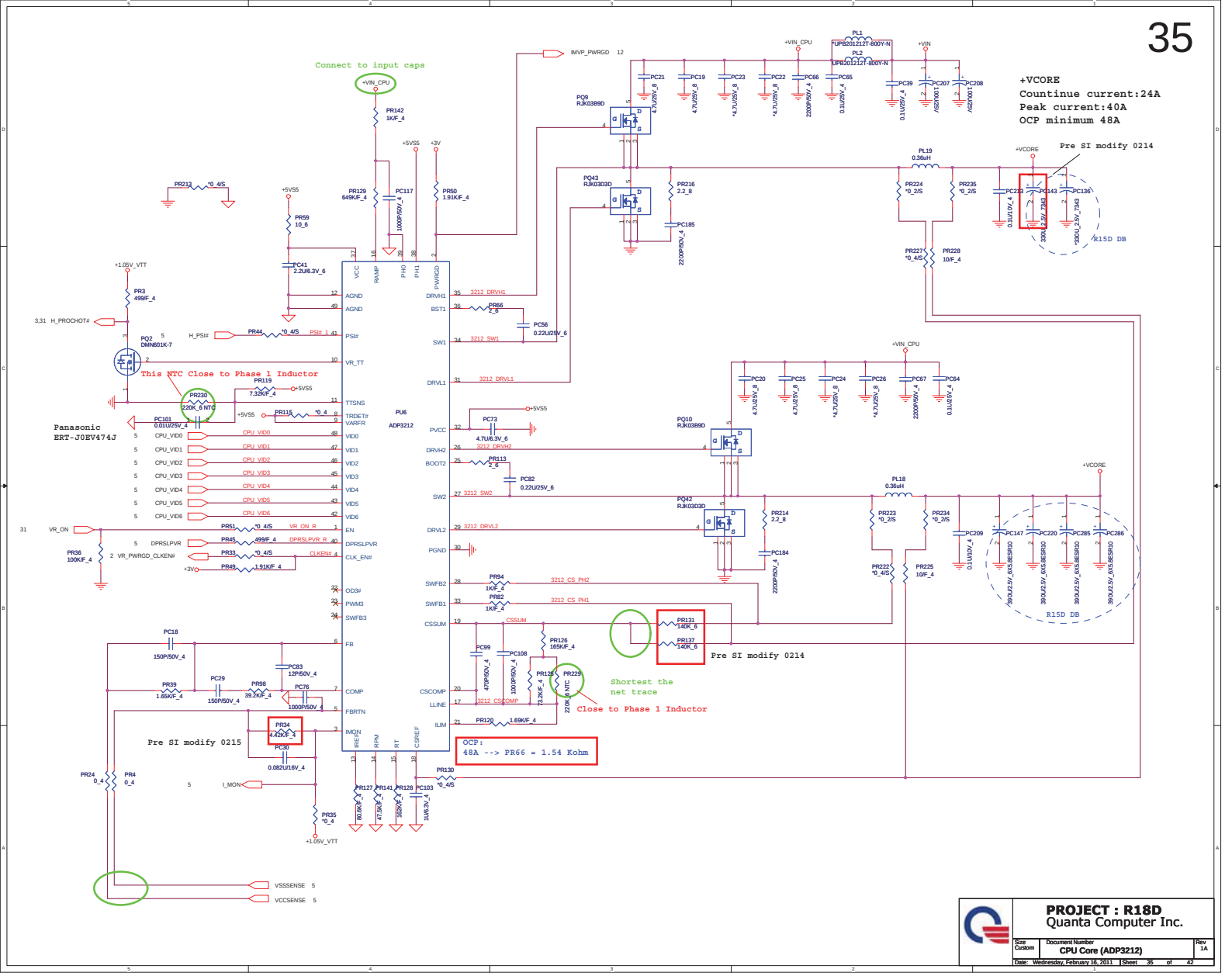
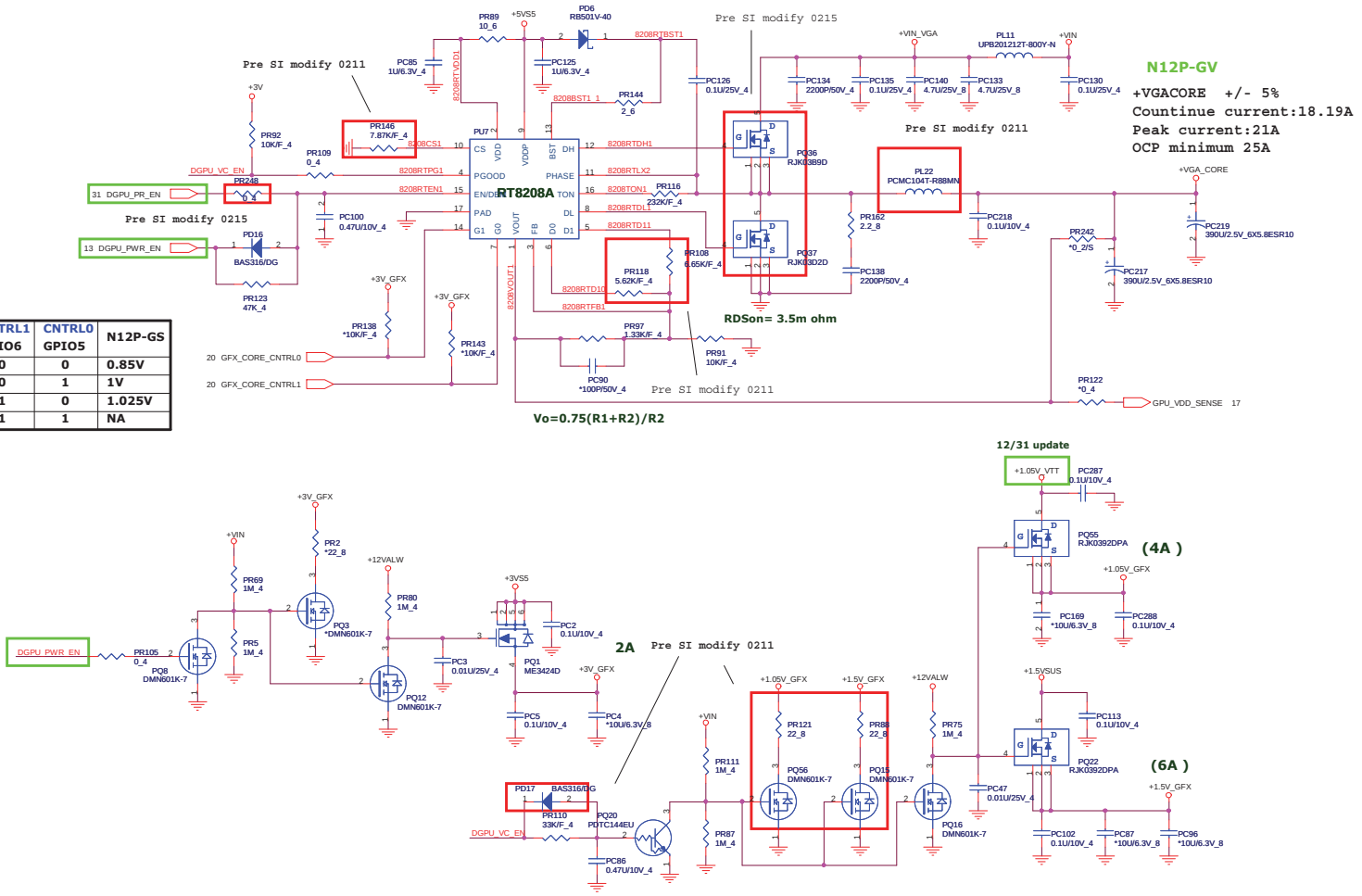
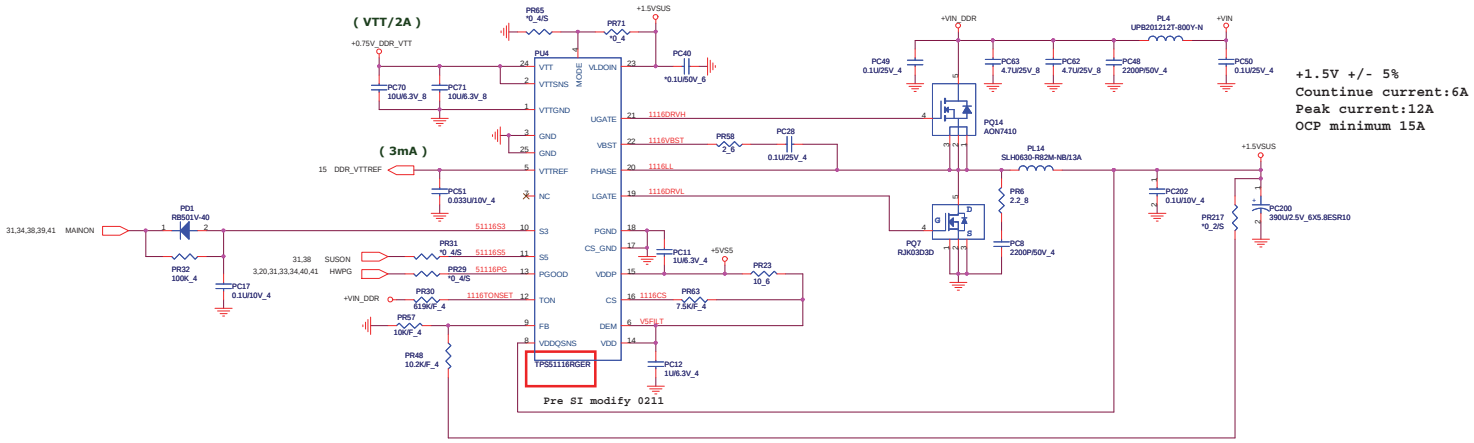




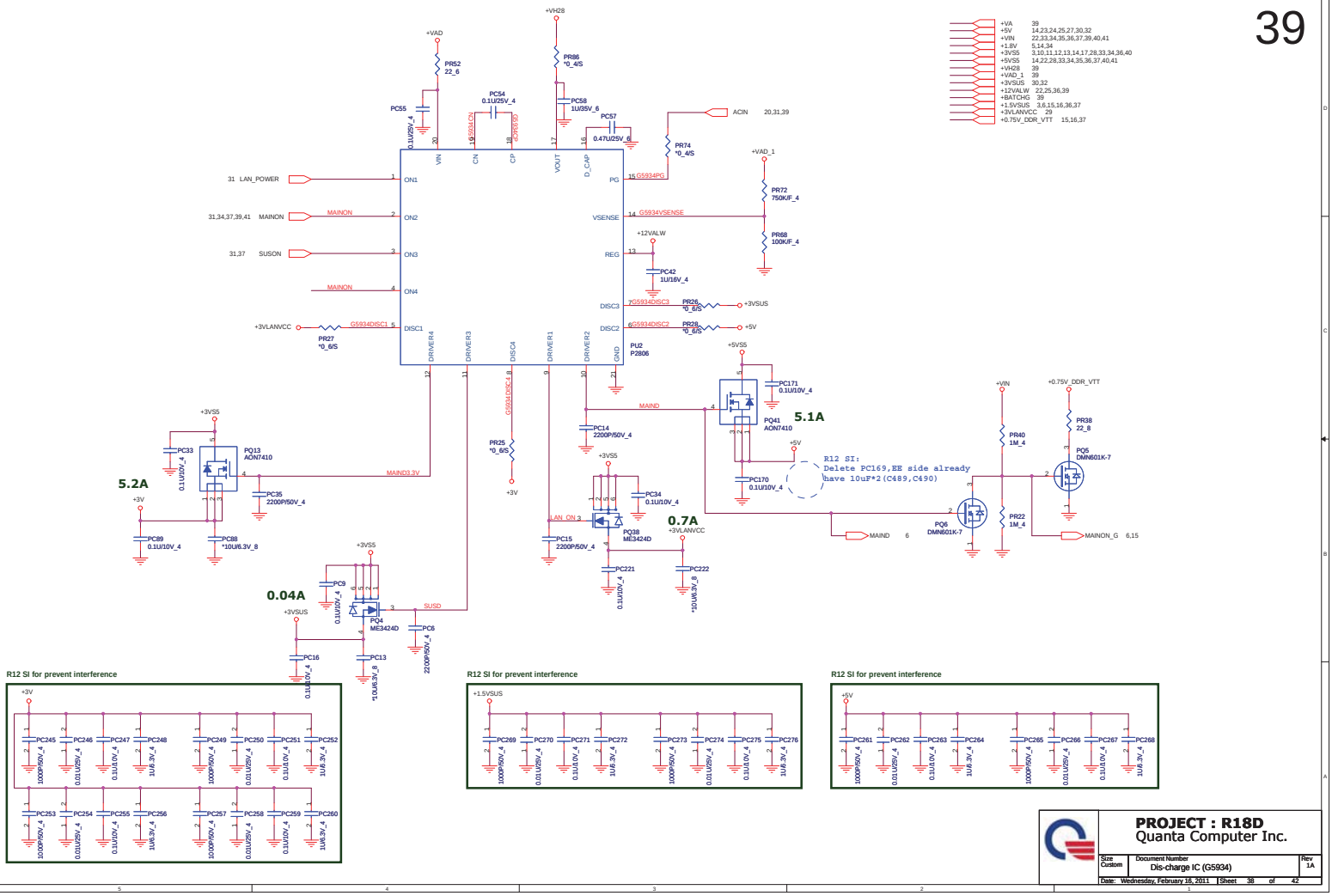
PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE (RT8208/1.8V)	1A

Date: Wednesday, February 16, 2011 | Sheet 36 of 42



PROJECT : R18D		
Quanta Computer Inc.		
Size: Custom	Document Number: DDR3 (RT8207)	Rev: 1A
Date: Wednesday, February 16, 2011	Sheet 37 of 42	



R12 SI for prevent interference

R12 SI for prevent interference

R12 SI for prevent interference

PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (G5934)	1A

Date: Wednesday, February 16, 2011 | Sheet 38 of 42

DC_JACK
90W

R12 PV:
change footprint.
R12 SI:
M/E modify.

Do Not add test pad on BATDIS_G signal

To PWR LED

Place this ZVS close to
Diode away +VIN

Place this ZVS close to
Far-Far away +VIN

Place this cap
close to EC

Place this cap
close to EC

Place this cap
close to EC

R12 SI:
M/E modify.

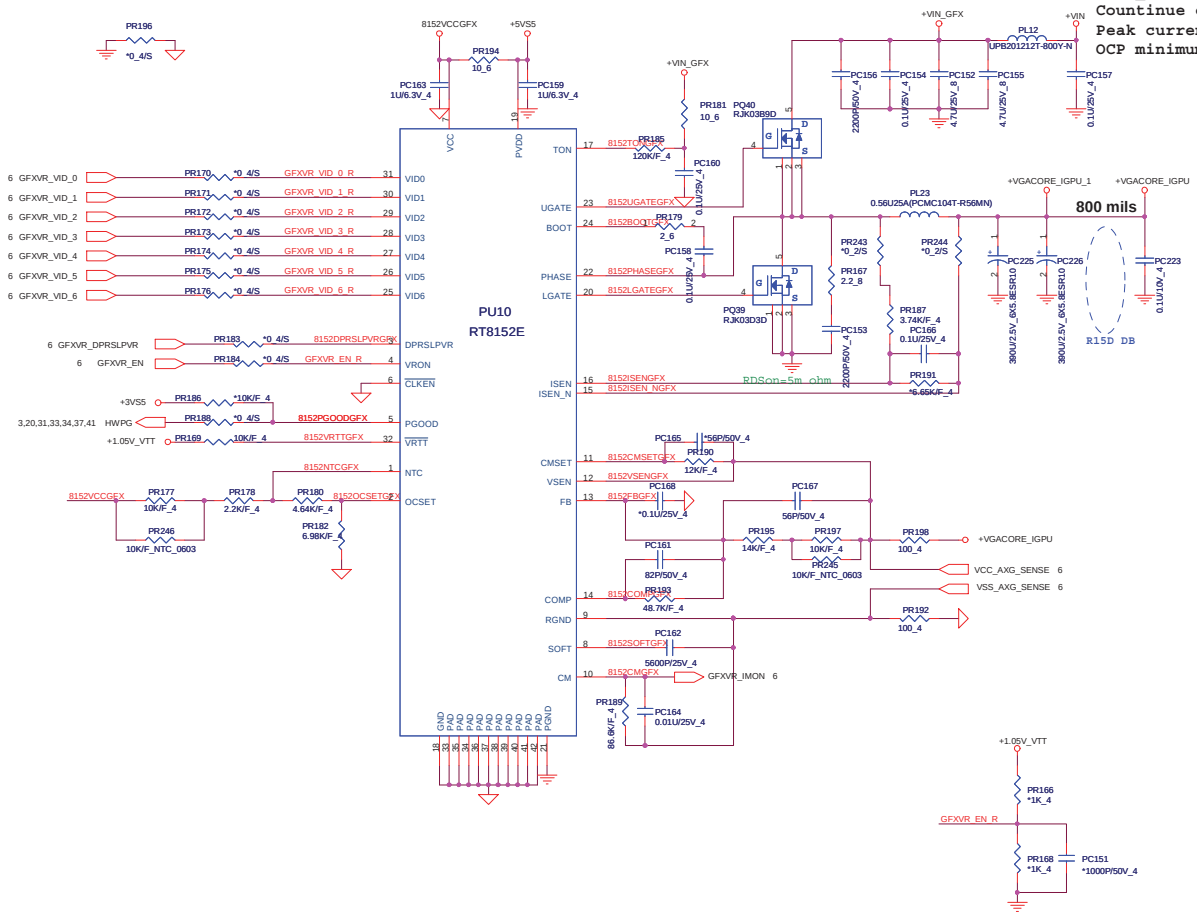
PU9
OZ8681

+VA 38
+VH28 38
+VAD_1 38
+3VPCU 10,22,30,31,33
+5VPCU 31,33
+BATCHG

PROJECT : R18D
Quanta Computer Inc.

Size: Custom | Document Number: Charger (OZ8681) | Rev: 1A
Date: Wednesday, February 16, 2011 | Sheet 39 of 42

+VGA_UMA +/- 5%
Countinue current:12A
Peak current:18A
OCP minimum 22A



PROJECT : R18D
Quanta Computer Inc.

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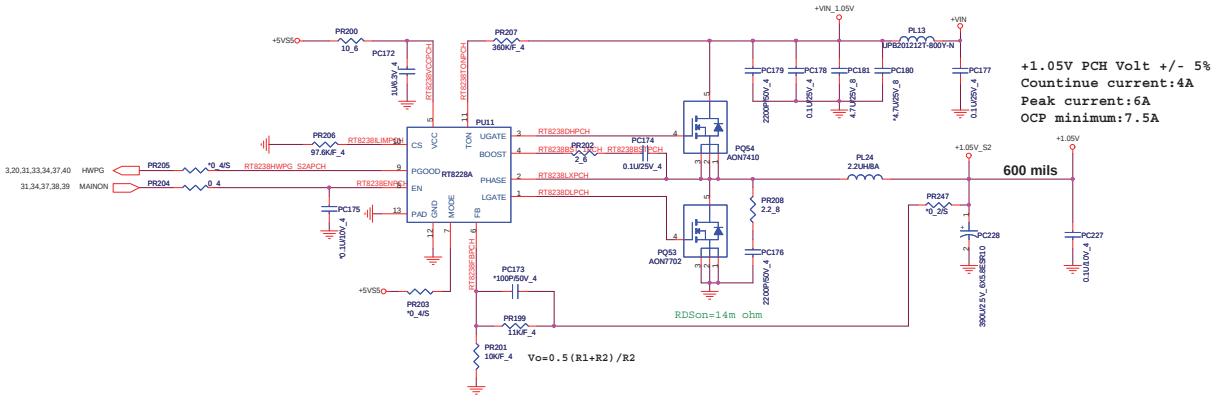

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-->Pre SI

Page 19

1.Delete L5005, C5096,C5097,C5098,C5099,C5100 and connect +SP_PLLVDD to +NV_PLLVDD

2.L5004 change to bead 220ohm (ESR=0.5) 0603.
3.C5089 change to 22uF_0805

Page 11

1.delete Q35.

Page 17

1.delete L5000 and C5074.
2.connect +3V_GFX to GPU ball AG9 with a 0.1uF cap C5075.
3.New add R5060 for test

4.L5001 change to bead 120ohm@100MHz (ESR=0.18ohm) 0603.
5.C5073 should be 4.7uF_X7R_0805.
6.C5072 should be 1uF_X7R_0603.
7.C5071 should be 0.1uF_X7R_0402.

8.PCIE change to PEX_TX0~7 and PEX_RX0~7 on GPU side for X8 lane configuration
9.unstuff R5009 and R5008 Q5002 stUff for test
9.delete L5002 for NVidai recommend

Page 18

1.L5003 change to bead 30ohm (ESR=0.01) 0603.
2.C5085 change to 1uF_X7R_0603
3.Delete C5084.

Page 21

1.R5096 and R5103 change to 162ohm_1%.

Page 31

1.New add R5105 and R5106 2.2K pull up resistors to +3V for GPUT_CLK and GPUT_DATA on EC side.

2.Delete D20,Q25,D19,R500.

Page 20

1.delete R5081,R5082,R5082.

2.New add R5085 and R5086 10K pull down resistors to GFX_CORE_CNTRL0 and GFX_CORE_CNTRL1

3.Change R5047 to 5K pull up for ROM_SCLK

4.Change R5080 to 10K for JTAG_TRST# pull down.
5.R5084 can be no stuff for JTAG_TCK
6.New add Q5010 for AC/Batt# function.

7.New add Q5011.

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C	**Change list**	2A

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