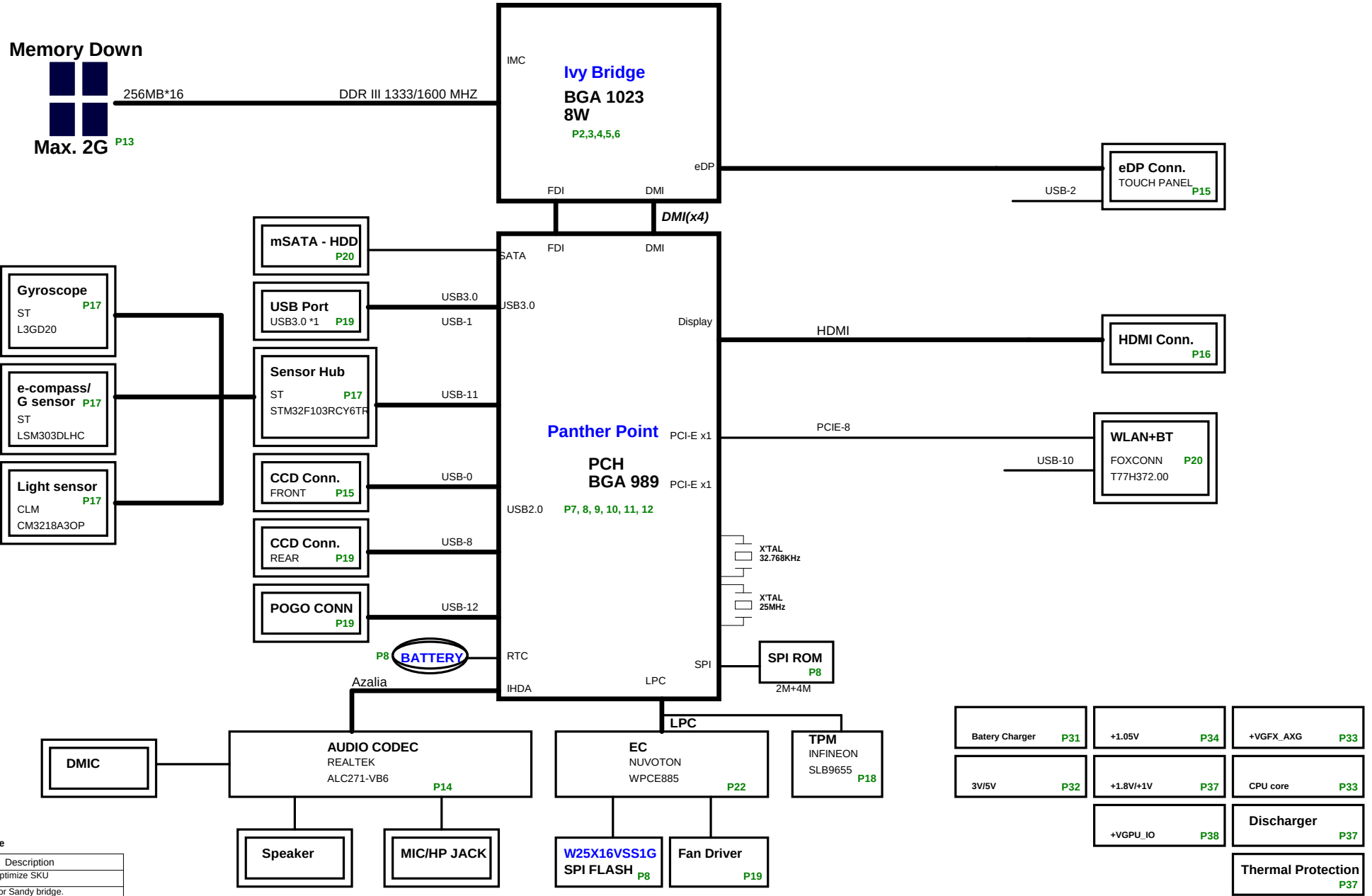
VER : 1A

Tablet SYSTEM BLOCK DIAGRAM

BOM P/N	Description



BOM Option Table

Reference	Description
EV@	Optimize SKU
SNB@	For Sandy bridge.
IVB@	For Ivy bridge.
IV@	For UMA.
*	do not stuff

Quanta Computer Inc.
PROJECT : EE3

Size	Document Number	Rev
	Block Diagram	3A

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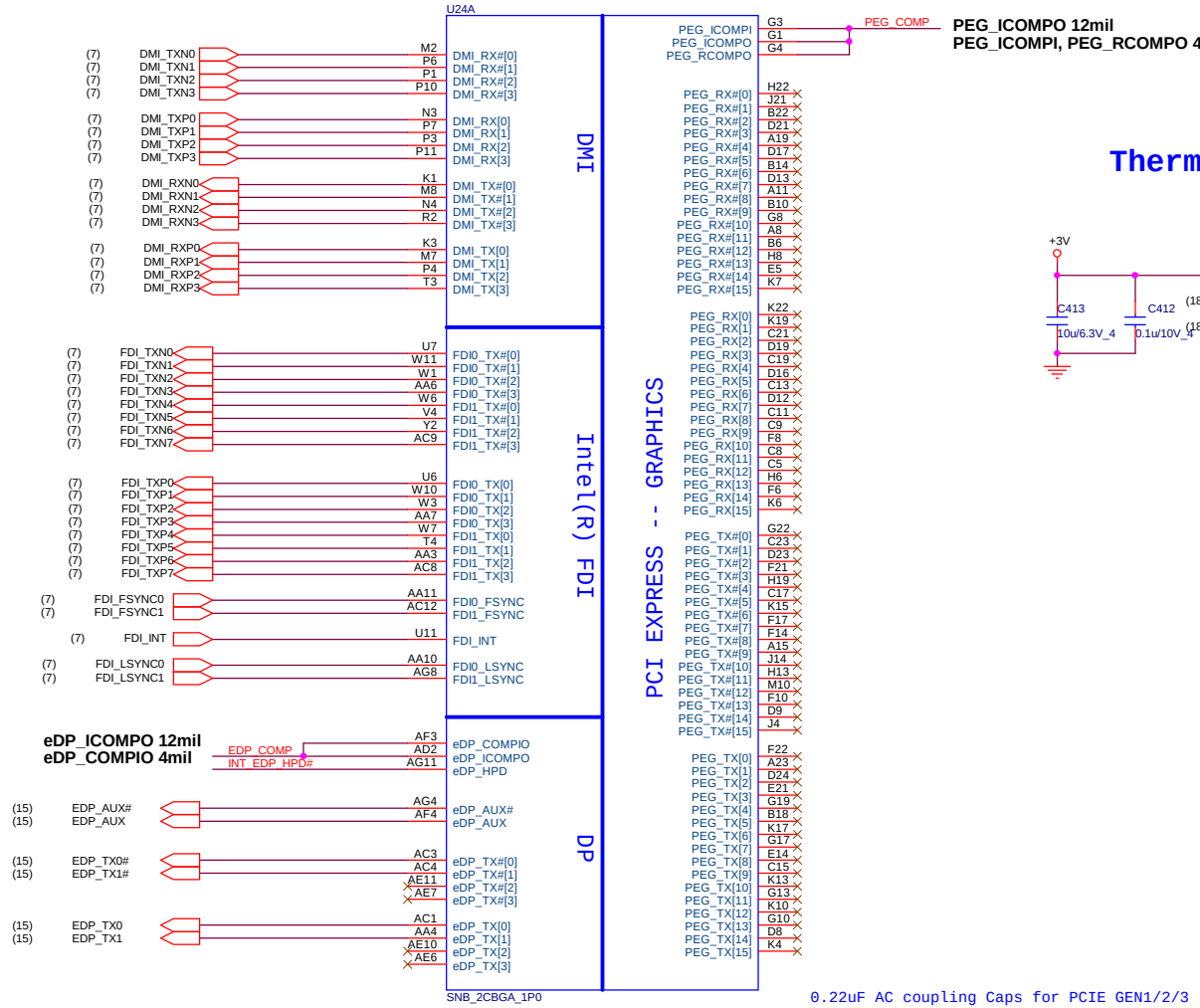
Ivy Bridge Processor (DMI,PEG,FDI)

PEG_ICOMPI and RCOMPO signals
should be shorted and routed with
- max length = 500 mils
- typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with
- max length = 500 mils
- typical impedance = 14.5 mohms

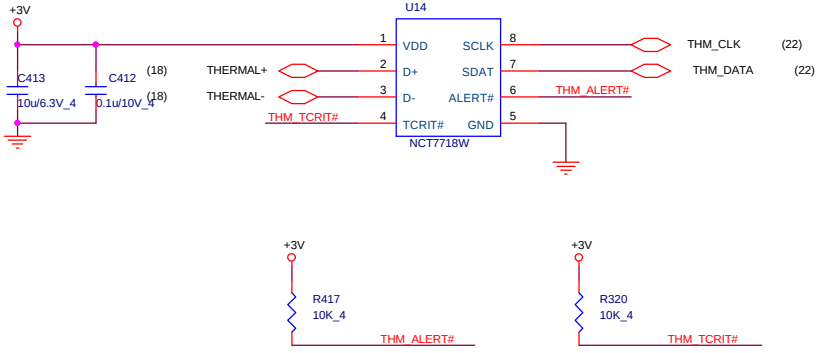


PEG_ICOMPO 12mil
PEG_ICOMPI, PEG_RCOMPO 4mil,

eDP_ICOMPO 12mil
eDP_COMPIO 4mil

0.22uF AC coupling Caps for PCIE GEN1/2/3

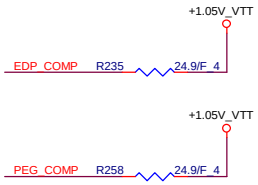
Thermal Sensor



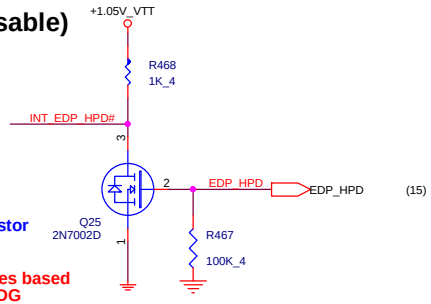
DP_COMPIO and ICOMPO signals
should be shorted near balls and routed with
- typical impedance < 25 mohms

DG 1.0 :
The recommended AC cap value is changed to 220nF for compatibility with PCIe Gen3 on future platforms.
For Gen2 only designs, it is acceptable to continue to use the 100nF capacitor.

DP & PEG Compensation



eDP Hot-plug (Disable)



CAD Note: Place PU resistor within 2 inches of CPU

HPD PU/PD resistor values based on CRB and different to DG

ALERT# Pull Up Value	Alert temperature point
2K ohm	**75 degree**
7.5K ohm	90 degree
10.5K ohm	100 degree
14K ohm	105 degree
18.7K ohm	110 degree

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PROJECT : EE3

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	Ivy Bridge 1/5	3A
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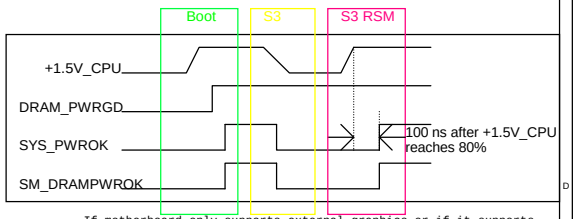
Ivy Bridge Processor (CLK,MISC,JTAG)



If motherboard only supports external graphics or if it supports Processor Graphics but without eDP:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistor

U24B

MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM

(8) H_SNB_IVB# — F49 PROC_SELECT#
TP71 — C57 PROC_DETECT#
TP95 — TP_CATERR# — C49 CATERR#
(22) EC_PECI — A48 PECI
(22,23,28) H_PROCHOT# — R512 56_4 H_PROCHOT#_R — C45 PROCHOT#
C503 2 1 *43P/50V_4N
(10) PM_THRMTRIP# — D45 THERMTRIP#

BCLK J3 — CLK_CPU_BCLKP (9)
BCLK# H2 — CLK_CPU_BCLKN (9)
DPLL_REF_CLK AG3 — TP88
DPLL_REF_CLK# AG1 — TP89
CLK_DPLL_SSCLKP (9)
CLK_DPLL_SSCLKN (9)
BCLK_ITP N59 CLK_PCIE_XDPP_R R483 *0_4 — CLK_PCIE_XDPP (9)
BCLK_ITP# N58 CLK_PCIE_XDPN_R R480 *0_4 — CLK_PCIE_XDPN (9)

Isolate Space:20mils

SM_DRAMRST# AT30 — CPU_DRAMRST# (4,22)
SM_RCOMP[0] BF44 SM_RCOMP_0 R448 140/F_4
SM_RCOMP[1] BE43 SM_RCOMP_1 R449 25.5/F_4
SM_RCOMP[2] BG43 SM_RCOMP_2 R450 200/F_4

CAD NOTE: All DDR_COMP signals should be routed such that :-
- max length = 500 mils
- trace width = 15mils and
- MB trace impedance < 68 mohms (worst case resistance)

Impedance 85ohm

PRDY# N53 XDP_PRDY# — TP69
PREQ# N55 XDP_PREQ#
TCK L56 XDP_TCLK — XDP_TCLK (8)
TMS L55 XDP_TMS — XDP_TMS (8)
TRST# J58 XDP_TRST#
TDI M60 XDP_TDI
TDO L59 XDP_TDO — XDP_TDO (8)
DBR# K58 XDP_DBRST#_R R255 0_4 — XDP_DBRST# (7)

BPM#[0] G58 — TP74
BPM#[1] E55 — TP73
BPM#[2] E59 — TP76
BPM#[3] G55 — TP70
BPM#[4] G59 — TP93
BPM#[5] H60 — TP92
BPM#[6] J59 — TP91
BPM#[7] J61 — TP90

SNB_2CBGA_1P0

Over 130 degree C will drive low

(7) PM_SYNC — C48 PM_SYNC
C493 0.1U/10V_4
(10) H_PWRGOOD — B46 UNCOREPWRGOOD
R519 10K_4
PM_DRAM_PWRGD_R — BE45 SM_DRAMPWROK
+1.05V_VTT R287 75/F_4 — TP80
CPU_PLTRST# R288 43_4 — CPU_PLTRST#_R — D44 RESET#
R289 *750/F_4

Isolate Space:20mils

Option for Prochot# function
68 ohm for unused, 62 ohm for used

+1.05V_VTT
H_PROCHOT# R520 62_4
XDP_TMS R252 51_4
TP101 XDP_TDI R254 51_4
TP97 XDP_TDO R253 51_4
XDP_PREQ# R250 *51_4
XDP_TCLK R261 51_4
TP102 XDP_TRST# R256 51_4

When MP, JTAG PU/PD resistor can be removed? (Yes Intel, TDI, TDO, TMS, TRST#, TCK,PREQ#, PRDY#)

Thermal Trip <CPU>

+1.05V_VTT
(7,28) IMVP_PWRGD — Q32 2N7002D
R508 1K_4
PM_THRMTRIP# — Q33 MMBT3904 — SYS_SHDN# (19,27,29)

s3 leakage circuit

If PM_DRAM_PWEGD connector,the R5180 must stuff.

+3V_S5
R222 *1K_4
R229 *10K_4
+1.35V_CPU
(7) SYS_PWROK
*2N7002DW Q24
PM_DRAM_PWRGD — R466 0_4

+3V_S5
C466 0.1u/10V_4
U23 74AHC1G09
4 PM_DRAM_PWRGD_Q
R228 *0_4

+1.35V_CPU
R224 200/F_4
R227 130/F_4 — PM_DRAM_PWRGD_R
R447 *39_4
Q16 *2N7002D
(5,29) MAINON_ON_G

(9,22)

+3V
C507 0.1U/10V_4
U28 74LVC1G07GW_NC
PCI_PLTRST# — CPU_PLTRST#
R290 *1.5K/F_4 — CPU_PLTRST#_R

IN	OUT
L	L
H	High-Z

Quanta Computer Inc.
PROJECT : EE3

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	Ivy Bridge 2/5	3A
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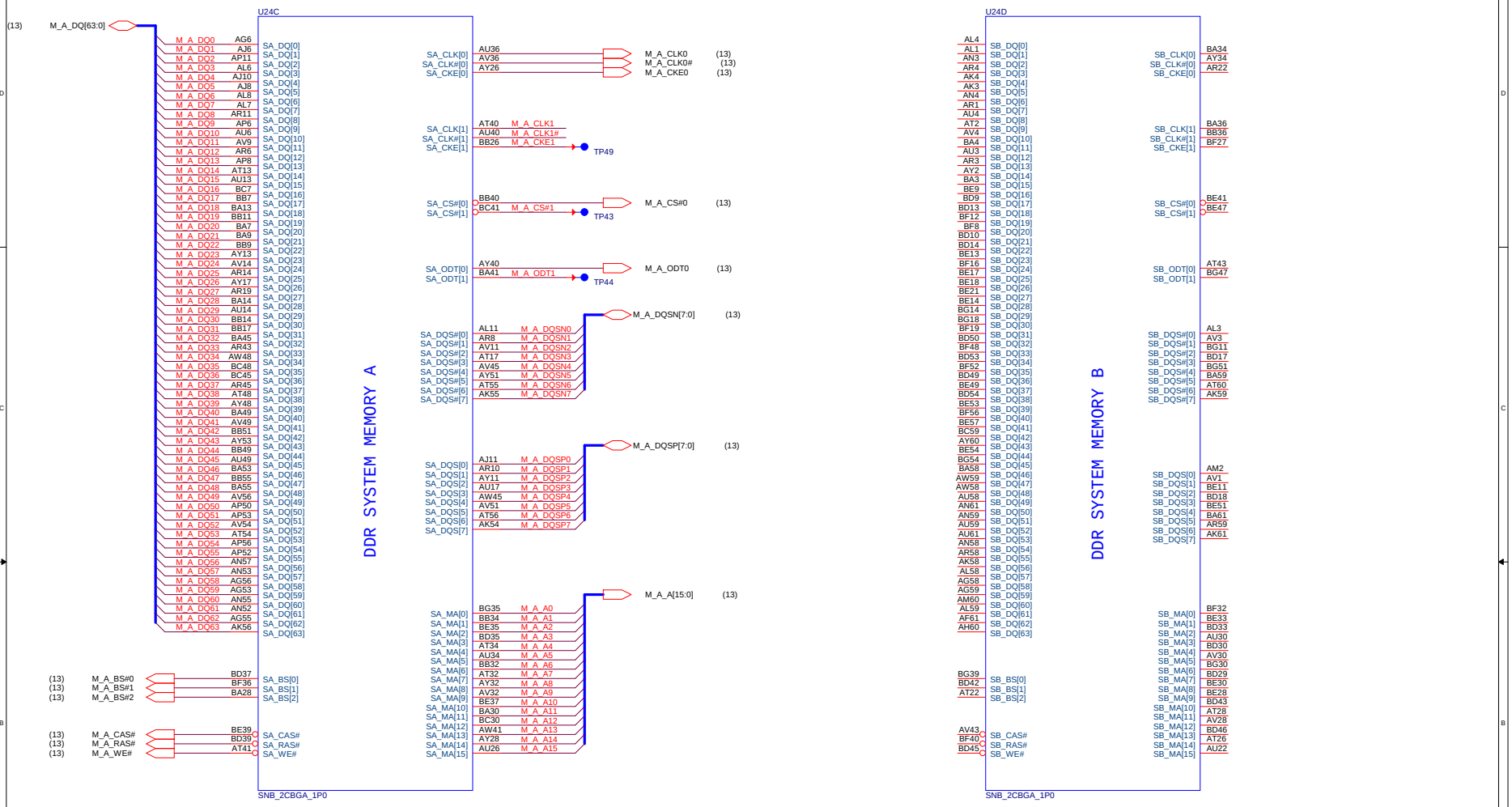
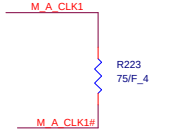
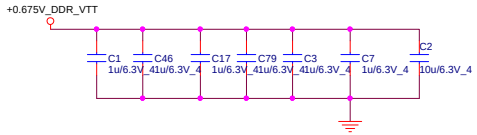
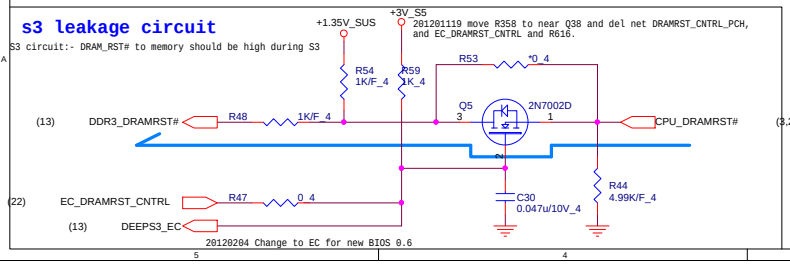
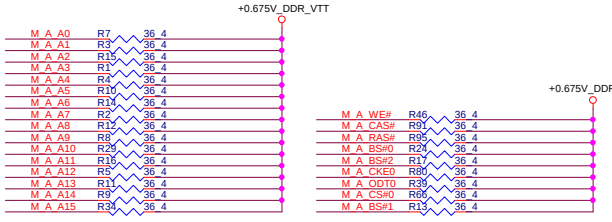
Sandy Bridge Processor (DDR3)











Quanta Computer Inc.		
PROJECT : EE3		
Size	Document Number: Ivy Bridge 3/5	Rev: 3A
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Sandy Bridge Processor (POWER)

CPU VCCIO
IVY 17W:8.5A

SNB : Spec	Cose down
330uF/6mohm x 2	330uF/6mohm x 1
10uF x 10	10uF x 10
1uF x 26	1uF x 26

CPU VCCAXG
IVY 17W:TDC 18A

Spec	Cose down
3.9mΩ/LoadlineDesign	3.9mΩ/LoadlineDesign
total : 1uF x 11	total : 1uF x 11
total : 10uF x 6	total : 10uF x 12
total : 22uF x 6	tatal : 470u x 1(power side*2)
tatal : 470u x 1(power side*2)	

CPU VDDQ
IVY 45W: 5A

Spec
330uF/6mohm x 1
10uF x 8
1uF x 10

U24F

+VCC_CORE

20120120 remove C621 for debug IC.

20120120 remove C622 for debug IC.

VCC[1] VCC[2] VCC[3] VCC[4] VCC[5] VCC[6] VCC[7] VCC[8] VCC[9] VCC[10] VCC[11] VCC[12] VCC[13] VCC[14] VCC[15] VCC[16] VCC[17] VCC[18] VCC[19] VCC[20] VCC[21] VCC[22] VCC[23] VCC[24] VCC[25] VCC[26] VCC[27] VCC[28] VCC[29] VCC[30] VCC[31] VCC[32] VCC[33] VCC[34] VCC[35] VCC[36] VCC[37] VCC[38] VCC[39] VCC[40] VCC[41] VCC[42] VCC[43] VCC[44] VCC[45] VCC[46] VCC[47] VCC[48] VCC[49] VCC[50] VCC[51] VCC[52] VCC[53] VCC[54] VCC[55] VCC[56] VCC[57] VCC[58] VCC[59] VCC[60] VCC[61] VCC[62] VCC[63] VCC[64] VCC[66] VCC[67] VCC[68] VCC[69] VCC[70] VCC[71] VCC[72] VCC[73] VCC[74] VCC[75] VCC[76]

CORE SUPPLY | PEG AND DDR | QUIET RAILS | SVID | SENSE LINES

POWER

+1.05V_VTT

8/3 Change form 7343 to 3528

VCCIO[1] VCCIO[2] VCCIO[3] VCCIO[4] VCCIO[5] VCCIO[6] VCCIO[7] VCCIO[8] VCCIO[9] VCCIO[10] VCCIO[11] VCCIO[12] VCCIO[13] VCCIO[14] VCCIO[15] VCCIO[16] VCCIO[17] VCCIO[18] VCCIO[19] VCCIO[20] VCCIO[21] VCCIO[22] VCCIO[23] VCCIO[24] VCCIO[25] VCCIO[26] VCCIO[27] VCCIO[28] VCCIO[29] VCCIO[30] VCCIO[31] VCCIO[32] VCCIO[33] VCCIO[34] VCCIO[35] VCCIO[36] VCCIO[37] VCCIO[38] VCCIO[39] VCCIO[40] VCCIO[41] VCCIO[42] VCCIO[43] VCCIO[44] VCCIO[45] VCCIO[46] VCCIO[47] VCCIO[48] VCCIO[49]

VCCIO50 VCCIO51

VCCIO_SEL

VCCPQE[1] VCCPQE[2]

VIDALERT# VIDSCLK VIDSOUT

VCC_SENSE VSS_SENSE

VCCIO_SENSE VSS_SENSE_VCCIO

IVY SPEC
22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

Voltage selection for VCCIO: this pin must be pulled high on the motherboard

On CRB
H_SNB_IVB#_PWRCTRL = low, 1.0V
H_SNB_IVB#_PWRCTRL = high/NC, 1.05V

CPU Core Power
IVY 17W:TDC 33A

IVY SPEC
1.9mΩ/LoadlineDesign
total : 2.2uF x 35
total : 22uF x 12
tatal : 470u x3(Power side*1)

Cose down
IVY SPEC
1.9mΩ/LoadlineDesign
total : 2.2uF x 35
total : 10uF x 12
tatal : 470u x1(Power side*1)

CPU VCCPL
IVY 17W:1.5A

Spec	Real
330uF/7mohm x 1	10uF x 1
1uF x 2	1uF x 2

IVY SPEC
330uF x1, 10uF_8 x1, 1uF_4 x2
Socket BOT edge.

CPU VCCSA
IVY 17W: 6A

Spec

330uF/7mohm x 1	Real
10uF x 5	10uF x 3
1uF x 5	

IVY SPEC
330uF x1, 10uF_8 x1 Socket BOT edge,
10uF_8 x2 Socket BOT cavity.

SNB_2CBGA_1P0

Sandy Bridge Processor (GRAPHIC POWER)

U24G

+VCC_GFX

VAXG[1] VAXG[2] VAXG[3] VAXG[4] VAXG[5] VAXG[6] VAXG[7] VAXG[8] VAXG[9] VAXG[10] VAXG[11] VAXG[12] VAXG[13] VAXG[14] VAXG[15] VAXG[16] VAXG[17] VAXG[18] VAXG[19] VAXG[20] VAXG[21] VAXG[22] VAXG[23] VAXG[24] VAXG[25] VAXG[26] VAXG[27] VAXG[28] VAXG[29] VAXG[30] VAXG[31] VAXG[32] VAXG[33] VAXG[34] VAXG[35] VAXG[36] VAXG[37] VAXG[38] VAXG[39] VAXG[40] VAXG[41] VAXG[42] VAXG[43] VAXG[44] VAXG[45] VAXG[46] VAXG[47] VAXG[48] VAXG[49] VAXG[50] VAXG[51] VAXG[52] VAXG[53] VAXG[54] VAXG[55] VAXG[56]

GRAPHICS | **POWER** | DDR3 - 1.5V RAILS

VAXG_SENSE VSSAXG_SENSE

SENSE LINES | 1.8V RAIL | QUIET RAILS

VCCPLL[1] VCCPLL[2] VCCPLL[3]

VCCSA[1] VCCSA[2] VCCSA[3] VCCSA[4] VCCSA[5] VCCSA[6] VCCSA[7] VCCSA[8] VCCSA[9] VCCSA[10] VCCSA[11] VCCSA[12] VCCSA[13] VCCSA[14] VCCSA[15] VCCSA[16]

SENSE LINES | SA RAIL

SNB_2CBGA_1P0

VCCAXG_SENSE/VSSAXG_SENSE R=100, Trace impedance 15.5~34.5, <25mils.

VCC_AXG_SENSE VSS_AXG_SENSE

8/3 Change form 7343 to 3528

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

SM_VREF +VDDR_REF_CPU

VDDQ[1] VDDQ[2] VDDQ[3] VDDQ[4] VDDQ[5] VDDQ[6] VDDQ[7] VDDQ[8] VDDQ[9] VDDQ[10] VDDQ[11] VDDQ[12] VDDQ[13] VDDQ[14] VDDQ[15] VDDQ[16] VDDQ[17] VDDQ[18] VDDQ[19] VDDQ[20] VDDQ[21] VDDQ[22] VDDQ[23] VDDQ[24] VDDQ[25] VDDQ[26]

20120807 Intel PDDG change

8/3 Change form 7343 to 3528

VCCDQ[1] VCCDQ[2]

20120807 Intel PDDG change

VDDQ_SENSE VSS_SENSE_VDDQ

VCCSA_SENSE

SNB_IVB# N.A at SNB EDS #27637 0.7v1

20120117 C767 for Intel fw issue, if solve need un-stuff.

VCCSA_VID0 VCCSA_VID1

A 1-K pull-down resistor should be placed on the VCCSA VID lines. This will ensure the VID is 00 prior to VCCIO stability..

R94 for SN Bridge

S3	STUFF	NO_STUFF
enable	-	R5347/R6362
disable	R5347/R6362	-

S3 circuit: 1.5V input to IVB is gated & IVB Read Vref 0.75V is gated

20120807 Intel PDDG change 4.5A

20120807 Intel PDDG change to 1.35V

For SN Bridge

VID[1]	+VCCSA
0	0.9V
1	0.8V

For IV Bridge

VID[0]	VID[1]	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

Layout note: need routing together and ALERT need between CLK and DATA

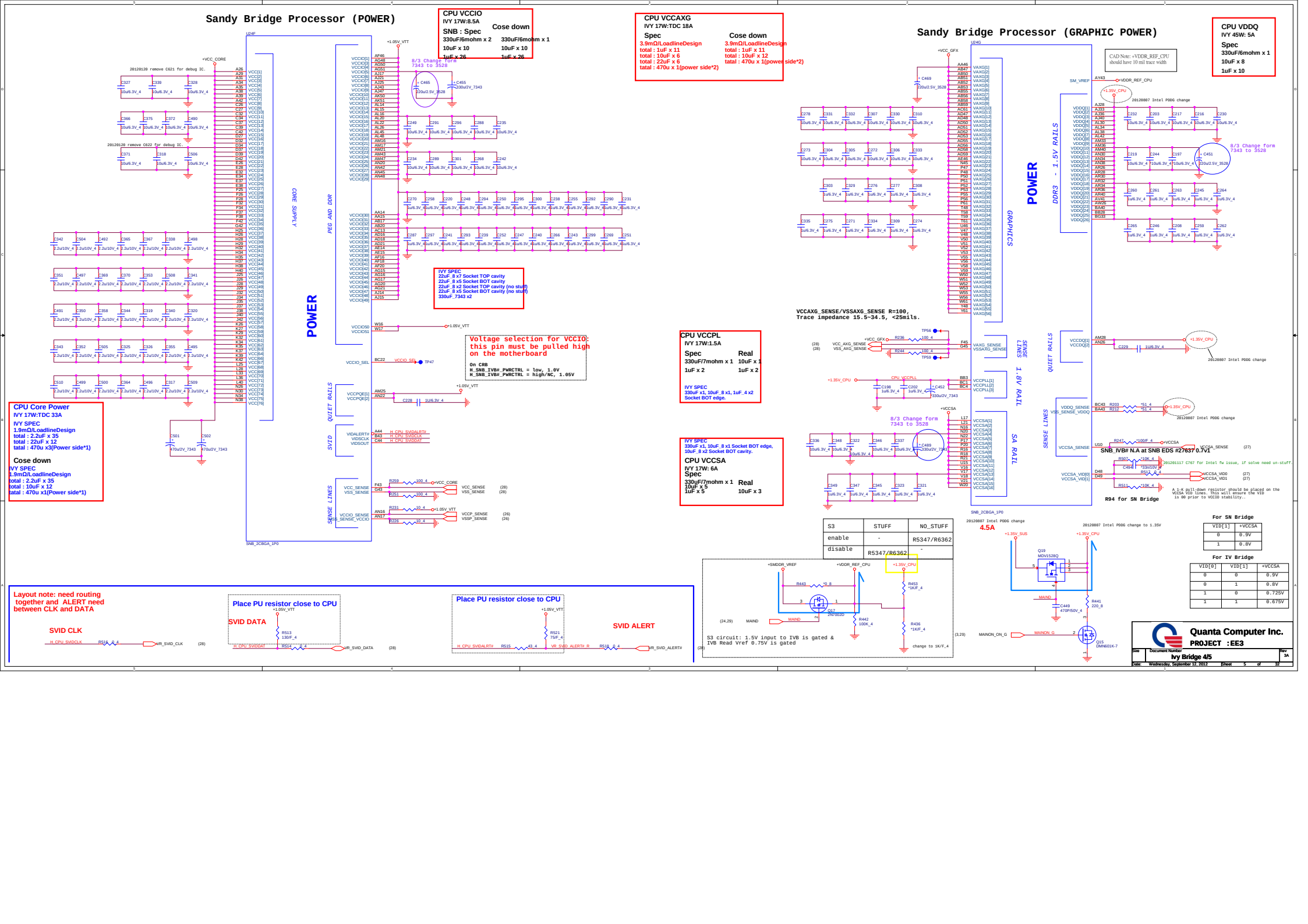
SVID CLK

Place PU resistor close to CPU

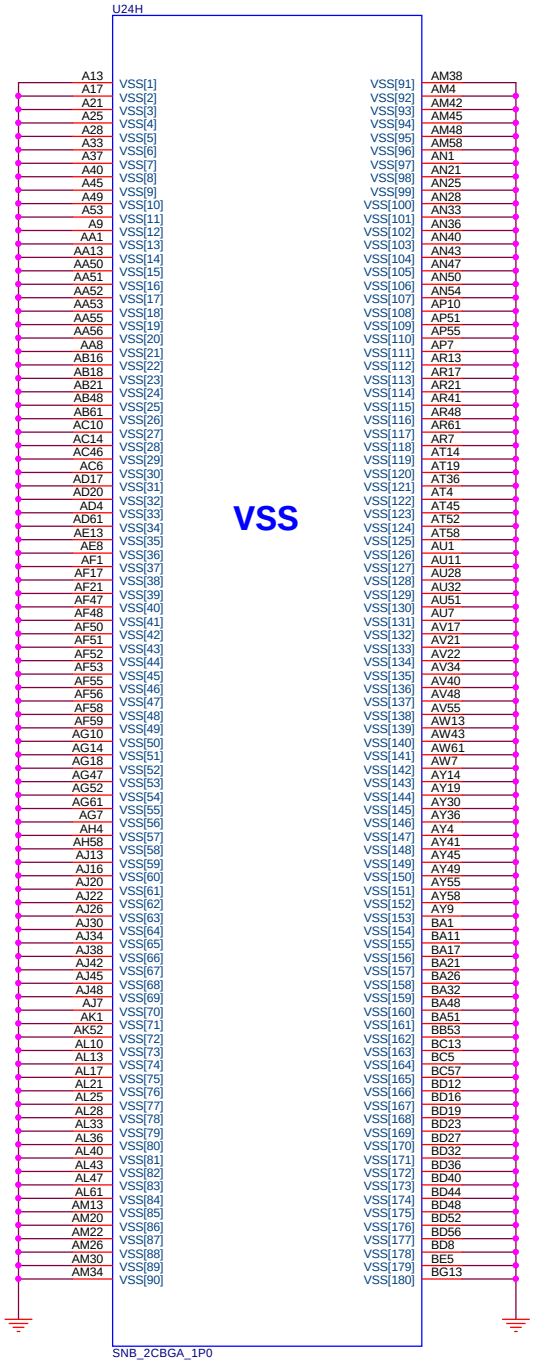
SVID DATA

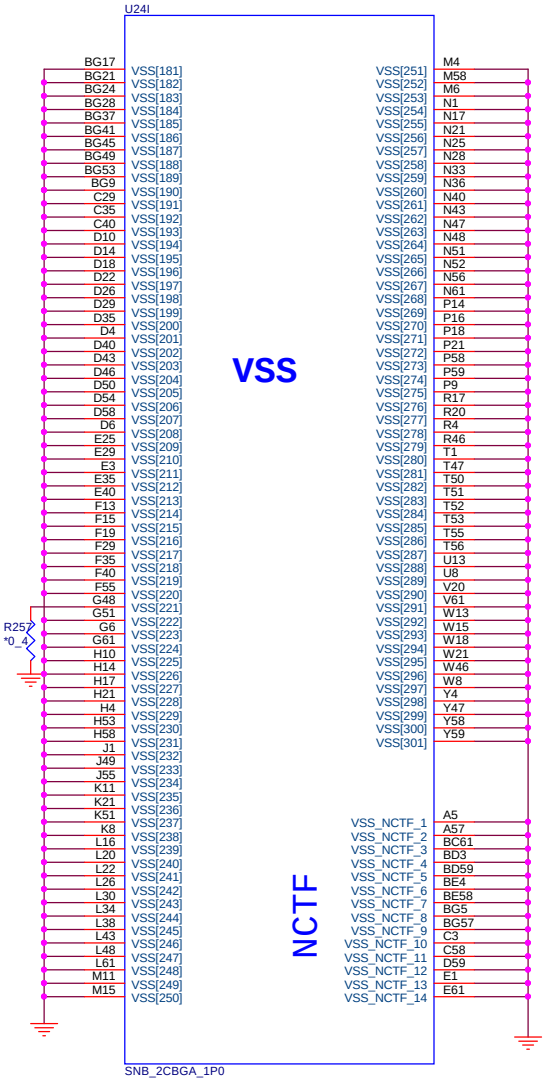
Place PU resistor close to CPU

SVID ALERT

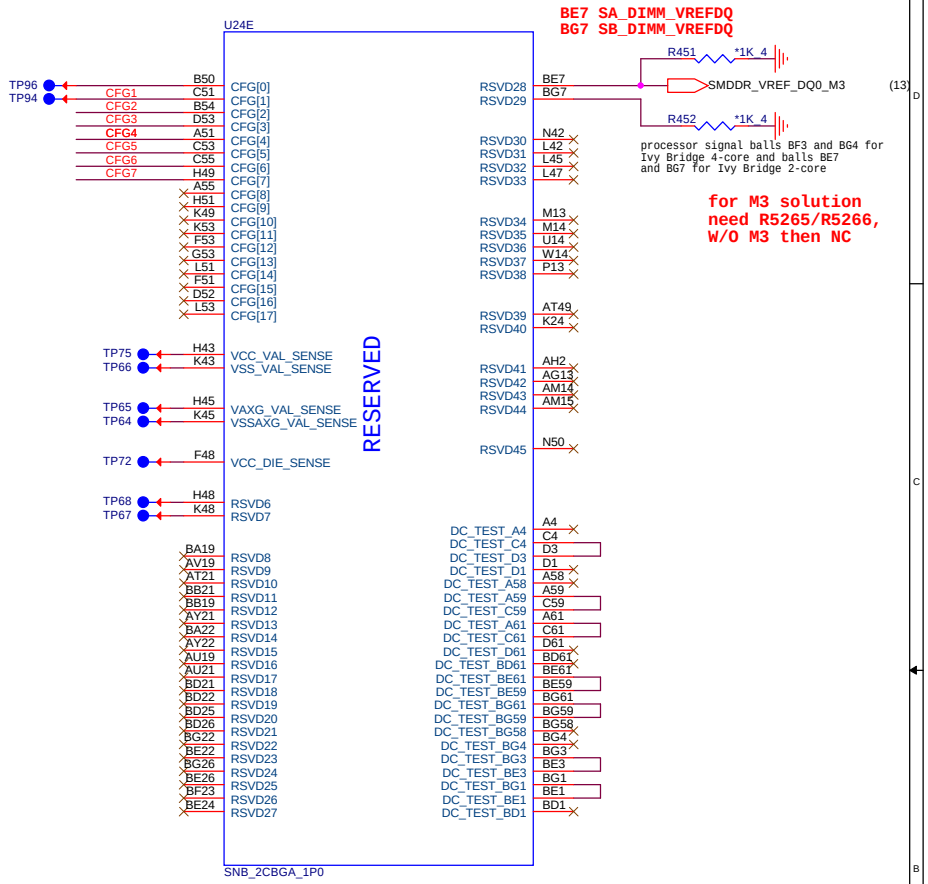


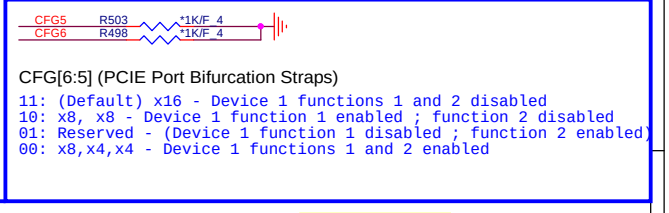
Sandy Bridge Processor (GND)





Sandy Bridge Processor (RESERVED, CFG)





Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	**Lane Reversed**
CFG3 (PCI-E Static x4 Lane Reversal)	**Normal Operation**	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	**Enable; An ext DP device is connected to eDP**
CFG7 (PEG Defer Training)	**PEG train immediately following xxRESETB de assertion**	PEG wait for BIOS training

Quanta Computer Inc.
PROJECT : EE3

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	Ivy Bridge 5/5	3A

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CPT/PPT (DMI,FDI,PM)

U21C

Need notice BIOS if DMI or FDI reverse.

DMI0RXN BC24
DMI1RXN BE20
DMI2RXN BG18
DMI3RXN BG20
DMI0RXP BE24
DMI1RXP BC20
DMI2RXP BJ18
DMI3RXP BJ20
DMI0TXN AW24
DMI1TXN AW20
DMI2TXN BB18
DMI3TXN AV18
DMI0TXP AY24
DMI1TXP AY20
DMI2TXP AY18
DMI3TXP AU18
DMI_ZCOMP BJ24
DMI_IRCOMP BG25
DMI2RBIAS BH21
+1.05V_VTT R486 49.9/F_4 DMI_COMP
R485 750/F_4

DMI

FDI_RXN0 BJ14
FDI_RXN1 AY14
FDI_RXN2 BE14
FDI_RXN3 BH13
FDI_RXN4 BC12
FDI_RXN5 BJ12
FDI_RXN6 BG10
FDI_RXN7 BG9
FDI_RXP0 BG14
FDI_RXP1 BB14
FDI_RXP2 BF14
FDI_RXP3 BG13
FDI_RXP4 BE12
FDI_RXP5 BG12
FDI_RXP6 BJ10
FDI_RXP7 BH9
FDI_INT AW16
FDI_FSYNC0 AV12
FDI_FSYNC1 BC10
FDI_LSYNC0 AV14
FDI_LSYNC1 BB10

FDI_TXN0 (2)
FDI_TXN1 (2)
FDI_TXN2 (2)
FDI_TXN3 (2)
FDI_TXN4 (2)
FDI_TXN5 (2)
FDI_TXN6 (2)
FDI_TXN7 (2)
FDI_TXP0 (2)
FDI_TXP1 (2)
FDI_TXP2 (2)
FDI_TXP3 (2)
FDI_TXP4 (2)
FDI_TXP5 (2)
FDI_TXP6 (2)
FDI_TXP7 (2)
FDI_INT (2)
FDI_FSYNC0 (2)
FDI_FSYNC1 (2)
FDI_LSYNC0 (2)
FDI_LSYNC1 (2)

FDI

20111102 FDI reverse
20111111 FDI change to normal

System Power Management

20110214 add SUSWAEN to SUSACK connector.

SUSWARN#_R R395 0_4
(22) SUSACK# R369 *0_4 SUSACK#_R C12
(3) XDP_DBRST# XDP_DBRST# K3
C178 *1U/10V_4
SYS_PWROK R184 0_4 SYS_PWROK_R P12
R173 *0_4 R166 0_4 EC_PWROK_R L22
PWROK_EC R160 0_4 R150 *0_4 APWROK_R L10
(3) PM_DRAM_PWRGD PM_DRAM_PWRGD B13
(22) PCH_RSMRST# PCH_RSMRST# C21
(20,22) IOAC_PCIERST# R370 *0_4 SUSWARN#_R K16
(22) DNBSWON# E20
TP24
(23) ACPRESENT ACPRESENT H20
PM_BATLOW# E10
PM_RI# A10

SUSACK# SYS_RESET# SYS_PWROK PWROK APWROK DRAMPWROK RSMRST# SUSWARN#/SUSPWRDNACK/GPIO30 PWRBTN# ACPRESENT / GPIO31 BATLOW# / GPIO72 RI#

+3V
+3V_S5
+3V_S5
+3V_S5
+3V_S5
DSW
+3V_S5
+3V_S5

CLKRUN# / GPIO32 N3 CLKRUN# (18,22)
SUS_STAT# / GPIO61 G8 TP31
SUSCLK / GPIO62 N14 PCH_SUSCLK TP41
SLP_S5# / GPIO63 D10 TP20
SLP_S4# H4 SUSC# (22)
SLP_S3# F4 SUSB# (22)
SLP_A# G10 SLP_A# TP29
SLP_SUS# G16 SLP_SUS# SLP_SUS# (11,22)
PMSYNCH AP14 PM_SYNC (3)
SLP_LAN# / GPIO29 K14 SLP_LAN#

DSWVREN A18 DSWVREN (8)
DPWROK E22 DPWROK_R R349 0_4 DPWROK (22)
WAKE# B9 PCIE_WAKE#_LAN

DPWROK need to be shorted to RSMRST# when Deep S4/S5 state is not support
20120104 change DPWROK from PCH_Rsmrst# to EC control.

Panther Point_R1P0

CPT/PPT (LVDS,DDI)

U21D

(15) INT_LVDS_BLON J47 L_BKLTEN
(15) INT_LVDS_DIGON M45 L_VDD_EN
(15) INT_LVDS_BRIGHT P45 L_BKLTCTL
T40 K47 L_DDC_CLK L_DDC_DATA
T45 P39 L_CTRL_CLK L_CTRL_DATA
AF37 AF36 LVD_IBG LVD_VBG
AE48 AE47 LVD_VREFH LVD_VREFL
AK39 AK40 LVDSA_CLK# LVDSA_CLK
AN48 AM47 AK47 AJ48 LVDSA_DATA#0 LVDSA_DATA#1 LVDSA_DATA#2 LVDSA_DATA#3
AN47 AM49 AK49 AJ47 LVDSA_DATA0 LVDSA_DATA1 LVDSA_DATA2 LVDSA_DATA3
AF40 AF39 LVDSB_CLK# LVDSB_CLK
AH45 AH47 AF49 AF45 LVDSB_DATA#0 LVDSB_DATA#1 LVDSB_DATA#2 LVDSB_DATA#3
AH43 AH49 AF47 AF43 LVDSB_DATA0 LVDSB_DATA1 LVDSB_DATA2 LVDSB_DATA3

LVDS

UM77 VGA/LVDS disable

N48 P49 T49 CRT_BLUE CRT_GREEN CRT_RED
T39 M40 CRT_DDC_CLK CRT_DDC_DATA
M47 M49 CRT_HSYNC CRT_VSYNC
DAC_IREF T43
T42 DAC_IREF CRT_IRTN
R460 1K/F_4
1% or 5%

CRT

Panther Point_R1P0

SDVO_TVCLKINN AP43
SDVO_TVCLKINP AP45
SDVO_STALLN AM42
SDVO_STALLP AM40
SDVO_INTN AP39
SDVO_INTP AP40
SDVO_CTRLCLK P38
SDVO_CTRLDATA M39
DDPB_AUXN AT49
DDPB_AUXP AT47
DDPB_HPD AT40
DDPB_0N AV42
DDPB_0P AV40
DDPB_1N AV45
DDPB_1P AV46
DDPB_2N AU48
DDPB_2P AU47
DDPB_3N AV47
DDPB_3P AV49
DDPC_CTRLCLK P46
DDPC_CTRLDATA P42
DDPC_AUXN AP47
DDPC_AUXP AP49
DDPC_HPD AT38
DDPC_0N AT47
DDPC_0P AY49
DDPC_1N AY43
DDPC_1P AY45
DDPC_2N BA47
DDPC_2P BA48
DDPC_3N BB41
DDPC_3P BB49
DDPD_CTRLCLK M43
DDPD_CTRLDATA M36
DDPD_AUXN AT45
DDPD_AUXP AT43
DDPD_HPD BH41
DDPD_0N BB43
DDPD_0P BB45
DDPD_1N BF44
DDPD_1P BE44
DDPD_2N BF42
DDPD_2P BE42
DDPD_3N BJ42
DDPD_3P BG42

Digital Display Interface

HDMI_DDCCLK_SW (16)
HDMI_DDCDATA_SW (16)
HDMI_HP (16)
INT_HDMITX2N_C AV42 INT_HDMITX2N_C (16)
INT_HDMITX2P_C AV40 INT_HDMITX2P_C (16)
INT_HDMITX1N_C AV45 INT_HDMITX1N_C (16)
INT_HDMITX1P_C AV46 INT_HDMITX1P_C (16)
INT_HDMITX0N_C AU48 INT_HDMITX0N_C (16)
INT_HDMITX0P_C AU47 INT_HDMITX0P_C (16)
INT_HDMICLK-_C AV47 INT_HDMICLK-_C (16)
INT_HDMICLK+_C AV49 INT_HDMICLK+_C (16)

INT. HDMI

DisplayPort C
DisplayPort D

PCH Pull-high/low(CLG)

+3V
+3V_S5
CLKRUN# R439 8.2K_4
XDP_DBRST# R424 4.99K/F_4
R430 *1K_4
PCH_RSMRST# R350 10K_4
SYS_PWROK R180 *10K_4
PM_RI# R347 10K_4
PM_BATLOW# R101 8.2K_4
PCIE_WAKE#_LAN R368 10K_4
SLP_LAN# R115 *10K_4
SUSWARN#_R R333 10K_4
ACPRESENT R55 *10K_4
PM_DRAM_PWRGD R335 200/F_4
wo S3 leakage, un-stuff R5180

System PWR_OK(CLG)

IMVP_PWRGD PU +3V
PWROK_EC PD
so AND gate output dont need PD again

+3V_S5
C415 0.1u/10V_4
to PCH Pin12, XDP and EE debug
(3) SYS_PWROK
U7 TC7SH08FU
PWROK_EC (22)
R79 100K_4
R52 *0_4

IMVP_PWRGD_R
U13 *TC7SH08
IMVP_PWRGD (3,28)
GFX_PWRGD (22,28)
C436 *0.1U/10V_4
R92 0_4
20111128 add 0ohm to passed IMVP_PERGD
include GFX_PWRGD to SYS_PWROK for PCH check

20121013 ADD FWSC for 200msce timing.
(22) FWSC
(22,25) +0.75V_ON
R559 0_4
R159 *0_4 APWROK_R
R140 10K_4

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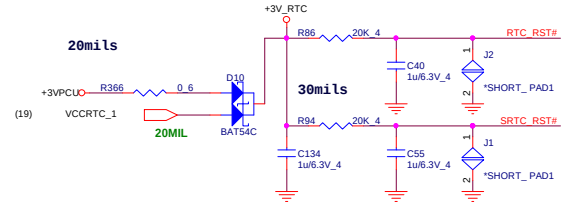
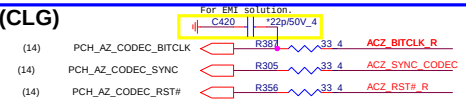
PCH2(CLG)

CPT/PPT (HDA,JTAG,SATA)

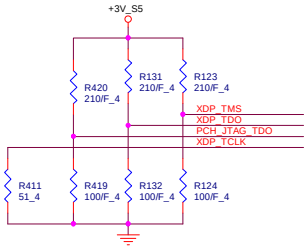
RTC Circuitry(RTC)



HDA Bus(CLG)

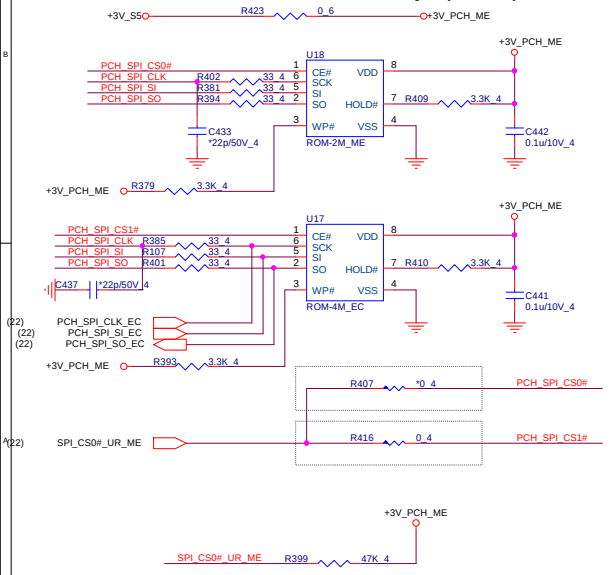


PCH JTAG Debug (CLG)

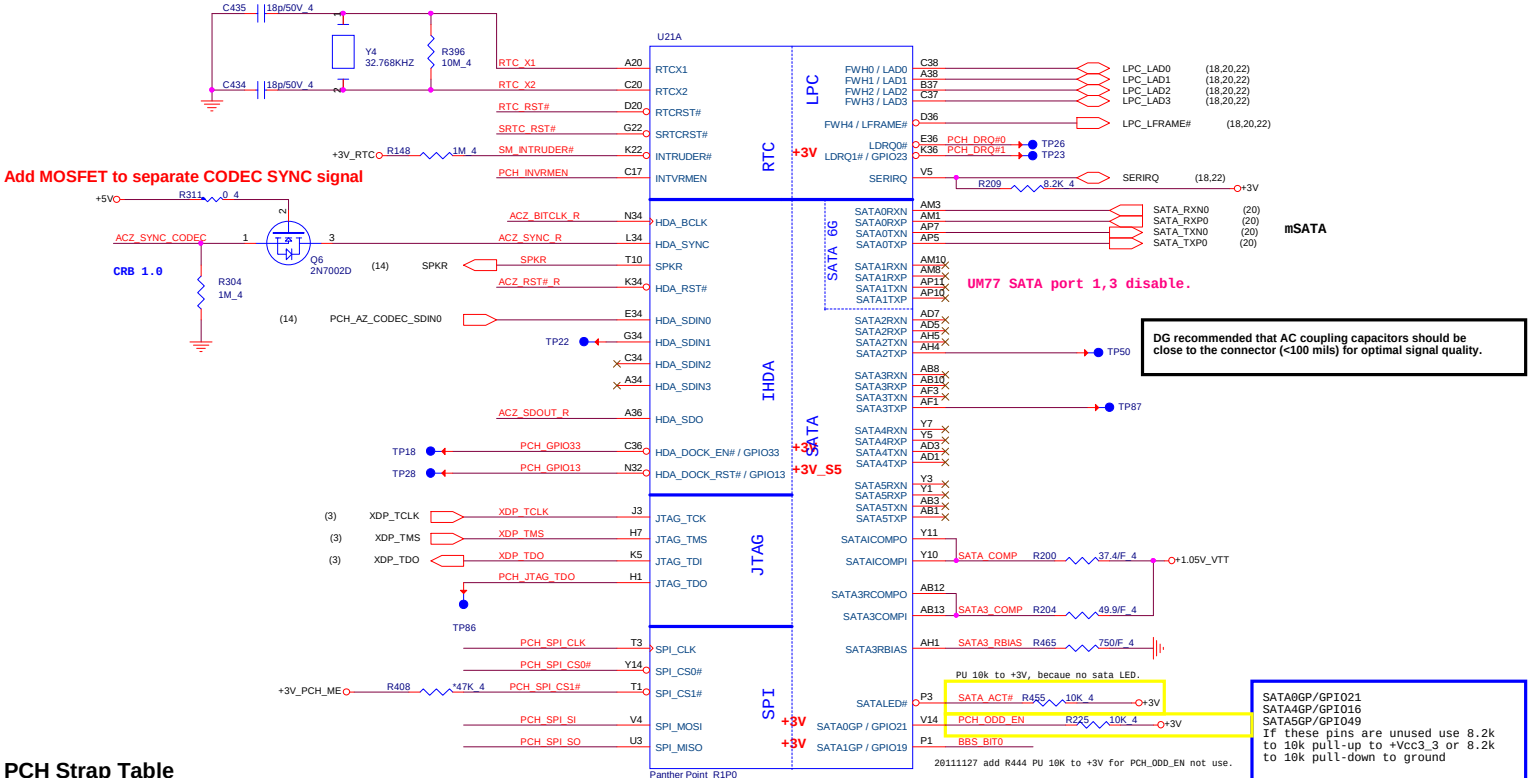


PCH Dual SPI (CLG)

W25Q32BVSSIG / AKE391P0N00------>4MB
AKE39GN0Q00 (realtek)
W25Q16BVSSIG / AKE38FP0N01-----><2MB
AKE38GN0Q00 (realtek)



Add MOSFET to separate CODEC SYNC signal



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI *; 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SDO	Flash Descriptor Security	RSMRST	0 = effect (default)(weak pull-down 20K) 1 = overridden
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss (weak pull-down 20K) 1 = Set to Vcc
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite internal PD	RSMRST	0 = Disable (Default) 1 = Enable
DSWVREN	DEEP S4/S5 well On Die DSW VR Enable	DSW	High = Enable (Default) Low = Disable
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)

Used as GPIO only. at chklist 1.2

Default weak pull-up on GNT0/1#
[Need external pull-down for LPC BIOS]

ME_WR default EC setting folating

for future CPU, Sandy Bridge NC
DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kOhm ±5% - R8361 change to 0 or not??

Needs to be pulled High for Huron River platform.
chklist 1.2

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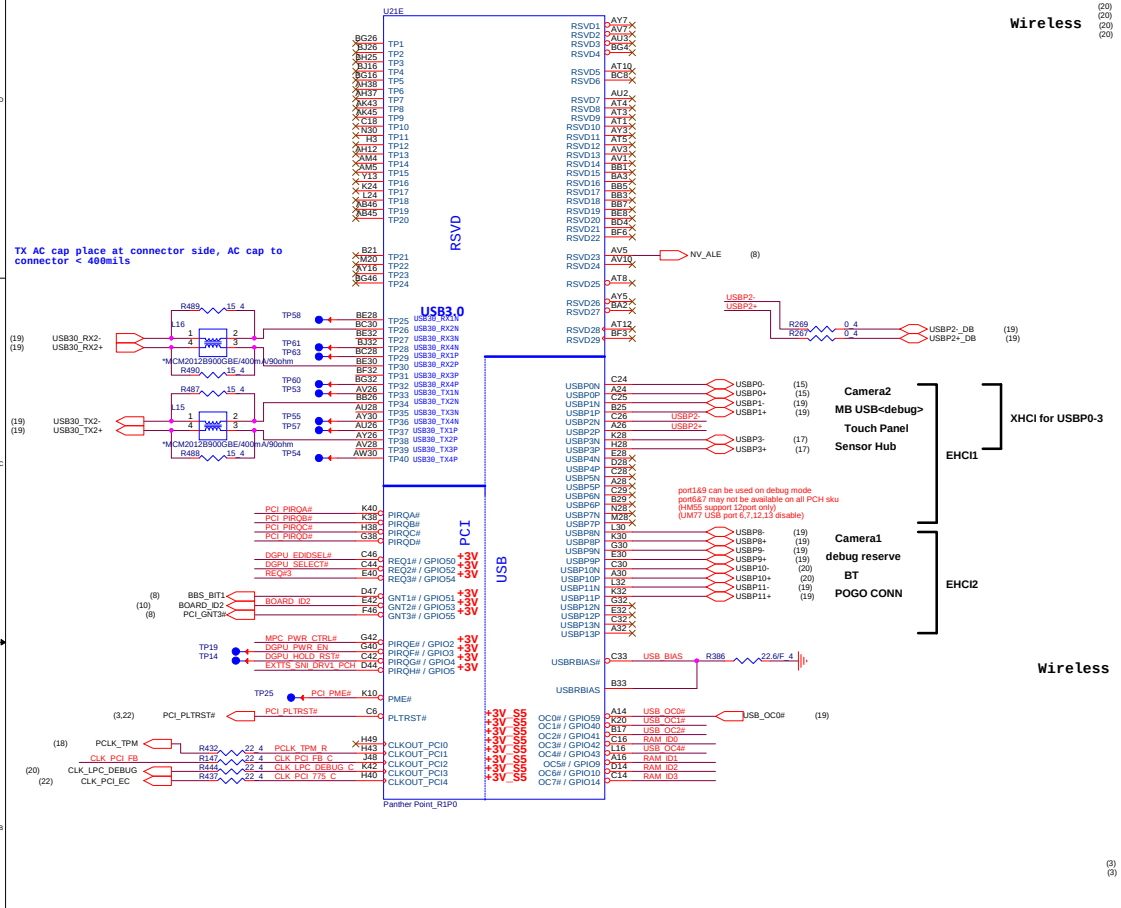
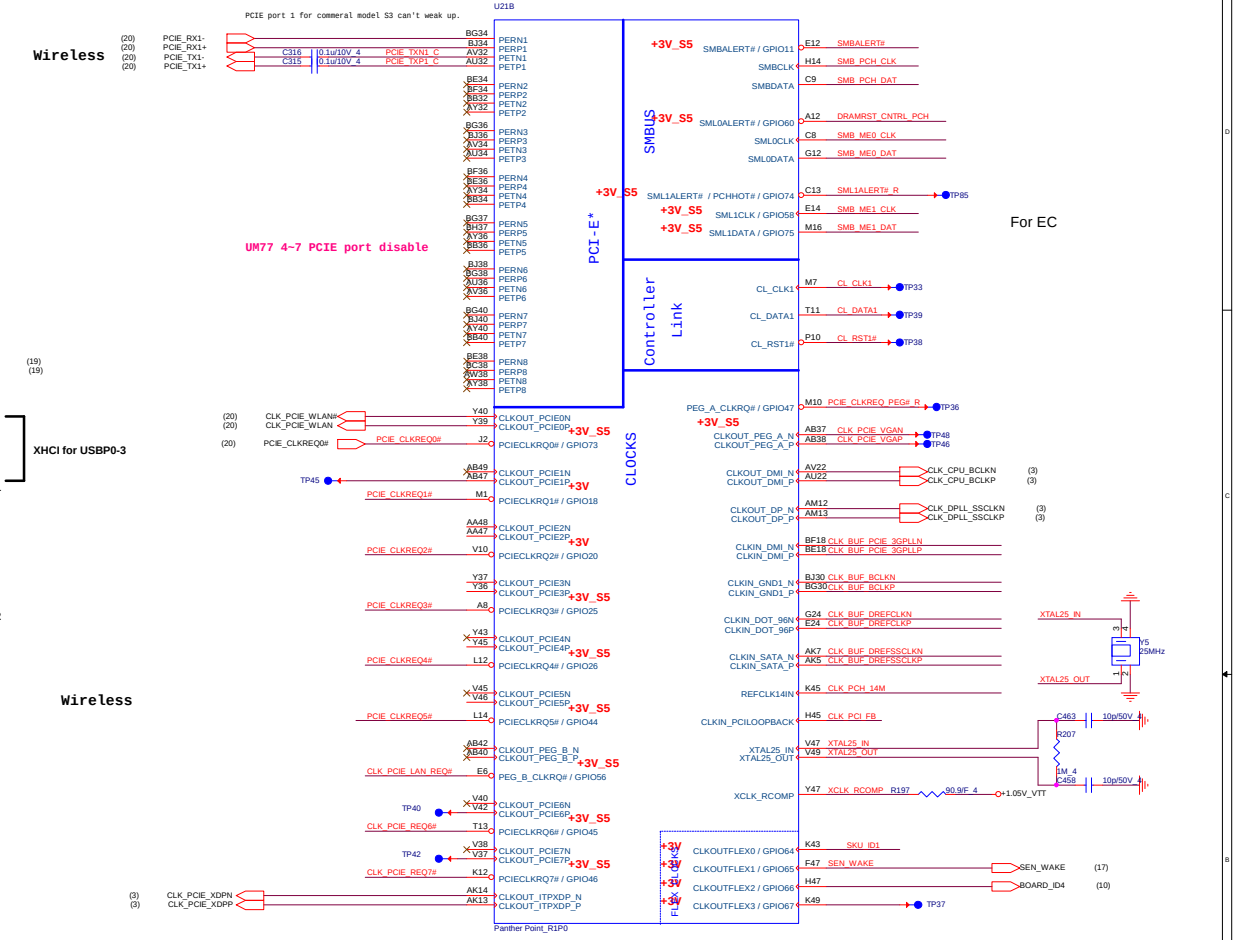
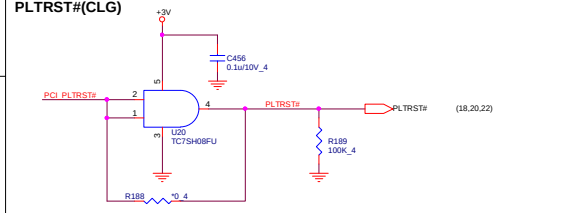
CPT/PPT (PCI,USB,NVRAM)



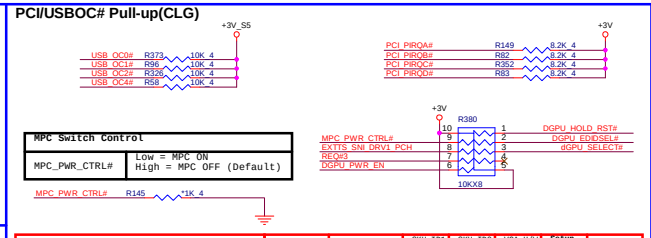
CPT/PPT (PCI-E,SMBUS,CLK)



PLTRST#(CLG)

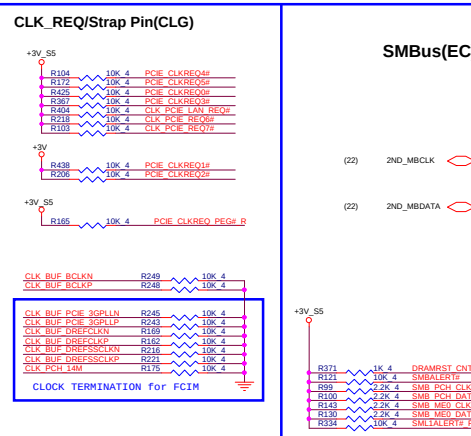


PCI/USBOC# Pull-up(CLG)

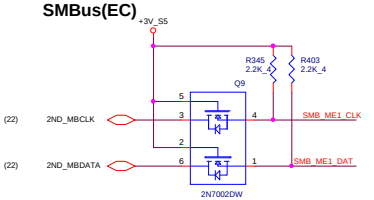


		SKU_ID1 (GPIO64)	SKU_ID0 (GPIO16)	VGA H/W Signal	Setup Menu	
UMA Only		0	0	UMA	Hidden	UMA boot
dGPU Only		0	1	GPU	Hidden	GPU boot
Switchable (Mux)		1	0	UMA+GPU	dGPU/SG	UMA boot
Optimize (Muxless)		1	1	UMA	UMA/SG	UMA boot

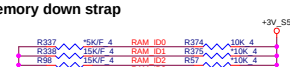
CLK_REQ/Strap Pin(CLG)



SMBus(EC)



DDRIII Memory down strap



RAM	RAM_ID0	RAM_ID1	RAM_ID2	RAM_ID3
Hynix 1333 sku1	0	0	0	0
Elpida 1333 sku3, 4	1	0	0	0
Elpida 1600 sku2	0	1	0	0

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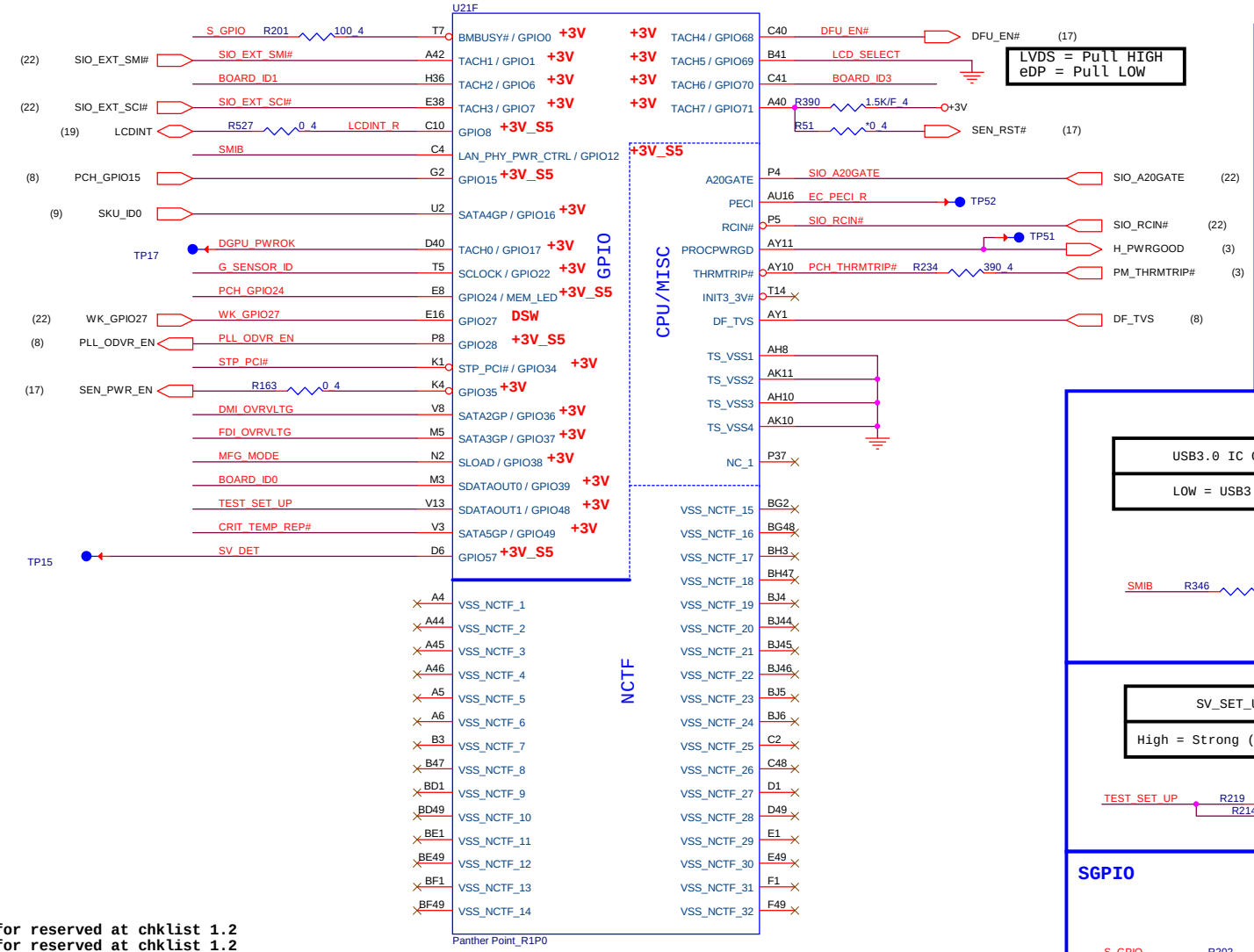
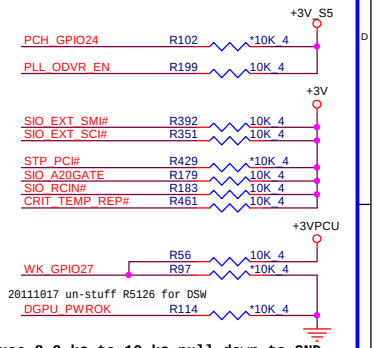
CPT/PPT (GPIO,VSS_NCTF,RSVD)



LVDS = Pull HIGH
eDP = Pull LOW

(17) DFU_EN#
(22) SIO_A20GATE
(22) SIO_RCIN#
(3) H_PWRGOOD
(3) PM_THRMTRIP#
(8) DF_TVS
(17) SEN_RST#

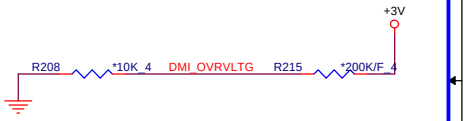
GPIO Pull-up/Pull-down(CLG)

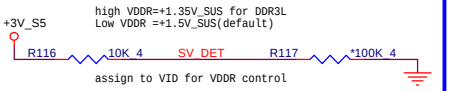


GPIO27 : If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

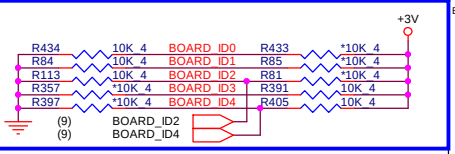
USB3.0 IC CTL
LOW = USB3.0 IC

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)





SV_SET_UP
High = Strong (Default)

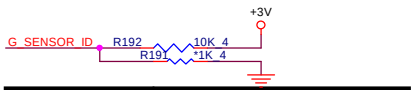


Board_ID4 Hight=Symatic, LOW=ELAN.
Board_ID1 Hight=non-TPM, LOW=TPM

SGPIO

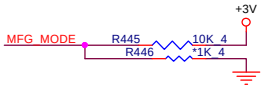
SATA2GP : strap for reserved at chklist 1.2
SATA3GP : strap for reserved at chklist 1.2
NOTE: The internal pull-down is disabled after PLTRST# deasserts.
NOTE: This signal should not be pulled high when strap is sampled.

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage



G_SENSOR_ID	High = Disable (Default) Low = Enable

MFG-TEST



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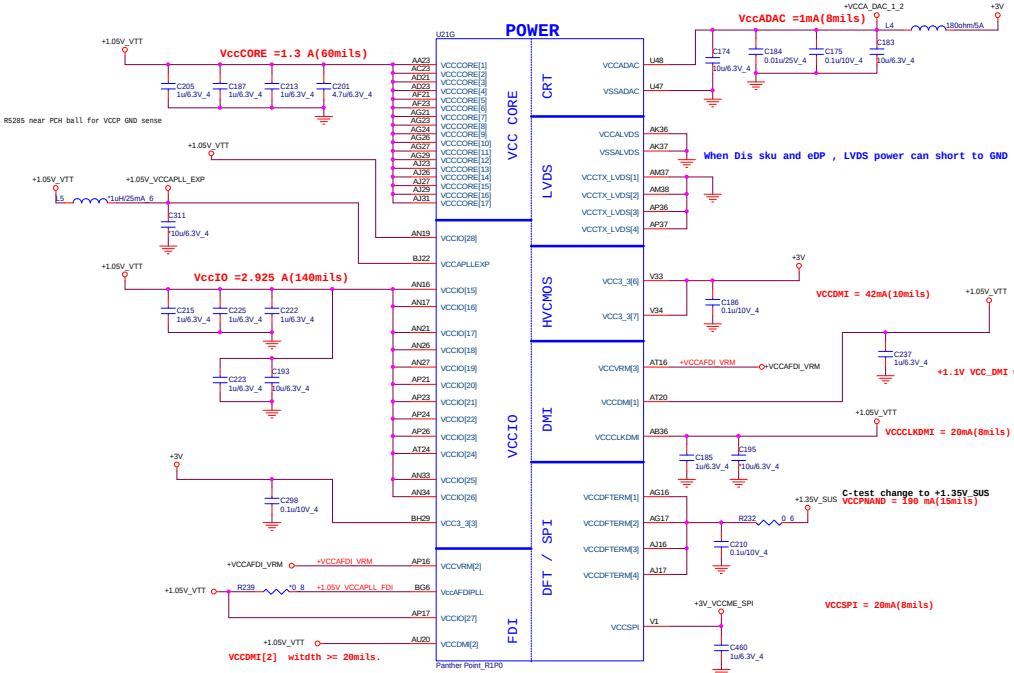
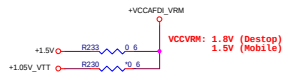
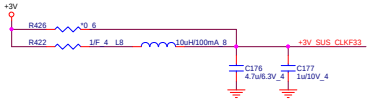
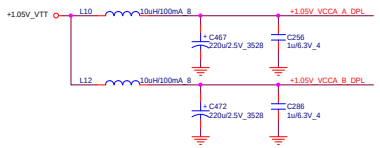
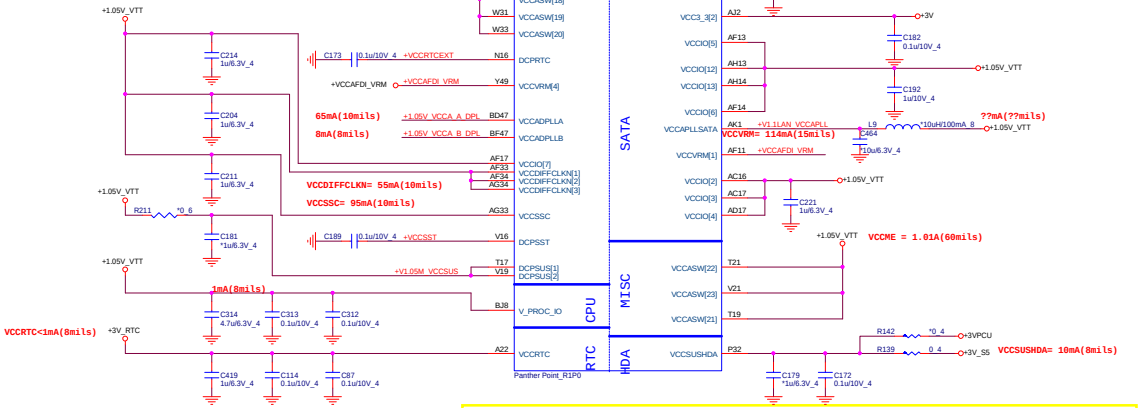
CPT/PPT (POWER)

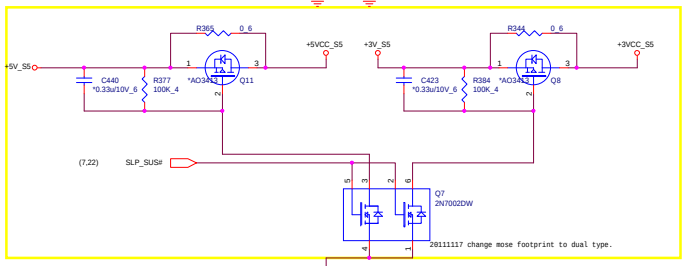












20111018 ADD DSW Cricuit
20111030 modify cuirucit.

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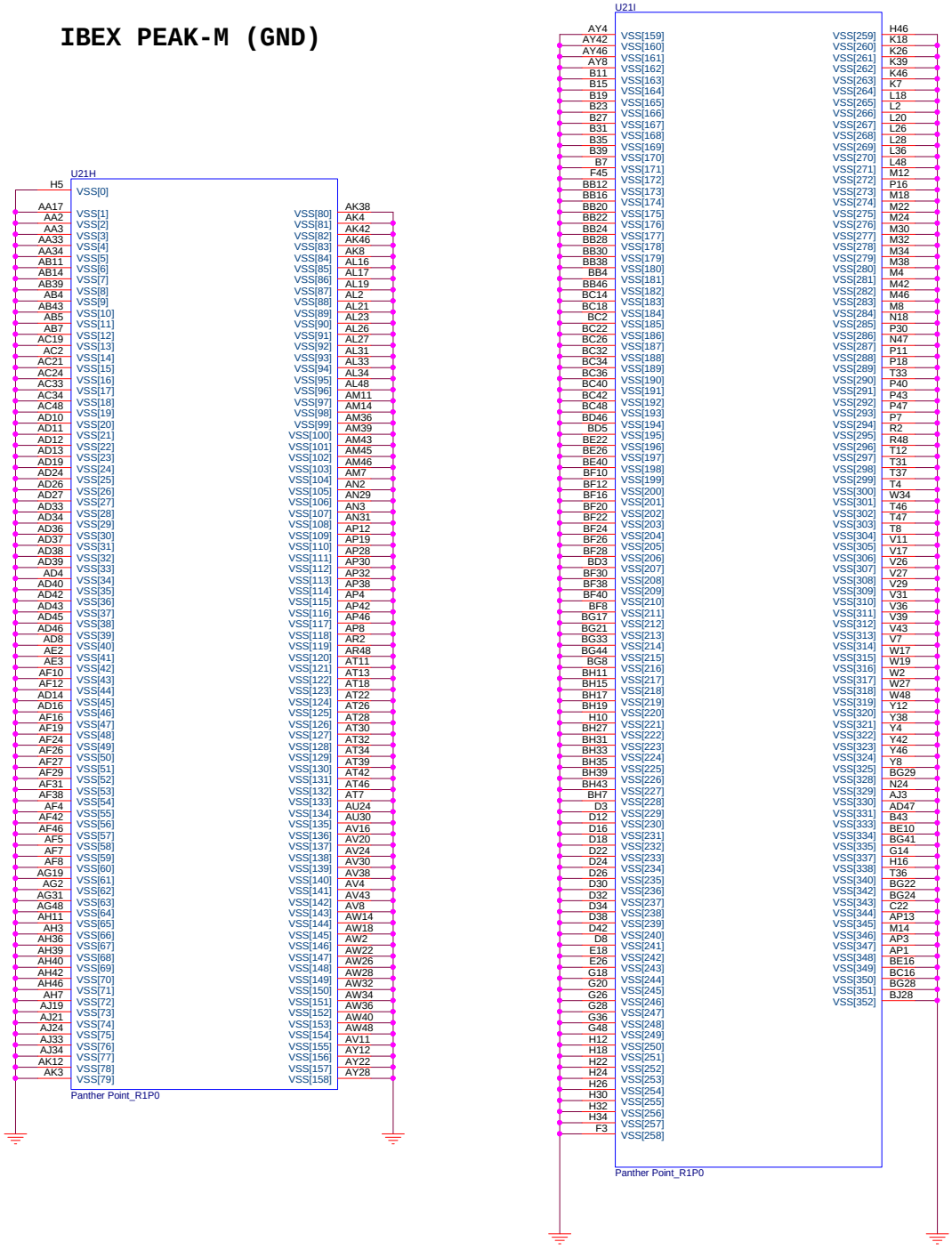
IBEX PEAK-M (GND)



Quanta Computer Inc.

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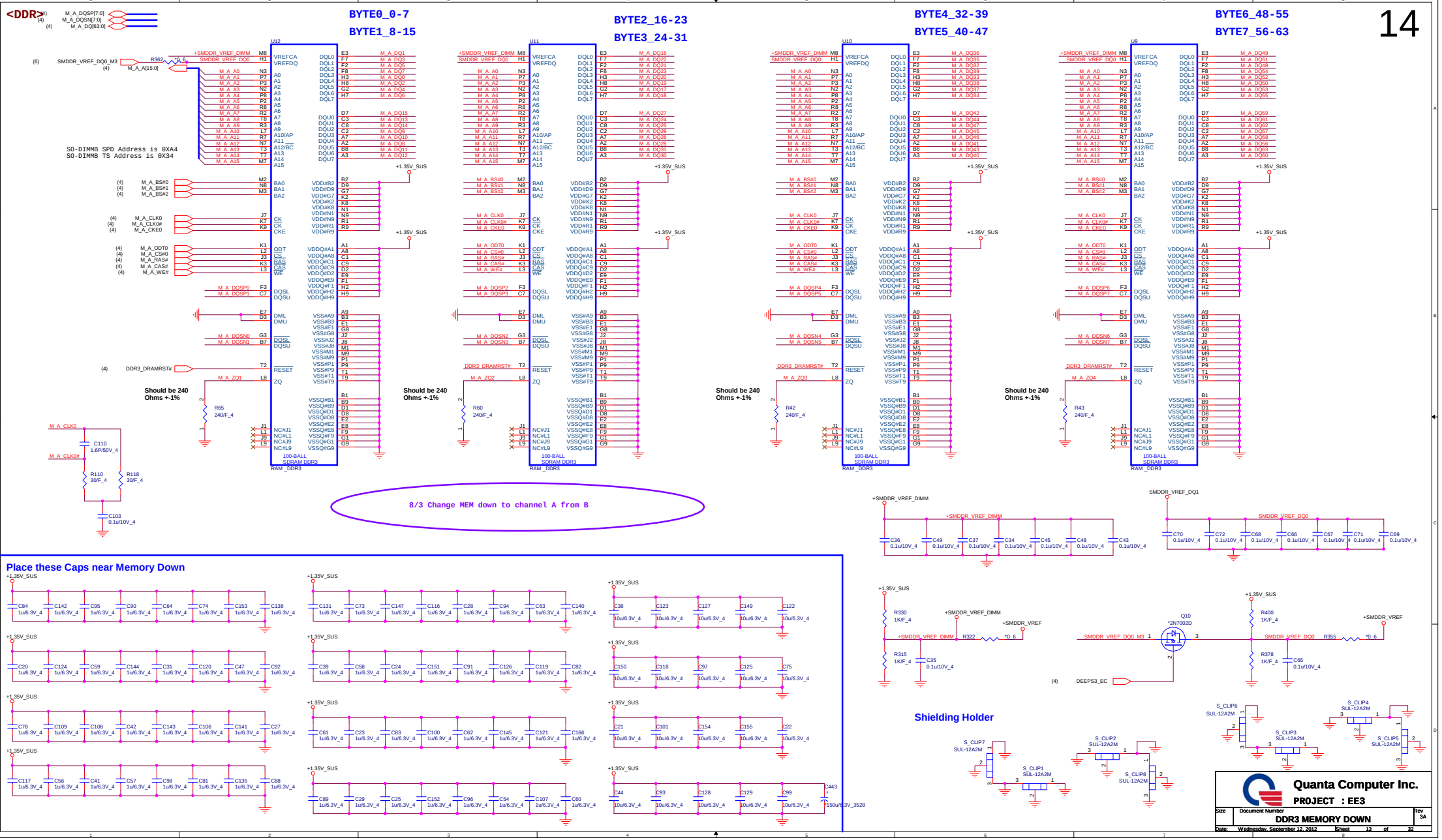
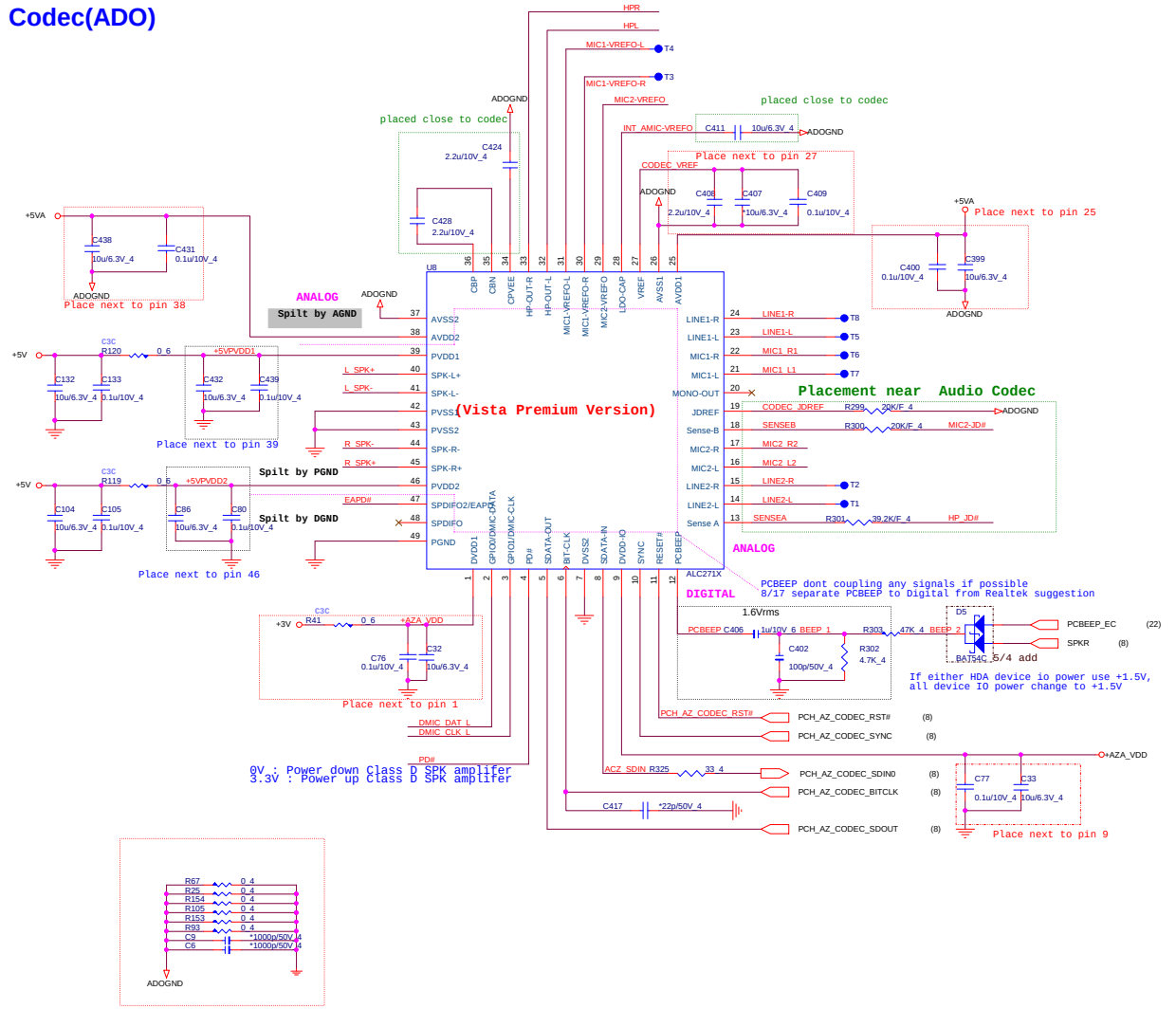
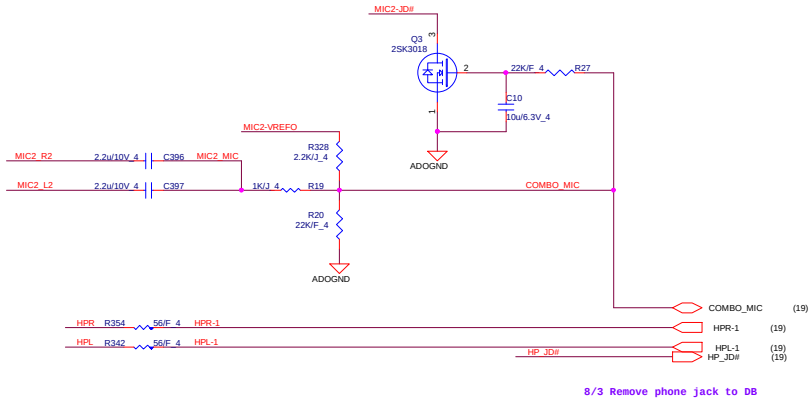

<DDR>
BYTE0_0-7
BYTE1_8-15
BYTE2_16-23
BYTE3_24-31
BYTE4_32-39
BYTE5_40-47
BYTE6_48-55
BYTE7_56-63
SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34
Should be 240 Ohms +-1%
8/3 Change MEM down to channel A from B
Place these Caps near Memory Down
Shielding Holder
Quanta Computer Inc.
PROJECT : EE3
DDR3 MEMORY DOWN
Wednesday, September 12, 2012

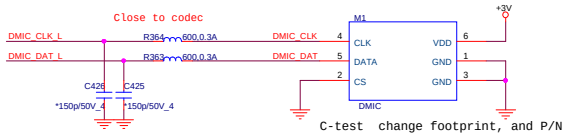
Codec(ADO)



HEADPHONE/Mic combo

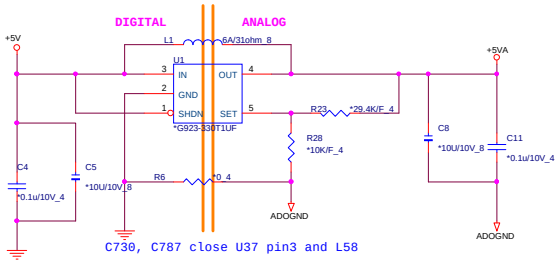


DMIC(ADO)

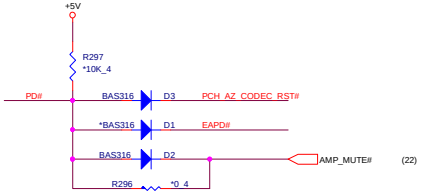


RF suggest to add R144,R149,C118,C134
Reserve for DMIC.(not use)

Power (ADO)

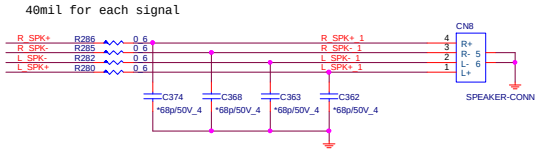


Mute(ADO)



Internal Speaker

Speaker connector
1st PN: DFHD04MRA75 CONN SMD HEADER 4P 1R MR(P1.25,H1.95)
2nd PN: DFHD04MR101 CONN SMD HEADER 4P 1R MR(P1.25,H1.9)
3rd PN: DFHD04MR102 CONN SMD HEADER 4P 1R MR(P1.25,H1.9)



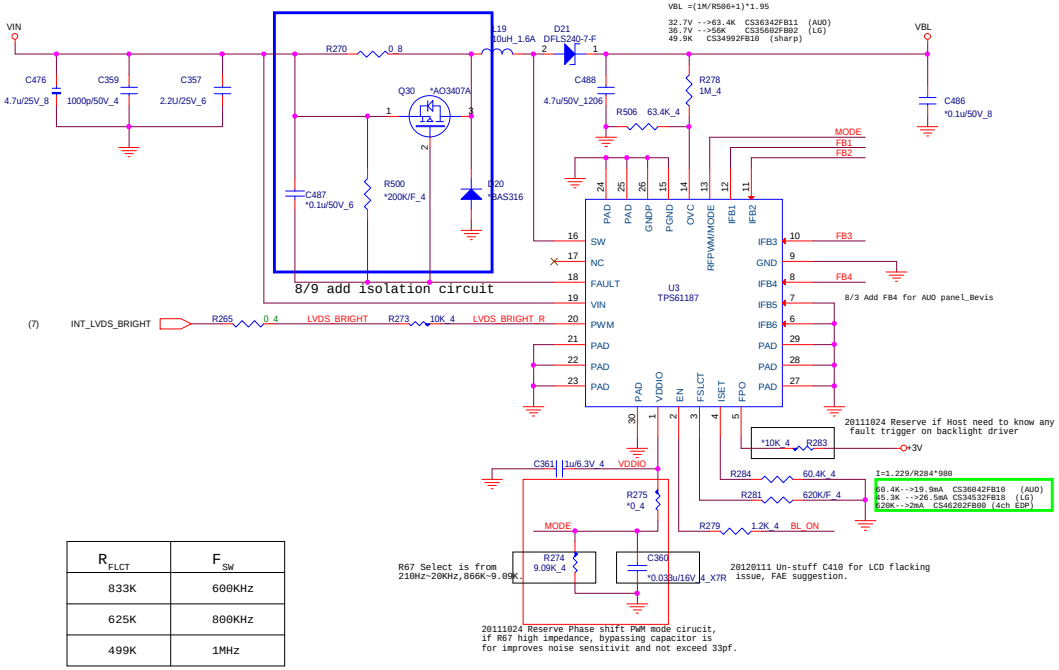
Quanta Computer Inc.
PROJECT : EE3

Size	Document Number	Rev
	ALC271/HP/DMIC/SPK	1A
Date: Wednesday, September 12, 2012	Sheet 14 of 32	

LED Driver-IC

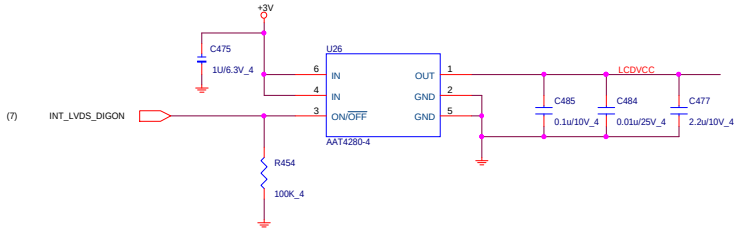
Penal SPEC:
Iout:72~82mA
Vout:27~29.7V
LED string 9S4P

SH@ ---> sharp panel

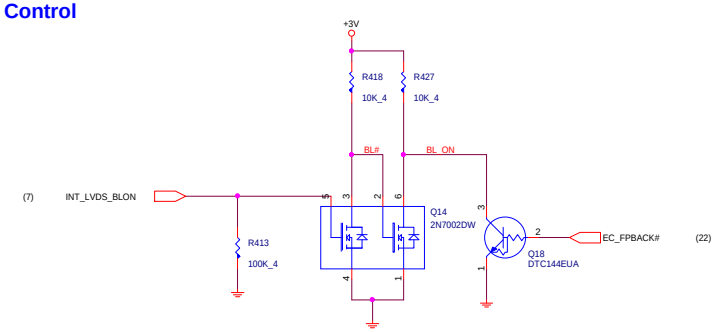


R_{FLCT}	F_{SW}
833K	600KHz
625K	800KHz
499K	1MHz

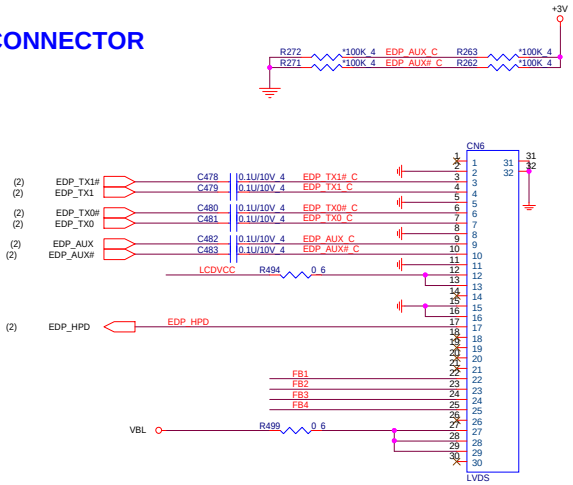
LCD Power



Backlight Control



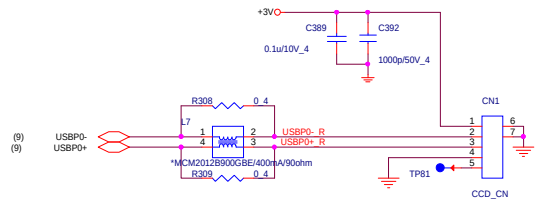
LCD CONNECTOR



C-test remove 4-ch circuit

FRONT CCD CONNECTOR

CCD +3V-current budget 0.2A

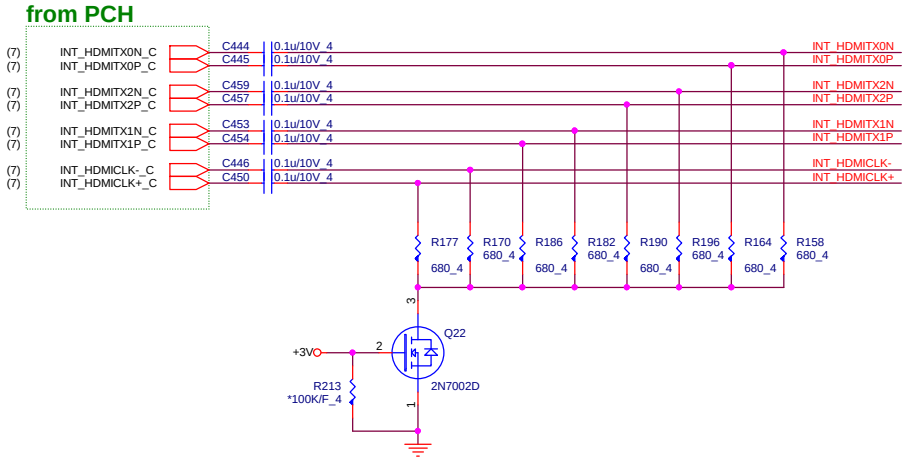


Quanta Computer Inc.
PROJECT : EE3

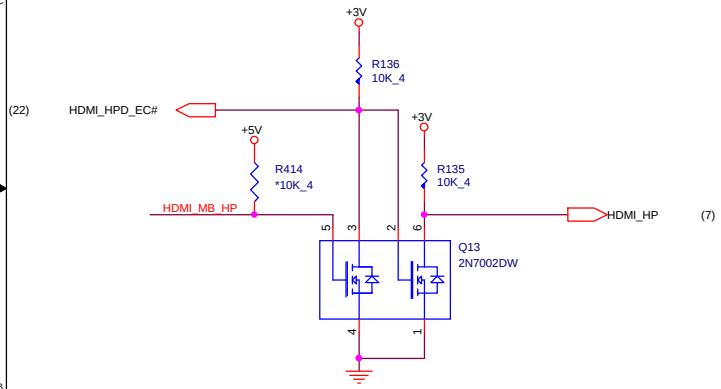
Size	Document Number	Rev
	EDP/LED DRIVER/CCD	3A

Date: Wednesday, September 12, 2012 Sheet 15 of 32

HDMI

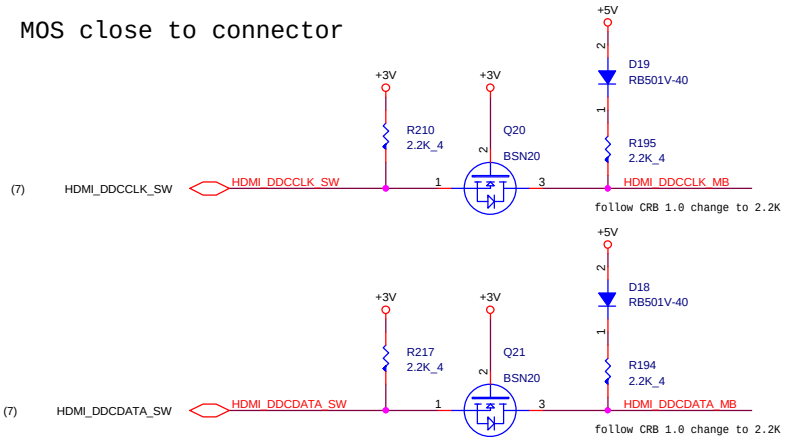


HDMI-detect

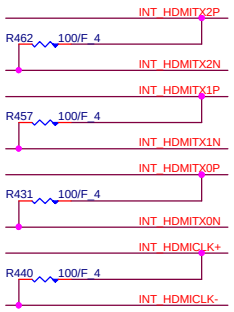


I2C

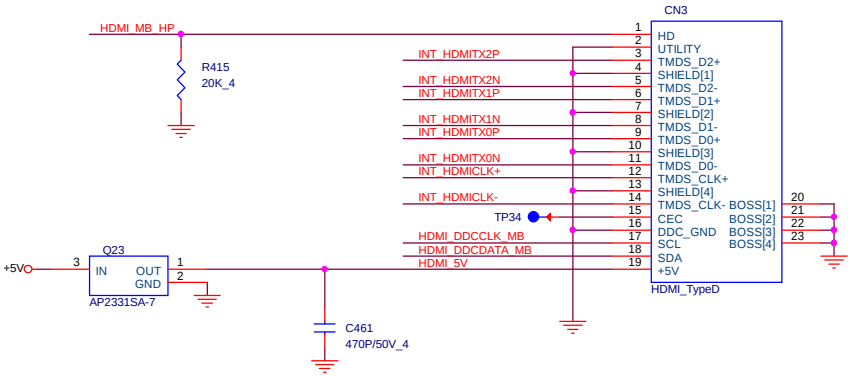
MOS close to connector



EMI



HDMI-Type D connector



ige to 20k.

Quanta Computer Inc.

PROJECT : EE3

Size	Document Number	Rev
	HDMI (PS8101)	3A
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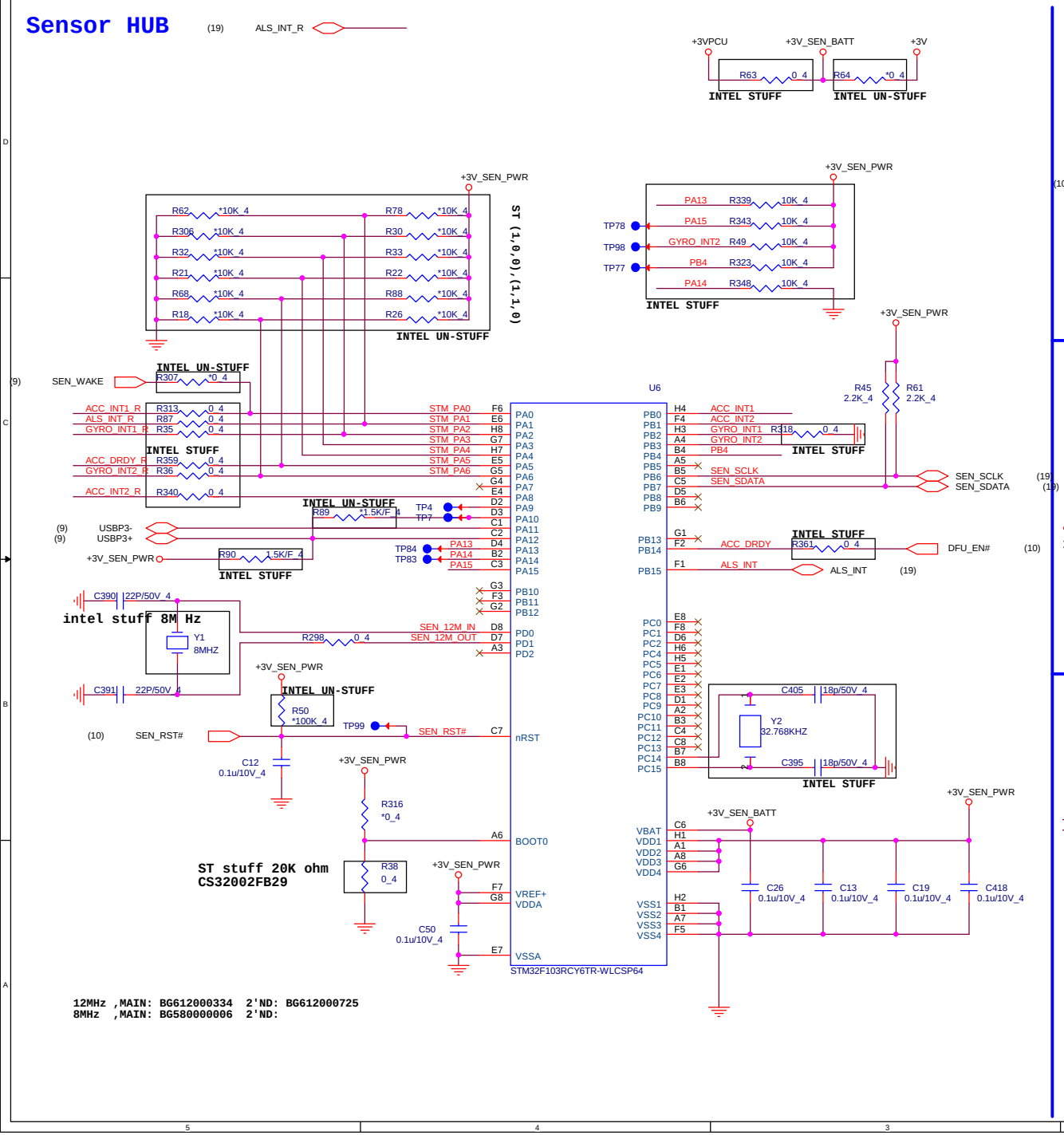
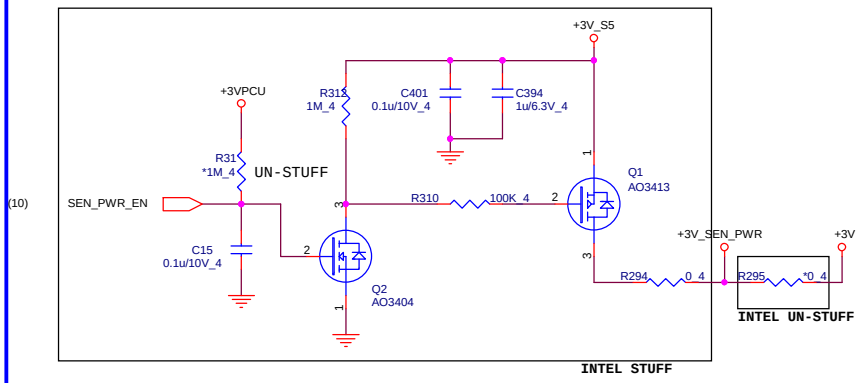
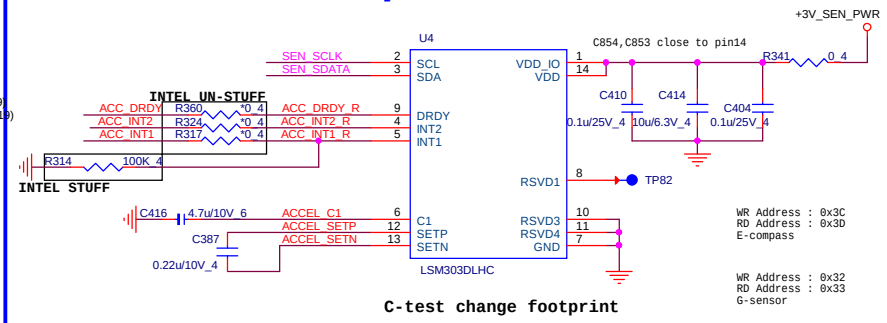
Sensor HUB



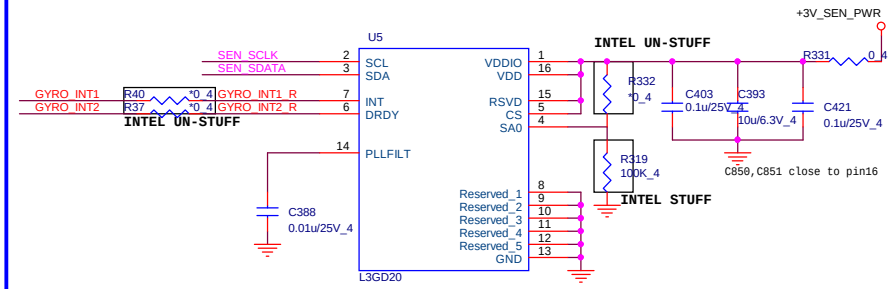


G-sensor/E-compass



C-test change footprint

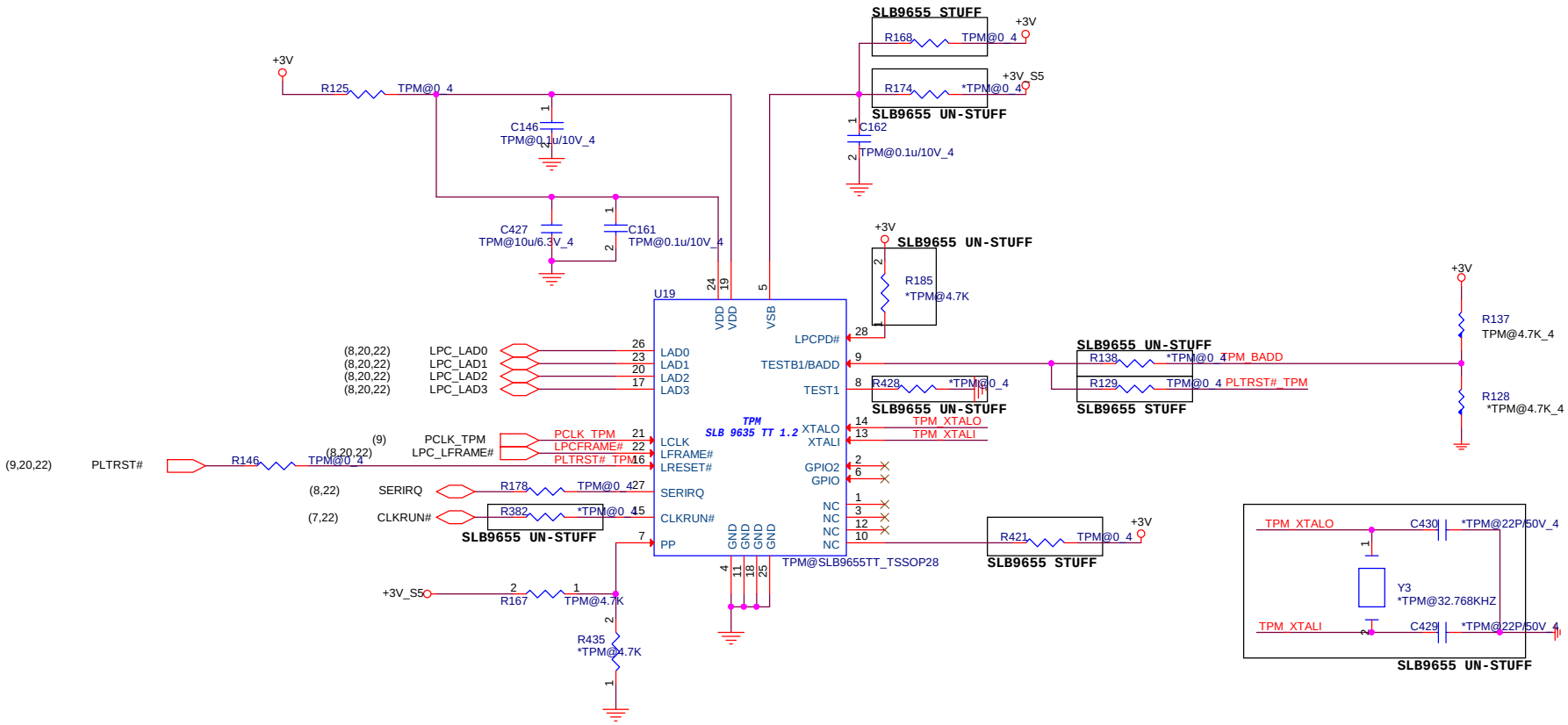
Gyroscope



WR Address : 0xD2
RD Address : 0xD3

Quanta Computer Inc.		
PROJECT : EE3		
Size	Document Number	Rev
	Sensor (Hub/Gyr/G+E)	1A
Date: Wednesday, September 12, 2012	Sheet 17 of 32	

TPM B-test change to AL009655K01



Thermal Remote Sensor

	Resiger Base Address
BADD=0	2E / 2F
BADD=1 (default)	4E / 4F

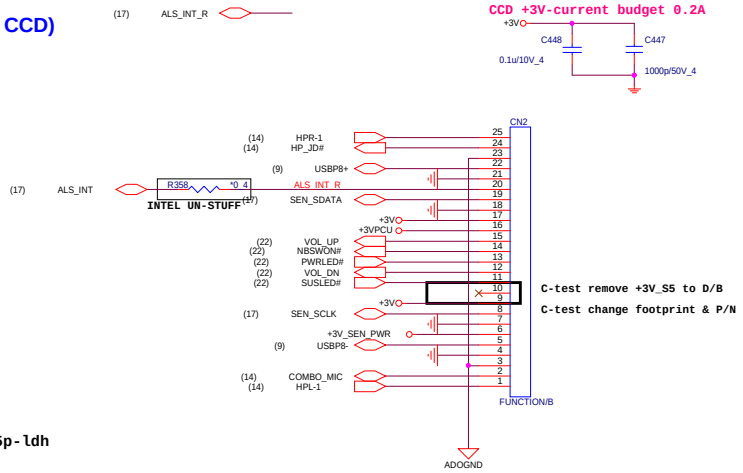
Quanta Computer Inc.

PROJECT : EE3

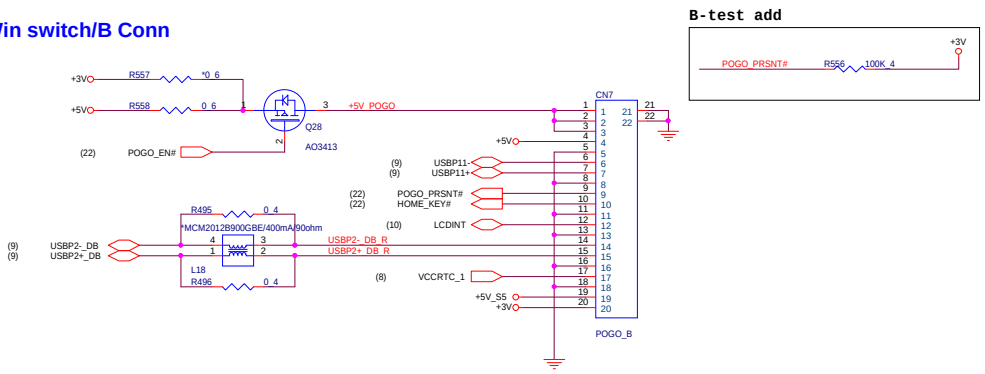
Size	Document Number	Rev
	RTS5209-GR (Card Reader)	1D

Date: Wednesday, September 12, 2012 Sheet 18 of 32

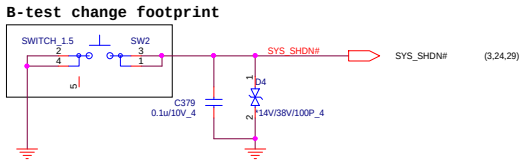
Audio/B CONN (REAR CCD)



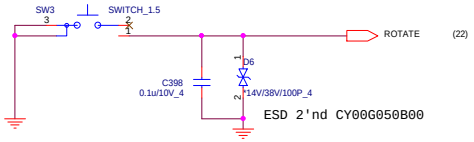
Win switch/B Conn



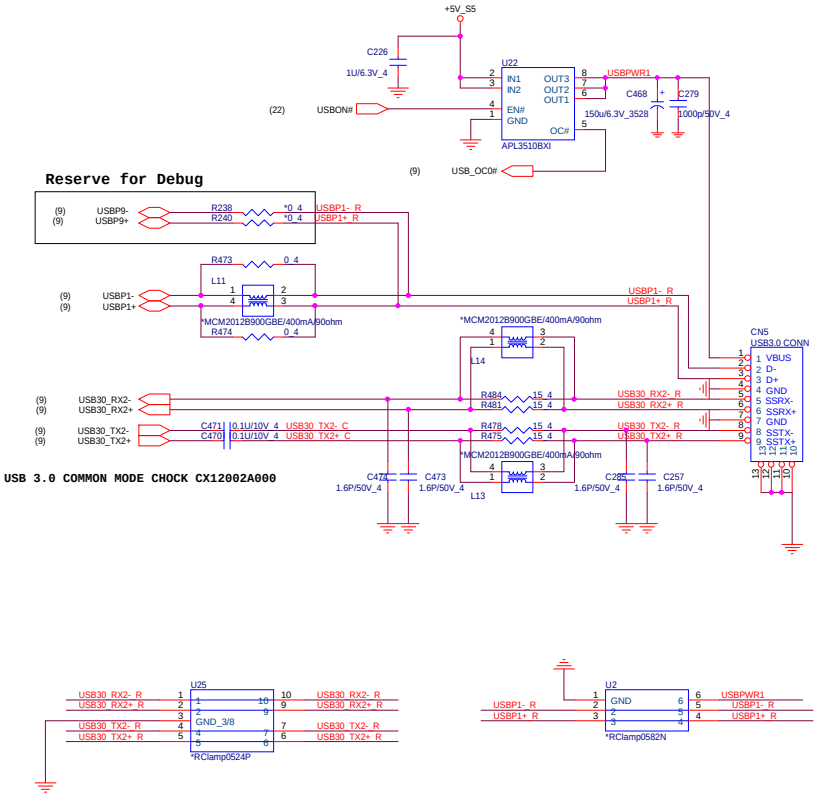
RESET SW



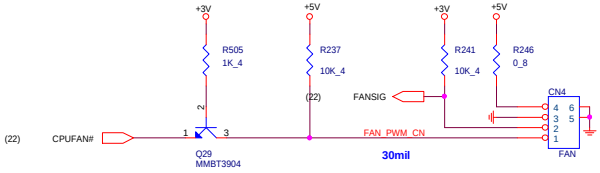
Rotate Switch



USB 3.0

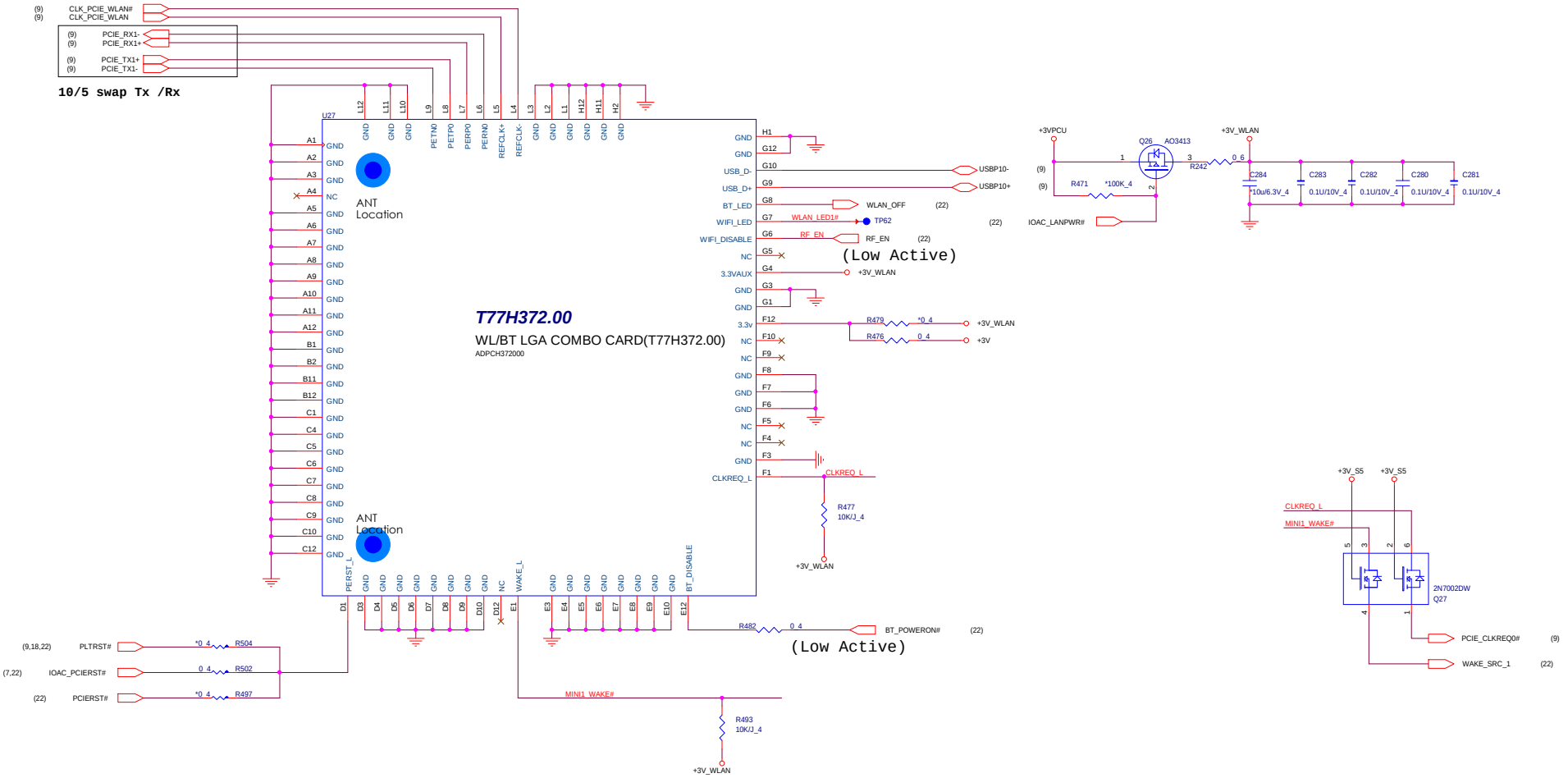


CPU FAN

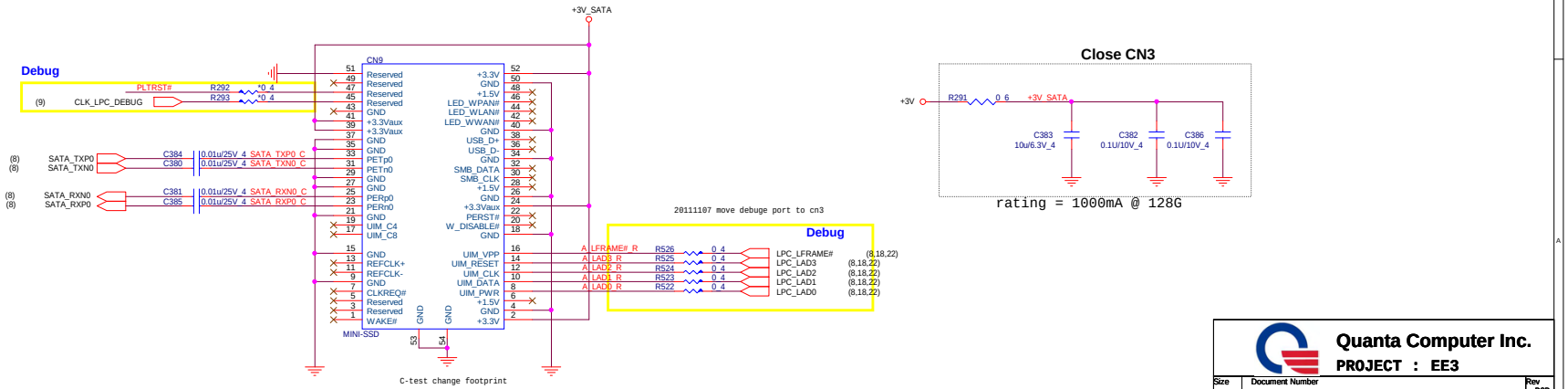


Quanta Computer Inc.		
PROJECT : EE3		
Size	Document Number: USB3.0/TPM/Fan	Rev: 3A
Date: Wednesday, September 12, 2012	Sheet 19 of 32	

Mini Card 1 (MPC)



mSATA



Quanta Computer Inc.			
PROJECT : EE3			
Size	Document Number		Rev
	Mini-Card/WL		B3B
Date:	Wednesday, September 12, 2012	Sheet 20 of 32	

SCREW HOLE

HOLE8
H-c236d126p2

HOLE6
*H-C197D98P2

HOLE14
*H-C197D98P2

HOLE11
*H-C197D98P2

HOLE9
*H-C197D98P2

HOLE7
*H-C197D98P2

HOLE13
*H-C197D98P2

HOLE12
*H-C197D98P2

HOLE10
*H-C197D98P2

HOLE2
*H-C197D98P2

HOLE5
*H-C197D98P2

HOLE3
*h-C51d51n

HOLE1
*h-O71x52d71x52n

HOLE4
*H-C87D87N

BATT Enable short pad

HOLE16
*O-EE3-1

BATT_EN# (23)

HOLE15
*O-EE3-1

BATT_EN#

PAD2
*spad-re315x226

EE RETURN-PATH CAPACITORS

+3V
C137 *0.1u/10V_4 +1.35V_SUS
C148 *0.1u/10V_4 +1.35V_SUS
C190 *0.1u/10V_4 +1.05V_VTT

VIN
C206 *0.1u/25V_4 +3V
C253 *0.1u/25V_4 +5V
C373 *0.1u/25V_4 +VCC_CORE
C376 *0.1u/25V_4 +3VPCU
C378 *0.1u/25V_4
C165 0.1u/25V_4
C233 *0.1u/25V_4
C356 *0.1u/25V_4
C324 0.1u/25V_4
C354 *0.1u/25V_4

VIN
C236 *2200p/50V_4

+1.35V_SUS
C139 *0.1u/10V_4 +3V
C115 0.1U/10V_4
C158 *470P/50V_4 +3V

+3V
C199 *0.1u/10V_4 +1.05V_VTT
C218 *0.1u/10V_4
C102 *470P/50V_4
C157 *2200p/50V_4
C377 *2200p/50V_4
C112 *2200p/50V_4
C254 *2200p/50V_4

+1.05V_VTT
C209 *0.1u/10V_4
C267 *2200p/50V_4

201201117 C765 for EMI suggestion.
201201119 Add C2765 for EMI suggestion to GND.

20111128 del C508/C704/C479/C497 and change path cap power well.

Quanta Computer Inc.
PROJECT : EE3

Size	Document Number	Rev
	Hole \ RETURN-PATH	3A

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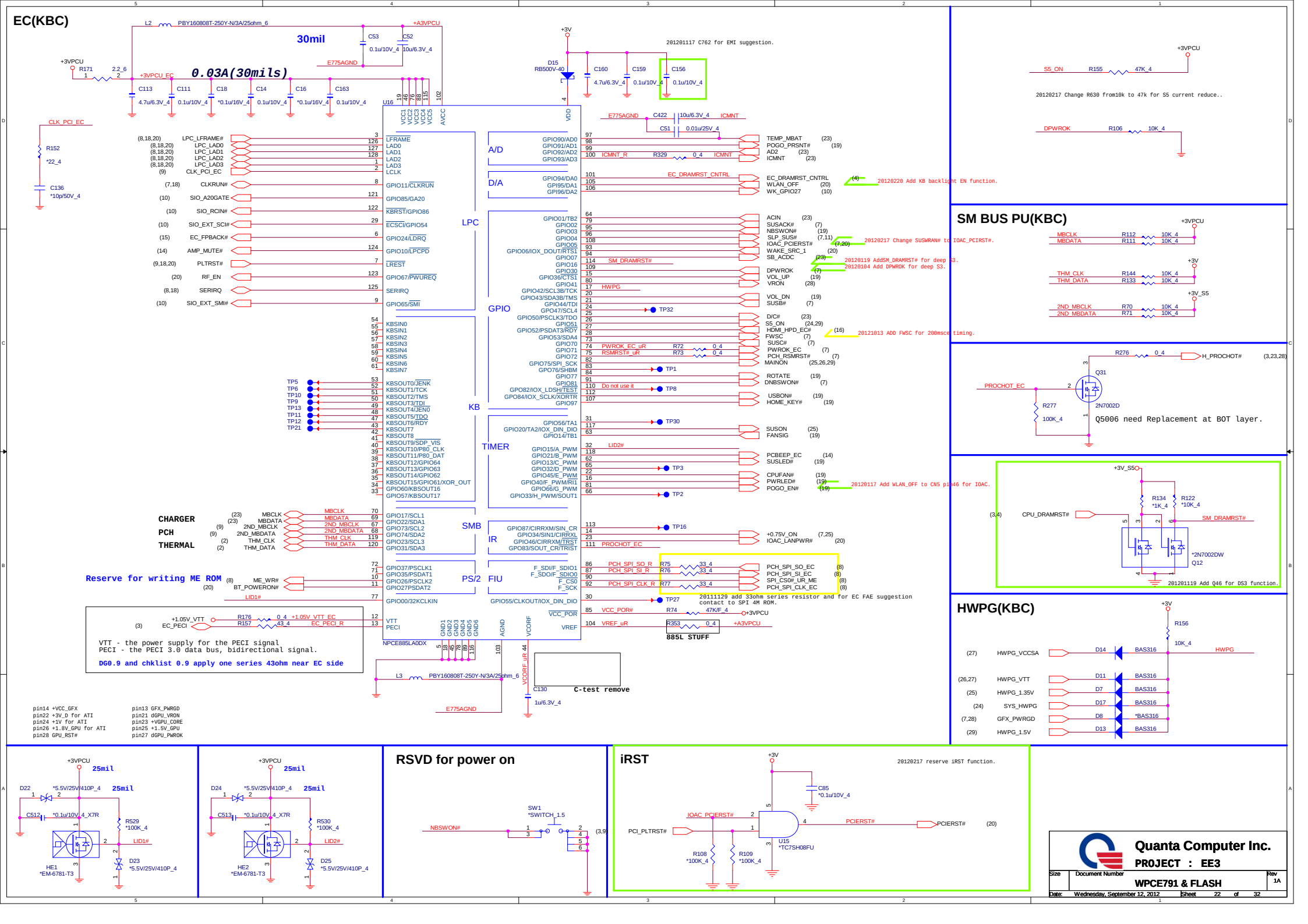
EC(KBC)



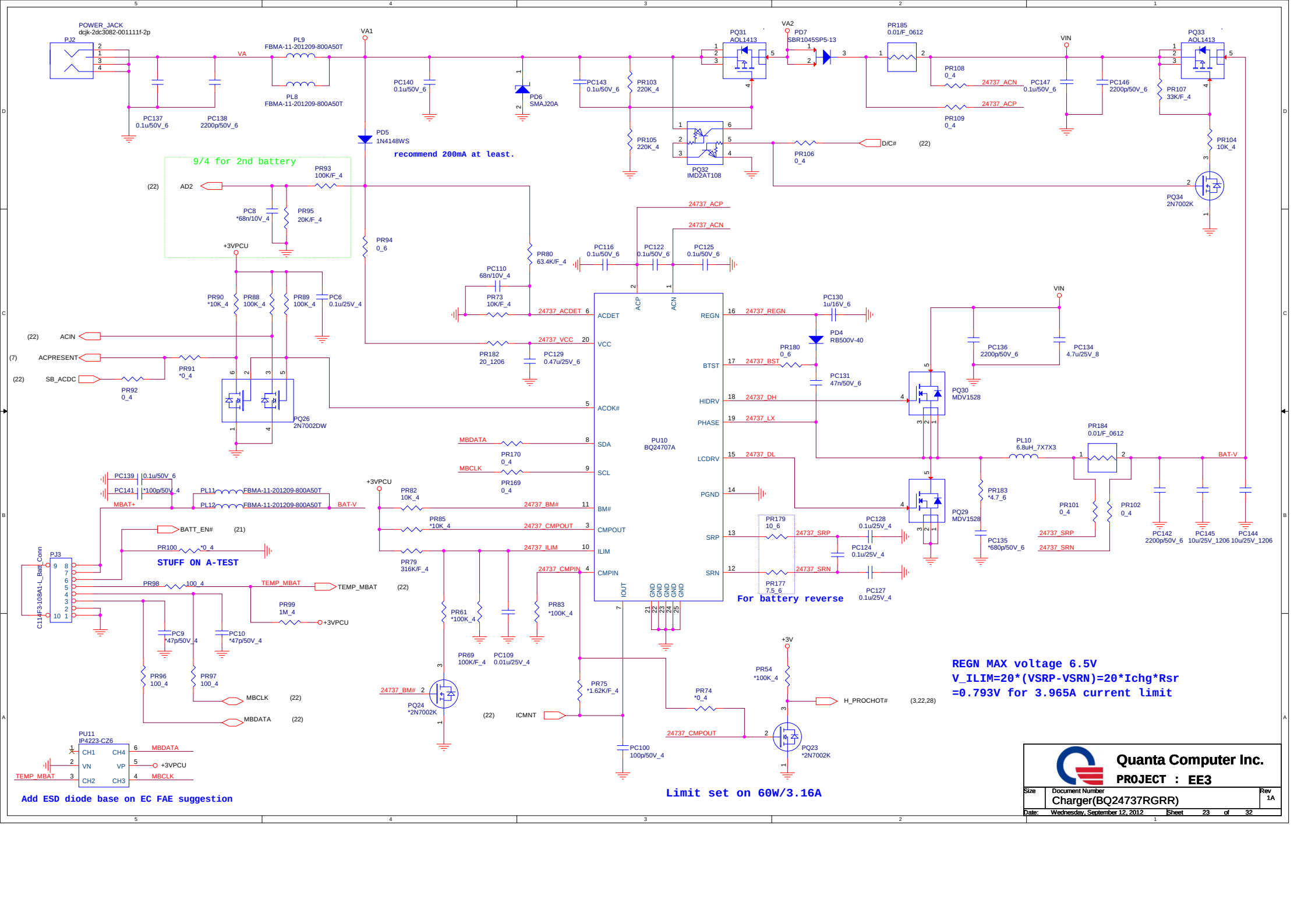
SM BUS PU(KBC)

HWPG(KBC)

RSVD for power on

iRST

Quanta Computer Inc.
PROJECT : EE3
Size | Document Number | Rev
WPCE791 & FLASH | 1A
Date: Wednesday, September 12, 2012 | Sheet 22 of 32


POWER_JACK
dcjk-2dc3082-001111f-2p
PJ2
VA
PL9
FBMA-11-201209-800A50T
PL8
FBMA-11-201209-800A50T
VA1
PC137
0.1u/50V_6
PC138
2200p/50V_6
PC140
0.1u/50V_6
PD5
1N4148WS
recommend 200mA at least.
PD6
SMAJ20A
PC143
0.1u/50V_6
PR103
220K_4
PR105
220K_4
PQ31
AOL1413
PQ32
IMD2AT108
VA2
PD7
SBR1045SP5-13
PR185
0.01/F_0612
PR108
0_4
PR109
0_4
24737_ACN
24737_ACP
PC147
0.1u/50V_6
VIN
PC146
2200p/50V_6
PQ33
AOL1413
PR107
33K/F_4
PR104
10K_4
PQ34
2N7002K
PR106
0_4
D/C#
(22)
9/4 for 2nd battery
PR93
100K/F_4
AD2
PC8
*68n/10V_4
PR95
20K/F_4
+3VPCU
PR94
0_6
PR80
63.4K/F_4
PC110
68n/10V_4
PR73
10K/F_4
24737_ACDET
PC116
0.1u/50V_6
PC122
0.1u/50V_6
PC125
0.1u/50V_6
PR90
*10K_4
PR88
100K_4
PR89
100K_4
PC6
0.1u/25V_4
ACIN
ACPRESENT
SB_ACDC
PR91
*0_4
PR92
0_4
PQ26
2N7002DW
PR182
20_1206
PC129
0.47u/25V_6
24737_VCC
PU10
BQ24707A
ACDET
VCC
ACOK#
SDA
SCL
BM#
CMPOUT
ILIM
CMPIN
IOUT
ACP
ACN
REGN
BTST
HIDRV
PHASE
LCDRV
PGND
SRP
SRN
24737_REGN
24737_BST
24737_DH
24737_LX
24737_DL
24737_SRP
24737_SRN
PC130
1u/16V_6
PD4
RB500V-40
PR180
0_6
PC131
47n/50V_6
PQ30
MDV1528
PQ29
MDV1528
PC136
2200p/50V_6
PC134
4.7u/25V_8
PL10
6.8uH_7X7X3
PR184
0.01/F_0612
PR183
*4.7_6
PC135
*680p/50V_6
PR101
0_4
PR102
0_4
PC142
2200p/50V_6
PC145
10u/25V_1206
PC144
10u/25V_1206
BAT-V
PC128
0.1u/25V_4
PC124
0.1u/25V_4
PC127
0.1u/25V_4
PR179
10_6
PR177
7.5_6
For battery reverse
MBDATA
MBCLK
PR170
0_4
PR169
0_4
PC139
0.1u/50V_6
PC141
*100p/50V_4
PL11
FBMA-11-201209-800A50T
PL12
FBMA-11-201209-800A50T
MBAT+
BAT-V
BATT_EN#
(21)
PR100
*0_4
STUFF ON A-TEST
PJ3
C114F3-10BA1-L_Batt_Conn
PR98
100_4
TEMP_MBAT
PR99
1M_4
PC9
*47p/50V_4
PC10
*47p/50V_4
PR96
100_4
PR97
100_4
MBCLK
MBDATA
PR82
10K_4
PR85
*10K_4
PR79
316K/F_4
PR61
*100K_4
PR83
*100K_4
PR69
100K/F_4
PC109
0.01u/25V_4
PQ24
*2N7002K
PR75
*1.62K/F_4
PC100
100p/50V_4
ICMNT
PR74
*0_4
PR54
*100K_4
PQ23
*2N7002K
H_PROCHOT#
(3,22,28)
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit
PU11
IP4223-CZ6
CH1
CH2
CH3
CH4
VN
VP
Add ESD diode base on EC FAE suggestion
Limit set on 60W/3.16A
Quanta Computer Inc.
PROJECT : EE3
Size
Document Number
Charger(BQ24737RGRR)
Rev
1A
Date: Wednesday, September 12, 2012
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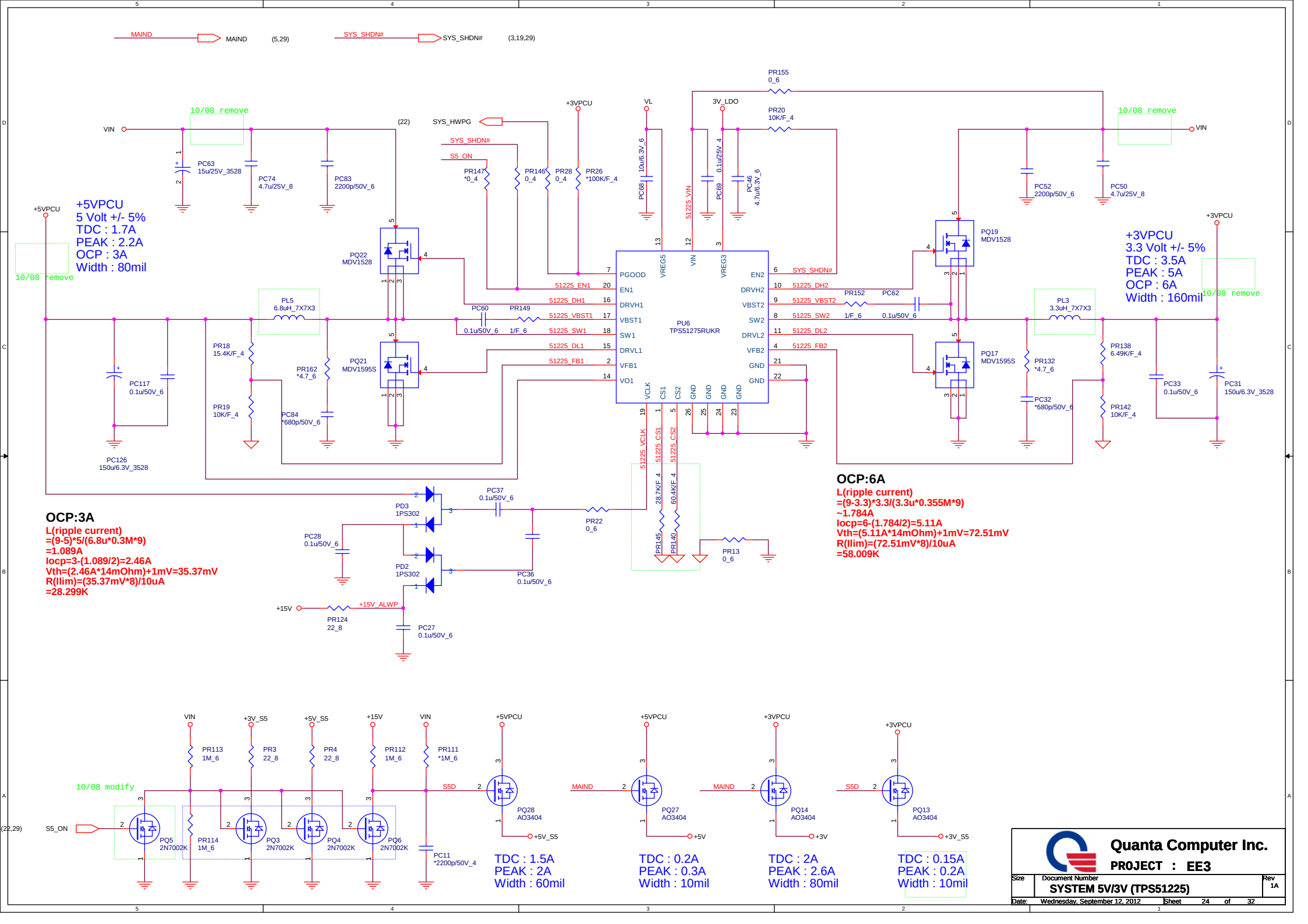
MAIND
MAIND (5,29)
SYS_SHDN#
SYS_SHDN# (3,19,29)
+5VPCU
5 Volt +/- 5%
TDC : 1.7A
PEAK : 2.2A
OCP : 3A
Width : 80mil
+3VPCU
3.3 Volt +/- 5%
TDC : 3.5A
PEAK : 5A
OCP : 6A
Width : 160mil
PU6
TPS51275RUKR
OCP:3A
L(ripple current)
=(9-5)*5/(6.8u*0.3M*9)
=1.089A
Iocp=3-(1.089/2)=2.46A
Vth=(2.46A*14mOhm)+1mV=35.37mV
R(Ilim)=(35.37mV*8)/10uA
=28.299K
OCP:6A
L(ripple current)
=(9-3.3)*3.3/(3.3u*0.355M*9)
~1.784A
Iocp=6-(1.784/2)=5.11A
Vth=(5.11A*14mOhm)+1mV=72.51mV
R(Ilim)=(72.51mV*8)/10uA
=58.009K
10/08 remove
10/08 modify
TDC : 1.5A
PEAK : 2A
Width : 60mil
TDC : 0.2A
PEAK : 0.3A
Width : 10mil
TDC : 2A
PEAK : 2.6A
Width : 80mil
TDC : 0.15A
PEAK : 0.2A
Width : 10mil
Quanta Computer Inc.
PROJECT : EE3
SYSTEM 5V/3V (TPS51225)
Size
Document Number
Rev 1A
Date: Wednesday, September 12, 2012
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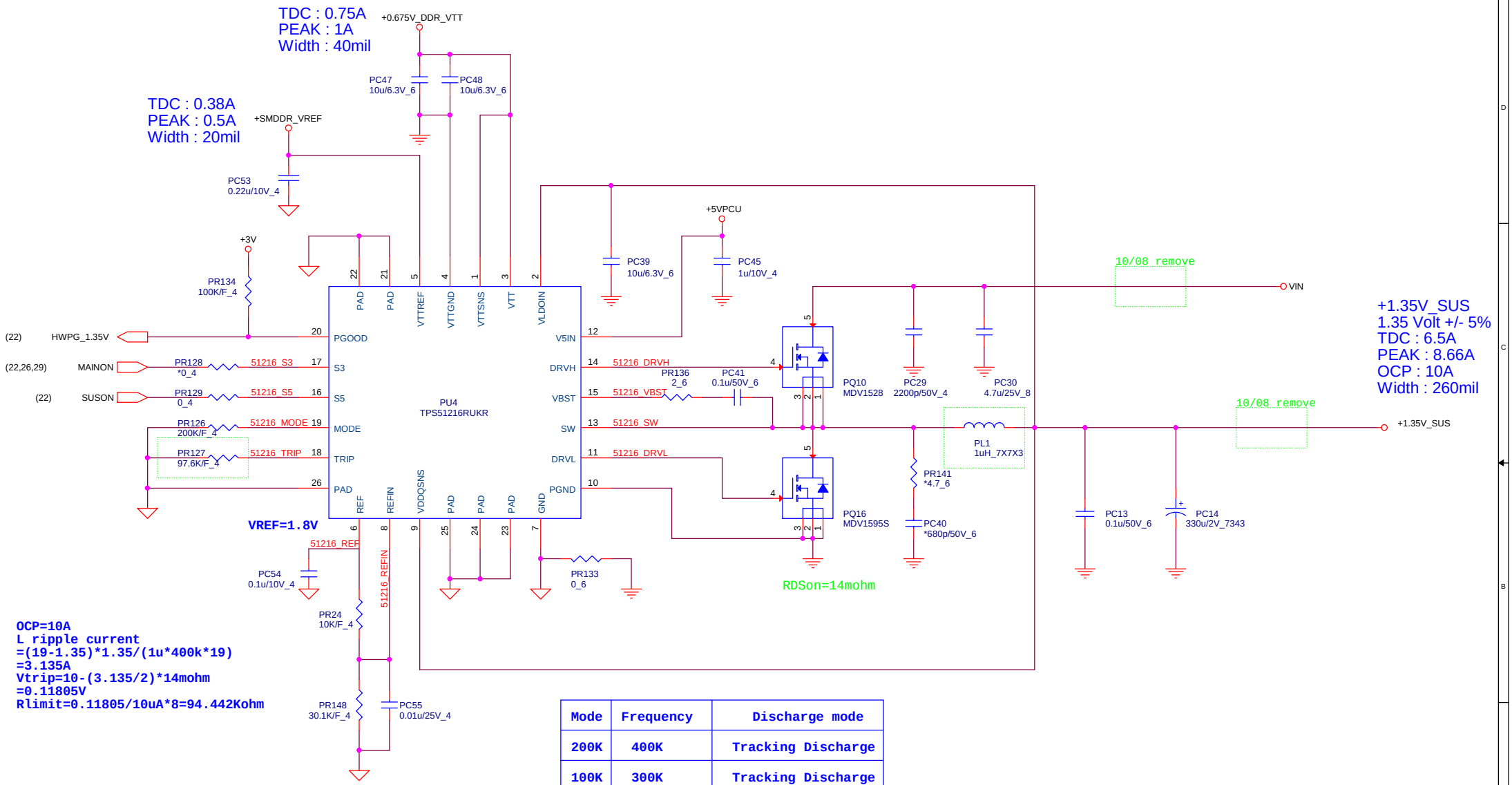

Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35V_SUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : EE3

Size	Document Number	Rev
	DDR 1.5V(TPS51216)	1A

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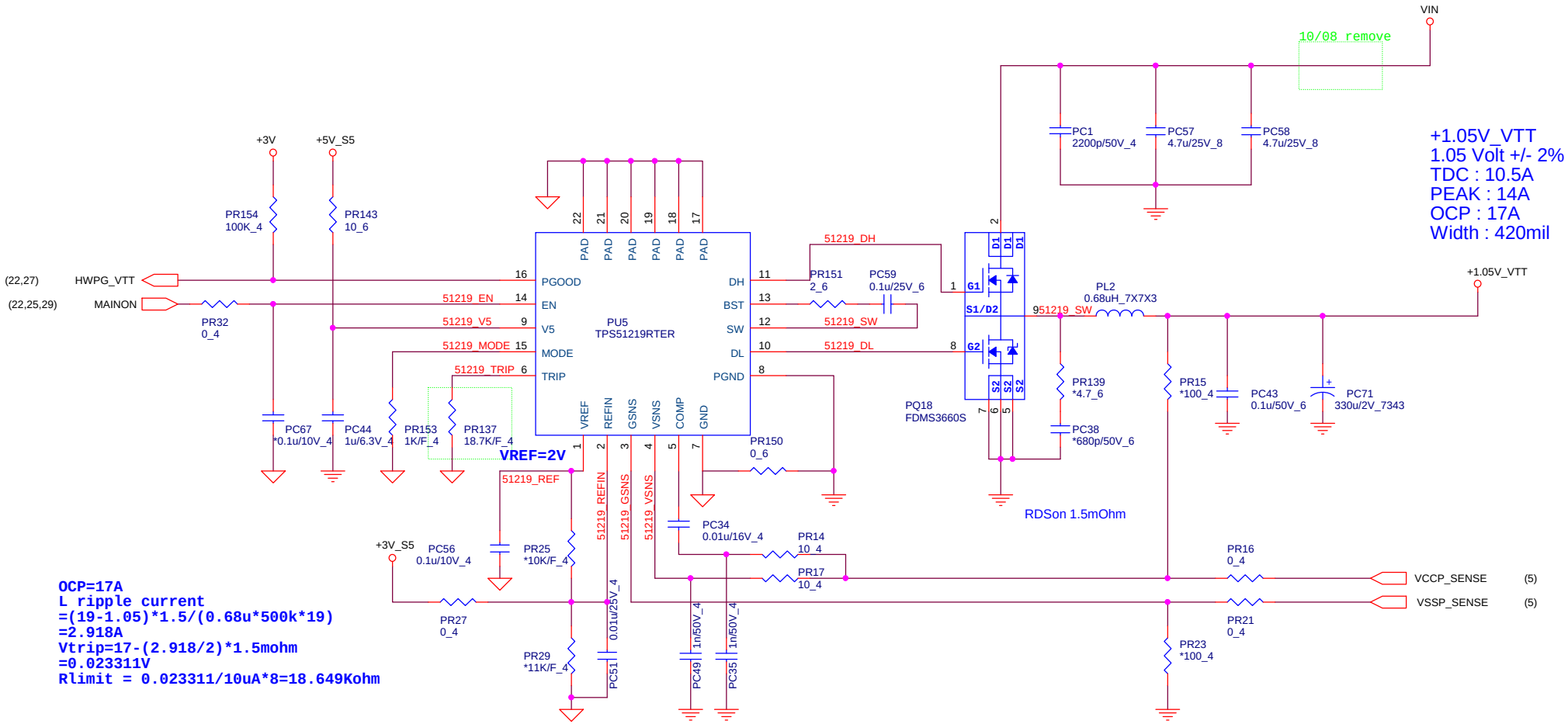

Quanta Computer Inc.		
PROJECT : EE3		
Size	Document Number: +1.05V (TPS51219)	Rev 1A
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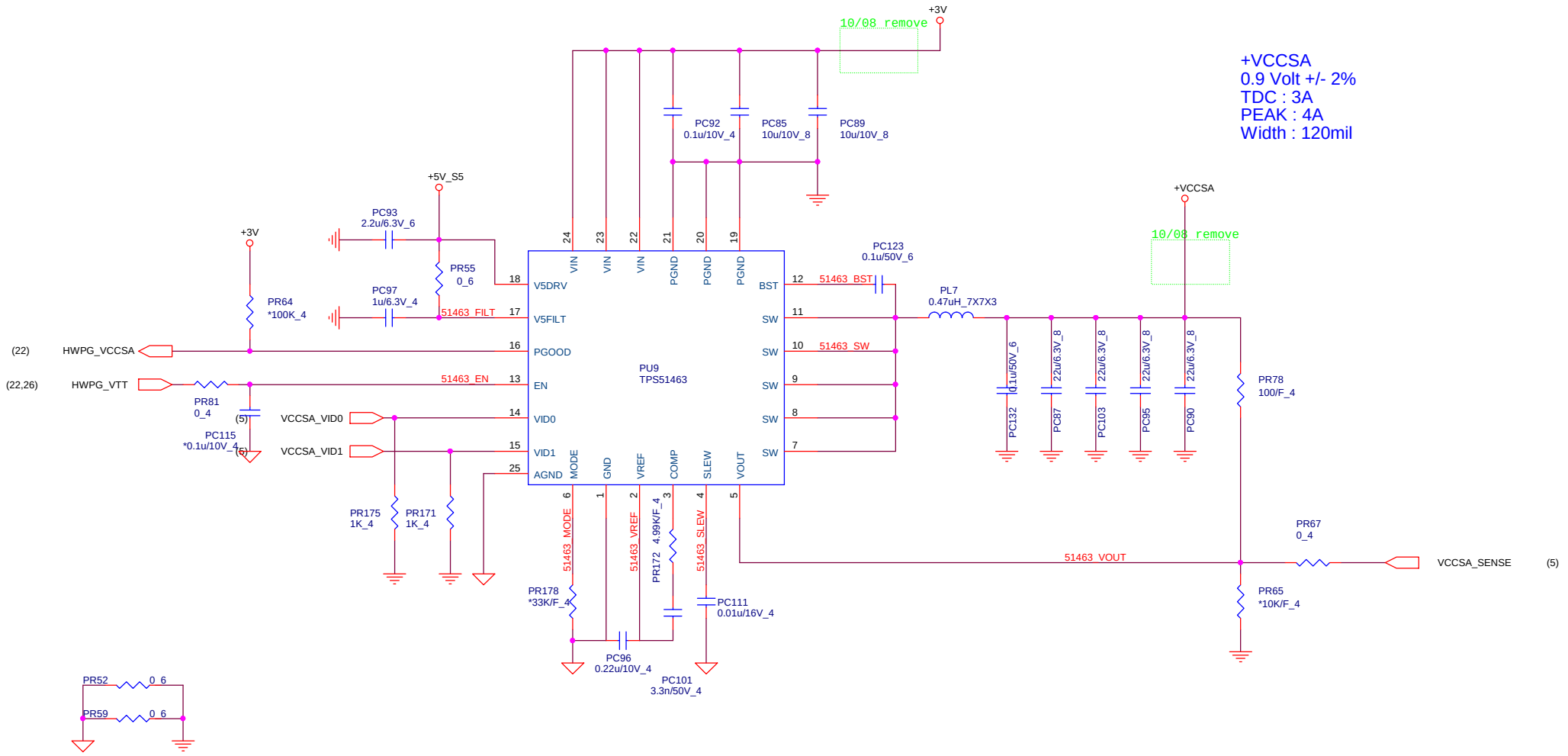

Huron River / Chief River

VID0	VID1	+VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

default 0.9V

Quanta Computer Inc.		
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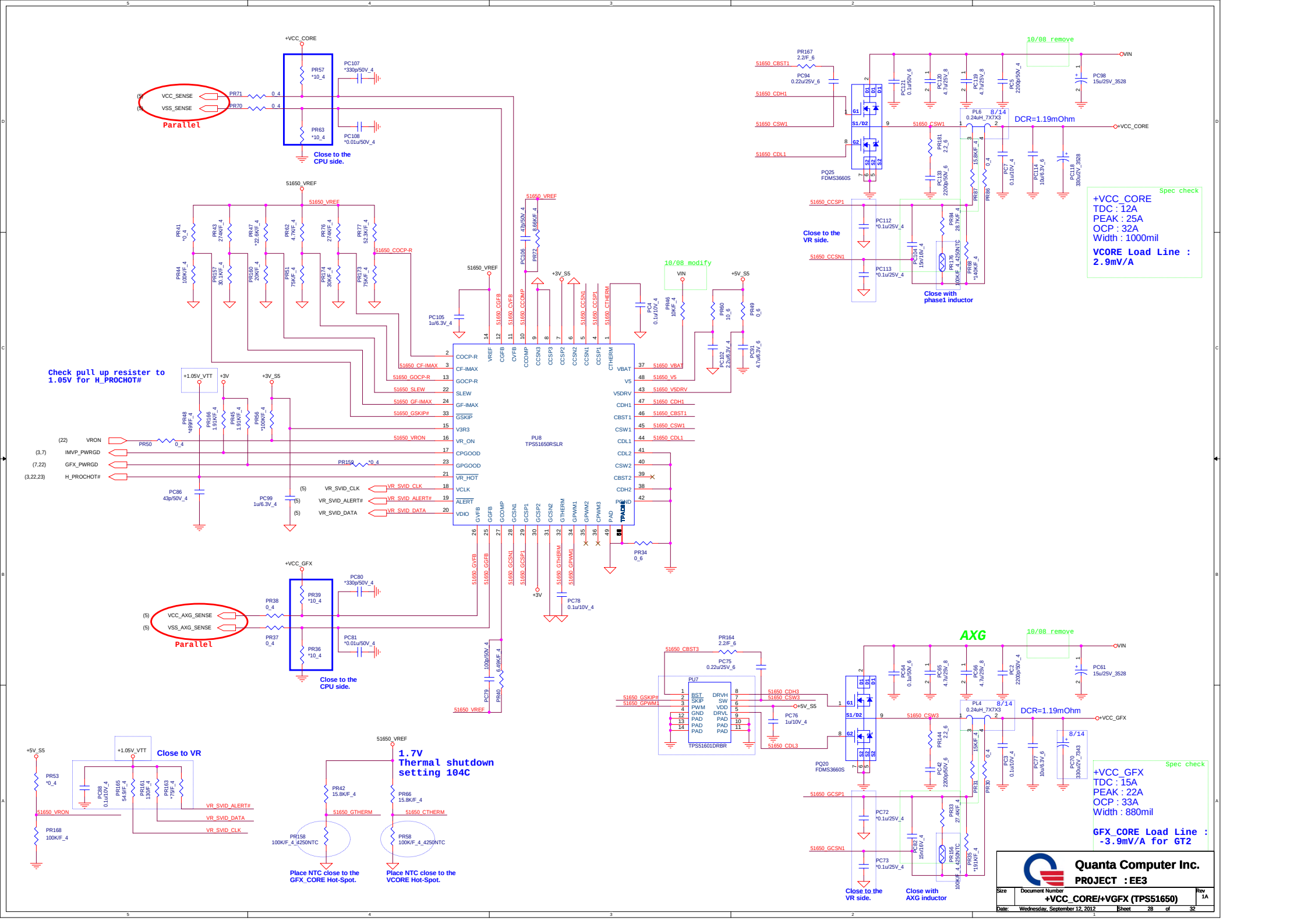
+VCC_CORE
PR57 *10_4
PC107 *330p/50V_4
PC108 *0.01u/50V_4
PR63 *10_4
VCC_SENSE
VSS_SENSE
PR71 0_4
PR70 0_4
Parallel
Close to the CPU side.
51650_VREF
PR41 *0_4
PR43 274K/F_4
PR47 *22.6K/F_4
PR62 4.7K/F_4
PR76 274K/F_4
PR77 52.3K/F_4
PR44 100K/F_4
PR157 30.1K/F_4
PR160 20K/F_4
PR51 75K/F_4
PR174 30K/F_4
PR173 75K/F_4
51650_COCP-R
PC105 1u/6.3V_4
PC106 47p/50V_4
PR72 8.66K/F_4
51650_CGFB
51650_CVFB
51650_CCOMP
51650_CCSN1
51650_CCSP1
51650_CTHERM
+3V_S5
10/08 modify
VIN
+5V_S5
PR46 10K/F_4
PR60 10_6
PR49 0_6
PC102 2.2u/6.3V_4
PC91 4.7u/6.3V_6
PC4 0.1u/10V_4
Check pull up resister to 1.05V for H_PROCHOT#
+1.05V_VTT
+3V
+3V_S5
PR48 *499/F_4
PR166 1.91K/F_4
PR45 1.91K/F_4
PR66 *100K/F_4
(22) VRON
(3,7) IMVP_PWRGD
(7,22) GFX_PWRGD
(3,22,23) H_PROCHOT#
PR50 0_4
PR159 *0_4
PC86 43p/50V_4
PC99 1u/6.3V_4
PU8
TPS51650RSLR
COCP-R
CF-IMAX
GOCP-R
SLEW
GF-IMAX
GSKIP
V3R3
VR_ON
CPGOOD
GPGOOD
VR_HOT
ALERT
VDIO
VREF
CGFB
CVFB
CCOMP
CCSN3
CCSP3
CCSP2
CCSN2
CCSN1
CCSP1
CTHERM
VBAT
V5
V5DRV
CDH1
CBST1
CSW1
CDL1
CDL2
CSW2
CBST2
CDH2
PGND
PAD
TPAD68
51650_CF-IMAX
51650_GOCP-R
51650_SLEW
51650_GF-IMAX
51650_GSKIP#
51650_VRON
51650_VBAT
51650_V5
51650_V5DRV
51650_CDH1
51650_CBST1
51650_CSW1
51650_CDL1
VR_SVID_CLK
VR_SVID_ALERT#
VR_SVID_DATA
PR34 0_6
51650_GVFB
51650_GGFB
51650_GCSN1
51650_GCSP1
51650_GTHERM
51650_GPWM1
51650_GPWM2
51650_CPWM3
+3V
PC78 0.1u/10V_4
+VCC_GFX
PC80 *330p/50V_4
PR39 *10_4
PR38 0_4
PR37 0_4
PR36 *10_4
PC81 *0.01u/50V_4
VCC_AXG_SENSE
VSS_AXG_SENSE
Parallel
Close to the CPU side.
PC100 100p/50V_4
PR40 6.49K/F_4
PC79
51650_VREF
PR167 2.2/F_6
PC94 0.22u/25V_6
51650_CBST1
51650_CDH1
51650_CSW1
51650_CDL1
PQ25 FDMS3660S
PC121 0.1u/50V_6
PC120 4.7u/25V_8
PC119 4.7u/25V_8
PC5 220p/50V_4
PC98 15u/25V_3528
10/08 remove
PL6 8/14 0.24uH_7X7X3
DCR=1.19mOhm
PR181 2.2_6
PC133 2200p/50V_6
PR187 15.8K/F_4
PR186 0_4
PC7 0.1u/10V_4
PC114 10u/6.3V_6
PC118 330u/2V_3528
Close to the VR side.
PC112 *0.1u/25V_4
PC113 *0.1u/25V_4
PC1041 15n/10V_4
PR84 28.7K/F_4
PR176 100K/F_4_4250NTC
PR88 *140K/F_4
Close with phase1 inductor
Spec check
+VCC_CORE
TDC : 12A
PEAK : 25A
OCP : 32A
Width : 1000mil
VCORE Load Line : 2.9mV/A
AXG
PR164 2.2/F_6
PC75 0.22u/25V_6
51650_CBST3
PU7
TPS51601DRBR
BST
SKIP
PWM
GND
PAD
DRVH
SW
VDD
DRVL
51650_GSKIP#
51650_GPWM1
51650_CDH3
51650_CSW3
51650_CDL3
+5V_S5
PC76 1u/10V_4
PC64 0.1u/50V_6
PC65 4.7u/25V_8
PC66 4.7u/25V_8
PC2 220p/50V_4
PC61 15u/25V_3528
PL4 8/14 0.24uH_7X7X3
DCR=1.19mOhm
PR144 2.2_6
PC42 2200p/50V_6
PR31 15K/F_4
PR30 0_4
PC3 0.1u/10V_4
PC77 10u/6.3V_6
PC70 330u/2V_7343
PQ20 FDMS3660S
PC72 *0.1u/25V_4
PC73 *0.1u/25V_4
PC321 15n/10V_4
PR33 27.4K/F_4
PR156 100K/F_4_4250NTC
PR35 *191K/F_4
Close to the VR side.
Close with AXG inductor
Spec check
+VCC_GFX
TDC : 15A
PEAK : 22A
OCP : 33A
Width : 880mil
GFX_CORE Load Line : -3.9mV/A for GT2
+5V_S5
+1.05V_VTT
Close to VR
PR53 *0_4
PC88 0.1u/10V_4
PR165 54.9K/F_4
PR161 130K/F_4
PR163 *75K/F_4
51650_VRON
PR168 100K/F_4
VR_SVID_ALERT#
VR_SVID_DATA
VR_SVID_CLK
51650_VREF
1.7V
Thermal shutdown setting 104C
PR42 15.8K/F_4
PR66 15.8K/F_4
51650_GTHERM
51650_CTHERM
PR158 100K/F_4_4250NTC
PR58 100K/F_4_4250NTC
Place NTC close to the GFX_CORE Hot-Spot.
Place NTC close to the VCORE Hot-Spot.
Quanta Computer Inc.
PROJECT : EE3
Size
Document Number
+VCC_CORE/+VGFX (TPS51650)
Rev 1A
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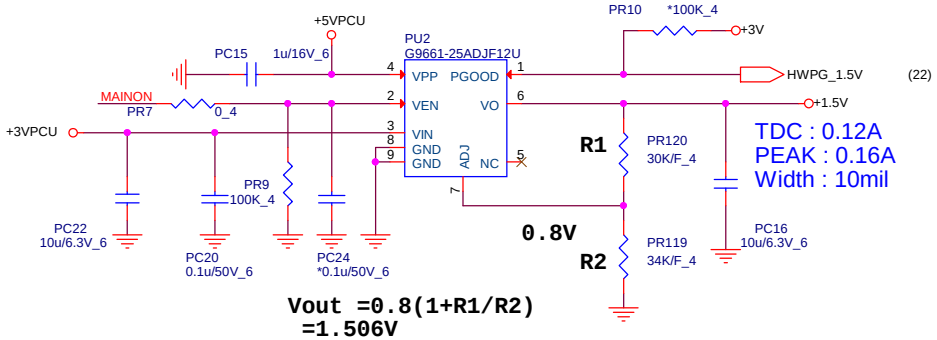
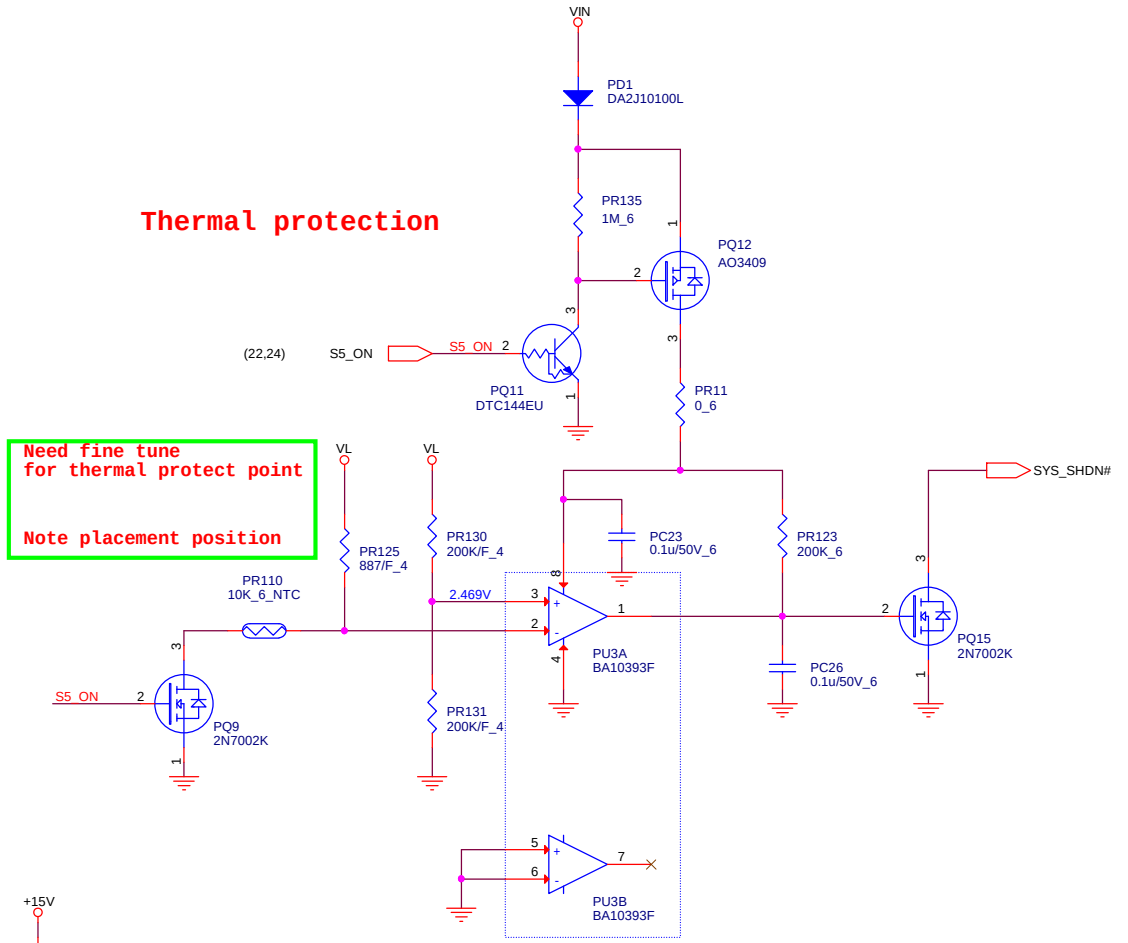


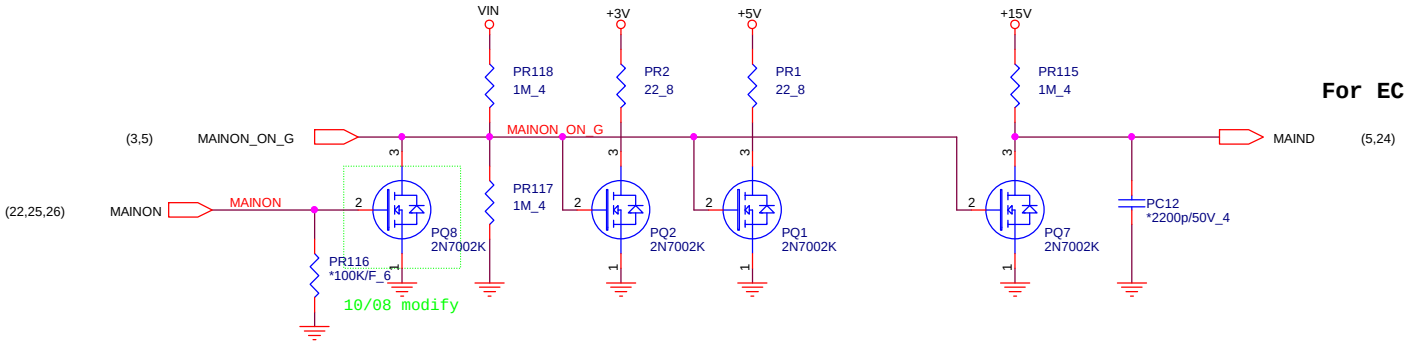
Vout =0.8(1+R1/R2)
=1.506V

C-test remove +1.8V

Thermal protection



For EC control thermal protection (output 3.3V)



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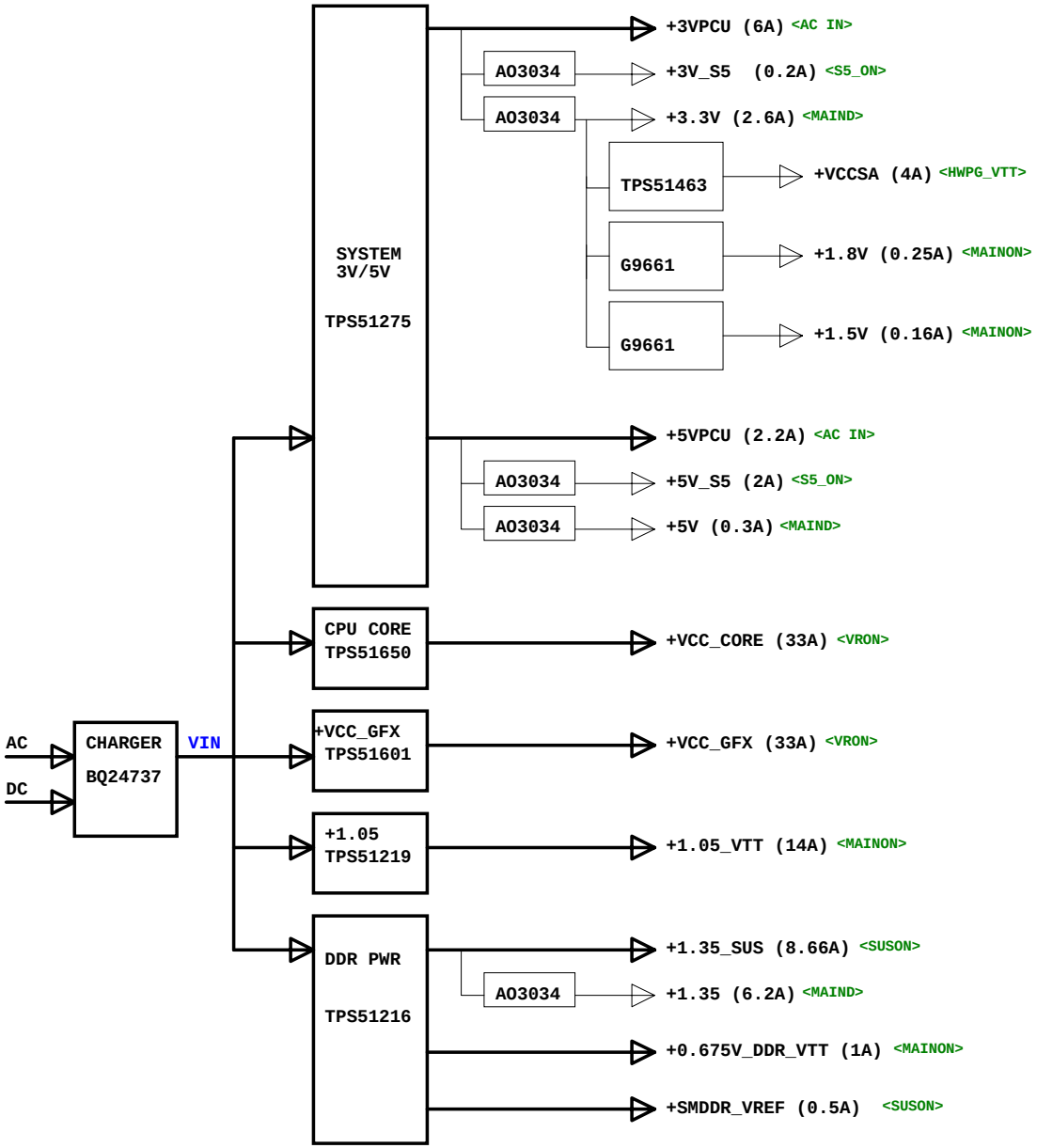
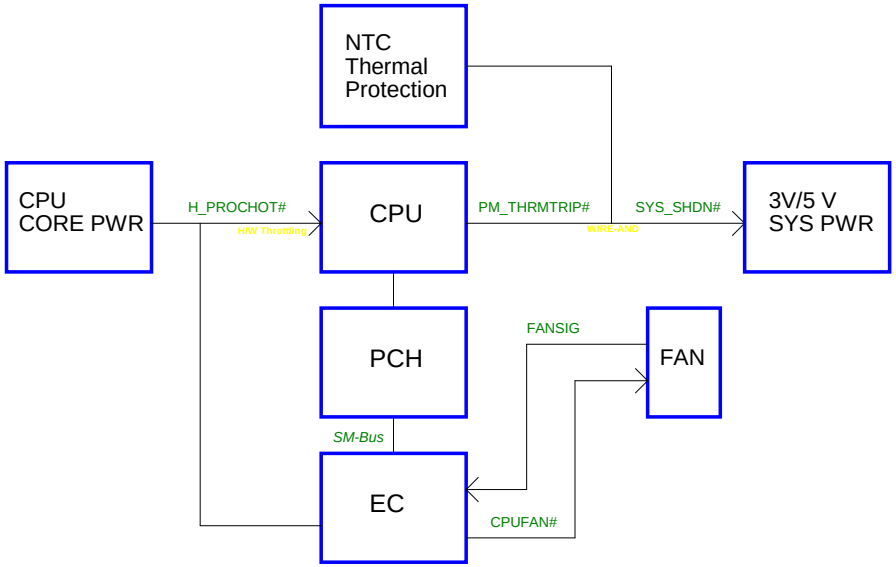
POWER TREE



Thermal Follow Chart



SM BUS ARRANGEMENT TABLE

SMBus	Function define	Address
SMB_PCH_CLK SMB_PCH_DAT	N/A	
SMB_ME0_CLK SMB_ME0_DAT	N/A	
SMB_ME1_CLK SMB_ME1_DAT	PCH - EC	0x96
STM_SCLK STM_SDATA	SENSOR HUB	
THM_CLK THM_DATA	EC - THERMAL	0x98
MBCLK MBDATA	EC - CHARGER EC - BATTERY	0x12 0x16

USB PORT TABLE

EHCI1		EHCI2	
USB0	CCD FRONT	USB8	CCD REAR
USB1	MB USB PORT	USB9	DEBUG RESERVE
USB2	TOUCH PANEL	USB10	BT
USB3	N/A	USB11	SENSOR HUB
USB4	N/A	USB12	POGO PIN
USB5	N/A	USB13	N/A
USB6	N/A		
USB7	N/A		

Quanta Computer Inc.
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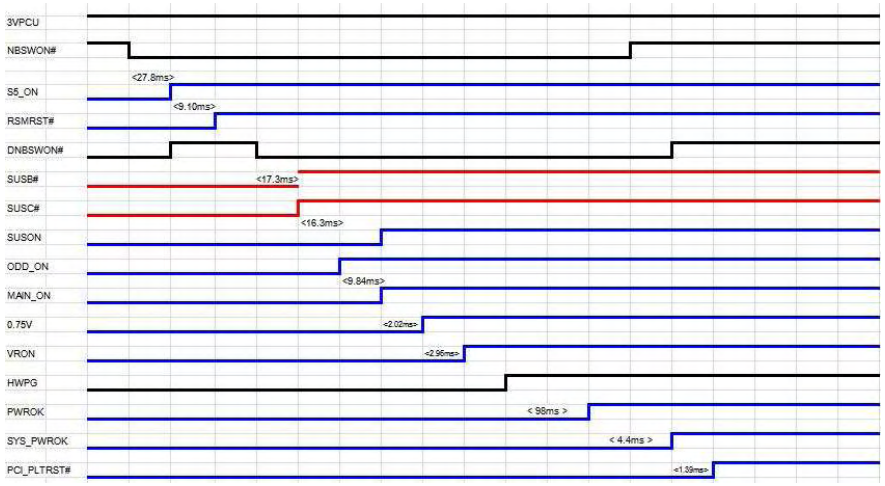

Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ALWAYS	S0	S3	S5
VIN	+10V~+19V	MAIN POWER	ALWAYS	O	O	O	O
+3V_RTC	+3V~+3.3V	RTC POWER	ALWAYS	O	O	O	O
+3VPCU	+3.3V	EC POWER/WLAN/Hall sensor/PCH	ALWAYS	O	O	O	O
+5VPCU	+5V	CHARGE POWER/1.5V PWM	ALWAYS	O	O	O	O
+15V	+15V	CHARGE PUMP POWER	ALWAYS	O	O	O	O
+3V_S5	+3.3V	LAN/SPI/TPM POWER/PCH	S5_ON		O	O	O
+5V_S5	+5V	USB/PCH POWER	S5_ON		O	O	O
+5V	+5V	HDD/ODD/Codec/HDMI POWER	MAINON		O		
+3V	+3.3V	PCH/GPU/Peripheral component/TP POWER	MAINON		O		
+1.35V_SUS	+1.35V	CPU/SODIMM CORE POWER	SUSON		O	O	
+0.675V_DDR_VTT	+0.675V	SODIMM Termination POWER	MAINON		O		
+VCC_GFX	variation	Internal GPU POWER	VRON		O		
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON		O		
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON		O		
+1.05V_VTT	+1.05V	PCH CORE POWER/IVY/SNB bridge VCCIO	MAINON		O		
+VCCSA	+0.9V	CPU POWER	HWPG_VTT		O		
+VCC_CORE	variation	CPU CORE POWER	VRON		O		
LCDVCC	+3.3V	eDP LCD POWER	LVDS_VDDEN		O		

Model	REV	CHANGE LIST
		FIRST RELEASED
EE3	1A	

CHANGE LIST

Model: EE3

FIRST RELEASED

1A

- 20120917 add R528 pull-up LCDINT to +3V
- 20120917 add C511 on TPM thermal sensor
- 20120917 change C110 to 1.8P between M_A_CLK0,M_A_CLK0#
- 20120917 del PJ1
- 20120918 Change PR145 for +5V OCP setting.
  Change PR140 for +3V OCP setting
  Change PC104 for Vcore DCR network
  Change PC82 for AXG DCR network
  Change PR72 for droop voltage setting
- 20120924 change C427 footprint to 0402
- 20121005 SWAP wireless TX,RX
- 20121008 C429,C430 change to 22p
- 20121008 remove jumper JP1~JP11
- 20121008 Change PQ5&8 to 2n7002K from DTC144EU
- 20121008 stuff R728,R730,R731,R732 EMI request for HDMI
- 20121008 add HE1,HE2
- 20121009 add 4-ch edp circuit
- 20121009 remove USB2 to EDP conn
- 20121009 modify CN7 add +5V_POGO to 3 pin
- 20121011 change R354,R342 to 56 ohm
- 20121011 change SW2 footrprint
- 20121011 change EC pin define POGO_PRSNT# (GPIO91), WAKE_SRC_1 (GPIO06)
- 20121011 add R556 pull high to +3V
- 20121011 add R557,R558 switch POGO power
- 20121011 chagne sensor hub USB to port 3
- 20121012 chagne POGO USB to port 11
- 20121013 EC add FWSC for 200msce timing and R559 to jump.
- 20121014 change Q23.2 to GND
- 20121014 sensor hub change to INTEL solution

2A

- 20121026 stuff R559 unstuff R159 ,change APWROK sequence
- 20121026 change R344,R365 circuit, unstuff Q11,Q8
- 20121116 change M1 footprint &P/N
- 20121116 change U4 footprint
- 20121116 change CN9 Mini pciE footprint
- 20121120 remove 4-ch edp circuit
- 20121120 change CN2 footprint & P/N, remove Pin10 +3V_S5
- 20121120 remove PU1 +1.8V plane
- 20121129 change PL4,PL6 footprint

MODEL	Z09 FROM	Z09 To
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	2A	3A
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B