ZK6 MB Block Diagram

VER : 1A

BOM P/N	Description
31ZK6MB0000 41ZK6CS0000 51ZK6SS0000 31ZK6MB0010 41ZK6CS0010 51ZK6SS0010	uma / mxm 00 / 10

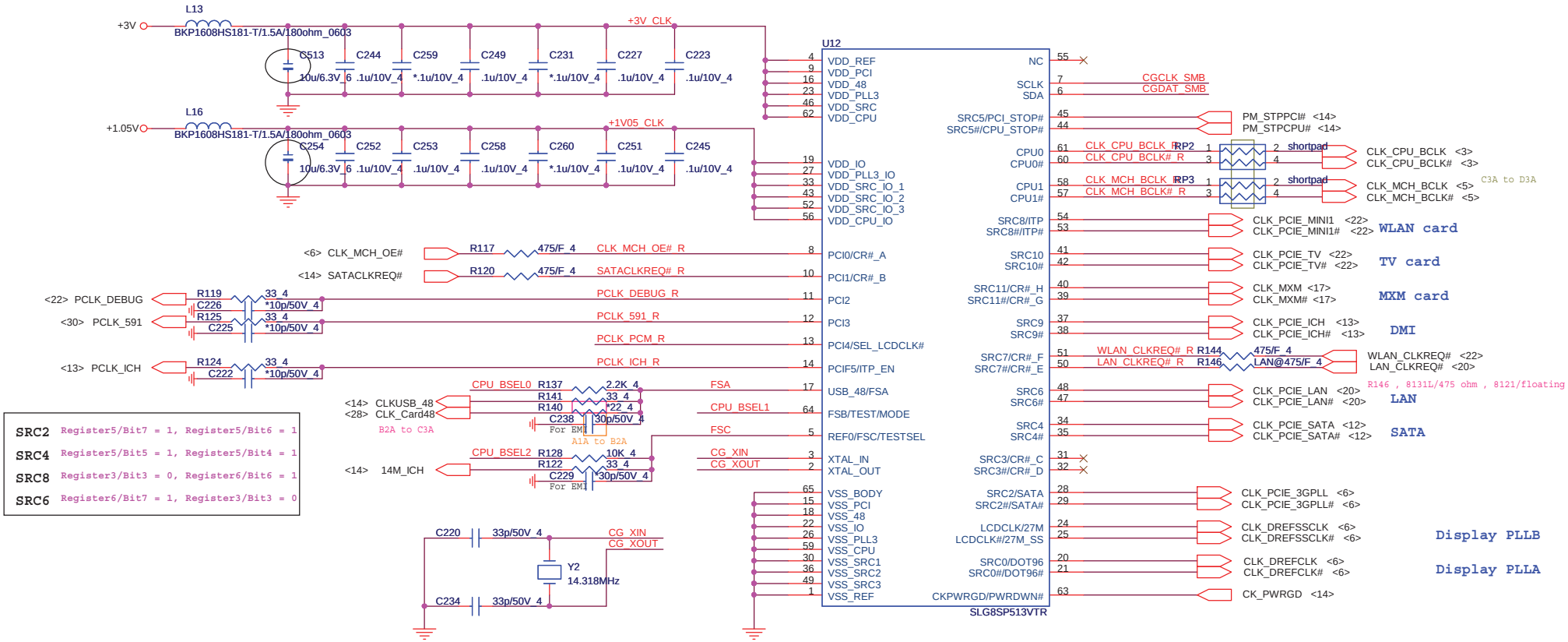
BOM Option Table

Reference	Description
I@	INT VGA
E@	EXT VGA
SP@	SPECIAL FOR EXT/INT VGA
*	DNI

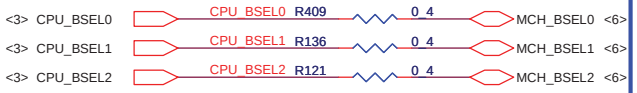
PENRYN 479 uFCPGA P3,4
FSB
LM95245 Thermal Sensor P3
Fan Driver P29
FSB(800/1066MHZ)
PCIE
CH7318 HDMI Level Shifter P19
HDMI Con. P19
SLG8SP513VTR CLOCK GENERATOR P2
X'TAL 14.318MHz
FSB
CANTIGA NB P5,P6,P7,P8, P9,P10,P11
DDR SYSTEM MEMORY
Graphics Interfaces
DMI
PCI-E x16
MXM 3 P17
EXT_HDMI
EXT_CRT
EXT_LVDS
INT_CRT
INT_LVDS
SWITCH CIRCUIT P18,P19
CRT Con. P18
LVDS/CCD/MIC Con. P18
USB-11
Int. MIC
DDRIII-SODIMM1
DDRIII-SODIMM2 P16
Dual Channel DDR III 800/1066 MHZ
DMI(x4)
SATA - HDD P23
SATA 0 & SATA 4
SATA - ODD P23
SATA 1
SATA 5
TI SN75LVCP412 Maxim 4951 Re-driver P28
USB/eSATA P28
USB-1
DMI
SATA
PCI-E
Intel ICH9M SB P12, 13, 14, 15
USB
RTC
IHDA
LPC
PCIE-2 & PCIE-4
MINI CARD WLAN/ TV P22
USB-2 & USB-3
PCIE-6
AR8131 GIGA LAN P20
X'TAL 25MHz
RJ45 P21
CCD P18
USB-6
USB Port x2 P28
USB-0 & USB-10
USB 2.0 (Port0~9)
USB/B Con. P28
USB-4 & USB-7
X'TAL 32.768KHz
Bluetooth Con. P21
USB-5
BATTERY P12
Finger Printer P29
USB-9
RTS5159 Cardreader Controller P26
FFC cable
Cardreader Con. 4 IN 1 P26
Azalia
MDC Con. P24
cable
RJ11 WIRE CONN.
LPC
X'TAL 32.768KHz
WPC775LDG EC P30
ALC888S-VC AUDIO CODEC P24
Int. MIC
MIC
MIC JACK P24
Power Board Con. P27
CIR P30
MMB Board Con. P27
Touch Pad Board Con. P29
AN12947A AUDIO AMP P25
MAX9737 SUB AMP P25
LINE IN P25
K/B Con. P29
W25X16VSS1G SPI FLASH P30
EM-6781-T3 HALL SENSOR P18
HP/SPDIF P25
Speaker P25
SUBWOOFER P25
THERMAL PROTECTION P36
2.5V/ 1.5V PWR DISCHARGER P37
ISL6251 CHARGER P31
ISL6237 3/5V SYS PWR P32
ISL6262A CPU CORE PWR P33
RT8202 +1.05V P34
ISL6263A +1.05V_AXG P35
TPS5116 DDR PWR P36
POWER TREE P38

Quanta Computer Inc.
PROJECT : ZK6
Size: Document Number: Block Diagram Rev 1A
Date: Friday, April 24, 2009 Sheet 1 of 42

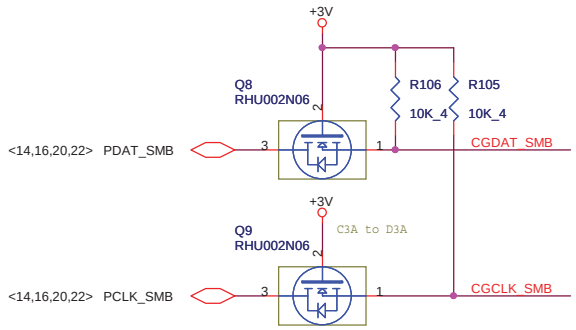
Clock Generator



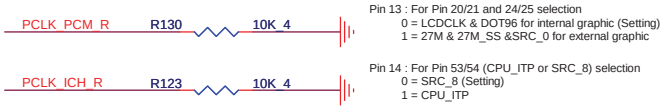
CPU Clock select



FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

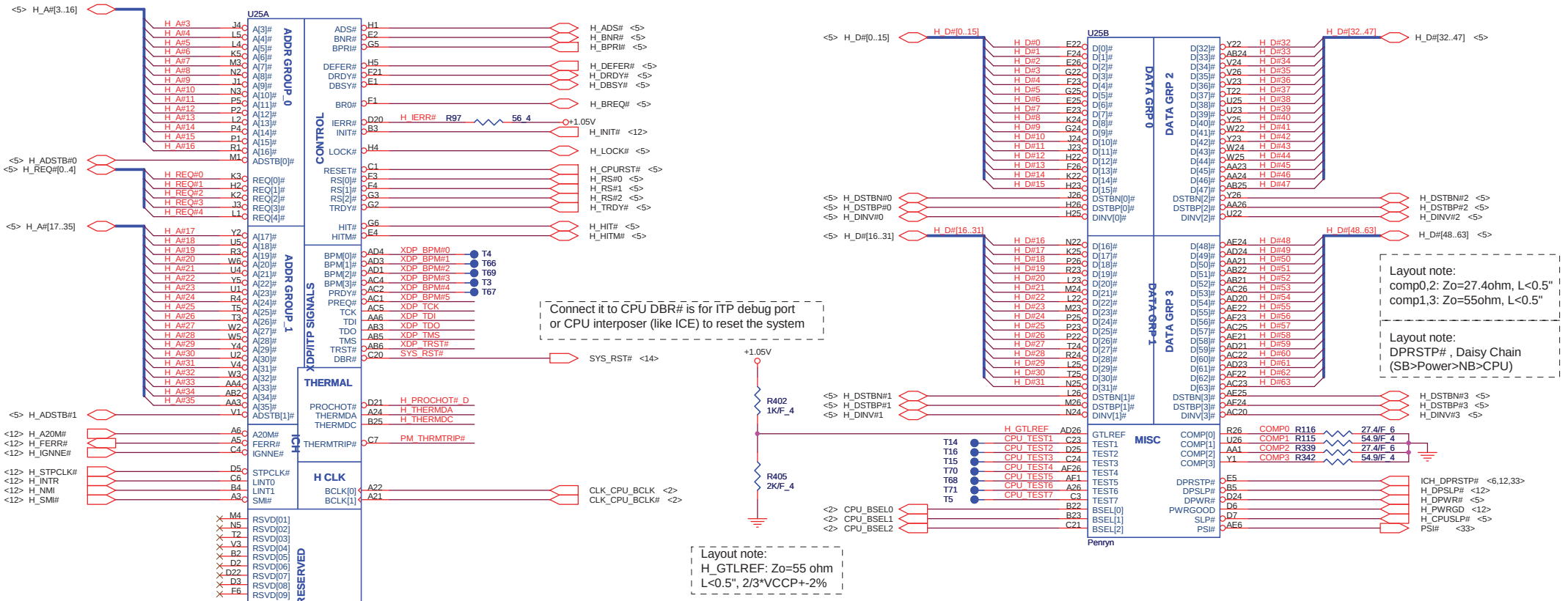


Clock Generator Strap table

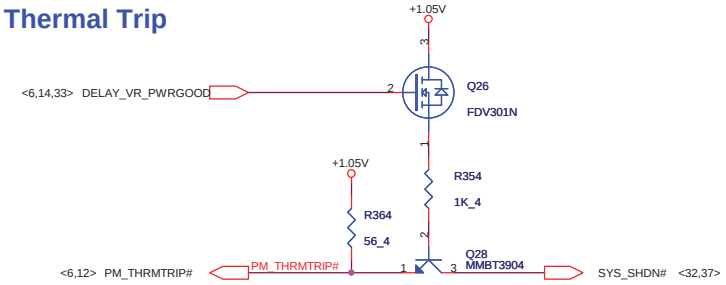


Quanta Computer Inc.
PROJECT : ZK6

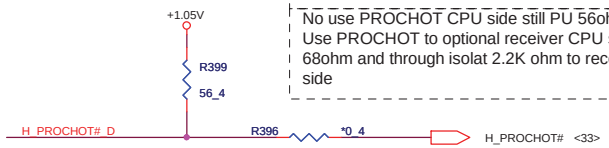
Size	Document Number	Rev
	CLOCK GENERATOR	1A
Date: Friday, April 24, 2009	Sheet 2 of 42	



Thermal Trip



Processor hot

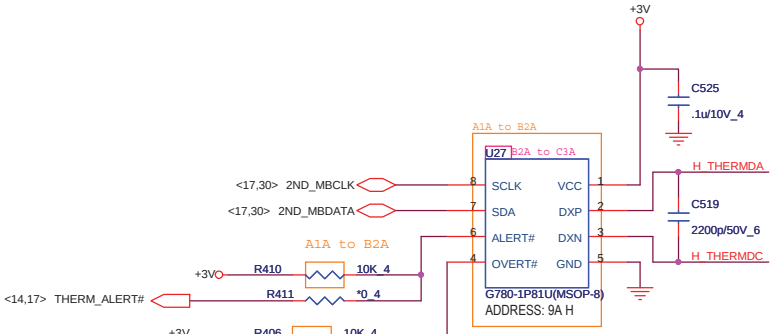


No use Thermal trip CPU side still PU 56ohm.
Use Thermal trip can share PU at SB side

No use PROCHOT CPU side still PU 56ohm.
Use PROCHOT to optional receiver CPU side PU 68ohm and through isolat 2.2K ohm to receiver side

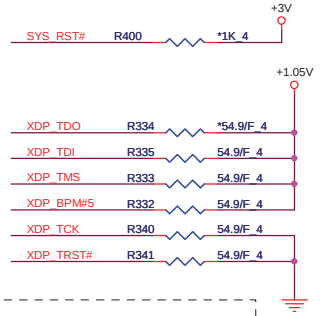
CPU 1/2

CPU Thermal monitor



NS	none
WINDBOND	AL83L771K02
GMT	AL000780003

XDP PU/PD



XDP_DBRESET# and XDP_TDO reserve for XDP

Quanta Computer Inc.
PROJECT : ZK6

Size	Document Number	Rev
	CPU Host Bus	1A
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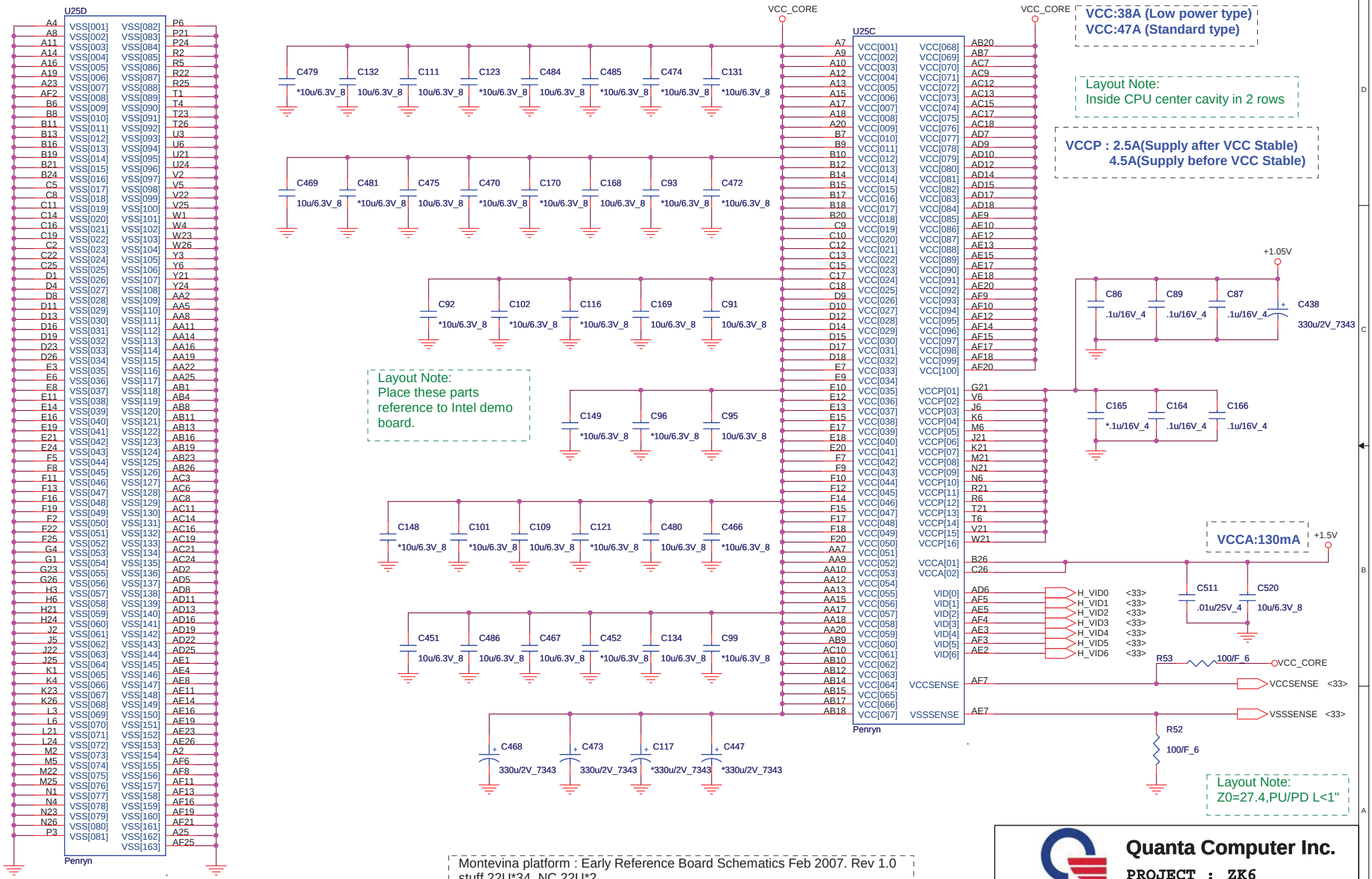
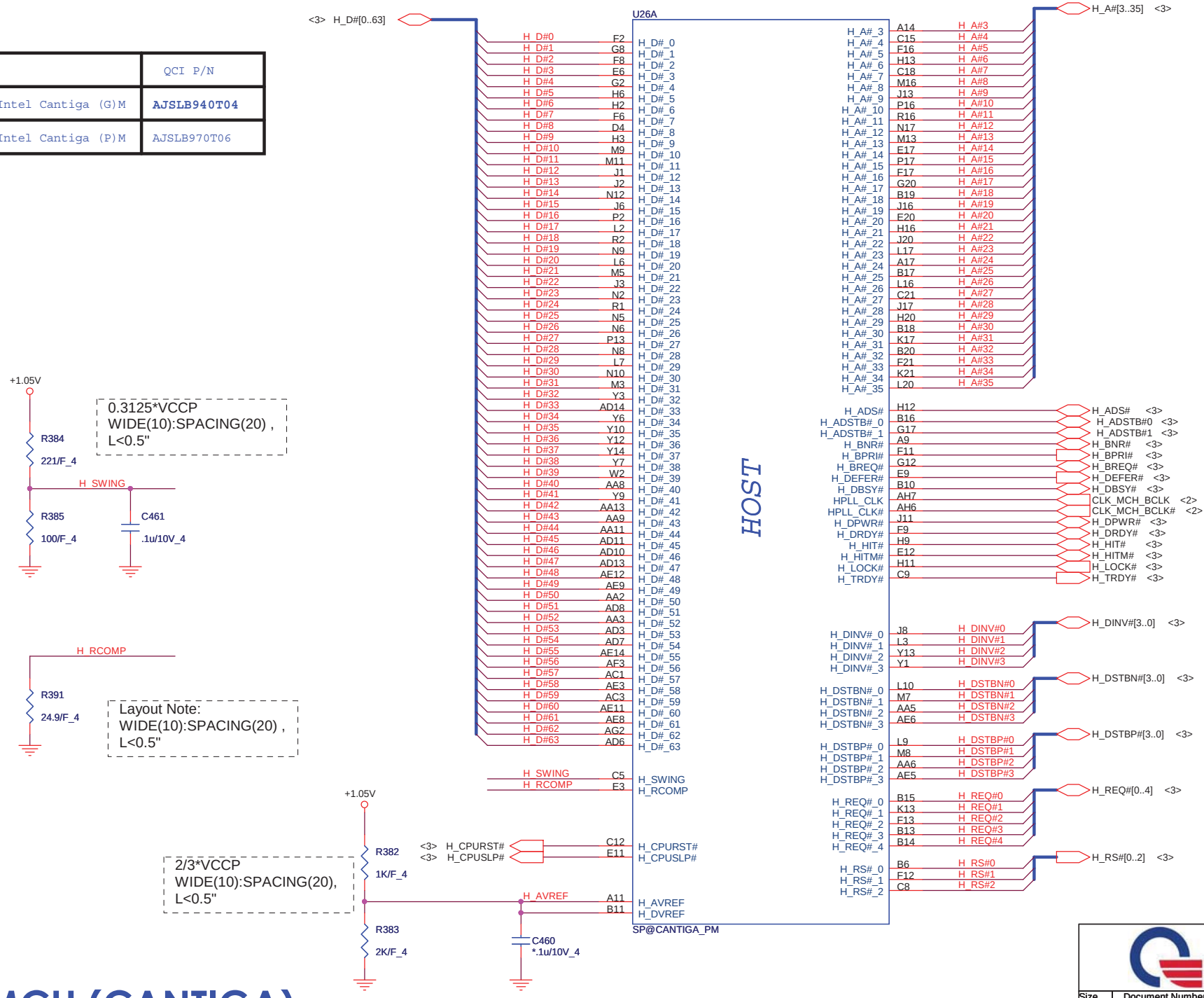


	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06



GMCH (CANTIGA)

Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	GMCH HOST	1A
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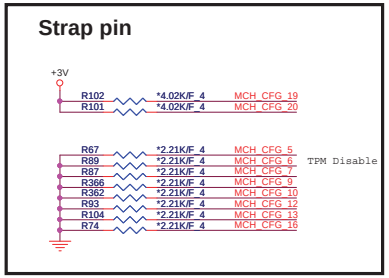
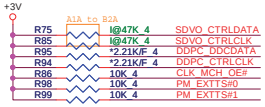
IV@
EV@

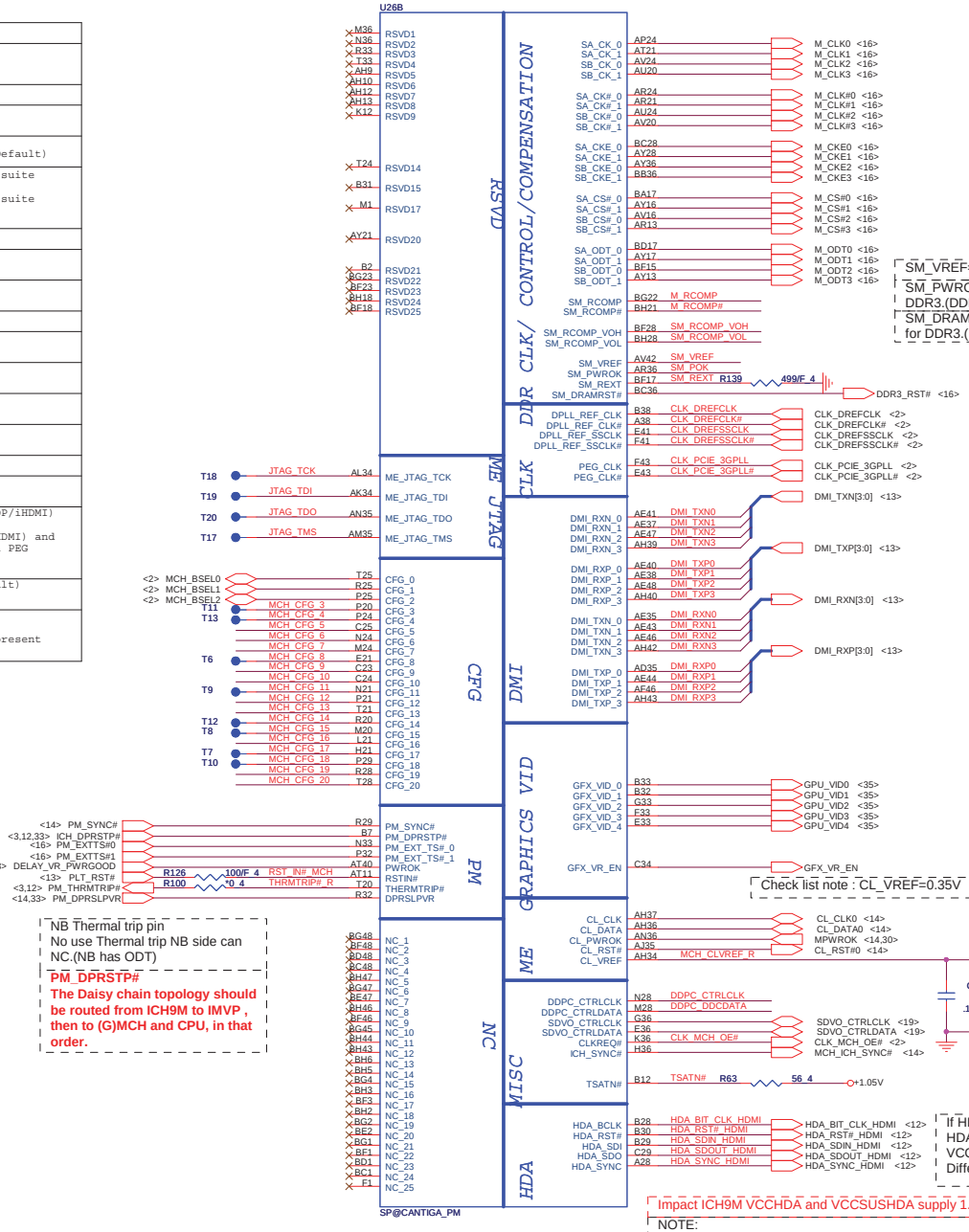
Strap table

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000= FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

Strap pin







NB Thermal trip pin
No use Thermal trip NB side can NC.(NB has ODT)

PM_DPRSTP#
The Daisy chain topology should be routed from ICH9M to IMVP , then to (G)MCH and CPU, in that order.

SM_VREF=0.5*VCC_SM
SM_PWROK only for DDR3.(DDR2 PD only)
SM_DRAMRST# only for DDR3.(DDR2:NC)

Check list note : CL_VREF=0.35V

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

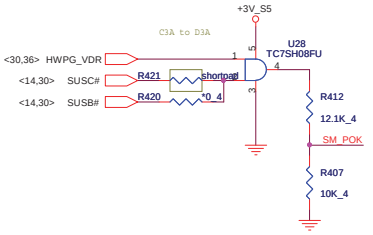
If HDMI not support
HDA --> NC
VCC_HDA-->GND
Differential signal-->NC

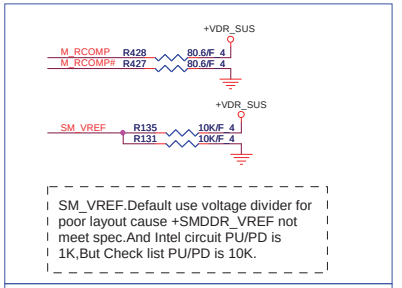
DDPC_CTRL for HDMI port C
SDVO_CTRL for HDMI port B

<Checklist ver0.8>
If TSATN# is not used, then it must be terminated with a 56-Ω pull-up resistor to VCCP.

<Pin out check issue>
Cantiga EDS 0.7 change Ball B12 to TSATN# from TSATN

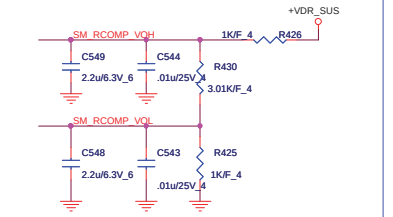
DDR3 PWROK



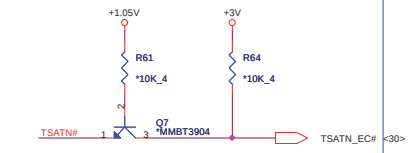


SM_VREF.Default use voltage divider for poor layout cause +SMDDR_VREF not meet spec.And Intel circuit PU/PD is 1K,But Check list PU/PD is 10K.

INTEL FAE Suggest PD for Ext graphics



NB Thermaltrip



<Checklist ver0.8>
If TSATN# is not used, then it must be terminated with a 56-Ω pull-up resistor to VCCP.

<Pin out check issue>
Cantiga EDS 0.7 change Ball B12 to TSATN# from TSATN

GMCH (CANTIGA)

Quanta Computer Inc.
PROJECT : ZK6
Size | Document Number: GMCH DMI | Rev 1A
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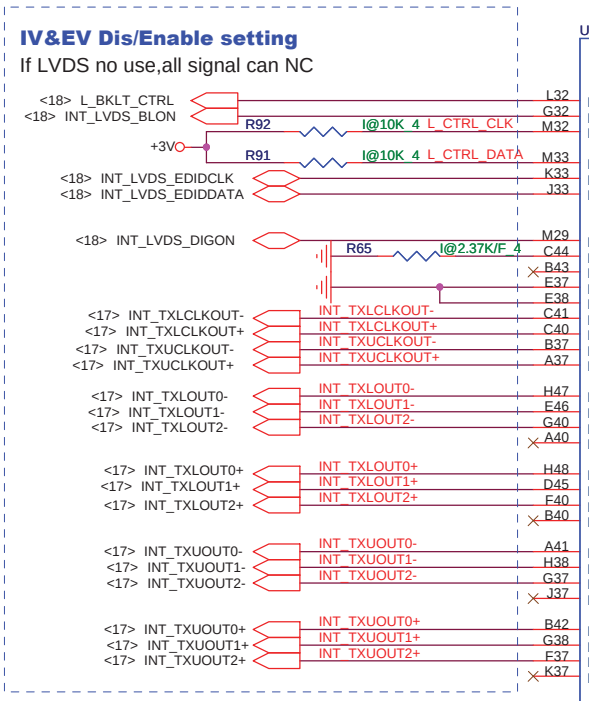
IV@

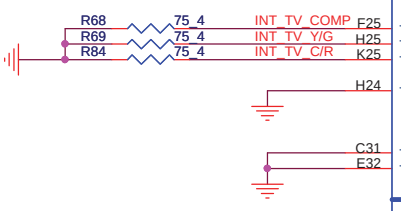
EV@

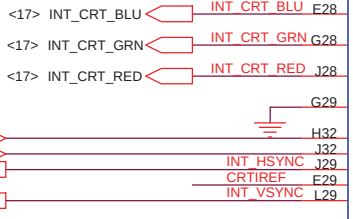
SP@

IV&EV Dis/Enable setting

If LVDS no use,all signal can NC

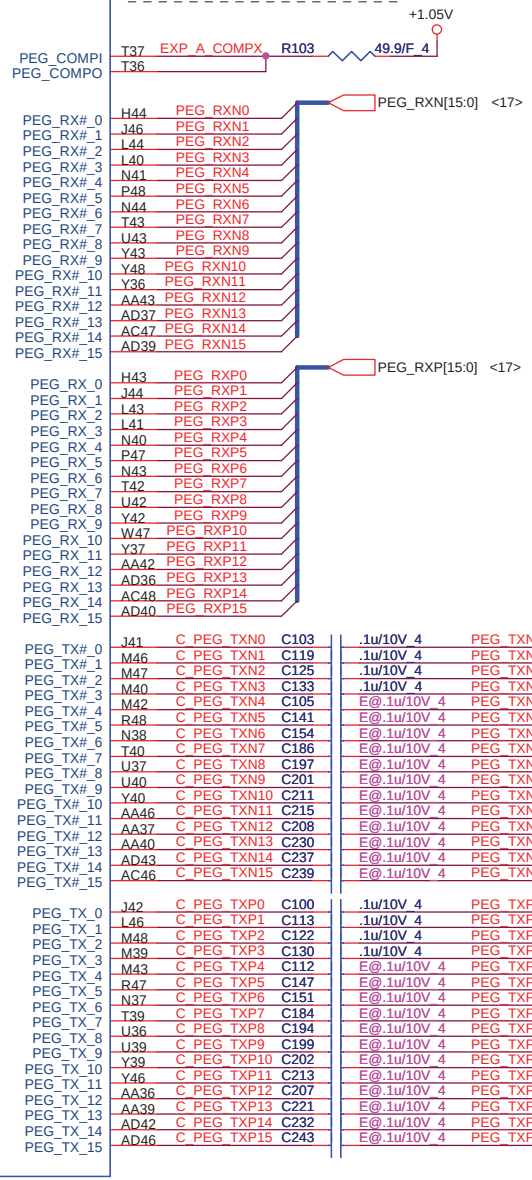






SP@CANTIGA_PM

L<0.5" , If PCIE not support still connect to +VCC_PEG



IV&EV Dis/Enable setting

<5/31>Montevina_Schematics_Checklist_Rev0_8
a)For TVOUT Disabled, TV_DCONSEL[1:0] Connect to GND. But design guide Rev0.7 show NC.What is correct.
b)For CRT DAC Disable, CRT_DDC_CLK, CRT_DDC_DATA . CRT_HSYNC, CRT_VSYNCThese signals should be connected to GND. But design guide Rev0.7 show NC, Intel suggest follow Design guide.

<check list>	<check list>
For EV@	For IV@
CRT R/G/B 0ohm to GND	CRT R/G/B 150ohm to GND
CRTIREF 0ohm to GND	CRTIREF 976 ohm to GND (>12")

CRTIREF
For IV: 1.02Kohm
For EV:0ohm

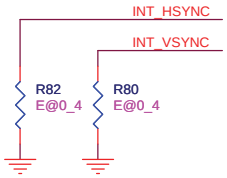
R72 SP@1K/F_4 CRTIREF

SP@

CRT_R/G/B
For IV: 150ohm
For EV:0ohm

R73 SP@150_4 INT_CRT_BLU
R83 SP@150_4 INT_CRT_GRN
R88 SP@150_4 INT_CRT_RED

MXM STUFFED.



CRTIREF pull down for IV cantiga 1.02k ohm/F

Quanta Computer Inc.		
PROJECT : ZK6		
Size	Document Number	Rev 1A
	GMCH VGA	
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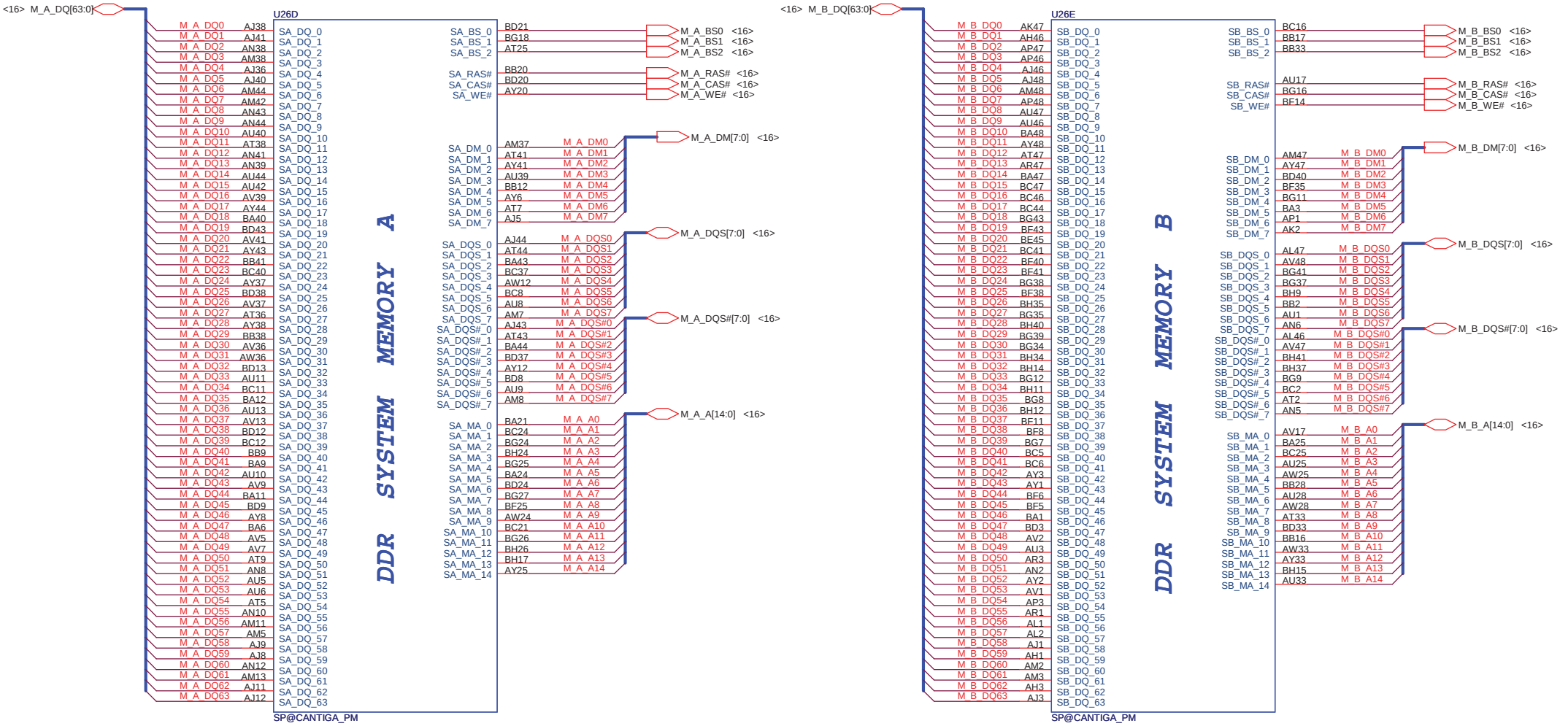

GMCH (CANTIGA)

Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	GMCH DDRIII	1A

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IV@

SP@

VCC_SM(1.5VSUS)
DDR3(800M) : 3162.5mA
DDR3(1067M) : 4140mA

Intel check list(Rev 0.8)
No description for VCC_SM bulk CAP
Intel CRB(Rev 0.7)
330U*1 Reserve near to power
330U*1 near to NB

Intel check list(Rev 0.8)
270U*1 near to power(+V1.05M).
270U*2 near to NB
Intel CRB(Rev 0.7)
270U*3 near to power(+V1.05M).
270U*1 near to NB
ESR=12m ohm

+VDR_SUS
C247 22u/6.3V_8
C217 22u/6.3V_8
C218 .1u/10V_4
C539 330u/2V_7343

U26G
VCC_SM_1 … VCC_SM_42
VCC_SM_36/NC … VCC_SM_42/NC
VCC SM POWER

+1.05V_AXG
VCC_AXG_NCTF_1 … VCC_AXG_NCTF_60
VCC GFX NCTF

1.05V
Graphics core
VCC_AXG
VCC_AXG_NCTF
6326.84mA

VCC_AXG_1 … VCC_AXG_42
VCC_AXG_SENSE
VSS_AXG_SENSE
VCC GFX

Voltage regulator is shared between the Graphics Core Rail, VCCA_HPLL,VCCA_MPLL,VCCA_PEG_PLL,VCCD_PEG_PLL, VCCA_SM_CK, VCCA_DPLLA, VCCA_DPLLB, VCCD_HPLL, VCCA_SM, VCC_AXF

IV@
Differential routing
<35> GFX_VCCSENSE
<35> GFX_VSSSENSE
R114 I@10/F_4
R110 I@10/F_4

1.8V
Internal connect to power
VCC_SM_LF1 … VCC_SM_LF7
VCC SM LF
C240 .1u/10V_4
C206 .1u/10V_4
C233 .22u/6.3V_4
C228 .22u/6.3V_4
C204 .47u/6.3V_4
C242 1u/10V_4
C236 1u/10V_4

1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm and VSS_AXG_SENSE PD with 10ohm for Intel suggest

SP@CANTIGA_PM

+1.05V
C190 .1u/10V_4
C210 .22u/6.3V_4
C212 .22u/6.3V_4
C161 22u/6.3V_8
C188 330u/2V_7343
Place close to the GMCH

U26F
VCC_1 … VCC_35
VCC CORE POWER

IV@
+1.05V
+1.05V_AXG
+1.05V_AXG_POWER
R357 I@0 8
R346 I@0 8
R353 I@0 8
R345 *0 8
R343 *0 8
R344 *0 8

IV&EV Dis/Enable setting
Design guide(Table 72)
For INT VGA diasble.VCC_AXG power can connect to GND

+1.05V_AXG
SP@
C189 I@330u/2V_7343
C504 I@330u/2V_7343
C177 I@.47u/6.3V_4
C187 SP@1u/10V_6
C181 I@10u/6.3V_8
C176 I@22u/6.3V_8
C183 I@.1u/10V_4
C179 I@.1u/10V_4
C178 I@.1u/10V_4
Place close to the GMCH
SP@IV Sutff 1uf
EVstuff 0 ohm
Cavity Capacitors

Intel check list(Rev 0.8)
220U*2 near to NB(ESR=15m ohm)
Intel CRB(Rev 0.7)
270U*4 near to power(+V1.05S).
330U*2 near to NB

VCC_NCTF_1 … VCC_NCTF_44
VCC NCTF POWER

VCC
VCC_NCTF
1210.34mA_EV
1930.4mA_IV
ME Engine
508.12mA
Total Max=2438.52mA

Quanta Computer Inc.
PROJECT : ZK6
Size | Document Number: GMCH VCC,NCTF | Rev 1A
Date: Friday, April 24, 2009 | Sheet 9 of 42

Power consumption reference to Intel Cantiga chipset EDS Volume1. Section 10

IV@
EV@
SP@

External Graphics (GMCH Integrated Graphics Disable)

VCCSYNC_CRT	GND
VCCA_CRT_DAC	GND
VCCD_LVDS	GND
VCC_TX_LVDS	GND
VCCA_LVDS	GND
VCCA_TVDAC	GND
VCCD_QDAC	GND
VCCA_DAC_BG	GND
VCC_AXG	GND
VCC_AXG_NCTF	GND

IV&EV Dis/Enable setting
SP@:INT use 0.01U
EXT use 0 ohm

1210 10UH, 10%
0.45A DCR_max = 0.39

IV&EV Dis/Enable setting
SP@:INT use 0.1U
EXT use 0 ohm

1.05V
64.8mA for DPLL_A/B

3.3V
73mA

3.3V
5mA

VCCA_DPLLA/B always keep to +1.05V
(If no use IV dynamic core power)

1210 10UH, 10%
0.45A DCR_max = 0.39

ESR=15 m

1.05V
24mA

1.8V
13.2mA

1.5V
414uA

1.05V
DDR2-800
720mA

1.05V
50mA

VCCA_PEG_PLL
+1.25V for Teenah use(100mA)

1.05V
139.2mA

1210 0.1uH, 20%, 1A,
DCR_max=0.078Ω

8.9 nH, 0.2 nH, 1A
DCR_max=32 m

1.05V
DDR2-800
26mA

CRB : 0 ohm
Check list : 2.2nH

3.3V
24.15mA for VCCA_TVA_DAC
39.48mA for VCCA_TVB_DAC
24.15mA for VCCA_TVC_DAC
Total 87.78mA

FB 180@100 MHz, 25% 1.5A
DCR_max=90 m

3.3V
79mA

IV&EV Dis/Enable setting
SP@:INT use 0.01U
EXT use 0 ohm

CRB no 10U
Check list need min 10U~100U for VCCA_TV_DAC

1.5V
50mA

SP@:INT use 0.1U
EXT use 0 ohm

VCCD_QDAC share to TV and CRT

VCCD_TVDAC always keep 0.1U/0.022U/10U to +1.5V

1.5V
35mA

1.5V
48.363mA for CRT
5mA for TV

FB 180@100 MHz, 25% 1.5A
DCR_max=90 m

1.5V
0.5mA

CRB no 10U
Check list need min 10U~100U
for VCCA_QDAC

FB 220 @100 MHz, 25%, 2A

1.05V
50mA

1.05V
157.2mA

IV&EV Dis/Enable setting
SP@:INT use 1 U
EXT use 0 ohm

LVDS digital(1.8V)
60.31mA

1.05V
FSB-1067
852mA

ESR= 12m ohm

Check list : 0.1UH
CRB : 0 ohm
1210 0.1 ?H, 20% 1A
DCR max = 78 m

1.05V
321.35mA

ESR = 60 m

Clock supply(1.5V)
DDR3(1066):149.5mA

0805 1UH , Rdc = 0.14 - 0.26.
Max rated current = 220 mA

IV&EV Dis/Enable setting
SP@:INT use 1000pf
EXT use 0 ohm

0805 100 nH, DCR=160 m

LVDS Transmitter(1.8V)
118.8mA

3.3V
105.3mA

1.05V
1782mA

1.05V
456mA

1.05V
Internal connect to power

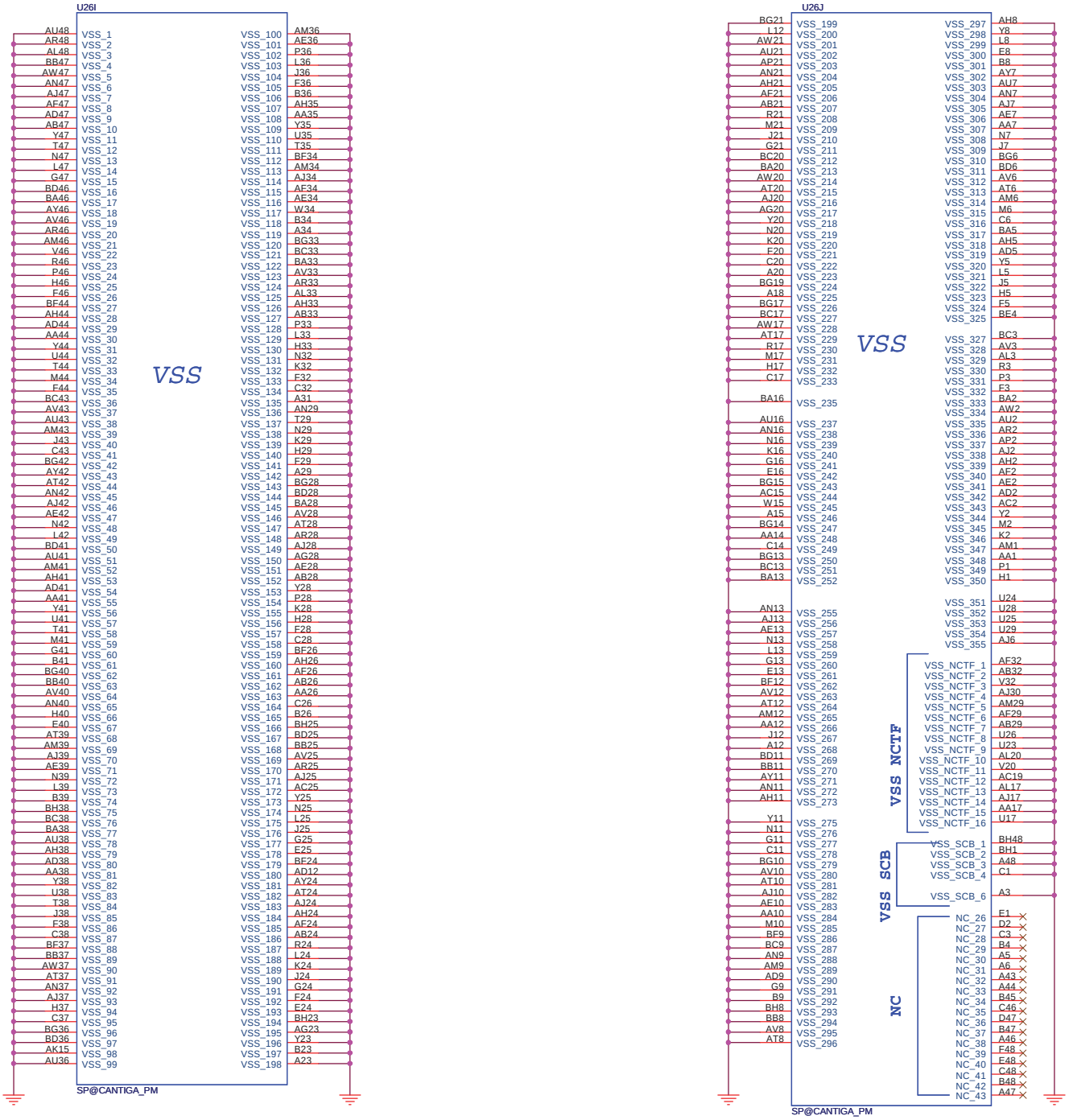
Power Net Name	Cantiga(V)
VCC_AXG_# VCC_AXG_NCTF_#	1.05V
VCCA_PEG_BG	1.5V
VCCA_DPLLA	1.05V
VCCA_DPLLB	1.05V
VCCA_SM_#	1.05V
VCCA_HPLL	1.05V
VCCA_MPLL	1.05V
VCCA_SM_CK_#	1.05V
VCCA_PEG_PLL	1.05V
VCC_AXF_#	1.05V
VCCD_HPLL	1.05V
VCCD_PEG_PLL	1.05V

GMCH (CANTIGA)

Quanta Computer Inc.
PROJECT : ZK6

Size	Document Number	Rev
	GMCH POWER	1A

Date: Friday, April 24, 2009 Sheet 10 of 42



GMCH (CANTIGA)

Quanta Computer Inc.

PROJECT : ZK6

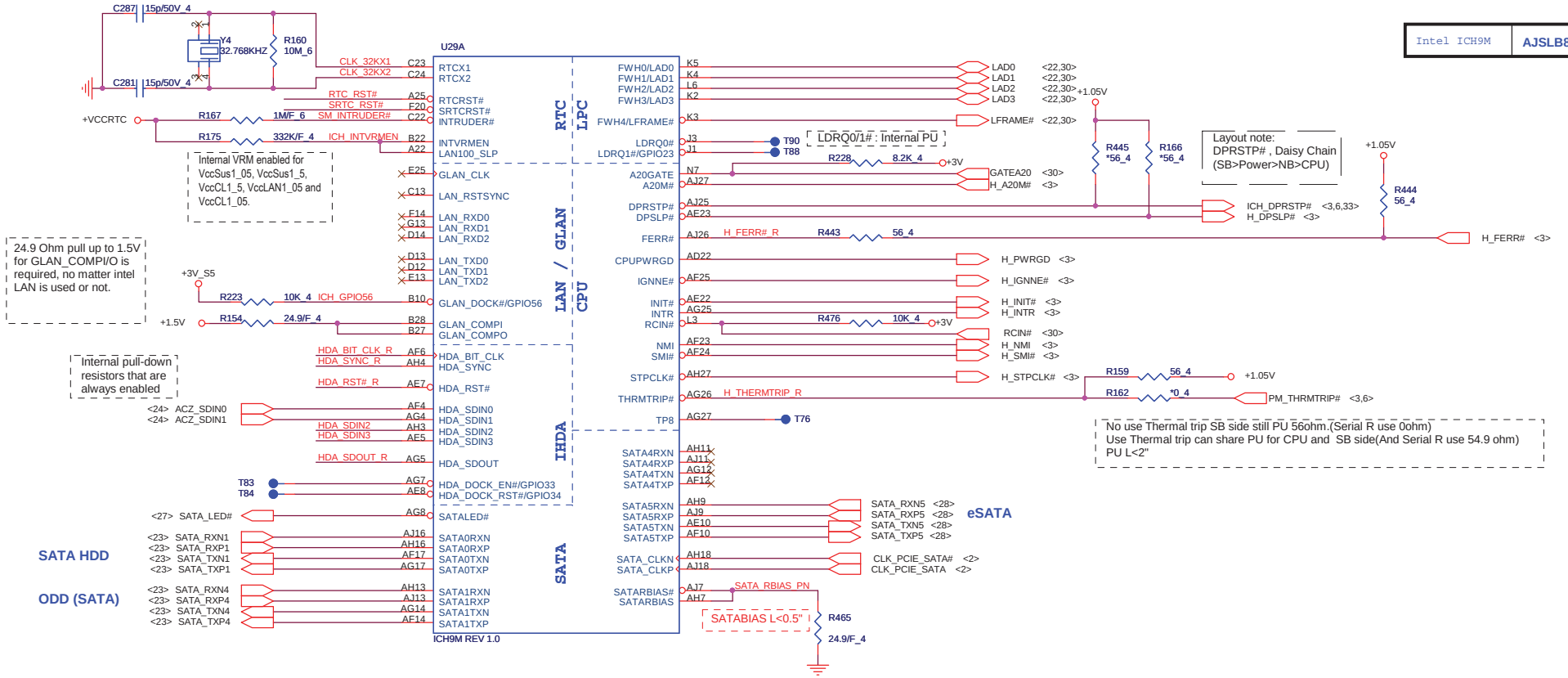
Size	Document Number	Rev
	GMCH VSS	1A
Date: Friday, April 24, 2009	Sheet 11 of 42	

ICH9M

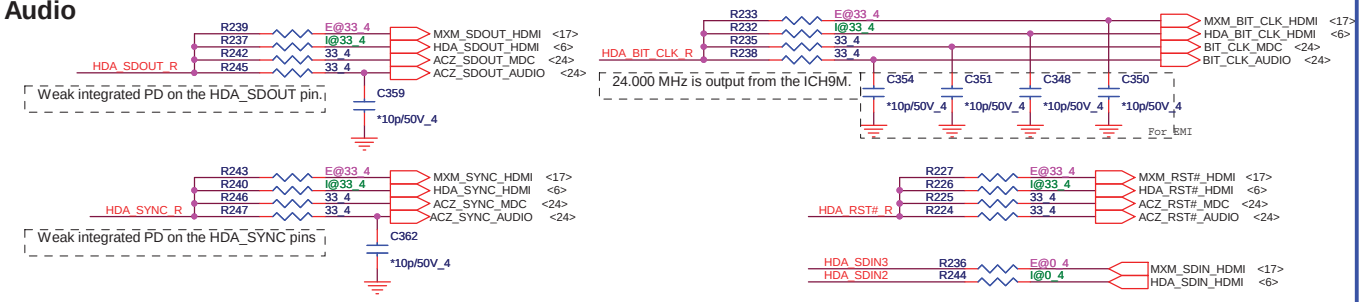
IV@

EV@

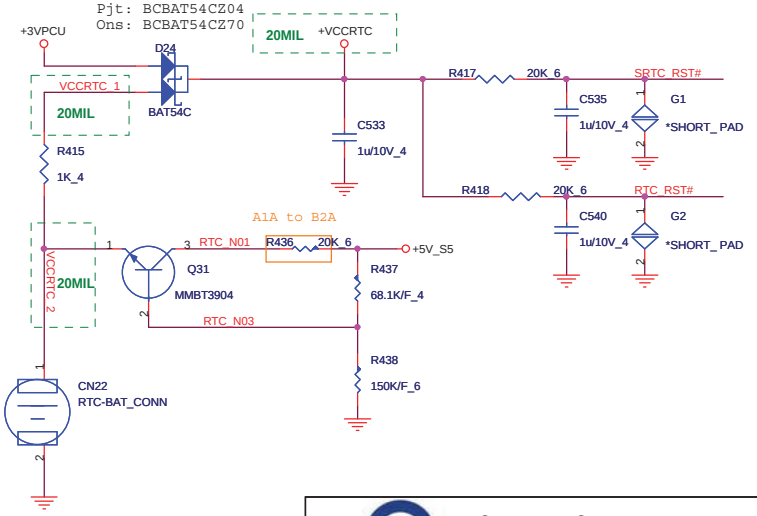
Intel ICH9M | AJSLB8Q0T03



HD Audio



RTC



South Bridge Strap Pin (1/3)

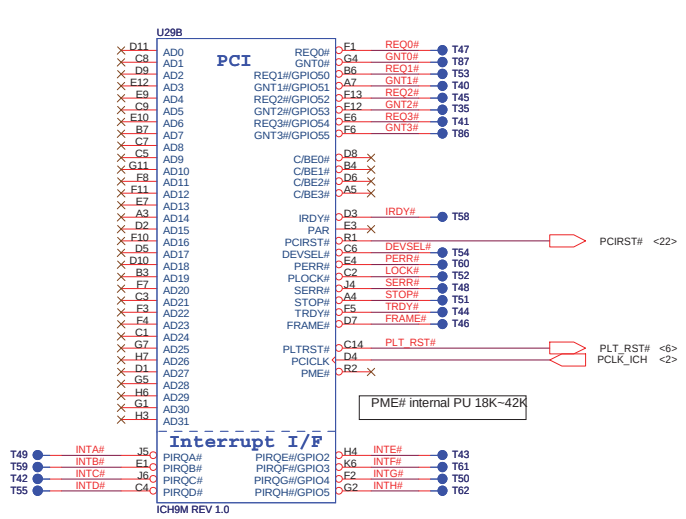
Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	ICH_TP3 / HDA_SDOUT: 0/0 RSVD; 0/1 Enter XOR Chain; 1/0 Normal opration(Default); 1/1 Set PCIE port config bit	<14> ICH_TP3 — ICH_TP3 — R182 *1K_4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		HDA_SDOUT_R — R234 *1K_4 — +3V

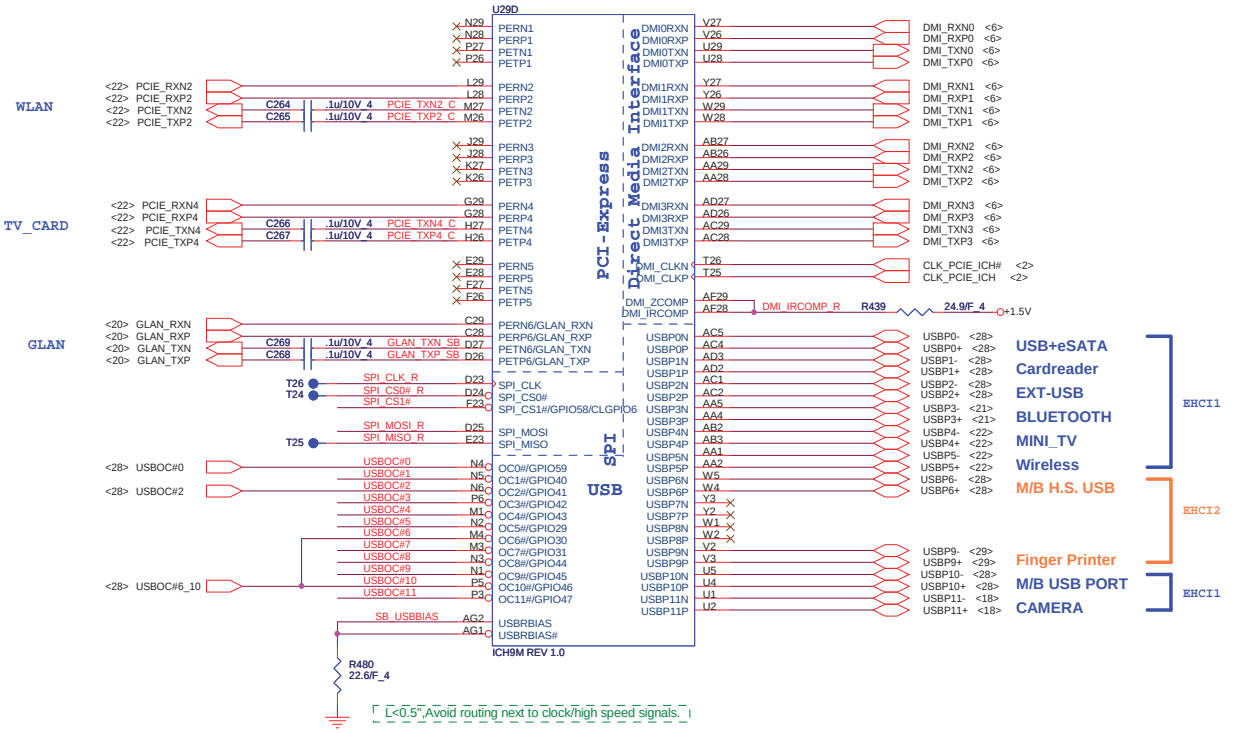
Quanta Computer Inc.

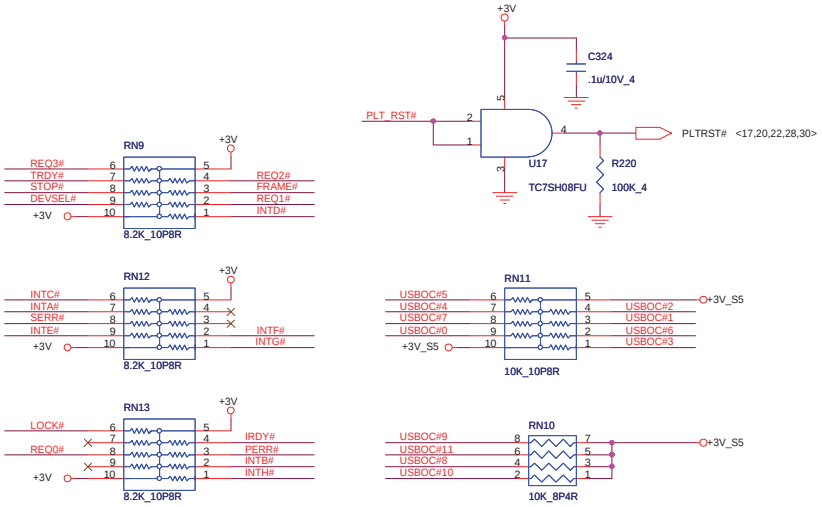
PROJECT : ZK6

Size	Document Number	Rev
	ICH9M HOST	1A
Date: Friday, April 24, 2009	Sheet 12 of 42	

ICH9M



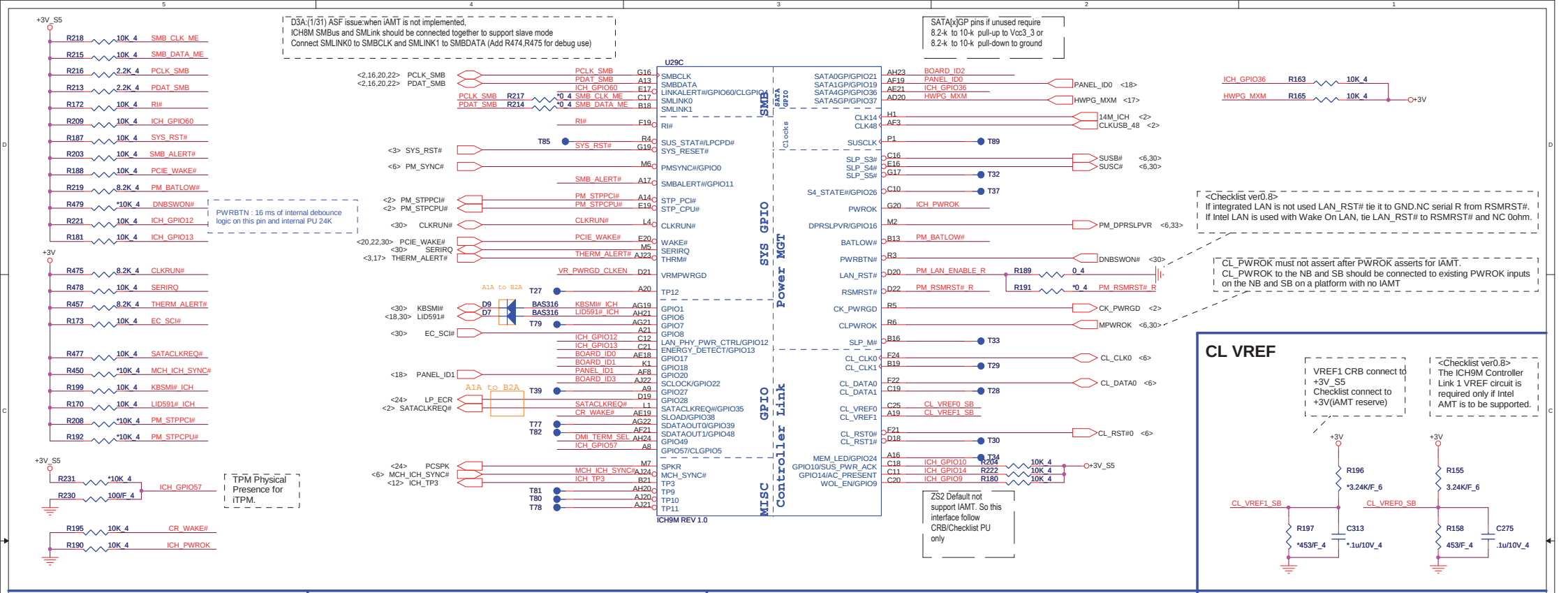




South Bridge Strap Pin (2/3)

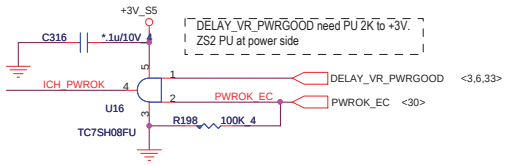
Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R485 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI_R R156 *10K_4 +3V_S5
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI	GNT0# R486 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1 / 0 / PCI 1 / 1 / **LPC(Default)**	SPI_CS1# R177 *1K_4

Quanta Computer Inc.
PROJECT : ZK6
Size | Document Number: ICH9M PCIE / PCI / USB | Rev 1A
Date: Friday, April 24, 2009 | Sheet 13 of 42

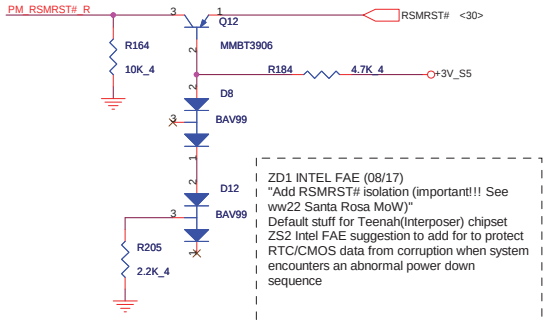


CL VREF

ICH PWROK

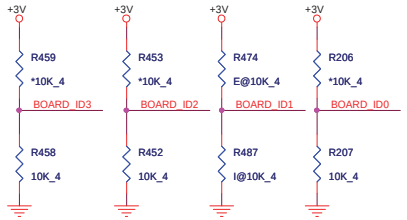


Resume RST



M/B ID

ID0 :: ZK=0 , ZR=1
ID1 :: UMA=0 , MXM=1

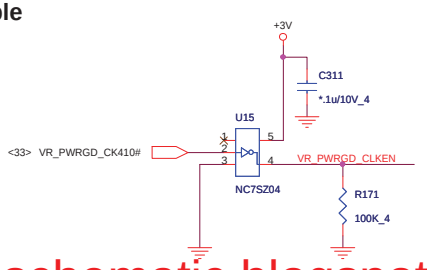


Board ID	ID3	ID2	ID1	ID0
default	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0

South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R229 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R446 *1K_4

CLK Enable



Quanta Computer Inc.
PROJECT : ZK6
Size | Document Number | ICH9M GPIO | Rev 1A
Date: Friday, April 24, 2009 | Sheet 14 of 42

ICH9M

IV@

EV@

Power consumption reference to Intel ICH9 Family EDS Rev 1.6

2~3.456v 3.6uA_G3

PER INTEL SUGGESTION: CHANGE TO 100OHM & 1UF

5V 2mA

5V S0:2mA S3/4/5:1mA

1.5V 646mA

1.5V 47mA

VCC1_5_A 1.5V 1342mA

1.5V 11mA

1.05V , Powered by VCC1_05 in S0

3.3V S0:19mA S3/4/5:78mA

If use SB MAC for LAN function. And support wake up need connect to relation power.

1.5V 23mA

1.5V 80mA

3.3V 1mA

1.05V 1634mA

1.5V 23mA

1.05V 50mA

1.05V 2mA

3.3V 308mA

3.3V S0:212mA S3/4/5:53mA

VCCSUS1_05 power by VCC1_05 in S0 / VCCSUS3_3 in S3/S4/S5

VCCSUS1_5 power by VCC1_5_A in S0 / VCCSUS3_3 in S3/S4/S5

3.3V S0:19mA S3/4/5:73mA

VCCCL1_05 power by VCC1_05_A in S0

VCCCL1_5 power by VCC1_5_A in S0

If use SB MAC for LAN function. And support wake up need connect to relation power.

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

Support INT HDMI HDA interface. These power only support 1.5V.Device must to meet.

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

U29F

ICH9M REV 1.0

U29E

ICH9M REV 1.0

Quanta Computer Inc.

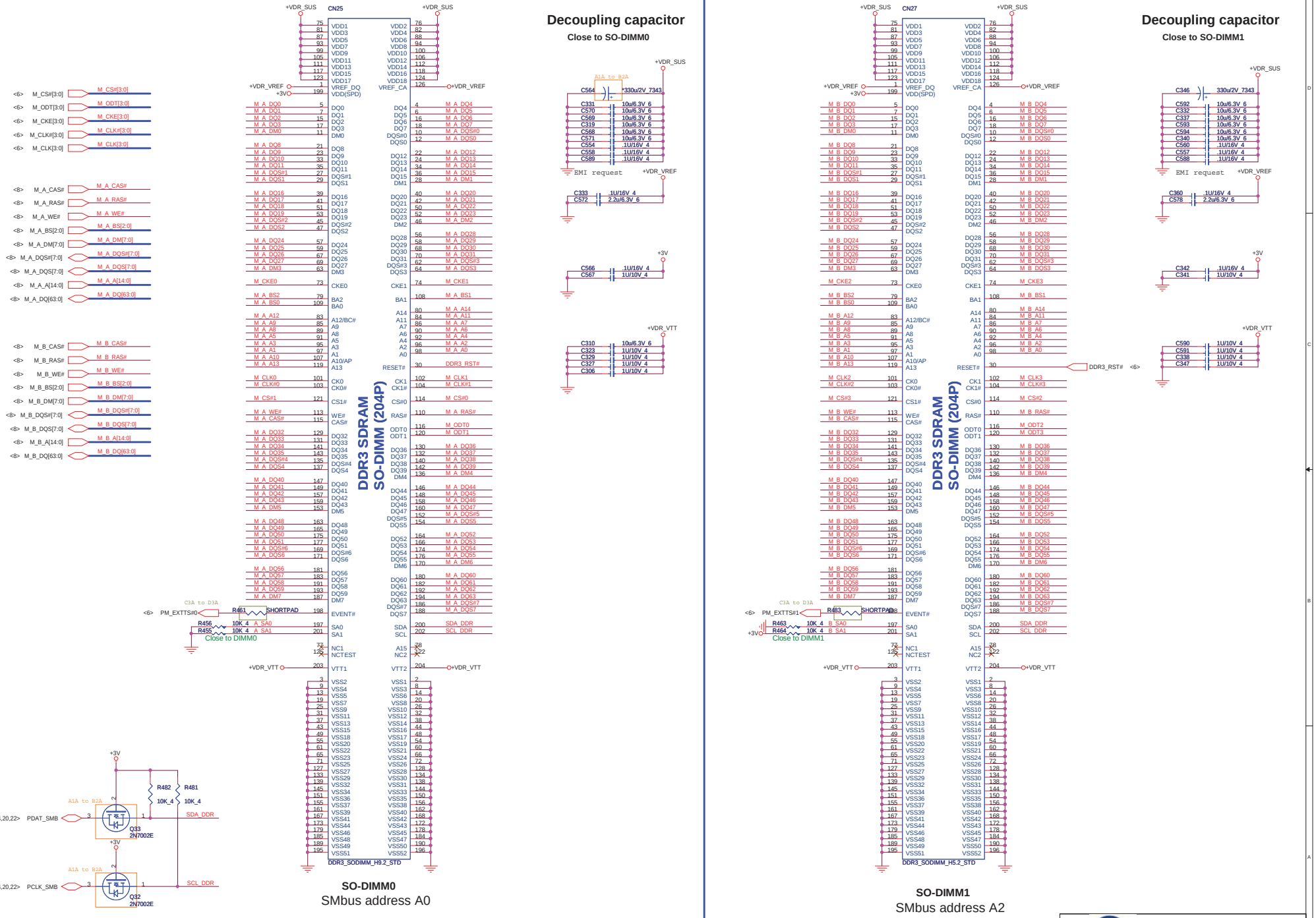
PROJECT : ZK6

Size	Document Number	Rev
	ICH9 POWER	1A

Date: Friday, April 24, 2009 Sheet 15 of 42

H=9.2mm / DGMK4000058

H=5.2mm / DGMK4000059



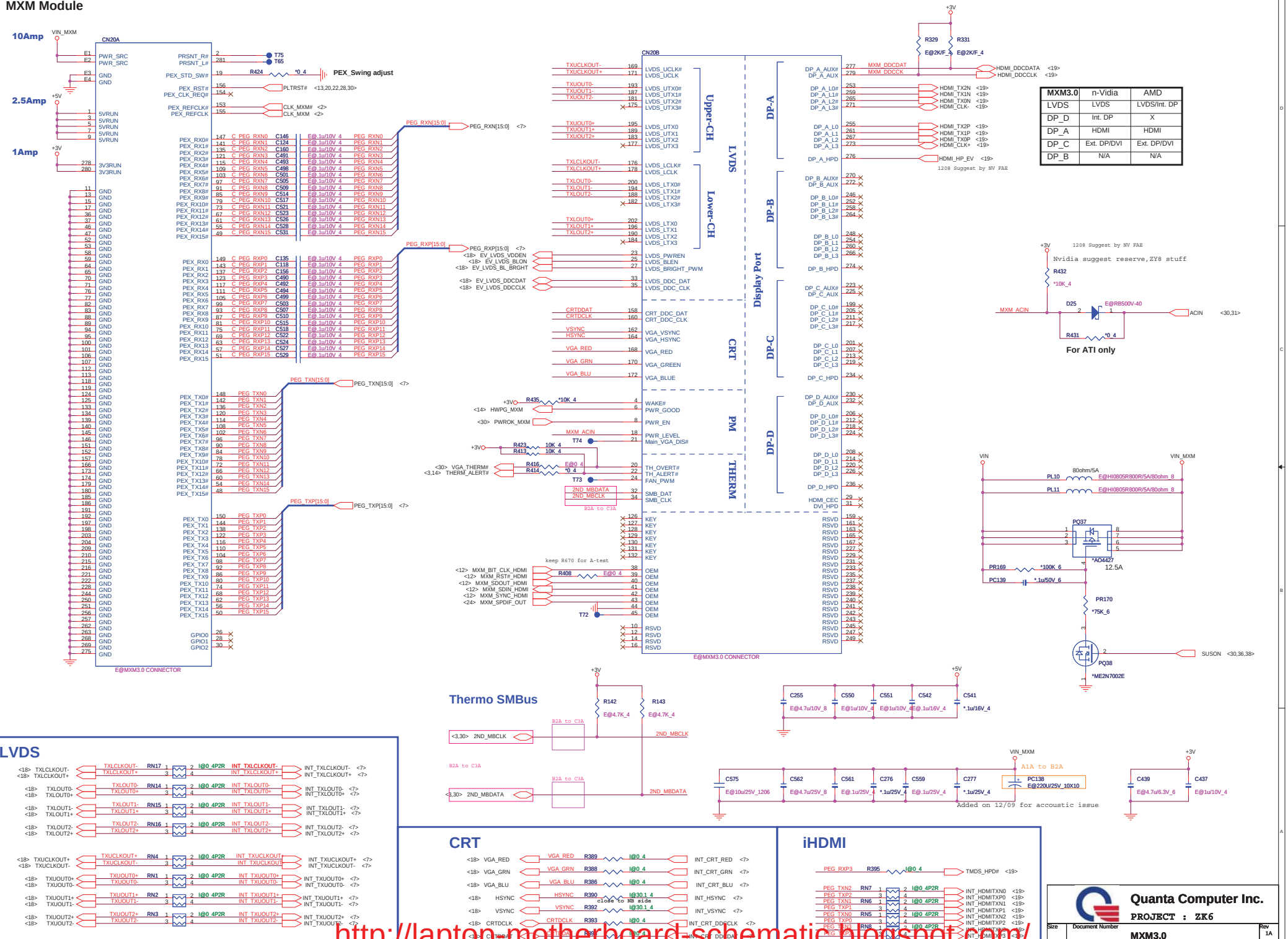
Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	DDRIII SO-DIMM	1A

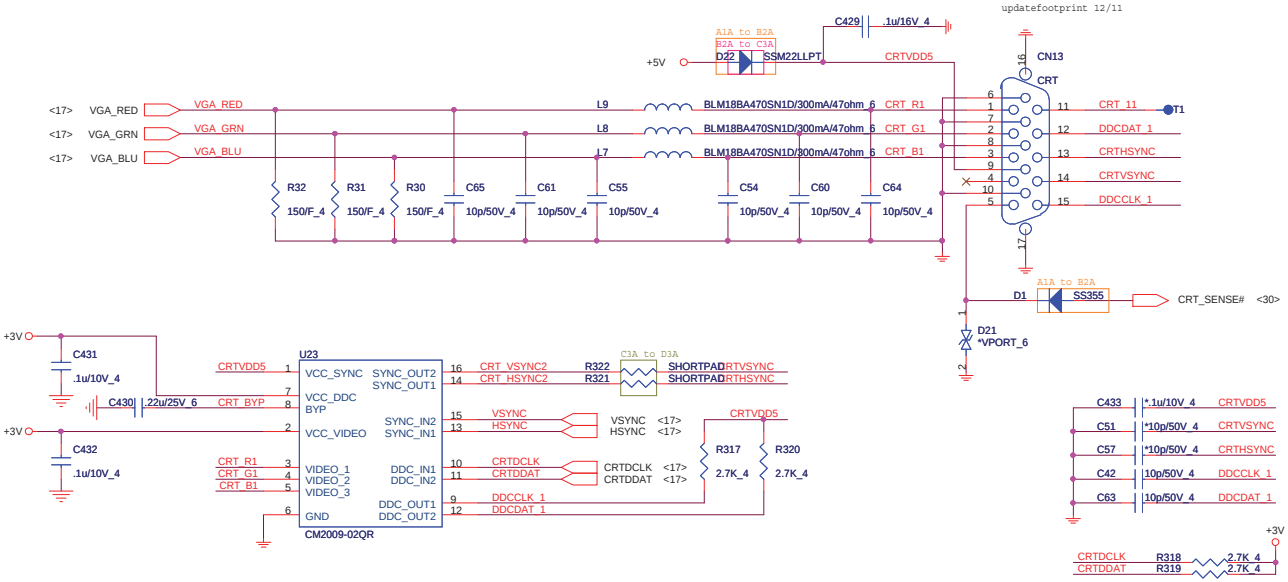
Date: Friday, April 24, 2009 Sheet 16 of 42

MXM Module



CRT

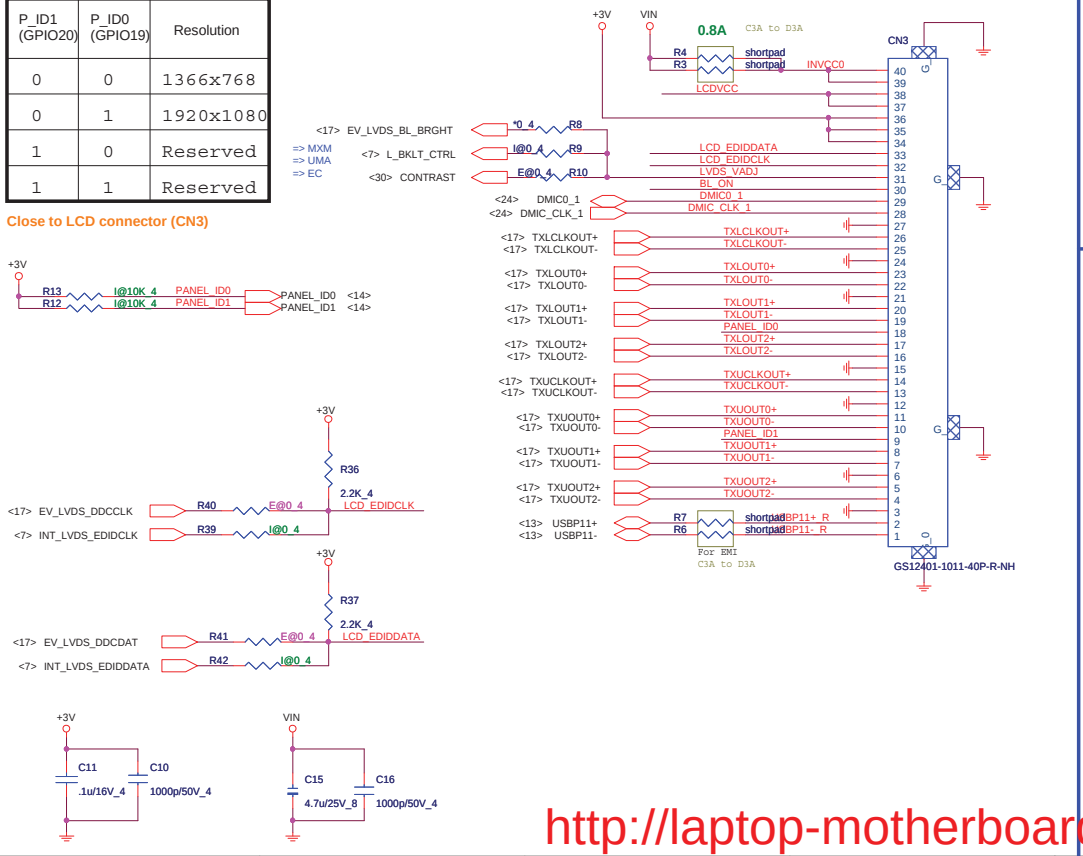
IV@
EV@



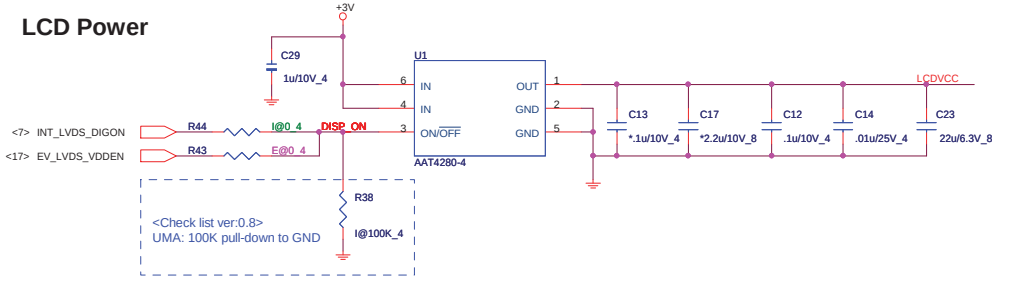
LVDS Panel ID (UMA only)

P_ID1 (GPIO20)	P_ID0 (GPIO19)	Resolution
0	0	1366x768
0	1	1920x1080
1	0	Reserved
1	1	Reserved

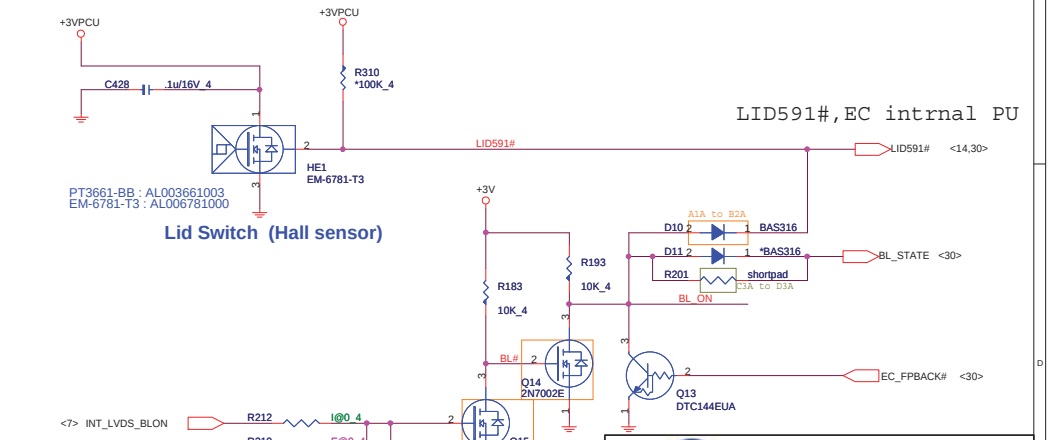
Close to LCD connector (CN3)



LCD Power



Backlight Control & LID



Quanta Computer Inc.
PROJECT : ZK6
Size | Document Number | CRT/LVDS/CAMERA/LID | Rev 1A
Date: Friday, April 24, 2009 | Sheet 18 of 42

I@ HDMI LEVEL SHIFTER

CH7318C :: AL007318002
PS8101T :: AL008101001

IV@
EV@
SP@

From GMCH

I@HDMI-detect

To GMCH

Voltage level 0.9V

Control by pin4 HPDEN_R

To GMCH

OE# control for power saving

Equalization Control		
PC1 PIN4	PC0 PIN3	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB

E@HDMI-detect

To MXM

Switch I2C E@ or I@

NV suggestion near HDMI connector

To MXM

To MXM

Switch E@ or I@

To MXM

ESD Protect

EMI

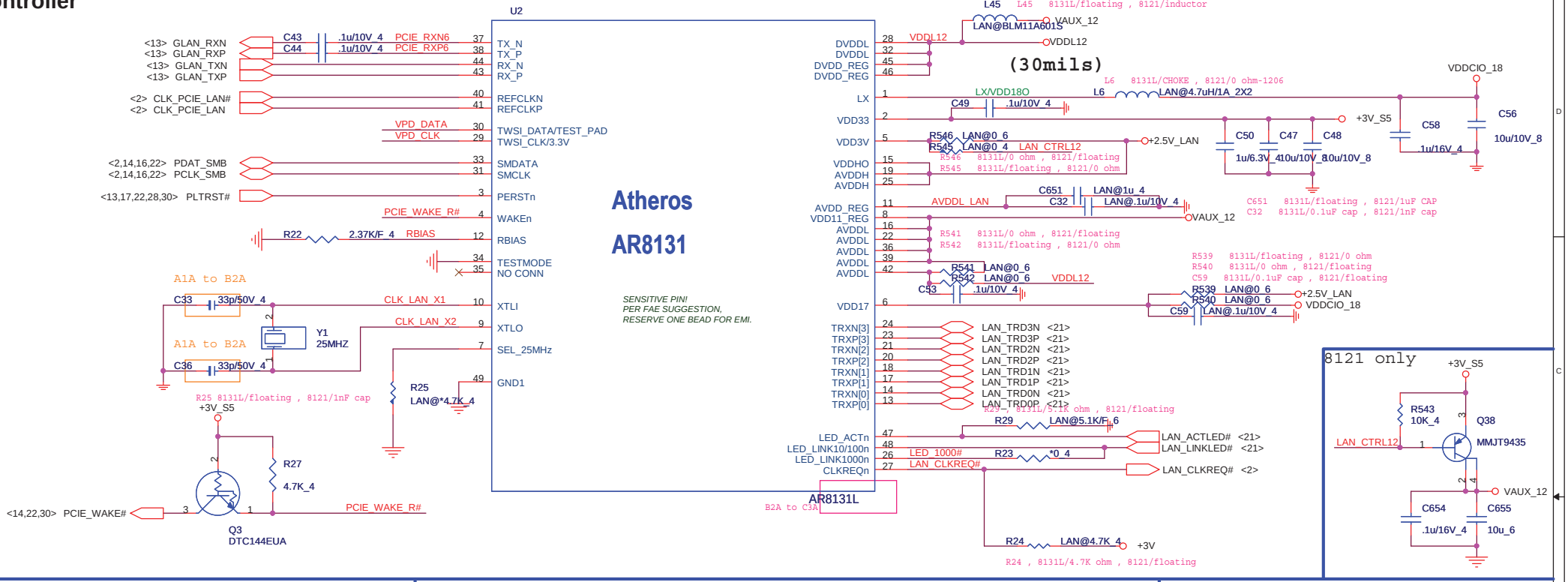
HDMI connector

Quanta Computer Inc.
PROJECT : ZK6

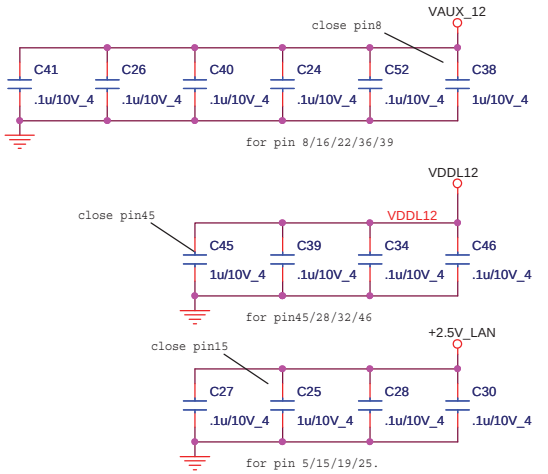
Size	Document Number	Rev
	HDMI (CH7318C)	1A

Date: Friday, April 24, 2009 Sheet 19 of 42

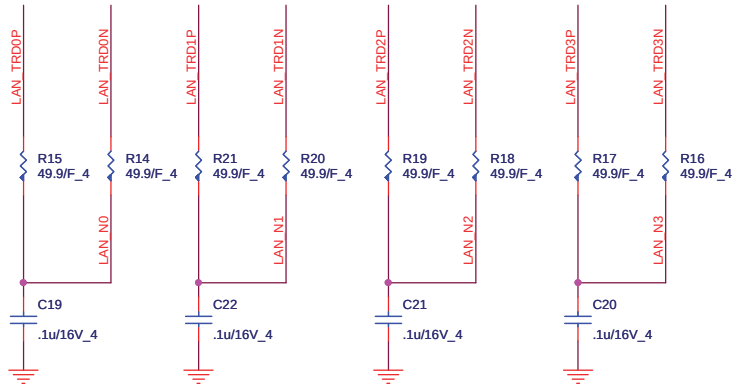
LAN Controller



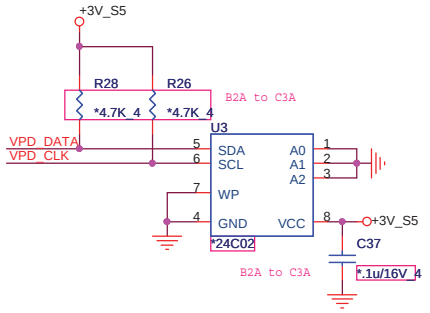
Decoupling CAP



PLACE NEAR IC SIDE



EEPROM

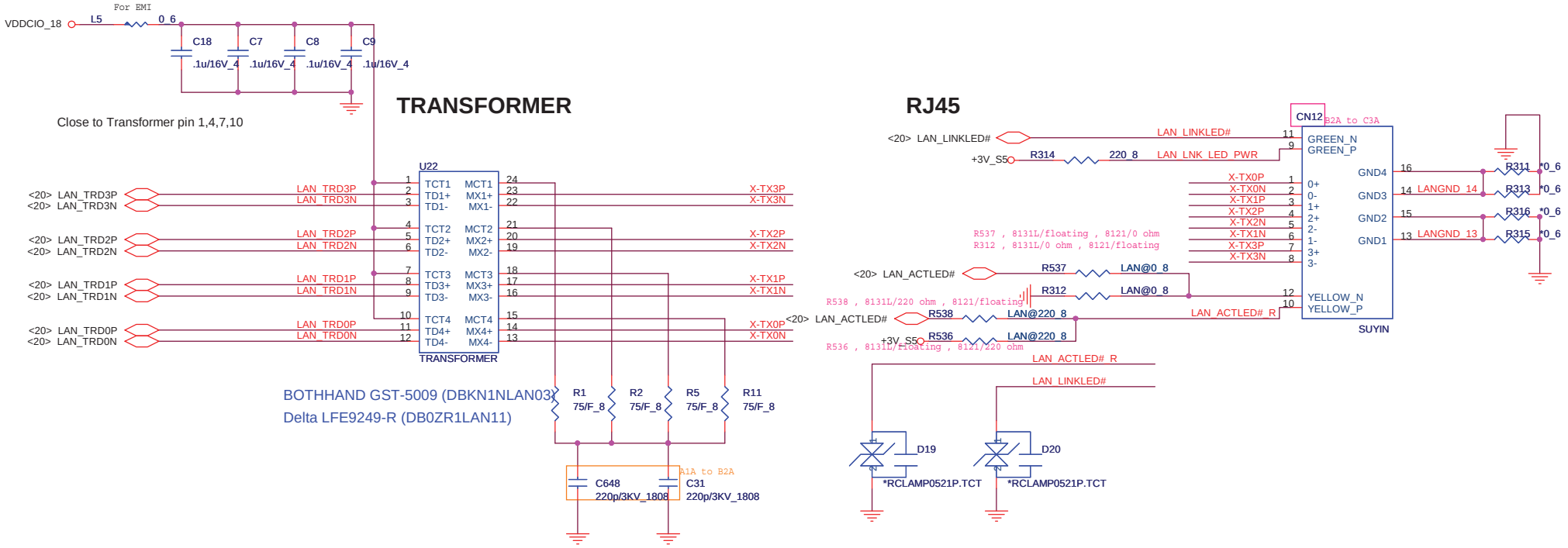


Quanta Computer Inc.

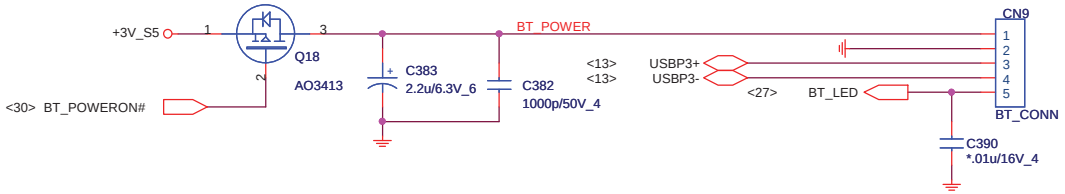
PROJECT : ZK6

Size	Document Number	Rev
	AR8131 GLAN	1A

Date: Friday, April 24, 2009 Sheet 20 of 42



BLUETOOTH CONNECTOR

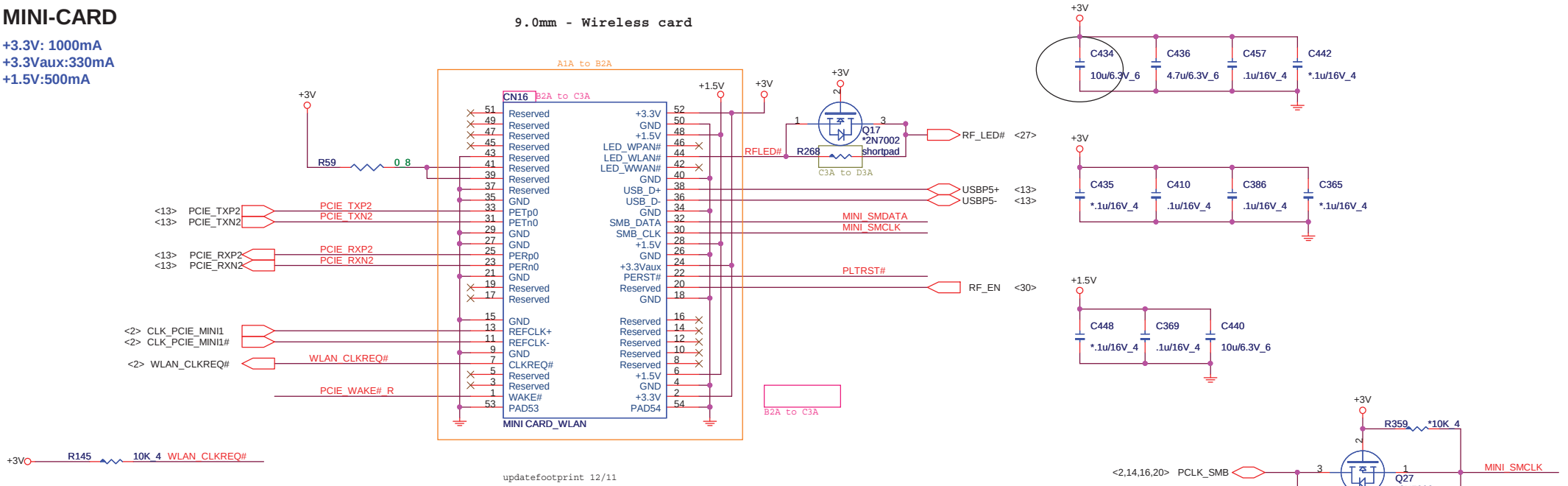


Quanta Computer Inc.		
PROJECT : ZK6		
Size	Document Number: LAN Transformer and RJ45/BT	Rev 1A
Date: Friday, April 24, 2009	Sheet 21 of 42	

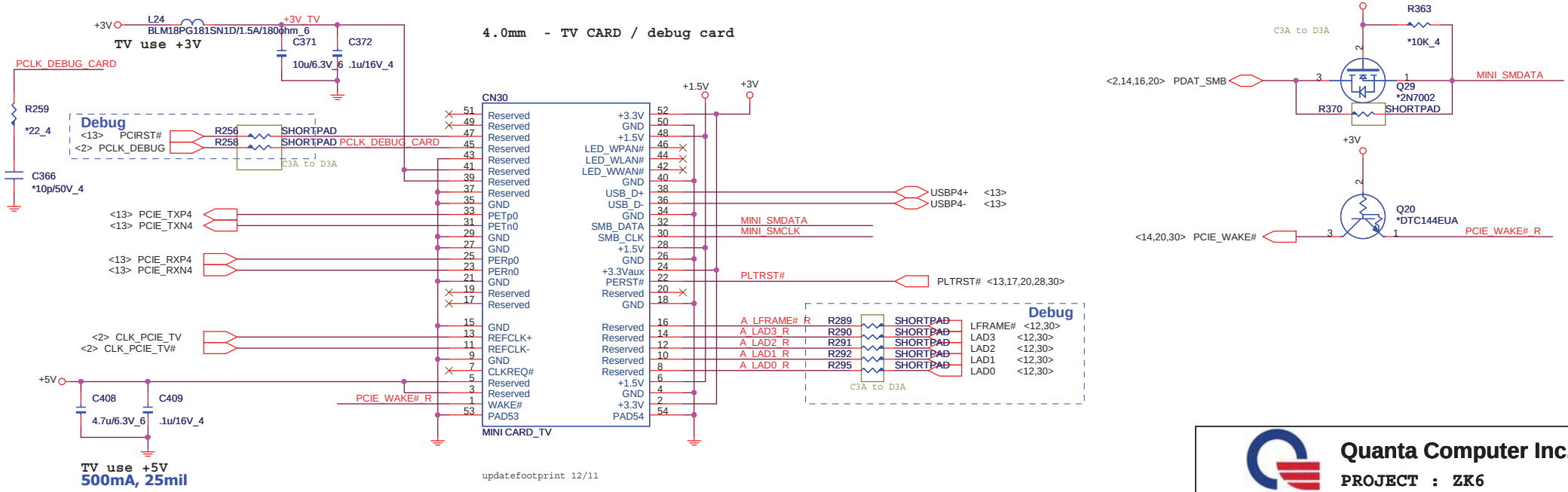
MINI-CARD

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

9.0mm - Wireless card

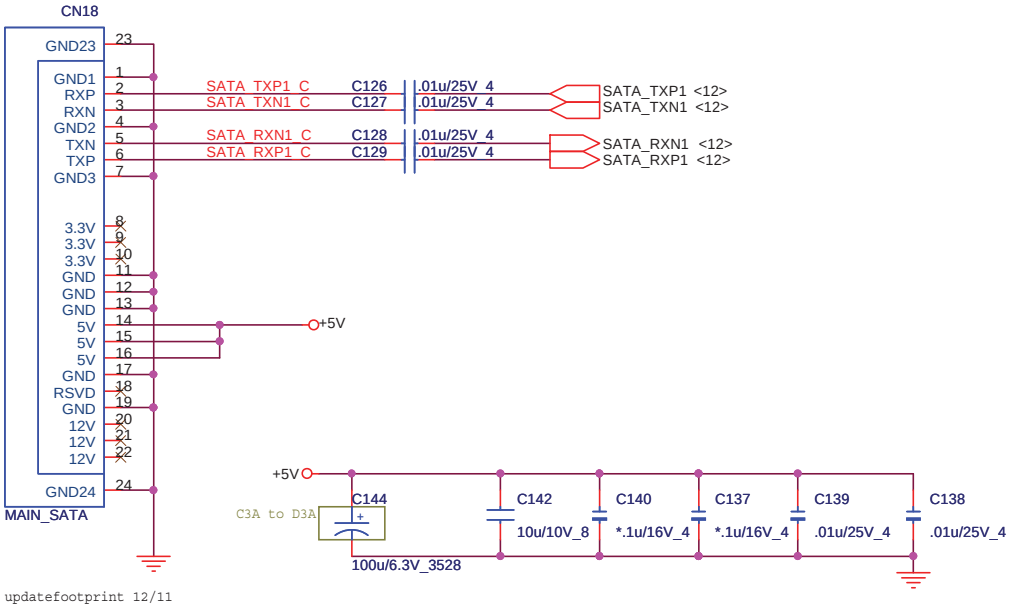


4.0mm - TV CARD / debug card



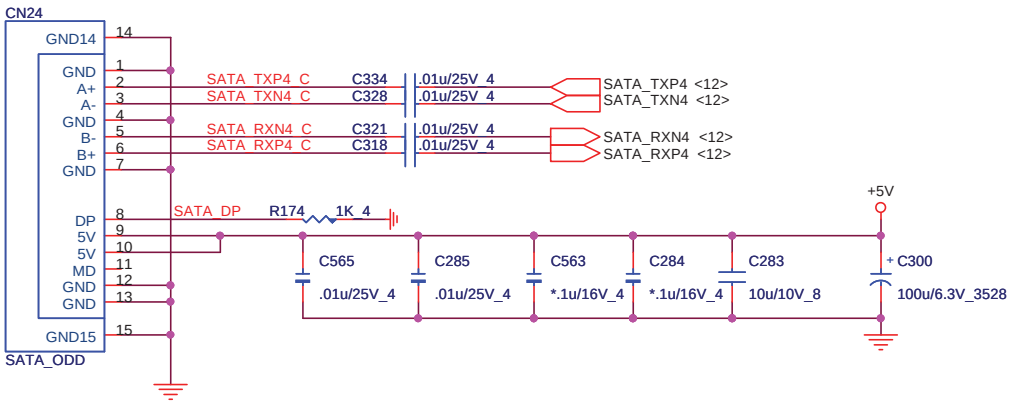
Quanta Computer Inc.		
PROJECT : ZK6		
Size	Document Number	Rev
	MINI PCI-E card/TV	1A
Date: Friday, April 24, 2009	Sheet 22 of 42	

MAIN SATA HDD



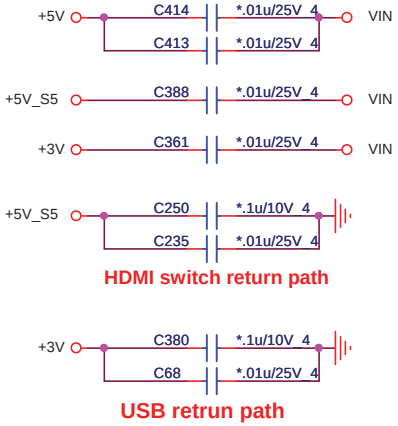
updatefootprint 12/11

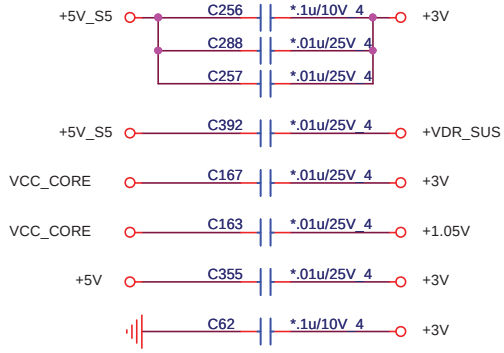
ODD (SATA)

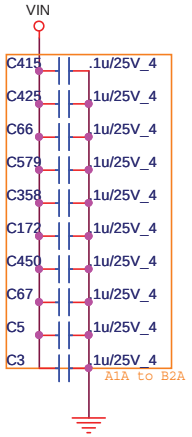


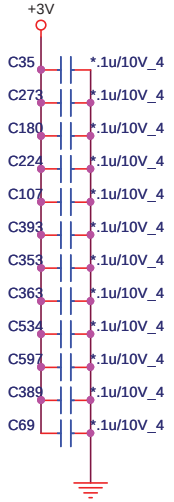
updatefootprint 12/11

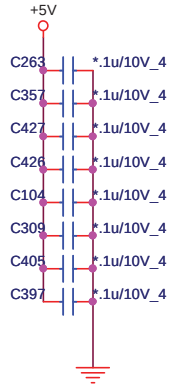
EE RETURN-PATH CAPACITORS









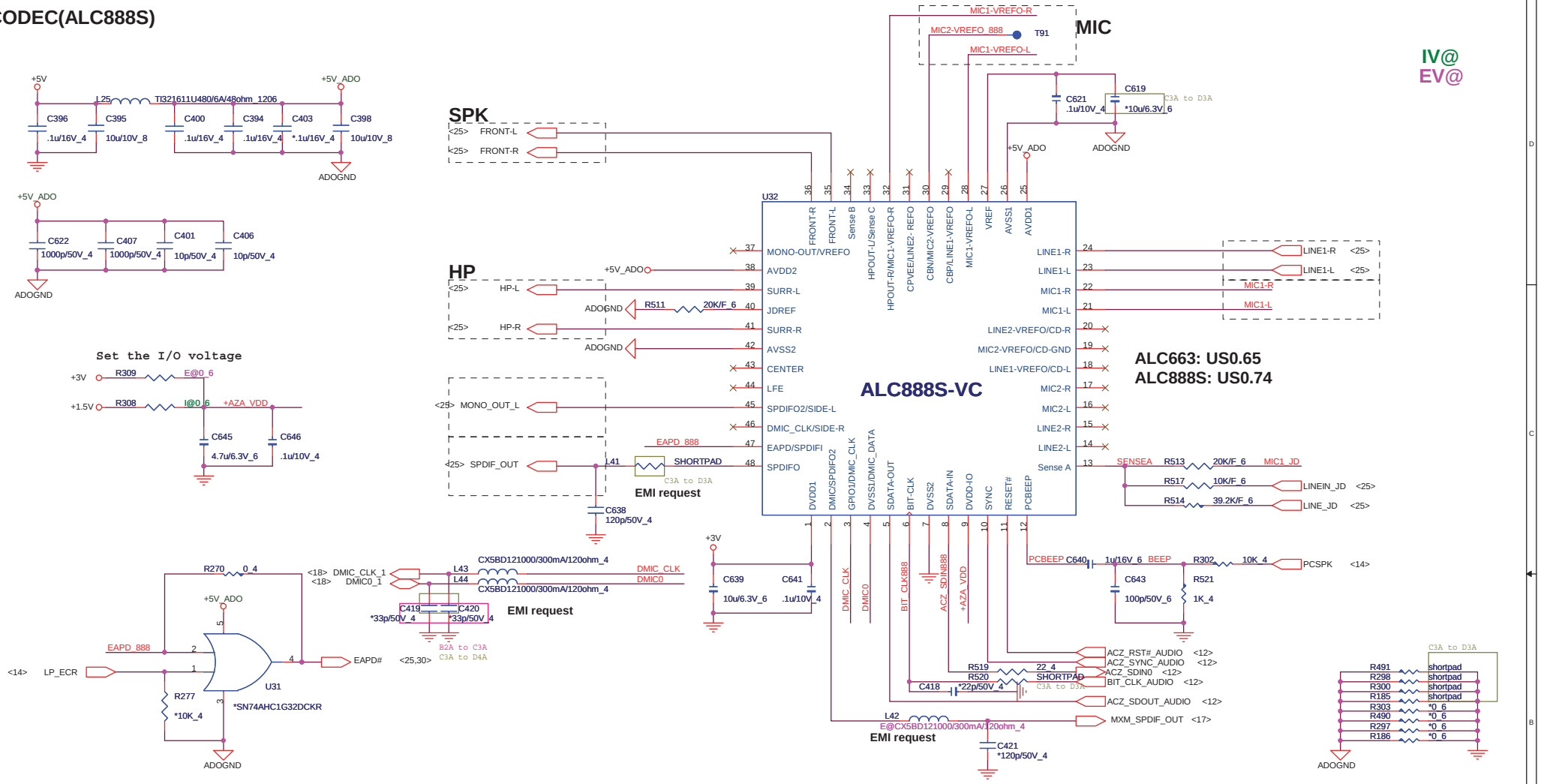


Quanta Computer Inc.

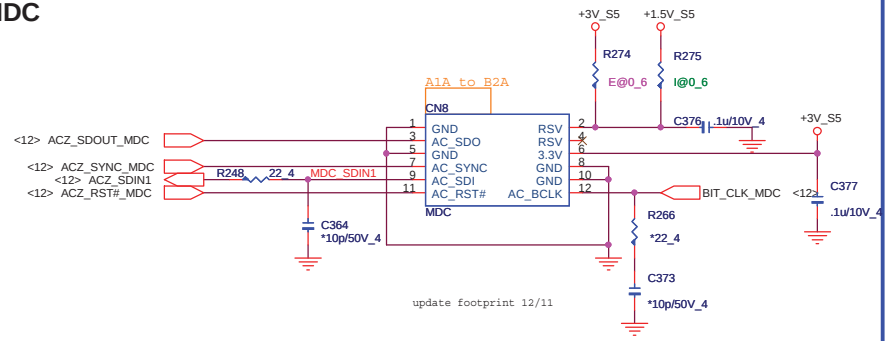
PROJECT : ZK6

Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	1A
Date: Friday, April 24, 2009	Sheet 23 of 42	

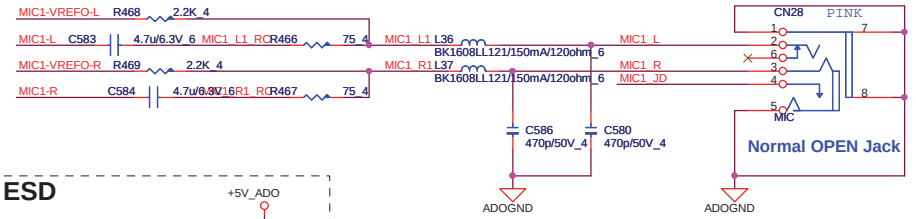
CODEC(ALC888S)



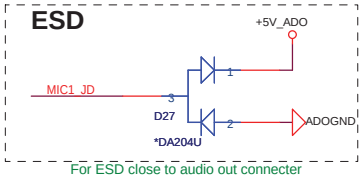
MDC



MIC



ESD

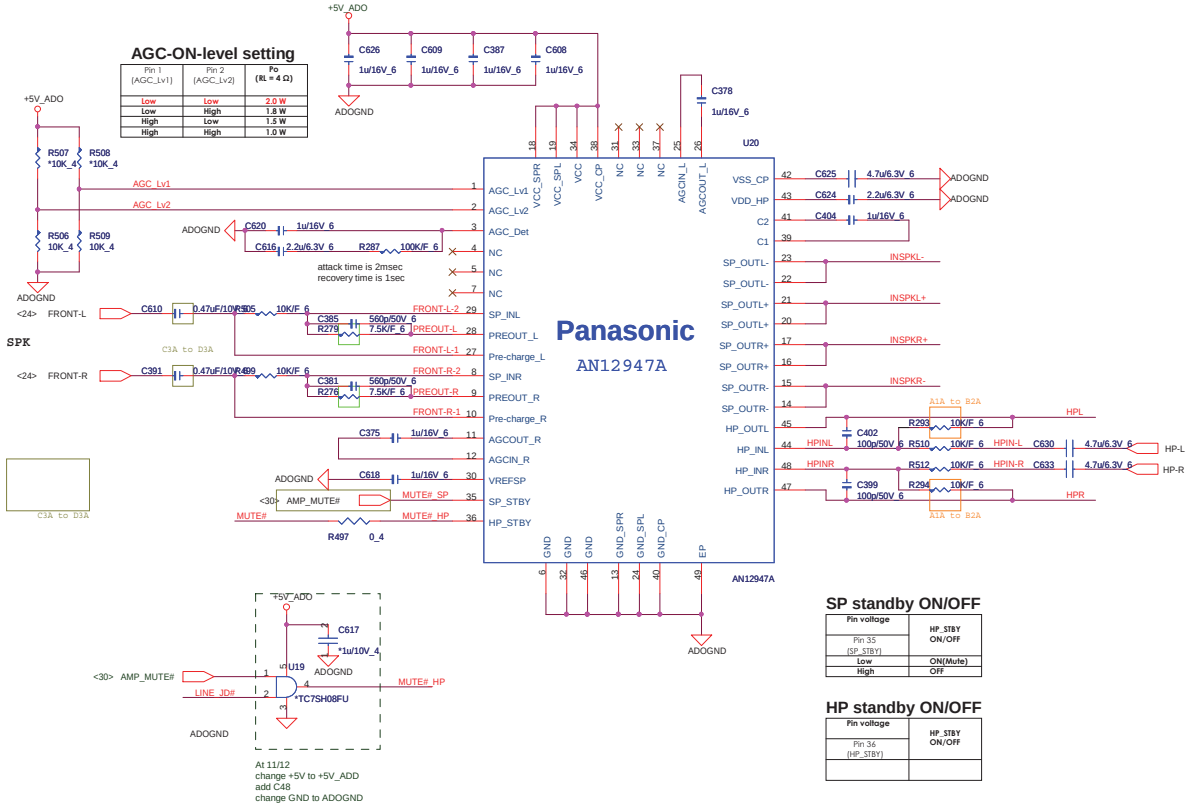


For ESD close to audio out connecter

CODEC & MDC

Quanta Computer Inc.		
PROJECT : ZK6		
Size	Document Number: REALTEK ALC663&888/MDC	Rev: 1A
Date: Friday, April 24, 2009	Sheet 24 of 42	

SPEAKER/HP AMP.



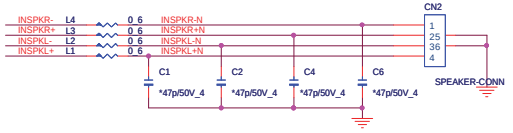
SP standby ON/OFF

Pin voltage	HP_STBY ON/OFF
Pin 35 (SP_STBY)	
Low	ON(Mute)
High	OFF

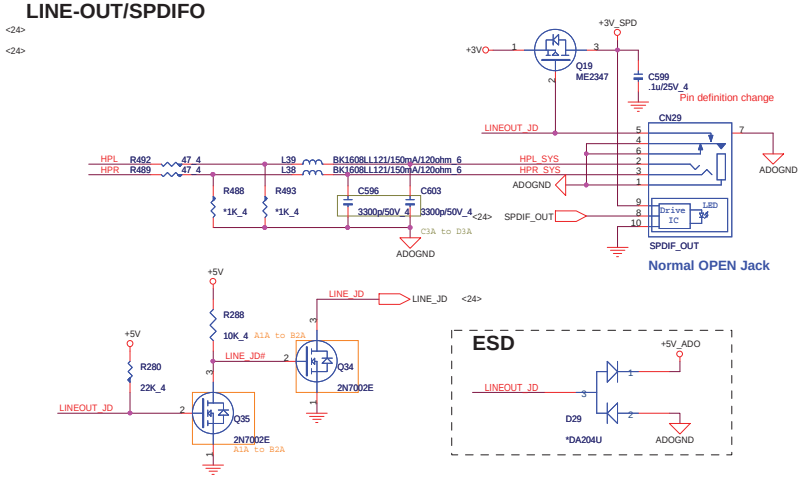
HP standby ON/OFF

Pin voltage	HP_STBY ON/OFF
Pin 36 (HP_STBY)	

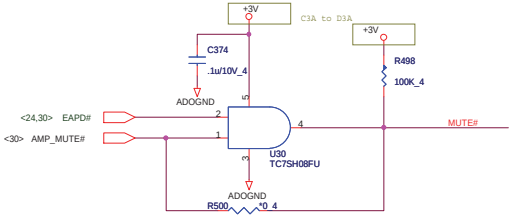
SPEAKER



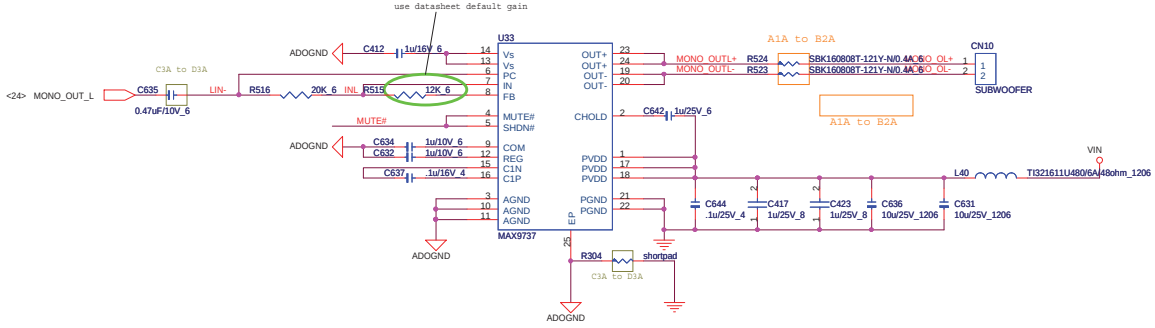
LINE-OUT/SPDIFO



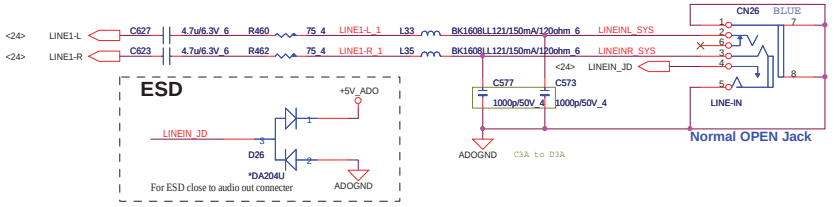
MUTE



SUBWOOFER



LINE IN



AMP& PHONE JACK & SUBWOOFER

Quanta Computer Inc.
PROJECT : ZK6
Size | Document Number | AMP /AUDIO JACK CONN | Rev 1A
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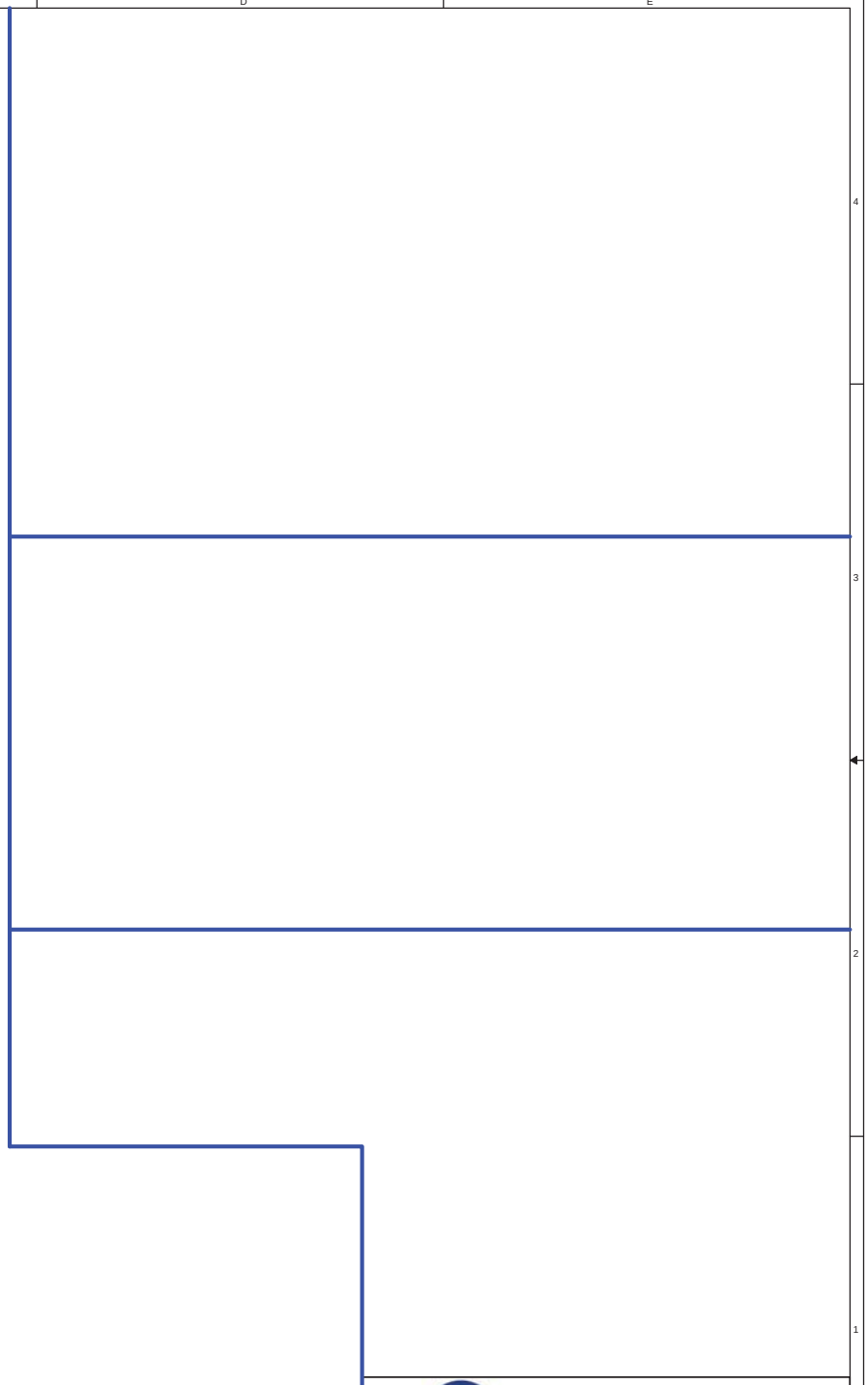

Quanta Computer Inc.

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Size	Document Number	Rev
	CARD READER RTS5159	1A

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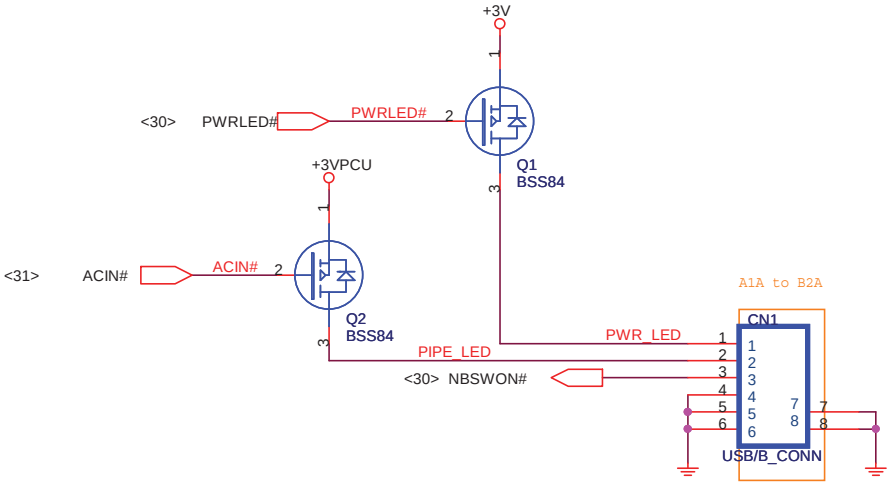
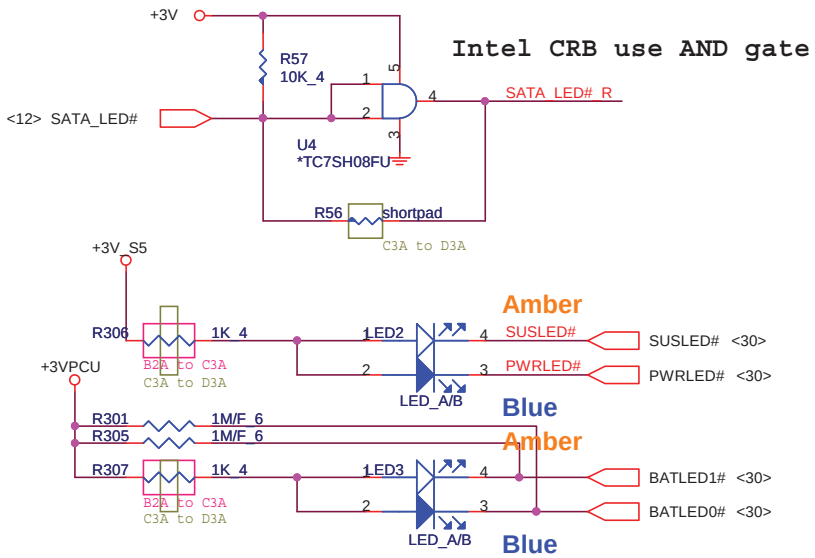
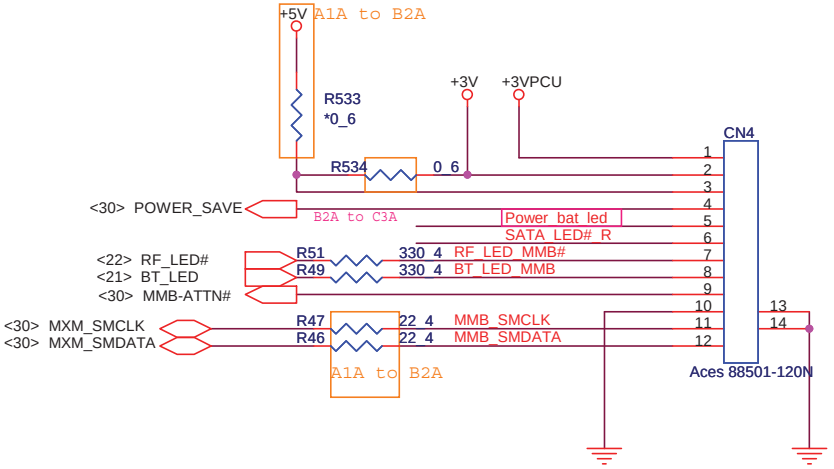
POWER BOARD

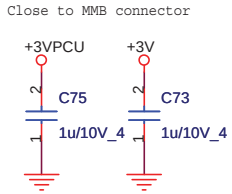


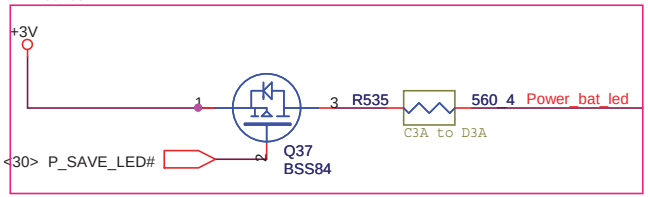
LED



MMB







Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	POWER/MMB/LAUNCH/LED	1A
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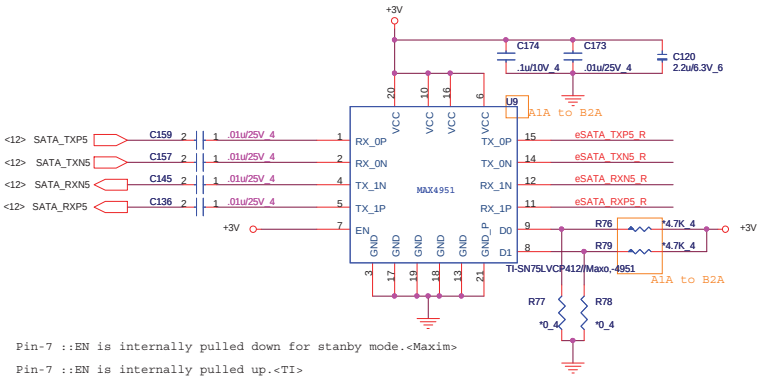
ESATA



Pin-7 ::EN is internally pulled down for stanby mode.<Maxim>

Pin-7 ::EN is internally pulled up.<TI>

Pin-8 ::BB is internally pulled down.<TI/MAXIM>

Pin-9 ::BA is internally pulled down.<TI/MAXIM>

EN	BA/D0	BB/D1	CH-0/A	CH-1/B
0	X	X	Standby	Standby
1	0	0	0dB	0dB
1	1	0	Pre-emphasis (5dB)	0dB
1	0	1	0dB	Pre-emphasis (5dB)
1	1	1	Pre-emphasis (5dB)	Pre-emphasis (5dB)

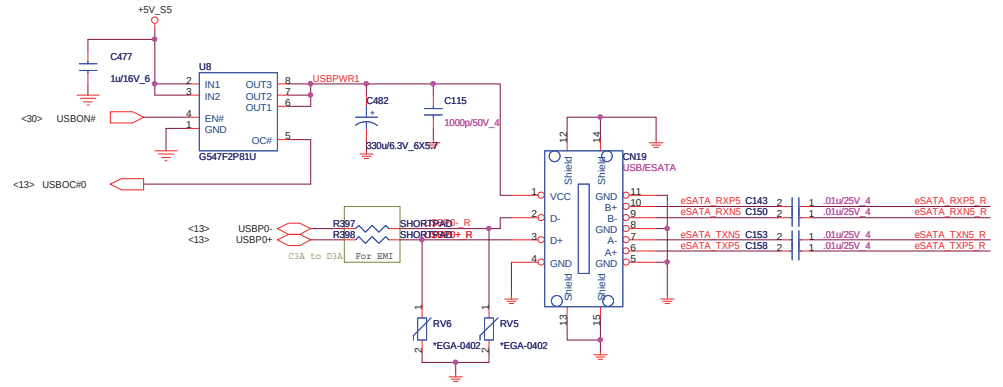
X=don't care

DG2.1 4.2.4 Terminating Unused SATA Interface

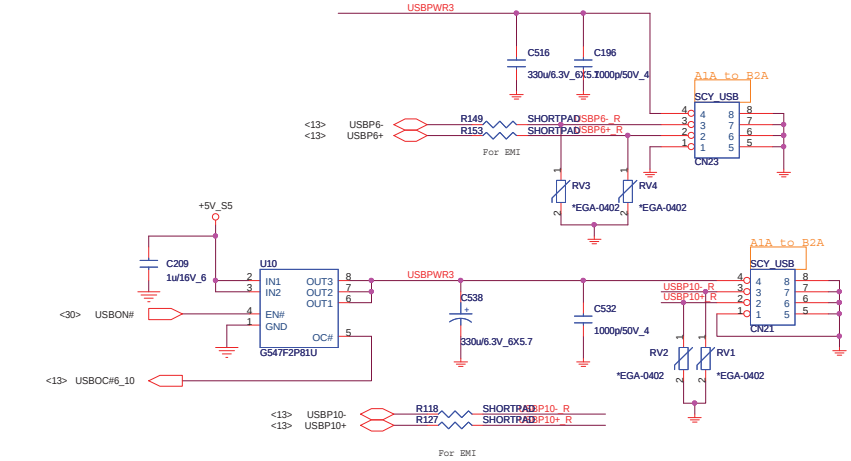
SATA[1:0]RXp/n, SATA[5:4]RXp/n connect to GND while SATA not be implemented

SATA_RXP5 R81 *8.2K_4

SATA_RXN5 R90 *8.2K_4



USB PORT



HOLES

H-C276D118P2-8 -- 1 pcs

HOLE12 *H-C276D118P2-8

H-C315D118P2-8-- 12 pcs

HOLE3 HOLE8 HOLE5 HOLE7 HOLE30 HOLE24 HOLE1 HOLE21 *H-C315D118P2-8

HOLE27 HOLE29 HOLE28 HOLE23 *H-C315D118P2-8

ADOGND

HOLE2 HOLE9 HOLE19 HOLE14 *H-C236D146P2-8

H-C236D146P2-8 -- 8 pcs

HOLE15 HOLE20 HOLE22 HOLE13 *H-C236D146P2-8

HOLE25 *H-TC236BC197D146P2

HOLE26 *H-TC236BC197D146P2

C3A to D3A

B2A to C3A

H-TC236BC197D146P2 -- 2 pcs

A1A to B2A

HOLE10 *h-c197d55pb

HOLE11 *h-c197d55pb

H-C197D55PB --2 pcs

HOLE16 *H-C197D55P2-8

HOLE17 *H-C197D55P2-8

H-C197D55P2-8 --2 pcs

HOLE31 *H-C354D295P2-8

H-C354D295P2-8 -- 1 pcs

HOLE18 *H-TC236BC276D118P2-8

H-TC236BC276D118P2-8 -- 1 pcs

PAD4 PAD7 PAD3 PAD1 PAD8 PAD10 *PAD-C157

PAD9 PAD13 PAD12 PAD5 PAD6 PAD2 PAD11 *PAD-C157

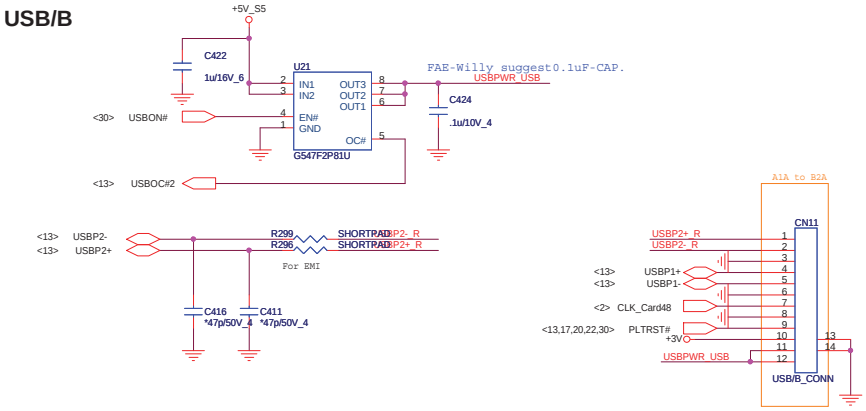
NONGND

HOLE6 *h-c98d98n

NONGND-Fan hole

HOLE4 O-ZK6-1

USB/B



Quanta Computer Inc.			
PROJECT : ZK6			
Size: D	Document Number: USB		Rev: 1A
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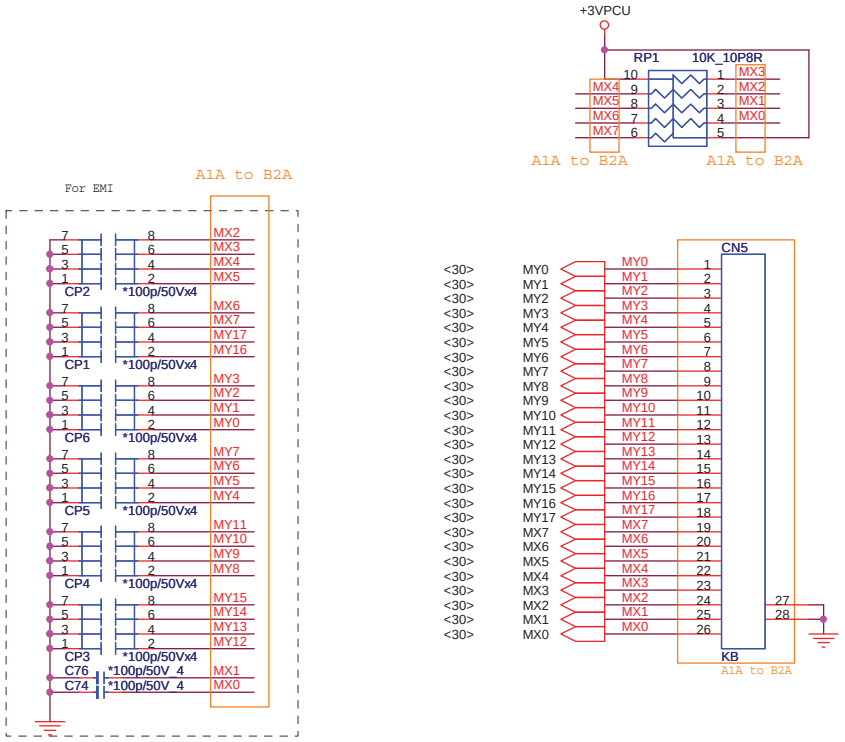
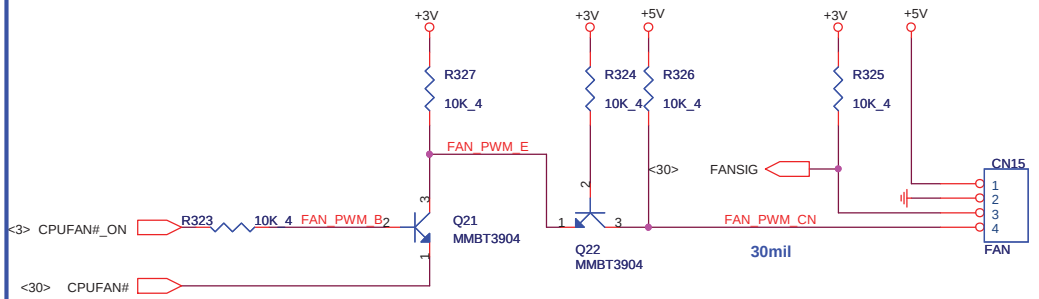
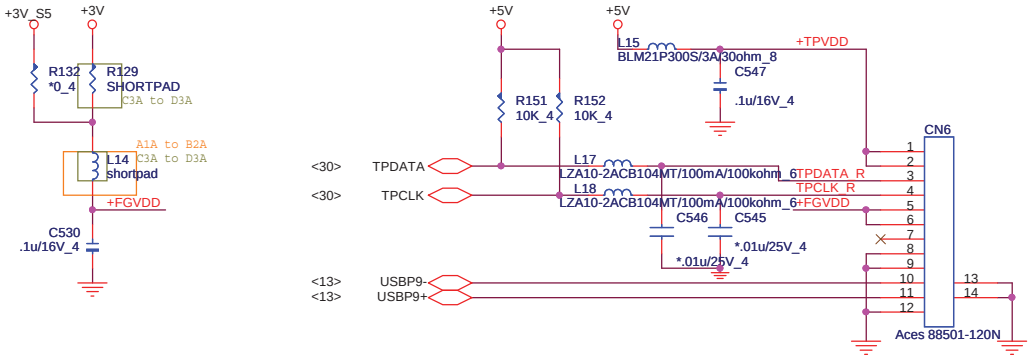
K/B



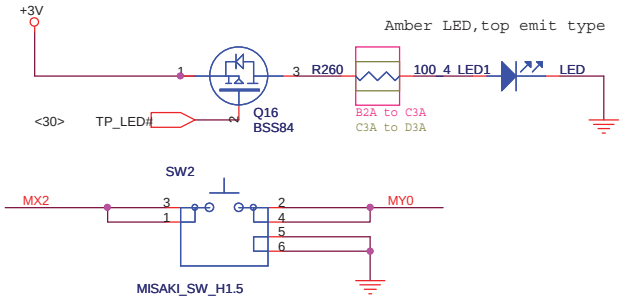
CPU FAN



TOUCHPAD & Finger-Printer CONN.



TP LOCK Button



Quanta Computer Inc.		
PROJECT : ZK6		
Size	Document Number	Rev
	KB/FAN/TP+FP	1A
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EC

I/O ADDRESS SETTING

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

BADDR0 — BADDR0_EC_R — R179 — 10K_4
BADDR1 — BADDR1_EC_R — R178 — *10K_4
SHBM — SHBM_R — R440 — 10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU

2ND_MBCLK — R419 — 10K_4 — +3V
2ND_MBDATA — R429 — 10K_4 — +3V
MBCLK — R434 — 10K_4 — +3VPCU
MBDATA — R433 — 10K_4 — +3VPCU
MXM_SMCLK — R168 — 10K_4 — +3V
MXM_SMDATA — R169 — 10K_4 — +3V
CRT_SENSE# — R441 — 4.7K_4 — +3V

ACER ID

U11 (24C02): SCL, SDA, WP, A0, A1, A2, VCC, GND
MXM_SMCLK — MXM_SMDATA
R134 — R133 — shorpad — *0_4 — C241 — *1u/16V_4
C3A to D3A / A2A to C3A

SPI FLASH

U14 (W25X16AVSSIG): SO, SI, SCK, CE, VDD, HOLD, WP, VSS
SPI_SDI_uR — R447 — 22_4 — SPI_SDI_uR_R
SPI_SDO_uR
SPI_SCK_uR
SPI_CS0#_uR — R448 — 10K_4 — +3VPCU
C292 — .1u/16V_4

1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

HWPG

<38> HWPG_1.8V — D14 — BAS316
<34> HWPG_1.05V — D15 — BAS316
<6,36> HWPG_VDR — D17 — BAS316
<32> SYS_HWPG — D13 — BAS316
<35> HWPG_GFX — D16 — BAS316
R194 — 10K_4 — +3V
HWPG — R202 — shorpad — MPWROK <6,14>

INTERNAL KEYBOARD STRIP SET

MY0 — R138 — 10K_4 — +3VPCU

CIR

Q36 *RHU002N06
R518 — *10K_4 — +3V_S5
R522 — *10K_4 — +3V_S5
R525 — 47_6 — C647 — 4.7u/10V_8
R526 — *47_6 — CIR_LED_PWR
U34 (IRM-V538-TR1): VCC, OUT, GND, GND
CIRR_X2 — CIRRX2
R527 — shortpad
D30 *VPORT

Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	WPCE775C_0DG & FLASH	1A

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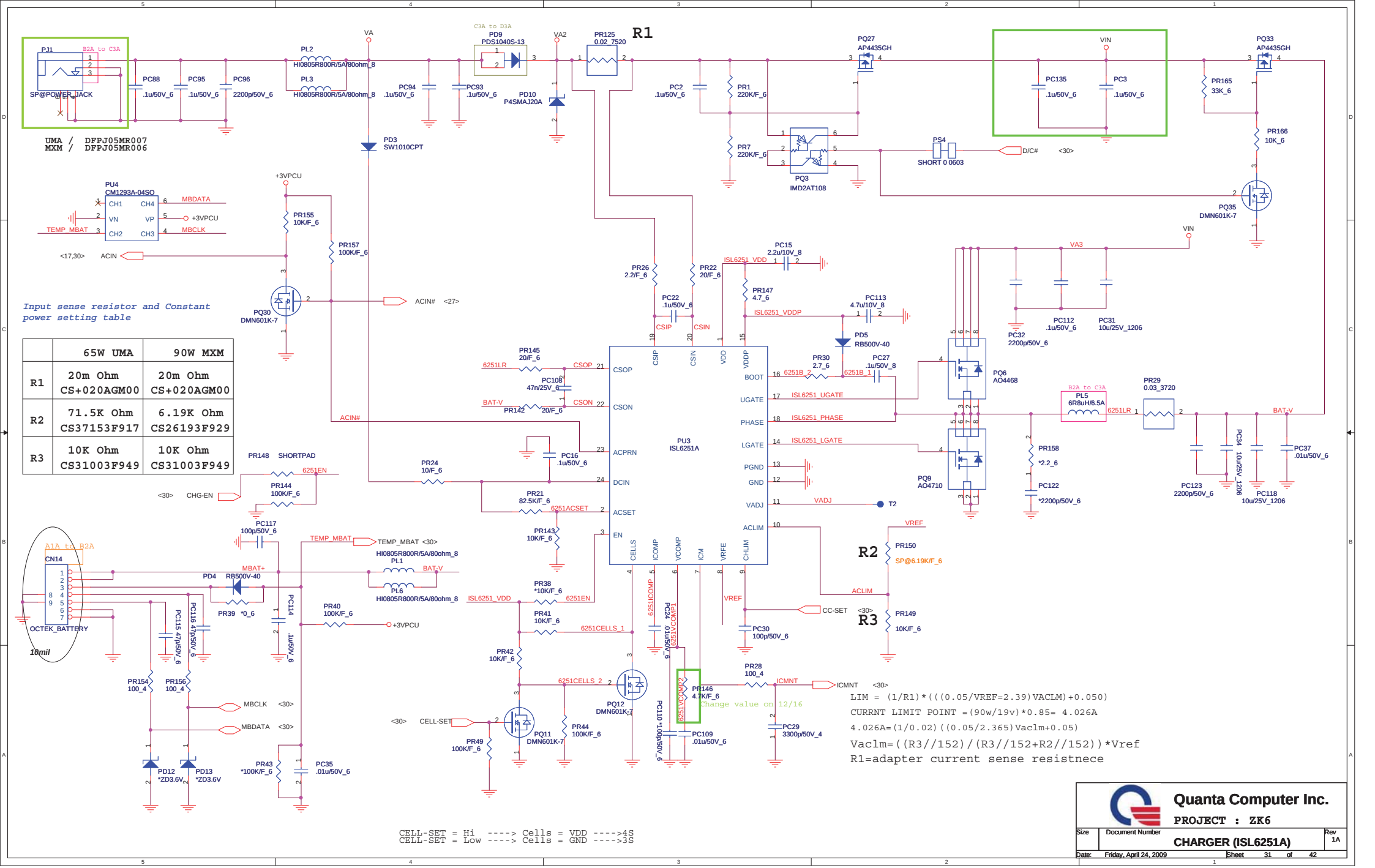
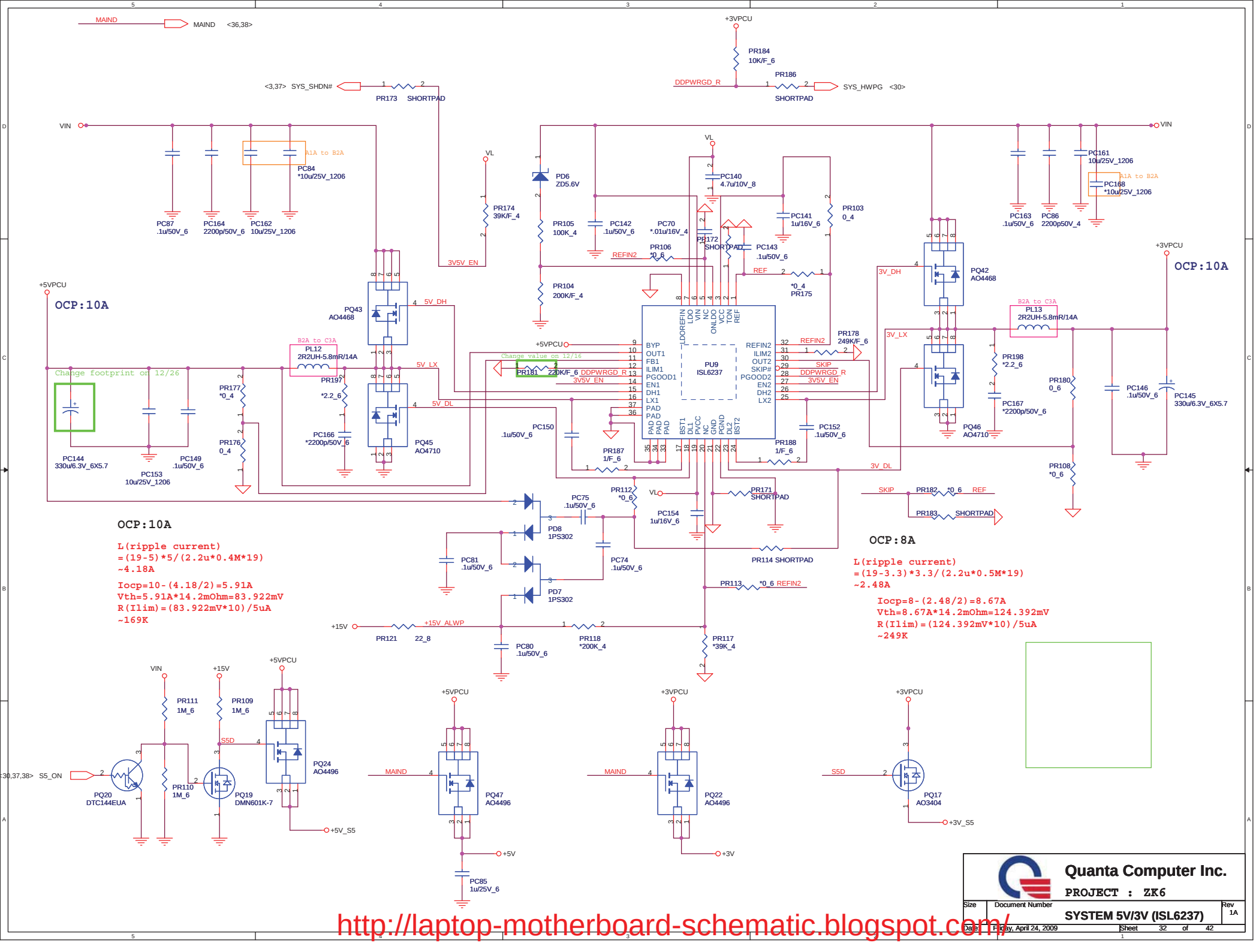
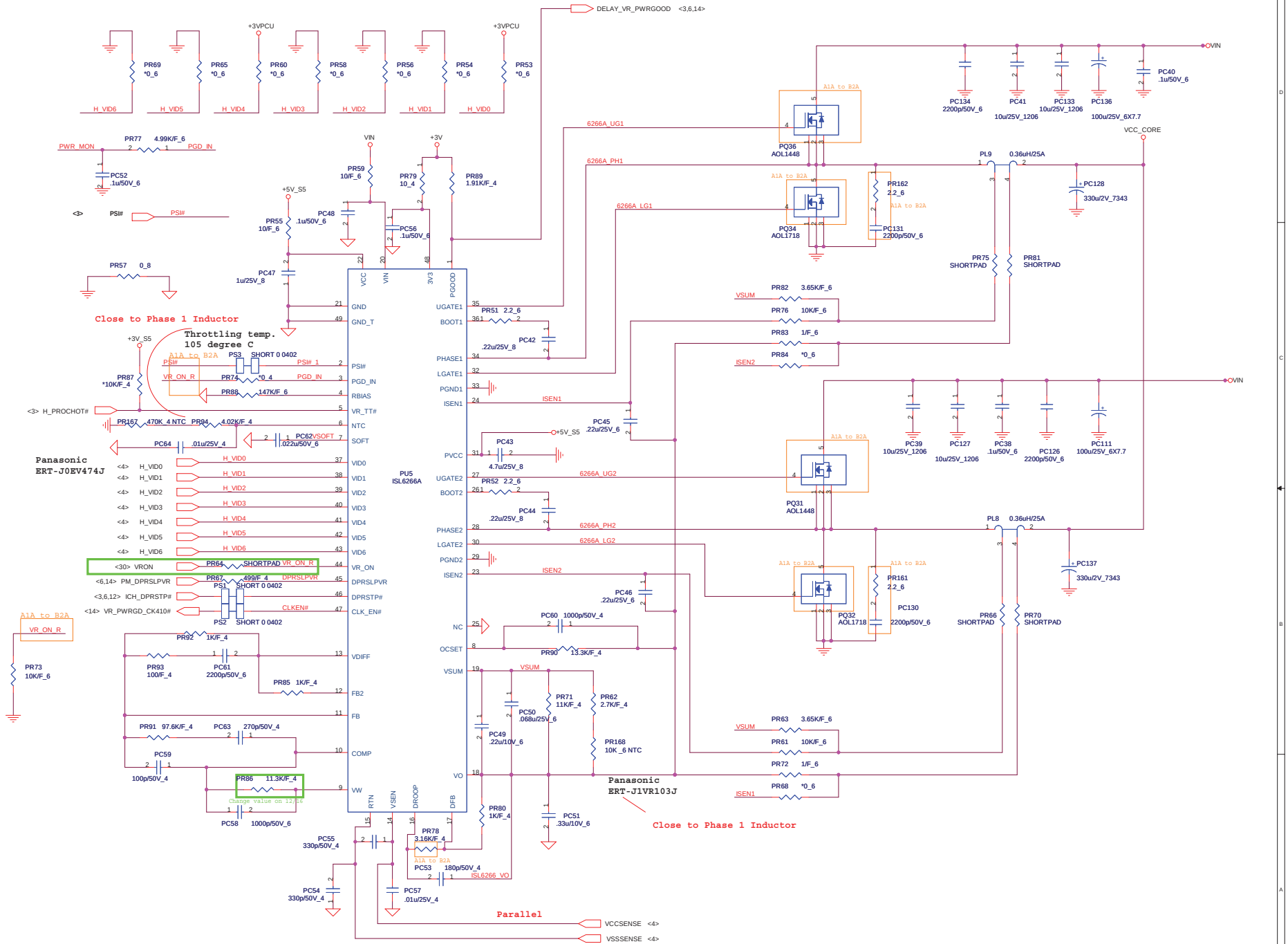
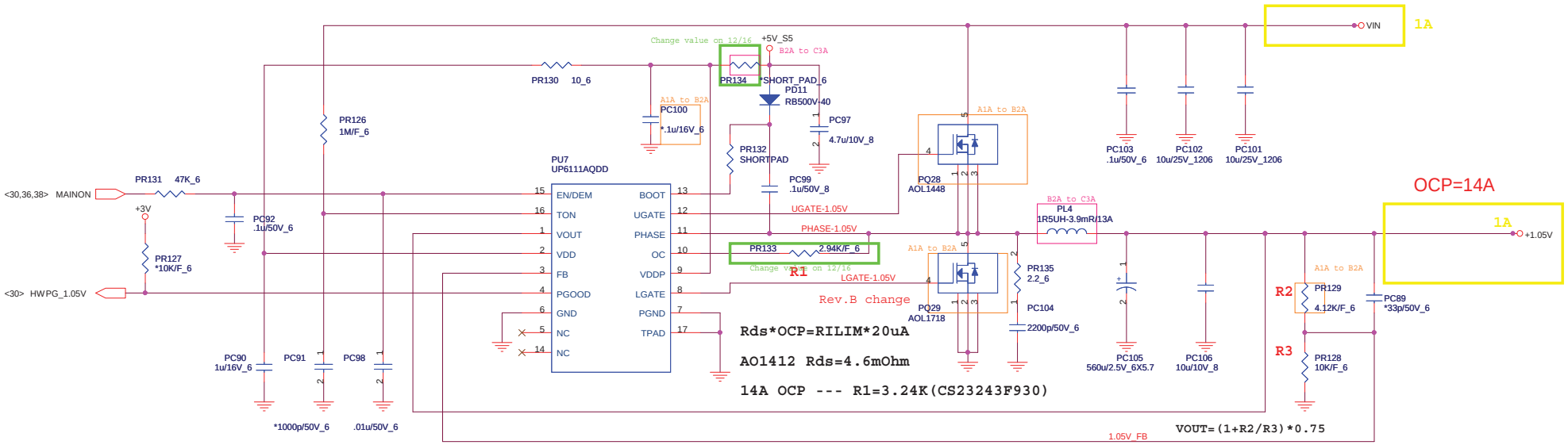






Quanta Computer Inc.			
PROJECT : ZK6			
Size	Document Number		Rev
	CPU CORE(ISL6266A)		1A
Date: Friday, April 14, 2006		Sheet 33 of 42	



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

Quanta Computer Inc.		
PROJECT : ZK6		
Size	Document Number	Rev
	VTT 1.05V (RT8202)	1A
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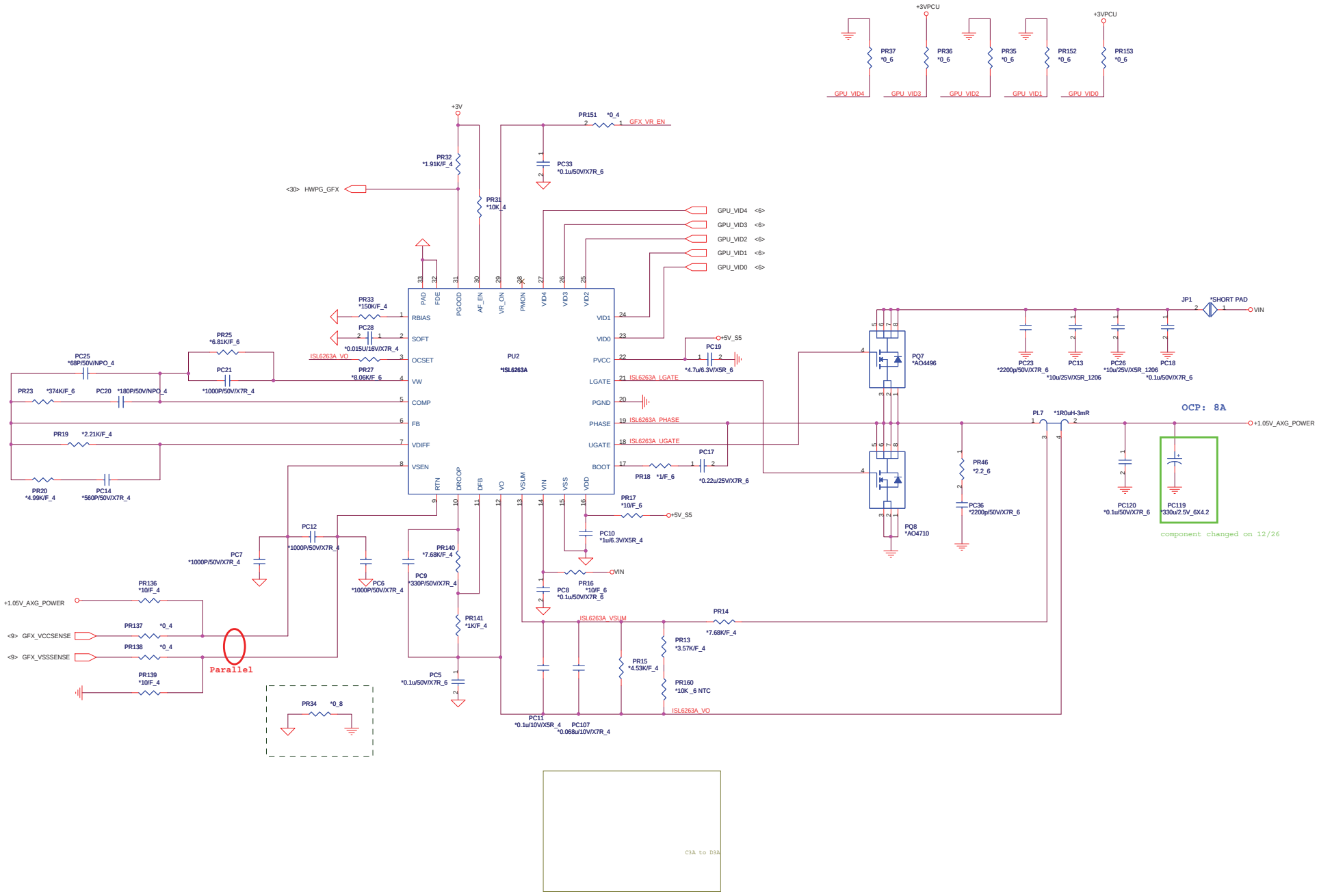
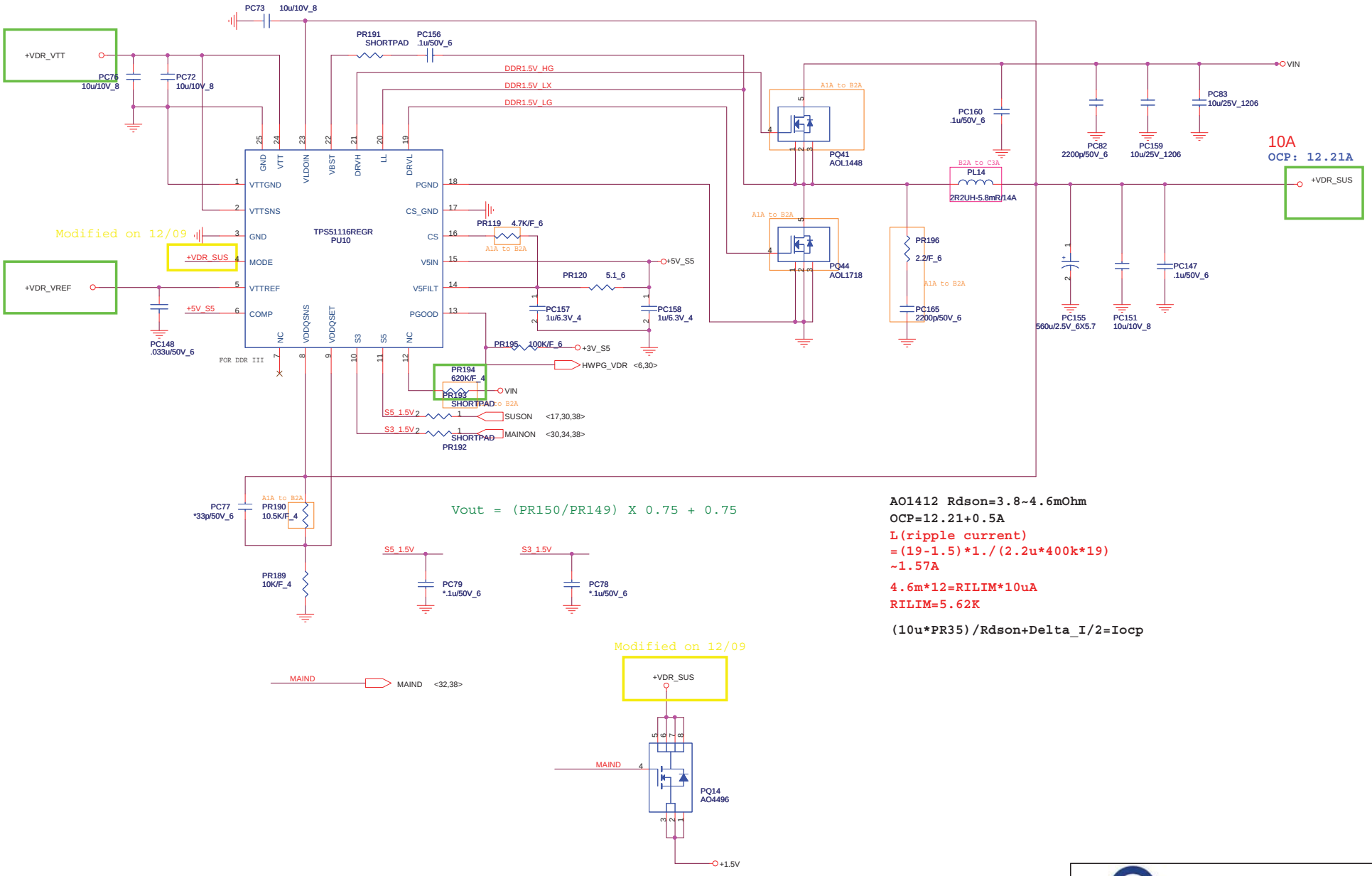
all component in this page would be stuff for UMA only



Quanta Computer Inc.
PROJECT : ZK6

Size	Document Number	Rev
	+1.05V_GFX-ISL6263A	1A
Date: Friday, April 24, 2009	Sheet 35 of 42	



Quanta Computer Inc.	PROJECT : ZK6	
Size	Document Number: DDR 1.8V(TPS51116)	Rev 1A
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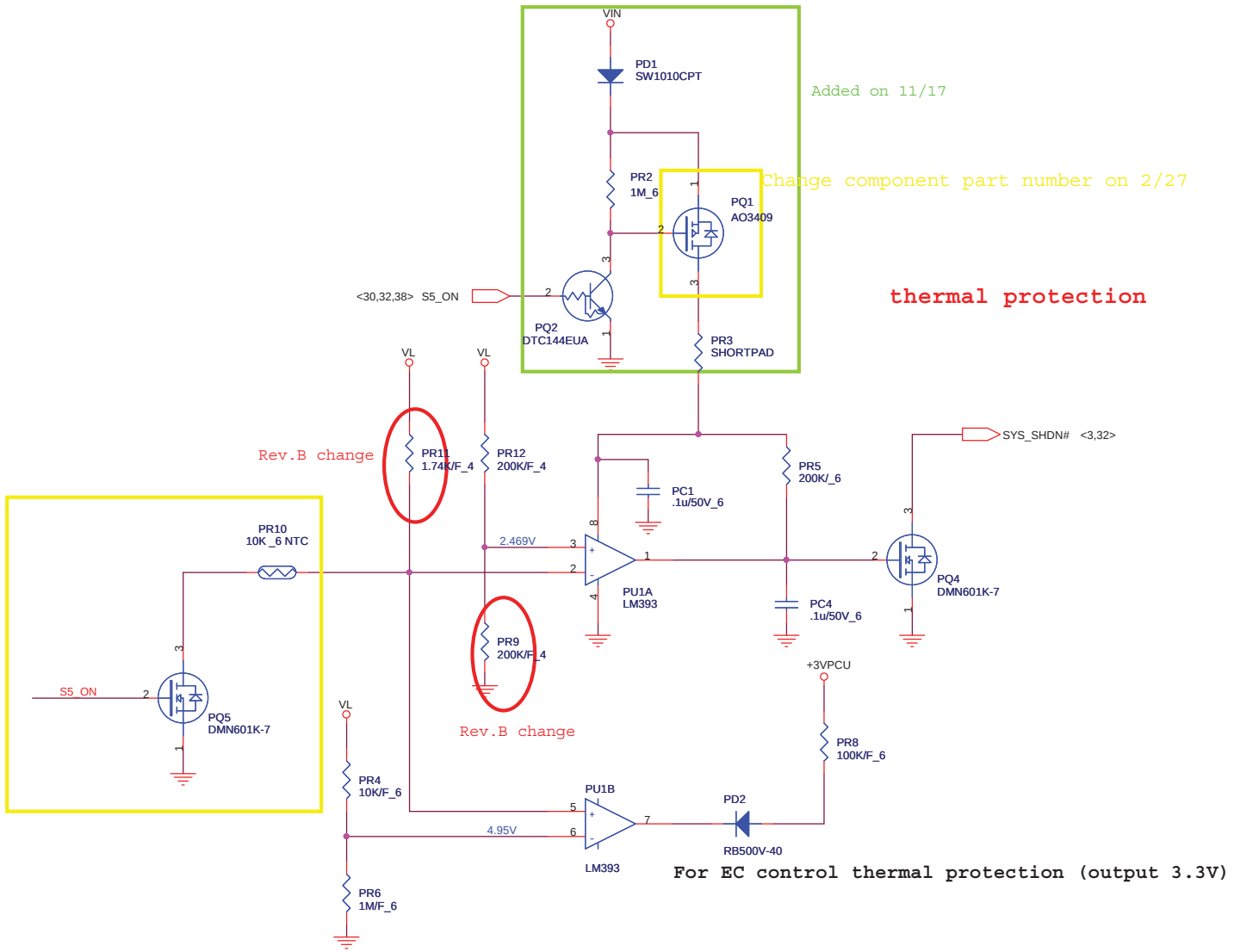

Quanta Computer Inc.

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Size	Document Number	Rev
	Thermal protect	1A
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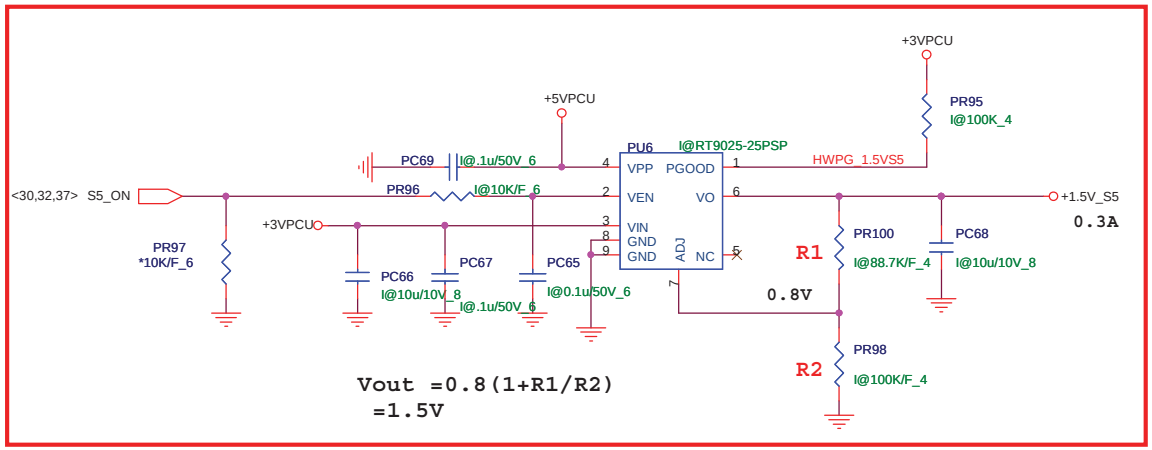

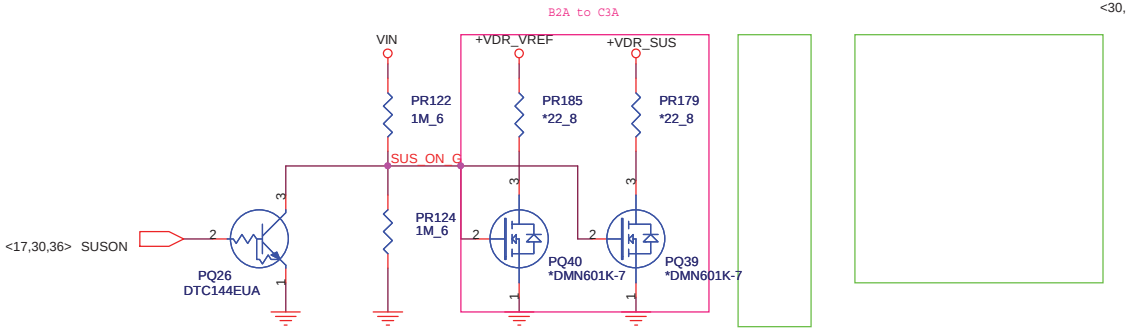

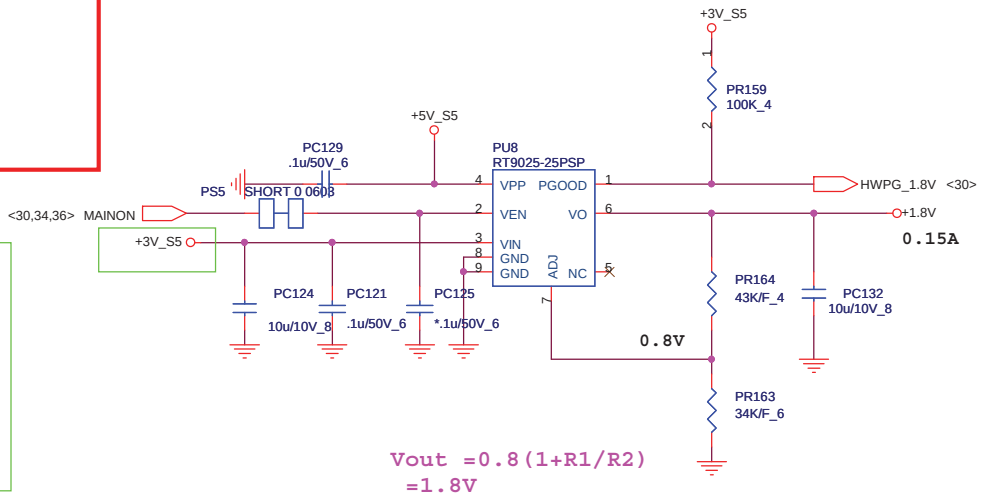

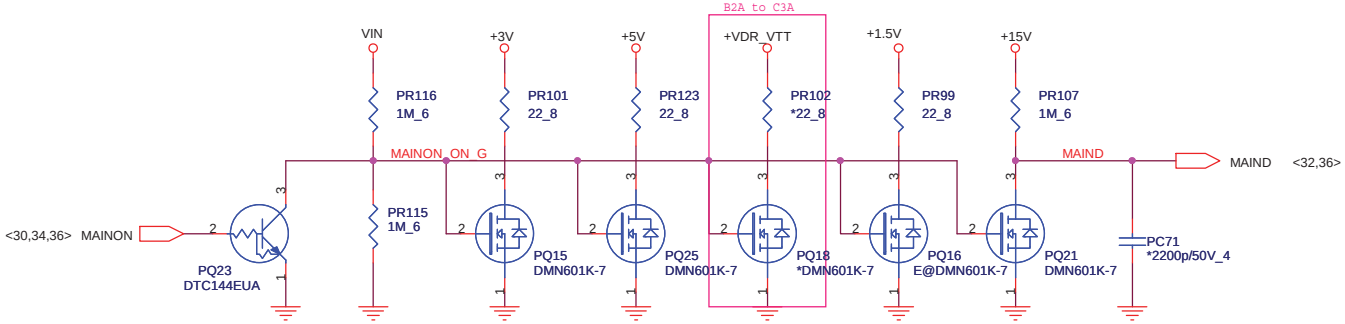

Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	Discharge (2.5V/1.5V)	1A
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