Li 37/39 Block Diagram

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

CPU CORE ISL6266A

CPU Penryn

478P (uPGA)/35W

CPU THERMAL SENSOR

14.318MHz

CLOCK GEN

ALPRS365B MLF64PIN

CLK_CPU_BCLK, CLK_CPU_BCLK#

CLK_MCH_BCLK, CLK_MCH_BCLK#

DREFCLK, DREFCLK#

DREFSSCLK, DREFSSCLK#

VCCP +1.5V AND GMCH 1.05V(RT8204)

DDRII SMDDR_VTERM 1.8V/1.8VSUS(RT8202)

DDRII-SODIMM1

DDRII-SODIMM2

DDRII 667 MHz

DDRII 667MHz

NORTH BRIDGE

Cantiga

GL40

CRT

LCD CONN

DMI LINK

32.768KHz

NBSRCCLK, NBSRCCLK#

SATA - HDD

SATA - CD - ROM

SATA0 150MB

SATA1 150MB

SOUTH BRIDGE

ICH-9M

PCIE X 6

USB X 12

USB2.0

USB2.0 Ports X 3

Webcam

Mini PCI-E x1

Express Card

PCI-E

Azalia

Mini PCI-E Card X 1

LAN Realtek 10/100 RTL8102EL

Express Card power switch RICOH R5538D (NewCard)

Realtek RTS5158E

24.576MHz

25MHz

RJ45

Memory CardReader

Codec Realtek ALC662-GR

Audio Amplifier TPA6017A2

Speaker

SYSTEM POWER MAX17101

32.768KHz

LPC

KBC

ITE 8502E-J

Keyboard

Touch Pad

SYSTEM CHARGER MAX17005

FAN

SPI ROM 8Mbits

Headphone LINE Out SPDIF

LINE IN

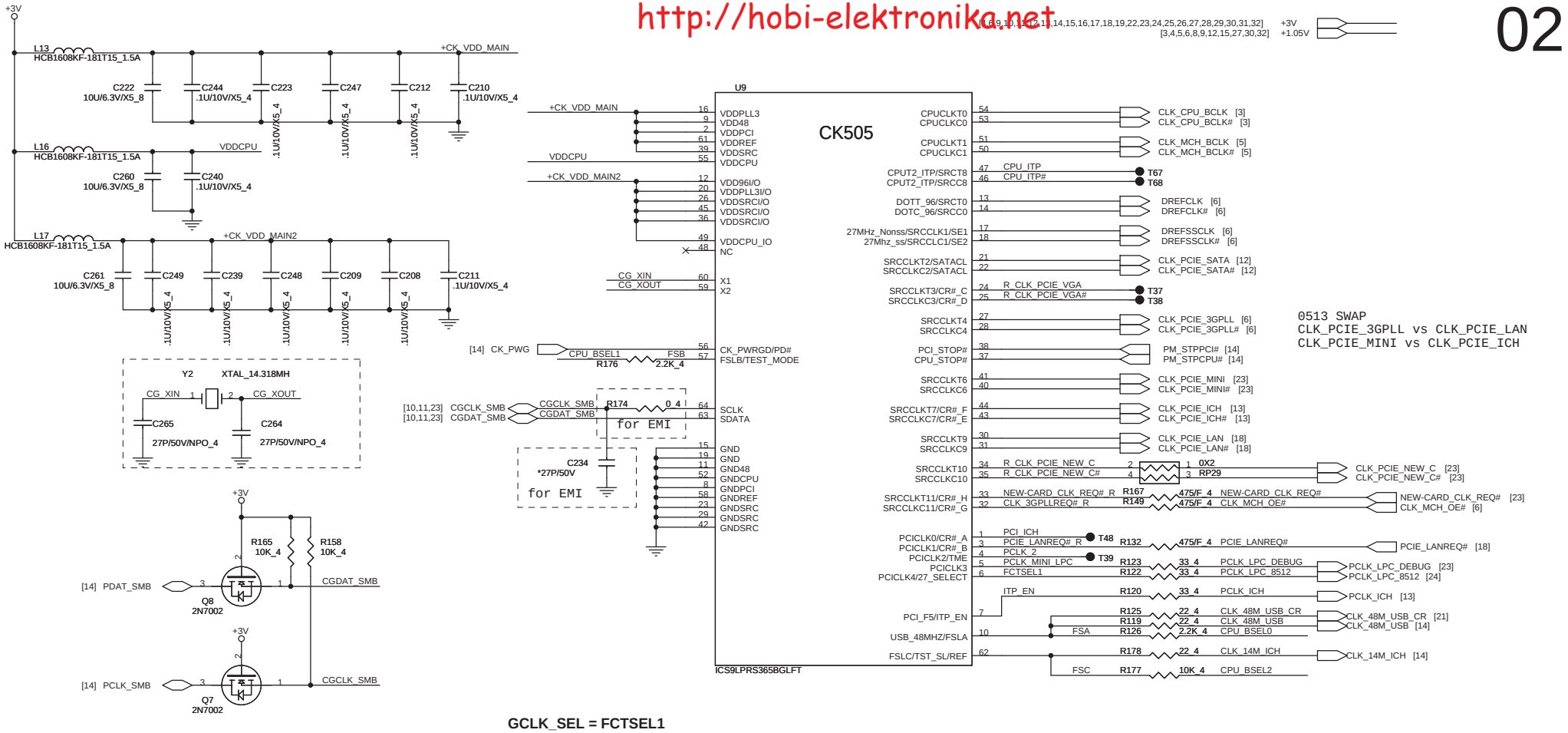
MIC

PROJECT : EF7

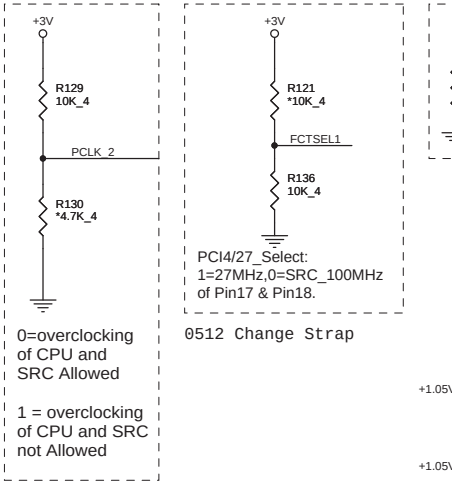
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

Date: Friday, June 13, 2008 Sheet 1 of 34

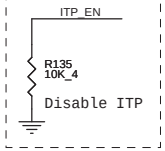


[1,6,9,10,13,14,15,16,17,18,19,22,23,24,25,26,27,28,29,30,31,32] +3V
[3,4,5,6,8,9,12,15,27,30,32] +1.05V



0428 correct Net name PCLK_2

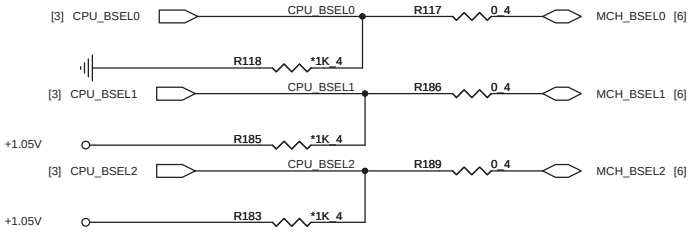
0512 Change Strap



GCLK_SEL = FCTSEL1

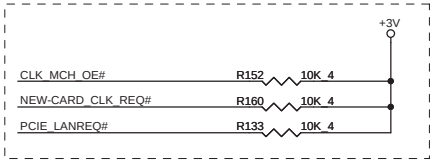
FCTSEL1 (PIN13)	PIN13	PIN14	PIN17	PIN18
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

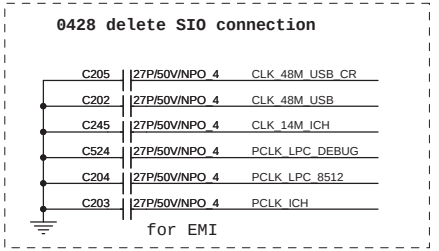
CPU Clock select



0519 Update BSEL default follwed CPU.

2 FSC	1 FSB	0 FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

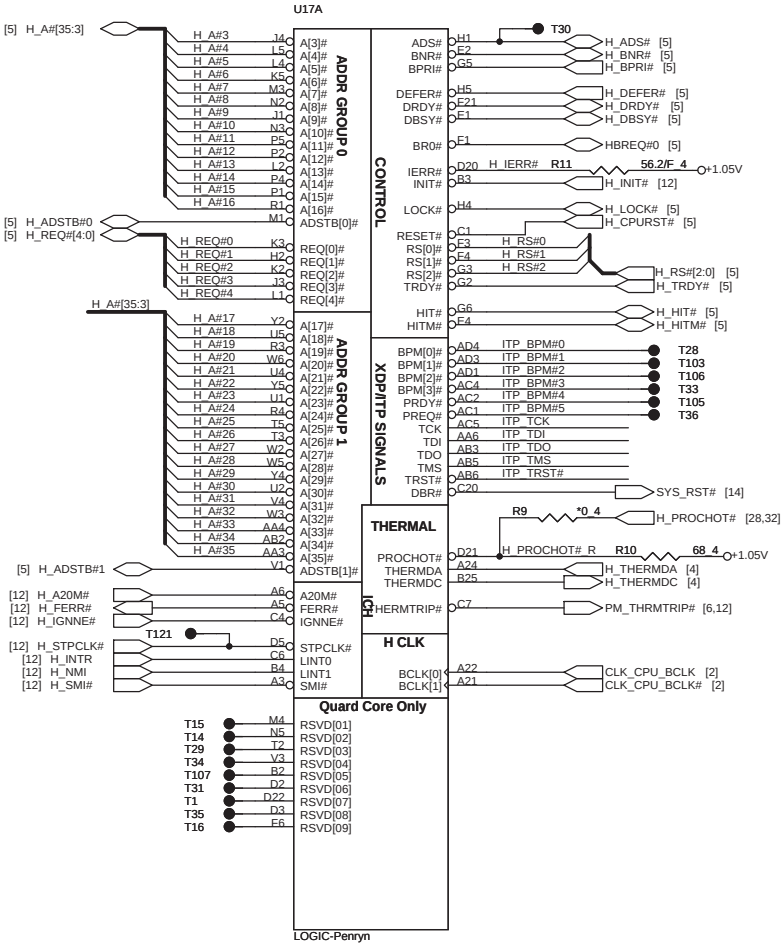


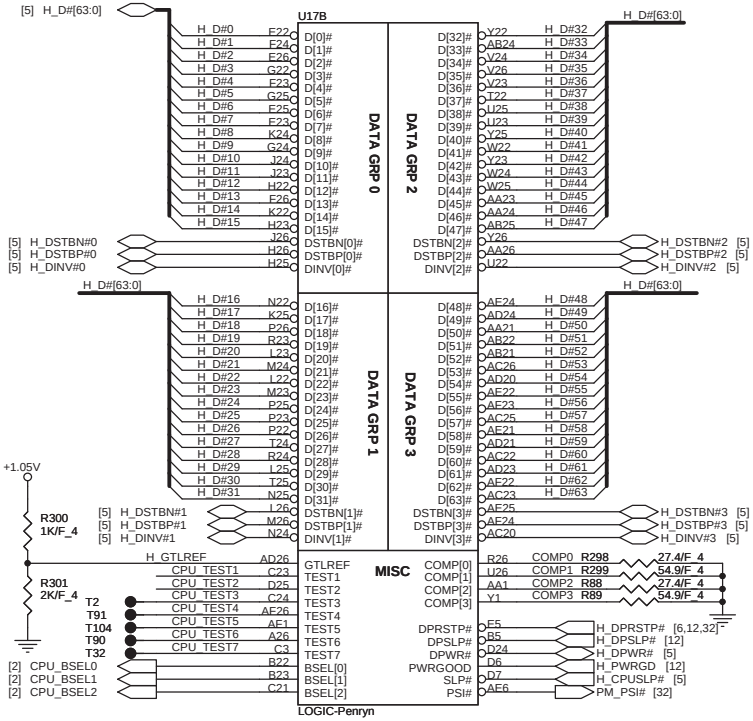


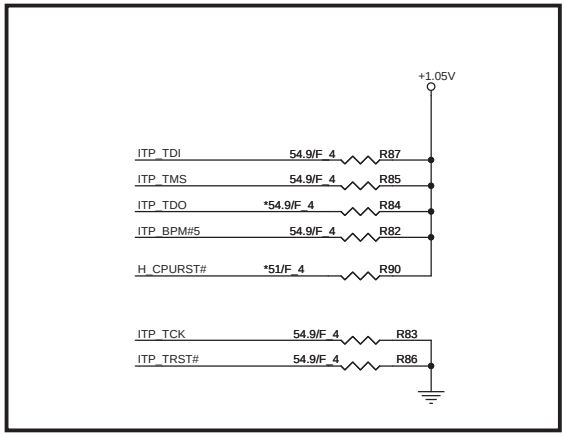
PROJECT : EF7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR	1A

Date: Wednesday, July 02, 2008 Sheet 2 of 34



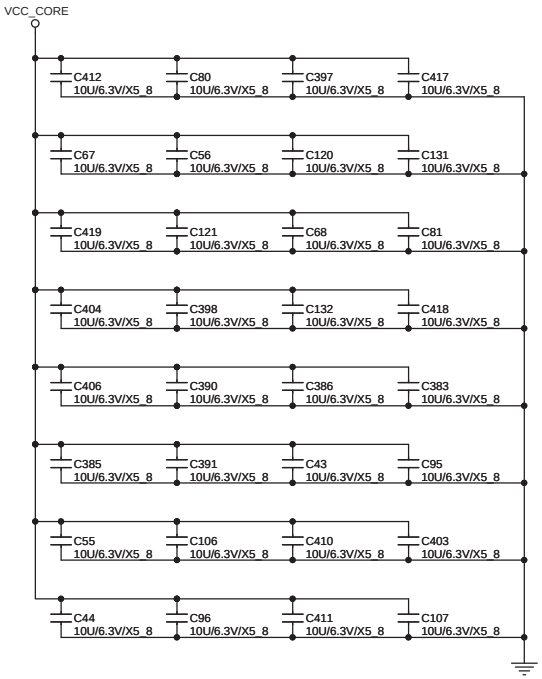


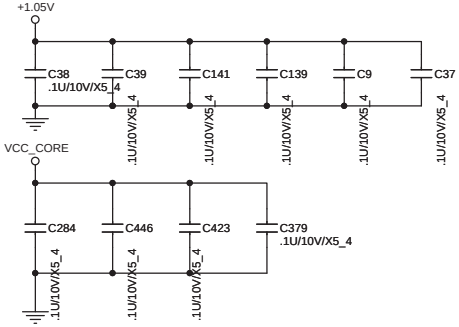


PROJECT : EF7
Quanta Computer Inc.

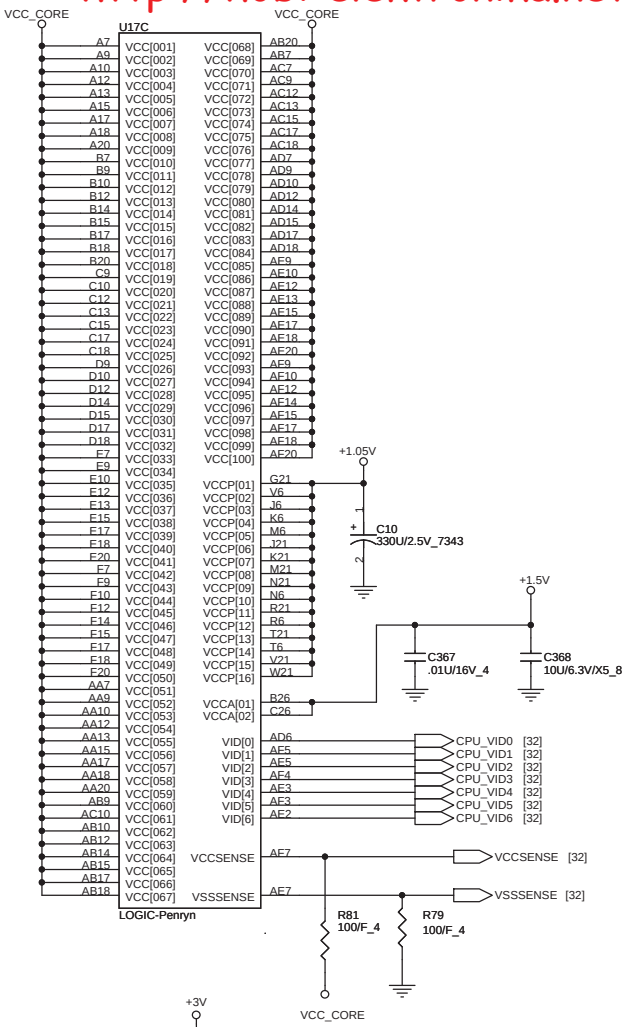
Size	Document Number	Rev
Custom	Penryn 1/2 Host	1A

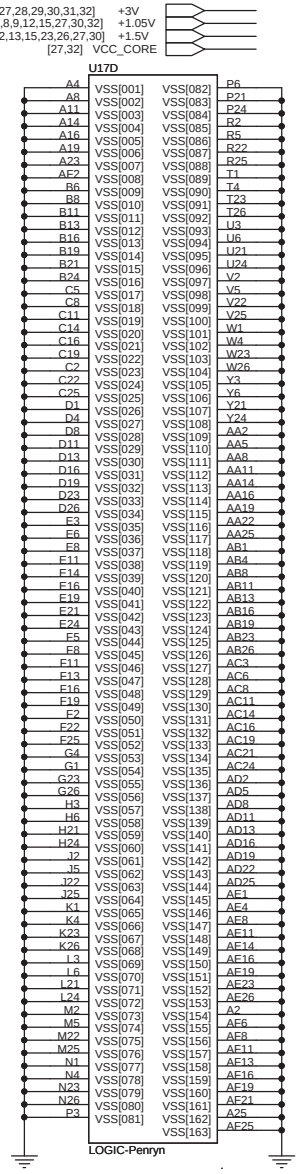
Date: Wednesday, July 02, 2008 Sheet 3 of 34

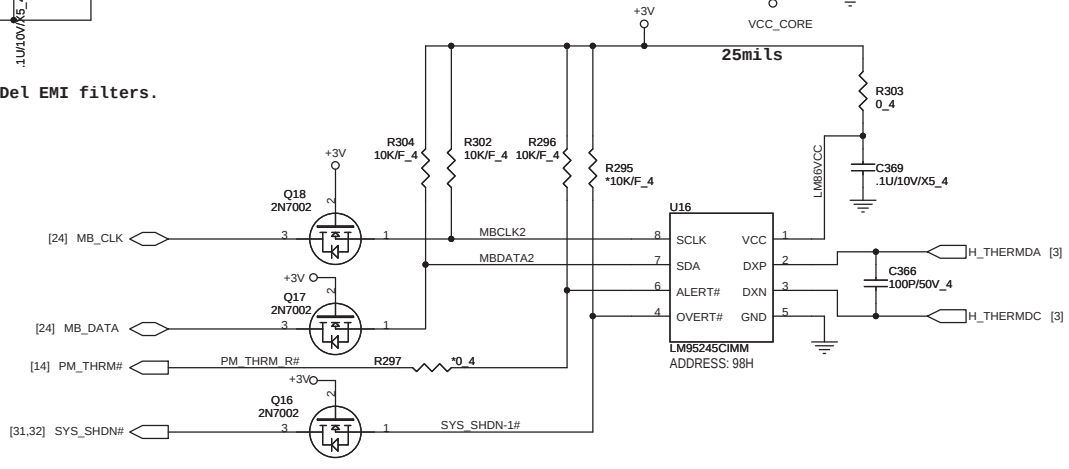




0519 Del EMI filters.

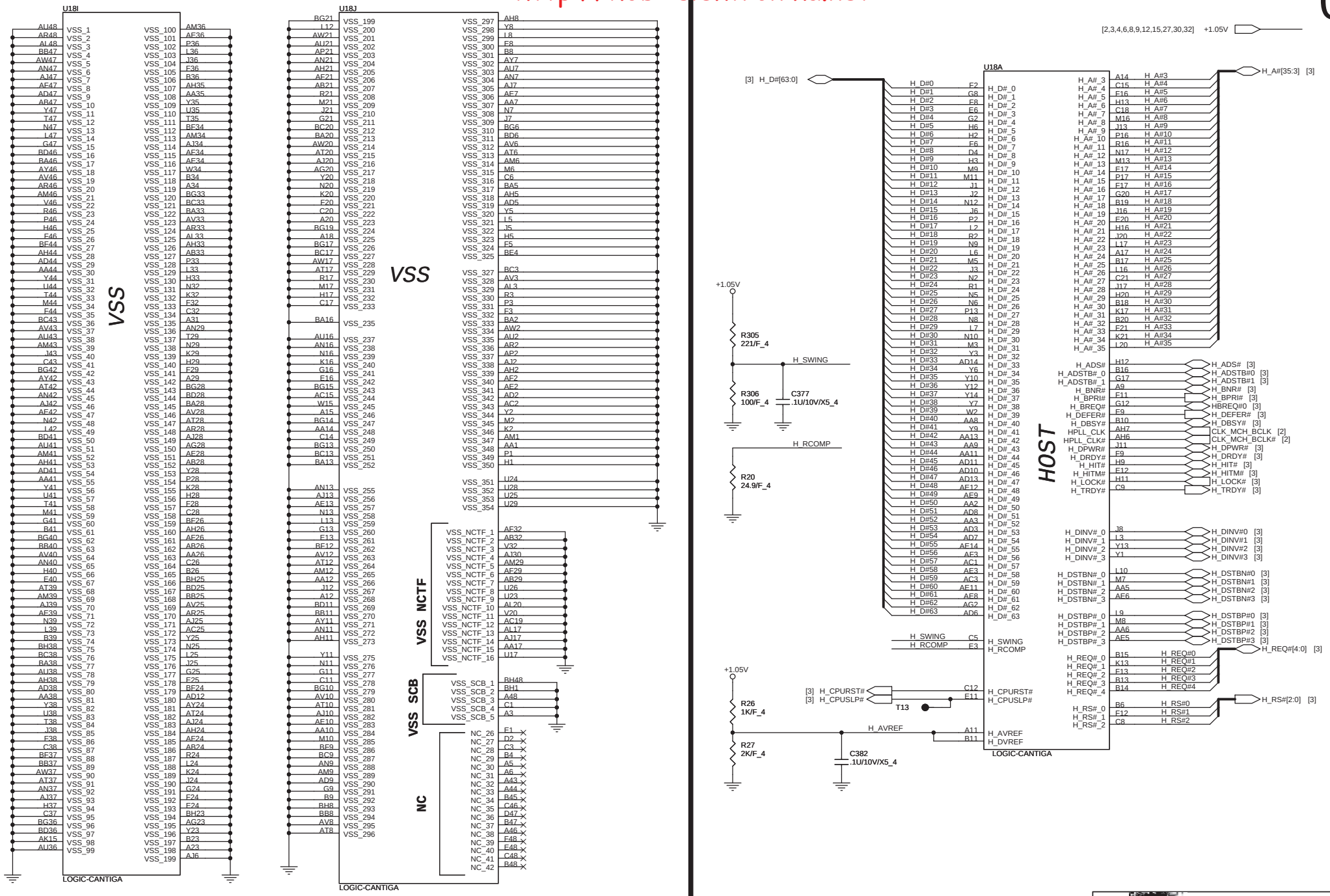






PROJECT : EF7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Penryn 2/2 Power&Thermal	1A
Date: Wednesday, July 02, 2008	Sheet 4 of 34	



PROJECT : EF7			
Quanta Computer Inc.			
Size: Custom	Document Number: Cantiga 1/5 Host&VSS		Rev: 1A
Date: Wednesday, July 02, 2008	Sheet 5 of 34		

MCH_CFG_5 DMIx2 selection

Low: DMIx2
High: DMIx4 (Default)

MCH_CFG_16 FSB Dynamic ODT

Low: Dynamic ODT disabled
High: Dynamic ODT enabled (Default)

MCH_CFG_9 PCI Express Graphic Lane

Low: Reverse Lane
High: Normal operation(Default)

MCH_CFG_19 DMI Lane Reversal

Low: Normal (Default)
High: Lane Reserved

MCH_CFG_6 iTPM Host Interface

Low: iTPM Host Interface enabled
High: iTPM Host Interface disabled (Default)

MCH_CFG_7 Intel (R) Management Engine Crypto

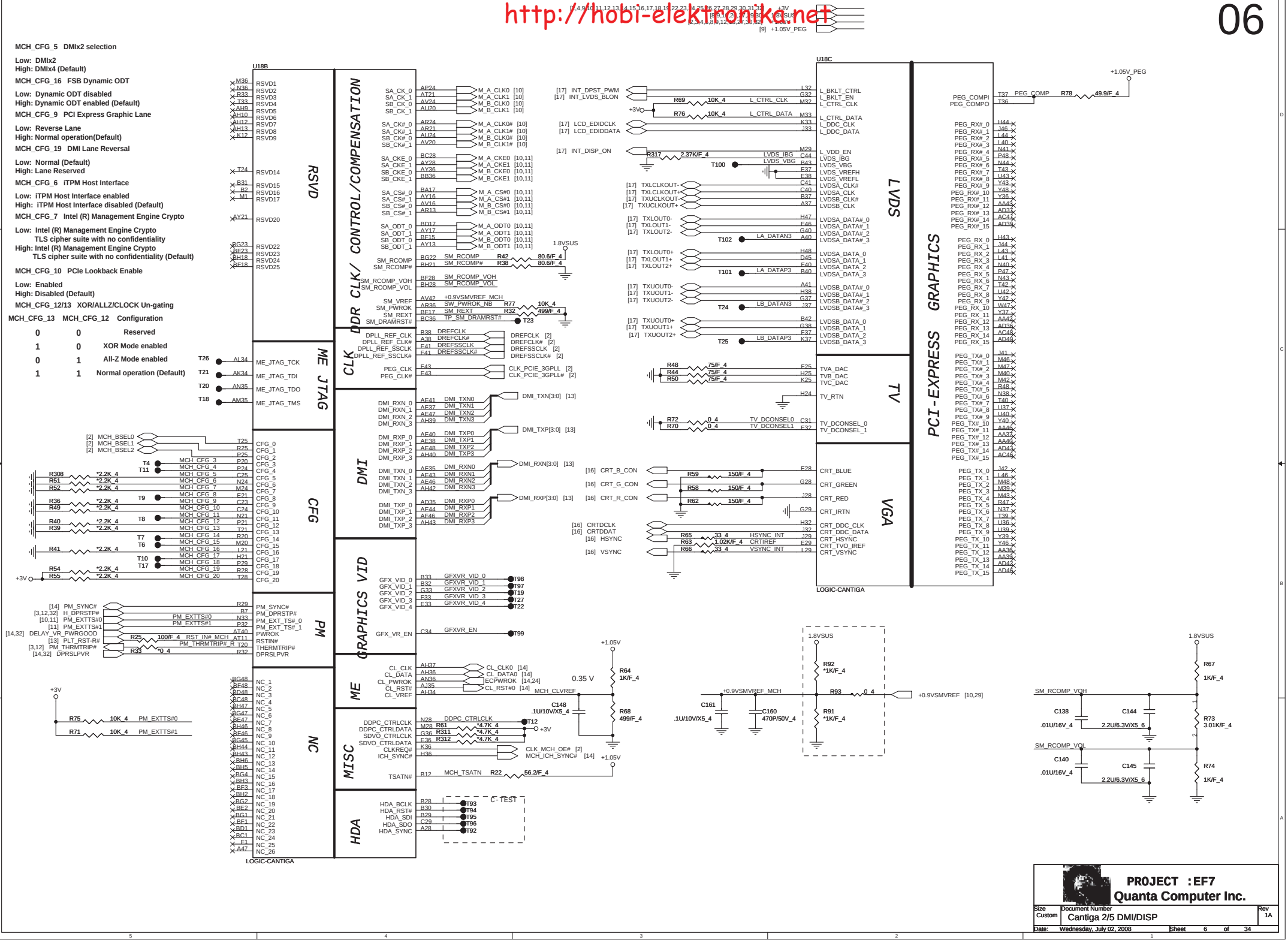
Low: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality
High: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality (Default)

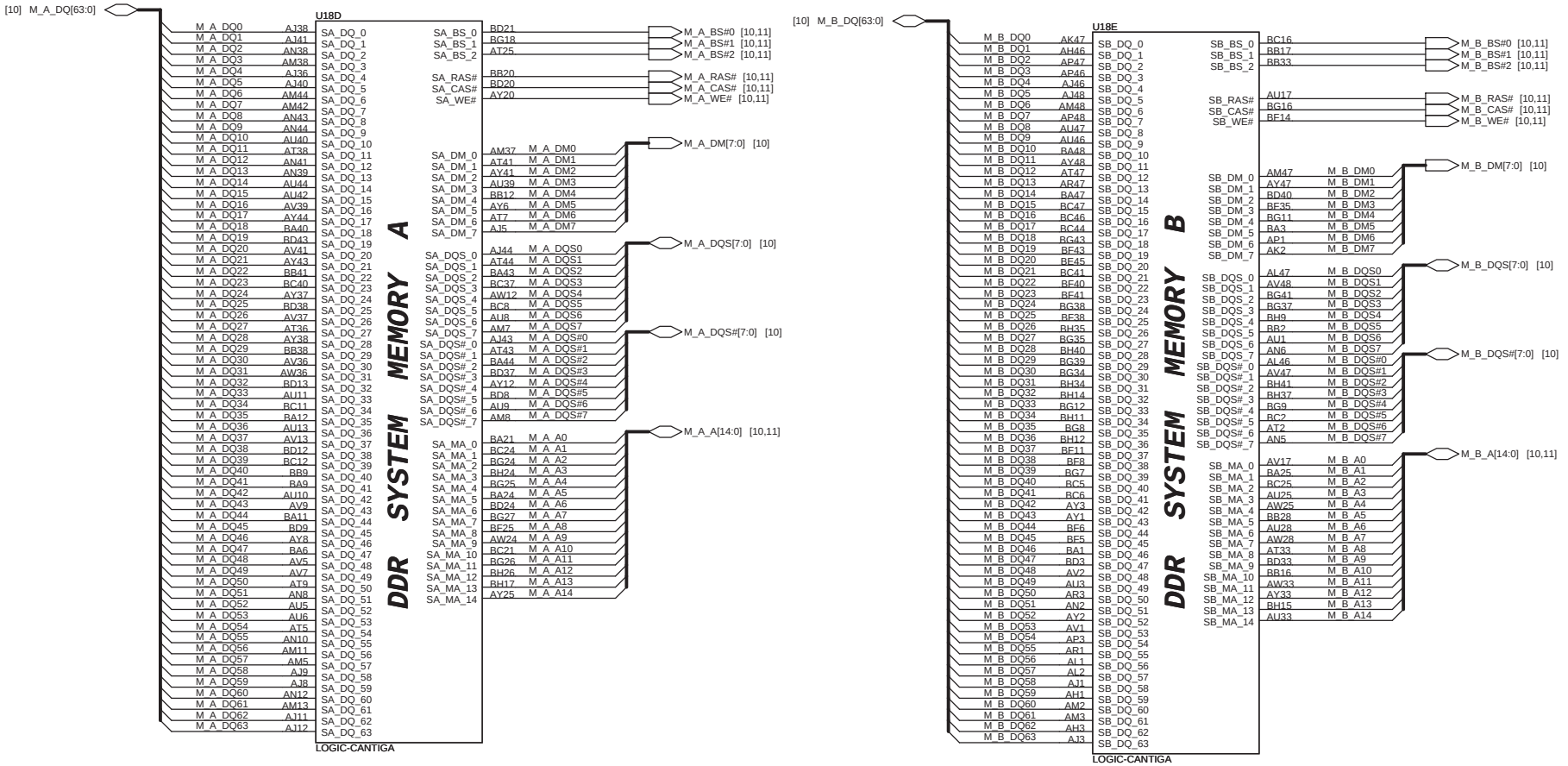
MCH_CFG_10 PCIe Lookback Enable

Low: Enabled
High: Disabled (Default)

MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating

MCH_CFG_13	MCH_CFG_12	Configuration
0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)



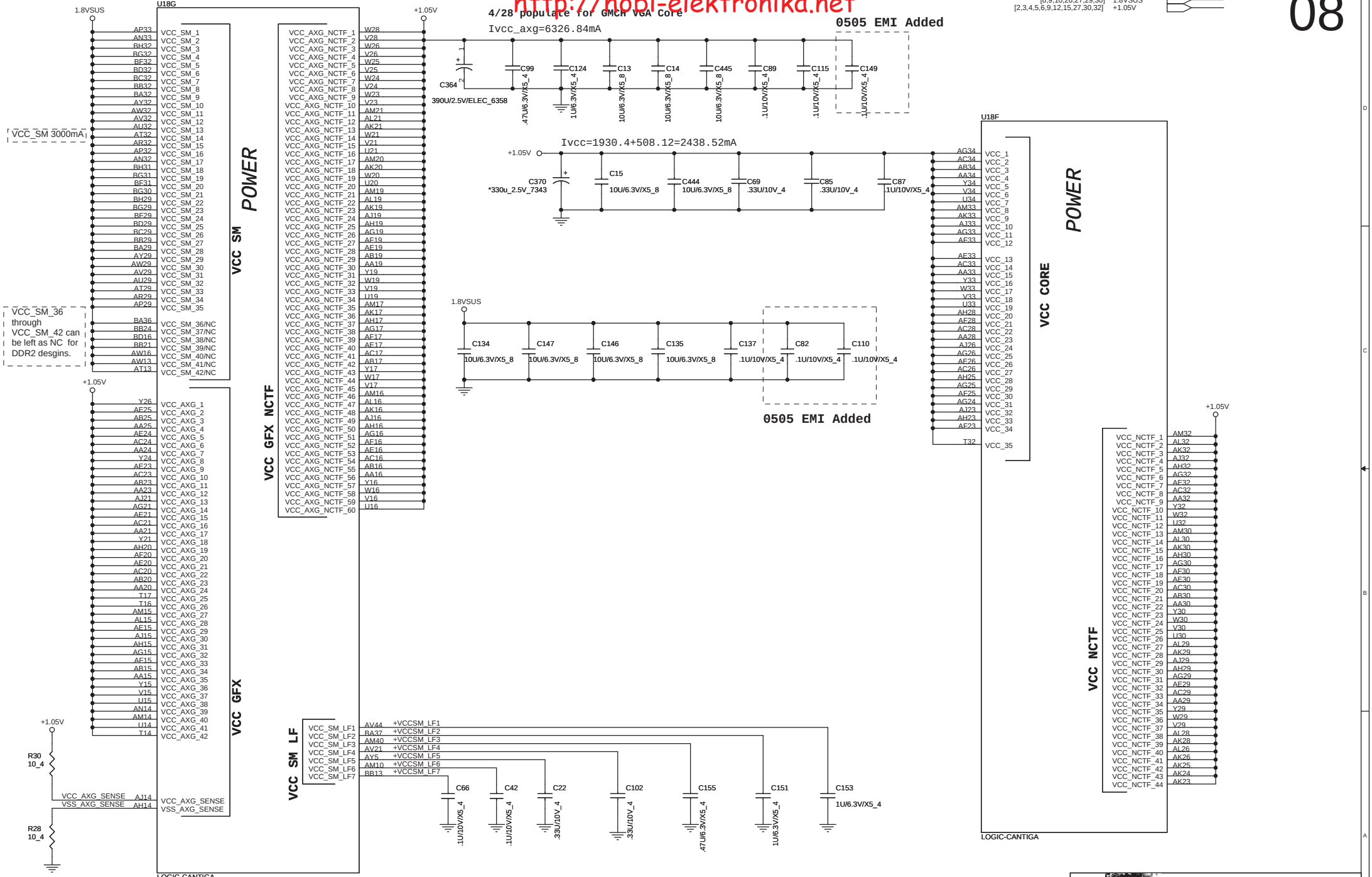


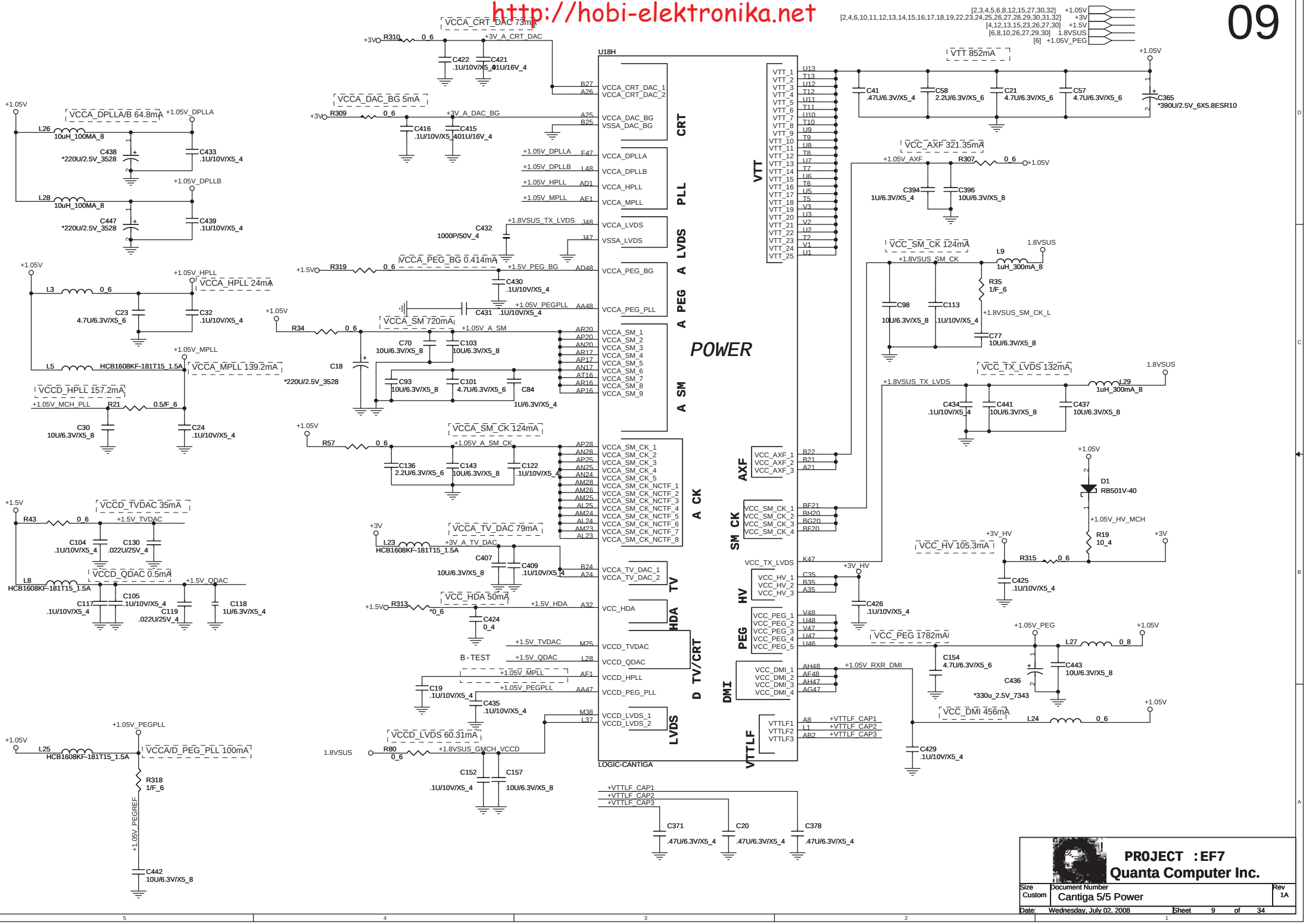
PROJECT : EF7
Quanta Computer Inc.

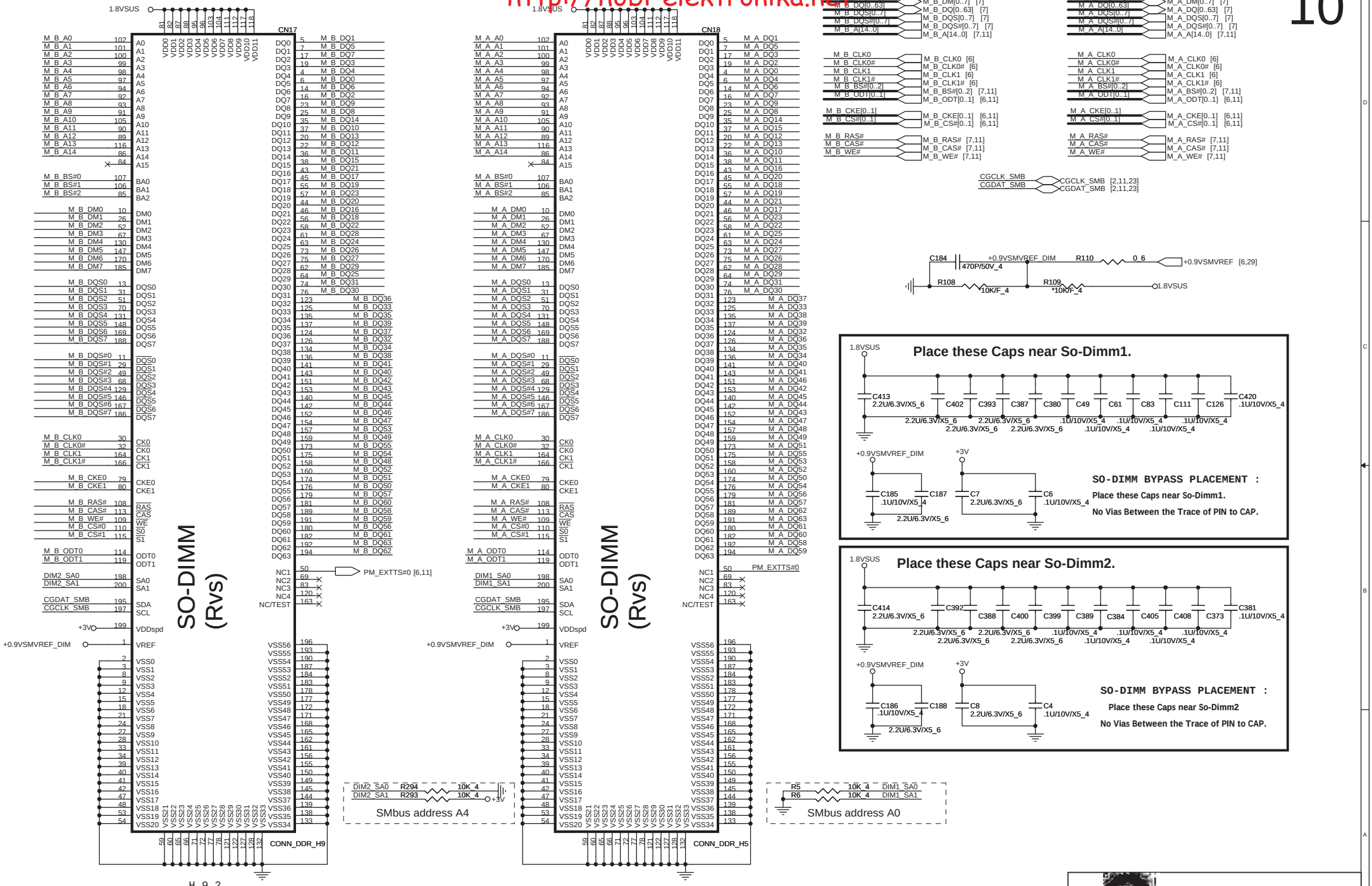
Size	Document Number	Rev
Custom	Cantiga 3/5 DDR2	1A

Date: Wednesday, July 02, 2008 Sheet 7 of 34

[6,9,10,26,27,29,30] 1.8VSUS
[2,3,4,5,6,9,12,15,27,30,32] +1.05V







H 9.2

H 5.2

PROJECT : EF7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2 1/2 DIMM	1A

Date: Wednesday, July 02, 2008 Sheet 10 of 34

[26,27,29] SMDDR_VTERM
[2,4,6,9,10,12,13,14,15,16,17,18,19,22,23,24,25,26,27,28,29,30,31,32] +3V

DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL

SMDDR_VTERM
C50 .1U/10V/X5_4 C78 .1U/10V/X5_4 C108 .1U/10V/X5_4 C40 .1U/10V/X5_4 C79 .1U/10V/X5_4 C123 .1U/10V/X5_4 C36 .1U/10V/X5_4

SMDDR_VTERM
C31 .1U/10V/X5_4 C133 .1U/10V/X5_4 C63 .1U/10V/X5_4 C114 .1U/10V/X5_4 C127 .1U/10V/X5_4 C97 .1U/10V/X5_4

DDRII B CHANNEL

SMDDR_VTERM
C100 .1U/10V/X5_4 C59 .1U/10V/X5_4 C116 .1U/10V/X5_4 C142 .1U/10V/X5_4 C71 .1U/10V/X5_4 C90 .1U/10V/X5_4 C62 .1U/10V/X5_4

SMDDR_VTERM
C112 .1U/10V/X5_4 C52 .1U/10V/X5_4 C86 .1U/10V/X5_4 C94 .1U/10V/X5_4 C34 .1U/10V/X5_4 C45 .1U/10V/X5_4

Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

[6,10] M_A_CS#0
[6,10] M_A_CKE1
[7,10] M_A_BS#0
[6,10] M_A_ODT0
[7,10] M_A_BS#1
[7,10] M_A_WE#
[7,10] M_A_CAS#

RP3: M_A_A13
RP19: M_A_A9, M_A_A5
RP14: M_A_A3, M_A_A1
RP24: M_A_A12
RP10: M_A_A10
RP20: M_A_A7, M_A_A11
RP16: M_A_A4, M_A_A2
RP8
RP22: M_A_A6, M_A_A8
RP6
R60: M_A_A14 — 56.2/F_4
R47: M_B_A14 — 56.2/F_4
56X2 — SMDDR_VTERM

[7,10] M_B_RAS#
[7,10] M_B_BS#2
[6,10] M_B_CKE0
[6,10] M_B_ODT0
[7,10] M_B_BS#1
[7,10] M_B_CAS#
[7,10] M_B_WE#
[7,10] M_B_BS#0
[7,10] M_A_RAS#
[6,10] M_B_CS#0
[6,10] M_B_ODT1
[6,10] M_B_CS#1
[6,10] M_A_CS#1
[6,10] M_A_ODT1
[6,10] M_B_CKE1
[7,10] M_A_BS#2
[6,10] M_A_CKE0

RP11: M_B_A0, M_B_A3
RP13: M_B_A1, M_B_A8
RP17: M_B_A5
RP15: M_B_A2, M_B_A4
RP21: M_B_A12
RP18: M_B_A7, M_B_A6
RP25: M_B_A9
RP7
RP5
RP9: M_B_A10
RP12
RP4: M_A_A0, M_B_A13
RP1
RP2
RP23: M_B_A11
RP26
56X2 — SMDDR_VTERM

M_B_A[14..0] M_B_A[14..0] [7,10]
M_A_A[14..0] M_A_A[14..0] [7,10]

Uninstall

+3V
R7 *200_4
C5 *.01U/16V_4
LM86_3V
DDR_THERMDA
DDR_THERMDC
Q1 *MMBT3904-7-F

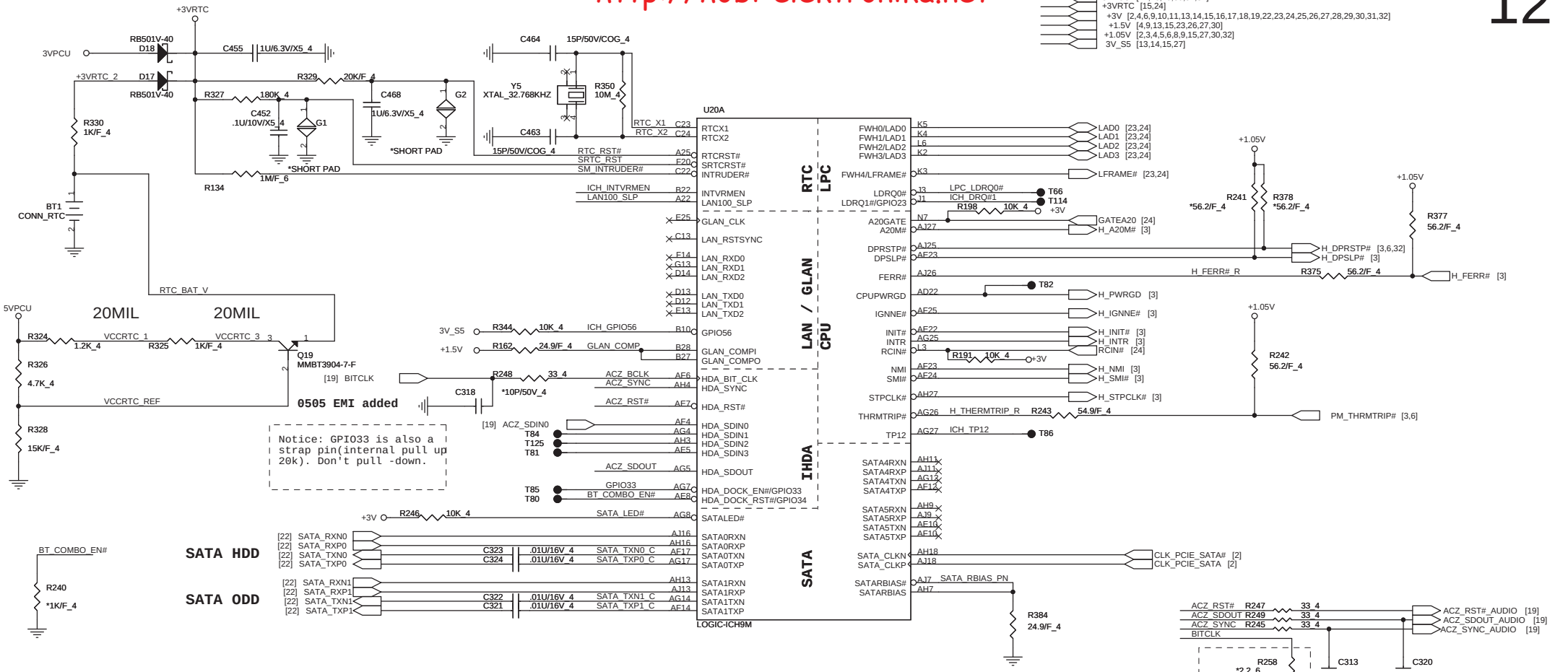
U1
[2,10,23] CGCLK_SMB — CGCLK_SMB — 8 SCLK
[2,10,23] CGDAT_SMB — CGDAT_SMB — 7 SDA
[6,10] PM_EXTTS#0 — PM_EXTTS#0 — 6 ALERT#
[6] PM_EXTTS#1 — R8 *0_4 — PM_EXTTS#1_D — 4 OVERT#
VCC 1
DXP 2
DXN 3
GND 5
*LM86CIMM

PROJECT : EF7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2 2/2 termination	1A

Date: Wednesday, July 02, 2008 Sheet 11 of 34

3VPCU [17,18,24,25,26,27,28,31,33]
5VPCU [27,28,29,30,31,32]
+3VRTC [15,24]
+3V [2,4,6,9,10,11,13,14,15,16,17,18,19,22,23,24,25,26,27,28,29,30,31,32]
+1.5V [4,9,13,15,23,26,27,30]
+1.05V [2,3,4,5,6,8,9,15,27,30,32]
3V_S5 [13,14,15,27]



SB Strap

ICH9-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH9-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPI_CS#1	
SPI	0	1	
PCI	1	0	
LPC	1	1	(default)

No Reboot Strap	
ACZ_SPKR	Low: Default Hi: No reboot

A16 swap override strap	
PCI_GNT#3	Low = A16 swap override enabled Hi = Default

TPM physical presence	
ICH_GPIO57	Low: Default

PROJECT : EF7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M 1/4 Host	1A

Date: Wednesday, July 02, 2008 Sheet 12 of 34

[4,9,12,15,23,26,27,30] +1.5V
[2,4,6,9,10,11,12,14,15,16,17,18,19,22,23,24,25,26,27,28,29,30,31,32] +3V
[12,14,15,27] 3V_S5

EXPRESS CARD (NEW CARD)

MINI CARD PCI-E(WLAN)

PCIE-LAN

U20D

PCI-Express

Direct Media Interface

SPI

USB

LOGIC-ICH9M

USB Connector
Card Reader
Webcam
BLUETOOTH

NEW CARD

USB Connector
USB Connector
WLAN Min-Card

RP28 RP27 RP30 RP31 8.2KX8

4/28 Delete HDCP ROM block

U20B

PCI

Interrupt I/F

LOGIC-ICH9M

Notice: GPIO55,53,51 signal has a week internal pull-up 20k for functional strap.Don't pull-down.

U8 *MC74VHC1G08DFT2G

C213 *.1U/10V_4

R164 100K_4

R161 *100K_4

R166 0_4

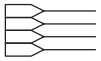
PLTRST# [18,23]

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT
CardBus/1394 /Card Reader	AD21	0	E,F

PROJECT : EF7 Quanta Computer Inc.			
Size: Custom	Document Number: ICH9-M 2/4 PCIE		Rev: 1A
Date: Wednesday, July 02, 2008	Sheet 13 of 34		

[4,9,12,13,15,23,26,27,30] +1.5V
[2,4,6,9,10,11,12,13,15,16,17,18,19,22,23,24,25,26,27,28,29,30,31,32] +3V
[12,13,15,27] 3V_S5
[21,23,26,27,32] 3VSUS



U20C

[2] PCLK_SMB
[2] PDAT_SMB
PCLK_SMB G16
PDAT_SMB A13
SMB_LINK_ALERT# E17
SMB_CLK_ME C17
SMB_DATA_ME B18
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
SMB

PM_RI# F19
RI#

T72
LPC_PD# R4
[3] SYS_RST# SYS_RST# G19
SUS_STAT#/LPCPD#
SYS_RESET#

[6] PM_SYNC# M6
PMSYNC#/GPIO0

SMB_ALERT# A17
SMBALERT#/GPIO11

[2] PM_STPPCI# A14
[2] PM_STPCPU# F19
STP_PCI#
STP_CPU#

[24] CLKRUN# CLKRUN# L4
CLKRUN#

[18,23] PCIE_WAKE# PCIE_WAKE# E20
[24] SERIRQ SERIRQ M5
[4] PM_THRM# PM_THRM# AJ23
WAKE#
SERIRQ
THRM#

VR_PWRGO_CLKEN D21
VRMPWRGD

T112 ICH_TP11 A20
TP11

SYS GPIO

T87 ICH_GPIO1 AG19
[24] KBSMI# KBSMI# AH21
[24] SCI# SCI# AG21
SWI# A21
T113 LAN_PHYPC C12
T61 ENERGY_DEC C21
T53 BOARD_ID0 AE18
ICH_GPIO18 K1
T116 BOARD_ID3 AJ22
WAN_OFF# A9
T109 D19
[23,25] WLAN_OFF#
ICH_GPIO35 I1
R429 0_4 ICH_GPIO38 AE19
[26] CAMERA_ON# ICH_GPIO39 AG22
T88 ICH_GPIO48 AF21
T89 ICH_GPIO49 AH24
T122 A8
[12] ICH_GPIO57

GPIO1
GPIO6
GPIO7
GPIO8
GPIO12
GPIO13
GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
GPIO27
GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5

GPIO Controller Link

[12,19] ACZ_SPKR M7
[6] MCH_ICH_SYNC# AJ24
[12] ICH_TP3 ICH_TP3 B21
ICH_TP8 AH20
T126 ICH_TP9 AJ20
T123 ICH_TP10 AJ21
T124

SPKR
MCH_SYNC#
TP3
TP8
TP9
TP10

MISC

LOGIC-ICH9M

SATA GPIO

SATA0GP/GPIO21 AH23 BOARD_ID2
SATA1GP/GPIO19 AF19 BOARD_ID1
SATA4GP/GPIO36 AF21 BOARD_ID4
SATA5GP/GPIO37 AD20 BOARD_ID5

Clocks

CLK14 H1 CLK_14M_ICH [2]
CLK48 AF3 CLK_48M_USB [2]
SUSCLK P1 SUSCLK T118

SLP_S3# C16 SUSB# [24]
SLP_S4# E16 SUSC# [24]
SLP_S5# G17 SLP_S5# T64

S4_STATE#/GPIO26 C10 S4_STATE# T57
PWROK G20 PM_ICH_PWROK
DPRSLPVR/GPIO16 M2 DPRSLPVR [6,32]
BATLOW# B13 PM_BATLOW#
PWRBTN# R3 DNBSWON# DNBSWON# [24]
LAN_RST# D20 ICH_LAN_RST# R144 0_4
RSMRST# D22 RSMRST# RSMRST# [24]
CK_PWRGD R5 CK_PWG [2]
CLPWROK R6 ECPWROK
SLP_M# B16 ICH_SLP_M# T111

Power MGT

CL_CLK0 F24 CL_CLK0 [6]
CL_CLK1 B19 CL_CLK1 [23]
CL_DATA0 F22 CL_DATA0 [6]
CL_DATA1 C19 CL_DATA1 [23]
CL_VREF0 C25 CL_VREF0_ICH
CL_VREF1 A19 CL_VREF1_ICH
CL_RST0# F21 CL_RST#0 [6]
CL_RST1# D18 CL_RST#1 [23]

MEM_LED/GPIO24 A16 BT_ON# BT_ON# [26]
GPIO10/SUS_PWR_ACK C18 SUS_PWR_ACK
GPIO14/AC_PRESENT C11 AC_PRESENT
WOL_EN/GPIO9 C20 ICH_WOL_EN T110
R146 100K_4

3V_S5
R336 *3.24K/F_4
+3V
R156 3.24K/F_4
0.405V
C466 *.1U/10V_4
R340 *453/F_4
C225 .1U/10V/X5_4
R157 453/F_4

SWI# R331 10K_4
PM_RI# R153 10K_4
SMB_CLK_ME R150 10K_4
SMB_DATA_ME R335 10K_4
DNBSWON# R362 10K_4
PCLK_SMB R142 2.2K_4
PDAT_SMB R345 2.2K_4
SMB_ALERT# R346 10K_4
PCIE_WAKE# R143 10K_4
PM_BATLOW# R337 8.2K_4
SMB_LINK_ALERT# R151 10K_4
SYS_RST# R148 10K_4

3V_S5

+3V
ICH_TP3 R347 *10K_4
PM_THRM# R388 8.2K_4
SERIRQ R194 10K_4
CLKRUN# R190 8.2K_4
KBSMI# R385 10K_4
SCI# R259 10K_4
ICH_GPIO35 R356 10K_4

ICH_GPIO38 R221 10K_4
SUS_PWR_ACK R147 10K_4
RSMRST# R145 10K_4

Notice: GPIO20 signal should not be pulled high for functional strap(internal pull down 20k).

Notice: GPIO49 is also a strap pin(internal pull up 20k). Don't pull-down.

0616 Connect GPIO38 R429 to CAMERA power ON in Ver.B

+3V
PR89 1K/F_4
VR_PWRGO_CLKEN
Q6 2N7002
[32] VR_PWRGD_CK410#
R138 100K_4

+3V 3VSUS
R124 *2K/F_4
C207 .1U/10V/X5_4
U7 MC74VHC1G08DFT2G
[6,32] DELAY_VR_PWRGOOD
[6,24] ECPWROK ECPWROK
PM_ICH_PWROK
R127 10K_4
R128 *0_4

+3V
R218 10K_4 BOARD_ID0 R217 *10K_4
R260 10K_4 BOARD_ID1 R261 *10K_4
R381 10K_4 BOARD_ID2 R382 *10K_4
R387 *10K_4 BOARD_ID3 R386 10K_4
R253 *10K_4 BOARD_ID4 R252 10K_4
R254 *10K_4 BOARD_ID5 R255 10K_4

Board ID For Function	0	1
ID0, GPIO17	Camera attached	Camera NC<Default>
ID1, GPIO19	UXGA support	XGA support<Default>
ID2, GPIO21	EF7 Keyboard	EF9 Keyboard<Default>
ID3	Default	
ID4	Default	
ID5	Default	

EC GPE2 Pin83 EF7 Keyboard EF9 Keyboard

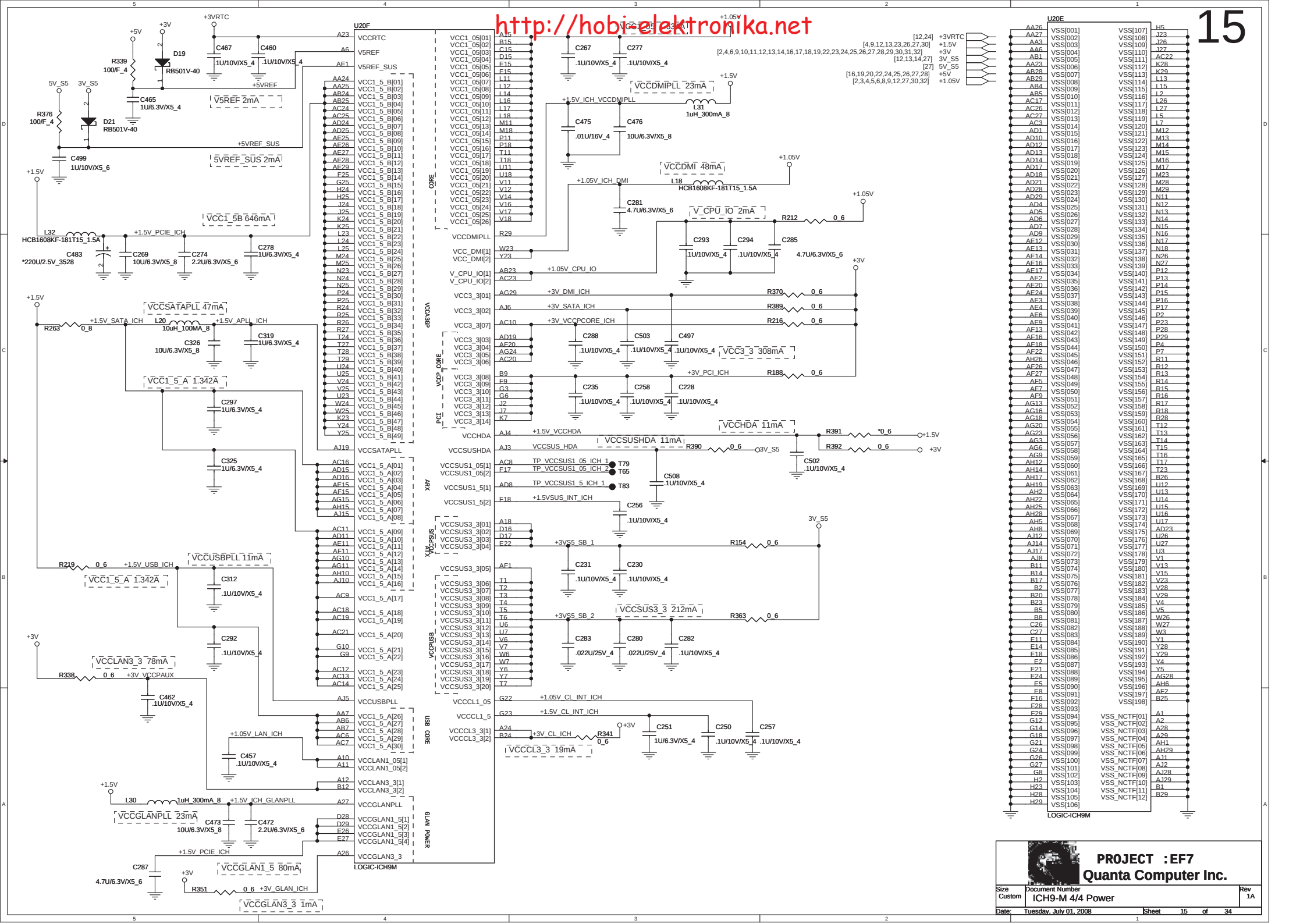
BOARD_ID0 BOARD_ID0 [26]
BOARD_ID1 BOARD_ID1 [17]
BOARD_ID2 BOARD_ID2 [26]

Camera HW detection
XGA/UXGA selection
EF7/EF9 keyboard selection

0609 Define ID for Ver.B
0626 Modify ID2 for leakage concern in Ver.B

PROJECT : EF7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M 3/4 GPIO	2A
Date: Wednesday, July 02, 2008	Sheet 14 of 34	



PROJECT : EF7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M 4/4 Power	1A

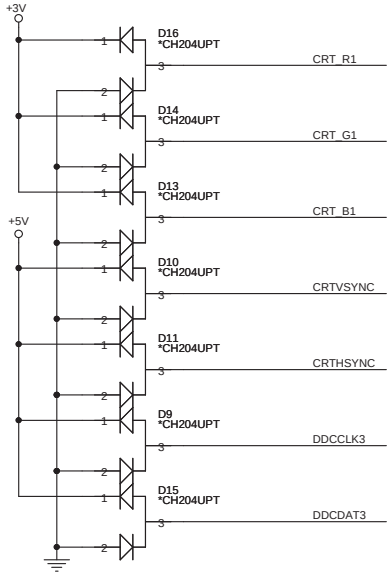
Date: Tuesday, July 01, 2008 Sheet 15 of 34

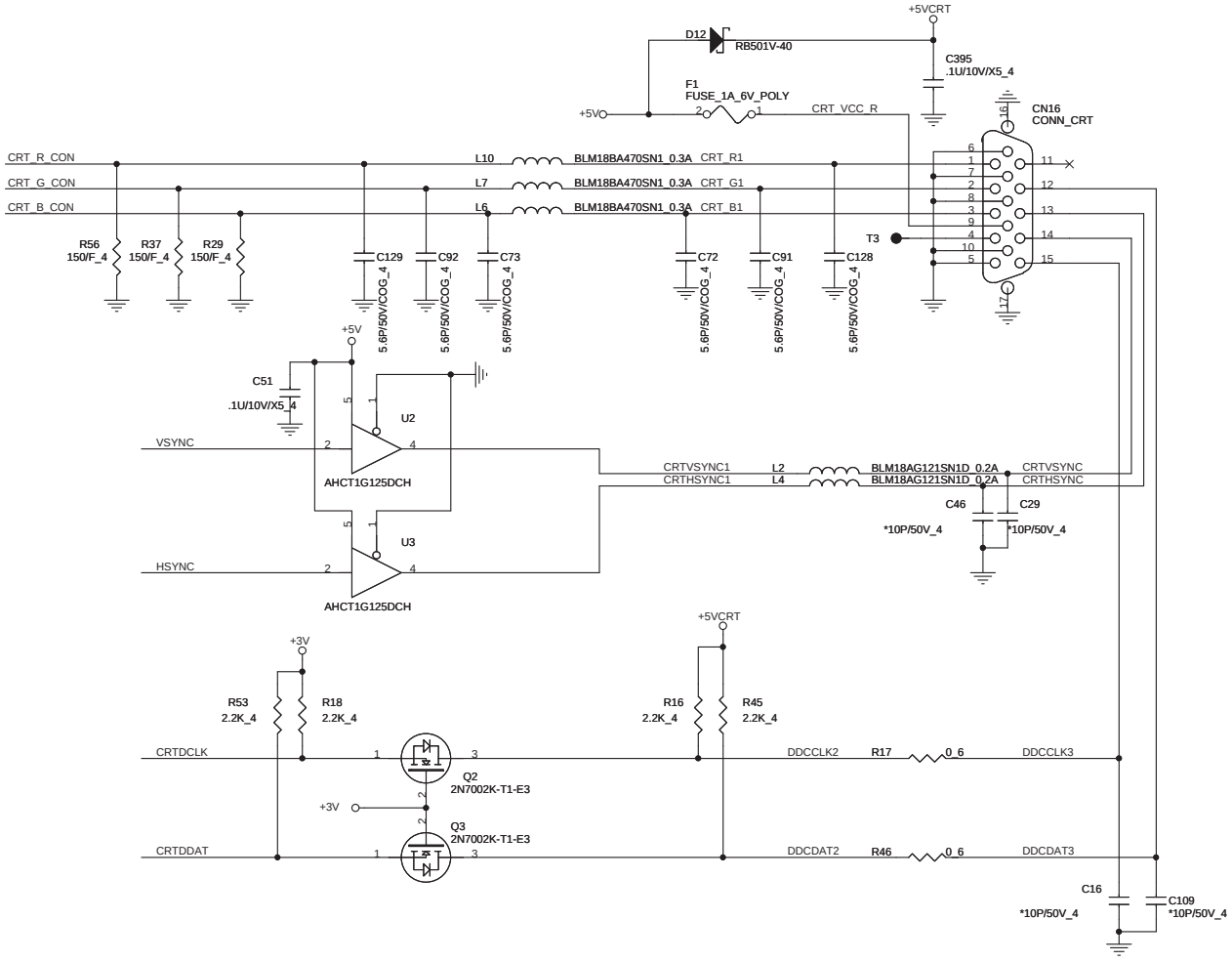
CRT PORT

[15,19,20,22,24,25,26,27,28] +5V
[2,4,6,9,10,11,12,13,14,15,17,18,19,22,23,24,25,26,27,28,29,30,31,32] +3V

[6] CRT_R_CON → CRT_R_CON
[6] CRT_G_CON → CRT_G_CON
[6] CRT_B_CON → CRT_B_CON
[6] HSYNC → HSYNC
[6] VSYNC → VSYNC
[6] CRTDCLK → CRTDCLK
[6] CRTDDAT → CRTDDAT

del VGA CRT
Mika 2008/04/10



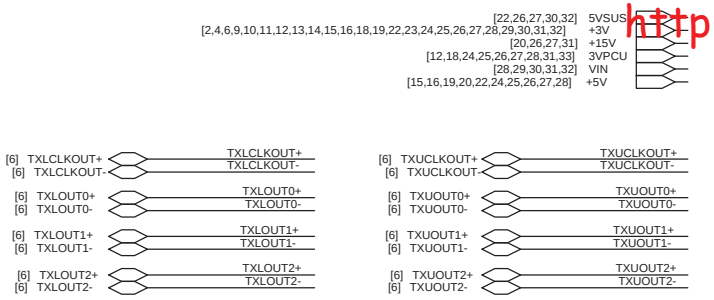


PROJECT : EF7
Quanta Computer Inc.

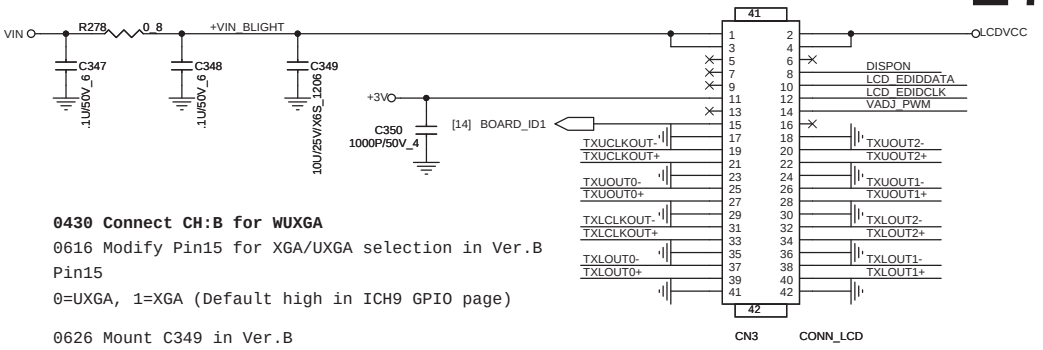
Size	Document Number	Rev
Custom	Conn-CRT	1A

Date: Tuesday, July 01, 2008 Sheet 16 of 34

LVDS



del VGA LVDS
Mika 2008/04/10

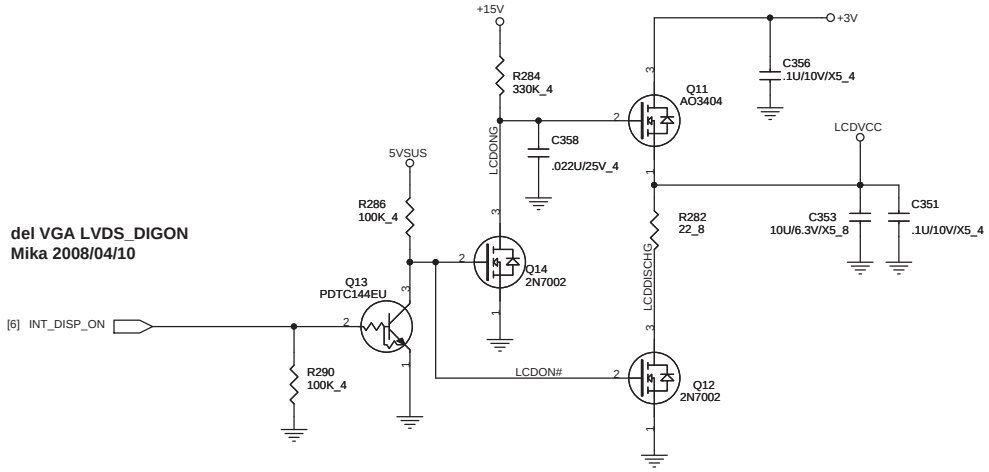


0430 Connect CH:B for WUXGA

0616 Modify Pin15 for XGA/UXGA selection in Ver.B
Pin15
0=UXGA, 1=XGA (Default high in ICH9 GPIO page)

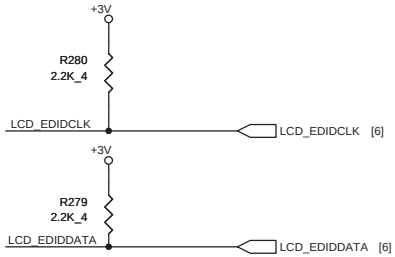
0626 Mount C349 in Ver.B

PANEL VCC CONTROL

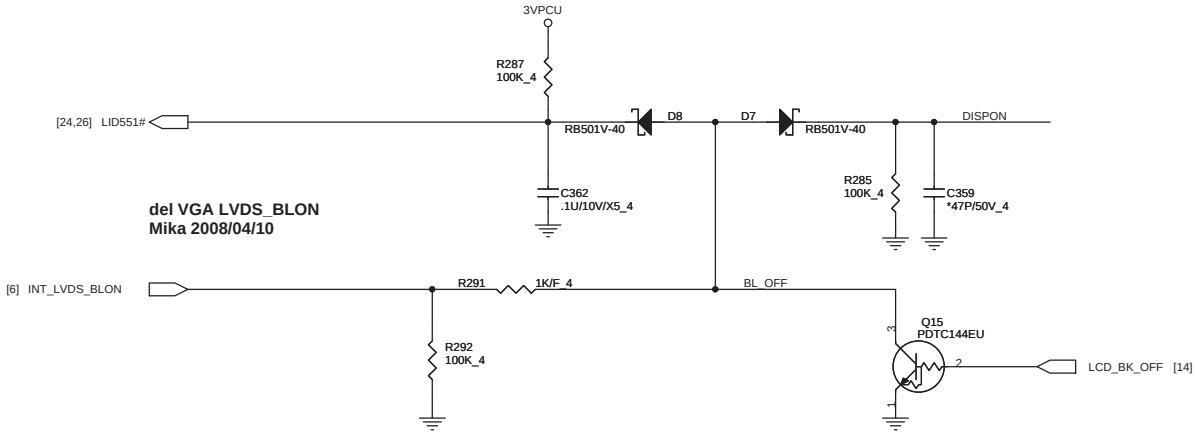


del VGA LVDS_DIGON
Mika 2008/04/10

del VGA EDID I2C
Mika 2008/04/10



Backlight Control

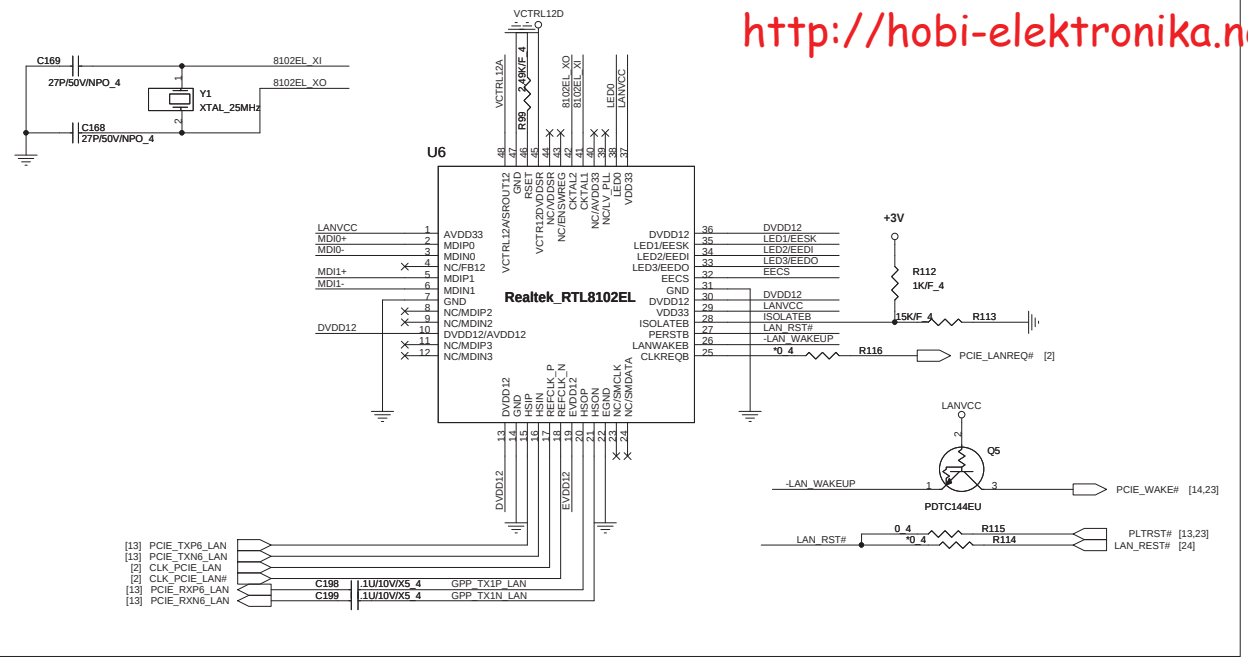


del VGA LVDS_BLON
Mika 2008/04/10

PROJECT : EF7
Quanta Computer Inc.

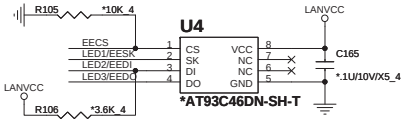
Size	Document Number	Rev
Custom	Conn-LCD & LID	2A

Date: Wednesday, July 02, 2008 Sheet 17 of 34



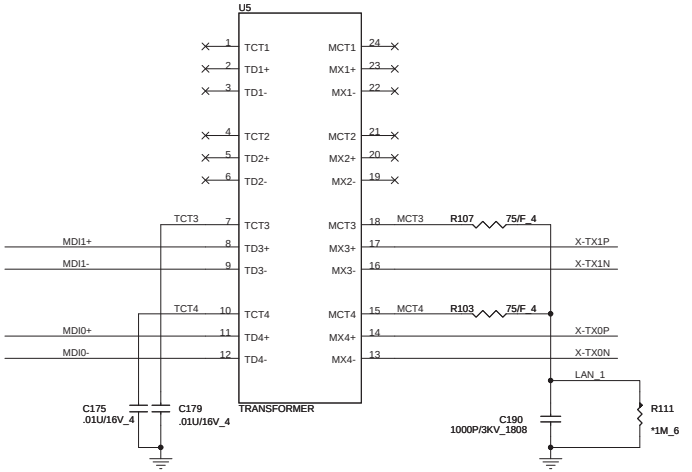
[27] LANVCC
[12,17,24,25,26,27,28,31,33] 3VPCU

EEPROM



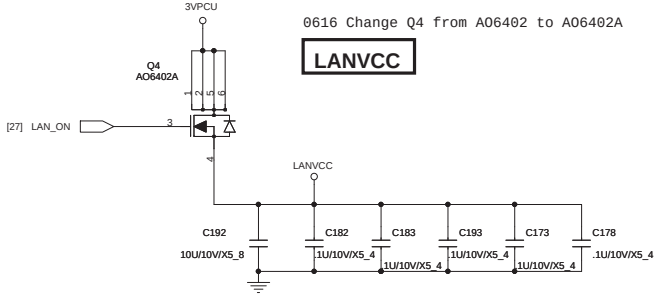
0616 Remove LAN EEPROM due to support on LAN chip in Ver.B

10/100 Transformer

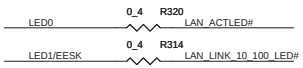


0616 Change Q4 from AO6402 to AO6402A

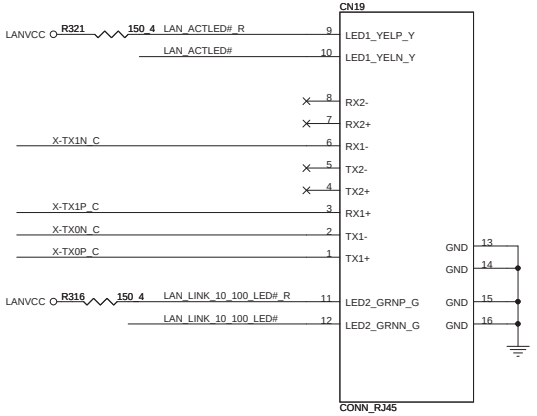
LANVCC



Check LED and EEPROM Mika

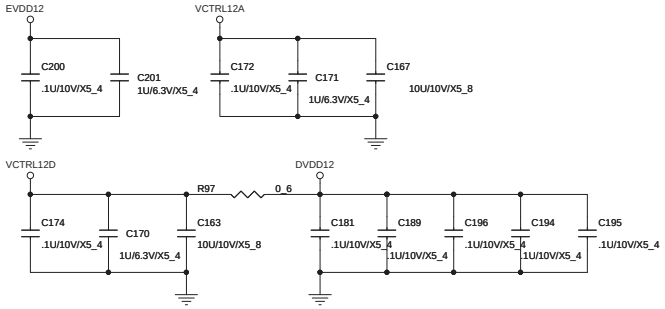


RJ45 Connector



For internal power used
Closed to pin19

For internal power used
Closed to pin48



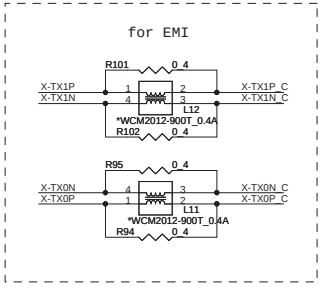
Closed to pin45

power source is from VCTRL12D

For RTL8102EL

VCTRL12A — EVDD12

DVDD12 — VCTRL12D

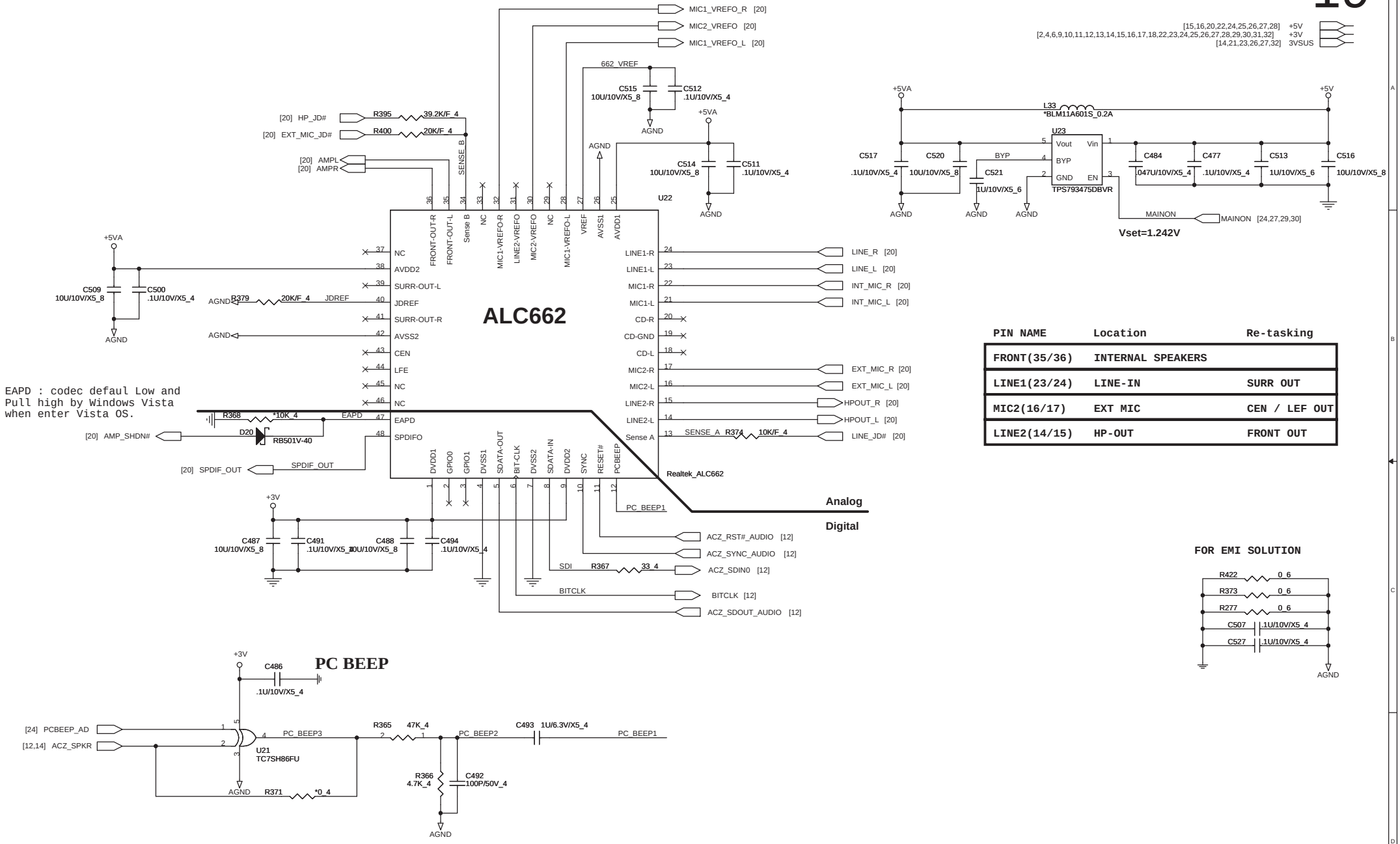


0519 SWAP signals.

PROJECT : EF7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN-Realtek RTL8102EL	2A

Date: Wednesday, July 02, 2008 Sheet 18 of 34



0627 Change U21 GND to AGND in Ver.B

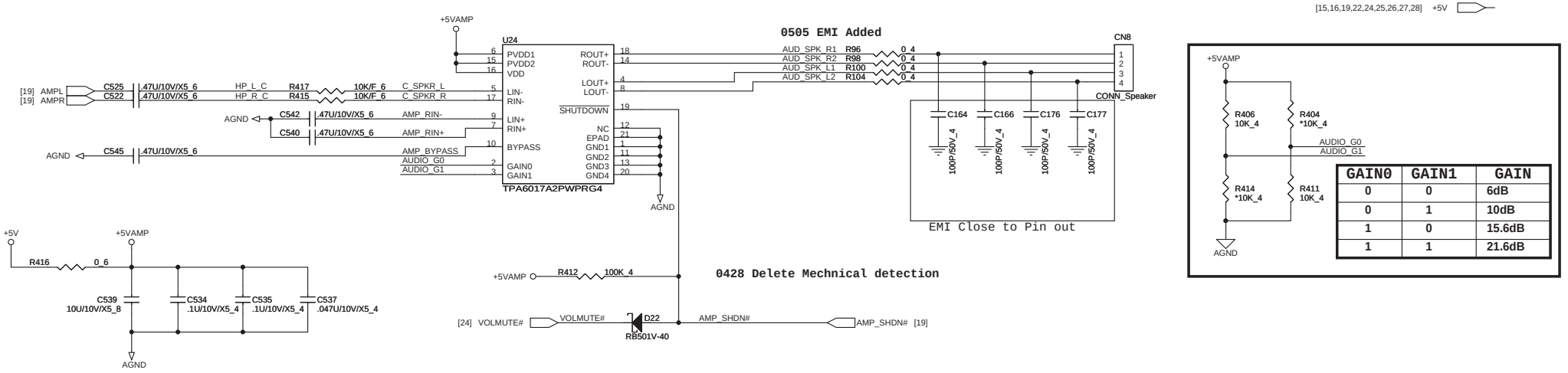
PIN NAME	Location	Re-tasking
FRONT(35/36)	INTERNAL SPEAKERS	
LINE1(23/24)	LINE-IN	SURR OUT
MIC2(16/17)	EXT MIC	CEN / LEF OUT
LINE2(14/15)	HP-OUT	FRONT OUT

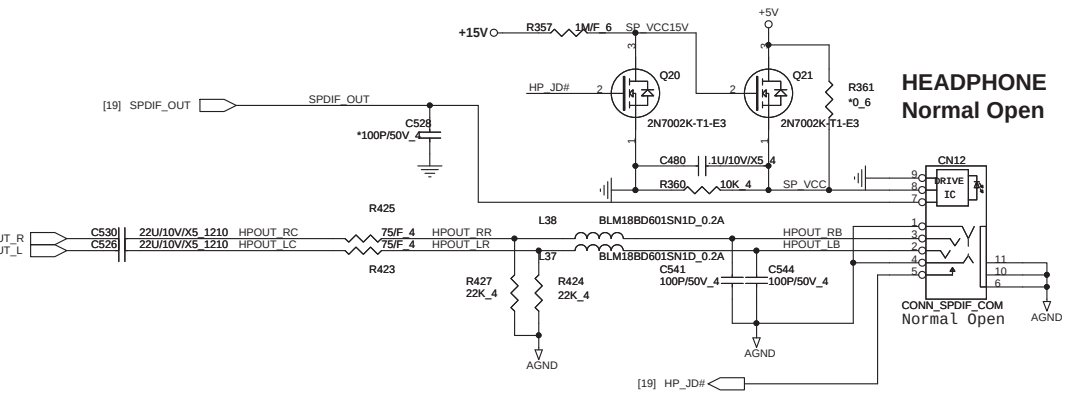
PROJECT : EF7
Quanta Computer Inc.

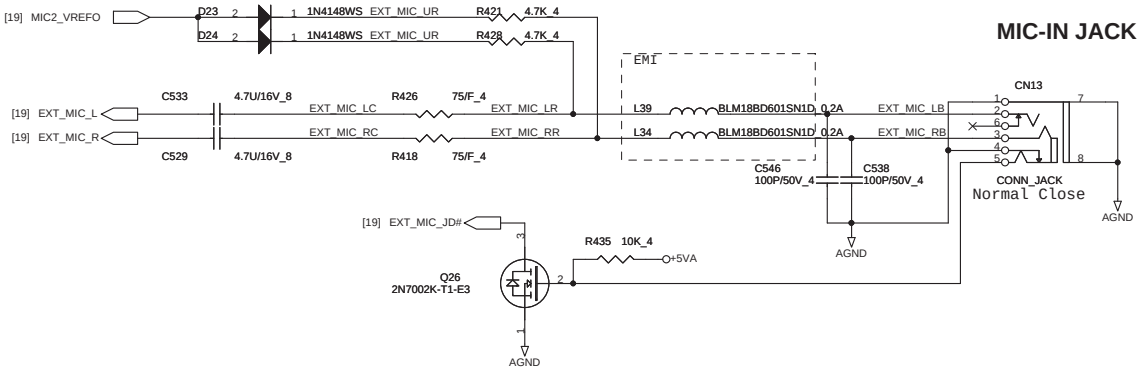
Size	Document Number	Rev
Custom	AUDIO-CODEC	2A

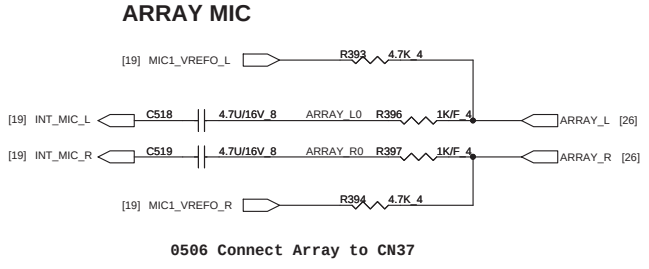
Date: Wednesday, July 02, 2008 Sheet 19 of 34

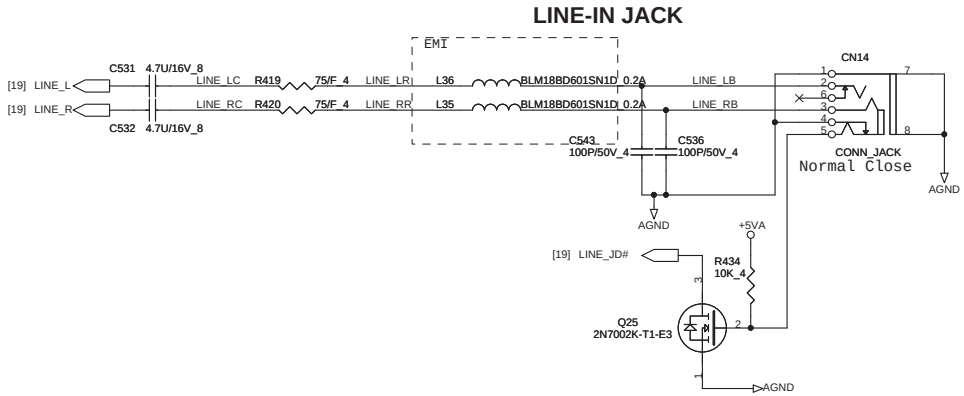
INTERNAL SPEAKER AMPLIFIER









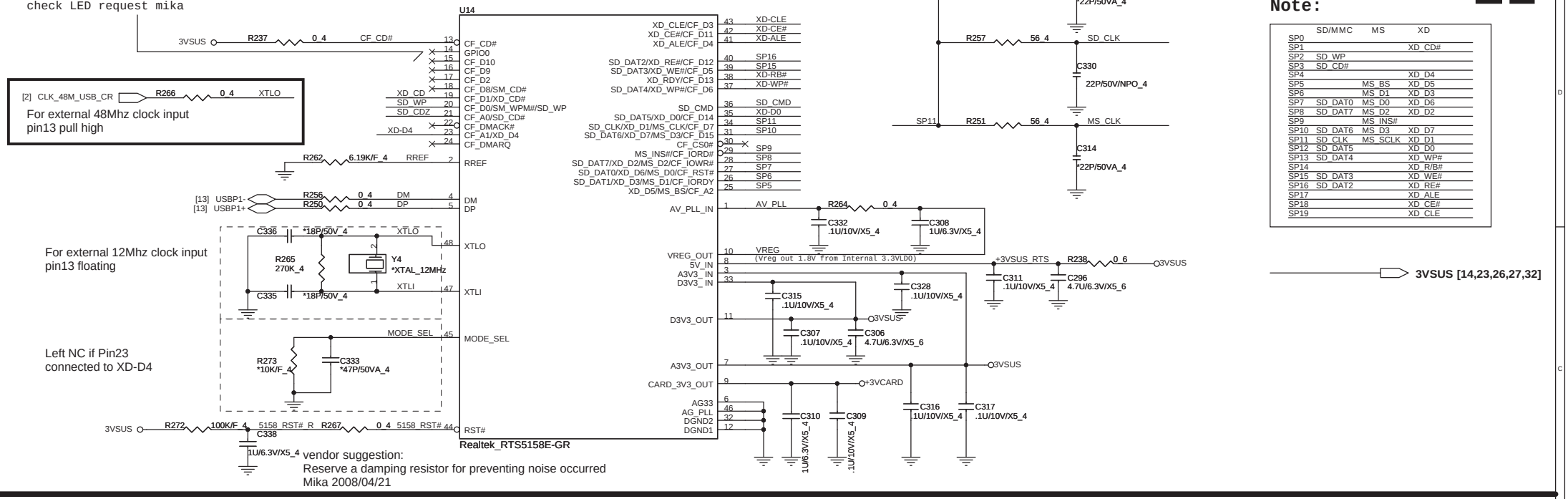


PROJECT : EF7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AUDIO-AMP&jacks	2A

Date: Tuesday, July 01, 2008 Sheet 20 of 34

Fix card reader led problem
check LED request mika



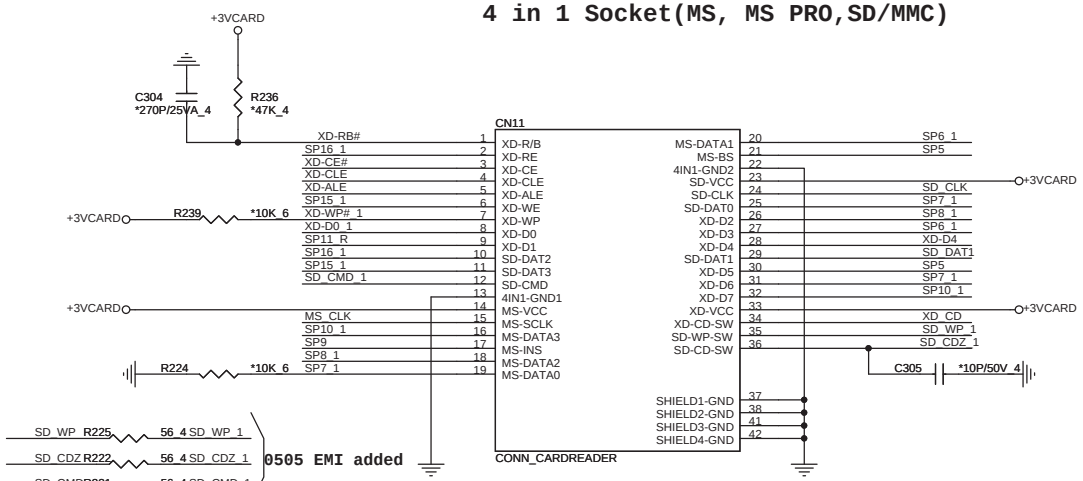
vendor suggestion:
Reserve a damping resistor for preventing noise occurred
Mika 2008/04/21

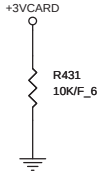
Note:

	SD/MMC	MS	XD
SP0			
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4			XD_D4
SP5		MS_BS	XD_D5
SP6		MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

3VSUS [14,23,26,27,32]

4 in 1 Socket(MS, MS PRO,SD/MMC)





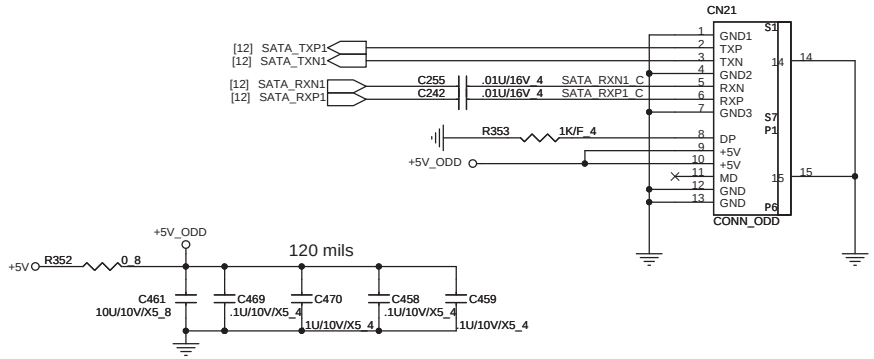
0616 Add 10K to GND for +3VCARD discharge in Ver.B

PROJECT : EF7
Quanta Computer Inc.

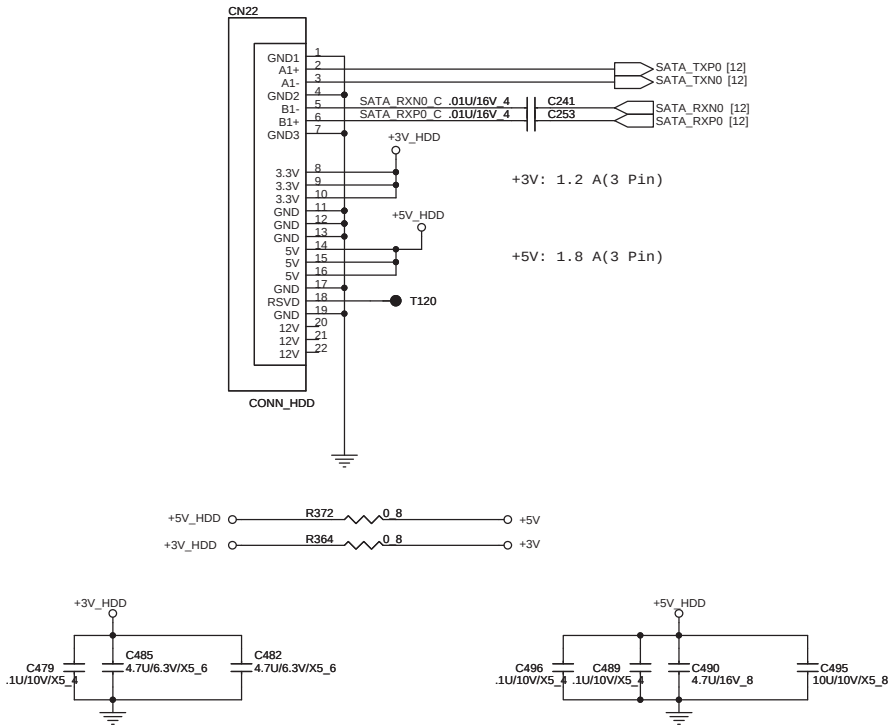
Size	Document Number	Rev
Custom	Card Reader-RTS5158E	2A

Date: Tuesday, July 01, 2008 Sheet 21 of 34

SATA CD-ROM

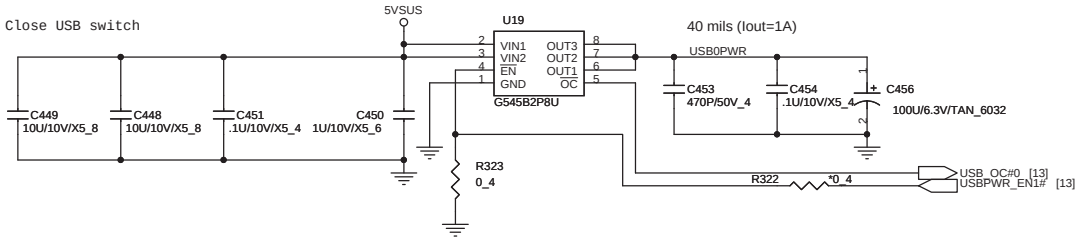


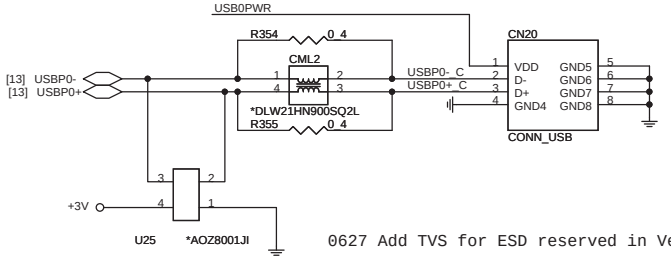
SATA-HDD CONNECTOR



USBX3

[17,26,27,30,32] 5VSUS
[15,16,19,20,24,25,26,27,28] +5V
[2,4,6,9,10,11,12,13,14,15,16,17,18,19,23,24,25,26,27,28,29,30,31,32] +3V

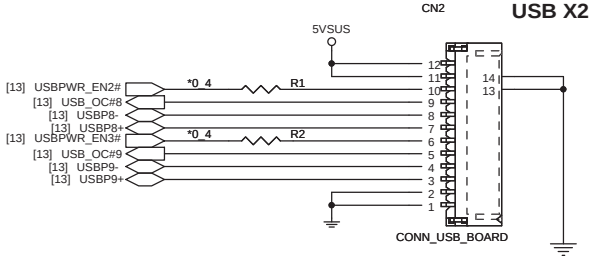


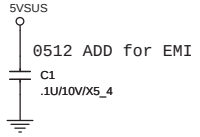


USB X1 at MB

0627 Add TVS for ESD reserved in Ver.B

USB X2 at Daughter Board



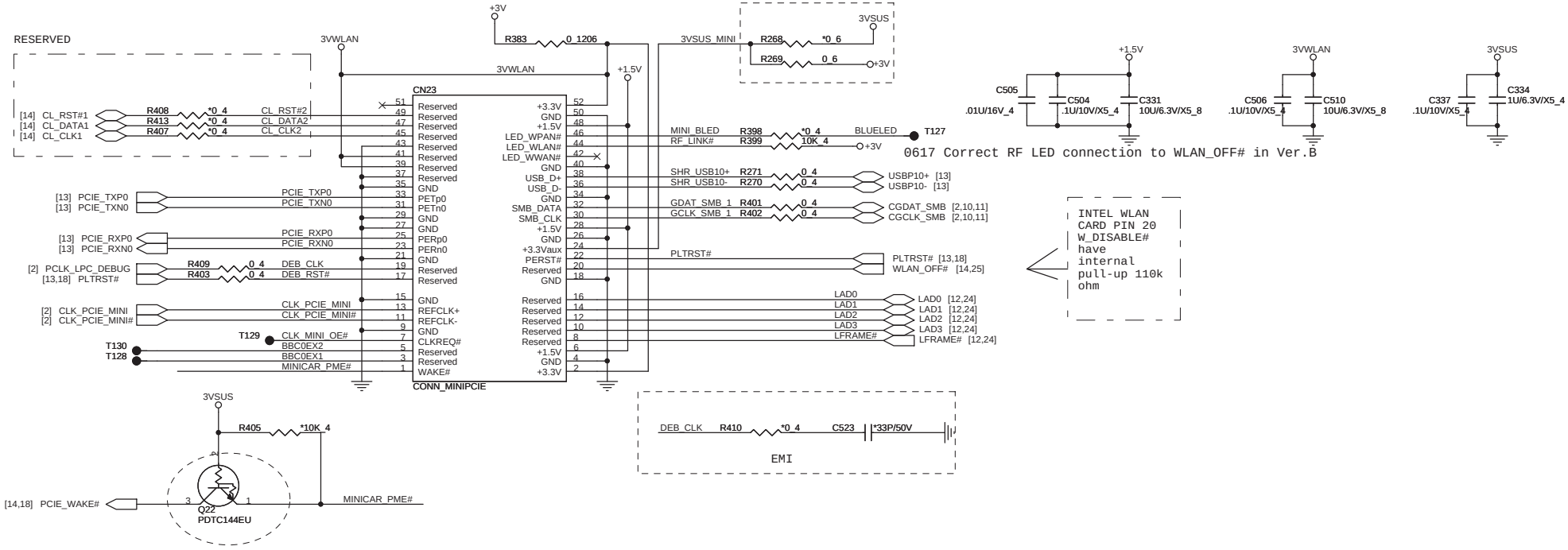


PROJECT : EF7
Quanta Computer Inc.

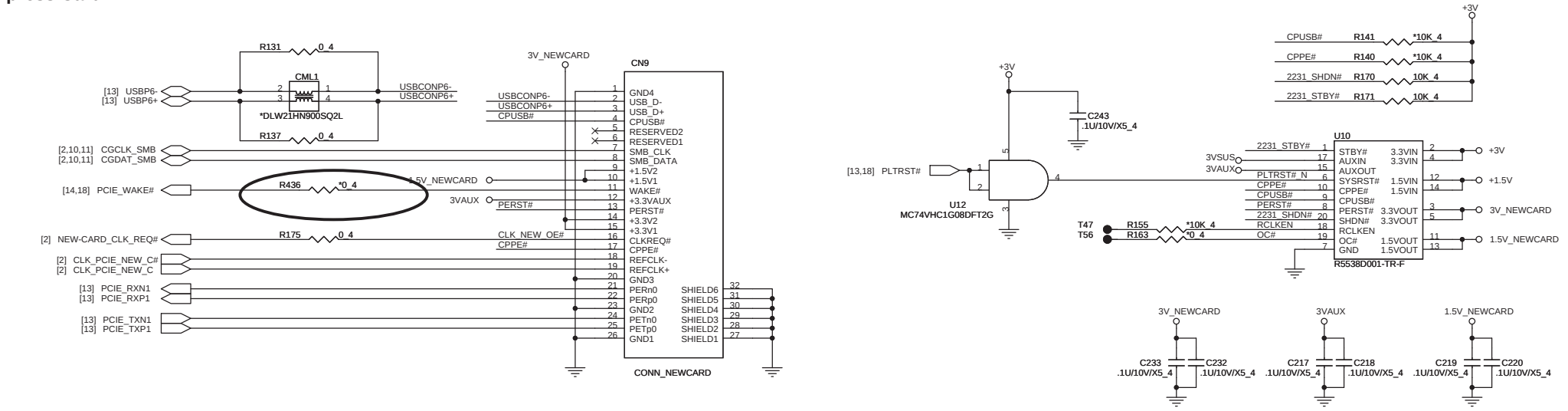
Size	Document Number	Rev
Custom	Conn-HDD/ODD/USB	2A
Date: Tuesday, July 01, 2008	Sheet 22 of 34	

Mini PCI-E Card 1
WLAN

[14,21,26,27,32] 3VSUS
[4,9,12,13,15,26,27,30] +1.5V
[2,4,6,9,10,11,12,13,14,15,16,17,18,19,22,24,25,26,27,28,29,30,31,32] +3V



Express Card



0627 Update Footprint in Ver.B
0702 Add R436 to Disconnect PCIE_WAKE# in Ver.B

PROJECT : EF7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Conn-Xpress Card	2A

Date: Thursday, July 03, 2008 Sheet 23 of 34

IT8502E

0616 Modify Pin83 for EF7/EF9 keyboard selection in Ver.B
0616 Mount R139 for EC_ACTIVE debug in Ver.B
0626 Correct MB_ID2EC netname in Ver.B

0516 Change ECACTIVE

0516 Change NBSWON control to Page33.

0428 Delete RF ON/OFF function

0505 Connect PCBEEP

0616 Reserve EC Pin81 in Ver.B

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

TMKBC Function	
High	Enable
Low	Disable

FLASH TYPE SELECT	
R?	
High	LPC/FWH FLASH ROM
Low	SPI FLASH ROM (Default)

IT8502IX / IT8502JX IT8512DX		
C723	0	0.1uF
C724	NC	1uF

For 8502JX

16MBit
FLASH_MX25L1605A

PROJECT : EF7
Quanta Computer Inc.

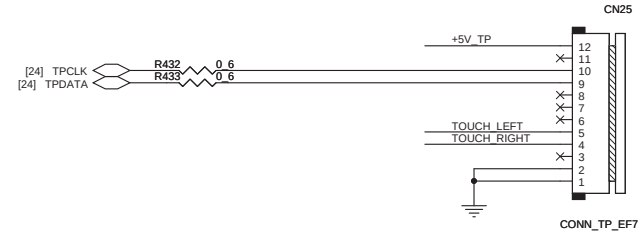
Size	Document Number	Rev
Custom	EC-KBC IT8502E	2A
Date: Wednesday, July 02, 2008	Sheet 24 of 34	

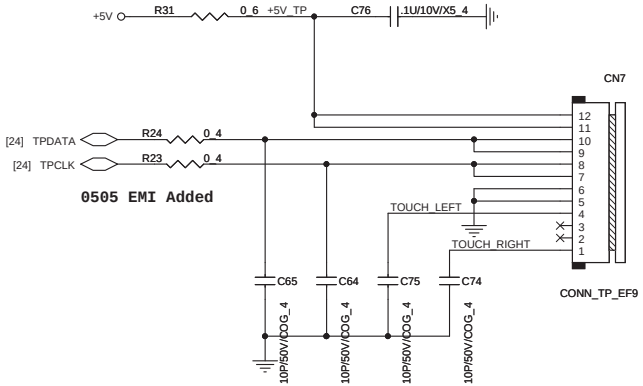
DUAL Layout for both 16" and 18.4"

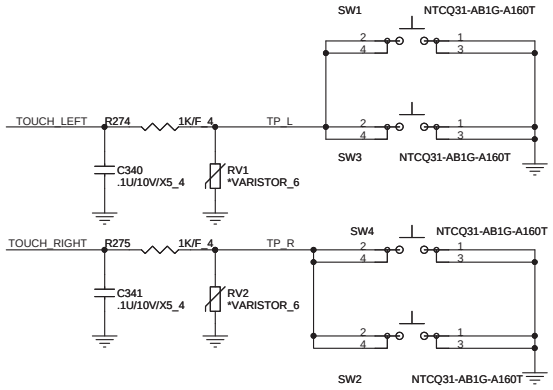
TOUCH PAD

[2,4,6,9,10,11,12,13,14,15,16,17,18,19,22,23,24,26,27,28,29,30,31,32] +3V
[15,16,19,20,22,24,26,27,28] +5V
[12,17,18,24,26,27,28,31,33] 3VPCU

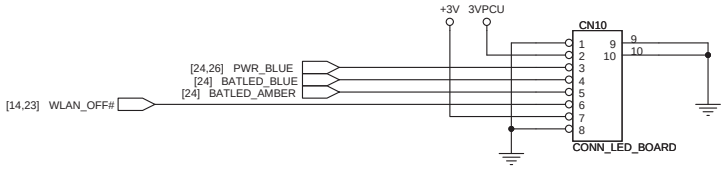
0617 Add one more touch PAD connector for EF7 different pin definition.
0625 Del C548/C549, Change R432/R433 to 0603 in Ver.B







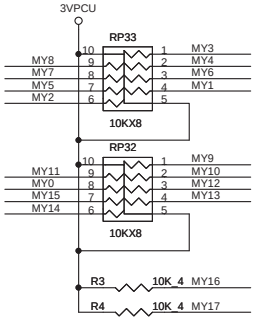
LED Board

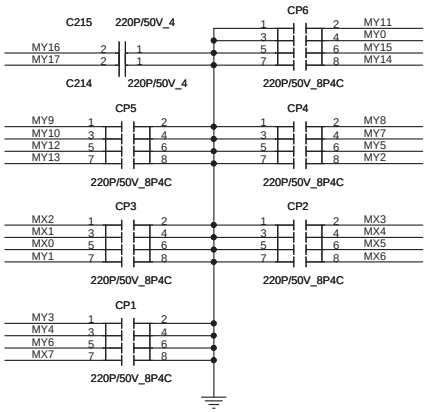


0617 Correct RF LED connection to WLAN_OFF# in Ver.B

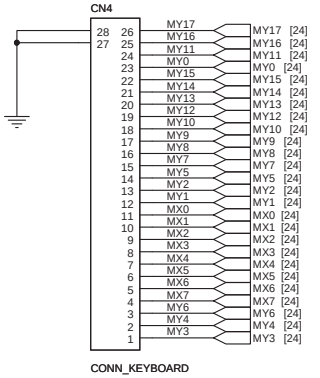
DUAL Layout for both 16" and 18.4"

KEYBOARD





0625 Delete CN1 in Ver.B



0514 Change CP6 to 2 0402 Capacitor
0514 Swap nets.

PROJECT : EF7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Conn-KB/TB/LEDs	2A

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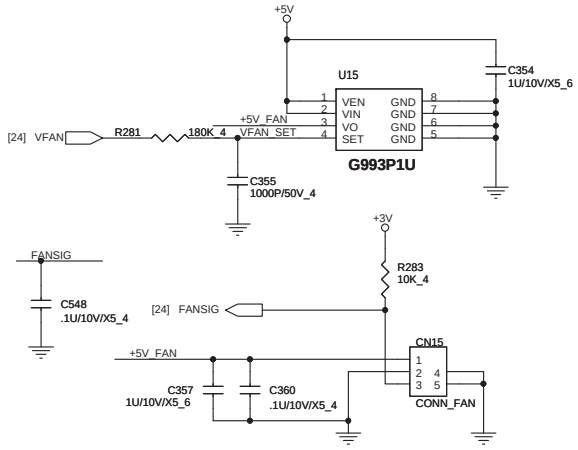
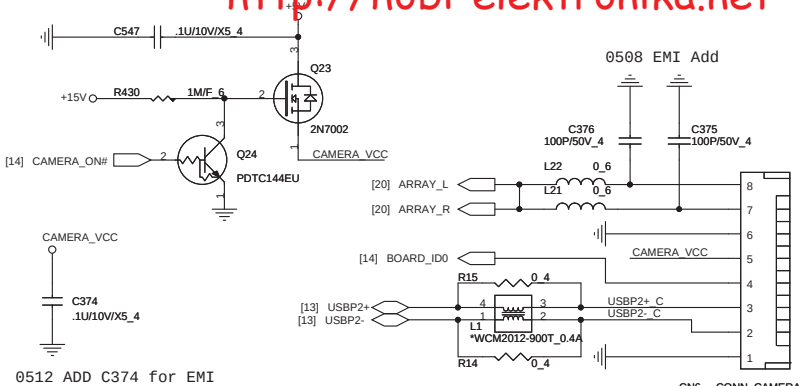
FAN CONTROL



0626 Add C548 for EMI in Ver.B

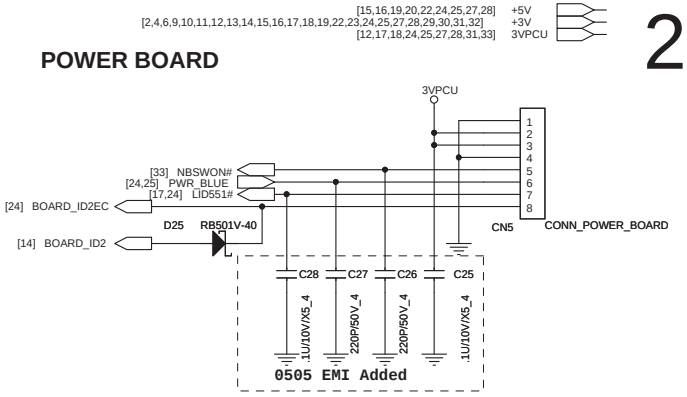
CAMERA Wire to Board



0512 ADD C374 for EMI
0519 SWAP USB signals for layout routing.
0616 Modify Pin4 for Camera HW detection in Ver.B
0616 Add Switch for Camera power control in Ver.B
0616 Modify inner MIC to MONO in Ver.B

Pin4
0= Camera present
1= Camera absent
(Default high)

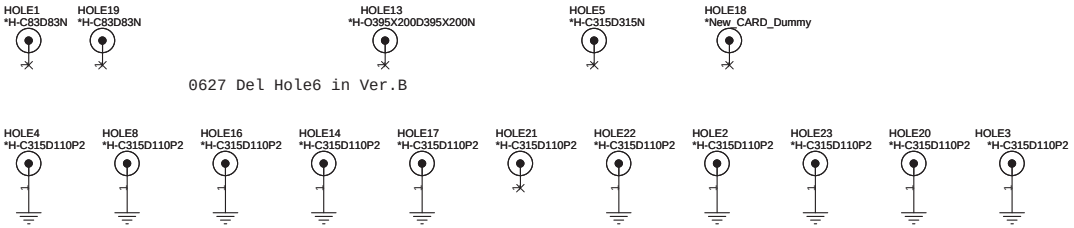
POWER BOARD



0616 Swap Pin1~Pin8 for Cable Assemble issue in Ver.B
0616 Modify Pin8 for EF7/EF9 selection in Ver.B
0626 Change C28 from 220P to 0.1U in Ver.B
0626 Add D25 for EC/ICH leakage in Ver.B

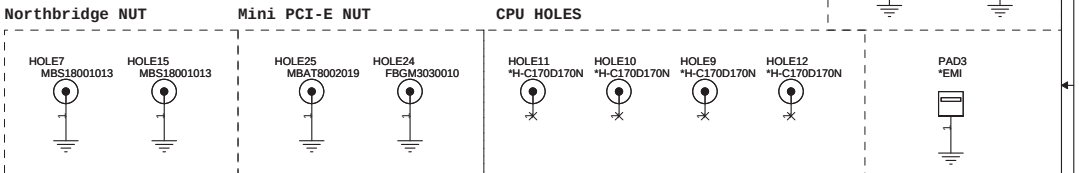
Pin8
0= EF7
1= EF9 <default>

HOLES and EMI PADS

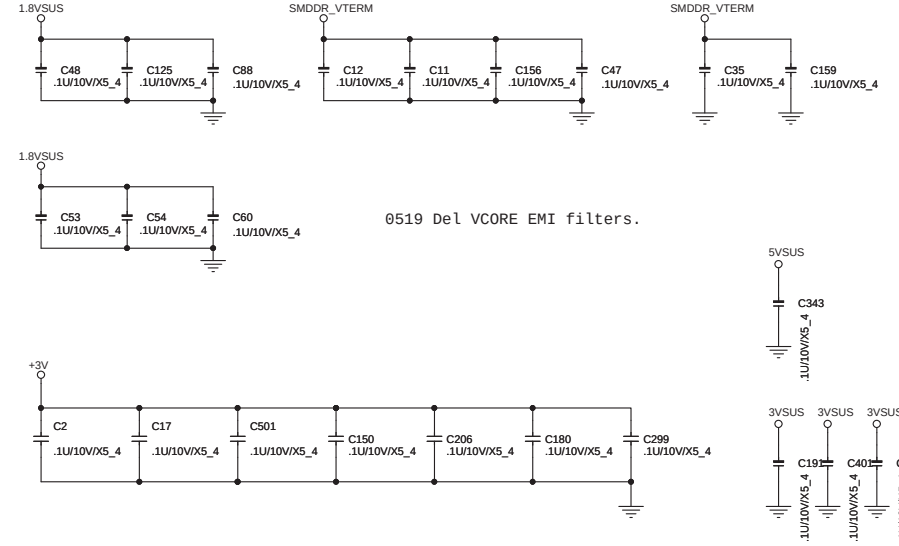


0627 Del Hole6 in Ver.B

0626 Reserve EMI PAD in Ver.B
0627 Modify Hole24 footprint in Ver.B **Thermal Module EMI spring**
0701 Add PAD3 for EMI in Ver.B

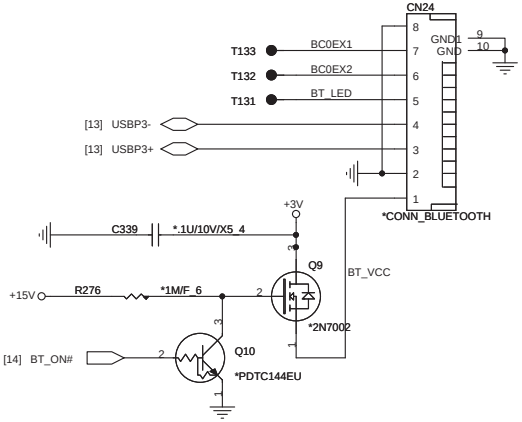


EMI reserved



0519 Del VCORE EMI filters.

BLUETOOTH



0616 Reserve Bluetooth function in Ver.B

PROJECT : EF7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Conn-BtoB/Fan/Holes/BT	2A

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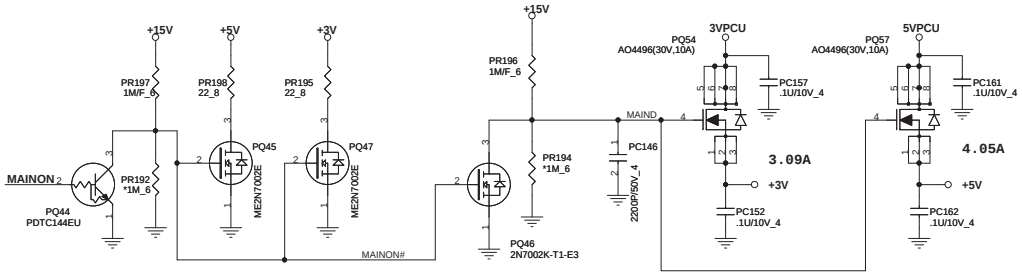
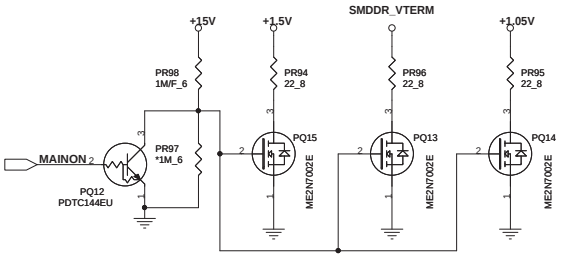
DISCHARGE

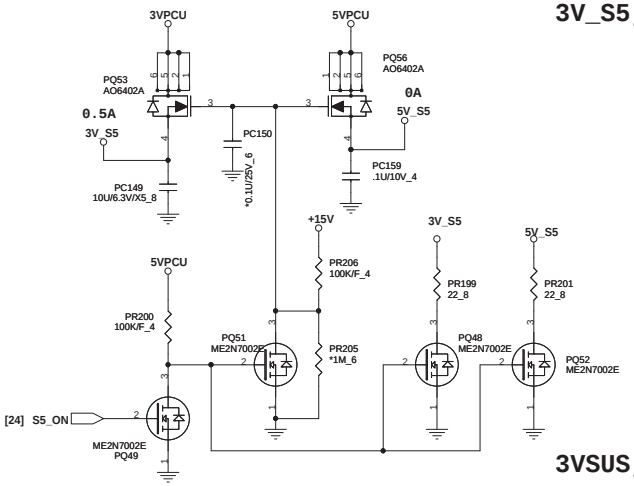


+3V, +5V

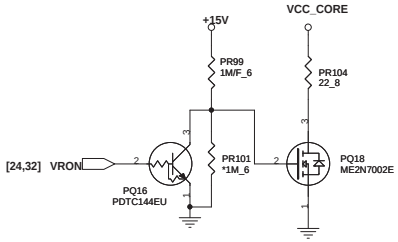
+1.5V, +1.05V



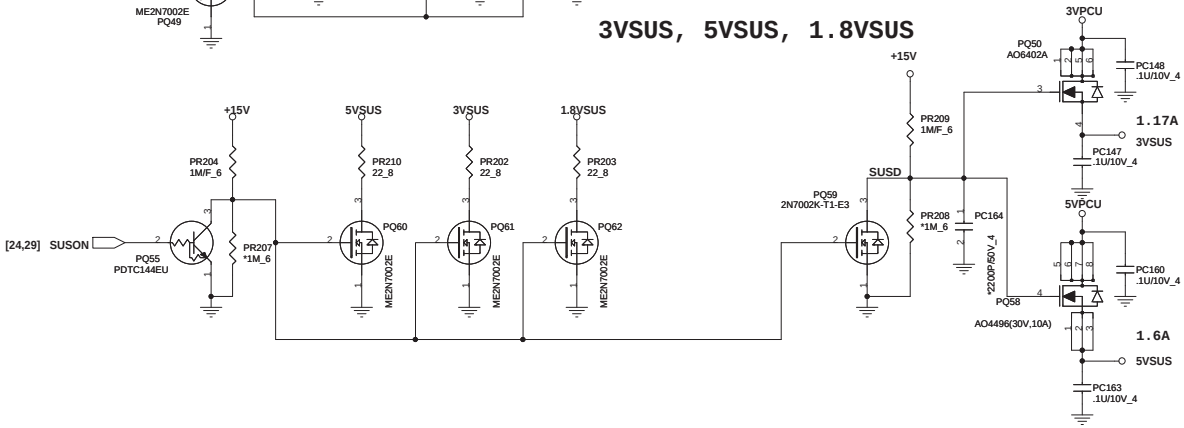
3V_S5, 5V_S5



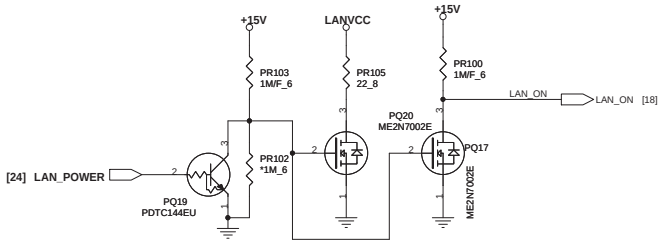
VCC_CORE



3VSUS, 5VSUS, 1.8VSUS



LANVCC



PROJECT : EF7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Power-Discharge	1A

Date: Wednesday, July 02, 2008 Sheet 27 of 34

R138=0.02m ohm for 65W adapter-->current limit is 3A;
R138=0.015m ohm for 90W adapter-->current limit is 4A;

0624 Change Charger circuit in Ver.B
0625 Remove PC72 connect from Vin1to Vin in Ver.B

0623 Mount PC82,PR133,PD16,PQ26 in Ver.B

AD overload throtling
65W Adapter: 0.4V/A
90W Adapter: 0.3V/A

Charge Currect=3A, SET 1.05V

0515 Change

0519 Modify

0623 Change PC73 material in Ver.B

0626 Add PR214 as Power debug function in Ver.B

CELL-SET=High-->4.2V/4S
CELL-SET=Low-->4.2V/3S

0515 Change

0623 Mount PD15,PQ24 in Ver.B

0516 Change

0623 Delete PD1 in Ver.B
0623 Change PD2 material in Ver.B

VOUT = (GAIN) (RSENSE)(ILOAD)

500mV/A for Batt I
dicharge sensing

To detect AD drop voltage 8 times -> Battery discharge

0513 Change from 100 to 100K

4 cell overload throtling

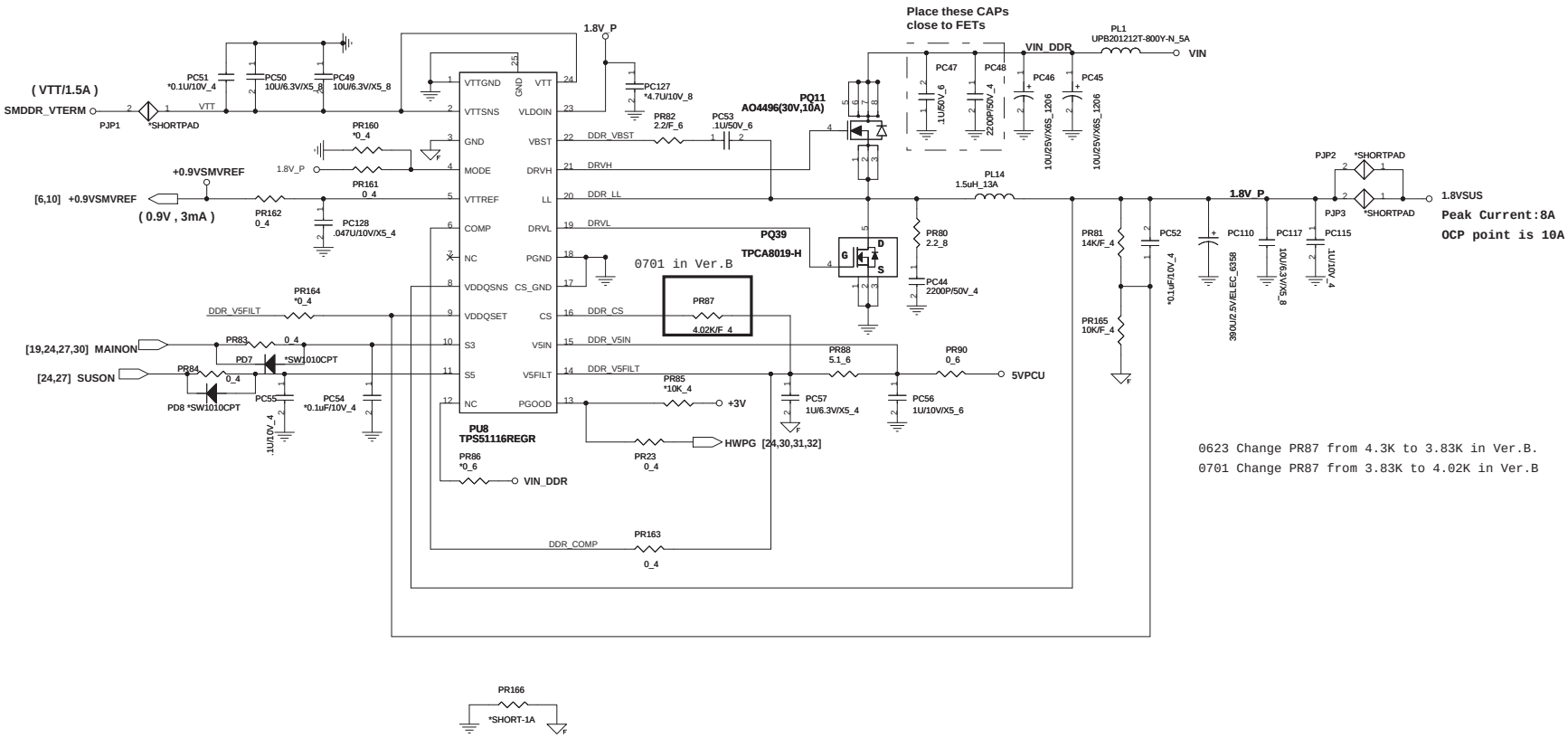
0515 Add for EMI
0616 Change Vin Filter to rating 50V, Size 0603 in Ver.B

Close to EC

0515 Modified for S5 Off

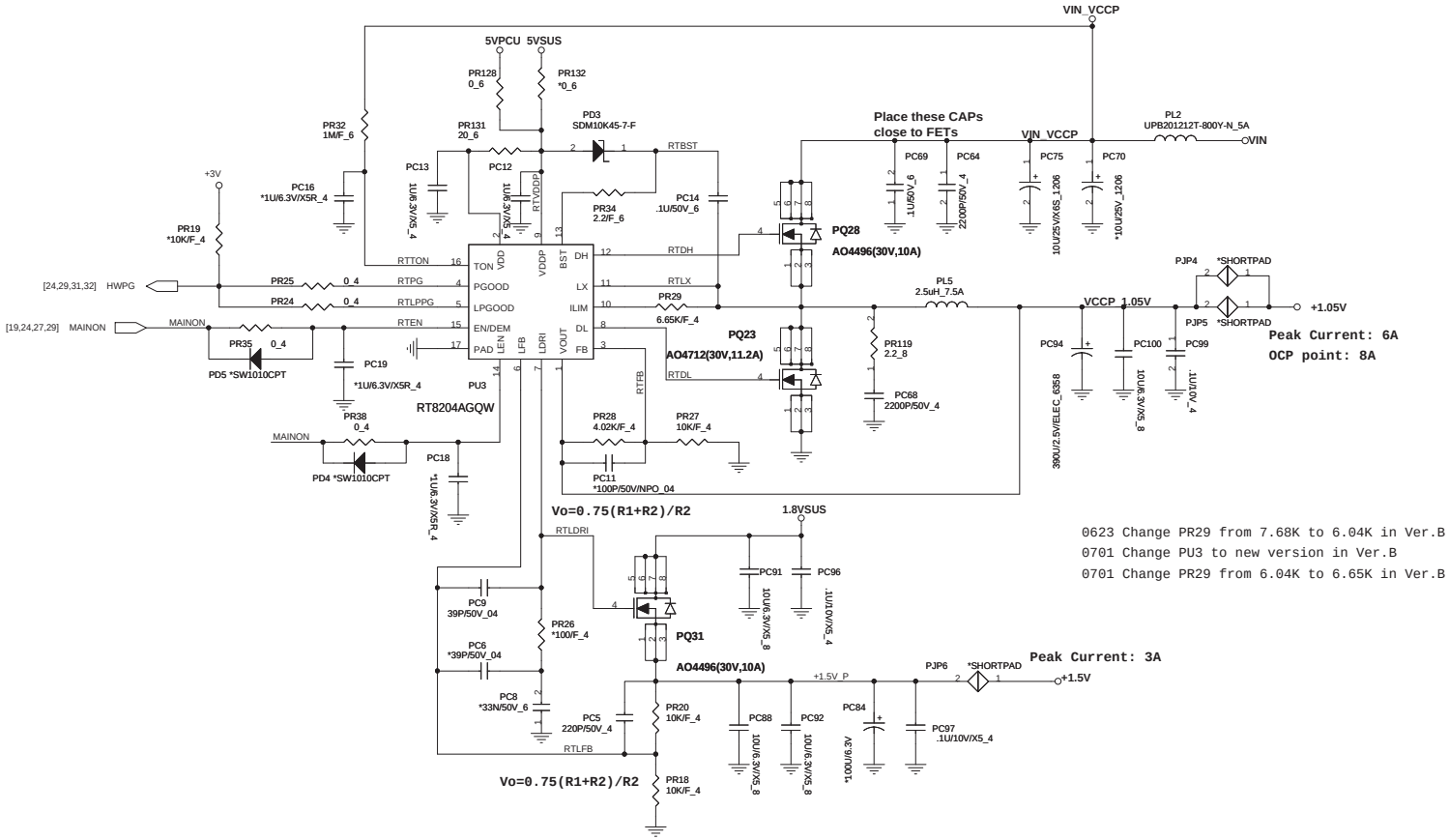
0617 change Battery connector to H8.2 in Ver.B
0623 Change PQ25 material in Ver.B

PROJECT : EF7
Quanta Computer Inc.
Size: Custom | Document Number: Power-Charger (MAX17005) | Rev: 2A
Date: Wednesday, July 02, 2008 | Sheet 28 of 34



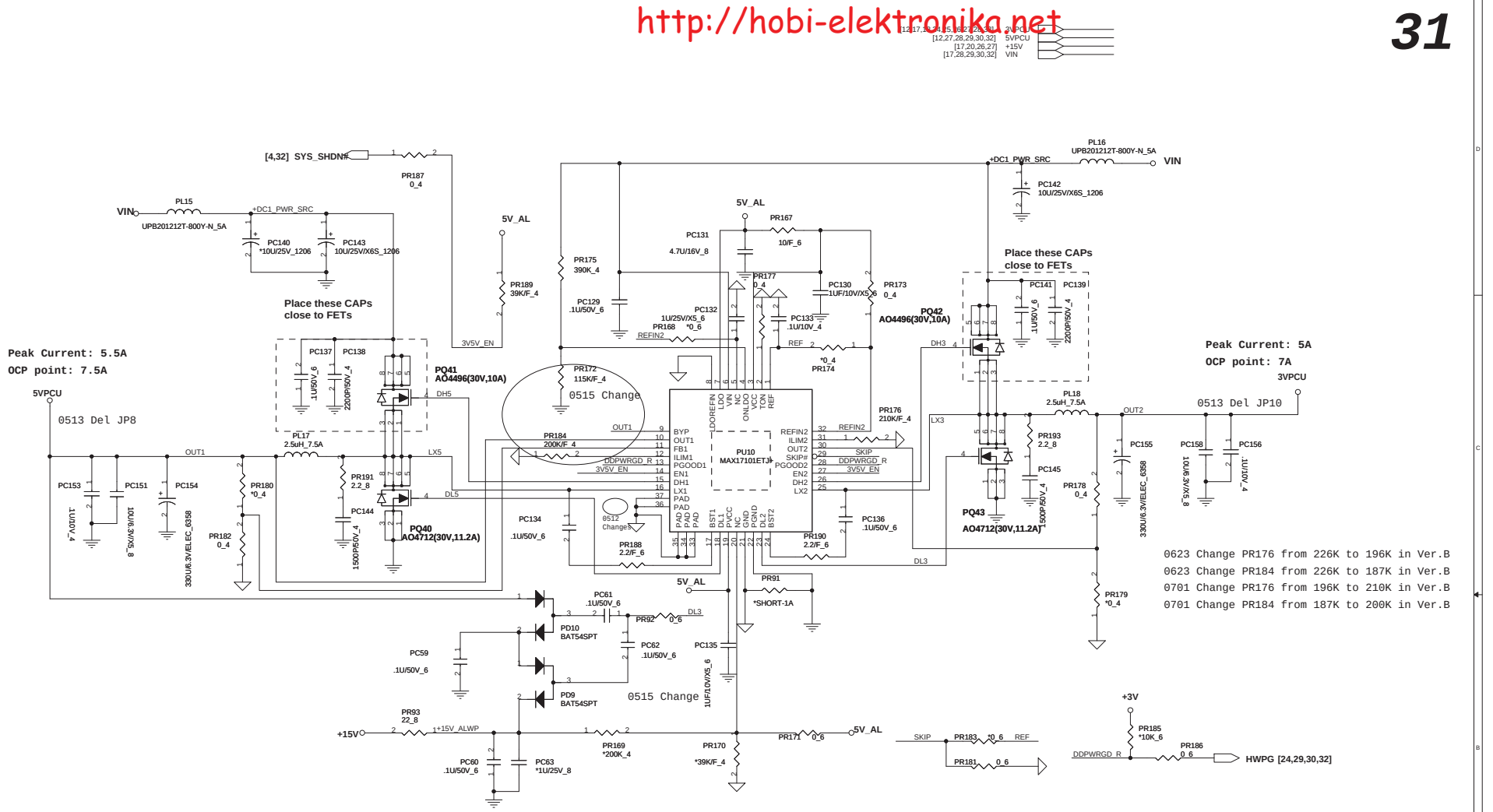
0623 Change PR87 from 4.3K to 3.83K in Ver.B.
0701 Change PR87 from 3.83K to 4.02K in Ver.B

PROJECT : EF7		
Quanta Computer Inc.		
Size: Custom	Document Number: Power-DDR2 (TPS51116REGR)	Rev: 2A
Date: Wednesday, July 02, 2008	Sheet 29 of 34	

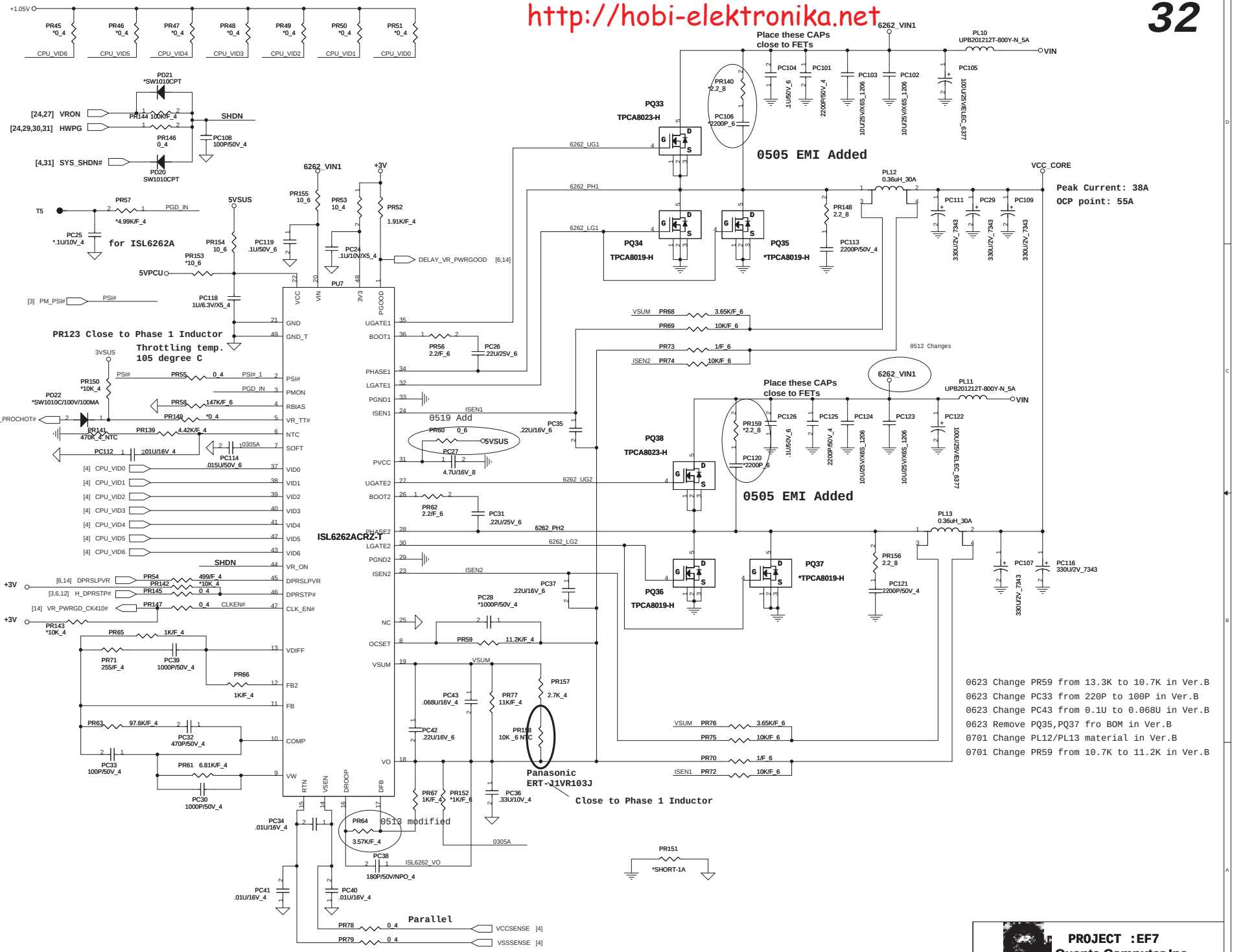


0623 Change PR29 from 7.68K to 6.04K in Ver.B
0701 Change PU3 to new version in Ver.B
0701 Change PR29 from 6.04K to 6.65K in Ver.B

PROJECT : EF7			
Quanta Computer Inc.			
Size: Custom	Document Number: Power-1.05V/1.5V (RT8204)		Rev: 2A
Date: Wednesday, July 02, 2008	Sheet 30 of 34		



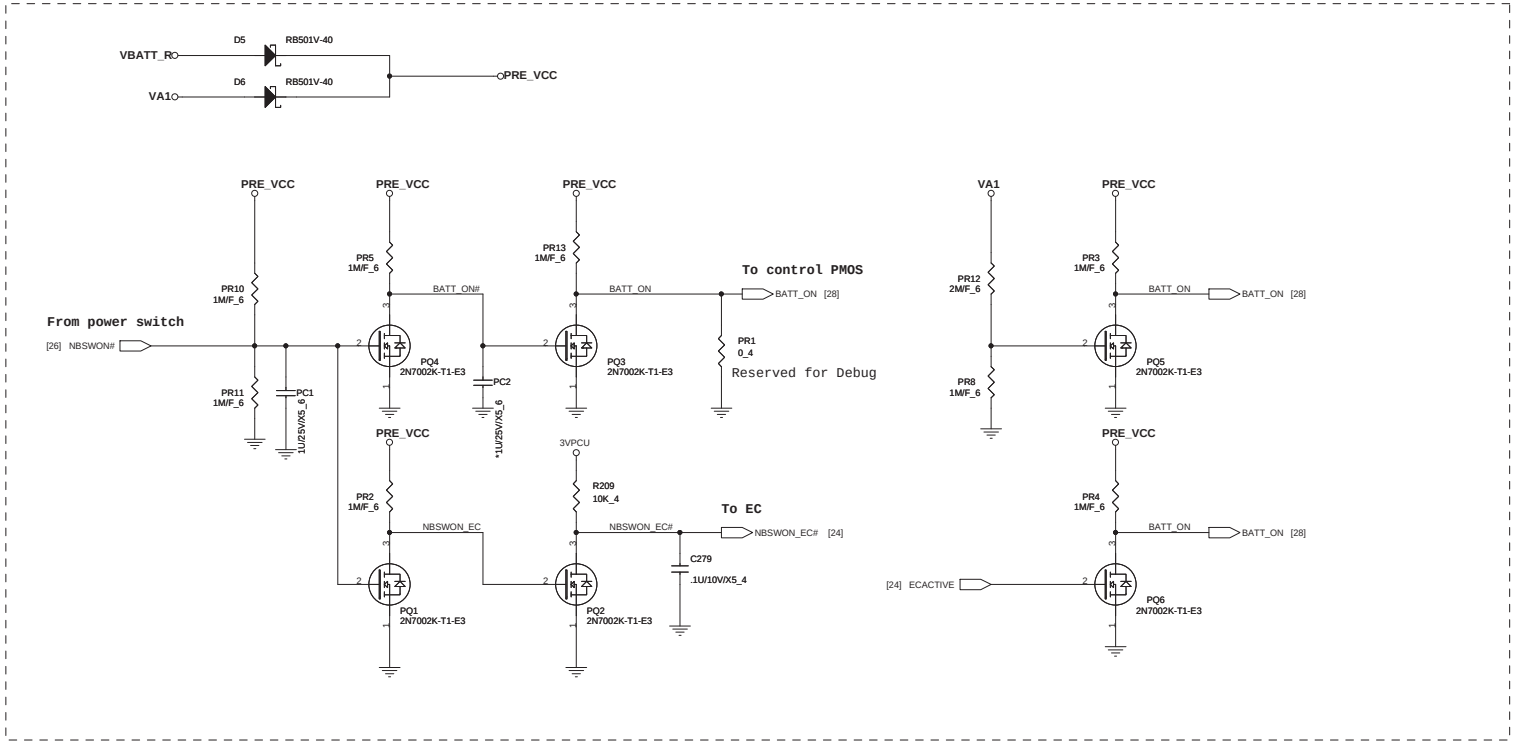
PROJECT : EF7		
Quanta Computer Inc.		
Size: Custom	Document Number: Power-3V/5V (MAX17101)	Rev: 2A
Date: Wednesday, July 02, 2008	Sheet 31 of 34	

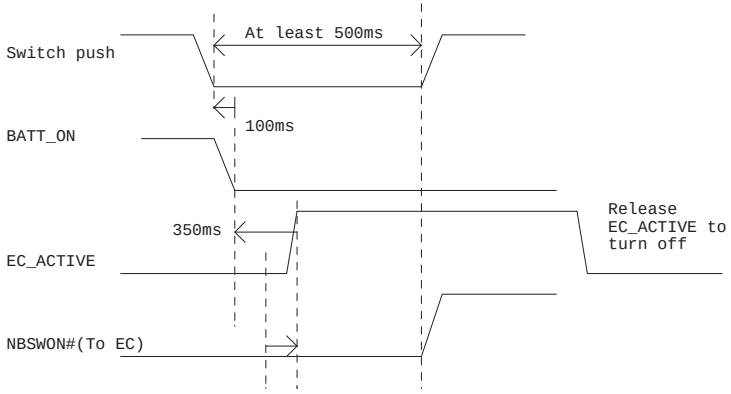


0623 Change PR59 from 13.3K to 10.7K in Ver.B
0623 Change PC33 from 220P to 100P in Ver.B
0623 Change PC43 from 0.1U to 0.068U in Ver.B
0623 Remove PQ35,PQ37 fro BOM in Ver.B
0701 Change PL12/PL13 material in Ver.B
0701 Change PR59 from 10.7K to 11.2K in Ver.B

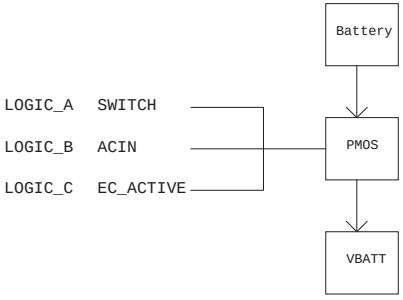
PROJECT : EF7 Quanta Computer Inc.		
Size: Custom	Document Number: Power-CPU (ISL6262A)	Rev: 2A
Date: Tuesday, July 01, 2008	Sheet 32 of 34	

0616 Remove PC2, Mount PC1 for S5-off circuit fine tune in Ver.B
0625 Mount PR1 to disable S5_off function in Ver.B





NBSWON# to trigger EC and apply EC_ACTIVE to high.



PROJECT : EF7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Power-S5 Off circuit	2A
Date: Tuesday, July 01, 2008	Sheet 33 of 34	

MODEL:	REV	CHANGE LIST
EF7 MB	1A	FIRST RELEASE
	2A	P14: (1) Define MB ID for "LCD/ Camera/ Keyboard" selection. (2) Connect ICH9 GPIO38 to Camera power ON/OFF control. (3) Set Board ID2 default High to prevent leakage. P17: (1) Modify CN3(LCD conn.) Pin15 for XGA/UXGA selection. (2) Mount C349 for EMI. P18: (1) Change Q4(Lan power switch) from AO6402 to AO6402A(BOM). (2) Remove extension EEPROM due to support in Lan Chip. P19: (1) Change U20 GND to AGND for Speaker noise issue. P20: (1) Add reverse circuit for MIC/Line in Jack sense.High for plug-in, Low for unplug. P21: (1) Add 10K to GND for +3VCARD to improve discharge path. P22: (1) Add TVS in USB trace for ESD reserved. P23: (1) Correct RF LED connection to WLAN_OFF# (2) Change New Card Footprint. (3) Add R436 to Delete PCIE_WAKE# for New Card due to we didn't support in suspend. P24: (1) Connect EC Pin83 for EF7/EF9 keyboard selection. (2) Reserve EC Pin81 for no use. (3) Mount R139 for S5_off EC_ACTIVE. (4) Correct MB_ID2 netname to MB_ID2EC. P25: (1) Correct RF LED connection to WLAN_OFF# (2) Add one more touch PAD connector for EF7 different pin definition. (3) Delete one Keyboard connector(CN1). P26: (1) Modify CN6(Camera conn.) Pin4 for Camera HW detection. (2) Swap CN5(power switch board) Pin definition for Cable Assemble issue. (3) Modify CN5 Pin8 for EF7/EF9 Keyboard selection. (4) Add Switch for Camera Power control. (5) Reserve BlueTooth function. (6) Modify inner MIC to Nomo in. (7) Change C28 From 220P to 0.1U for EMI. (8) Add C548 for EMI. (9) Reserve PAD1/PAD2 for EMI. (10) Add D25 for BOARD ID2 to prevent 3VPCU/+3V leakage. (11) Modify Hole24 footprint, Del Hole6. (12) Add PAD3 for EMI. POWER PAGES P28: (1) Change Vin EMI filter to .1U/50V/0603 Size...rating error. Charger (2) Change Battery connector to H8.2....ID issue. (3) Del PD1 to directly connect H_PROCHOT#.....reserve for 4Cell debug. (4) Change PD2 part number........fine tune rating. (5) Change PC73 part number.........fine tune rating. (6) Change PQ25 part number........fine tune rating. (7) Mount PC82,PR133,PD16,PQ26,PD15,PQ24,PR123,PR112......battery learning fine tune. (8) Change Charger PMOS circuit.....power fine tune. (9) Remove PC72 from Vin1 to Vin......power fine tune. (10) Add PR214 for Power debug. P29: (1)Change PR87 from 4.3K to 3.83K....OCP DDR (2) Delete JP1,JP5. and add short PAD....Reserved for power debug. (3) Change PR87 from 3.83K to 4.02K....OCP P30: (1) Change PR29 fro 7.68K to 6.04K.....OCP 1.05V (2) Delete JP3,JP4, and add short PAD.....Reserved for power debug. 1.5V (3) Change PU3 to new revision.....New revision. (4) Change PR29 from 6.04K to 6.65K.....OCP P31: (1) Change PR176 from 226K to 196K.....OCP 3V/5V (2) Change PR184 from 226K to 187K.....OCP (3) Change PR176 from 196K to 210K.....OCP (4) Change PR184 from 187K to 200K.....OCP P32: (1) Modify PC35/PC37/PC42 Part number to .22U/16V/X7 0603 size.....Correct BOM error. VCORE (2) Chanfe PR59 from 13.3K to 10.7K....OCP. (3) Change PC33 from 220P to 100P....power fine tune. (4) Change PC43 from 0.1U to 0.068U.....power fine tune. (5) Remove PQ35,PQ37 from BOM......Consider current rating VS thermal. (6) Change PL12/PL13 rating from 25A to 30A.....power fine tune. (7) Change PR59 from 10.7K to 11.2K.....OCP P33: (1) Remove PC2, Mount PC1 for Battery S5-off circuit fine tune. (2) Mount PR1 to disable S5_Off function.

MODEL / PAGE	EF7 MB FROM	TO
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	2A
15	1A	
16	1A	
17	1A	2A
18	1A	2A
19	1A	2A
20	1A	2A
21	1A	2A
22	1A	2A
23	1A	2A
24	1A	2A
25	1A	2A
26	1A	2A
27	1A	
28	1A	2A
29	1A	2A
30	1A	2A
31	1A	2A
32	1A	2A
33	1A	2A
34	1A	2A

Project : EF7 MB	MB Assy' P/N: 31EF7MB0000	Document No.: 204
Approved by : Vincent Wang	Drawing by :CHARLIE GU	DATE: 2008/6/13

PROJECT :EF7
Quanta Computer Inc.

Size	Document Number	Rev
C	A to B Changes	2A

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